THE DATASHEET OF

LM3646YFQR

LM3646 1.5-A Synchronous Boost Converter With Dual High-Side Current Sources and I²C-Compatible Interface

1 Features

- High-Side Current Sources Allowing for Grounded LED Cathode for Improved Thermal Management
- > 85% Efficiency in Torch and Flash Modes
- Small Solution Size < 20 mm²
- Accurate and Programmable Flash LED Current from 24 mA to 1.5 A in 11.7-mA Steps
- Accurate and Programmable Torch LED Current from 2.5 mA to 187 mA in 1.5-mA Steps
- Dual 1.5-A High-Side Current Sources for Dual LED Drive
- Hardware Flash and Torch Enables
- Hardware Enable Pin
- Soft-Start Operation for Battery Protection
- LED Thermal Sensing and Current Scale-Back
- Synchronization Input for RF Power Amplifier Pulse Events
- VIN Flash Monitor Optimization
- 1-MHz I²C-Compatible Interface
- I²C-Programmable NTC Trip Point
- 0.4-mm Pitch, 20-Bump DSBGA

2 Applications

Camera Phone LED Flash and Torch

3 Description

The LM3646 utilizes a 4-MHz fixed-frequency synchronous boost converter to provide power to dual 1.5-A constant current LED sources. The high-side current sources allow for grounded cathode LED operation providing flash current up to 1.5 A total. An adaptive headroom regulation scheme ensures the LED currents remain in regulation and maximizes efficiency. The combination of dual LED driving capability, high LED current, small solution size and high level of adjustability make the LM3646 perfect for camera phone LED flash and torch applications.

The LM3646 is controlled through an I²C-compatible interface. The main features of the LM3646 include: a hardware flash enable (STROBE) input for direct triggering of the flash pulse, a hardware Torch enable (TORCH) for movie mode or flashlight functions, a TX input which forces the flash pulse into a low-current torch mode allowing for synchronization to RF power amplifier events or other high-current conditions, an integrated comparator designed to monitor an NTC thermistor and provide an interrupt to the LED current, and a programmable input voltage monitor which monitors the battery voltage and can reduce the flash current during low battery conditions. A hardware enable (ENABLE) input provides a hardware shutdown during system software failures.

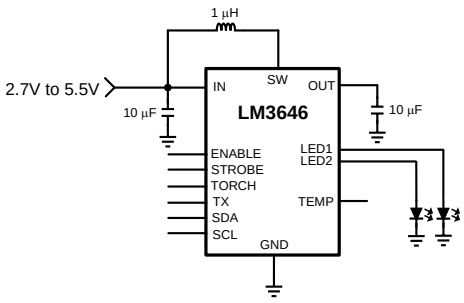
The 4-MHz switching frequency, overvoltage protection, and adjustable current limit allow for the use of tiny, low-profile inductors and (10-µF) ceramic capacitors. The device is available in a small 20-bump DSBGA package and operates over the –40°C to 85°C temperature range.

Device Information(1)

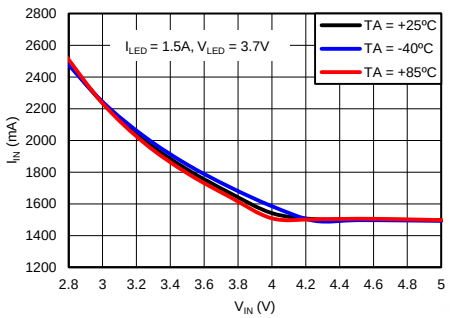
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3646	DSBGA (20)	2.015 mm x 1.615 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit



System Performance



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Original (December 2013) to Revision A **Page**

- Added *Device Information* and *Handling Rating* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; moved some curves to *Application Curves* section ... 1
- Deleted "TX interrupt" ... 12
- Changed reference to "Max LED Control Register (0x05)" to "Enable Register (0x01)" ... 14
- Added Control Truth table ... 17

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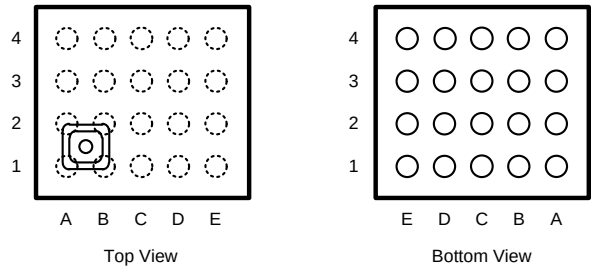
5 Pin Configuration and Functions

DSBGA Package
20 Pins



Pin Functions

PIN			TYPE	DESCRIPTION
NUMBER	COUNT	NAME		
A1, B1	2	GND	-	Ground.
A2, B2	2	SW	O	Drain Connection for Internal NMOS and Synchronous PMOS Switches.
A3, B3, C3	3	OUT	O	Step-Up DC/DC Converter Output. Connect a 10-µF ceramic capacitor between this pin and GND.
A4,B4	2	LED1	O	High-Side Current Source Output for Flash LED. Both bumps must be connected for proper operation.
C1	1	AGND	-	Analog Ground.
C2	1	TORCH	I	Active High Hardware Torch Enable. Drive TORCH high to turn on Torch/Movie Mode. Used for External PWM mode. Has an internal pull-down resistor of 200 kΩ between TORCH and GND.
C4, D4	2	LED2	O	High-Side Current Source Output for Flash LED. Both bumps must be connected for proper operation.
D1	1	IN	I	Input Voltage Connection. Connect IN to the input supply, and bypass to GND with a 10-µF or larger ceramic capacitor.
D2	1	SCL	I	Serial Clock Input.
D3	1	ENABLE	I	Active High Enable Pin. High = Standby, Low = Shutdown/Reset. Has an internal pull-down resistor of 200 kΩ between ENABLE and GND.
E1	1	TEMP	O	Threshold Detector for LED Temperature Sensing and Current Scale Back.
E2	1	SDA	I/O	Serial Data Input/Output.
E3	1	STROBE	I	Active High Hardware Flash Enable. Drive STROBE high to turn on Flash LEDs. STROBE overrides TORCH. Has an internal pull-down resistor of 200 kΩ between STROBE and GND.
E4	1	TX	I	Configurable Dual Polarity Power Amplifier Synchronization Input. Has an internal pull-down resistor of 200 kΩ between TX and GND.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
SCL, SDA, ENABLE, STROBE, TX, TORCH, LED1, LED2, TEMP	−0.3	the lesser of (VIN+0.3) w/ 6 max	V
IN, SW, OUT	−0.3	6	V
Continuous power dissipation(3)	Internally Limited		
Junction temperature ($T_{J\text{-}MAX}$)		150	°C
Maximum lead temperature (soldering)	See(4)		

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 135°C (typ.). Thermal shutdown is verified by design.
(4) For detailed soldering specifications and information, please refer to Texas Instruments Application Note 1112: *DSBGA Wafer Level Chip Scale Package* (SNVA009).

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2500	2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1500	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
VIN	2.7	5.5	V
Junction temperature (T_J)	−40	125	°C
Ambient temperature (T_A) (3)	−40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (TA-MAX) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$.

6.4 Thermal Information

THERMAL METRIC(1)		LM3646 YFQ 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Typical (TYP) limits apply for T_A = 25°C. Minimum (MIN) and maximum (MAX) limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C). Unless otherwise specified, V_{IN} = 3.6 V.(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT SOURCE SPECIFICATIONS							
$I_{LED1/2}$	Current source accuracy	1.5A Flash, V_{OUT} = 4 V, LED1 or LED2 Active		1.395 (−7%)	1.5	1.605 (7%)	A
		93.4 mA Torch, V_{OUT} = 3.6 V, LED1 or LED2 Active		84.06 (−10%)	93.4	102.74 (10%)	mA
V_{OUT} - $V_{LED1/2}$	Current source regulation	I_{LED} = 1.5A	Flash		250	280 (12%)	mV
		I_{LED} = 93.4 mA	Torch		150	172.5 (15%)	
STEP-UP DC/DC CONVERTER SPECIFICATIONS							
I_{CL}	Switch current limit			−15%	1	15%	A
				−10%	3.1	10%	
V_{OVP}	Output overvoltage protection trip point	ON threshold		4.85	5.0	5.15	V
		OFF threshold		4.65	4.8	4.95	
R_{PMOS}	RPMOS switch on-resistance	I_{PMOS} = 1A			85		mΩ
R_{NMOS}	NMOS switch on-resistance	I_{NMOS} = 1A			65		
UVLO	Undervoltage lockout threshold	Falling V_{IN}		2.74	2.8	2.85	V
$V_{NTC-Trip}$	NTC comparator trip threshold			−6%	600	6%	mV
I_{NTC}	NTC Current			−6%	50	6%	µA
$V_{NTC-Open}$	NTC open trip threshold			2.2	2.3	2.4	V
$V_{NTC-Short}$	NTC short trip threshold			75	100	125	mV
V_{IVFM}	Input voltage flash monitor trip threshold			−5%	2.9	5%	V
f_{SW}	Switching frequency	2.8 V ≤ V_{IN} ≤ 4.8 V		3.72	4	4.28	MHz
I_{SD}	Shutdown supply current	Device disabled, EN = 0 V 2.8 V ≤ V_{IN} ≤ 4.8 V			0.1	1.3	µA
I_{SB}	Standby supply current	Device disabled, EN = 1.8 V 2.8 V ≤ V_{IN} ≤ 4.8 V			2.5	10	µA
ENABLE, STROBE, TORCH, TX VOLTAGE SPECIFICATIONS							
V_{IL}	Input logic low	2.8 V ≤ V_{IN} ≤ 4.2 V		0		0.4	V
V_{IH}	Input logic high			1.2		V_{IN}	
I^2C-COMPATIBLE INTERFACE SPECIFICATIONS (SCL, SDA)							
V_{IL}	Input logic low	2.8 V ≤ V_{IN} ≤ 4.2 V		0		0.4	V
V_{IH}	Input logic high			1.2		V_{IN}	
V_{OL}	Output logic low	I_{LOAD} = 1.5 mA				300	mV
t_{SCL}	SCL clock period			1			µs

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are 100% production tested at an ambient temperature (T_A) of 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods.

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6.6 Timing Requirements

DELAY	EXPLANATION	TIME
t_a	Time for the LED current to start ramping up after an I^2C Write command.	560 µs
t_b	Time for the LED current to start ramping down after an I^2C Stop command.	120 µs
t_c	Time for the LED current to start ramping up after the STROBE pin is raised high.	560 µs
t_d	Time for the LED current to start ramping down after the STROBE pin is pulled low.	8 µs
t_e	Time for the LED current to start ramping up after the TORCH pin is raised high.	560 µs
t_f	Time for the LED current to start ramping down after the TORCH pin is pulled low.	8 µs
t_g	Time for the LED current to start ramping down after the TX pin is pulled high.	3 µs
t_h	Time for the LED current to start ramping up after the TX pin is pulled low, provided the part has not timed out in flash mode.	2 µs

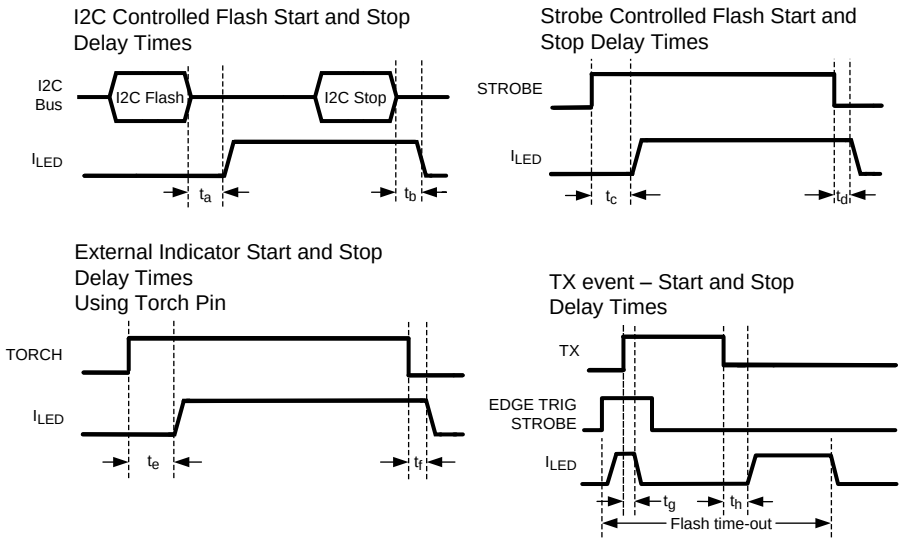

Figure 1. Control Logic Delays

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6.7 Typical Characteristics

Unless otherwise specified: T_A= 25°C; V_{IN} = 3.6 V; V_{EN} = V_{IN}; C_{IN} = 10 µF; C_{OUT} = 10 µF; L = 1 µH.

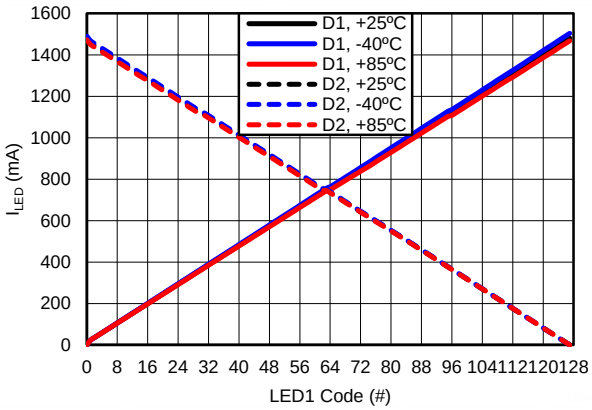

Figure 2. Flash LED Current vs. Brightness Code

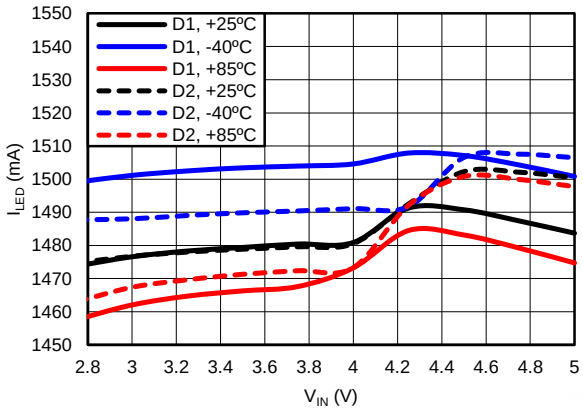

Figure 3. Flash LED Current Line Regulation, I_{LED} = 1.5A

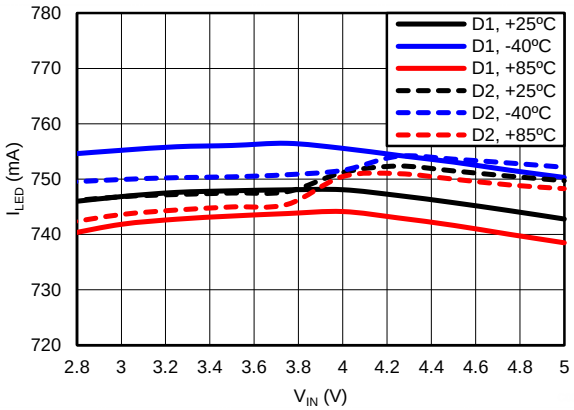

Figure 4. Flash LED Current Line Regulation, I_{LED1} = I_{LED2} = 0.75A

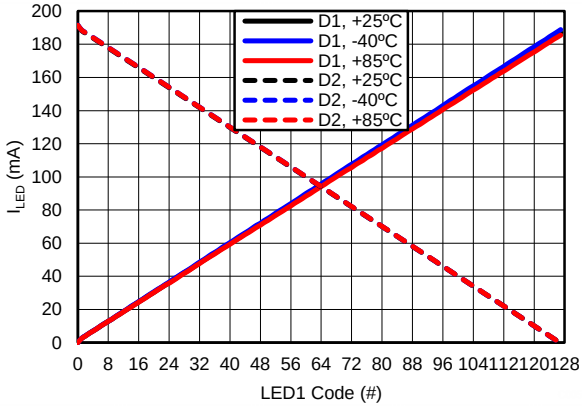

Figure 5. Torch LED Current vs. Brightness Code

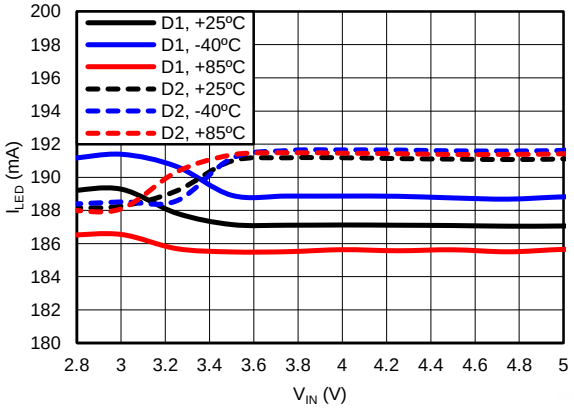

Figure 6. Torch LED Current Line Regulation, I_{LED} = 187.1 mA

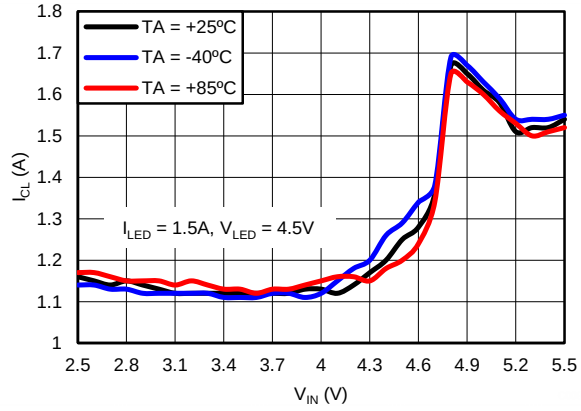

Figure 7. Inductor Current vs. Input Voltage, CL= 1 A

Typical Characteristics (continued)

Unless otherwise specified: T_A= 25°C; V_{IN} = 3.6 V; V_{EN} = V_{IN}; C_{IN} = 10 µF; C_{OUT} = 10 µF; L = 1 µH.

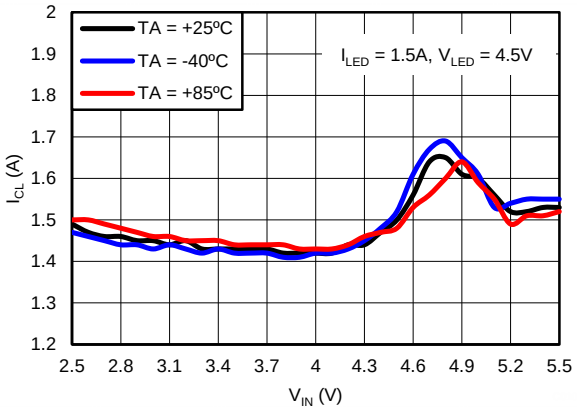

Figure 8. Inductor Current vs. Input Voltage, CL = 1.3 A

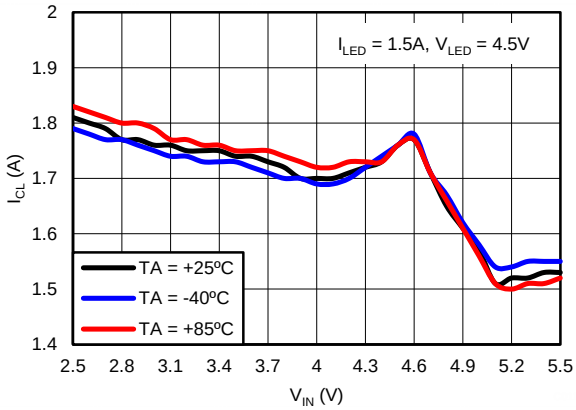

Figure 9. Inductor Current vs. Input Voltage, CL = 1.6 A

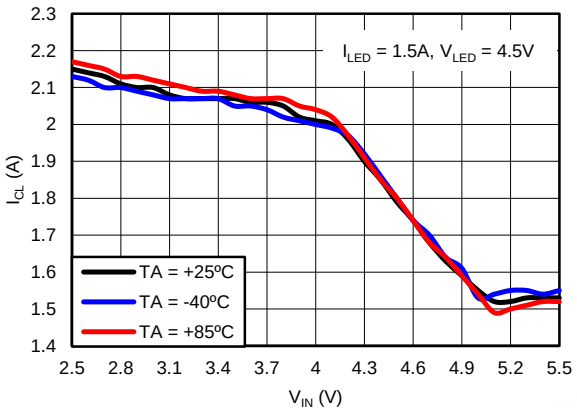

Figure 10. Inductor Current vs. Input Voltage, CL = 1.9 A

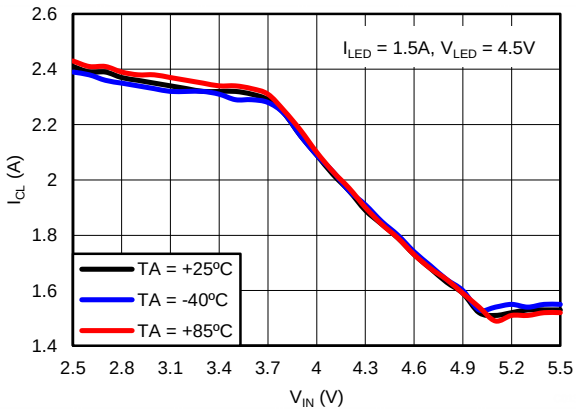

Figure 11. Inductor Current vs. Input Voltage, CL = 2.2 A

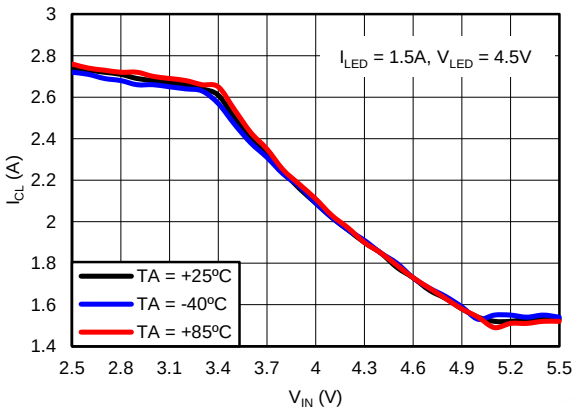

Figure 12. Inductor Current vs. Input Voltage, CL = 2.5 A

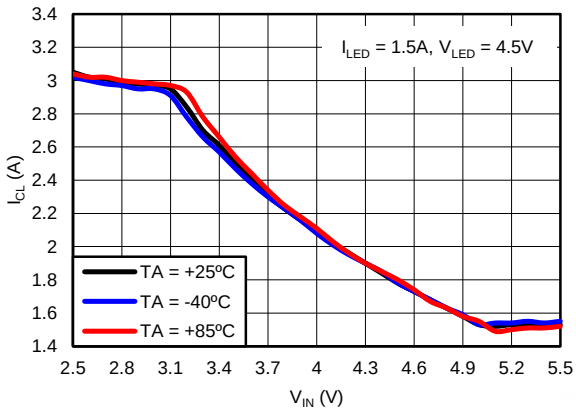

Figure 13. Inductor Current vs. Input Voltage, CL = 2.8 A

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Typical Characteristics (continued)

Unless otherwise specified: T_A= 25°C; V_{IN} = 3.6 V; V_{EN} = V_{IN}; C_{IN} = 10 µF; C_{OUT} = 10 µF; L = 1 µH.

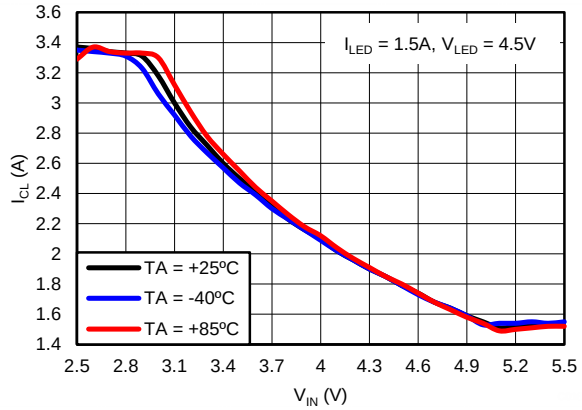

Figure 14. Inductor Current vs. Input Voltage, CL = 3.1 A

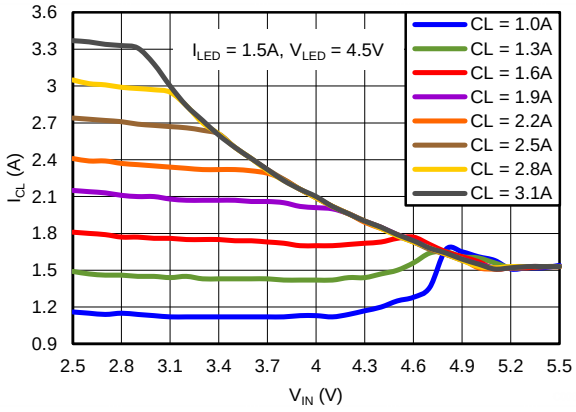

Figure 15. Inductor Current Limit vs. Input Voltage

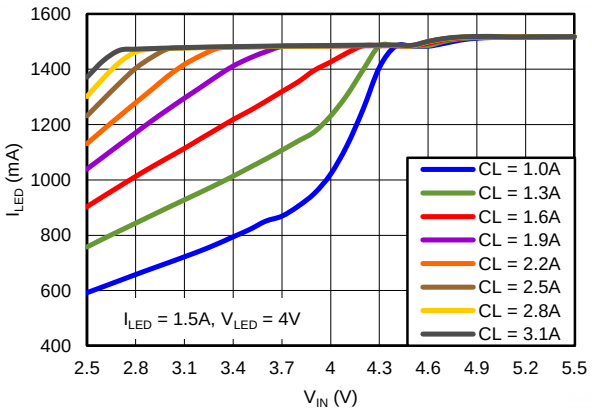

Figure 16. Flash LED Current vs. Input Voltage in Current Limit

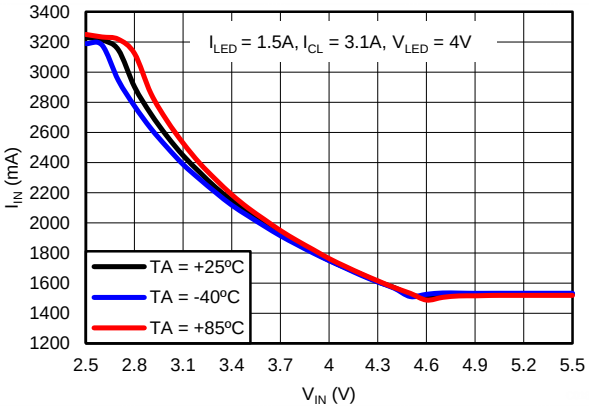

Figure 17. Input Current vs. Input Voltage

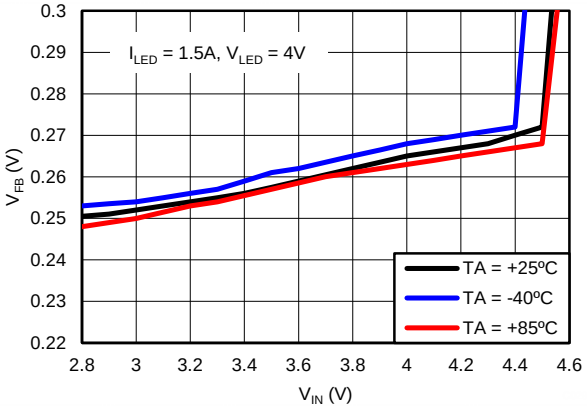

Figure 18. Current Source Headroom vs. Input Voltage

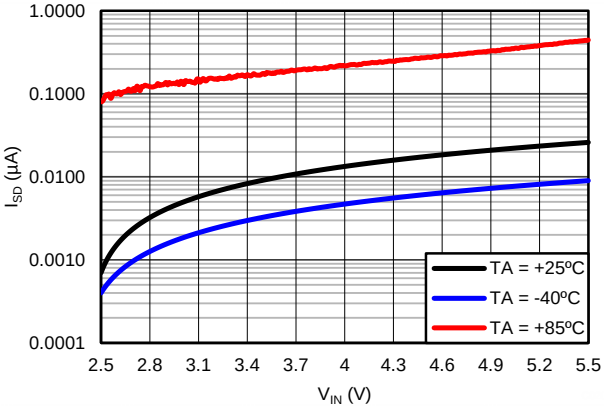

Figure 19. Shutdown Current vs. Input Voltage

Typical Characteristics (continued)

Unless otherwise specified: T_A= 25°C; V_{IN} = 3.6 V; V_{EN} = V_{IN}; C_{IN} = 10 µF; C_{OUT} = 10 µF; L = 1 µH.

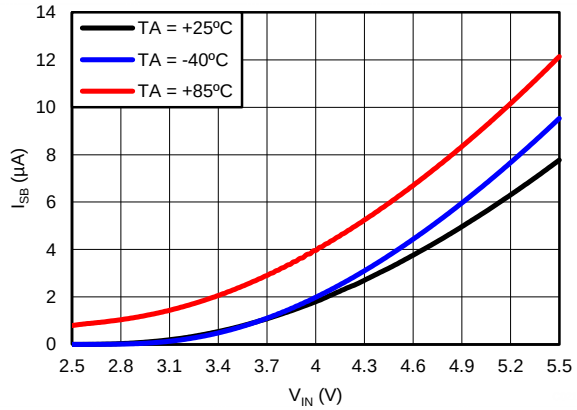

Figure 20. Standby Current vs. Input Voltage, V_{EN} = 1.8 V

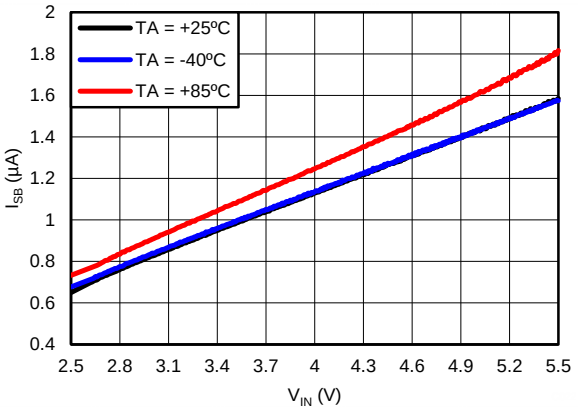

Figure 21. Standby Current vs. Input Voltage, V_{EN} = VIN

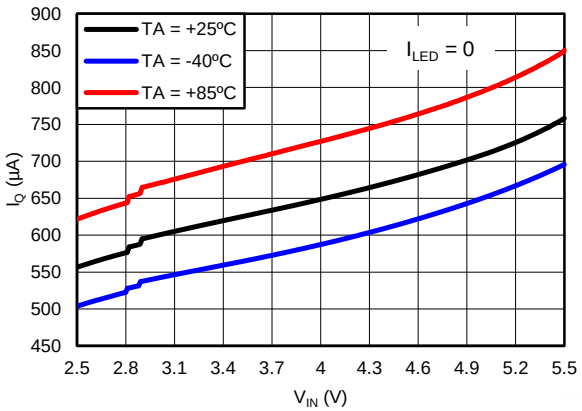

Figure 22. Input Current vs. Input Voltage in Pass Mode

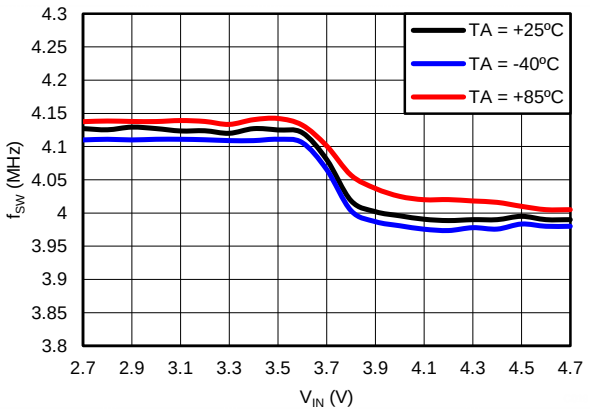

Figure 23. Frequency vs. Input Voltage

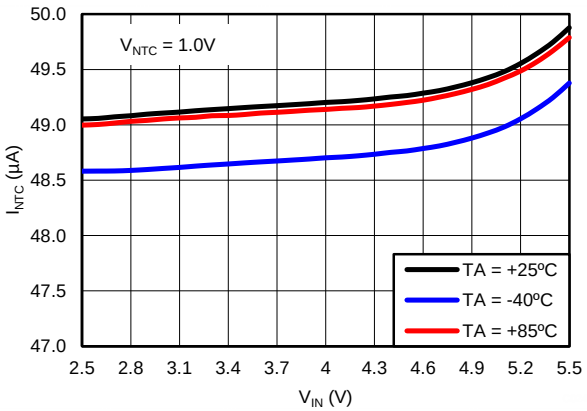

Figure 24. NTC Bias Current vs. Input Voltage

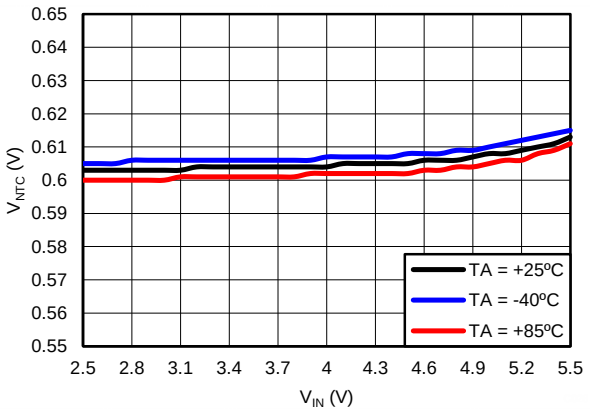

Figure 25. NTC Threshold vs. Input Voltage, V_{NTC} = 0.6 V

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Typical Characteristics (continued)

Unless otherwise specified: T_A= 25°C; V_{IN} = 3.6 V; V_{EN} = V_{IN}; C_{IN} = 10 µF; C_{OUT} = 10 µF; L = 1 µH.

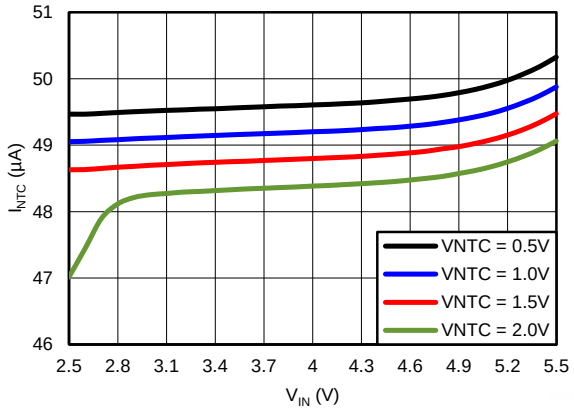

Figure 26. NTC Bias Current vs. Input Voltage at Different V_{NTC}

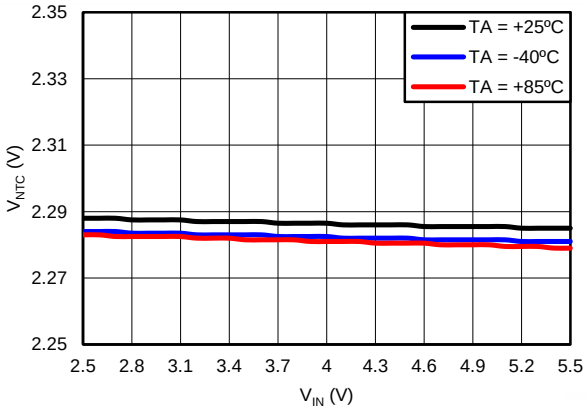

Figure 27. NTC Open Threshold vs. Input Voltage

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7 Detailed Description

7.1 Overview

The LM3646 is a high-power white LED flash driver capable of delivering up to 1.5 A (total LED current) into two parallel LEDs. The device incorporates a 4-MHz constant frequency, synchronous Current-Mode PWM boost converter, and two high-side current sources to regulate the LED current over the 2.7 V to 5.5 V input voltage range.

The LM3646 PWM converter switches and maintains at least V_{HR} across the current sources (LED1 and LED2). This minimum headroom voltage ensures that the current source remains in regulation. If the input voltage is above the LED voltage + current source headroom voltage, the device does not switch and turns the PFET on continuously (Pass Mode). In Pass Mode the difference between (V_{IN} - I_{LED} x R_{PMOS}) and the voltage across the LED is dropped across the current sources.

The LM3646 has three logic inputs including a hardware Flash Enable (STROBE), a hardware Torch Enable (TORCH) used for external Torch Mode control, and a Flash Interrupt input (TX) designed to interrupt the flash pulse during high battery current conditions. All three logic inputs have internal 200 kΩ (typ.) pull-down resistors to GND.

Additional features of the LM3646 include an internal comparator for LED thermal sensing via an external NTC thermistor and an input voltage monitor that can reduce the Flash current (during low V_{IN} conditions).

Control of the LM3646 is done via an I^2C-compatible interface. This includes adjustment of the Flash and Torch current levels, current source selection, changing the Flash Timeout Duration, changing the switch current limit, and enabling the NTC block. Additionally, there are flag and status bits that indicate flash current time-out, LED over-temperature condition, LED failure (open/short), device thermal shutdown and V_{IN} undervoltage conditions.

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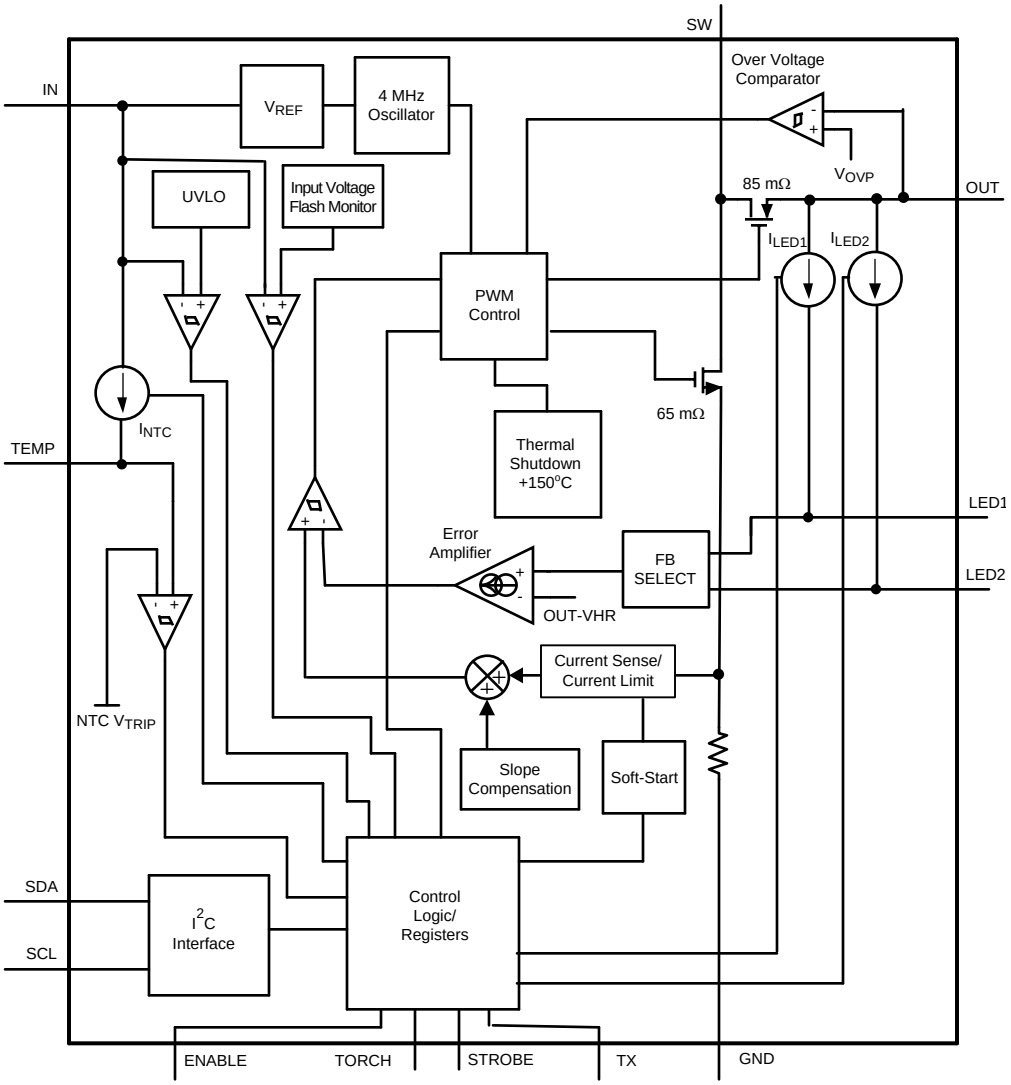
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Flash Mode

In Flash Mode, the LED current sources (LED1/2) provide 128 target current levels from 0 mA to 1500 mA. The Flash currents are adjusted via bits[3:0] of the *Max LED Current Control Register (0x05)* and bits[6:0] of the *LED1 Flash Current Control Register (0x06)*. Flash Mode is activated by the *Enable Register (0x01)*, or by pulling the STROBE pin HIGH. Once the Flash sequence is activated the current source (LED) will ramp up to the programmed Flash current by stepping through all current steps until the programmed current is reached.

While both LED1 and LED2 are capable of delivering 1.5A to the LED, the sum total of the LED current will not exceed the value stored in the Max LED Current Control Register. LED1 will receive the current value stored in the LED1 Flash Current Control Register, and LED2 will receive the difference of the value stored in the MAX LED Current Control Register and LED1 Flash Current Control Register.

If LED1 and LED2 Active:

LED1 = LED1 Flash Current Control Value

LED2 = MAX Flash Current Control Value - LED1 Flash Current Control Value

If MAX Flash Current Control Value < LED1 Flash Current Control Value

LED1 = MAX Flash Current Control Value

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Feature Description (continued)

LED2 = Off

If the LED1 Current Control Value is set to a level that is higher than the MAX Flash LED Current Control Value, LED1 receives the MAX Flash LED Current Control value, and LED2 is disabled.

When the part is enabled in Flash Mode through the Enable Register or the STROBE pin, all mode bits in the Enable Register are cleared after completion of the flash event. Before the device can be enabled again, the mode bits need to be set.

7.3.2 Torch Mode

In Torch Mode, the LED current sources (LED1/2) provide 128 target current levels from 0 mA to 187.5 mA. The Torch currents are adjusted via bits[6:4] of the *Max LED Current Control Register (0x05)* and bits[6:0] of the *LED1 Torch Current Control Register (0x07)*. Torch Mode is activated by the *Enable Register (0x01)*, or by pulling the TORCH pin HIGH. Once the TORCH sequence is activated the current source (LED) will ramp up to the programmed Torch current by stepping through all current steps until the programmed current is reached.

LED1 receives the current value stored in the LED1 Torch Current Control Register, and LED2 receives the difference of the value stored in the MAX LED Current Control Register and LED1 Torch Current Control Register.

If LED1 and LED2 Active:

LED1 = LED1 Torch Current Control Value

LED2 = MAX Torch Current Control Value - LED1 Torch Current Control Value

If MAX Torch Current Control Value < LED1 Torch Current Control Value

LED1 = MAX Torch Current Control Value

LED2 = Off

If the LED1 Torch Current Control Value is set to a level that is higher than the MAX Torch LED Current Control Value, LED1 receives the MAX Torch LED Current Control value, and LED2 is disabled. Torch Mode is not affected by Flash Timeout.

7.4 Device Functional Modes

7.4.1 Start-Up (Enabling the Device)

Turn on of the LM3646 Torch and Flash Modes can be done through the *Enable Register (0x01)*. On start-up, when V_{OUT} is less than V_{IN}, the internal synchronous PFET turns on as a current source and delivers 200 mA (typ.) to the output capacitor. During this time the current source (LED) is off. When the voltage across the output capacitor reaches 2.2 V (typ.) the current source turns on. At turnon the current source steps through each FLASH or TORCH level until the target LED current is reached. This gives the device a controlled turn-on and limits inrush current from the VIN supply.

7.4.2 Pass Mode

The LM3646 starts up in Pass Mode and stays there until Boost Mode is needed to maintain regulation. In Pass Mode the boost converter does not switch and the synchronous PFET turns fully on bringing V_{OUT} up to V_{IN} - (I_{LED} x R_{PMOS}). In Pass Mode the inductor current is not limited by the peak current limit. In this situation the output current must be limited to 2A. If the voltage difference between V_{OUT} and V_{LED} falls below V_{HR}, the device switches to Boost Mode.

7.4.3 Power Amplifier Synchronization (TX)

The TX pin is a Power Amplifier Synchronization input. This is designed to reduce the flash LED current and thus limit the battery current during high battery current conditions such as PA transmit events. When the LM3646 is engaged in a Flash event and the TX pin is pulled high, the LED current is forced into Torch Mode at the programmed Torch current setting. If the TX pin is then pulled low before the Flash pulse terminates, the LED current will return to the previous Flash current level. At the end of the Flash time-out, whether the TX pin is high or low, the LED current will turn off. The TX input can be disabled by setting bit TX Pin Enable to a '0' in the *Enable Register (0x01)*.

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Device Functional Modes (continued)

7.4.4 Input Voltage Flash Monitor (IVFM)

The LM3646 has the ability to adjust the flash current based upon the voltage level present at the IN pin utilizing an Input Voltage Flash Monitor. The IVFM block has an adjustable threshold (IVM-D) ranging from 2.9 V to 3.2 V in 100-mV steps as well as adjustable hysteresis. The IVFM threshold and hysteresis are controlled by bits[4:3] and bits[2:1] respectively, in the *IVFM Mode Register (0x02)*. *Flags Register1 (0x08)* has the IVFM flag (bit[3]) set when the input voltage crosses the IVFM value. The IVFM threshold sets the input voltage boundary that forces the LM3646 to stop ramping the flash current during startup in Stop and Hold Mode, or to actively adjust the LED current lower in Down Adjust Mode, or to continuously adjust the LED current up and down in Up & Down mode.

Stop and Hold Mode (Figure 28): Stops Current Ramp and Holds the level for the remaining flash if V_{IN} crosses IVM-D Line. Sets IVFM Flag (bit[3] in Flags Register1) upon crossing IVM-D Line.

Down Mode (Figure 29): Adjusts current down if V_{IN} crosses IVM-D Line and stops decreasing once V_{IN} rises above the IVM-D line + the IVFM hysteresis setting. The LM3646 will decrease the current throughout the flash pulse anytime the input voltage falls below the IVM-D line, not just once. The flash current will not increase again until the next flash. Sets IVFM Flag (bit[3] in Flags Register1) upon crossing IVM-D Line.

Up and Down Mode (Figure 30): Adjusts current down if V_{IN} crosses IVM-D Line and adjusts current up if V_{IN} rises above the IVM-D line + the IVFM hystersis setting. In this mode, the current will continually adjust with the rising and falling of the input voltage throughout the entire flash pulse. Sets IVFM Flag (bit[3] in Flags Register1) upon crossing IVM-D Line.

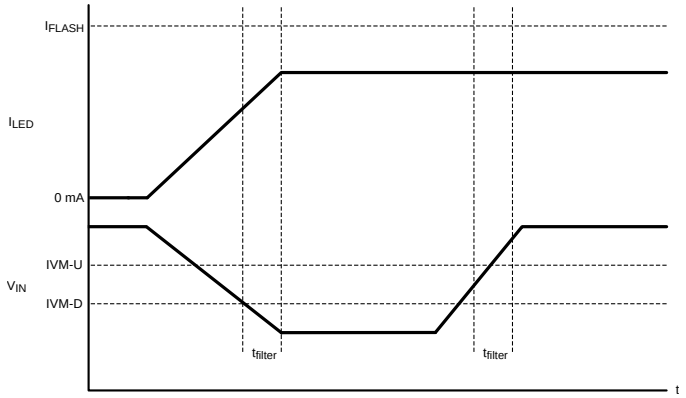

Figure 28. IVFM Stop and Hold Mode

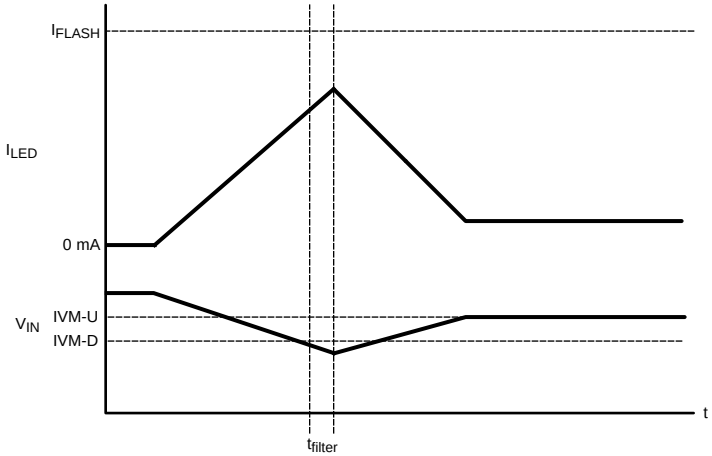

Figure 29. IVFM Down Mode

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Device Functional Modes (continued)

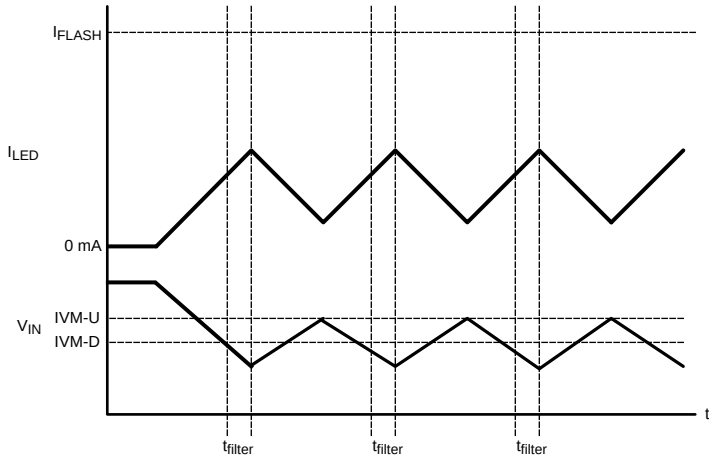

Figure 30. IVFM Up and Down Mode

7.4.5 Fault/Protections

7.4.5.1 Fault Operation

Upon entering a fault condition, the LM3646 sets the appropriate flag in the *Flags Register1 (0x08)* or *Flags Register2 (0x09)*, and place the part into standby by clearing and locking the Torch Enable bit (bit[7] in *LED1 Torch Current Control Register (0x07)*) and Mode Bits (M1, M0) in the *Enable Register (0x01)*, until the Flags Register1 or Flags Register2 is read back via I^2C.

7.4.5.2 Flash Time-Out

The Flash Time-Out period sets the amount of time that the Flash Current is being sourced from the current source (LED). The LM3646 has 8 timeout levels ranging 50 ms to 400 ms in 50 ms steps. The Flash Time-Out period is controlled by bits[2:0] in the *Flash Timing Register (0x04)*. Flash Time-Out only applies to the Flash Mode operation. The mode bits are cleared and bit[0] is set in the *Flags Register1 (0x08)* upon a Flash Timeout.

7.4.5.3 Overvoltage Protection (OVP)

The output voltage is limited to typically 5 V (see $\mathbf{V_{OVP}}$ Spec). In situations such as an open LED, the LM3646 raises the output voltage in order to try to keep the LED current at its target value. When V_{OUT} reaches 5 V (typ.) the overvoltage comparator trips and turns off the internal NFET. When V_{OUT} falls below the "**V_{OVP} Off Threshold**", the LM3646 begins switching again. The mode bits are cleared, and the OVP flag is set (bit[7] in *Flags Register1 (0x08)*) when an OVP condition is present for 512 microseconds, preventing momentary OVP events from forcing the part to shut down.

7.4.5.4 Current Limit

The LM3646 features 8 selectable inductor current limits ranging from 1 A to 3.1 A in 300-mA steps. The current limit is programmable through bits[7:5] of the *Enable Register (0x01)* of the I^2C-compatible interface. When the inductor current limit is reached, the LM3646 terminates the charging phase of the switching cycle.

Since the current limit is sensed in the NMOS switch, there is no mechanism to limit the current when the device operates in Pass Mode. In Boost Mode or Pass Mode if V_{OUT} falls below 2.3 V, the part stops switching, and the PFET operates as a current source limiting the current to 200 mA. This prevents damage to the LM3646 and excessive current draw from the battery during output short-circuit conditions. The mode bits are not cleared upon a Current Limit event, but the OCP flag (bit[4]) in *Flags Register1 (0x08)* is set.

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Device Functional Modes (continued)

7.4.5.5 NTC Thermistor Input (TEMP)

The TEMP pin serves as a threshold detector for negative temperature coefficient (NTC) thermistors. It interrupts the LED current and sets the NTC TRIP flag bit[6] in *Flags Register1 (0x08)* when the voltage at TEMP goes below the programmed threshold. The NTC threshold voltage is adjustable from 200 mV to 900 mV in 100 mV steps via the *NTC and Torch Ramp Register (0x03)*. The NTC current is set to 50 µA. When an over-temperature event is detected, the LM3646 is forced into shutdown. The NTC detection circuitry can be enabled or disabled via bit[4] of the *Enable Register (0x01)*. If Enabled, the NTC block will turn on and off during the start and stop of a Flash/Torch event. The mode bits are cleared upon an NTC event.

Additionally, the NTC input looks for an open NTC connection and a short NTC connection. If the NTC input falls below 100 mV, the NTC short flag is set (bit[1] in *Flags Register2 (0x09)*), and the part is disabled. If the NTC input rises above 2.3 V, the NTC Open flag is set (bit[0] in Flags Register2), and the part is disabled. These fault detections can be individually disabled/enabled via the NTC Open Detect Enable bit in *IVFM Mode Register (0x02)* and the NTC Short Fault Enable bit in Flags Register2.

7.4.5.6 Undervoltage Lockout (UVLO)

The LM3646 has an internal comparator that monitors the voltage at IN and forces the LM3646 into shutdown if the input voltage drops to 2.8 V. If the UVLO monitor threshold is tripped, the UVLO flag bit is set in *Flags Register1 (0x08)*. If the input voltage rises above 2.8 V, the LM3646 is not available for operation until there is an I^2C read command initiated for the Flags Register1. Upon a read, Flags Register1 is cleared, and normal operation can resume if the input voltage is greater than 2.8 V. This feature can be disabled by writing a '0' to the UVLO Enable bit in the *IVFM Mode Register (0x02)*. The mode bits are cleared upon a UVLO event.

7.4.5.7 Thermal Shutdown (TSD)

When the LM3646's die temperature reaches 135°C the boost converter shuts down, and the NFET and PFET turn off, as does the current source (LED). When the thermal shutdown threshold is tripped, a '1' gets written to bit[5] of *Flags Register1 (0x08)* (Thermal Shutdown bit), and the LM3646 will go into standby. The LM3646 is allowed to restart only after Flags Register1 is read, clearing the fault flag. Upon restart, if the die temperature is still above 135°C, the LM3646 resets the Fault flag and re-enters standby. The mode bits are cleared upon a TSD.

7.4.5.8 LED and/or VOUT Short Fault

The LED Fault flags (bit[2] or bit[3]) in *Flags Register2 (0x09)* read back a '1' if the part is active in Flash or Torch Mode and either LED output experiences a short condition. The Output Short Fault flag (bit[1] in *Flags Register1 (0x08)*) reads back a '1' if the part is active in Flash or Torch Mode and the boost output experiences a short condition. An LED short condition is determined if the voltage at LED goes below 500 mV (typ.); VOUT short condition occurs if the voltage at OUT goes below 2.1 V (typ.) while the device is in Torch or Flash Mode. There is a delay of 256 µs deglitch time before the LED flag is valid and 2.048 ms before the VOUT flag is valid. This delay is the time between when the Flash or Torch current is triggered, and when the LED voltage and the output voltage are sampled. The LED and VOUT short flags can only be reset to '0' by removing power to the LM3646, or by reading back the Flags Register1 or Flags Register2. The mode bits are cleared upon an LED and/or VOUT short fault.

7.5 Programming

7.5.1 Control Truth Table

Table 1. Control Truth Table

MODE1	MODE0	STROBE EN	TORCH EN	STROBE PIN	TORCH PIN	ACTION
0	X	X	0	X	X	Standby
0	X	X	1	X	pos edge	Ext Torch
1	1	1	X	pos edge	X	Ext Flash
1	0	X	0	X	X	Int Torch
1	1	0	X	X	X	Int Flash

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7.5.2 I²C-Compatible Interface

7.5.2.1 Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW.

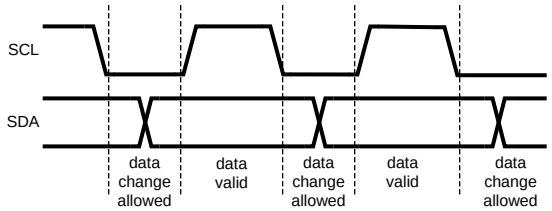

Figure 31. Data Validity Diagram

A pull-up resistor between the controller's VIO line and SDA must be greater than [(**VIO-V_{OL}) / 3mA**] to meet the V_{OL} requirement on SDA. Using a larger pullup resistor results in lower switching current with slower edges, while using a smaller pullup results in higher switching currents with faster edges.

7.5.2.2 START and STOP Conditions

START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C-compatible master always generates START and STOP conditions. The I²C-compatible bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I²C-compatible master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

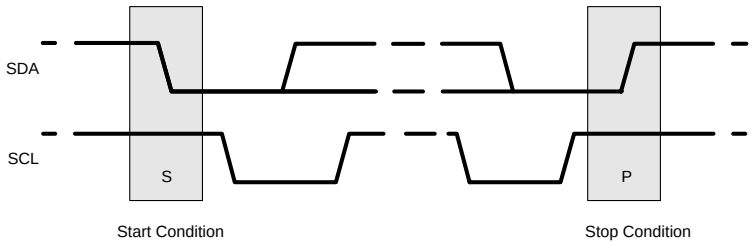

Figure 32. Start and Stop Conditions

7.5.2.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LM3646 pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LM3646 generates an acknowledge after each byte is received. There is no acknowledge created after data is read from the LM3646.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM3646 7-bit address is 0x67 (Figure 33). For the eighth bit, a '0' indicates a WRITE, and a '1' indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

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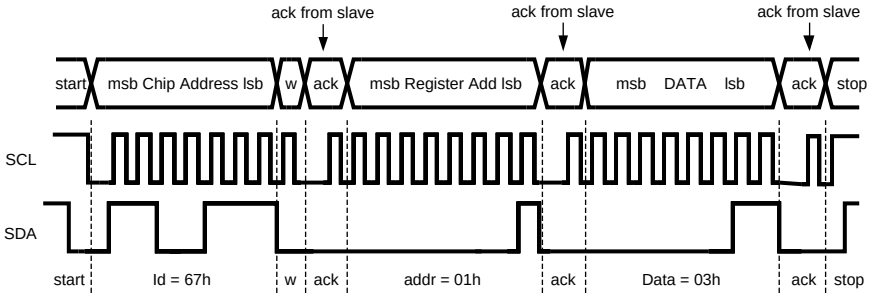

w = write (SDA = "0") , r = read (SDA = "1") , ack = acknowledge (SDA pulled down by either master or slave), id = chip address, 67h for LM3646

Figure 33. Write Cycle for the LM3646

7.5.2.4 I²C-Compatible Chip Address

The device address for the LM3646 is 1100111 (67). After the START condition, the I²C-compatible master sends the 7-bit address followed by an eighth read or write bit (R/W). R/W = 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the device address selects the register address to which the data will be written. The third byte contains the data for the selected register.

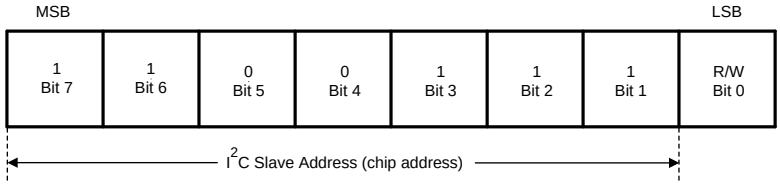

Figure 34. I²C-Compatible Device Address for LM3646

7.6 Register Map

Table 2. LM3646 Internal Registers

Register Name	Internal Hex Address	Power On/RESET Value(1)
SILICON REVISION REGISTER	0x00	0x11
ENABLE REGISTER	0x01	0xE0
IVFM MODE REGISTER	0x02	0xA4
NTC AND TORCH RAMP REGISTER	0x03	0x20
FLASH TIMING REGISTER	0x04	0x42
MAX LED CURRENT CONTROL REGISTER	0x05	0x7F
LED1 FLASH CURRENT CONTROL REGISTER	0x06	0x7F
LED1 TORCH CURRENT CONTROL REGISTER	0x07	0x7F
FLAGS REGISTER1	0x08	0x00
FLAGS REGISTER2	0x09	0x30

(1) All unused bits are internally pulled HIGH.

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7.6.1 Silicon Revision Register (0x00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU		Chip ID Current Value = '010'			Silicon Revision Current Value = '001'		

7.6.2 Enable Register (0x01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Inductor Current Limit 000 = 1.0A 001 = 1.3A 010 = 1.6A 011 = 1.9A 100 = 2.2A 101 = 2.5A 110 = 2.8A 111 = 3.1A (default)			**NTC Enable** 0 = Disabled (default) 1 = Enabled	**TX Pin Enable** 0 = Disabled (default) 1 = Enabled	**Soft-Start Enable** Enable 0 = Disabled (default) 1 = Enabled	**LED Mode Bits: M1, M0** 00 = Standby (default) 01 = Standby 10 = Torch 11 = Flash	

NTC Enable Enables or Disables the NTC detection block when the LM3646 is enabled

TX Pin EN Enables the TX pin and TX current reduction function

Soft-Start EN Enables the Pass-Mode startup sequence

LED Mode Bits (M1, M0)

00–Standby Off

01–Standby Off

10–Torch Sets Torch Mode. If Torch EN = 0, Torch will start after I^2C-compatible command.

11–Flash Sets Flash Mode. If Strobe EN = 0, Flash will start after I^2C-compatible command.

7.6.3 IVFM Mode Register (0x02)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UVLO Enable(2.8 V) 0 = Disabled 1 = Enabled (default)	**IVFM Filter** 0 = 4 µs (default) 1 = 256 µs	**IVFM Enable** 0 = Disabled 1 = Enabled (default)	**IVFM Level Adjust Threshold** 00 = 2.9V (default) 01 = 3.0V 10 = 3.1V 11 = 3.2V		**IVFM Mode/Hysteresis** 00 = Ramp and Hold 01 = 0mV Hyst 10 = 50 mV Hyst (default) 11 = 100 mV Hyst		**NTC Open Fault Enable** 0 = Disabled (default) 1 = Enabled

7.6.4 NTC and Torch Ramp Register (0x03)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Boost Mode 00 = Automatic (default) 01 = Force Pass-Mode 10 = Force Boost-Mode 11 = Automatic		**NTC Trip Thresholds** 000 = 200 mV 001 = 300 mV 010 = 400 mV 011 = 500 mV 100 = 600 mV (default) 101 = 700 mV 110 = 800 mV 111 = 900 mV			**Torch Current Ramp Times** 000 = Ramp Disabled (default) 001 = 16 ms 010 = 32 ms 011 = 64 ms 100 = 128 ms 101 = 256 ms 110 = 512 ms 111 = 1024 ms		

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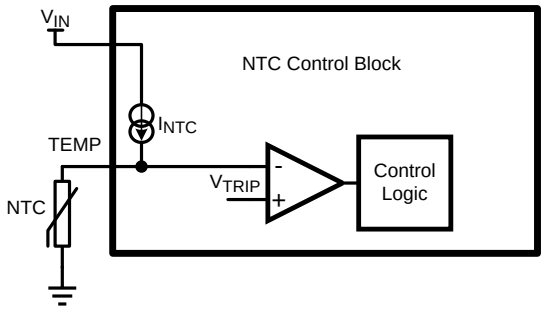

Figure 35. NTC Control Block

The TEMP node is connected to an NTC resistor as shown in Figure 35. A constant current source from the input is connected to this node. Any change in the voltage because of a change in the resistance of the NTC resistor is compared to a set V_{TRIP}. The trip thresholds are selected by Bits[5:3] of the NTC and Torch Ramp Register.

7.6.5 Flash Timing Register (0x04)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IVFM Modulation	**Strobe Usage**	**Flash Ramp Time**			**Flash Time-Out Time**		
0 = Down Adjust (default) 1 = Up/Down Adjust	0 = Level 1 = Edge (default)	000 = 256 µs (default) 001 = 512 µs 010 = 1.024 ms 011 = 2.048 ms 100 = 4.096 ms 101 = 8.192 ms 110 = 16.384 ms 111 = 32.768 ms			000 = 50 ms 001 = 100 ms 010 = 150 ms (default) 011 = 200 ms 100 = 250 ms 101 = 300 ms 110 = 350 ms 111 = 400 ms		

7.6.6 Max LED Current Control Register (0x05)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LED Short Fault Enable	**Max Torch Current**			**Max Flash Current**			
0 = Down Adjust (default) 1 = Up/Down Adjust	000 = 23.04 mA 001 = 46.48 mA 010 = 69.91 mA 011 = 93.35 mA 100 = 116.79 mA 101 = 140.23 mA 110 = 163.66 mA 111 = 187.10 mA (default)			0000 = 93.35 mA 0001 = 187.10 mA 0010 = 280.85 mA 0011 = 374.60 mA 0100 = 468.35 mA 0101 = 562.10 mA 0110 = 655.85 mA 0111 = 749.60 mA 1000 = 843.35 mA 1001 = 937.10 mA 1010 = 1030.85 mA 1011 = 1124.60 mA 1100 = 1218.35 mA 1101 = 1312.10 mA 1110 = 1405.85 mA 1111 = 1499.60 mA (default)		

If LED1 and LED2 Active:

LED2 = MAX Current Control Value - LED1 Current Control Value

If MAX Current Control Value < LED1 Current Control Value

LED1 = MAX Current Control Value

LED2 = Off

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7.6.7 LED1 Flash Current Control Register (0x06)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Strobe Pin Enable Bit 0 = Disabled (default) 1 = Enabled	**LED1 Flash Current Level** 0x00= 0 mA, LED1 Disabled, LED2 = Max Flash Current 0x01 = 23.04 mA 0x02 = 34.76 mA 0x03 = 46.48 mA 0x04 = 58.19 mA . . . 0x7D = 1476.16 mA 0x7E = 1487.88 mA 0x7F = 1499.60 mA, LED2 Disabled (default)						

7.6.8 LED1 Torch Current Control Register (0x07)

LED1 TORCH CURRENT CONTROL REGISTER (0x07)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Torch Pin Enable Bit 0 = Disabled (default) 1 = Enabled	**LED1 Torch Current Level** 0x00= 0 mA, LED1 Disabled, LED2 = Max Torch Current 0x01 = 2.53 mA 0x02 = 3.99 mA 0x03 = 5.46 mA 0x04 = 6.92 mA . . . 0x7D = 184.17 mA 0x7E = 185.64 mA 0x7F = 187.10 mA, LED2 Disabled (default)						

7.6.9 Flags Register1 (0x08)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OVP 0 = Default	NTC TRIP 0 = Default	THERMAL SHUTDOWN 0 = Default	OCP 0 = Default	IVFM 0 = Default	UVLO 0 = Default	VOUT SHORT FAULT 0 = Default	FLASH TIMEOUT 0 = Default

OVP Fault	Over-Voltage Protection tripped. Open Output capacitor or open LED.
NTC Trip Fault	NTC Threshold crossed.
Thermal Shutdown Fault	LM3646 Die temperature reached thermal shutdown value.
Over-Current Protection Event Flag	Inductor Current limit value was reached.
IVFM Flag	IVFM block adjusted LED current.
UVLO Fault	UVLO Threshold crossed.
VOUT Short Fault	VOUT Short detected.
Time-Out Flag	Flash Time-Out detected.

Note: Faults require an I^2C read-back of the "Flags Register" to resume operation. Flags report an event occurred, but do not inhibit future functionality. A read-back of the Flags Register will only get updated again if the fault or flag is still present upon a restart.

7.6.10 Flags Register2 (0x09)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	**SOFTWARE RESET Bit** 0 = Normal Operation (Default) 1 = RESET	**Fault Shutdown Enable** 0 = Disabled 1 = Enabled (default)	**NTC Short Fault Enable** 0 = Disabled 1 = Enabled (default)	**LED2 Short Fault** 0 = Default	**LED1 Short Fault** 0 = Default	**NTC Short Flag** 0 = Default	**NTC Open Flag** 0 = Default

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Software Reset Bit	Writing to this bit resets the LM3646 to the default power up conditions. This bit self-clears upon assertion.
Fault Shutdown Enable	When Enabled, faults will force the LM3646 to shutdown. When disabled, faults will not force the LM3646 to shutdown. The LM3646 protection mechanisms will remain active until the part is manually disabled via the I^2C bus.
NTC Short Fault Enable	When enabled, NTC Short faults will be detected and reported. When disabled, NTC Short faults will not be detected or reported.
LED2 Short Fault	Set to a '1' if LED2 is shorted.
LED1 Short Fault	Set to a '1' if LED1 is shorted.
NTC Short Fault	The NTC Short Flag is set if the NTC pin voltage crosses below 100 mV during operation.
NTC Open Fault	The NTC Open Flag is set if the NTC pin voltage crosses above 2.3V during operation.

Note: An I^2C readback of the Flags Register2 will clear both the NTC Open and NTC Short Flags.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3646 can drive two flash LED at currents up to 1.5 A total. The 4-MHz DC/DC boost regulator allows for the use of small value discrete external components.

8.2 Typical Application

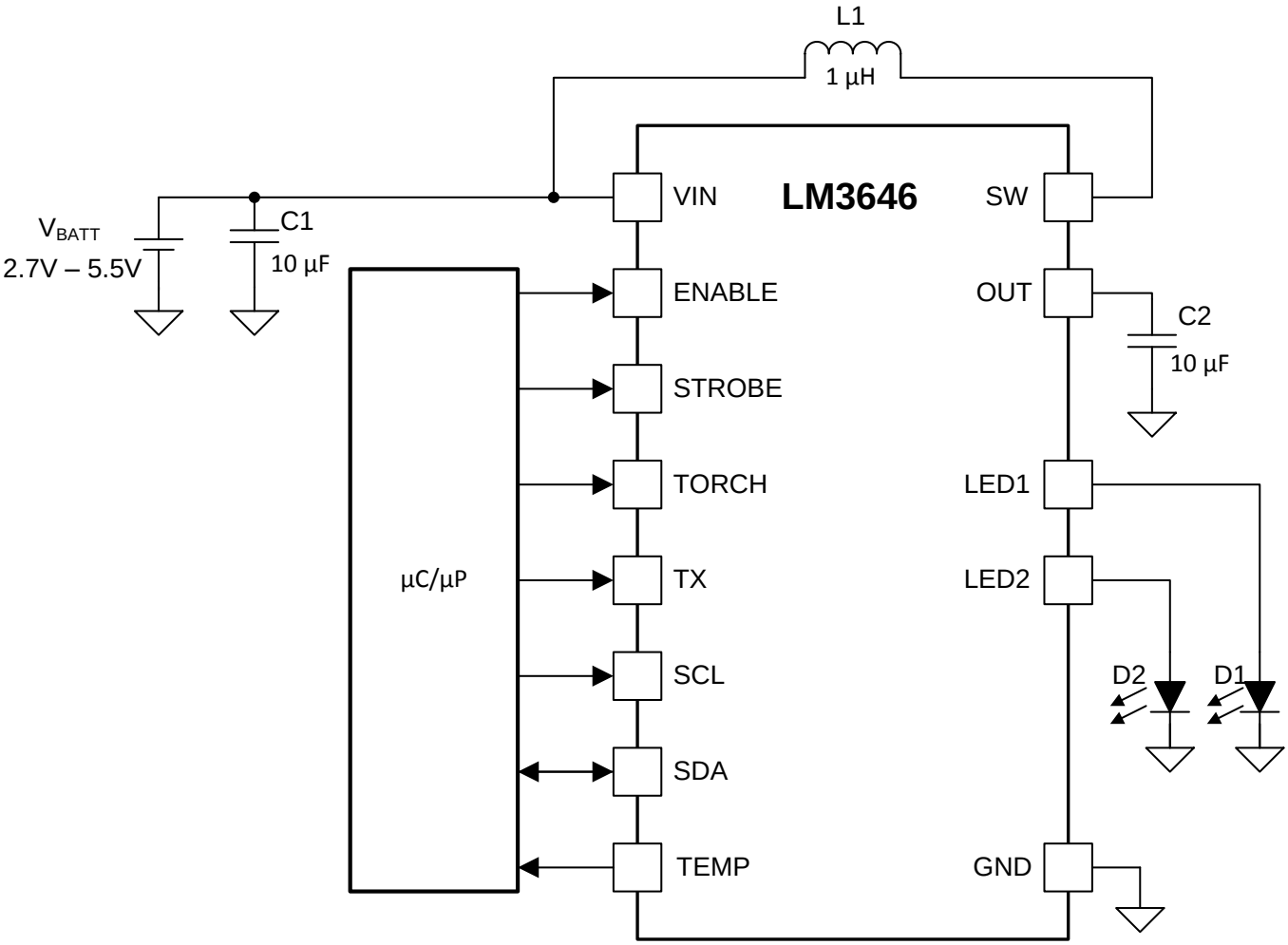

Figure 36. Typical Application Circuit

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Typical Application (continued)

8.2.1 Design Requirements

Example requirements based on default register values:

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 5.5 V
Brightness control	I^2C Register
Inductor	1-µH, 3.1-A saturation Current
LED configuration	2 Flash LEDs
Maximum flash brightness	1.5 A
Flash brightness	1.5 A on LED1, LED2 Disabled

8.2.2 Detailed Design Procedure

8.2.2.1 Output Capacitor Selection

The LM3646 is designed to operate with at least a 10-µF ceramic output capacitor. When the boost converter is running, the output capacitor supplies the load current during the boost converter's on-time. When the NMOS switch turns off, the inductor energy is discharged through the internal PMOS switch, supplying power to the load and restoring charge to the output capacitor. This causes a sag in the output voltage during the on-time and a rise in the output voltage during the off-time. The output capacitor is therefore chosen to limit the output ripple to an acceptable level depending on load current and input/output voltage differentials and also to ensure the converter remains stable.

For proper operation the output capacitor must be at least a 10-µF ceramic. Larger capacitors such as a 22-µF or capacitors in parallel can be used if lower output voltage ripple is desired. To estimate the output voltage ripple considering the ripple due to capacitor discharge (ΔVQ) and the ripple due to the capacitor's ESR (ΔVESR), use the following equations:

For continuous conduction mode, the output voltage ripple due to the capacitor discharge is:

$$\Delta V_Q = \frac{I_{LED} \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times C_{OUT}} \quad (1)$$

The output voltage ripple due to the output capacitor's ESR is found by:

$$\Delta V_{ESR} = R_{ESR} \times \left(\frac{I_{LED} \times V_{OUT}}{V_{IN}} + \Delta I_L \right)$$

where

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \quad (2)$$

In ceramic capacitors the ESR is very low so a close approximation is to assume that 80% of the output voltage ripple is due to capacitor discharge and 20% from ESR. Table 3 lists different manufacturers for various output capacitors and their case sizes suitable for use with the LM3646.

8.2.2.2 Input Capacitor Selection

Choosing the correct size and type of input capacitor helps minimize the voltage ripple caused by the switching of the LM3646 device's boost converter, and reduces noise on the boost converter's input pin that can feed through and disrupt internal analog signals. In the Figure 36 a 10-µF ceramic input capacitor works well. It is important to place the input capacitor as close as possible to the LM3646's input (IN) pin. This reduces the series resistance and inductance that can inject noise into the device due to the input switching currents. Table 3 lists various input capacitors that are recommended for use with the LM3646.

Table 3. Recommended Input/Output Capacitors (X5R Dielectric)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	VOLTAGE RATING
TDK Corporation	C1608JB0J106M	10 µF	0603 (1.6 mm × 0.8 mm × 0.8 mm)	6.3V
TDK Corporation	C2012JB1A106M	10 µF	0805 (2.0 mm × 1.25 mm × 1.25 mm)	10V

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Table 3. Recommended Input/Output Capacitors (X5R Dielectric) (continued)

MANUFACTURER	PART NUMBER	VALUE	CASE SIZE	VOLTAGE RATING
TDK Corporation	C2012JB0J226M	22 µF	0805 (2.0 mm × 1.25 mm ×1.25 mm)	6.3V
Murata	GRM21BR61A106KE19	10 µF	0805 (2.0 mm × 1.25 mm × 1.25 mm)	10V
Murata	GRM21BR60J226ME39L	22 µF	0805 (2.0 mm × 1.25 mm × 1.25 mm)	6.3V

8.2.2.3 Inductor Selection

The LM3646 is designed to use a 1 µH or 2.2 µH inductor. Table 4 lists various inductors and their manufacturers that can work well with the LM3646. When the device is boosting (V_{OUT} > V_{IN}) the inductor will typically be the largest area of efficiency loss in the circuit. Therefore, choosing an inductor with the lowest possible series resistance is important. Additionally, the saturation rating of the inductor should be greater than the maximum operating peak current of the LM3646. This prevents excess efficiency loss that can occur with inductors that operate in saturation and prevents over-heating of the inductor and further efficiency loss. For proper inductor operation and circuit performance ensure that the inductor saturation and the peak current limit setting of the LM3646 is greater than I_{PEAK} in the following calculation:

$$I_{PEAK} = \frac{I_{LOAD}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + \Delta I_L \quad \text{where} \quad \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \tag{3}$$

where f_{SW} = 4 MHz, and efficiency can be found in the *Typical Characteristics* plots.

Table 4. Recommended Inductors

MANUFACTURER	VALUE	PART NUMBER	DIMENSIONS (L×W×H)	I_{SAT}	R_{DC}
TOKO	1 µH	1286AS-H-1R0N	2.0 mm × 1.6 mm × 1.2 mm	3.1A	68 mΩ
TOKO	1 µH	1285AS-H-1R0M	2.0 mm × 1.6 mm × 1.0 mm	2.7A	80 mΩ
TDK	1 µH	TFM201610G-1R0M-T05	2.0 mm × 1.6 mm × 1.0 mm	2.9A	60 mΩ

8.2.2.4 NTC Thermistor Selection

The TEMP pin is a comparator input for flash LED thermal sensing. NTC Mode is intended to monitor an external thermistor which monitors LED temperature and prevents LED overheating. An internal comparator checks the voltage on the TEMP pin against the trip point programmed in the *NTC and Torch Ramp Register (0x03)*. The thermistor is driven by an internally regulated current source, and the voltage on the TEMP pin is related to the source current and the NTC resistance. NTC thermistors have a temperature to resistance relationship of:

$$R(T) = R_{25°C} \times e^{\left[\beta\left(\frac{1}{T\,°C + 273} - \frac{1}{298}\right)\right]} \tag{4}$$

where β is given in the thermistor datasheet and $R_{25°C}$ is the thermistor's value at 125°C.

Table 5. Application Circuit Component List

COMPONENT	MANUFACTURER	VALUE	PART NUMBER	SIZE	CURRENT/VOLTAGE RATING (RESISTANCE)
L	TOKO	1 µH	1286AS-H-1R0N	2.0 mm x 1.6 mm x 1.2 mm	I_{SAT} = 3.1 A (68 mΩ)
COUT1,2	Murata	10 µF	GRM188R60J106M	1.6 mm x 0.8 mm x 0.8 mm (0603)	6.3 V
CIN1,2	Murata	10 µF	GRM188R60J106M	1.6 mm x 0.8 mm x 0.8 mm (0603)	6.3 V

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8.2.3 Application Curves

Unless otherwise specified: T_A= 25°C; V_{IN} = 3.6 V; V_{EN} = V_{IN}; C_{IN} = 10 µF; C_{OUT} = 10 µF; L = 1 µH.

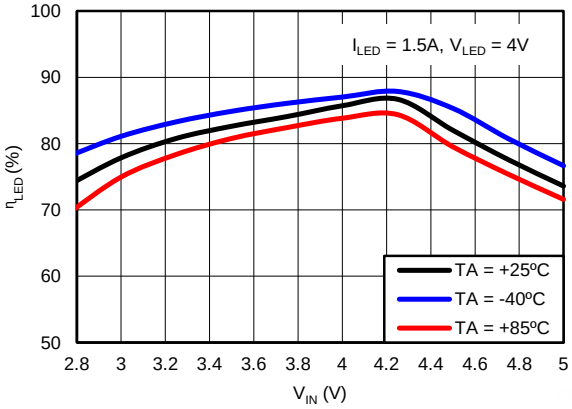


Figure 37. Flash LED Efficiency vs. Input Voltage

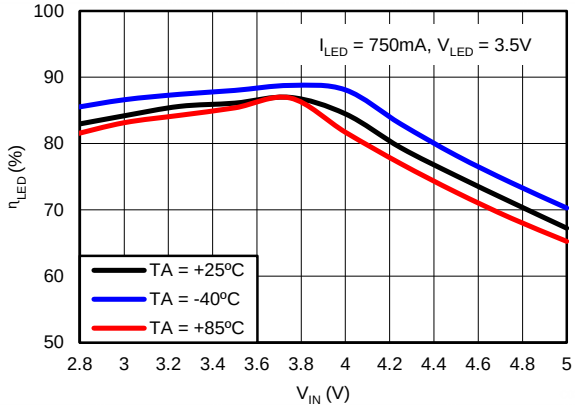


Figure 38. Flash LED Efficiency vs. Input Voltage

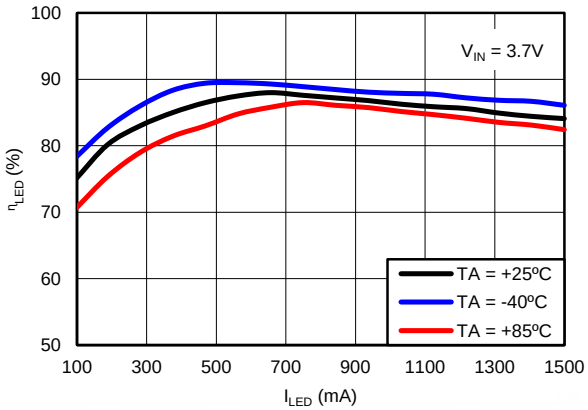


Figure 39. Flash LED Efficiency vs. LED Current

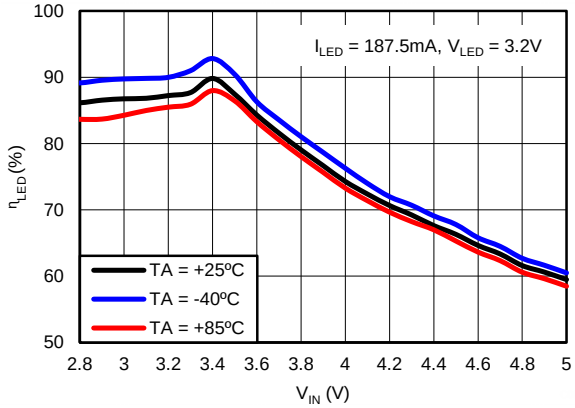


Figure 40. Torch LED Efficiency vs. Input Voltage

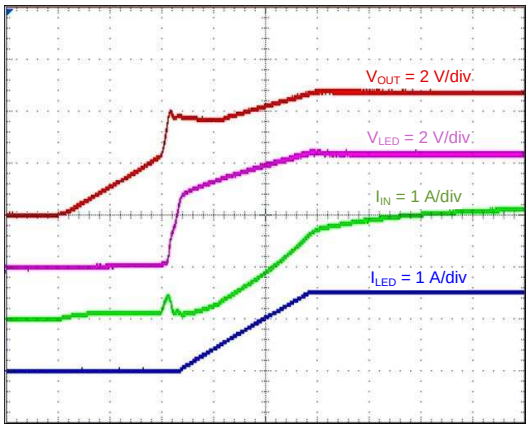


Figure 41. Flash Ramp-Up

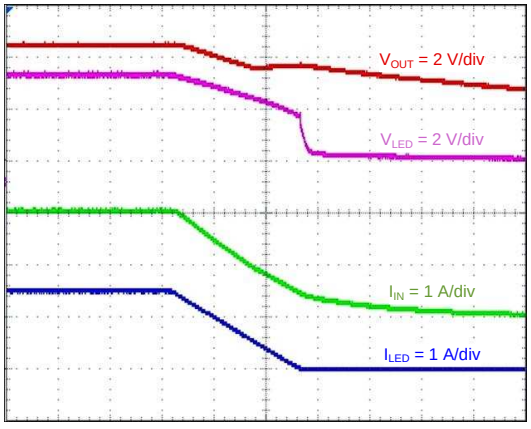
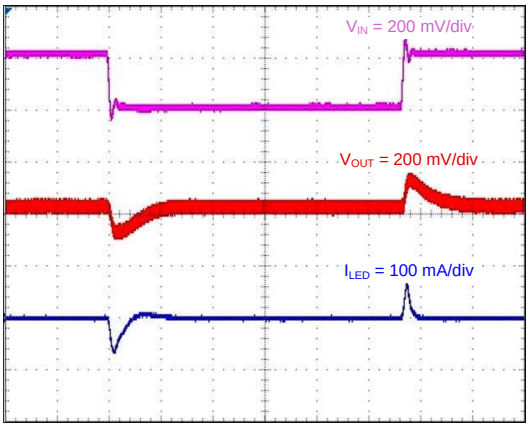


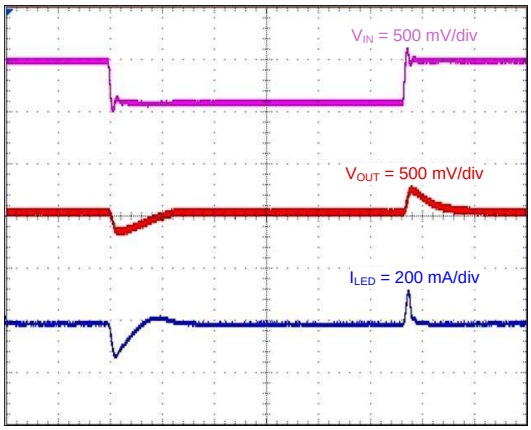
Figure 42. Flash Ramp-Down

Unless otherwise specified: T_A= 25°C; V_{IN} = 3.6 V; V_{EN} = V_{IN}; C_{IN} = 10 µF; C_{OUT} = 10 µF; L = 1 µH.



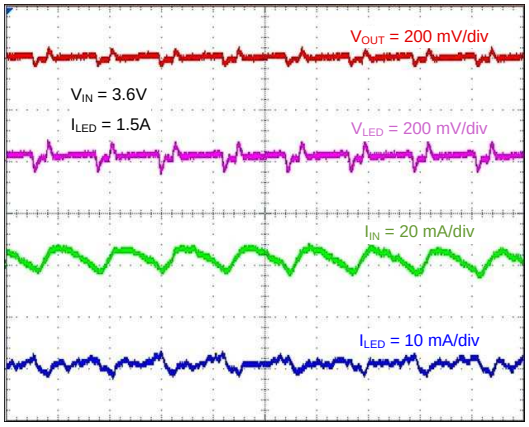
t – Time Base – 40 µs/div

Figure 43. Line-step (200 mV) During Flash



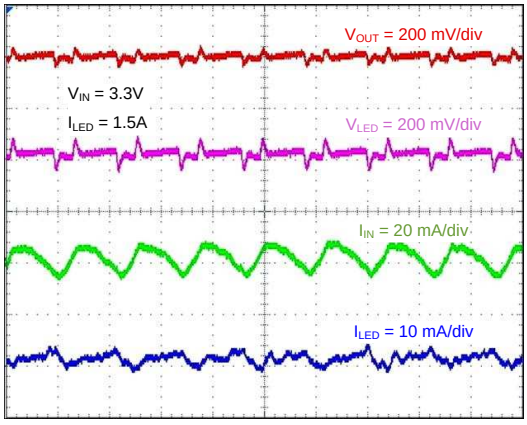
t – Time Base – 40 µs/div

Figure 44. Line-step (400 mV) During Flash



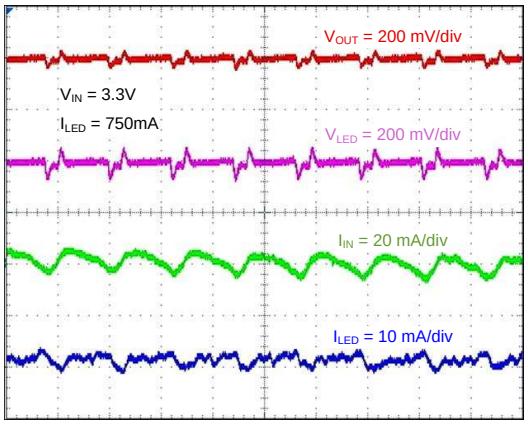
t – Time Base – 200 ns/div

Figure 45. LED Current Ripple



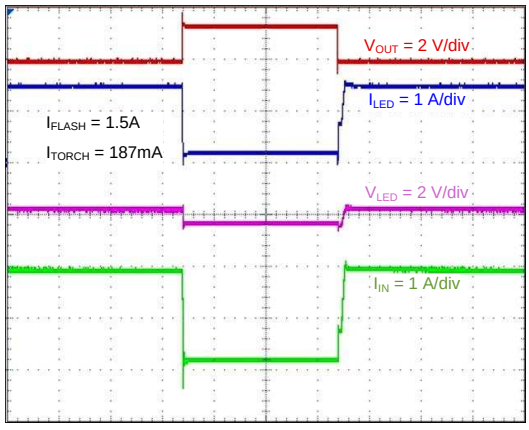
t – Time Base – 200 ns/div

Figure 46. LED Current Ripple



t – Time Base – 200 ns/div

Figure 47. LED Current Ripple



t – Time Base – 1 ms/div

Figure 48. TX-Mask Event, Default Settings

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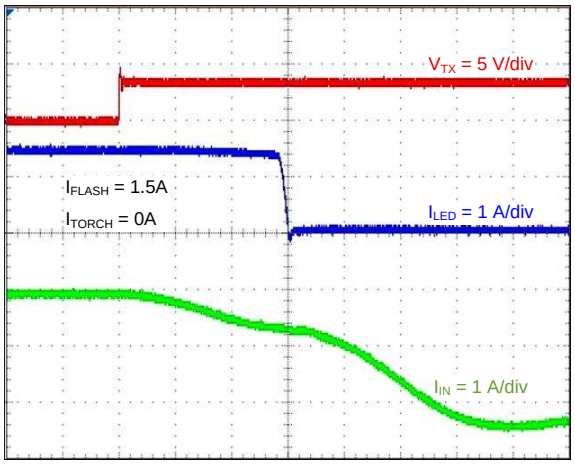
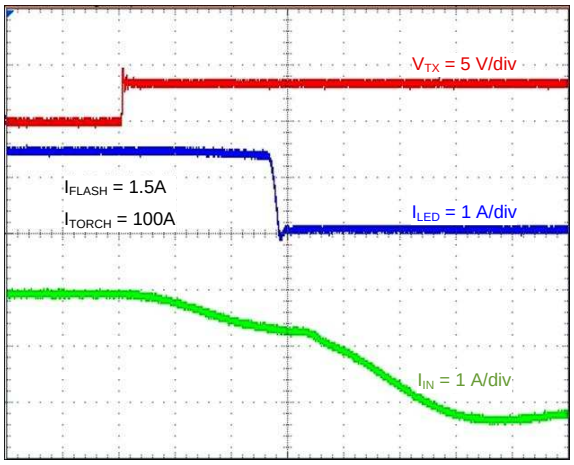
Unless otherwise specified: T_A= 25°C; V_{IN} = 3.6 V; V_{EN} = V_{IN}; C_{IN} = 10 µF; C_{OUT} = 10 µF; L = 1 µH.



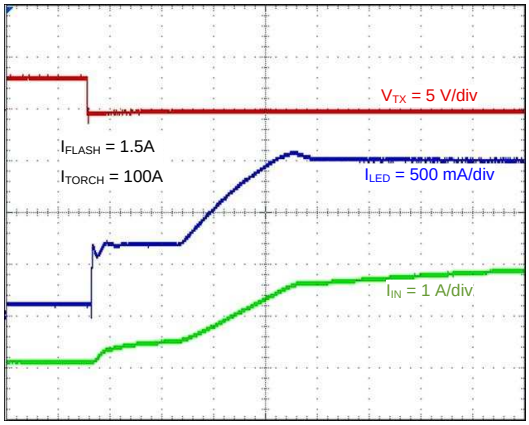
t – Time Base – 1 µs/div

Figure 49. TX Signal Low-to-High Transition



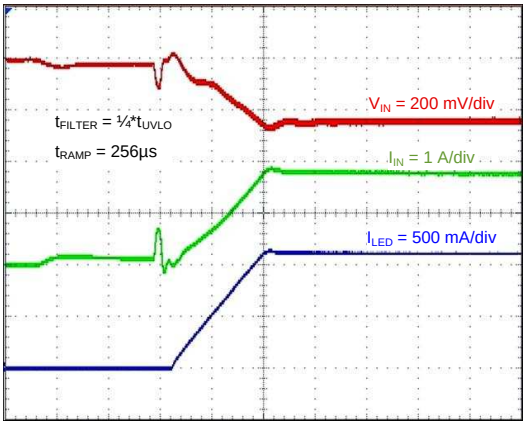
t – Time Base – 1 µs/div

Figure 50. TX Signal Low-to-High Transition



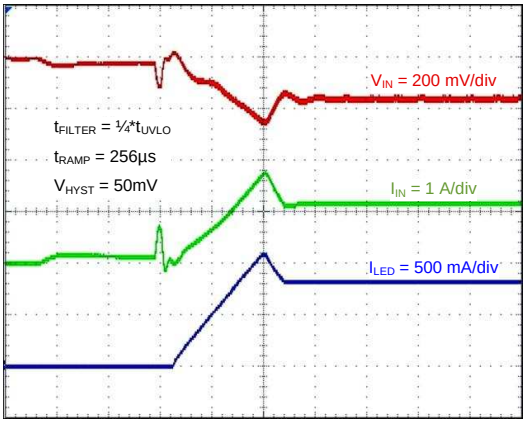
t – Time Base – 40 µs/div

Figure 51. TX Signal High-to-Low Transition



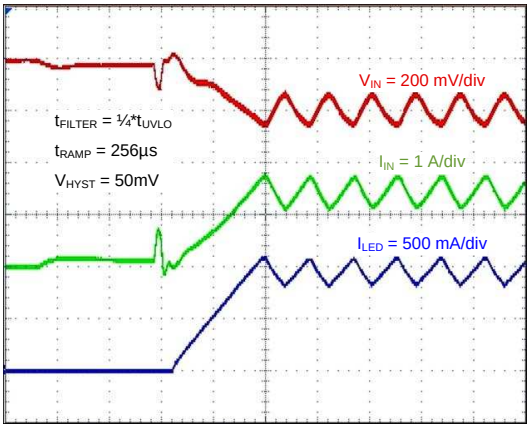
t – Time Base – 100 µs/div

Figure 52. Input Voltage Flash Monitor, Stop & Hold Mode, Default settings



t – Time Base – 100 µs/div

Figure 53. Input Voltage Flash Monitor, Down Mode, Default Settings



t – Time Base – 100 µs/div

Figure 54. Input Voltage Flash Monitor, Up & Down Mode, Default Settings

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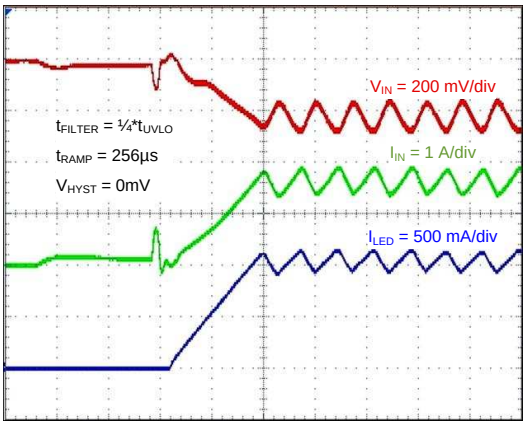
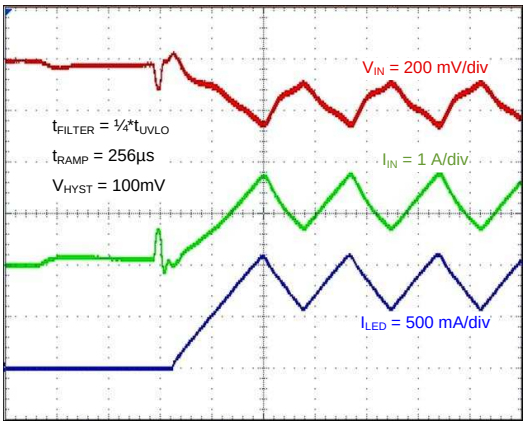
Unless otherwise specified: T_A= 25°C; V_{IN} = 3.6 V; V_{EN} = V_{IN}; C_{IN} = 10 µF; C_{OUT} = 10 µF; L = 1 µH.



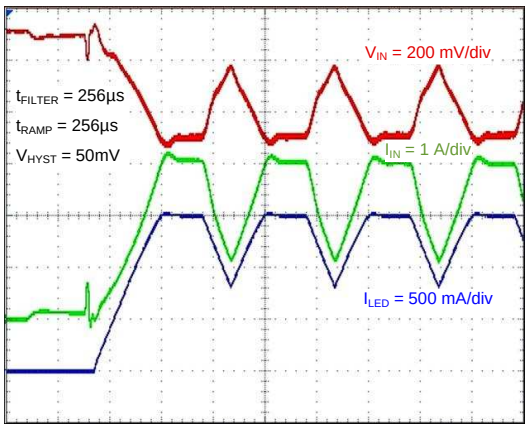
t – Time Base – 100 µs/div

Figure 55. Input Voltage Flash Monitor, Up & Down Mode,



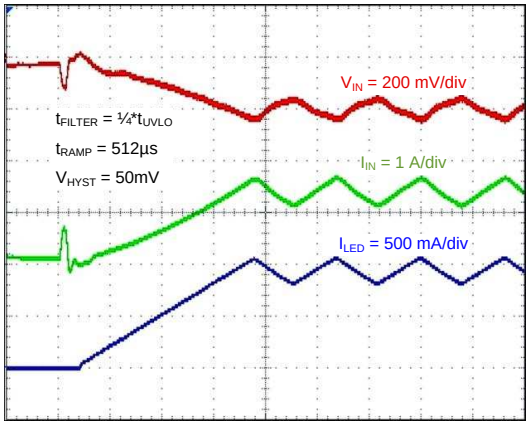
t – Time Base – 100 µs/div

Figure 56. Input Voltage Flash Monitor, Up & Down Mode,



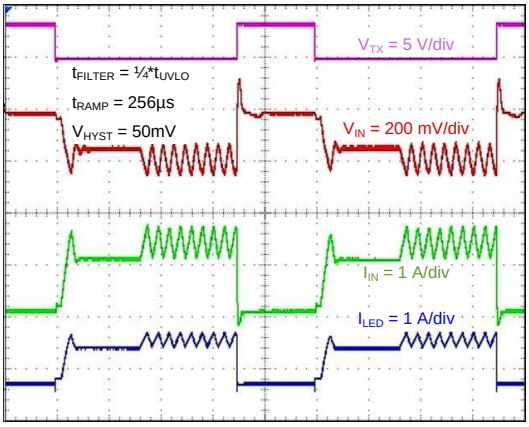
t – Time Base – 200 µs/div

Figure 57. Input Voltage Flash Monitor, Up & Down Mode



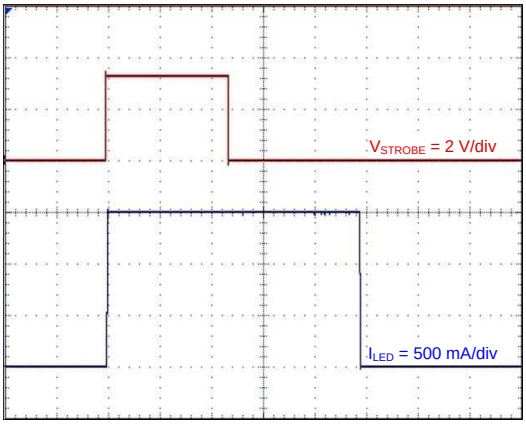
t – Time Base – 100 µs/div

Figure 58. Input Voltage Flash Monitor, Up & Down Mode



t – Time Base – 400 µs/div

Figure 59. Input Voltage Flash Monitor, Up & Down Mode with TX Event



t – Time Base – 20 ms/div

Figure 60. Edge-Sensitive Strobe

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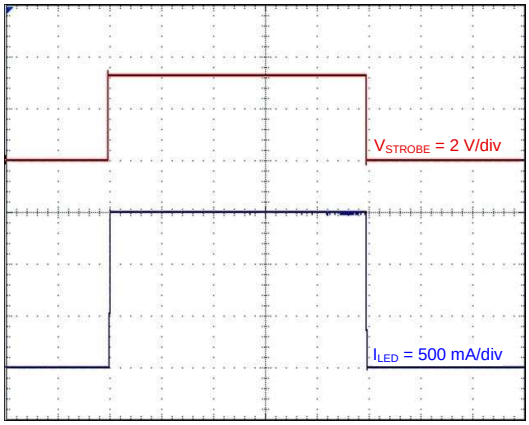
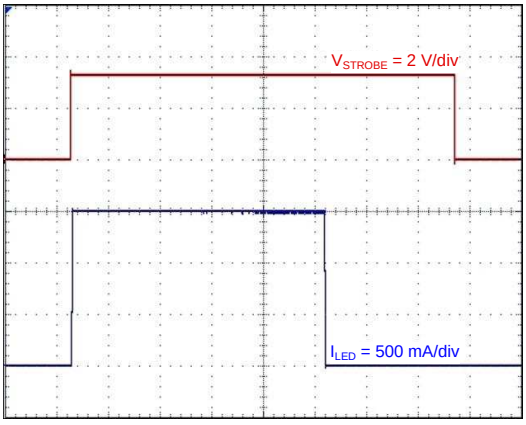
Unless otherwise specified: T_A= 25°C; V_{IN} = 3.6 V; V_{EN} = V_{IN}; C_{IN} = 10 µF; C_{OUT} = 10 µF; L = 1 µH.



t – Time Base – 20 ms/div

Figure 61. Level-Sensitive Strobe without Timeout



t – Time Base – 20 ms/div

Figure 62. Level-Sensitive Strobe with Timeout

9 Power Supply Recommendations

The LM3646 is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the LM3646 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

The high switching frequency and large switching currents of the LM3646 make the choice of layout important. The following steps should be used as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range.

1. Place C_{IN} on the top layer (same layer as the LM3646) and as close to the device as possible. The input capacitor conducts the driver currents during the low-side MOSFET turn-on and turn-off and can see current spikes over 1 A in amplitude. Connecting the input capacitor through short, wide traces to both the IN and GND pins will reduce the inductive voltage spikes that occur during switching and which can corrupt the V_{IN} line.
2. Place C_{OUT} on the top layer (same layer as the LM3646) and as close as possible to the OUT and GND pins. The returns for both C_{IN} and C_{OUT} should come together at one point, as close to the GND pin as possible. Connecting C_{OUT} through short, wide traces will reduce the series inductance on the OUT and GND pins that can corrupt the OUT and GND lines and cause excessive noise in the device and surrounding circuitry.
3. Connect the inductor on the top layer close to the SW pin. There should be a low-impedance connection from the inductor to SW due to the large DC inductor current, and at the same time, the area occupied by the SW node should be small to reduce the capacitive coupling of the high dV/dt present at SW that can couple into nearby traces.
4. Avoid routing logic traces near the SW node to avoid any capacitively coupled voltages from SW onto any high impedance logic lines such as TORCH, STROBE, ENABLE, TEMP, TX, SDA and SCL. A good approach is to insert an inner layer GND plane underneath the SW node and between any nearby routed traces. This creates a shield from the electric field generated at SW.
5. Terminate the Flash LED cathodes directly to the GND pin of the LM3646. If possible, route the LED returns with a dedicated path to keep the high amplitude LED currents out of the GND plane. For Flash LEDs that are routed relatively far away from the LM3646, a good approach is to sandwich the forward and return current paths over the top of each other on two layers. This will help in reducing the inductance of the LED current paths.

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10.2 Layout Example

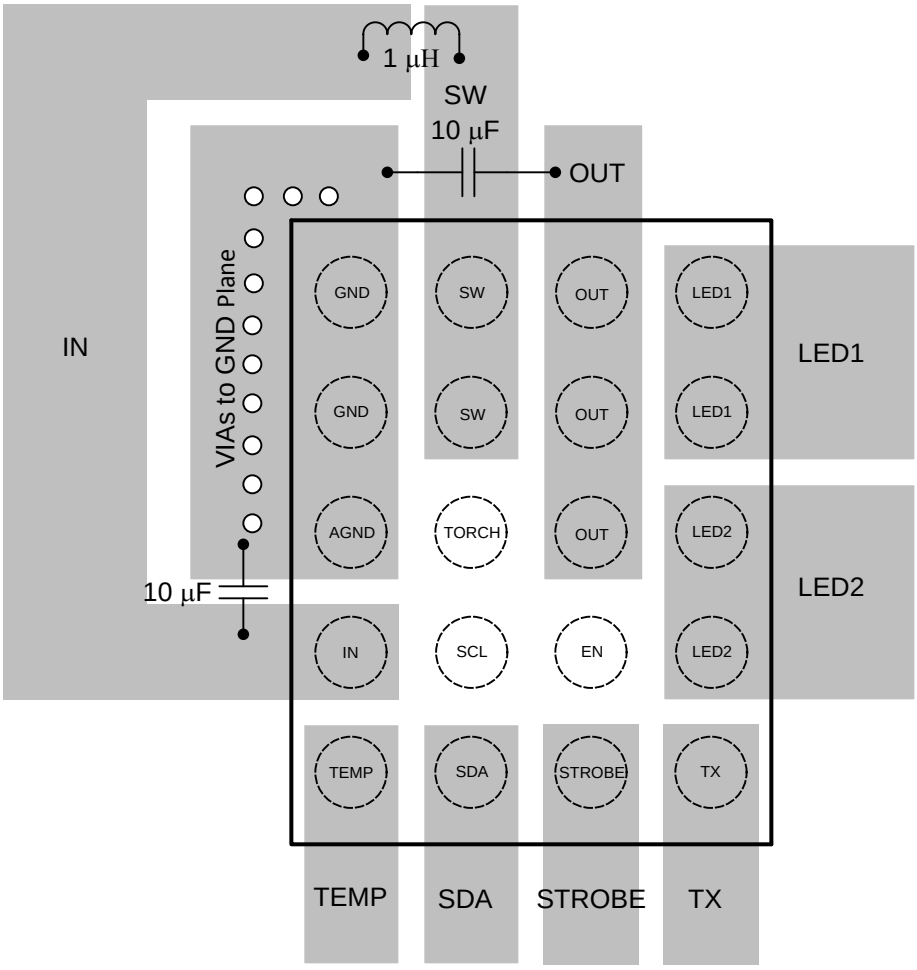

Figure 63. LM3646 Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments Application Note 1112: *DSBGA Wafer Level Chip Scale Package* (SNVA009).

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3646YFQR	ACTIVE	DSBGA	YFQ	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3646	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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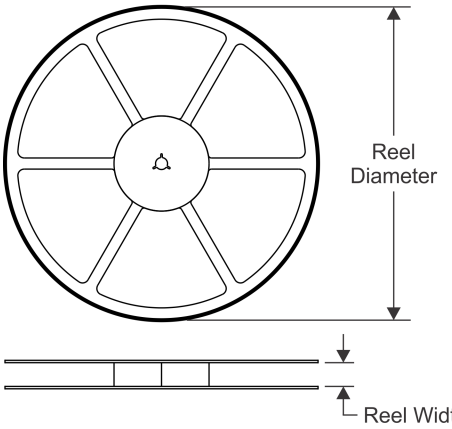
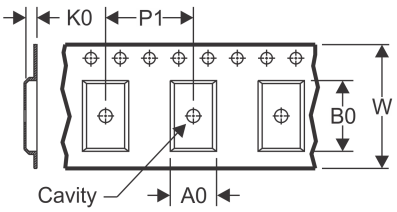
TAPE AND REEL INFORMATION

REEL DIMENSIONS

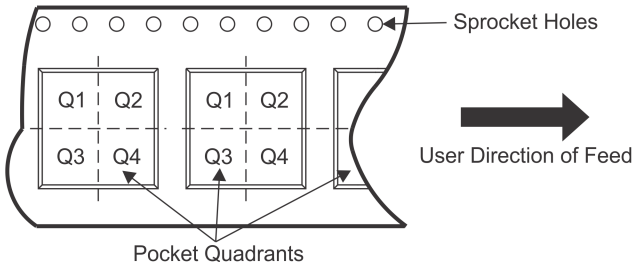


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

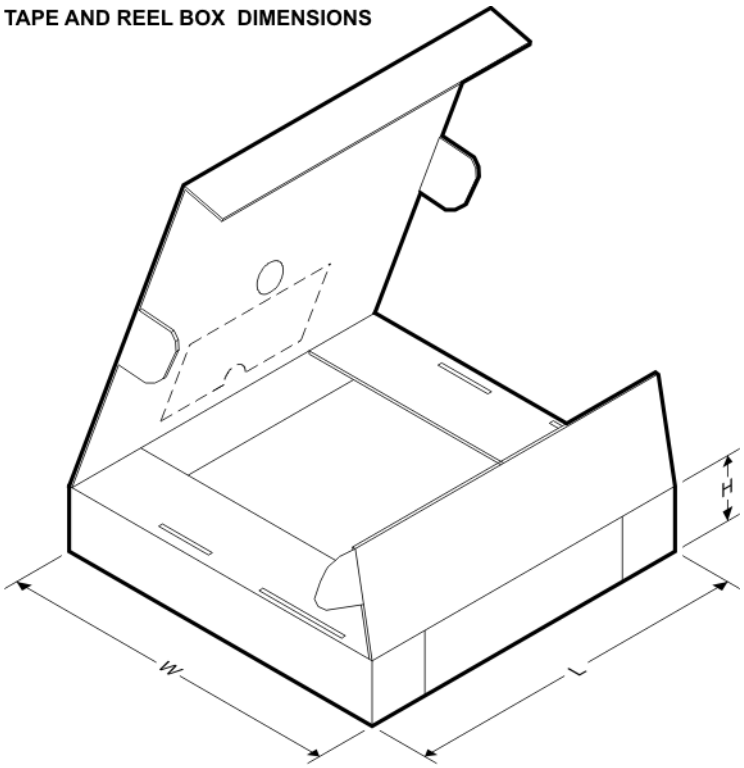
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3646YFQR	DSBGA	YFQ	20	3000	178.0	8.4	1.78	2.2	0.78	4.0	8.0	Q1

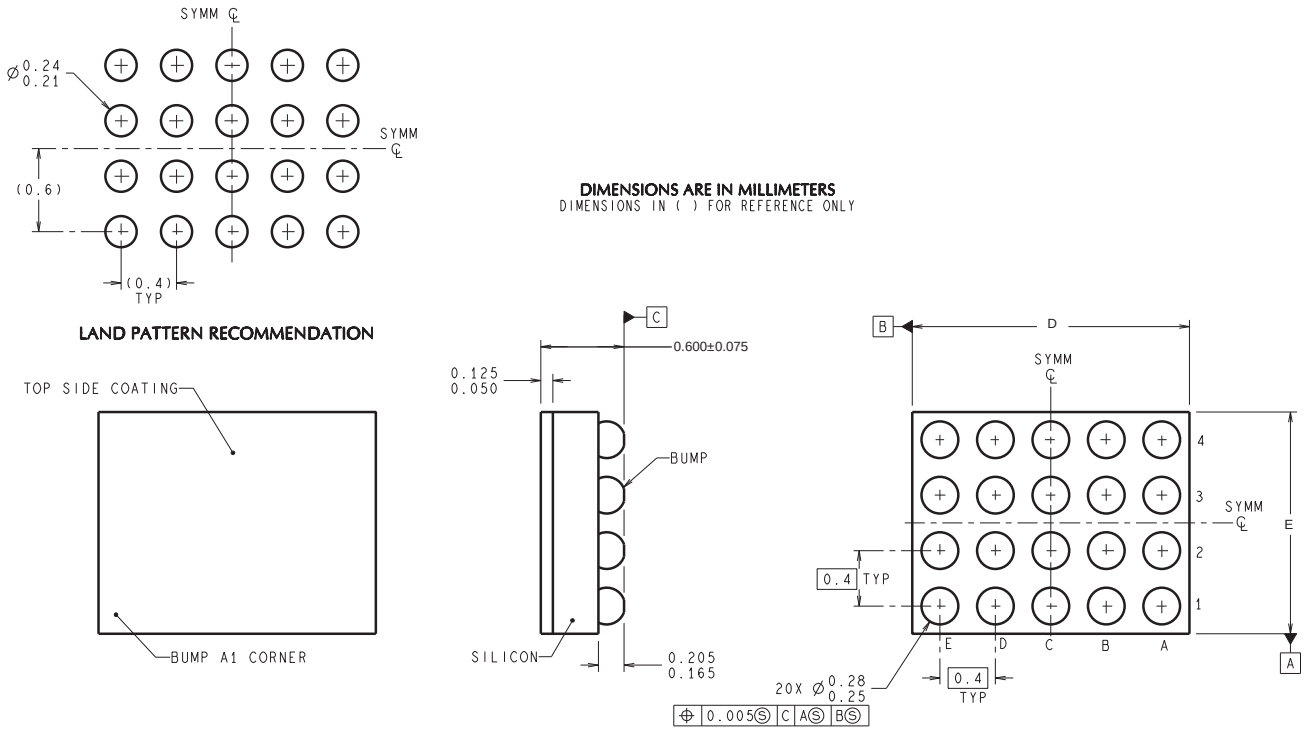
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3646YFQR	DSBGA	YFQ	20	3000	220.0	220.0	35.0

YFQ0020



D: Max = 2.04 mm, Min = 1.98 mm

E: Max = 1.64 mm, Min = 1.58 mm

4215083/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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