THE DATASHEET OF

LM360N

LM160/LM360 High Speed Differential Comparator

Check for Samples: LM160, LM360

FEATURES

- **Ensured high speed: 20 ns max**
- **Tight delay matching on both outputs**
- **Complementary TTL outputs**
- **High input impedance**
- **Low speed variation with overdrive variation**
- **Fan-out of 4**
- **Low input offset voltage**
- **Series 74 TTL compatible**

DESCRIPTION

The LM160/LM360 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the μA760/μA760C, for which it is a pin-for-pin replacement. The device has been optimized for greater speed, input impedance and fan-out, and lower input offset voltage. Typically delay varies only 3 ns for overdrive variations of 5 mV to 400 mV.

Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital convertors and zero-crossing detectors in disk file systems.

CONNECTION DIAGRAMS

TO-99 Package

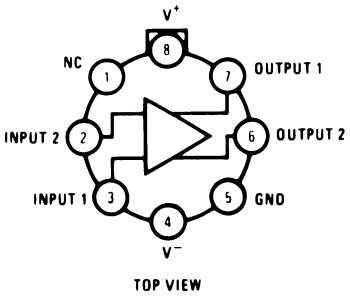


Figure 1. Package Number LMC0008C (1)

SOIC or PDIP Package

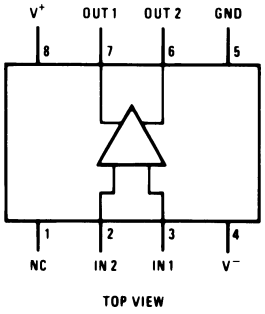


Figure 2. Package Number D0008A or P0008E

(1) Also available in SMD# 5962-8767401

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Positive Supply Voltage		+8V
Negative Supply Voltage		−8V
Peak Output Current		20 mA
Differential Input Voltage		±5V
Input Voltage		$V^+ \geq V_{IN} \geq V^-$
ESD Tolerance (3)		1600V
Operating Temperature Range	LM160	−55°C to +125°C
	LM360	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature	(Soldering, 10 sec.)	260°C
Soldering Information		
PDIP Package	Soldering (10 seconds)	260°C
SOIC Package	Vapor Phase (60 seconds)	215°C
	Infrared (15 seconds)	220°C
See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.		

(1) The device may be damaged if used beyond the maximum ratings.
(2) Refer to RETS 160X for LM160H, LM160J-14 and LM160J military specifications.
(3) Human body model, 1.5 kΩ in series with 100 pF.

Electrical Characteristics

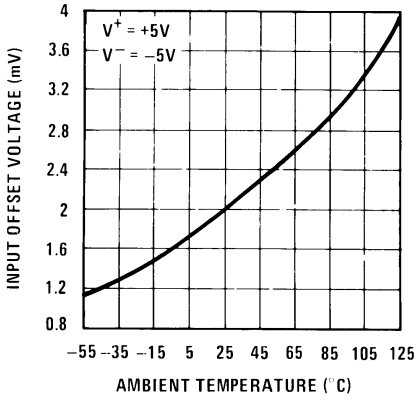
($T_{MIN} \le T_A \le T_{MAX}$)

Parameter	Conditions	Min	Typ	Max	Units
Operating Conditions					
Supply Voltage V_{CC}^+		4.5	5	6.5	V
Supply Voltage V_{CC}^-		−4.5	−5	−6.5	V
Input Offset Voltage	$R_S \le 200\Omega$		2	5	mV
Input Offset Current			0.5	3	µA
Input Bias Current			5	20	µA
Output Resistance (Either Output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	T_A = 25°C, V_S = ±5V (1) (2)		13	25	ns
	T_A = 25°C, V_S = ±5V (3) (2)		12	20	ns
	T_A = 25°C, V_S = ±5V (4) (2)		14		ns
Response Time Difference between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	T_A = 25°C (1) (2)		2		ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$)	T_A = 25°C (1) (2)		2		ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	T_A = 25°C (1) (2)		2		ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	T_A = 25°C (1) (2)		2		ns
Input Resistance	f = 1 MHz		17		kΩ
Input Capacitance	f = 1 MHz		3		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		8		µV/°C
Average Temperature Coefficient of Input Offset Current			7		nA/°C
Common Mode Input Voltage Range	V_S = ±6.5V	±4	±4.5		V
Differential Input Voltage Range		±5			V
Output High Voltage (Either Output)	I_{OUT} = −320 µA, V_S = ±4.5V	2.4	3		V
Output Low Voltage (Either Output)	I_{SINK} = 6.4 mA		0.25	0.4	V
Positive Supply Current	V_S = ±6.5V		18	32	mA
Negative Supply Current	V_S = ±6.5V		−9	−16	mA

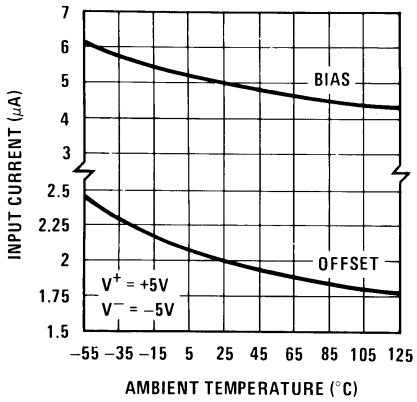
(1) Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.
(2) Measurements are made in AC Test Circuit, Fanout = 1
(3) Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.
(4) Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

Typical Performance Characteristics

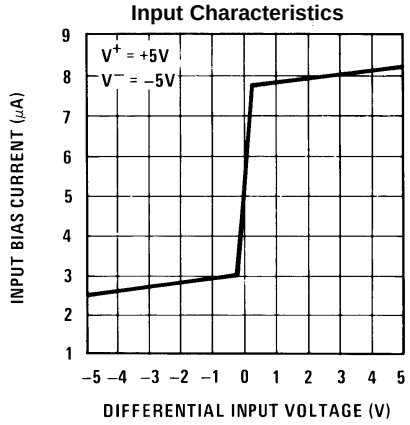
Offset Voltage



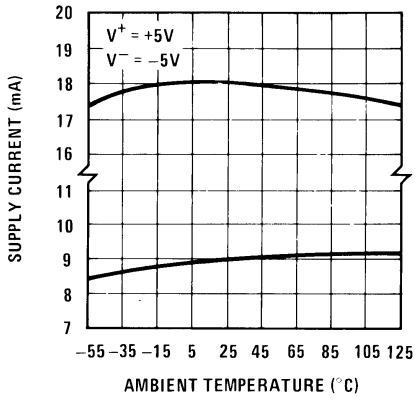
Input Current vs Ambient Temperature



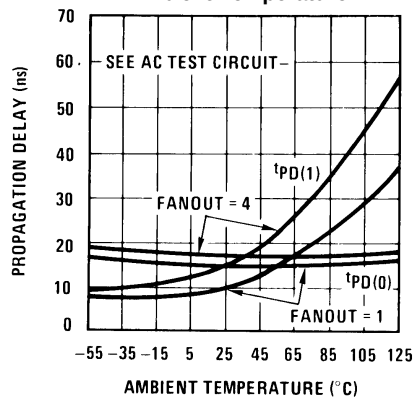
Input Characteristics



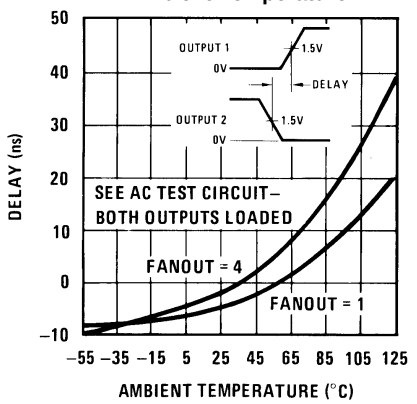
Supply Current vs Ambient Temperature



Propagation Delay vs Ambient Temperature

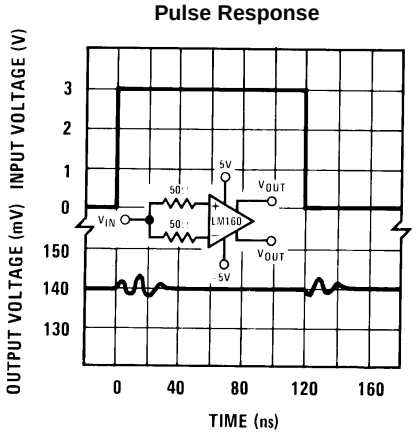


Delay of Output 1 With Respect to Output 2 vs Ambient Temperature

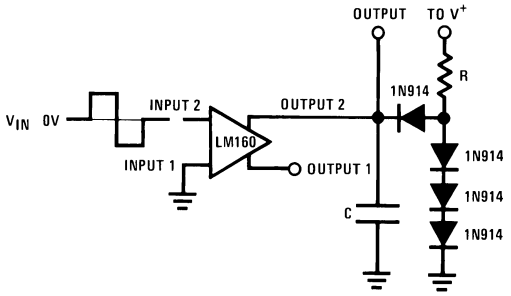


Typical Performance Characteristics (continued)

Common-Mode Pulse Response

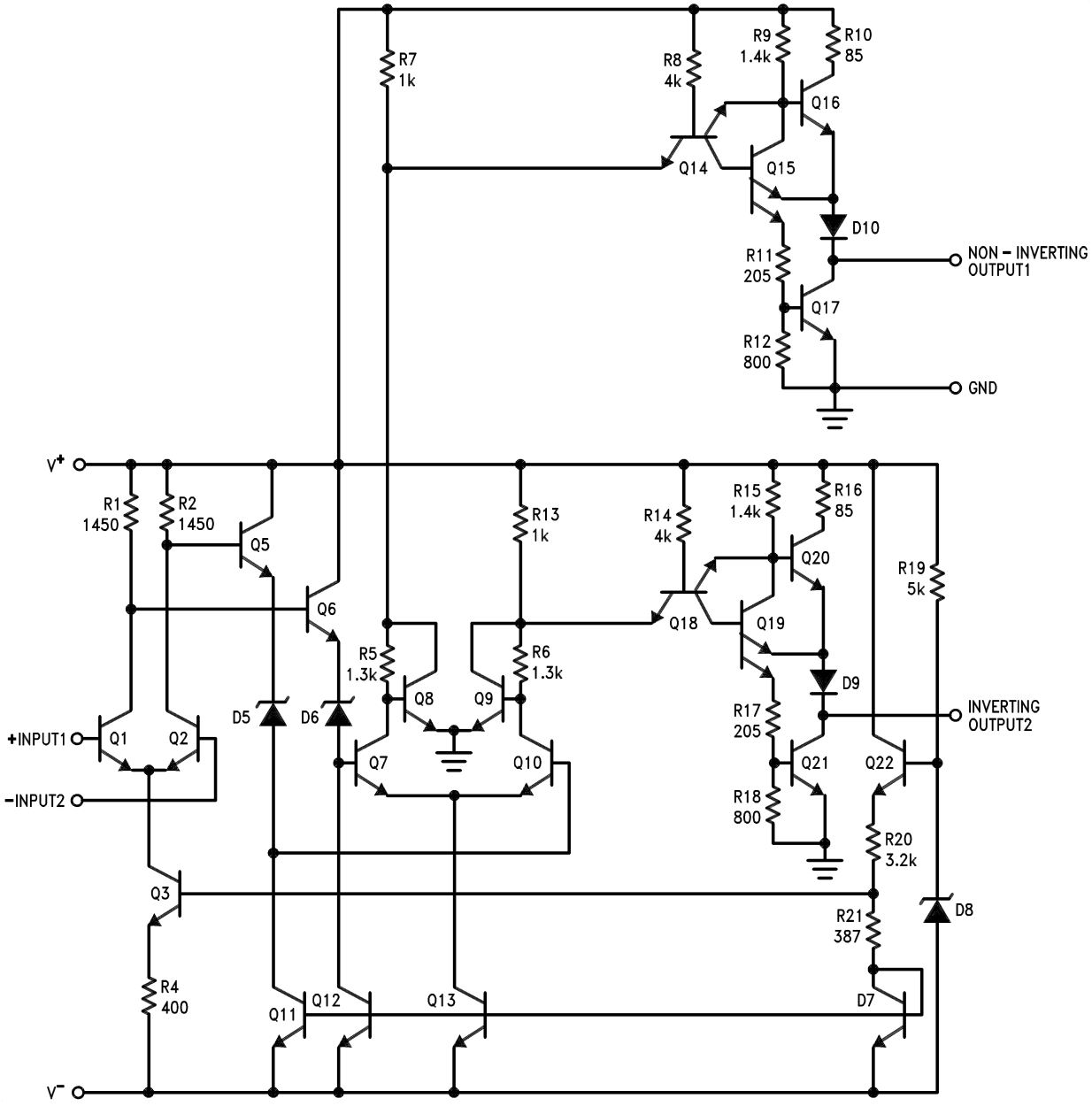


AC TEST CIRCUIT



V_{IN}=±50 mV	FANOUT=1	FANOUT=4
V^+=+5V	R=2.4k	R=630Ω
V^-=−5V	C=15 pF	C=30 pF

SCHEMATIC DIAGRAM



REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM360M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM 360M	
LM360M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM 360M	Samples
LM360MX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70	LM 360M	
LM360MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM 360M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

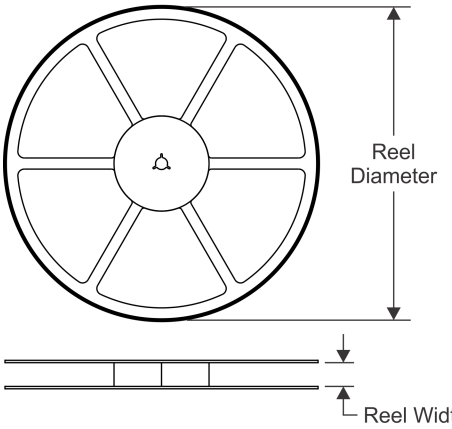
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

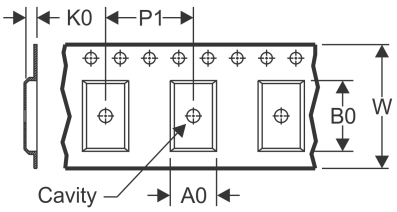
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

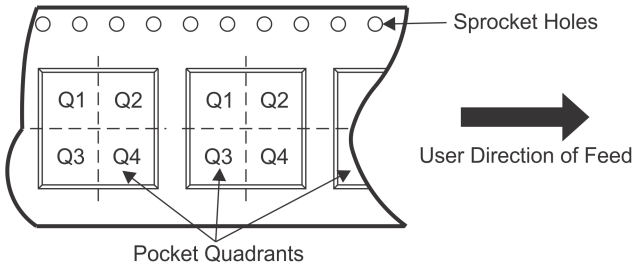


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

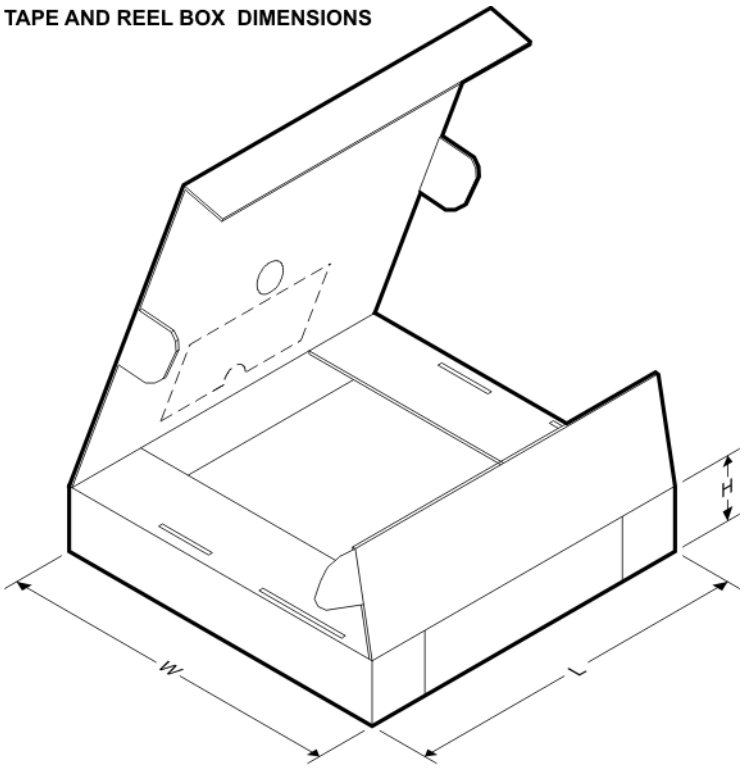
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

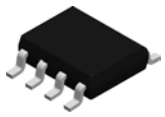
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM360MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM360MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM360MX	SOIC	D	8	2500	367.0	367.0	35.0
LM360MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

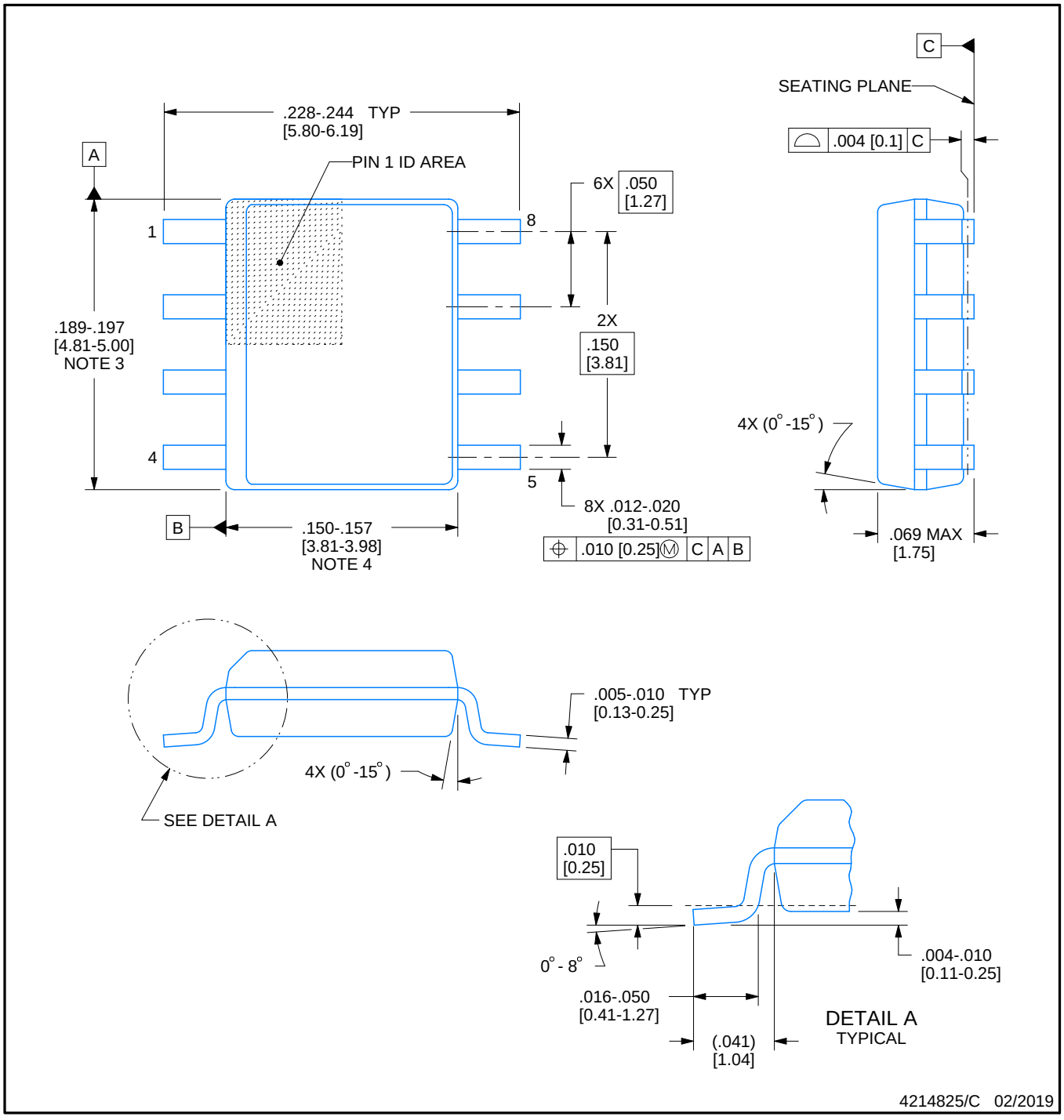


PACKAGE OUTLINE

D0008A

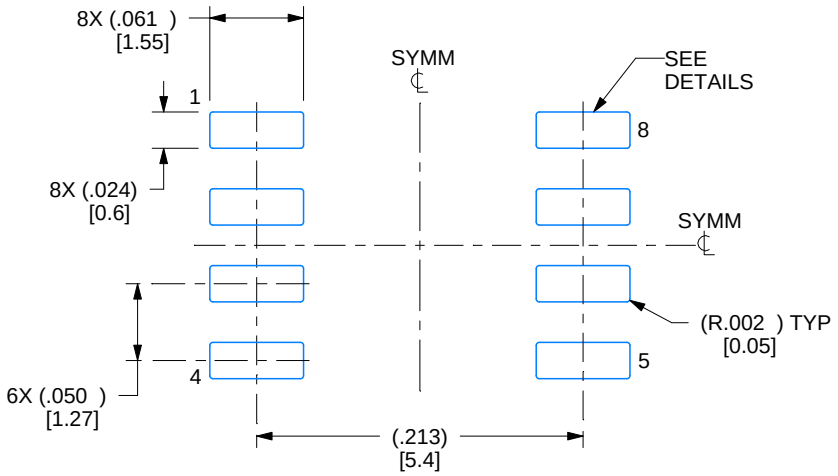
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

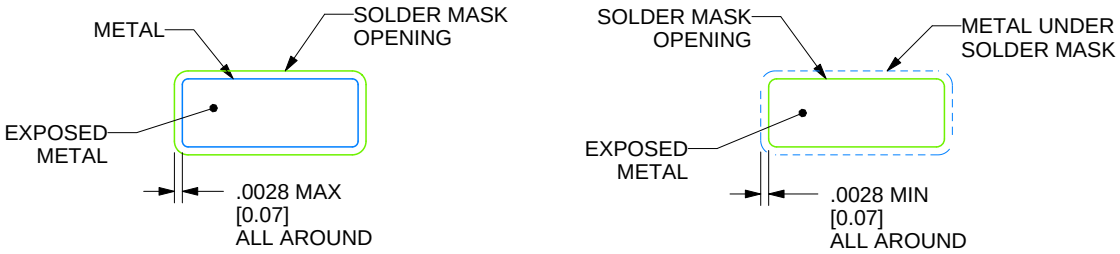


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

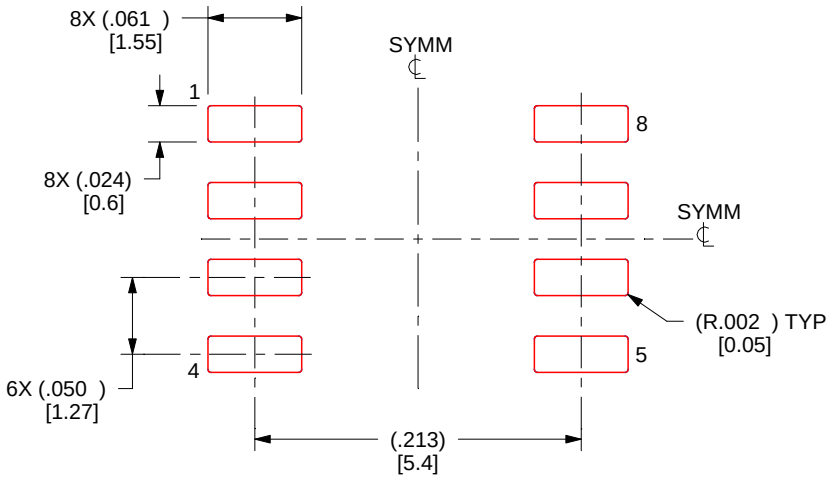
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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