THE DATASHEET OF

LM3549SQX/NOPB

LM3549 High Power Sequential LED Driver

Check for Samples: LM3549

FEATURES

- **Over-Current Protection**
- **Over-Temperature Protection**
- **I²C Compatible Interface**
- **Under-Voltage Lockout**
- **LED Open and Short Protection and Detection**
- **95% Peak Efficiency Buck-Boost Converter**
- **NVM Memory for Calibration Data and Standalone Usage without I²C Control**
- **Soft Start**

APPLICATIONS

- **Portable Video Projectors**
- **High Power LED Driving**

KEY SPECIFICATIONS

- **Integrated buck-boost Converter**
- **Programmable LED Drivers**
- **700 mA Maximum Drive Current**
- **±6% Current Accuracy Over Temperature**
- **24-pin WQFN Package**

DESCRIPTION

The LM3549 is a high power LED driver with up to 700mA output current. It has three constant current LED drivers and a buck boost SMPS for driving RGB LEDs with high efficiency. LED drivers are designed for sequential drive so only one driver can be enabled at a time.

LED driver output current settings can be stored to integrated non-volatile memory which allows stand-alone operation without I²C interface. Non-volatile memory is rewritable so current setting can be changed if needed.

The LM3549 has a fault detection feature that can detect several different fault conditions. In case of a fault error flags are set and FAULT output sends interrupt to control logic. Error flags can be read through I²C interface.

Total brightness can be controlled with PWM input or with master fader register if I²C interface is used.

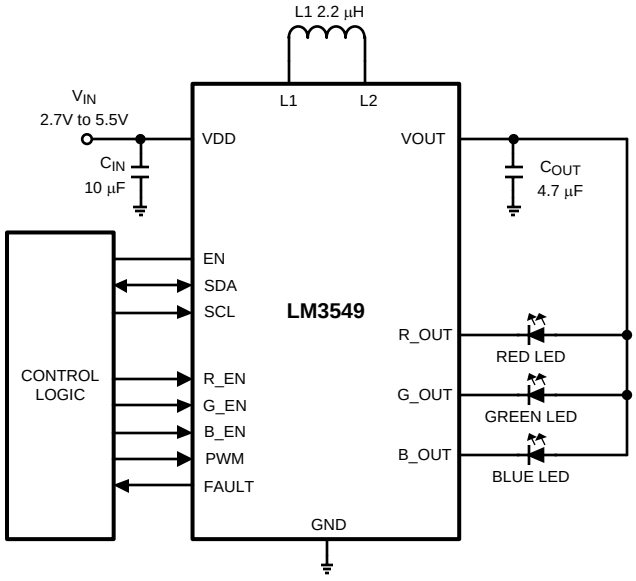

Figure 1. Typical Application Circuit

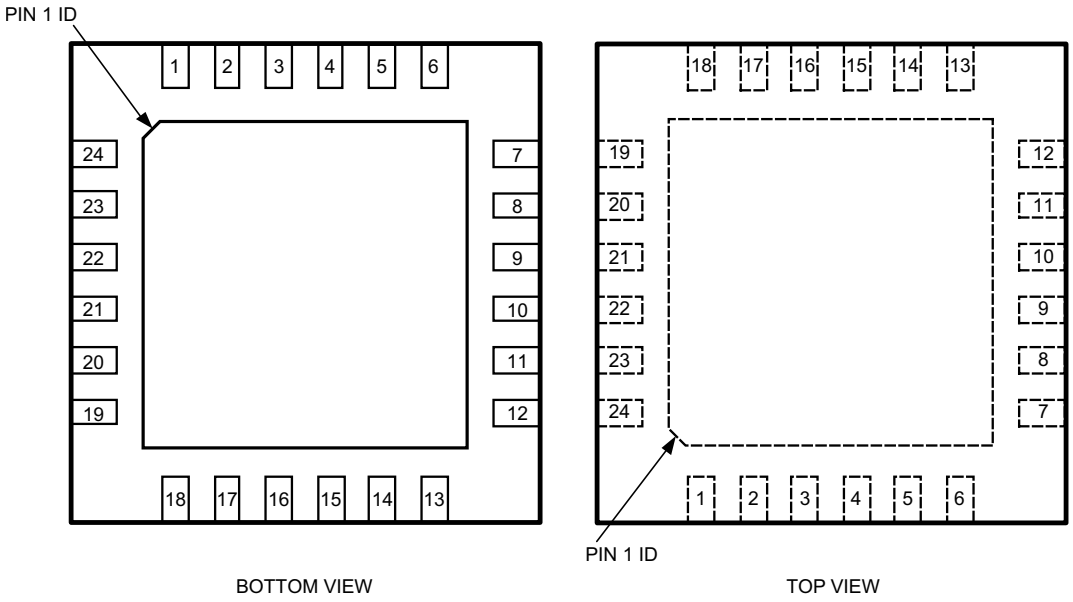

Figure 2. 24–Pin WQFN Package, No Pullback
See package number RTW0024A

Pin Descriptions

Name	Pin No.	Type	Description
NC	1		
L1	2	A	Inductor positive terminal 1
L1	3	A	Inductor positive terminal 2
GND_SW	4	G	SMPS ground
L2	5	A	Inductor negative terminal 1
L2	6	A	Inductor negative terminal 2
VOUT	7	A	Buck boost output terminal 1
NC	8		
VOUT	9	A	Buck boost output terminal 2
R_EN	10	DI	Red output enable
VDDS	11	P	Supply voltage
G_EN	12	DI	Green output enable
B_EN	13	DI	Blue output enable
PWM	14	DI	Master fader input
GND	15	G	Ground
R_OUT	16	A	R output
G_OUT	17	A	G output
B_OUT	18	A	B output
FAULT	19	DO	Fault detection interrupts output. Active LOW open drain output.
SDA	20	DI/O	I2C Data
SCL	21	DI	I2C Clock
EN	22	DI	Enable and IO reference level
VDDP	23	P	SMPS supply voltage
NC	24		

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2) (3)

VDD and VOUT pins	−0.3V to 6.0V
Voltage on all other pins	−0.3V (V_{IN}+0.3V) w/6.0V max
Continuous Power Dissipation (4)	Internally Limited
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering)	(5)
ESD Rating (6)	
Human Body Model	2.0kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=+150°C (typ.) and disengages at T_J=+140°C (typ.).
(5) For detailed soldering specifications and information, please refer to **Application Note AN-1187**: *Leadless Leadframe Package (LLP).*(SNOA401)
(6) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7)

Operating Ratings (1) (2)

Input Voltage Range	2.7V to 5.5V
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range (3)	−30°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply performance limits. For performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high-power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), WQFN-24 Package (1)	35 - 50°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Electrical Characteristics (1) (2)

Limits in standard type face are for T_A = 25°C. Limits in **boldface type** apply over the full operating ambient temperature range (−30°C ≤ T_A ≤ +85°C). Unless otherwise noted, specifications apply to Figure 1 with: V_{IN} = 3.6V, C_{IN} = 10 µF, C_{OUT} = 4.7µF and L1 = 2.2 µH. (3)

Parameter		Test Conditions	Min	Typ	Max	Units
V_{IN}	Supply voltage	Minimum voltage for startup	2.7			V
		Full output power	3.1		5.5	
I_{IN} (IVDDP + IVDDS)	Shutdown supply current	EN low			1	µA
	Standby supply current	EN High, x_EN low		0.4	1	mA
I_{IN} (IVDDS)	Active mode supply current	EN High, x_EN high, RGB outputs open		1.6	3	mA

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test, or statistical analysis. Typical (Typ) numbers represent the most likely norm.
(3) C_{IN}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

Electrical Characteristics[1] [2] (continued)

Limits in standard type face are for T_A = 25°C. Limits in **boldface type** apply over the full operating ambient temperature range (−30°C ≤ T_A ≤ +85°C). Unless otherwise noted, specifications apply to Figure 1 with: V_{IN} = 3.6V, C_{IN} = 10 µF, C_{OUT} = 4.7µF and L1 = 2.2 µH. [3]

Parameter		Test Conditions	Min	Typ	Max	Units
Drivers (R_OUT, G_OUT, B_OUT)						
$I_{OUT\ MIN}$	Minimum output current		97	107	118	mA
$I_{OUT\ MAX}$	Maximum output current		690	705	720	mA
I_{LIM}	Current limit				15	%
R_{OUT}	Driver on resistance	I_{OUT} = 500 mA		0.2		Ω
Driver System Characteristics						
I_{OUT}	Current accuracy	After settling, 500 mA (ISET = 276h)	**−6**	±1	**+6**	%
t_r	Current rise time				50	µs
t_f	Current fall time				50	µs
I_{STEP}	Current step			0.64		mA
Buck or Boost Converter						
	Positive current limit range	Programmable	500		2000	mA
	Positive current limit accuracy	Set to 1000 mA	-20		+20	%
	Negative current limit range	Programmable	550		2200	mA
	Negative current limit accuracy	Set to 550 mA	-20		+20	%
$V_{OUT\ MAX}$	Maximum output voltage				4.6	V
f_{SW}	Switching frequency		2.25	2.4	2.55	MHz
$r_{DSON\ P1S}$	P1 on resistance in buck mode (small)			100		mΩ
$r_{DSON\ P1L}$	P1 on resistance in boost mode (large)			55		mΩ
$r_{DSON\ N1}$	N1 on resistance			160		mΩ
$r_{DSON\ N3}$	N3 on resistance in buck mode	VOUT = 0.8V		70		mΩ
$r_{DSON\ P2}$	P2 on resistance in boost mode	VOUT = 3.6V		65		mΩ
$r_{DSON\ N2}$	N2 on resistance			150		mΩ
PWM Input (Global brightness control)						
f_{PWM}	PWM frequency	7-bit resolution	4		20	kHz
		8-bit resolution	4		10	
		9-bit resolution	4		5	
t_{TO}	Timeout	For PWM zero	260	300	340	µs
t_{ON}	Minimum on time			1		µs
t_{OFF}	Minimum off time			1		µs
Logic Input EN						
VIL	Logic input low level				0.5	V
VIH	Logic input high level		1.2			V
Logic Inputs SDA, SCL, R_EN, G_EN, B_EN, PWM						
VIL	Logic input low level	VEN = 1.65 to VDD			0.2* VEN	V
VIH	Logic input high level	VEN = 1.65 to VDD	0.8* VEN			V
Logic Outputs SDA, FAULT						
VOL	Output low level	I_{OUT} = 3 mA			0.5	V

BLOCK DIAGRAM

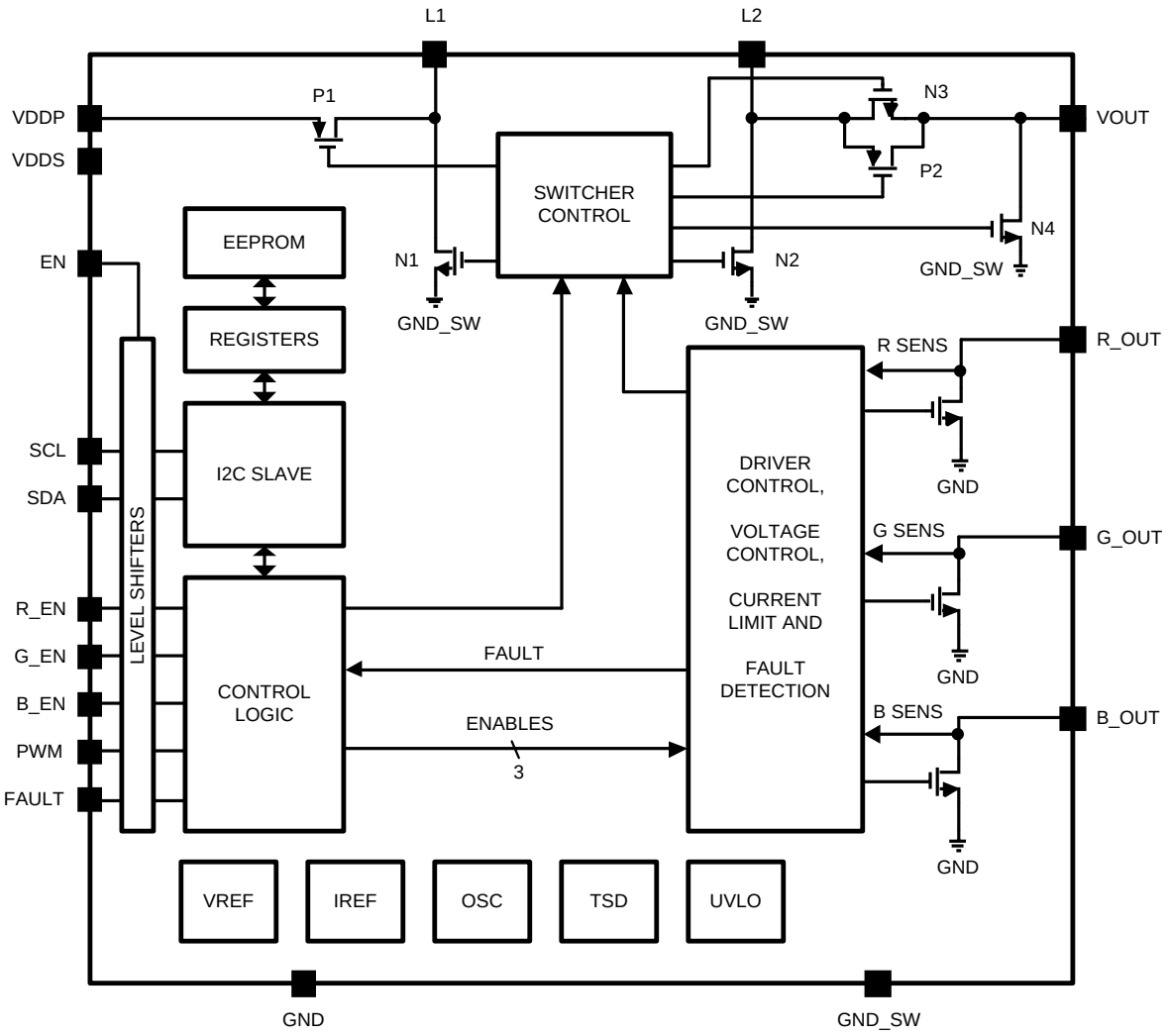

Figure 3. LM3549 Block Diagram

Modes of Operation

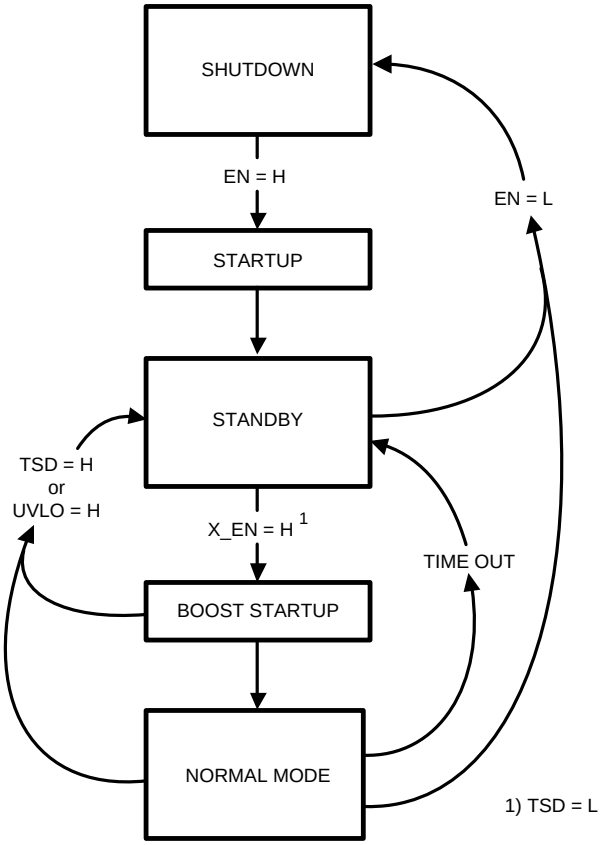

Figure 4. Modes of Operation

SHUTDOWN: Shutdown mode is entered always if EN is low or internal Power On Reset (POR) is active. Power on reset will activate during the chip startup or when the supply voltage VDD falls below 1.5V. This is the low power consumption mode, when all circuit functions are disabled.

STARTUP: When EN input is pulled high, the internal startup sequence powers up all the needed internal blocks (VREF, Oscillator, etc.). EEPROM values are also read to registers during Startup.

STANDBY: After Startup device enters Standby mode. In standby mode all support blocks are active but buck-boost converter and the drivers are disabled. Control registers can be written in this mode and the control bits are effective immediately. EEPROM writing is allowed only in standby mode.

BOOST STARTUP: Soft start for boost output is generated in the boost startup mode. The boost output is raised in a low current mode. Soft start time can be set with registers. The boost startup is entered from Standby if any of the X_EN inputs is pulled high.

NORMAL: During normal mode user controls the chip using the X_EN inputs. In normal mode buck-boost converter and drivers are active. Device returns to standby mode if all X_EN inputs are low for time period set by Time out register. If EN input is pulled low device goes to shutdown mode.

TSD: If the chip temperature rises too high, the thermal shutdown (TSD) disables the chip operation and Standby mode is entered until no thermal shutdown event is present.

Typical Performance Characteristics

Standby Supply Current vs. Input Voltage

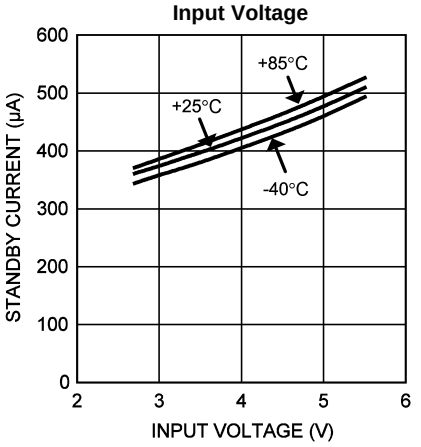

Figure 5.

Active Mode Supply Current vs Input Voltage (LED Open)

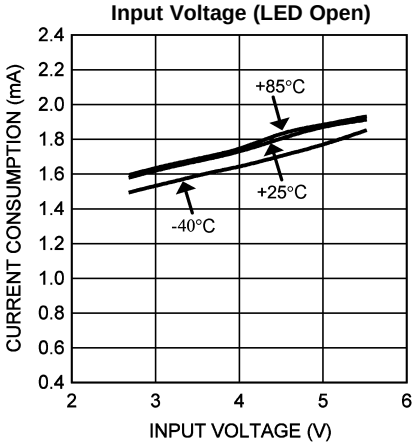

Figure 6.

LED Current vs Current Setting V_{IN} = 3.8V

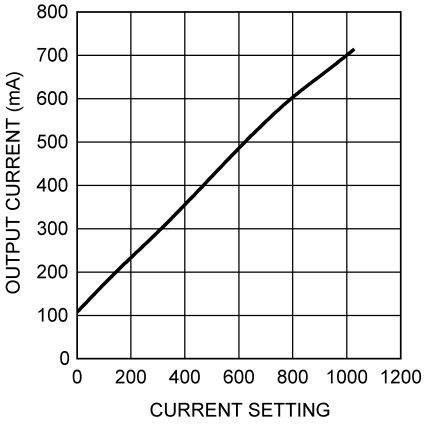

Figure 7.

Driver Current vs. Input Voltage (I_{OUT} = 500 mA)

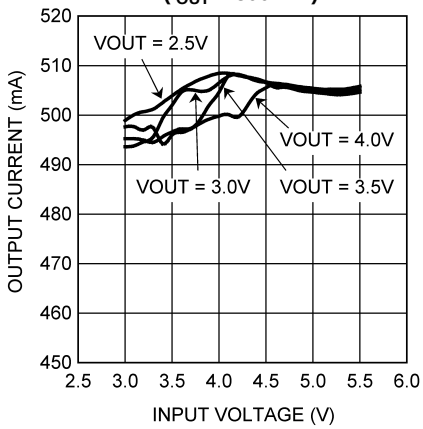

Figure 8.

Driver Resistance vs VIN (I_{OUT} = 500 mA)

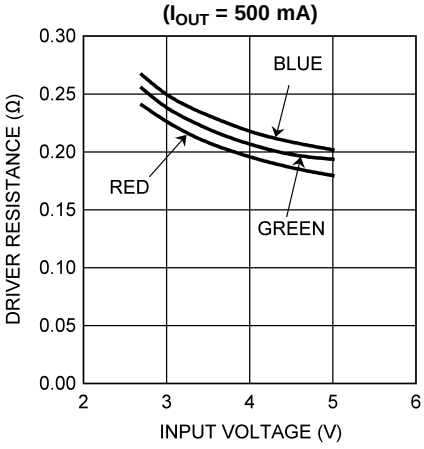

Figure 9.

LED Driver Resistance vs Output Current (V_{IN} = 3.8V)

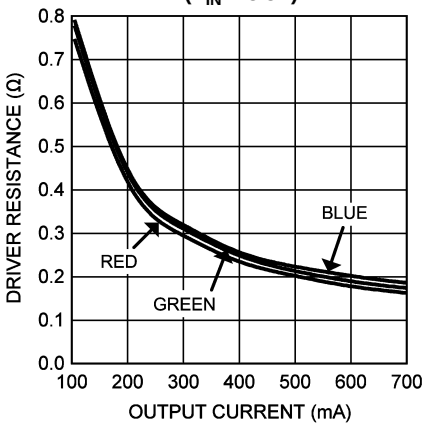

Figure 10.

Typical Performance Characteristics (continued)

LED Drive Efficiency vs Output Current (V_{OUT} = 3.4V)

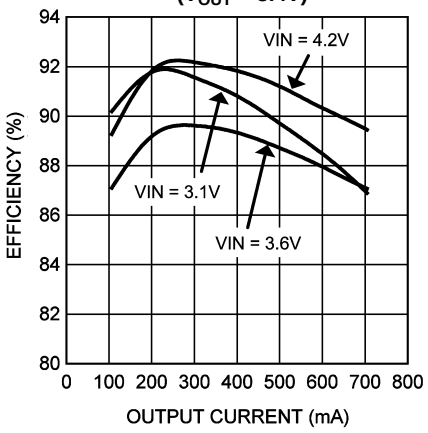

Figure 11.

LED Drive Efficiency vs Input Voltage (I_{OUT} = 300 mA)

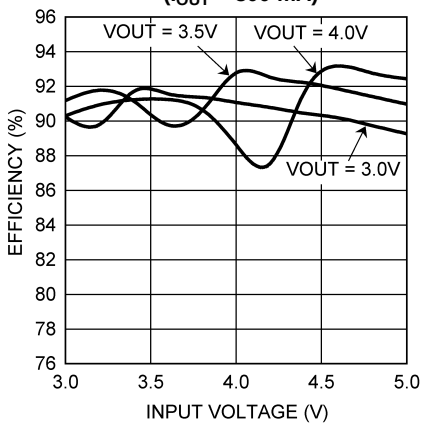

Figure 12.

PWM Output Current Control

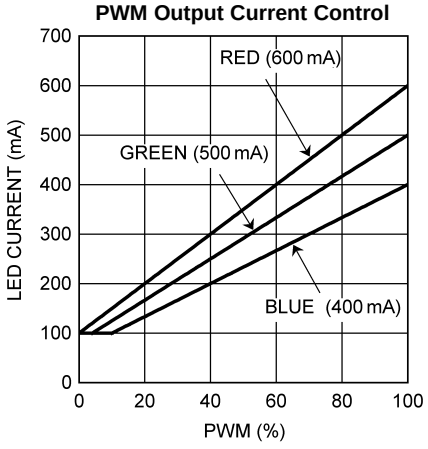

Figure 13.

Master Fader Register Current Control

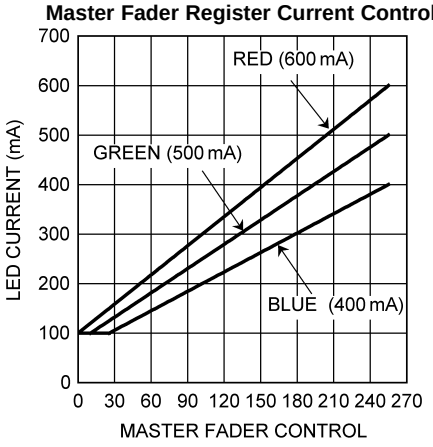

Figure 14.

OPERATION DESCRIPTION

LM3549 is a sequential LED driver for portable video projectors. It has three high current low side drivers and a buck-boost DC-DC converter. Only single LED can be enabled at any given time. DC-DC converter quickly adjusts the output voltage to a suitable level based on each LED's forward voltage. This minimizes the power dissipation at the drivers and maximizes the system efficiency.

Figure 15 shows a typical timing of a portable video projector light source. Each frame is divided into 10 individual color sequences. White balance is achieved by adjusting the driver currents.

Timing of LM3549 depends solely on the R_EN, G_EN and B_EN inputs. Each driver's current is set with I^2C registers and current levels can be stored to internal EEPROM. After correct current values are stored to EEPROM LM3549 can be used in application without I^2C interface.

Full frame	1/60Hz	16.66 ms
Red	Full frame x 7.5%	1.25 ms
Green	Full frame x 11%	1.822 ms
Blue	Full frame x 12.5%	2.08 ms

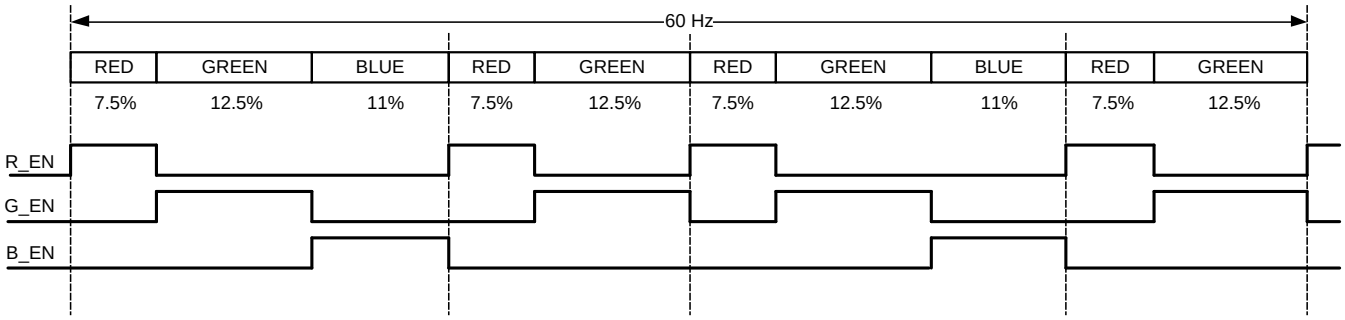

Figure 15. Timing Chart

CONTROL INTERFACE

Even though each driver has its own control input only one driver can be enabled at any given time. If second control is pulled high while previous color is active second output won't be enabled until the first input is pulled low. This can be seen on Figure 16. G_EN is pulled high while R_EN is still high. G_OUT is not activated until R_EN is pulled low. Next B_EN and R_EN are both pulled high while G_EN is high. When G_EN is pulled low R_OUT is enabled because R_EN has higher priority (Priority order: RGB).

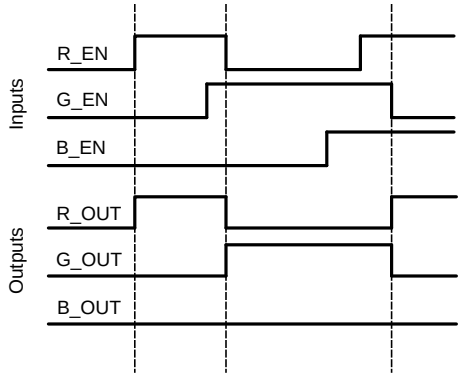

Figure 16. Control Signals

CONTROL REGISTERS

Figure 17 shows the structure of the control registers. Control registers consists of volatile dynamic registers and non volatile EEPROM.

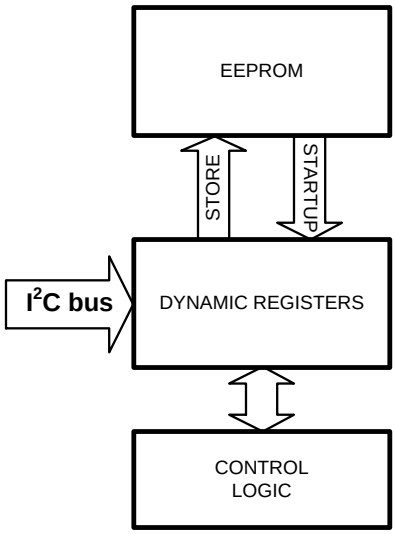

Figure 17. Register Structure

All I^2C register read write commands are done to volatile dynamic registers. Dynamic registers are also used to set the device parameters. All registers except FAULT and EEPROM CONTROL register can be stored to EEPROM. EEPROM values are automatically read to dynamic registers during startup. This makes device use very versatile. After calibration device can be used even without I^2C control. If system has I^2C bus, control registers can be written to adjust parameters on the fly. If registers need to be set back to default values this can be done by first writing 04h to register 40h (EE init bit to “1”) followed by 01h to register 40h (EE read bit to “1”).

EEPROM PROGRAMMING

EEPROM values can be rewritten if device needs recalibration. This can be done for example if white point changes due to aging effect of the LEDs. To store current register values to EEPROM user needs to first write 04h to register 40h (EE init bit to “1”) followed by 02h to register 40h (EE prog bit to “1”). LM3549 Internal charge pump generates the high voltage required for programming the EEPROM. To be able to generate this high voltage Vin needs to be set to 5V during EEPROM programming. EEPROM programming should be completed within approximately 200 ms. Once EEPROM programming is completed LM3549 sets EE_ready bit to 1. After this Vin voltage can be set back to normal operating level. EEPROM programming should always be done in standby mode.

CURRENT SETTING

There are three 10 bit current settings for each driver. 10 bits are divided into two eight bit registers. First register holds the eight least significant bits (LSB) and the second register holds the two most significant bits (MSB). These settings are grouped into three banks. IR0, IG0 and IB0 form a bank0; IR1, IG1 and IB1 form a bank1 and IR2, IG2 and IB2 form a bank2. For example IR0_MSB holds the two MSB for red on bank0 and IR0_LSB the eight LSB for red on bank0. Bank is selected with BANK_SEL register (00 = bank0, 01 = bank1 and 10 or 11 = bank2).

Current setting is linear up to 550mA output current (see figure LED Current vs Current Setting in Typical Performance Characteristics). 550mA current is achieved with current setting I_{SET} = 710. After this the current step decreases slightly. For currents up to 550 mA current setting can be calculated using formula:

I_{SET} = (target current in mA - 100 mA)/(650mA/1024)

Fot currents between 550mA and 700mA current setting can be calculated using formula:

I_{SET} = (target current in mA - 550 mA)/0.479 mA + 710

BRIGHTNESS CONTROL

Output current of all drivers can be adjusted using PWM input or FADER register. This can be used to easilly adjust the total brightness of the LEDs. Brightness control function can be enabled from the CTRL register as seen in table below. In case of PWM input brightness control (BRC) is the positive duty cycle of the input signal. In case of FADER register brightness is MASTER FADER[7:0]/255.

MFE	PWM	Brightness Control
0	0	No brightness control
0	1	PWM input
1	0	FADER register
1	1	PWM input

The maximum currents of the drivers are set in the current setting registers. Brightness control keeps the ratio of the driver currents constant and adjusts the output currents based on the highest current setting. Driver currents can be adjusted between 100 mA to the maximum current set in the registers (see figures PWM Output Current Control and Master Fader Register Current Control in Typical Performance Characteristics).

I_{SET1} =highest current setting

I_{SET2} =current setting 2

I_{SET3} =current setting 3

R1 =(I_{SET2}/I_{SET1}), ratio of current 2 and the highest current

R2 =(I_{SET3}/I_{SET1}), ratio of current 3 and the highest current

BRC =brightness control

I1 = I_{SET1} x BRC)

I2 = I1 x R1

I3 = I1x R2

PWM TIMING

Figure 18 shows example of PWM brightness control. PWM input can be change at any given time but control takes effect when next enable is pulled high. To ensure that control takes effect for the next color time from PWM change to next enable needs to be greater than timeout time (300 µs typical).

At the beginning of the example frame PWM input is changed from 100% to 80% while green driver is enabled. Brightness level is not changed in the middle of the green frame but at the beginning of the next color which in this example is blue. During next green PWM is set back to 100%. This is done at least 300 µs before next enable is pulled high and control takes effect then. During next green PWM is changed to 0%. Time from PWM change to next enable (blue) is less than 300 µs and control don't take effect when blue starts but one color later, what in this example is red.

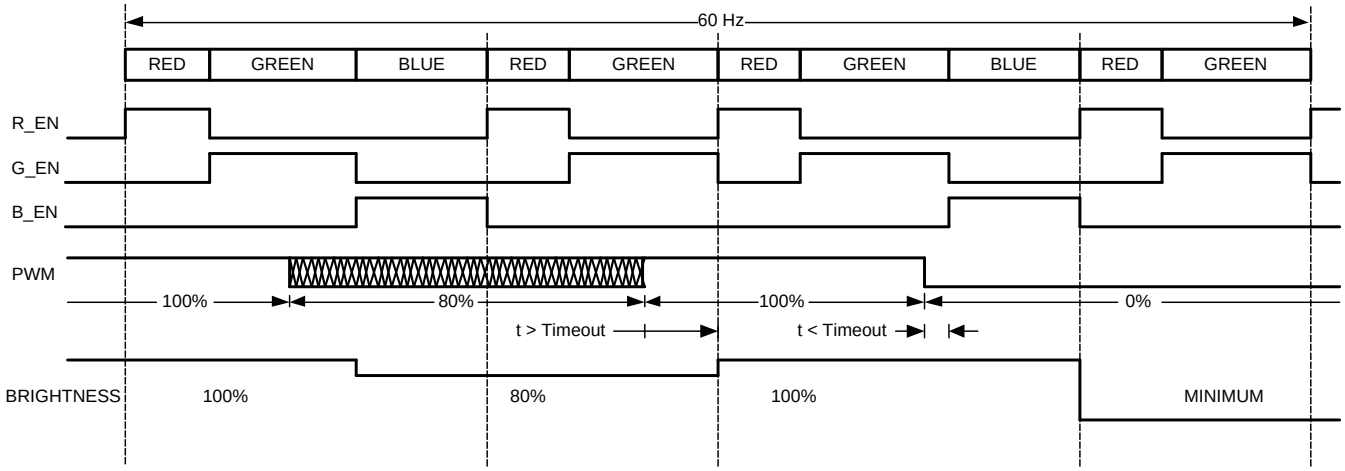

Figure 18. PWM Timing

FAULT DETECTION

LM3549 can detect several different fault conditions. These are LED open, LED short, thermal shutdown (TSD), under voltage lockout (UVLO) and buck-boost converter over current protection (OCP). If any of the fault conditions occur corresponding fault bit is set in the fault register. If fault mask bit is not set also Fault output is pulled low. Reading Fault register resets its value to zero and sets Fault output to high impedance state.

LED OPEN FAULT

Open fault is generated when at the end of color VOUT is at maximum and no current is flowing through driver (VDx = 0V). Also OCP fault needs to be low. Open fault can be generated by broken LED or a soldering defect.

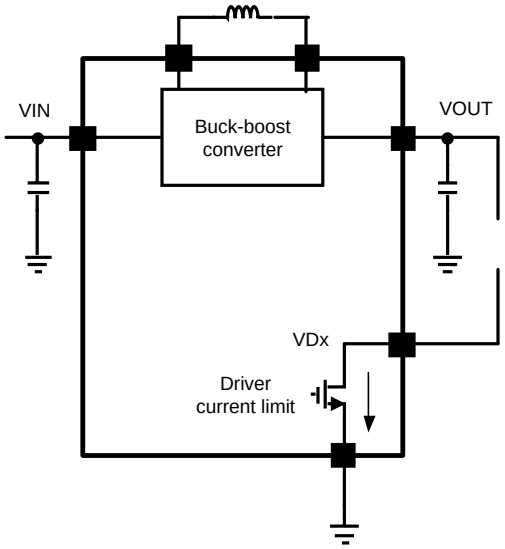

Figure 19. LED Open Fault

LED SHORT FAULT

Short fault is detected when VOUT < 1.0V at the end of a color. Short fault is generated when VOUT is shorted to driver by soldering defect or faulty LED. Driver current limit limits the maximum current. Depending on output current and positive limit settings, LED short can also generate OCP fault to fault register.

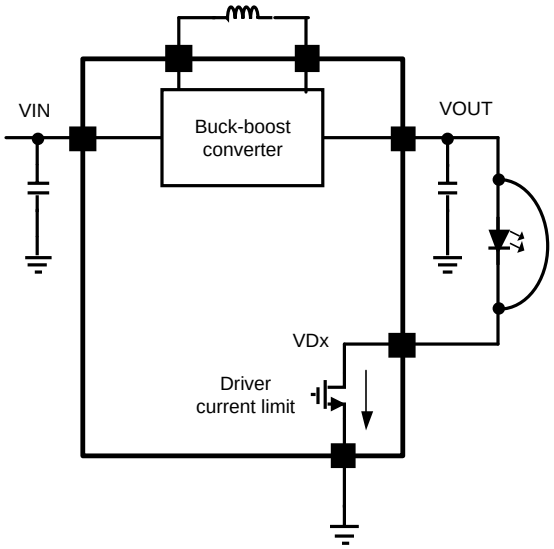

Figure 20. LED Short Fault

TSD FAULT

Thermal shutdown (TSD) fault is generated if junction temperature rises above TSD level. TSD engages at T_J= 150°C (typ) and disengages at T_J = 140°C (typ). TSD sets device to standby mode. Occasionally a false TSD fault is generated to Fault register when device goes from shutdown mode to standby mode. It is good practice to reset the fault register by reading it every time after device is set from shutdown mode to standby mode.

UVLO FAULT

Under voltage lock out (UVLO) fault is generated if VIN drops below UVLO level (~2.5V). UVLO sets device to standby mode. When VIN rises back above the 2.5V device exits UVLO. If control register values were changed from EEPROM defaults they need to be rewritten to registers because UVLO condition can generate EEPROM read sequence.

OVER CURRENT PROTECTION FAULT

Over current protection (OCP) fault is generated when positive current limit is active at the end of a color. It is important to notice that OCP fault is not always set when positive current limit is activated. Positive current limit can activate during normal operation when buck-boost is adjusting the output voltage to a higher level. OCP can be caused by short from VOUT to GND, short from driver to GND or if too low positive current limit value is set for desired output current.

I²C Compatible Interface

I²C ADDRESS

LM3549 I²C address is 36 hex (7 bits).

I²C SIGNALS

The SCL pin is used for the I²C clock and the SDA pin is used for bidirectional data transfer. Both these signals need a pull-up resistor according to I²C specification. The values of the pull-up resistors are determined by the capacitance of the bus (typ. ~1.8k). Signal timing specifications are shown in Table 1.

I²C VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

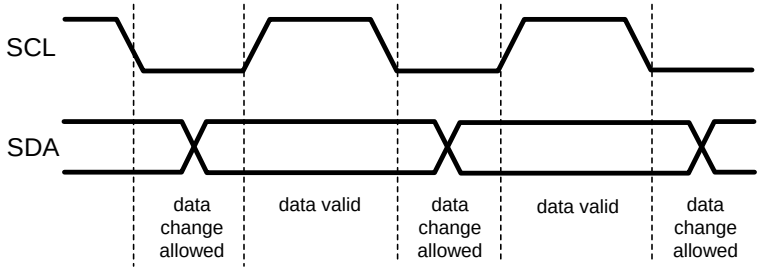

Figure 21. I²C Signals: Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I2C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

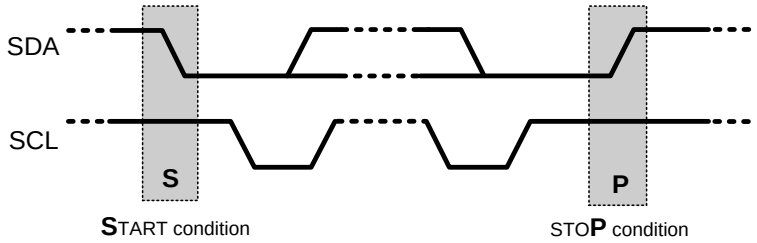

Figure 22. Start and Stop Conditions

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the ninth clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM3549 address is 36 hex. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

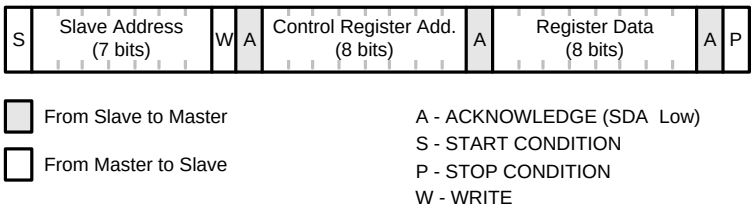

Figure 23. I²C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in Figure 24

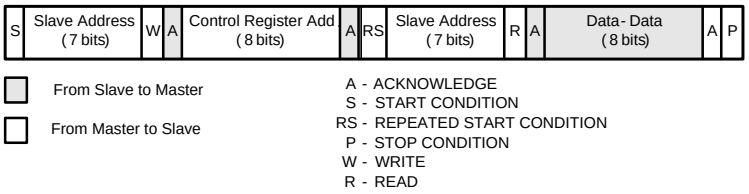

Figure 24. I²C Read Cycle

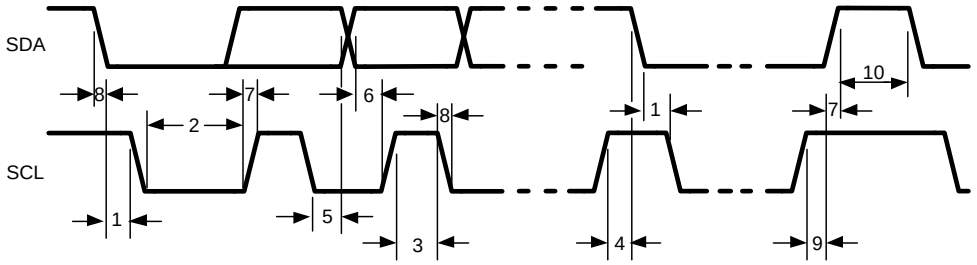

Figure 25. I²C Timing Diagram

Table 1. I²C Timing Parameters

Symbol	Parameter	Limit		Units
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold	300	900	ns
5	Data Hold Time (input direction)	0	900	ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	20 + 0.1Cb	300	ns
8	Fall Time of SDA and SCL	15 + 0.1Cb	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
Cb	Capacitive Load for Each Bus Line	10	200	pF

Register Map

ADDR	NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT	NOTE
00H	BANK_SEL							Bank_sel[1:0]		00H	EEPROM
01H	IR0_LSB	Red 0 [7:0]								81H	EEPROM
02H	IR0_MSB	N/A						Red 0 [9:8]		01H	EEPROM
03H	IG0_LSB	Green 0 [7:0]								81H	EEPROM
04H	IG0_MSB	N/A						Green 0 [9:8]		01H	EEPROM
05H	IB0_LSB	Blue 0 [7:0]								81H	EEPROM
06H	IB0_MSB	N/A						Blue 0 [9:8]		01H	EEPROM
07H	IR1_LSB	Red 1 [7:0]								E7H	EEPROM
08H	IR1_MSB	N/A						Red 1 [9:8]		00H	EEPROM

ADDR	NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT	NOTE
09H	IG1_LSB	Green 1 [7:0]								E7H	EEPROM
0AH	IG1_MSB	N/A						Green 1 [9:8]		00H	EEPROM
0BH	IB1_LSB	Blue 1 [7:0]								E7H	EEPROM
0CH	IB1_MSB	N/A						Blue 1 [9:8]		00H	EEPROM
0DH	IR2_LSB	Red 2 [7:0]								4DH	EEPROM
0EH	IR2_MSB	N/A						Red 2 [9:8]		00H	EEPROM
0FH	IG2_LSB	Green 2 [7:0]								4DH	EEPROM
10H	IG2_MSB	N/A						Green 2 [9:8]		00H	EEPROM
11H	IB2_LSB	Blue 2 [7:0]								4DH	EEPROM
12H	IB2_MSB	N/A						Blue 2 [9:8]		00H	EEPROM
13H	FADER	MASTER FADER [7:0]								FFH	EEPROM
14H	CTRL	N/A		SOFT START[1:0]		TIME OUT[1:0]		MFE	PWM	00H	EEPROM
15H	ILIMIT	N/A		POS_LIMIT[1:0]		N/A		NEG_LIMIT[1:0]		11H	EEPROM
16H	F_MASK	N/A			SHORT	OPEN	UVLO	TSD	OCP	00H	EEPROM
17H	FAULT	N/A	SHORT[1:0]		OPEN[1:0]		UVLO	TSD	OCP	00H	Read Only
19H	USR1	User Register1[7:0]								00H	EEPROM
1AH	USR2	User Register2[7:0]								00H	EEPROM
40H	EEPROM CONTROL	EE ready					EE init	EE prog	EE read	00H	R/W

I²C Register Details

00h BANK_SEL[1:0]

Bank selection register. Selects one of the three current setting banks.

BIT		BANK SELECTION
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank 2

01h IR0_LSB and 02h IR0_MSB

Red LED current setting for Bank 0. IR0_LSB holds the eight least significant bits and IR0_MSB the two most significant bits.

03h IG0_LSB and 04h IG0_MSB

Green LED current setting for Bank 0. IG0_LSB holds the eight least significant bits and IG0_MSB the two most significant bits.

05h IB0_LSB and 06h IB0_MSB

Blue LED current setting for Bank 0. IB0_LSB holds the eight least significant bits and IB0_MSB the two most significant bits.

07h IR1_LSB and 08h IR1_MSB

Red LED current setting for Bank 1. IR1_LSB holds the eight least significant bits and IR1_MSB the two most significant bits.

09h IG1_LSB and 0Ah IG1_MSB

Green LED current setting for Bank 1. IG1_LSB holds the eight least significant bits and IG1_MSB the two most significant bits.

0Bh IB1_LSB and 0Ch IB1_MSB

Blue LED current setting for Bank 1. IB1_LSB holds the eight least significant bits and IB1_MSB the two most significant bits.

0Dh IR2_LSB and 0Eh IR2_MSB

Red LED current setting for Bank 2. IR2_LSB holds the eight least significant bits and IR2_MSB the two most significant bits.

0Fh IG2_LSB and 10h IG2_MSB

Green LED current setting for Bank 2. IG2_LSB holds the eight least significant bits and IG2_MSB the two most significant bits.

11h IB2_LSB and 12h IB2_MSB

Blue LED current setting for Bank 2. IB2_LSB holds the eight least significant bits and IB2_MSB the two most significant bits.

13h FADER

Master fader control register. Can be used to control the total brightness of the LEDs if MFE is enabled.

14h CTRL

Control register. Controls many of the LM3549 features.

BIT[1:0] PWM and MFE

Control register bits [1:0] can be used to enable master control or PWM brightness control.

MFE	PWM	BRIGHTNESS CONTROL
0	0	No brightness control
0	1	PWM input
1	0	Master input
1	1	PWM input

BIT[3:2] TIME OUT[1:0]

Selects how long device stays in active mode after all x_EN controls have been set low

BIT		TIME OUT
0	0	125 ms
0	1	250 ms
1	0	500 ms
1	1	1s

BIT[5:4] SOFT START[1:0]

Enables soft start feature and selects soft start time.

BIT		SOFT START TIME
0	0	disabled
0	1	0.5s
1	0	1s
1	1	2s

15h ILIMIT

ILIMIT register sets the buck-boost converters current limit values.

BIT[1:0] NEG_LIMIT[1:0]

Selects buck-boost converters negative current limit.

BIT		NEGATIVE CURRENT LIMIT
0	0	550 mA
0	1	1100 mA
1	0	1650 mA
1	1	2200 mA

BIT[5:4] POS_LIMIT[1:0]

Selects buck-boost converters positive current limit.

BIT		POSITIVE CURRENT LIMIT
0	0	500 mA
0	1	1000 mA
1	0	1500 mA
1	1	2000 mA

16h F_MASK

Fault output mask register. Can be used to disable fault output from desired faults.

17h FAULT

Fault register. If fault occurs corresponding fault bits are set in fault register. Reading Fault register resets it. Read only register.

BIT[0] OCP

Over current protection. Buck-boost converters current limit has been reached.

BIT[1] TSD

Thermal shutdown fault. Junction temperature has risen abowe TSD level.

BIT[2] UVLO

Under voltage lock-out. Input voltage has fallen below UVLO threshold level.

BIT[4:3] OPEN[1:0]

LED open fault.

BIT		FAULT
0	0	No fault
0	1	Red open
1	0	Green open
1	1	Blue open

BIT[6:5] SHORT[1:0]

LED short fault.

BIT		FAULT
0	0	No fault
0	1	Red short
1	0	Green short
1	1	Blue short

19h and 1AH USR1 and USR2

User registers 1 and 2. Can be used to store any user data. No affect on the device.

40h EEPROM CONTROL

EEPROM Control register. This register is used to program EEPROM. EEPROM programming is described in the EEPROM Programming chapter.

Table 2. Recommended External Components

Symbol	Symbol Explanation	Value	Type	Example
CIN	Input Capacitor	10 µF,6.3V/10V	X7R	
COUT	Output Capacitor	4.7 µF, 6.3V/10V	X7R	
L1	Switcher Inductor	2.2 µH, 1900 mA		TDK VLF4014ST-2R2M1R9

REVISION HISTORY

Changes from Original (May 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3549SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-30 to 85	L3549SQ	Samples
LM3549SQE/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-30 to 85	L3549SQ	Samples
LM3549SQX/NOPB	ACTIVE	WQFN	RTW	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-30 to 85	L3549SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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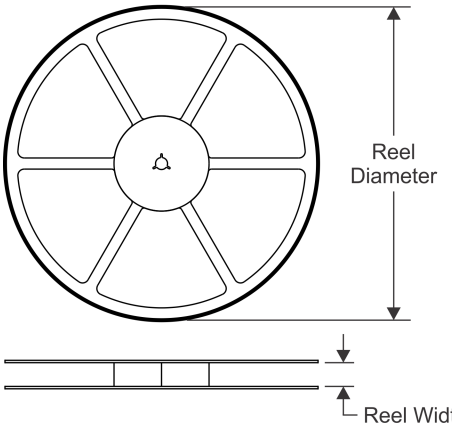
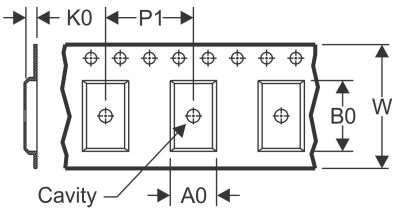
TAPE AND REEL INFORMATION

REEL DIMENSIONS

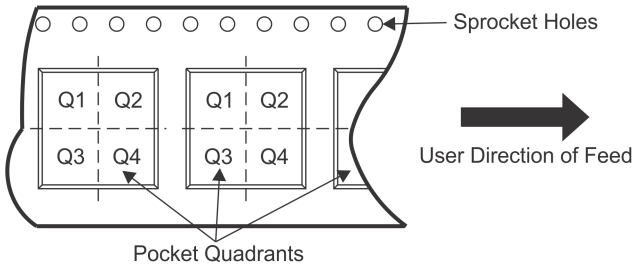


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

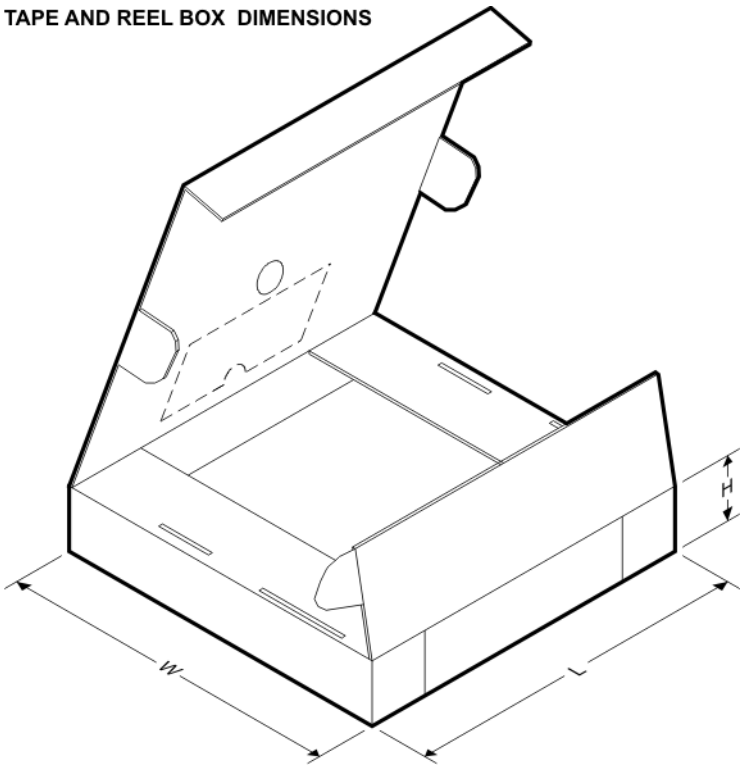
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3549SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM3549SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM3549SQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

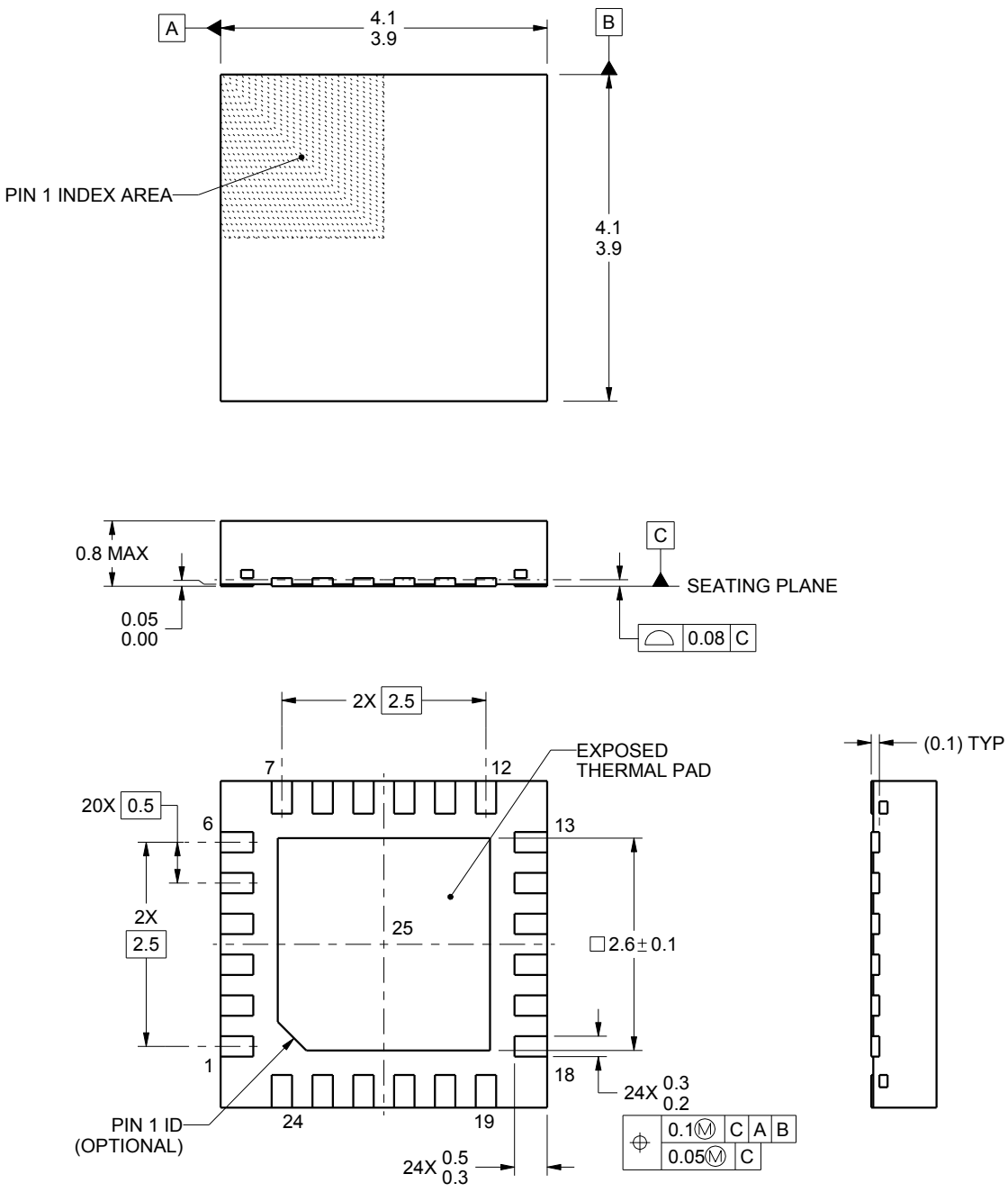
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3549SQ/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LM3549SQE/NOPB	WQFN	RTW	24	250	210.0	185.0	35.0
LM3549SQX/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0

PACKAGE OUTLINE

RTW0024A

WQFN - 0.8 mm max height

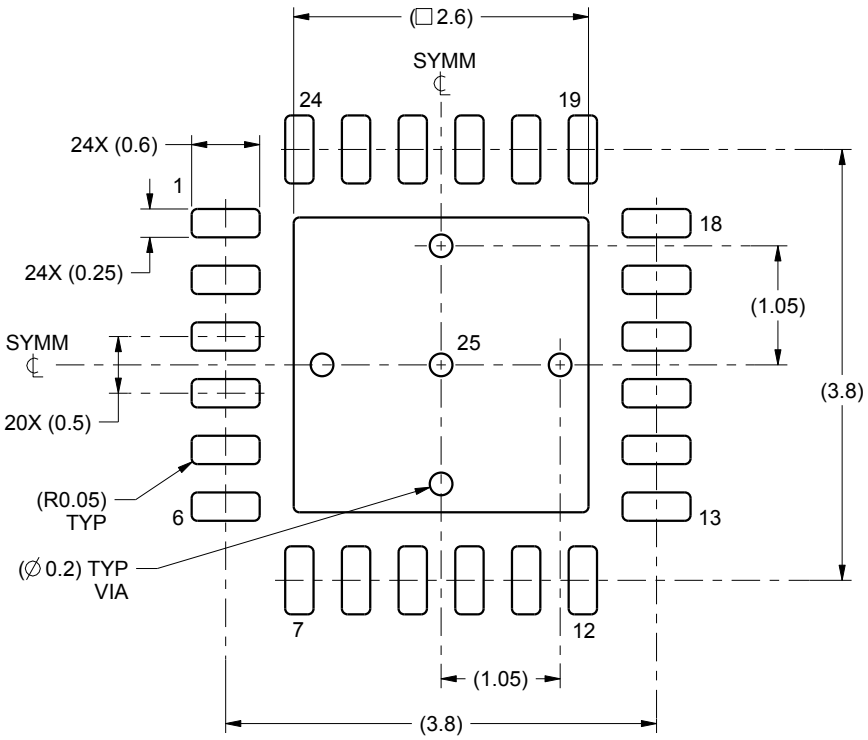
PLASTIC QUAD FLATPACK - NO LEAD



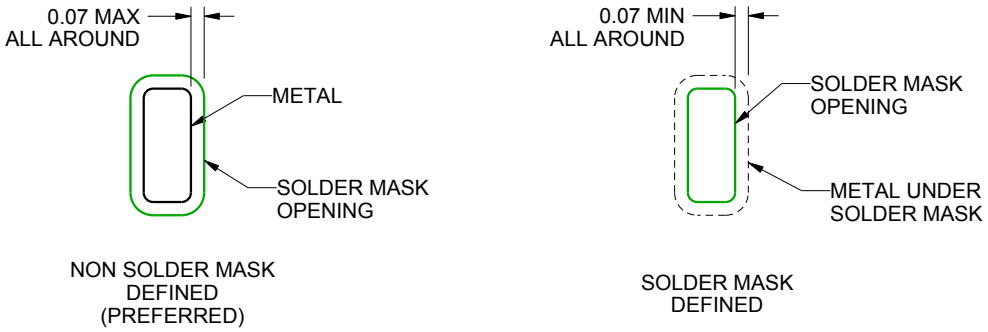
4222815/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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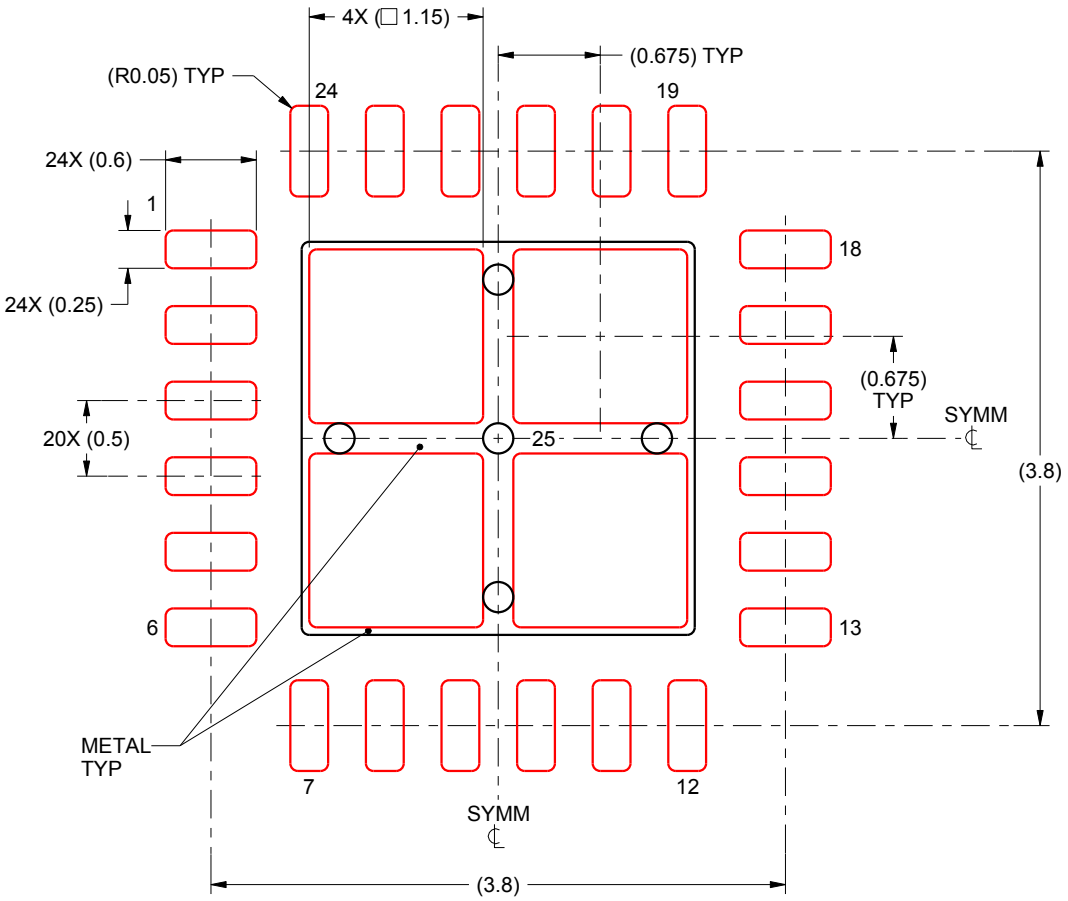
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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