THE DATASHEET OF

LM3502SQ-44/NOPB

LM3502 Step-Up Converter for White LED Applications

Check for Samples: LM3502

FEATURES

- **Drive up to 4, 6, 8 or 10 White LEDs for Dual Display Backlighting**
- **>80% Efficiency**
- **Output Voltage Options: 16V , 25V , 35V, and 44V**
- **Input Under-Voltage Protection**
- **Internal Soft Start Eliminating Inrush Current**
- **1 MHz Constant Switching Frequency**
- **Wide Input Voltage: 2.5V to 5.5V**
- **Small External Components**
- **Low Profile Packages: <1 mm Height**
  - **10 Bump DSBGA**
  - **16 Pin WQFN**

APPLICATIONS

- **Dual Display Backlighting in Portable Devices**
- **Cellular Phones and PDAs**

DESCRIPTION

The LM3502 is a white LED driver for lighting applications. For dual display or large single white LED string backlighting applications, the LM3502 provides a complete solution. The LM3502 contains two internal white LED current bypass FET(Field Effect Transistor) switches that are ideal for controlling dual display applications. The white LED current can be adjusted with a PWM signal directly from a microcontroller without the need of an RC filter network.

Typical Application

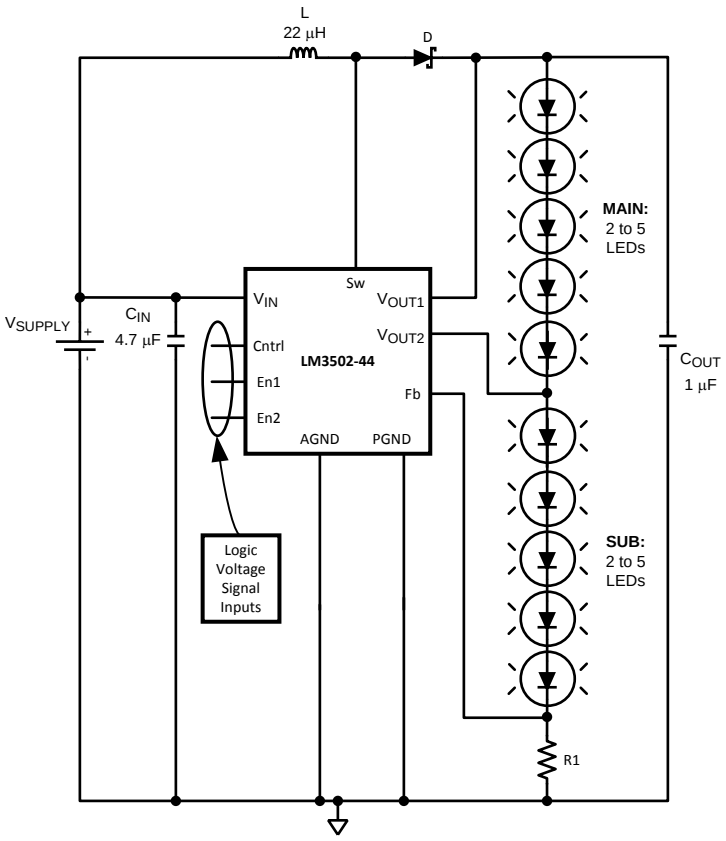


Figure 1. Blacklight Configuration with 10 White LEDs

DESCRIPTION (CONTINUED)

With no external compensation, cycle-by-cycle current limit, over-voltage protection, and under-voltage protection, the LM3502 offers superior performance over other application specific standard product step-up white LED drivers.

Connection Diagrams

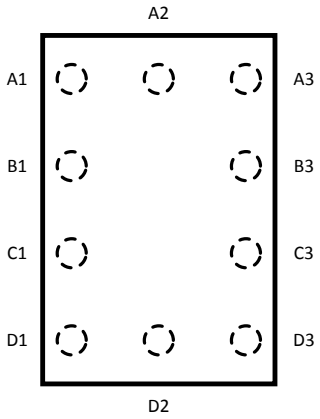


Figure 2. TOP VIEW
10-Bump Thin DSBGA
See Package Number (YPA0010)

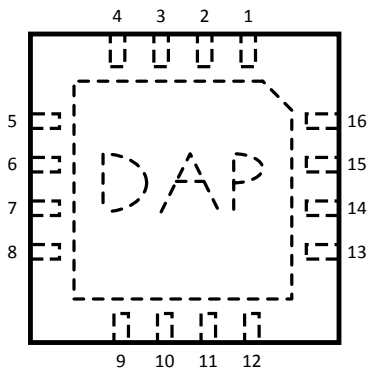


Figure 3. TOP VIEW
16-Lead Thin WQFN
See Package Number (RGH0016A)

PIN DESCRIPTIONS

Bump #	Pin #	Name	Description
A1	9	Cntrl	Shutdown Control Connection
B1	7	Fb	Feedback Voltage Connection
C1	6	V_{OUT2}	Drain Connections of The NMOS and PMOS Field Effect Transistor (FET) Switches (Figure 4: N2 and P1)
D1	4	V_{OUT1}	Over-Voltage Protection (OVP) and Source Connection of The PMOS FET Switch (Figure 4: P1)
D2	2 and 3	Sw	Drain Connection of The Power NMOS Switch (Figure 4: N1)
D3	15 and 16	PGND	Power Ground Connection
C3	14	AGND	Analog Ground Connection
B3	13	V_{IN}	Supply or Input Voltage Connection
A3	12	En2	NMOS FET Switch Control Connection
A2	10	En1	PMOS FET Switch Control Connection
	1	NC	No Connection
	5	NC	No Connection
	8	NC	No Connection
	11	NC	No Connection
	DAP	DAP	Die Attach Pad (DAP), must be soldered to the printed circuit board's ground plane for enhanced thermal dissipation.

Cntrl (Bump A1): Shutdown control pin

When V_{Cntrl} is ≥ 1.4V, the LM3502 is enabled or ON. When V_{Cntrl} is ≤ 0.3V, the LM3502 will enter into shutdown mode operation. The LM3502 has an internal pull down resistor on the Cntrl pin, thus the device is normally in the off state or shutdown mode of operation.

Fb (Bump B1): Output voltage feedback connection

The white LED string network current is set/programmed using a resistor from this pin to ground.

V_{OUT2} (Bump C1): Drain connections of the internal PMOS and NMOS FET switches

. (Figure 4: P1 and N2). It is recommended to connect 100nF at V_{OUT2} for the LM3502-35V

and LM3502-44 versions if V_{OUT2} is not used.

V_{OUT1} (Bump D1): Source connection of the internal PMOS FET switch (Figure 4: P1) and OVP sensing node

The output capacitor must be connected as close to the device as possible, between the V_{OUT1} pin and ground plane. Also connect the Schottky diode as close as possible to the V_{OUT1} pin to minimize trace resistance and EMI radiation.

Sw (Bump D2): Drain connection of the internal power NMOS FET switch (Figure 4: N1)

Minimize the metal trace length and maximize the metal trace width connected to this pin to reduce EMI radiation and trace resistance.

PGND (Bump D3): Power ground pin

Connect directly to the ground plane.

AGND (Bump C3): Analog ground pin

Connect the analog ground pin directly to the PGND pin.

V_{IN} (Bump B3): Supply or input voltage connection pin

The C_{IN} capacitor should be as close to the device as possible, between the V_{IN} pin and ground plane.

En2 (Bump A3): Enable pin for the internal NMOS FET switch (Figure 4: N2) during device operation

When V_{En2} is ≤ 0.3V, the internal NMOS FET switch turns on and the SUB display turns off. When V_{En2} is ≥ 1.4V, the internal NMOS FET switch turns off and the SUB display turns on. The En2 pin has an internal pull down resistor, thus the internal NMOS FET switch is normally in the on state of operation with the SUB display turned off.

If V_{En1} and V_{En2} are ≤ 0.3V and V_{Cntrl} is ≥ 1.4V, the LM3502 will enter a low I_Q shutdown mode of operation where all the internal FET switches are off. If V_{OUT2} is not used, En2 must be grounded or floating and use En1 along with Cntrl, to enable the device.

En1 (Bump A2): Enable pin for the internal PMOS FET switch (Figure 4: P1) during device operation

When V_{En1} is ≤ 0.3V, the internal PMOS FET switch turns on and the MAIN display is turned off. When V_{En1} is ≥ 1.4V, the internal PMOS FET switch turns off and the MAIN display is turned on. The En1 pin has an internal pull down resistor, thus the internal PMOS FET switch is normally in the on state of operation with the MAIN display turned off. If V_{En1} and V_{En2} are ≤ 0.3V and V_{Cntrl} is ≥ 1.4V, the LM3502 will enter a low I_Q shutdown mode of operation where all the internal FET switches are off. If V_{OUT2} is not used, En2 must be grounded and use En1 a long with Cntrl, to enable the device.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

V_{IN} Pin	−0.3V to +5.5V
Sw Pin	−0.3V to +48V
Fb Pin	−0.3V to +5.5V
Cntrl Pin	−0.3V to +5.5V
V_{OUT1} Pin	−0.3V to +48V
V_{OUT2} Pin	−0.3V to V_{OUT1}
En1	−0.3V to +5.5V
En2	−0.3V to +5.5V
Continuous Power Dissipation	Internally Limited
Maximum Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	−65°C to +150°C
ESD Rating (4) Human Body Model: Machine Model:	 2 kV 200V

(1) All voltages are with respect to the potential at the GND pin.
(2) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical characteristic specifications do not apply when operating the device outside of its rated operating conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Operating Conditions (1)(2)

Junction Temperature (T_J) Range	−40°C to +125°C
Ambient Temperature (T_A) Range	−40°C to +85°C
Input Voltage, V_{IN} Pin	2.5V to 5.5V
Cntrl, En1, and En2 Pins	0V to 5.5V

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical characteristic specifications do not apply when operating the device outside of its rated operating conditions.
(2) All voltages are with respect to the potential at the GND pin.

Thermal Properties (1)

Junction-to-Ambient Thermal Resistance (θ_{JA})	
DSBGA Package	65°C/W
WQFN Package	49°C/W

(1) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See Thermal Properties for the thermal resistance. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_D(MAX) = (T_J(MAX) - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature. For more information on this topic, please refer toApplication Note 1187: Leadless Leadframe Package (LLP) and Application Note 1112 for DSBGA chip scale package.

Preliminary Electrical Characteristics (1) (2)

Limits in standard typeface are for T_J = 25°C. Limits in **bold typeface** apply over the full operating junction temperature range (−40°C ≤ T_J ≤ +125°C). Unless otherwise specified, V_{IN} = 2.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage		2.5		5.5	V
I_Q	Non-Switching Switching Shutdown Low I_Q Shutdown	Fb > 0.25V Fb = 0V, Sw Is Floating Cntrl = 0V Cntrl = 1.5V, En1 = En2 = 0V		0.5 1.9 0.1 6	**1** **3** **3** **15**	mA mA µA µA
V_{Fb}	Feedback Voltage		**0.18**	0.25	**0.3**	V

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.

Preliminary Electrical Characteristics (1) (2) (continued)

Limits in standard typeface are for T_J = 25°C. Limits in **bold typeface** apply over the full operating junction temperature range (−40°C ≤ T_J ≤ +125°C). Unless otherwise specified, V_{IN} = 2.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CL}	NMOS Power Switch Current Limit	−16, Fb = 0V −25, Fb = 0V −35, Fb = 0V −44, Fb = 0V	**250** **400** **450** **450**	400 600 750 750	**650** **800** **1050** **1050**	mA
I_{Fb}	Feedback Pin Bias Current (3)	Fb = 0.25V		64	**500**	nA
F_S	Switching Frequency		**0.8**	1	**1.2**	MHz
$R_{DS(ON)}$	NMOS Power Switch ON Resistance (Figure 4: N1)	I_{Sw} = 500 mA		0.55	**1.1**	Ω
$R_{PDS(ON)}$	PMOS ON Resistance of V_{OUT1}/V_{OUT2} Switch (Figure 4: N1)	I_{PMOS} = 20 mA, En1 = 0V, En2 = 1.5V		5	**10**	Ω
$R_{NDS(ON)}$	NMOS ON Resistance of V_{OUT2}/Fb Switch (Figure 4: N2)	I_{NMOS} = 20 mA, En1 = 1.5V, En2 = 0V		2.5	**5**	Ω
D_{MAX}	Maximum Duty Cycle	Fb = 0V	**90**	95		%
I_{Cntrl}	Cntrl Pin Input Bias Current (4)	Cntrl = 2.5V Cntrl = 0V		7 0.1	**14**	µA
I_{Sw}	Sw Pin Leakage Current (5)	Sw = 42V, Cntrl = 0V		0.01	**5**	µA
$I_{VOUT1(OFF)}$	V_{OUT1} Pin Leakage Current (5)	V_{OUT1} = 14V, Cntrl = 0V (16) V_{OUT1} = 23V, Cntrl = 0V (25) V_{OUT1} = 32V, Cntrl = 0V (35) V_{OUT1} = 42V, Cntrl = 0V (44)		0.1 0.1 0.1 0.1	**3** **3** **3** **3**	µA
$I_{VOUT1(ON)}$	V_{OUT1} Pin Bias Current (5)	V_{OUT1} = 14V, Cntrl = 1.5V (16) V_{OUT1} = 23V, Cntrl = 1.5V (25) V_{OUT1} = 32V, Cntrl = 1.5V (35) V_{OUT1} = 42V, Cntrl = 1.5V (44)		40 50 50 85	**80** **100** **100** **140**	µA
I_{VOUT2}	V_{OUT2} Pin Leakage Current (5)	Fb = 0V, Cntrl = 0V, V_{OUT2} = 42V		0.1	**3**	µA
UVP	Under-Voltage Protection	On Threshold Off Threshold	 **2.2**	2.4 2.3	**2.5**	V
OVP	Over-Voltage Protection (6)	On Threshold (16) Off Threshold (16) On Threshold (25) Off Threshold (25) On Threshold (35) Off Threshold (35) On Threshold (44) Off Threshold (44)	**14.5** **14.0** **22.5** **21.5** **32.0** **31.0** **40.5** **39.0**	15.5 15 24 23 34 33 42 41	**16.5** **16.0** **25.5** **24.5** **35.0** **34.0** **43.5** **42.0**	V
V_{En1}	PMOS FET Switch Enabling Threshold (Figure 4: P1)	Off Threshold (Display Lighting) On Threshold (Display Lighting)	 **1.4**	0.8 0.8	**0.3**	V
V_{En2}	NMOS FET Switch Enabling Threshold (Figure 4: N2)	Off Threshold (Display Lighting) On Threshold (Display Lighting)	 **1.4**	0.8 0.8	**0.3**	V
V_{Cntrl}	Device Enabling Threshold	Off Threshold OnThreshold	 **1.4**	0.8 0.8	**0.3**	V
T_{SHDW}	Shutdown Delay Time		8	12	16	ms
I_{En1}	En1 Pin Input Bias Current	En1 = 2.5V En1 = 0V		7 0.1	**14**	µA

(3) Current flows out of the pin.
(4) Current flows into the pin.
(5) Current flows into the pin.
(6) The on threshold indicates that the LM3502 is no longer switching or regulating LED current, while the off threshold indicates normal operation.

Preliminary Electrical Characteristics (1) (2) (continued)

Limits in standard typeface are for T_J = 25°C. Limits in **bold typeface** apply over the full operating junction temperature range (−40°C ≤ T_J ≤ +125°C). Unless otherwise specified, V_{IN} = 2.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{En2}	En2 Pin Input Bias Current	En2 = 2.5V En2 = 0V		7 0.1	**14**	µA

BLOCK DIAGRAM

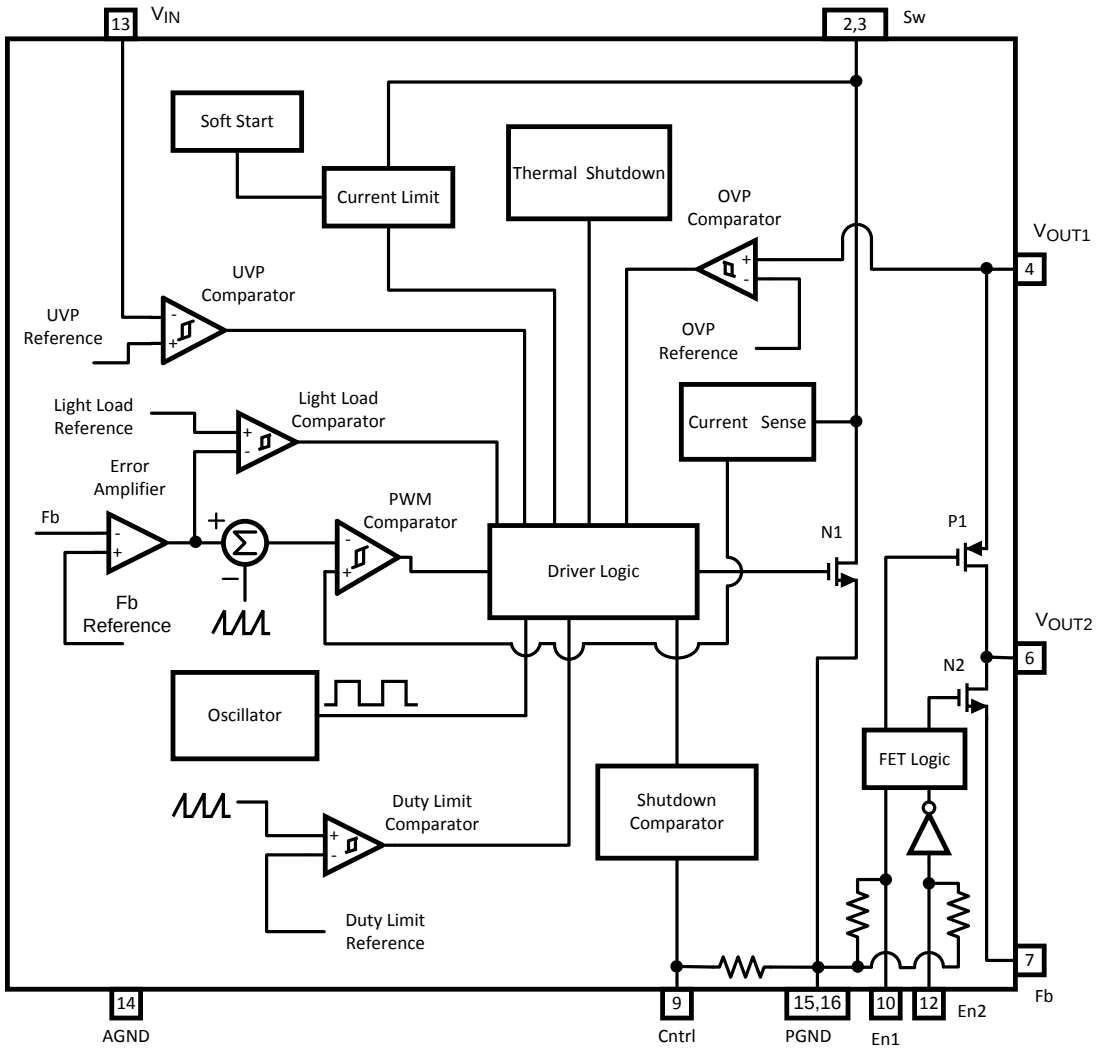


Figure 4. Block Diagram

Detailed Description of Operation

The LM3502 utilizes an asynchronous current mode pulse-width-modulation (PWM) control scheme to regulate the feedback voltage over specified load conditions. The DC/DC converter behaves as a controlled current source for white LED applications. The operation can best be understood by referring to the block diagram in Figure 4 for the following operational explanation. At the start of each cycle, the oscillator sets the driver logic and turns on the internal NMOS power device, N1, conducting current through the inductor and reverse biasing the external diode. The white LED current is supplied by the output capacitor when the internal NMOS power device, N1, is turned on. The sum of the error amplifier's output voltage and an internal voltage ramp are compared with the sensed power NMOS, N1, switch voltage. Once these voltages are equal, the PWM

comparator will then reset the driver logic, thus turning off the internal NMOS power device, N1, and forward biasing the external diode. The inductor current then flows through the diode to the white LED load and output capacitor. The inductor current recharges the output capacitor and supplies the current for the white LED load. The oscillator then resets the driver logic again repeating the process. The output voltage of the error amplifier controls the current through the inductor. This voltage will increase for larger loads and decrease for smaller loads limiting the peak current in the inductor and minimizing EMI radiation. The duty limit comparator is always operational, it prevents the internal NMOS power switch, N1, from being on for more than one oscillator cycle and conducting large amounts of current. The light load comparator allows the LM3502 to properly regulate light/small white LED load currents, where regulation becomes difficult for the LM3502's primary control loop. Under light load conditions, the LM3502 will enter into a pulse skipping pulse-frequency-mode (PFM) of operation where the switching frequency will vary with the load.

The LM3502 has 2 control pins, En1 and En2, used for selecting which segment of a single white LED string network is active for dual display applications. En1 controls the main display (MAIN) segment of the single string white LED network between pins V_{OUT1} and V_{OUT2}. En2 controls the sub display (SUB) segment of the single string white LED network between the V_{OUT2} and Fb. For a quick review of the LM3502 control pin operational characteristics, see Figure 5.

When the Cntrl pin is ≥ 1.4V, the LM3502 will enter in low I_Q state if both En1 and En2 ≤ 0.3V. At this time, both the P1 and N2 FETs will turn off. The output voltage will be a diode drop below the supply voltage and the soft-start will be reset limiting the peak inductor current at the next start-up.

The LM3502 is designed to control the LED current with a PWM signal without the use of an external RC filter. Utilizing special circuitry, the LM3502 can operate over a large range of PWM frequencies without restarting the soft-start allowing for fast recovery at high PWM frequencies. Figure 6 represents a PWM signal driving the Cntrl pin where t_L is defined as the low time of the signal. The following is true:

- If t_L < 12ms (typical): The device will stop switching during this time and the soft-start will not be reset allowing LED current PWM control.
- If t_L > 12ms (typical): The device will shutdown and the soft-start will reset to prevent high peak currents at the next startup. Both the N2 and P1 switches will turn off.

The LM3502 has dedicated protection circuitry active during normal operation to protect the integrated circuit (IC) and external components. The thermal shutdown circuitry turns off the internal NMOS power device, N1, when the internal semiconductor junction temperature reaches excessive levels. The LM3502 has a under-voltage protection (UVP) comparator that disables the internal NMOS power device when battery voltages are too low, thus preventing an on state where the internal NMOS power device conducts large amounts of current. The over-voltage protection (OVP) comparator prevents the output voltage from increasing beyond the protection limit when the white LED string network is removed or if there is a white LED failure. OVP allows for the use of low profile ceramic capacitors at the output. The current though the internal NMOS power device, N1, is monitored to prevent peak inductor currents from damaging the IC. If during a cycle (cycle=1/switching frequency) the peak inductor current exceeds the current limit for the LM3502, the internal NMOS power device will be turned off for the remaining duration of that cycle.

Cntrl*	En1	En2	Result* (See **Figure 1** and **Figure 2**)	Shutdown	
				Shutdown	Low I_Q
1.4V	0.3V	0.3V	**[**P1→OFF N2→OFF N1→OFF**] or [**MAIN→OFF SUB→OFF N1→OFF**]**		X
1.4V	1.4V	0.3V	**[**P1→OFF N2→ON N1→Switching**] or [**MAIN→ON SUB→OFF N1→Switching**]**		
1.4V	0.3V	1.4V	**[**P1→ON N2→OFF N1→Switching**] or [**MAIN→OFF SUB→ON N1→Switching**]**		
1.4V	1.4V	1.4V	**[**P1→OFF N2→OFF N1→Switching**] or [**MAIN→ON SUB→ON N1→Switching**]**		
0.3V	0.3V	0.3V	**[**P1→OFF N2→OFF N1→OFF**] or [**MAIN→OFF SUB→OFF N1→OFF**]**	X	
0.3V	1.4V	0.3V	**[**P1→OFF N2→OFF N1→OFF**] or [**MAIN→OFF SUB→OFF N1→OFF**]**	X	
0.3V	0.3V	1.4V	**[**P1→OFF N2→OFF N1→OFF**] or [**MAIN→OFF SUB→OFF N1→OFF**]**	X	
0.3V	1.4V	1.4V	**[**P1→OFF N2→OFF N1→OFF**] or [**MAIN→OFF SUB→OFF N1→OFF**]**	X	
***Table is only valid for when the Cntrl pin signal is a non-periodic logic signal, not a PWM signal.**					

Figure 5. Operational Characteristics Table

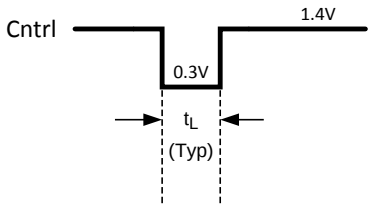


Figure 6. Control Signal Waveform

Typical Performance Characteristics

(Circuit in Figure 1: L = DO1608C-223 and D = MBRM140T3. Efficiency: $\eta = P_{OUT}/P_{IN} = [(V_{OUT} - V_{Fb}) * I_{OUT}]/[V_{IN} * I_{IN}]$. T_A= 25°C, unless otherwise stated.)

I_Q (Non-Switching) vs V_{IN}

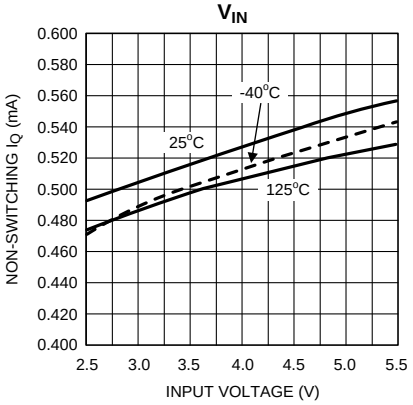


Figure 7.

Switching Frequency vs Temperature

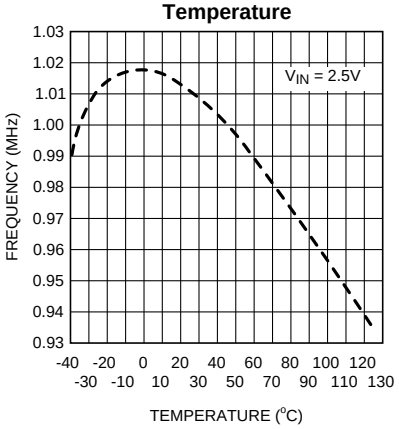


Figure 8.

I_Q (Switching) vs V_{IN}

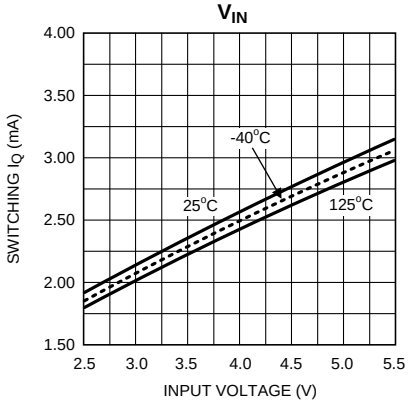


Figure 9.

I_Q (Switching) vs Temperature

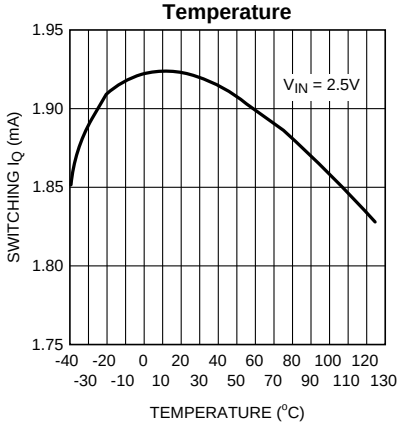


Figure 10.

10 LED Efficiency vs LED Current

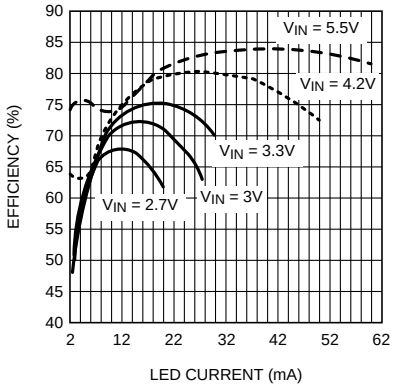


Figure 11.

8 LED Efficiency vs LED Current

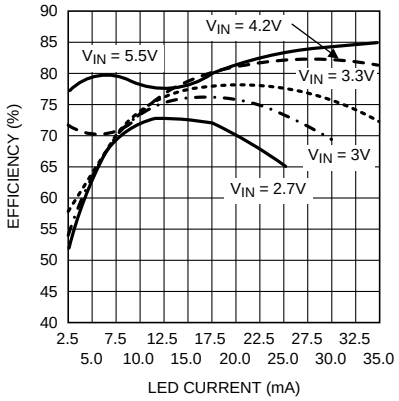


Figure 12.

Typical Performance Characteristics (continued)

(Circuit in Figure 1: L = DO1608C-223 and D = MBRM140T3. Efficiency: $\eta = P_{OUT}/P_{IN} = [(V_{OUT} - V_{Fb}) * I_{OUT}]/[V_{IN} * I_{IN}]$. T_A= 25°C, unless otherwise stated.)

6 LED Efficiency vs LED Current

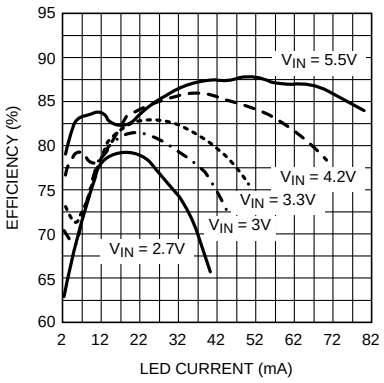


Figure 13.

4 LED Efficiency vs LED Current

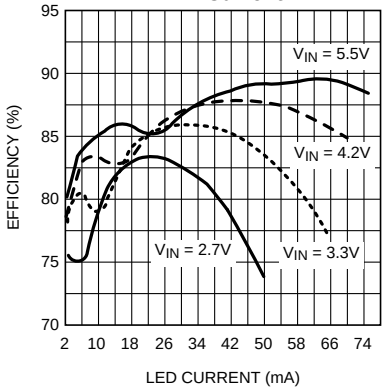


Figure 14.

Cntrl Pin Current vs Cntrl Pin Voltage

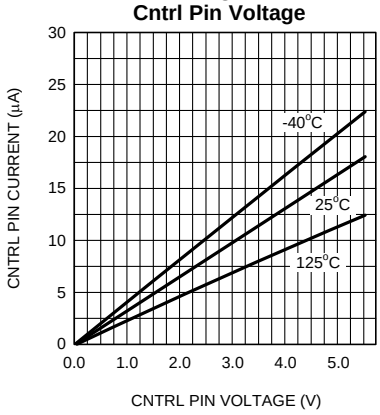


Figure 15.

Maximum Duty Cycle vs Temperature

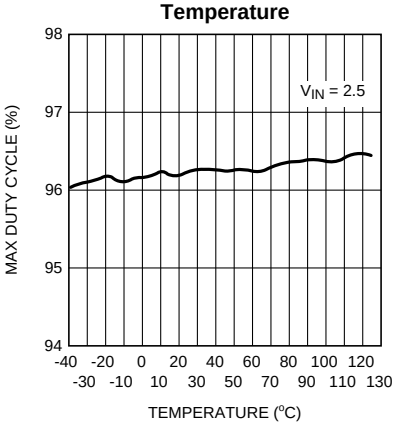


Figure 16.

En1 Pin Current vs En1 Pin Voltage

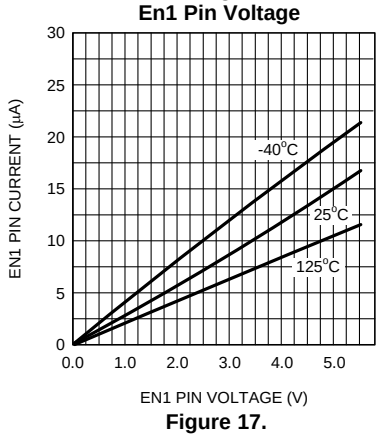


Figure 17.

En2 Pin Current vs En2 Pin Voltage

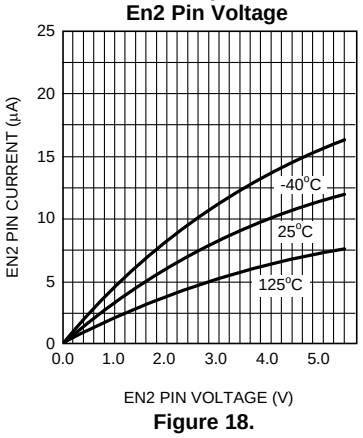


Figure 18.

Typical Performance Characteristics (continued)

(Circuit in Figure 1: L = DO1608C-223 and D = MBRM140T3. Efficiency: η = P_{OUT}/P_{IN} = [(V_{OUT} – V_{Fb}) * I_{OUT}]/[V_{IN} * I_{IN}]. T_A= 25°C, unless otherwise stated.)

V_{OUT1} Pin Current vs V_{OUT1} Pin Voltage

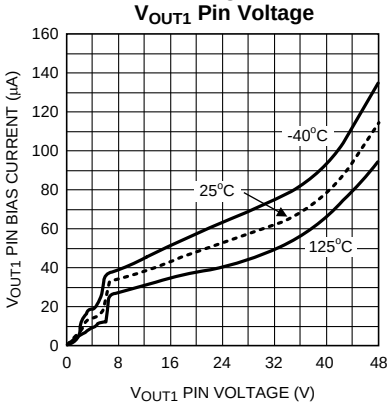


Figure 19.

Power NMOS $R_{DS(ON)}$ (Figure 4: N1) vs V_{IN}

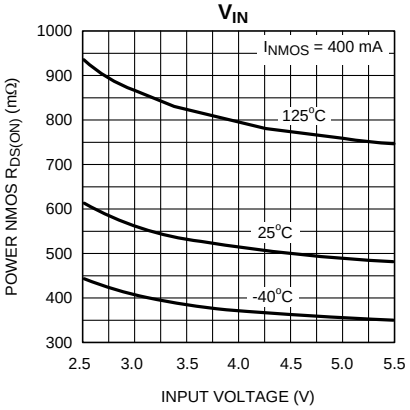


Figure 20.

NMOS $R_{DS(ON)}$ (Figure 4: N2) vs V_{IN}

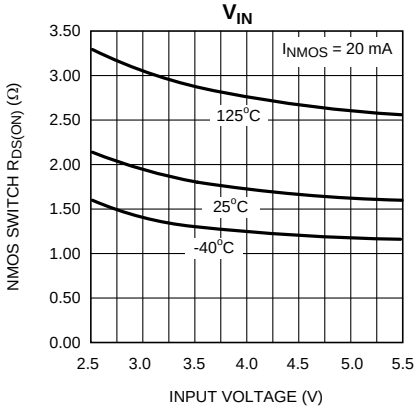


Figure 21.

PMOS $R_{DS(ON)}$ (Figure 4: P1) vs V_{IN}

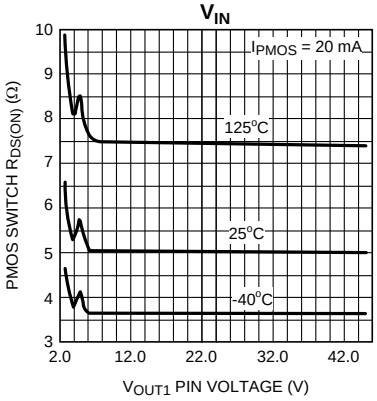


Figure 22.

Feedback Voltage vs Temperature

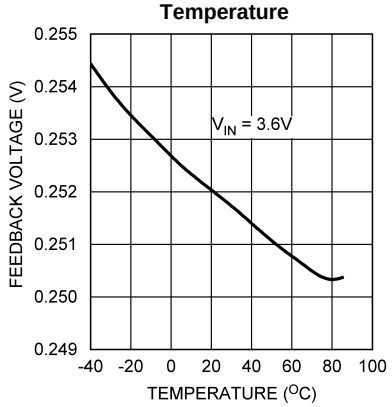


Figure 23.

Current Limit (LM3502-16) vs V_{IN}

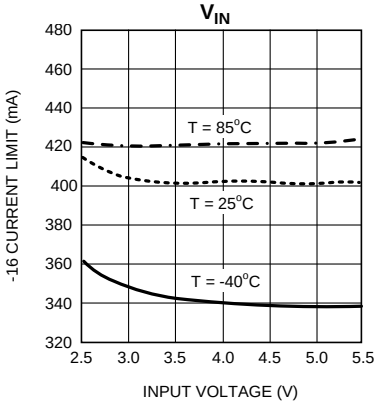


Figure 24.

Typical Performance Characteristics (continued)

(Circuit in Figure 1: L = DO1608C-223 and D = MBRM140T3. Efficiency: η = P_{OUT}/P_{IN} = [(V_{OUT} – V_{Fb}) * I_{OUT}]/[V_{IN} * I_{IN}]. T_A= 25°C, unless otherwise stated.)

Current Limit (LM3502-16) vs Temperature

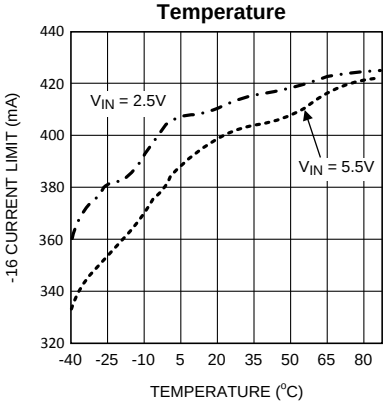


Figure 25.

Current Limit (LM3502-25) vs V_{IN}

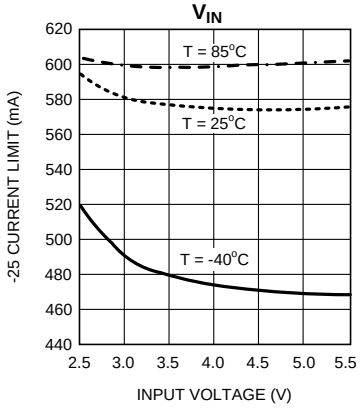


Figure 26.

Current Limit (LM3502-25) vs Temperature

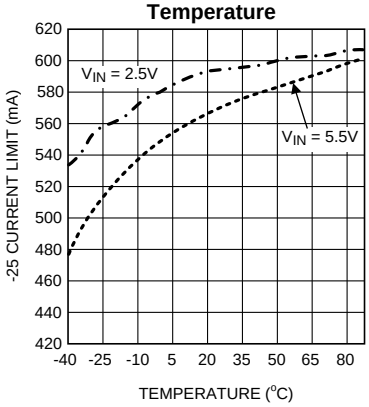


Figure 27.

Current Limit (LM3502-35/44) vs Temperature

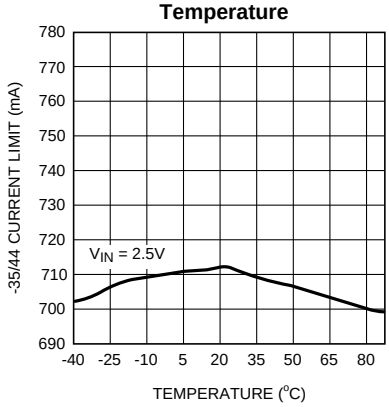


Figure 28.

Current Limit (LM3502-35/44) vs V_{IN}

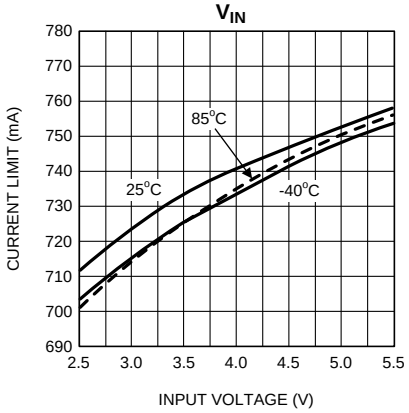


Figure 29.

APPLICATION INFORMATION

WHITE LED CURRENT SETTING

The LED current is set using the following equation:

$$I_{LED} = \frac{V_{Fb}}{R1} \quad (1)$$

where

- I_{LED}: White LED Current.
- V_{Fb}: Feedback Pin Voltage. V_{Fb} = 0.25V, Typical.
- R1: Current Setting Resistor.

WHITE LED DIMMING

For dimming the white LED string with a pulse-width-modulated (PWM) signal on the Cntrl pin, care must taken to balance the tradeoffs between audible noise and white LED brightness control. For best PWM duty cycle vs. white LED current linearity, the PWM frequency should be between 200Hz and 500Hz. Other PWM frequencies can be used, but the linearity over input voltage and duty cycle variation will not be as good as what the 200Hz to 500Hz PWM frequency spectrum provides. To minimize audible noise interference, it is recommended that a output capacitor with minimal susceptibility to piezoelectric induced stresses be used for the particular applications that require minimal or no audible noise interference.

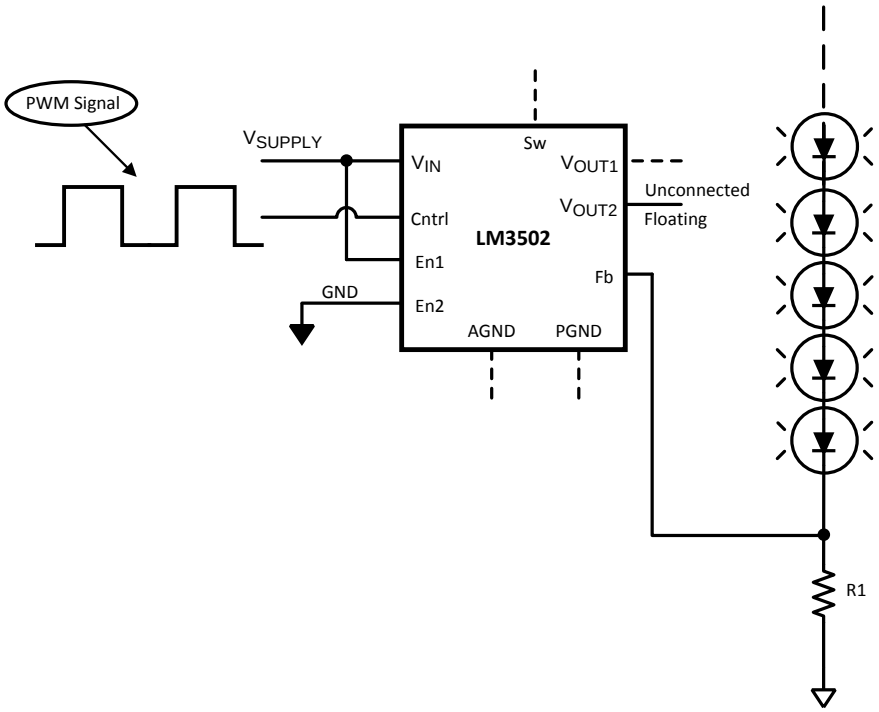


Figure 30.

If V_{OUT2} is not used , En2 must be grounded

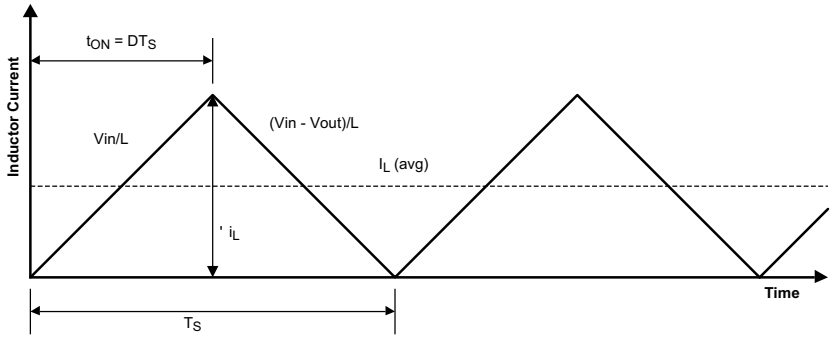


Figure 31. Inductor Current Waveform

CONTINUOUS AND DISCONTINUOUS MODES OF OPERATION

Since the LM3502 is a constant frequency pulse-width-modulated step-up regulator, care must be taken to make sure the maximum duty cycle specification is not violated. The duty cycle equation depends on which mode of operation the LM3502 is in. The two operational modes of the LM3502 are continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Continuous conduction mode refers to the mode of operation where during the switching cycle, the inductor current never goes to and stays at zero for any significant amount of time during the switching cycle. Discontinuous conduction mode refers to the mode of operation where during the switching cycle, the inductor current goes to and stays at zero for a significant amount of time during the switching cycle. Figure 31 illustrates the threshold between CCM and DCM operation. In Figure 31, the inductor current is right on the CCM/DCM operational threshold. Using this as a reference, a factor can be introduced to calculate when a particular application is in CCM or DCM operation. R is a CCM/DCM factor we can use to compute which mode of operation a particular application is in. If R is ≥ 1, then the application is operating in CCM. Conversely, if R is < 1, the application is operating in DCM. The R factor inequalities are a result of the components that make up the R factor. From Figure 31, the R factor is equal to the average inductor current, I_L(avg), divided by half the inductor ripple current, Δi_L. Using Figure 31 the following equation can be used to compute R factor:

$$R = \frac{2 * I_L(avg)}{\Delta i_L}$$

$$I_L(avg) = \frac{[I_{OUT}]}{[(1-D) * Eff]}$$

$$\Delta i_L = \frac{[V_{IN} * D]}{[L * Fs]}$$

$$R = \frac{[2 * I_{OUT} * L * Fs * (V_{OUT})^2]}{[(V_{IN})^2 * Eff * (V_{OUT} - V_{IN})]} \quad (2)$$

where

- V_{IN}: Input Voltage.
- V_{OUT}: Output Voltage.
- Eff: Efficiency of the LM3502.
- Fs: Switching Frequency.
- I_{OUT}: White LED Current/Load Current.
- L: Inductance Magnitude/Inductor Value.
- D: Duty Cycle for CCM Operation.
- Δi_L: Inductor Ripple Current
- I_L(avg): Average Inductor Current

For CCM operation, the duty cycle can be computed with:

$$D = \frac{t_{ON}}{T_S}$$

$$D = \frac{[V_{OUT} - V_{IN}]}{[V_{OUT}]}$$

where

- D: Duty Cycle for CCM Operation.
- V_{OUT}: Output Voltage.
- V_{IN}: Input Voltage. (3)

For DCM operation, the duty cycle can be computed with:

$$D = \frac{t_{ON}}{T_S}$$

$$D = \sqrt{\frac{[2 * I_{OUT} * L * (V_{OUT} - V_{IN}) * Fs]}{[(V_{IN})^2 * Eff]}}$$

where

- D: Duty Cycle for DCM Operation.
- V_{OUT}: Output Voltage.
- V_{IN}: Input Voltage.
- I_{OUT}: White LED Current/Load Current.
- Fs: Switching Frequency.
- L: Inductor Value/Inductance Magnitude. (4)

INDUCTOR SELECTION

In order to maintain inductance, an inductor used with the LM3502 should have a saturation current rating larger than the peak inductor current of the particular application. Inductors with low DCR values contribute decreased power losses and increased efficiency. The peak inductor current can be computed for both modes of operation: CCM and DCM.

The cycle-by-cycle peak inductor current for CCM operation can be computed with:

$$I_{Peak} \approx I_L\,(avg) + \frac{\Delta i_L}{2}$$

$$I_{Peak} \approx \frac{[I_{OUT}]}{[(1 - D) * Eff]} + \frac{[V_{IN} * D]}{[2 * L * Fs]}$$

where

- V_{IN}: Input Voltage.
- Eff: Efficiency of the LM3502.
- Fs: Switching Frequency.
- I_{OUT}: White LED Current/Load Current.
- L: Inductance Magnitude/Inductor Value.
- D: Duty Cycle for CCM Operation.
- I_{PEAK}: Peak Inductor Current.
- Δi_L: Inductor Ripple Current.
- I_L(avg): Average Inductor Current. (5)

The cycle-by-cycle peak inductor current for DCM operation can be computed with:

$$I_{Peak} \approx \frac{[V_{IN} * D]}{[L * Fs]}$$

where

- V_{IN}: Input Voltage.

- Fs: Switching Frequency.
- L: Inductance Magnitude/Inductor Value.
- D: Duty Cycle for DCM Operation.
- I_{PEAK}: Peak Inductor Current. (6)

The minimum inductance magnitude/inductor value for the LM3502 can be calculated using the following, which is only valid when the duty cycle is > 0.5:

$$L > \frac{[V_{IN} * R_{DS(ON)} * ((D/D') - 1)]}{[1.562 * Fs]}$$

where

- D: Duty Cycle.
- D: 1–D.
- $R_{DS(ON)}$: NMOS Power Switch ON
- V_{IN}: Input Voltage.
- L: Inductance Magnitude/Inductor Value. (7)

This equation gives the value required to prevent subharmonic oscillations. The result of this equation and the inductor average and ripple current should be accounted for when choosing an inductor value.

Some recommended inductor manufacturers included but are not limited to:

CoilCraft	DO1608C-223	www.coilcraft.com
	DT1608C-223	

CAPACITOR SELECTION

Multilayer ceramic capacitors are the best choice for use with the LM3502. Multilayer ceramic capacitors have the lowest equivalent series resistance (ESR). Applied voltage or DC bias, temperature, dielectric material type (X7R, X5R, Y5V, etc), and manufacturer component tolerance have an affect on the true or effective capacitance of a ceramic capacitor. Be aware of how your application will affect a particular ceramic capacitor by analyzing the aforementioned factors of your application. Before selecting a capacitor always consult the capacitor manufacturer's data curves to verify the effective or true capacitance in your application.

INPUT CAPACITOR SELECTION

The input capacitor serves as an energy reservoir for the inductor. In addition to acting as an energy reservoir for the inductor the input capacitor is necessary for the reduction in input voltage ripple and noise experienced by the LM3502. The reduction in input voltage ripple and noise helps ensure the LM3502's proper operation, and reduces the effect of the LM3502 on other devices sharing the same supply voltage. To ensure low input voltage ripple, the input capacitor must have an extremely low ESR. As a result of the low input voltage ripple requirement multilayer ceramic capacitors are the best choice. A minimum capacitance of 2.0 µF is required for normal operation, so consult the capacitor manufacturer's data curves to verify whether the minimum capacitance requirement is going to be achieved for a particular application.

OUTPUT CAPACITOR SELECTION

The output capacitor serves as an energy reservoir for the white LED load when the internal power FET switch (Figure 4: N1) is on or conducting current. The requirements for the output capacitor must include worst case operation such as when the load opens up and the LM3502 operates in over-voltage protection (OVP) mode operation. A minimum capacitance of 0.5µF is required to ensure normal operation. Consult the capacitor manufacturer's data curves to verify whether the minimum capacitance requirement is going to be achieved for a particular application.

Some recommended capacitor manufacturers included but are not limited to:

Taiyo Yuden	GMK212BJ105MD (0805/35V)	www.t-yuden.com
muRata	GRM40-035X7R105K (0805/50V)	www.murata.com

TDK	C3216X7R1H105KT (1206/50V)	www.tdktca.com
	C3216X7R1C475K (1206/16V)	
AVX	08053D105MAT (0805/25V)	www.avxcorp.com
	08056D475KAT (0805/6.3V)	
	1206ZD475MAT (1206/10V)	

DIODE SELECTION

To maintain high efficiency it is recommended that the average current rating (I_F or I_O) of the selected diode should be larger than the peak inductor current (I_{Lpeak}). At the minimum, the average current rating of the diode should be larger than the maximum LED current. To maintain diode integrity the peak repetitive forward current (I_{FRM}) must be greater than or equal to the peak inductor current (I_{Lpeak}). Diodes with low forward voltage ratings (V_F) and low junction capacitance magnitudes (C_J or C_T or C_D) are conducive to high efficiency. The chosen diode must have a reverse breakdown voltage rating (V_R and/or V_{RRM}) that is larger than the output voltage (V_{out}). No matter what type of diode is chosen, Schottky or not, certain selection criteria must be followed:

1. V_R and $V_{RRM} > V_{OUT}$
2. I_F or $I_O \geq I_{LOAD}$ or I_{OUT}
3. $I_{FRM} \geq I_{Lpeak}$

Some recommended diode manufacturers included but are not limited to:

Vishay	SS12(1A/20V)	www.vishay.com
	SS14(1A/40V)	
	SS16(1A/60V)	
On Semiconductor	MBRM120E (1A/20V)	www.onsemi.com
	MBRS1540T3 (1.5A/40V)	
	MBR240LT (2A/40V)	
Central Semiconductor	CMSH1- 40M (1A/40V)	www.centralsemi.com

SHUTDOWN AND START-UP

On startup, the LM3502 contains special circuitry that limits the peak inductor current which prevents large current spikes from loading the battery or power supply. When Cntrl ≥ 1.4V and both the En1 and En2 signals are less than 0.3V, the LM3502 will enter a low I_Q state and regulation will end. During this low I_Q mode the output voltage is a diode drop below the supply voltage and the soft-start will be reset to limit the peak inductor current at the next startup. When both En1 and En2 are less than 0.3V, the P1 PMOS and N2 NMOS switches will turn off.

When Cntrl < 0.3V for more than 12ms, typicaly, the LM3502 will shutdown and the output voltage will be a diode drop below the supply voltage. If the Cntrl pin is low for more than 12ms, the soft-start will reset to limit the peak inductor current at the next startup.

When Cntrl is < 0.3 but for less than 12ms, typically, the device will not shutdown and reset the soft-start but shut off the NMOS N1 Power Device to allow for PWM contrl of the LED current.

THERMAL SHUTDOWN

The LM3502 stops regulating when the internal semiconductor junction temperature reaches approximately 140°C. The internal thermal shutdown has approximately 20°C of hysteresis which results in the LM3502 turning back on when the internal semiconductor junction temperature reaches 120°C. When the thermal shutdown temperature is reached, the softstart is reset to prevent inrush current when the die temperature cools.

UNDER VOLTAGE PROTECTION

The LM3502 contains protection circuitry to prevent operation for low input supply voltages. When Vin drops below 2.3V, typically the LM3502 will no longer regulate. In this mode, the output volage will be one diode drop below Vin and the softstart will be reset. When Vin increases above 2.4V, typically, the device will begin regulating again.

OVER VOLTAGE PROTECTION

The LM3502 contains dedicated circuitry for monitoring the output voltage. In the event that the LED network is disconnected from the LM3502, the output voltage will increase and be limited to 15.5V(typ.) for the 16V version , 24V(typ.) for the 25V version, 34V(typ.) for the 35V version and 42V(typ.) for the 44V version (see eletrical table for more details). In the event that the network is reconnected, regulation will resume at the appropriate output voltage.

LAYOUT CONSIDERATIONS

All components, except for the white LEDs, must be placed as close as possible to the LM3502. The die attach pad (DAP) must be soldered to the ground plane.

The input bypass capacitor C_{IN}, as shown in Figure 1, must be placed close to the IC and connect between the V_{IN} and PGND pins. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with C_{IN} to shunt any high frequency noise to ground. The output capacitor, C_{OUT}, must be placed close to the IC and be connected between the V_{OUT1} and PGND pins. Any copper trace connections for the C_{OUT} capacitor can increase the series resistance, which directly effects output voltage ripple and efficiency. The current setting resistor, R1, should be kept close to the Fb pin to minimize copper trace connections that can inject noise into the system. The ground connection for the current setting resistor network should connect directly to the PGND pin. The AGND pin should be tied directly to the PGND pin. Trace connections made to the inductor should be minimized to reduce power dissipation and increase overall efficiency while reducing EMI radiation. For more details regarding layout guidelines for switching regulators, refer to Applications Note AN-1149.

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3502ITL-16/NOPB	LIFEBUY	DSBGA	YPA	10	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SANB	
LM3502ITL-25/NOPB	LIFEBUY	DSBGA	YPA	10	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SAPB	
LM3502ITL-44/NOPB	LIFEBUY	DSBGA	YPA	10	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	SDLB	
LM3502SQ-16/NOPB	LIFEBUY	WQFN	RGH	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00048B	
LM3502SQ-25/NOPB	LIFEBUY	WQFN	RGH	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00049B	
LM3502SQ-35/NOPB	LIFEBUY	WQFN	RGH	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00044B	
LM3502SQ-44/NOPB	LIFEBUY	WQFN	RGH	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00050B	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

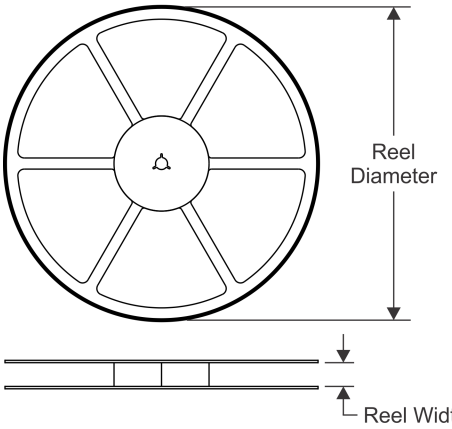
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

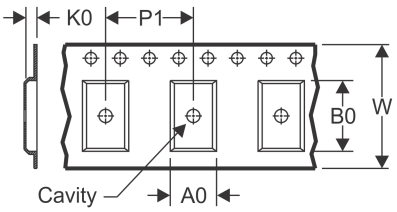
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

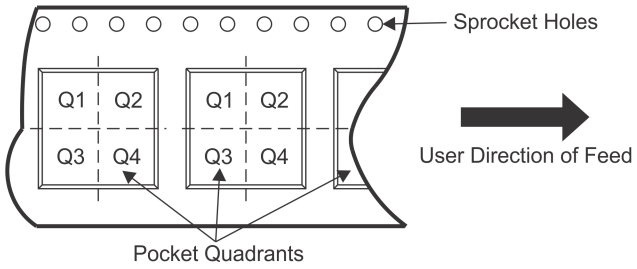


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

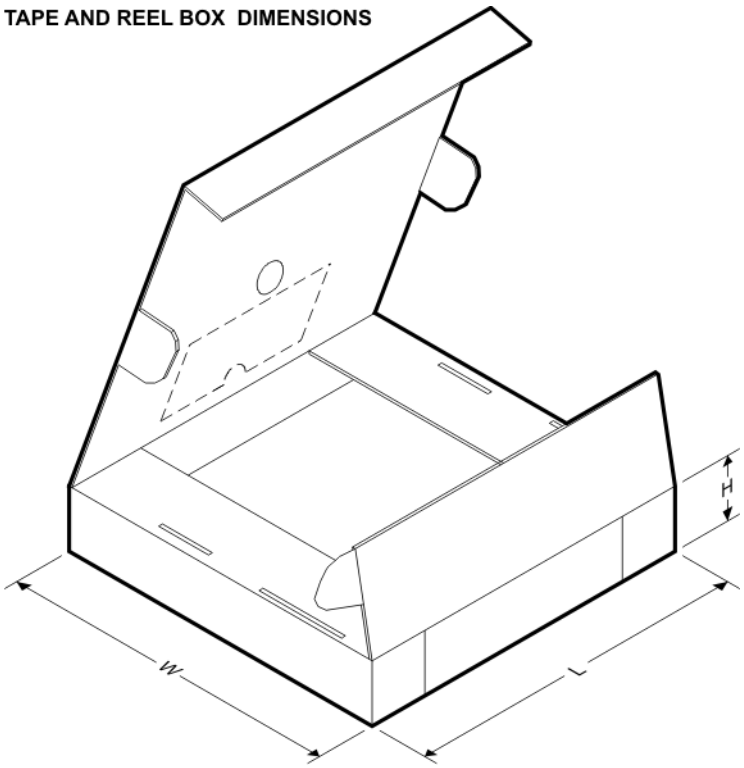
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

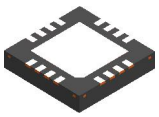
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3502ITL-16/NOPB	DSBGA	YPA	10	250	178.0	8.4	2.03	2.21	0.76	4.0	8.0	Q1
LM3502ITL-25/NOPB	DSBGA	YPA	10	250	178.0	8.4	2.03	2.21	0.76	4.0	8.0	Q1
LM3502ITL-44/NOPB	DSBGA	YPA	10	250	178.0	8.4	2.03	2.21	0.76	4.0	8.0	Q1
LM3502SQ-16/NOPB	WQFN	RGH	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM3502SQ-25/NOPB	WQFN	RGH	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM3502SQ-35/NOPB	WQFN	RGH	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM3502SQ-44/NOPB	WQFN	RGH	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

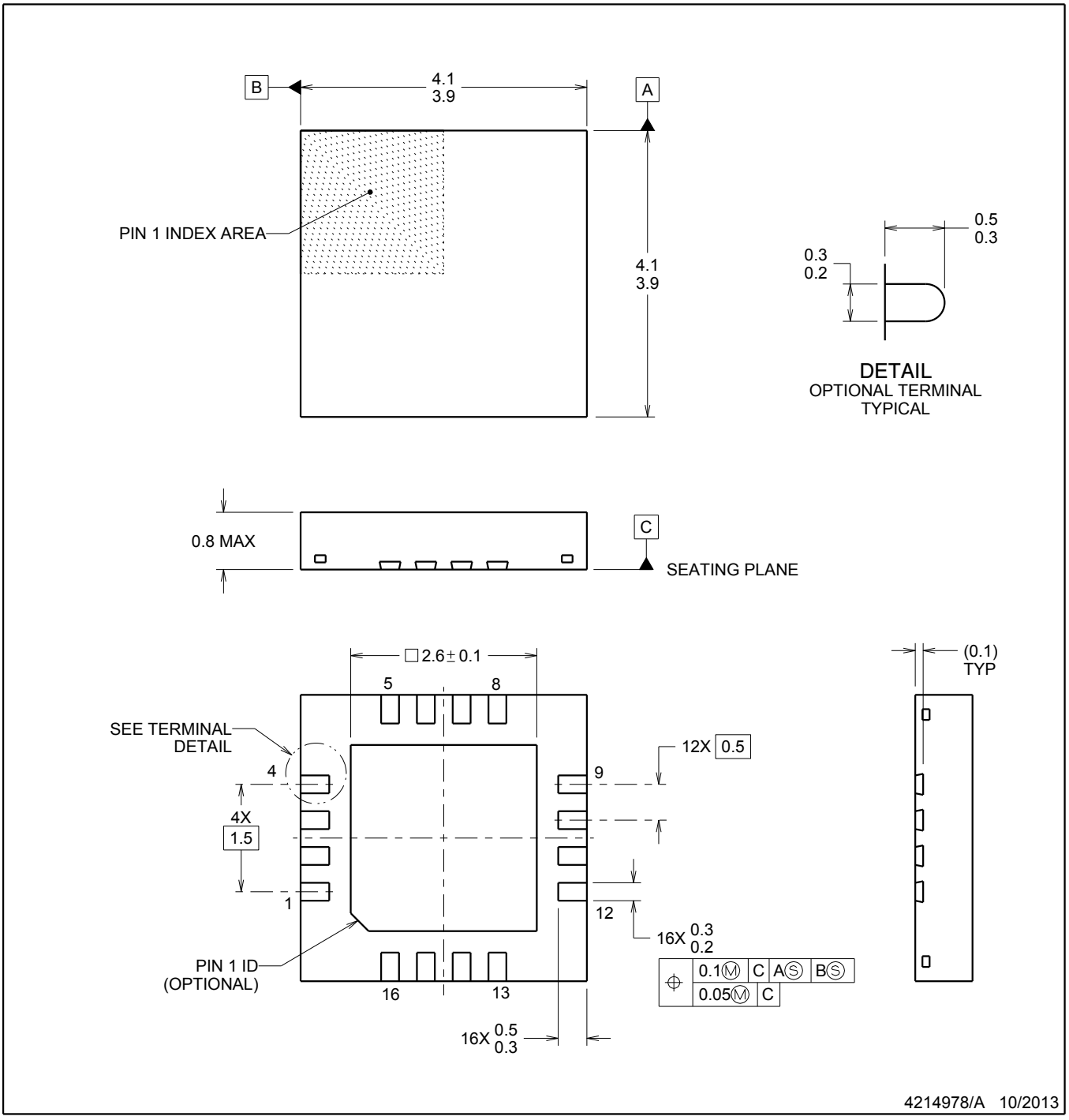
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3502ITL-16/NOPB	DSBGA	YPA	10	250	210.0	185.0	35.0
LM3502ITL-25/NOPB	DSBGA	YPA	10	250	210.0	185.0	35.0
LM3502ITL-44/NOPB	DSBGA	YPA	10	250	210.0	185.0	35.0
LM3502SQ-16/NOPB	WQFN	RGH	16	1000	210.0	185.0	35.0
LM3502SQ-25/NOPB	WQFN	RGH	16	1000	210.0	185.0	35.0
LM3502SQ-35/NOPB	WQFN	RGH	16	1000	210.0	185.0	35.0
LM3502SQ-44/NOPB	WQFN	RGH	16	1000	210.0	185.0	35.0



RGH0016A

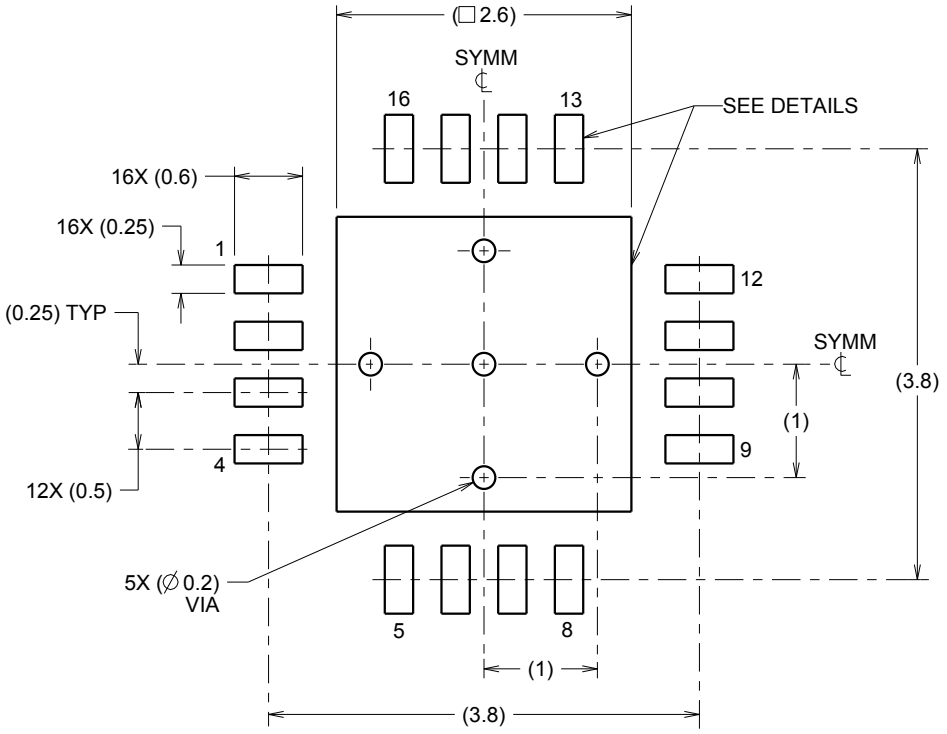
WQFN - 0.8 mm max height

WQFN

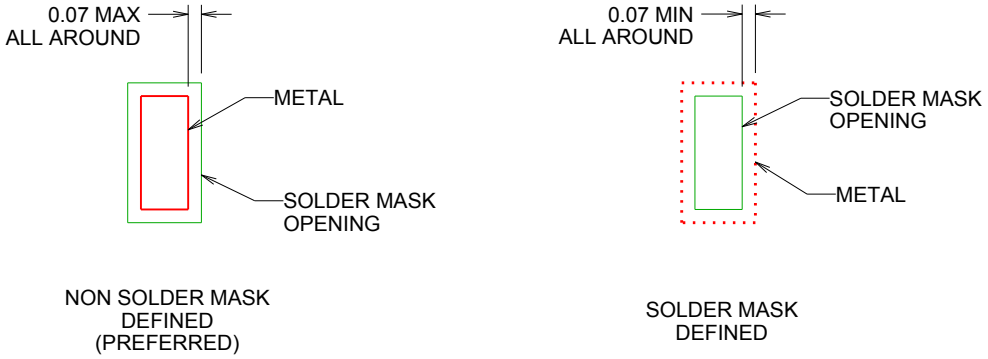


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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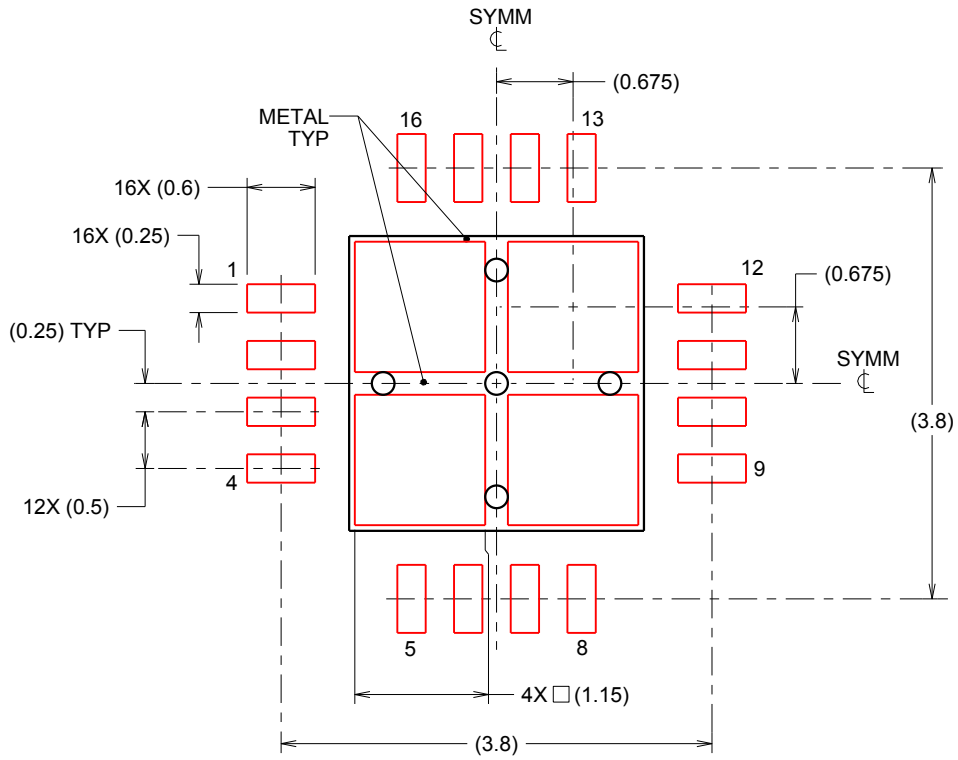
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

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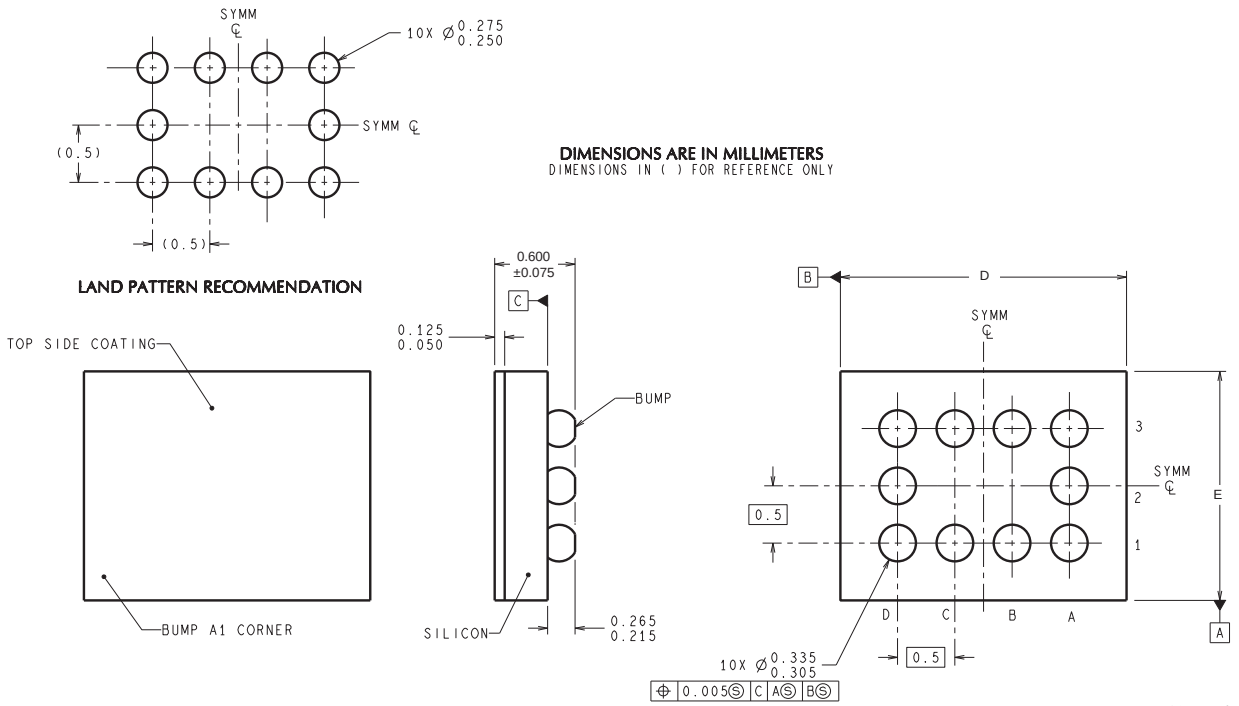
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YPA0010



TLP10XXX (Rev D)

D: Max = 2.124 mm, Min =2.063 mm

E: Max = 1.946 mm, Min =1.885 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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