



THE DATASHEET OF LM348DR

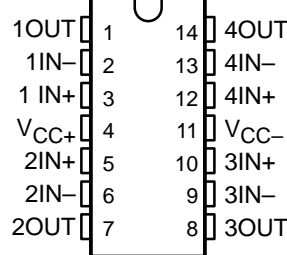


LM148, LM248, LM348 QUADRUPLE OPERATIONAL AMPLIFIERS

SLOS058C – OCTOBER 1979 – REVISED DECEMBER 2002

- μ A741 Operating Characteristics
- Low Supply-Current Drain . . . 0.6 mA Typ (per amplifier)
- Low Input Offset Voltage
- Low Input Offset Current
- Class AB Output Stage
- Input/Output Overload Protection
- Designed to Be Interchangeable With Industry Standard LM148, LM248, and LM348

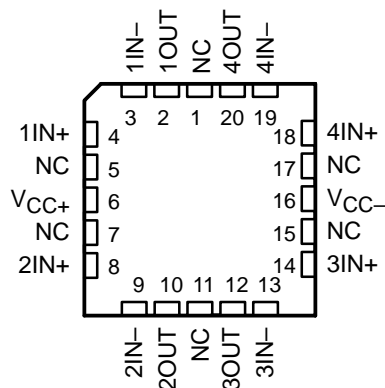
LM148 . . . J PACKAGE
LM248 . . . D OR N PACKAGE
LM348 . . . D, N, OR NS PACKAGE
(TOP VIEW)



description/ordering information

The LM148, LM248, and LM348 are quadruple, independent, high-gain, internally compensated operational amplifiers designed to have operating characteristics similar to the μ A741. These amplifiers exhibit low supply-current drain and input bias and offset currents that are much less than those of the μ A741.

LM148 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

| T _A | V _{IO} max AT 25°C | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|--------------------------------|-----------|--------------|--------------------------|---------------------|
| | | | | | |
| 0°C to 70°C | 6 mV | PDIP (N) | Tube of 25 | LM348N | LM348N |
| | | SOIC (D) | Tube of 50 | LM348D | LM348 |
| | | | Reel of 2500 | LM348DR | |
| –25°C to 85°C | 6 mV | SOP (NS) | Reel of 2000 | LM348NSR | LM348 |
| | | PDIP (N) | Tube of 25 | LM248N | LM248N |
| | | | SOIC (D) | Tube of 50 | LM248D |
| Reel of 2500 | LM248DR | | | | |
| –55°C to 125°C | 5 mV | CDIP (J) | Tube of 25 | LM148J | LM148J |
| | | LCCC (FK) | Tube of 50 | LM148FK | LM148FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

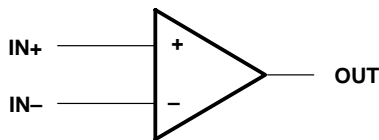
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

LM148, LM248, LM348 QUADRUPLE OPERATIONAL AMPLIFIERS

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symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | | | |
|---|--------------|-------|----------------|
| Supply voltage, V_{CC+} (see Note 1): | LM148 | | 22 V |
| | LM248, LM348 | | 18 V |
| Supply voltage, V_{CC-} (see Note 1): | LM148 | | -22 V |
| | LM248, LM348 | | -18 V |
| Differential input voltage, V_{ID} (see Note 2): | LM148 | | 44 V |
| | LM248, LM348 | | 36 V |
| Input voltage, V_I (either input, see Notes 1 and 3): | LM148 | | -22 V |
| | LM248, LM348 | | -18 V |
| Duration of output short circuit (see Note 4) | | | Unlimited |
| Operating virtual junction temperature, T_J | | | 150°C |
| Package thermal impedance, θ_{JA} (see Notes 5 and 6): | D package | | 86°C/W |
| | N package | | 80°C/W |
| | NS package | | 76°C/W |
| Package thermal impedance, θ_{JC} (see Notes 7 and 8): | FK package | | 5.61°C/W |
| | J package | | 15.05°C/W |
| Case temperature for 60 seconds: FK package | | | 260°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J package | | | 300°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, N, or NS package | | | 260°C |
| Storage temperature range, T_{stg} | | | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$.
 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or the value specified in the table, whichever is less.
 4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
 5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 6. The package thermal impedance is calculated in accordance with JESD 51-7.
 7. Maximum power dissipation is a function of $T_J(max)$, θ_{JC} , and T_C . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 8. The package thermal impedance is calculated in accordance with MIL-STD-883.

recommended operating conditions

| | MIN | MAX | UNIT |
|---------------------------|-----|-----|------|
| Supply voltage, V_{CC+} | 4 | 18 | V |
| Supply voltage, V_{CC-} | -4 | -18 | V |



electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

| PARAMETER | TEST CONDITION [†] | LM148 | | | LM248 | | |
|--|---|----------|----------|-----|----------|----------|-----|
| | | MIN | TYP | MAX | MIN | TYP | MAX |
| V_{IO} Input offset voltage | $V_O = 0$ 25°C Full range | 1 | 5 | 5 | 1 | 1 | 6 |
| I_{IO} Input offset current | $V_O = 0$ 25°C Full range | 4 | 25 | 75 | 4 | 4 | 50 |
| I_B Input bias current | $V_O = 0$ 25°C Full range | 30 | 100 | 325 | 30 | 30 | 200 |
| V_{ICR} Common-mode input voltage range | Full range | ± 12 | | | ± 12 | | |
| V_{OM} Maximum peak output voltage swing | $R_L = 10$ k Ω 25°C | ± 12 | ± 13 | | ± 12 | ± 13 | |
| | $R_L \geq 10$ k Ω Full range | ± 12 | | | ± 12 | | |
| | $R_L = 2$ k Ω 25°C | ± 10 | ± 12 | | ± 10 | ± 12 | |
| | $R_L \geq 2$ k Ω Full range | ± 10 | | | ± 10 | | |
| AVD Large-signal differential voltage amplification | $V_O = \pm 10$ V, $R_L \geq 2$ k Ω 25°C Full range | 50 | 160 | | 25 | 160 | 21 |
| r_i Input resistance [‡] | | 25 | | | 15 | | 11 |
| B_1 Unity-gain bandwidth | AVD = 1 25°C | 0.8 | 2.5 | | 0.8 | 2.5 | 0.1 |
| ϕ_m Phase margin | AVD = 1 25°C | | | | | 60° | |
| CMRR Common-mode rejection ratio | $V_{IC} = V_{ICRmin}$, $V_O = 0$ 25°C Full range | 70 | 90 | | 70 | 90 | 71 |
| kSVR Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$) | $V_{CC\pm} = \pm 9$ V to ± 15 V, $V_O = 0$ 25°C Full range | 77 | 96 | | 77 | 96 | 77 |
| IOS Short-circuit output current | | 77 | | | 77 | | 77 |
| ICC Supply current (four amplifiers) | $V_O = 0$ | | ± 25 | | | ± 25 | |
| | $V_O = V_{OM}$ | | | | | | |
| V_{O1}/V_{O2} Crosstalk attenuation | No load f = 1 Hz to 20 kHz | 2.4 | 3.6 | | 2.4 | 4.5 | |
| | | 120 | | | 120 | | |

[†] All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for LM148, -25°C to 85°C for LM248, and 0°C to 70°C for LM348.

[‡] This parameter is not production tested.

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operating characteristics, $V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|---|-----|-----|-----|------------------------|
| SR Slew rate at unity gain | $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, See Figure 1 | | 0.5 | | $\text{V}/\mu\text{s}$ |

PARAMETER MEASUREMENT INFORMATION

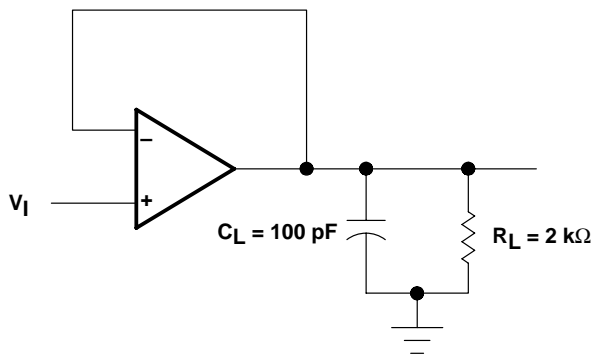


Figure 1. Unity-Gain Amplifier

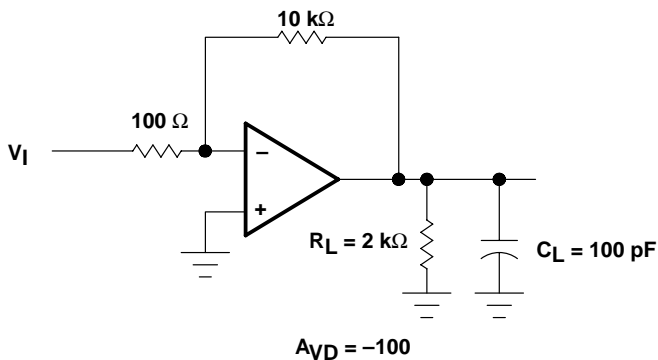


Figure 2. Inverting Amplifier

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LM148FKB | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | LM148FKB | Samples |
| LM148J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | LM148J | Samples |
| LM148JB | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | LM148JB | Samples |
| LM248D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -25 to 85 | LM248 | Samples |
| LM248DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -25 to 85 | LM248 | Samples |
| LM248N | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -25 to 85 | LM248N | Samples |
| LM348D | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LM348 | Samples |
| LM348DG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LM348 | Samples |
| LM348DR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LM348 | Samples |
| LM348DRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LM348 | Samples |
| LM348DRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LM348 | Samples |
| LM348N | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | LM348N | Samples |
| LM348NSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LM348 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM248DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| LM348DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| LM348DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| LM348NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM248DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| LM348DR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| LM348DR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| LM348NSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



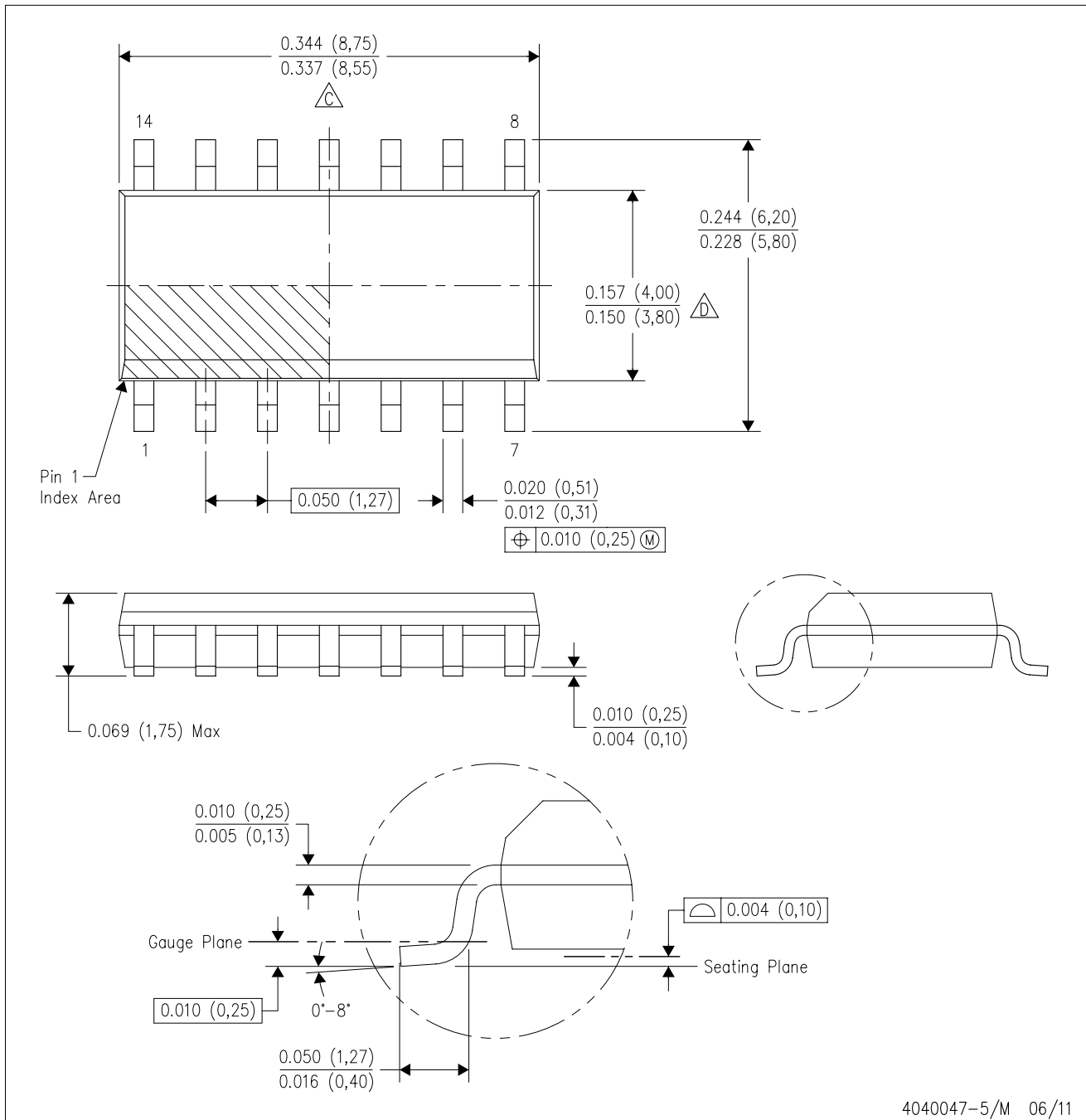
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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