THE DATASHEET OF

LM3445M/NOPB

LM3445 TRIAC Dimmable Offline LED Driver

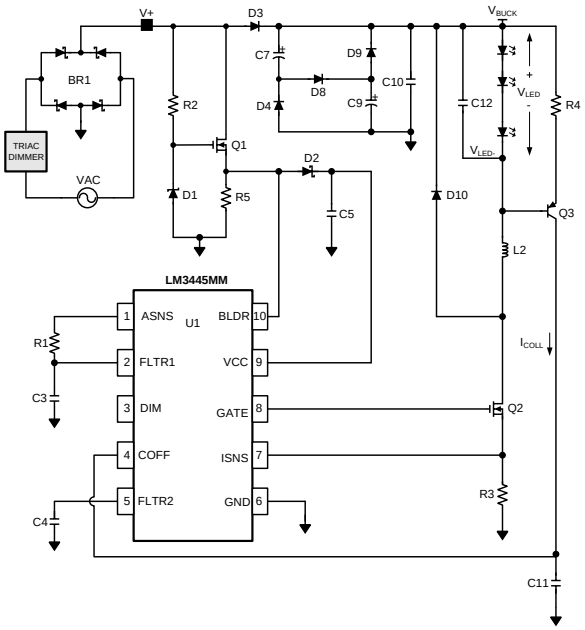
1 Features

- TRIAC Dim Decoder Circuit for LED Dimming
- Application Voltage Range 80 V_{AC} to 277 V_{AC}
- Capable of Controlling LED Currents Greater Than 1 A
- Adjustable Switching Frequency
- Low Quiescent Current
- Adaptive Programmable Off-Time Allows for Constant Ripple Current
- Thermal Shutdown
- No 120-Hz Flicker
- Low Profile 10-Pin VSSOP Package or 14-Pin SOIC
- Patented Drive Architecture

2 Applications

- Retro Fit TRIAC Dimming
- Solid State Lighting
- Industrial and Commercial Lighting
- Residential Lighting

Typical LM3445 LED Driver Application Circuit



3 Description

The LM3445 is an adaptive constant off-time AC/DC buck (step-down) constant current controller designed to be compatible with TRIAC dimmers. The LM3445 provides a constant current for illuminating high power LEDs and includes a TRIAC dim decoder. The dim decoder allows wide range LED dimming using standard TRIAC dimmers. The high frequency capable architecture allows the use of small external passive components. The LM3445 includes a bleeder circuit to ensure proper TRIAC operation by allowing current flow while the line voltage is low to enable proper firing of the TRIAC. A passive PFC circuit ensures good power factor by drawing current directly from the line for most of the cycle, and provides a constant positive voltage to the buck regulator. Additional features include thermal shutdown, current limit and V_{CC} under-voltage lockout.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3445	VSSOP (10)	3.00 mm × 3.00 mm
	SOIC (14)	3.91 mm × 8.65 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency vs Line Voltage

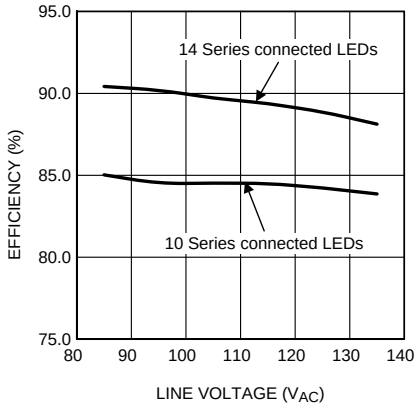


Table of Contents

4 Revision History

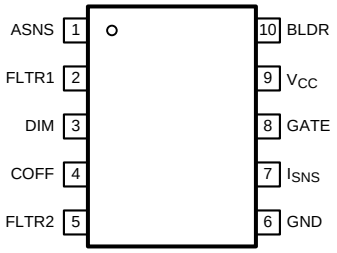
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (May 2013) to Revision M	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Removed maximum lead temperature (soldering).	4

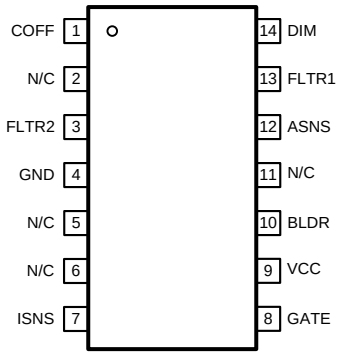
Changes from Revision K (May 2013) to Revision L	Page
• Changed layout of National Data Sheet to TI format	32

5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



D Package
14-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC	VSSOP		
ASNS	12	1	O	PWM output of the TRIAC dim decoder circuit. Outputs a 0 to 4-V PWM signal with a duty cycle proportional to the TRIAC dimmer on-time.
BLDR	10	10	I	Bleeder pin. Provides the input signal to the angle detect circuitry as well as a current path through a switched 230-Ω resistor to ensure proper firing of the TRIAC dimmer.
COFF	1	4	I	OFF time setting pin. A user set current and capacitor connected from the output to this pin sets the constant OFF time of the switching controller.
DIM	14	3	I/O	Input/output dual function dim pin. This pin can be driven with an external PWM signal to dim the LEDs. It may also be used as an output signal and connected to the DIM pin of other LM3445s or other LED drivers to dim multiple LED circuits simultaneously.
FLTR1	13	2	I	First filter input. The 120-Hz PWM signal from ASNS is filtered to a DC signal and compared to a 1 to 3 V, 5.85-kHz ramp to generate a higher frequency PWM signal with a duty cycle proportional to the TRIAC dimmer firing angle. Pull above 4.9-V (typical) to tri-state DIM.
FLTR2	3	5	I	Second filter input. A capacitor tied to this pin filters the PWM dimming signal to supply a DC voltage to control the LED current. Could also be used as an analog dimming input.
GATE	8	8	O	Power MOSFET driver pin. This output provides the gate drive for the power switching MOSFET of the buck controller.
GND	4	6	—	Circuit ground connection
ISNS	7	7	I	LED current sense pin. Connect a resistor from main switching MOSFET source, ISNS to GND to set the maximum LED current.
N/C	2, 5, 6, 11	—	—	No Connect
VCC	9	9	O	Input voltage pin. This pin provides the power for the internal control circuitry and gate driver.

6 Specifications

6.1 Absolute Maximum Ratings

See(1) (2)(3)

	MIN	MAX	UNIT
BLDR to GND	–0.3	17	V
V_{CC}, GATE, FLTR1 to GND	–0.3	14	V
ISNS to GND	–0.3	2.5	V
ASNS, DIM, FLTR2, COFF to GND	–0.3	7	V
COFF Input Current		100	mA
Continuous Power Dissipation(4)		Internally Limited	
Junction Temperature (T_{J-MAX})		150	°C
Storage Temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) All voltages are with respect to the potential at the GND pin, unless otherwise specified.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typ.) and disengages at +T_J = 145°C (typ).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human Body Model, applicable std. JESD22-A114-C.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
V_{CC}	8	12	V
Junction Temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM3445		UNIT
		DGS (VSSOP)	D (SOIC)	
		10 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	159	82.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.5	40.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.7	37.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.3	6.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.5	37.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

All Typical limits are for T_J = 25°C and all Maximum and Minimum limits apply over the full Operating Temperature Range (T_J = −40°C to +125°C). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = +25ºC, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BLEEDER						
R_{BLDR}	Bleeder resistance to GND	I_{BLDR} = 10 mA		230	325	Ω
V_{CC} SUPPLY						
I_{VCC}	Operating supply current			2	2.85	mA
$V_{CC\text{-}UVLO}$	Rising threshold			7.4	7.7	V
	Falling threshold		6	6.4		
	Hysterisis			1		
COFF						
V_{COFF}	Time out threshold		1.225	1.276	1.327	V
R_{COFF}	Off timer sinking impedance			33	60	Ω
t_{COFF}	Restart timer			180		µs
CURRENT LIMIT						
V_{ISNS}	ISNS limit threshold		1.174	1.269	1.364	V
t_{ISNS}	Leading edge blanking time			125		ns
	Current limit reset delay			180		µs
	ISNS limit to GATE delay	ISNS = 0 to 1.75-V step		33		ns
INTERNAL PWM RAMP						
f_{RAMP}	Frequency			5.85		kHz
V_{RAMP}	Valley voltage		0.96	1	1.04	V
	Peak voltage		2.85	3	3.08	
D_{RAMP}	Maximum duty cycle		96.5%	98%		
DIM DECODER						
t_{ANG_DET}	Angle detect rising threshold	Observed on BLDR pin	6.79	7.21	7.81	V
V_{ASNS}	ASNS filter delay			4		µs
	ASNS VMAX		3.85	4	4.15	V
I_{ASNS}	ASNS drive capability sink	V_{ASNS} = 2 V		7.6		mA
	ASNS drive capability source	V_{ASNS} = 2 V		–4.3		
	DIM low sink current	V_{DIM} = 1 V	1.65	2.8		
	DIM High source current	V_{DIM} = 4 V		–4	–3	
V_{DIM}	DIM low voltage	PWM input voltage threshold	0.9	1.33		V
	DIM high voltage			2.33	3.15	
V_{TSTH}	Tri-state threshold voltage	Apply to FLTR1 pin		4.87	5.25	V
R_{DIM}	DIM comparator tri-state impedance		10			MΩ
CURRENT SENSE COMPARATOR						
V_{FLTR2}	FLTR2 open circuit voltage		720	750	780	mV
R_{FLTR2}	FLTR2 impedance			420		kΩ
V_{OS}	Current sense comparator offset voltage		–4	0.1	4	mV
GATE DRIVE OUTPUT						
V_{DRVH}	GATE high saturation	I_{GATE} = 50 mA		0.24	0.5	V
V_{DRVL}	GATE low saturation	I_{GATE} = 100 mA		0.22	0.5	
I_{DRV}	Peak souce current	GATE = V_{CC}/2		–0.77		A
	Peak sink current	GATE = V_{CC}/2		0.88		

Electrical Characteristics (continued)

All Typical limits are for T_J = 25°C and all Maximum and Minimum limits apply over the full Operating Temperature Range (T_J = −40°C to +125°C). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = +25ºC, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DV}	Rise time	C_{load} = 1 nF		15		ns
	Fall time	C_{load} = 1 nF		15		
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature	See (1)		165		°C
	Thermal shutdown hysteresis			20		

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

6.6 Typical Characteristics

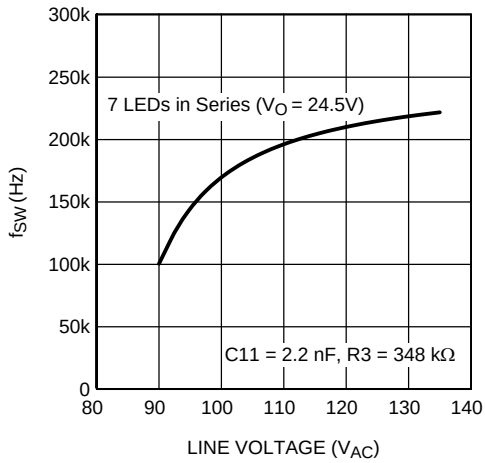


Figure 1. f_{SW} vs Input Line Voltage

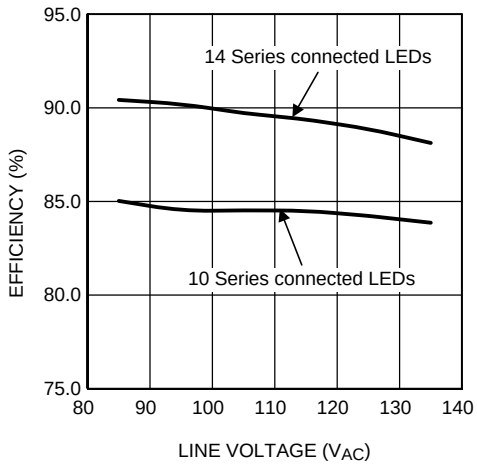


Figure 2. Efficiency vs Input Line Voltage

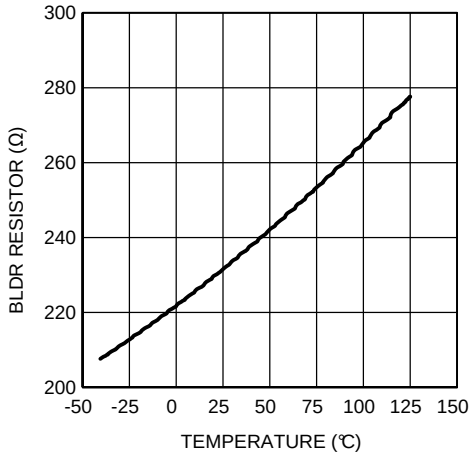


Figure 3. BLDR Resistor vs Temperature

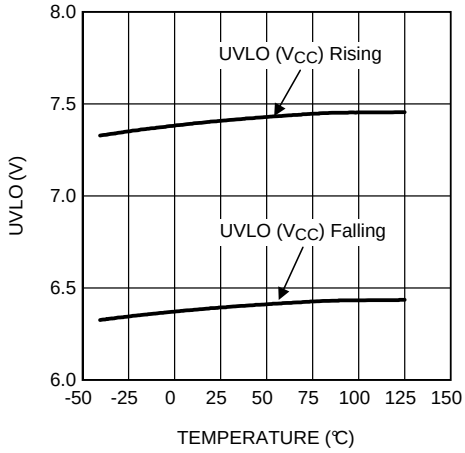


Figure 4. V_{CC} UVLO vs Temperature

Typical Characteristics (continued)

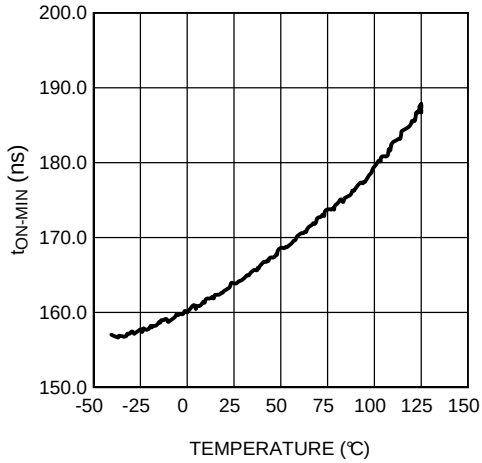


Figure 5. Min On-Time (t_{ON}) vs Temperature

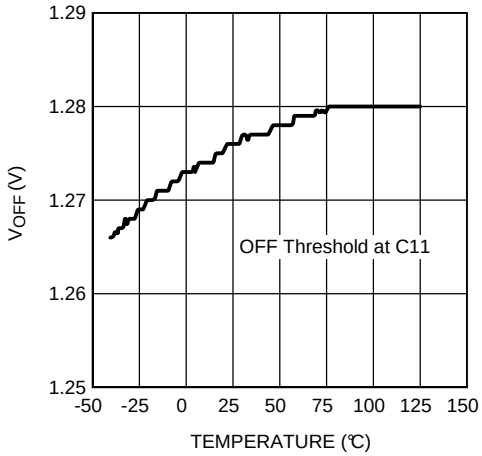


Figure 6. Off Threshold (C11) vs Temperature

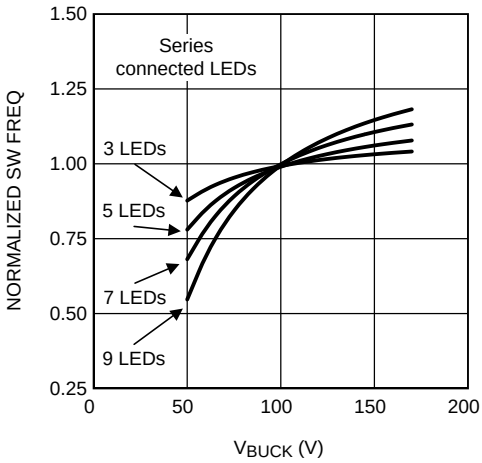


Figure 7. Normalized Variation in f_{SW} over V_{BUCK} Voltage

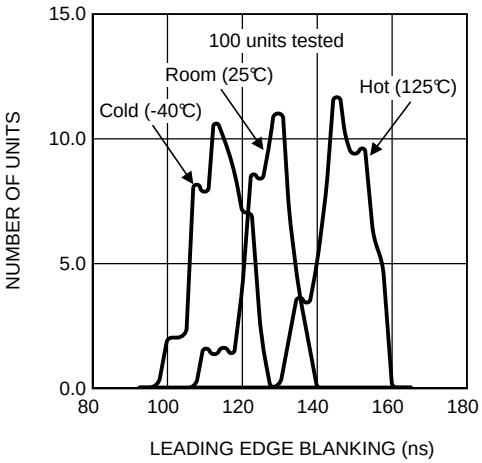


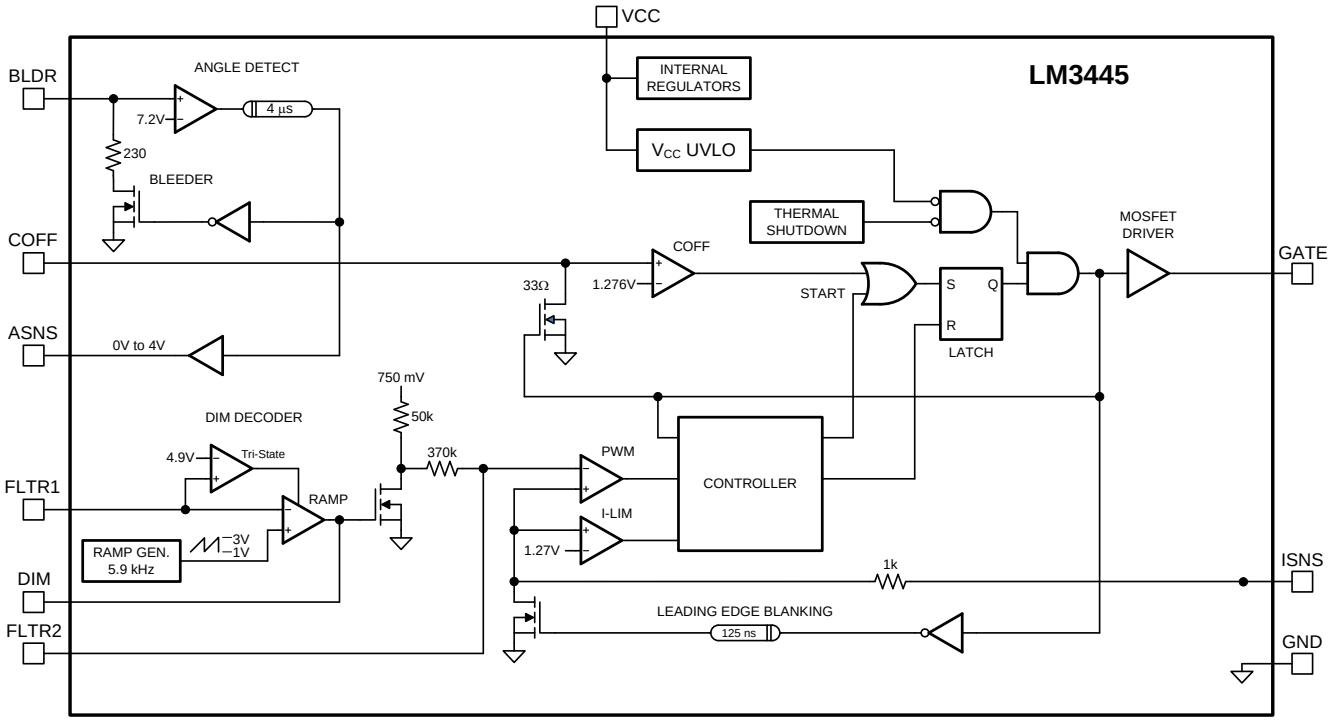
Figure 8. Leading Edge Blanking Variation Over Temperature

7 Detailed Description

7.1 Overview

The LM3445 contains all the necessary circuitry to build a line-powered (mains powered) constant current LED driver whose output current can be controlled with a conventional TRIAC dimmer.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Overview of Phase Control Dimming

A basic phase controlled TRIAC dimmer circuit is shown in Figure 9.

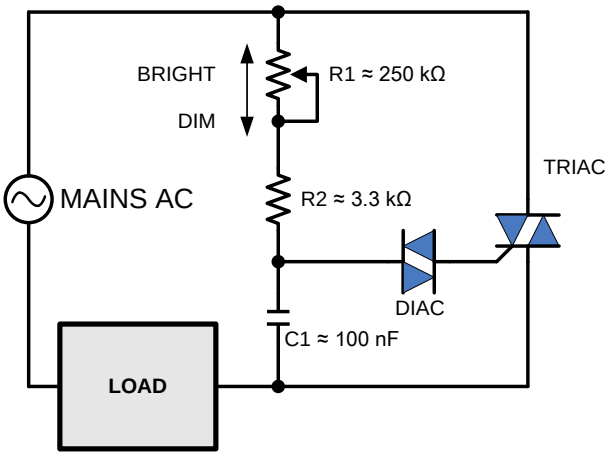


Figure 9. Basic TRIAC Dimmer

Feature Description (continued)

An RC network consisting of R1, R2, and C1 delay the turn on of the TRIAC until the voltage on C1 reaches the trigger voltage of the diac. Increasing the resistance of the potentiometer (wiper moving downward) increases the turn-on delay which decreases the on-time or conduction angle of the TRIAC (θ). This reduces the average power delivered to the load. Voltage waveforms for a simple TRIAC dimmer are shown in Figure 10. Figure 10a shows the full sinusoid of the input voltage. Even when set to full brightness, few dimmers will provide 100% on-time, i.e., the full sinusoid.

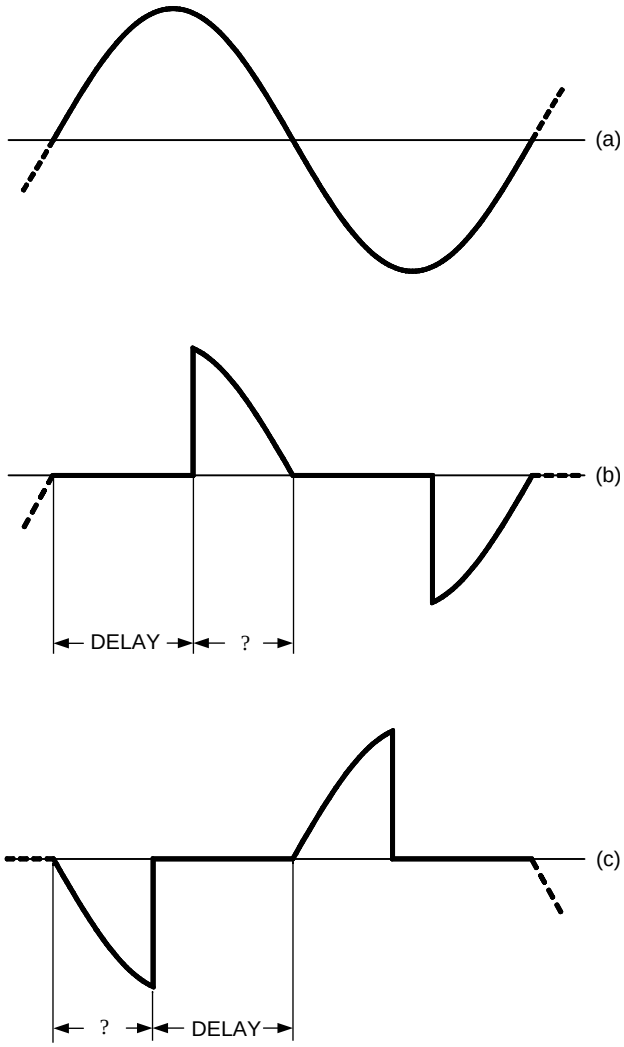


Figure 10. Line Voltage and Dimming Waveforms

Figure 10b shows a theoretical waveform from a dimmer. The on-time is often referred to as the conduction angle and may be stated in degrees or radians. The off-time represents the delay caused by the RC circuit feeding the TRIAC. The off-time be referred to as the firing angle and is simply 180° - θ.

Figure 10c shows a waveform from a so-called reverse phase dimmer, sometimes referred to as an electronic dimmer. These typically are more expensive, microcontroller based dimmers that use switching elements other than TRIACs. Note that the conduction starts from the zero-crossing, and terminates some time later. This method of control reduces the noise spike at the transition.

Since the LM3445 has been designed to assess the relative on-time and control the LED current accordingly, most phase-control dimmers, both forward and reverse phase, may be used with success.

Feature Description (continued)

7.3.2 Theory of Operation

Refer to Figure 11 which shows the LM3445 along with basic external circuitry.

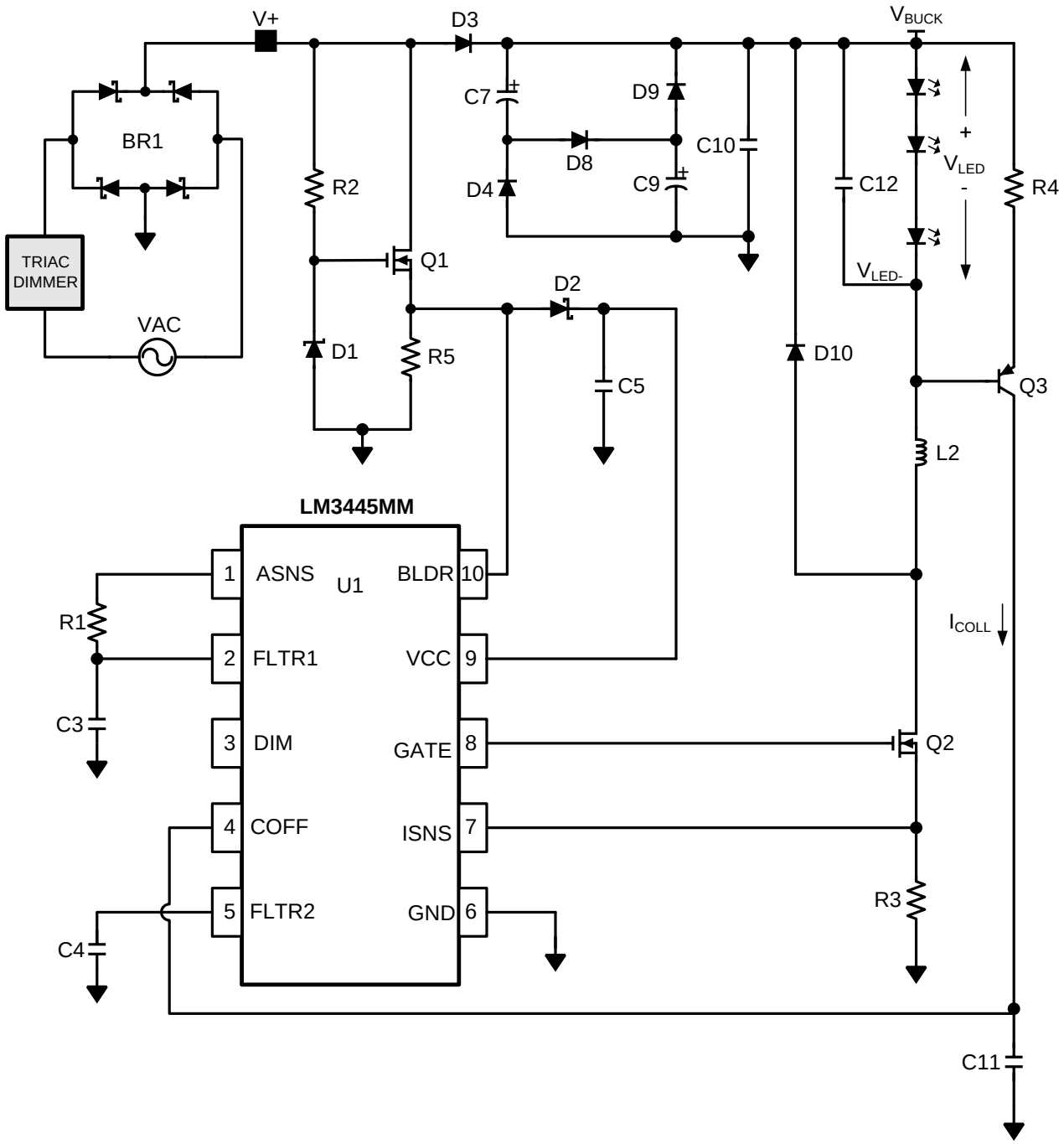


Figure 11. LM3445 Schematic

Feature Description (continued)

7.3.3 Sensing the Rectified TRIAC Waveform

A bridge rectifier, BR1, converts the line (mains) voltage (Figure 12c) into a series of half-sines as shown in Figure 12b. Figure 12a shows a typical voltage waveform after diode D3 (valley fill circuit, or V_{BUCK}).

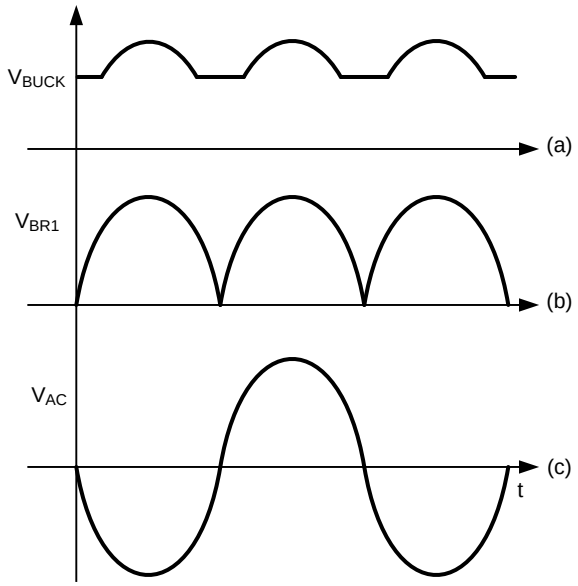


Figure 12. Voltage Waveforms After Bridge Rectifier Without TRIAC Dimming

Figure 13c and Figure 13b show typical TRIAC dimmed voltage waveforms before and after the bridge rectifier. Figure 13a shows a typical TRIAC dimmed voltage waveform after diode D3 (valley fill circuit, or V_{BUCK}).

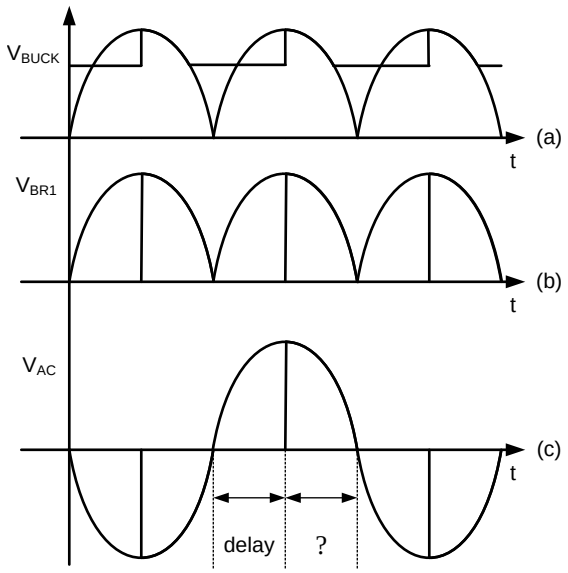


Figure 13. Voltage Waveforms After Bridge Rectifier With TRIAC Dimming

Feature Description (continued)

7.3.4 LM3445 Line Sensing Circuitry

An external series pass regulator (R2, D1, and Q1) translates the rectified line voltage to a level where it can be sensed by the BLDR pin on the LM3445.

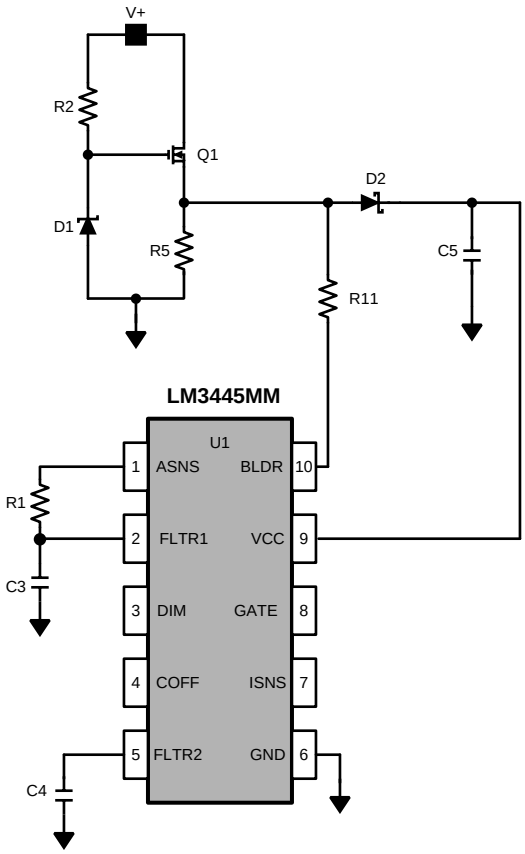


Figure 14. LM3445 AC Line Sense Circuitry

D1 is typically a 15-V Zener diode which forces transistor Q1 to stand-off most of the rectified line voltage. Having no capacitance on the source of Q1 allows the voltage on the BLDR pin to rise and fall with the rectified line voltage as the line voltage drops below zener voltage D1 (see Angle Detect).

A diode-capacitor network (D2, C5) is used to maintain the voltage on the VCC pin while the voltage on the BLDR pin goes low. This provides the supply voltage to operate the LM3445.

Resistor R5 is used to bleed charge out of any stray capacitance on the BLDR node and may be used to provide the necessary holding current for the dimmer when operating at light output currents.

7.3.5 TRIAC Holding Current Resistor

In order to emulate an incandescent light bulb (essentially a resistor) with any LED driver, the existing TRIAC will require a small amount of holding current throughout the AC line cycle. An external resistor (R5) needs to be placed on the source of Q1 to GND to perform this function. Most existing TRIAC dimmers only require a few milliamps of current to hold them on. A few less expensive TRIACs sold on the market will require a bit more current. The value of resistor R5 will depend on:

- What type of TRIAC the LM3445 will be used with
- How many light fixtures are running off of the TRIAC

Feature Description (continued)

With a single LM3445 circuit on a common TRIAC dimmer, a holding current resistor between 3 kΩ and 5 kΩ will be required. As the number of LM3445 circuits is added to a single dimmer, the holding resistor R5's resistance can be increased. A few TRIAC dimmers will require a resistor as low as 1 kΩ or lower for a single LM3445 circuit. The trade-off will be performance vs efficiency. As the holding resistor R5 is increased, the overall efficiency per LM3445 will also increase.

7.3.6 Angle Detect

The Angle Detect circuit uses a comparator with a fixed threshold voltage of 7.21 V to monitor the BLDR pin to determine whether the TRIAC is on or off. The output of the comparator drives the ASNS buffer and also controls the Bleeder circuit. A 4 µs delay line on the output is used to filter out noise that could be present on this signal.

The output of the Angle Detect circuit is limited to a 0 V to 4 V swing by the buffer and presented to the ASNS pin. R1 and C3 comprise a low-pass filter with a bandwidth on the order of 1 Hz.

The Angle Detect circuit and its filter produce a DC level which corresponds to the duty cycle (relative on-time) of the TRIAC dimmer. As a result, the LM3445 will work equally well with 50-Hz or 60-Hz line voltages.

7.3.7 Bleeder

While the BLDR pin is below the 7.21-V threshold, the bleeder MOSFET is on to place a small load (230 Ω) on the series pass regulator. This additional load is necessary to complete the circuit through the TRIAC dimmer so that the dimmer delay circuit can operate correctly. Above 7.21 V, the bleeder resistor is removed to increase efficiency.

7.3.8 FLTR1 Pin

The FLTR1 pin has two functions. Normally, it is fed by ASNS through filter components R1 and C3 and drives the dim decoder. However, if the FLTR1 pin is tied above 4.9 V (typical), for example, to VCC, the Ramp Comparator is tri-stated, disabling the dim decoder. See *Master/Slave Operation*

7.3.9 Dim Decoder

The ramp generator produces a 5.85-kHz saw tooth wave with a minimum of 1 V and a maximum of 3 V. The filtered ASNS signal enters pin FLTR1 where it is compared against the output of the Ramp Generator.

The output of the ramp comparator will have an on-time which is inversely proportional to the average voltage level at pin FLTR1. However, since the FLTR1 signal can vary between 0 V and 4 V (the limits of the ASNS pin), and the Ramp Generator signal only varies between 1 V and 3 V, the output of the ramp comparator will be on continuously for V_{FLTR1} < 1 V and off continuously for V_{FLTR1} > 3 V. This allows a decoding range from 45° to 135° to provide a 0 to 100% dimming range.

The output of the ramp comparator drives both a common-source N-channel MOSFET through a Schmitt trigger and the DIM pin (see *Master/Slave Operation* for further functions of the DIM pin). The MOSFET drain is pulled up to 750 mV by a 50-kΩ resistor.

Since the MOSFET inverts the output of the ramp comparator, the drain voltage of the MOSFET is proportional to the duty cycle of the line voltage that comes through the TRIAC dimmer. The amplitude of the ramp generator causes this proportionality to "hard limit" for duty cycles above 75% and below 25%.

The MOSFET drain signal next passes through an RC filter comprised of an internal 370-kΩ resistor, and an external capacitor on pin FLTR2. This forms a second low pass filter to further reduce the ripple in this signal, which is used as a reference by the PWM comparator. This RC filter is generally set to 10 Hz.

The net effect is that the output of the dim decoder is a DC voltage whose amplitude varies from near 0 V to 750 mV as the duty cycle of the dimmer varies from 25% to 75%. This corresponds to conduction angles of 45° to 135°, respectively.

The output voltage of the Dim Decoder directly controls the peak current that will be delivered by Q2 during its on-time. See *Buck Converter* for details.

As the TRIAC fires beyond 135°, the DIM decoder no longer controls the dimming. At this point the LEDs will dim gradually for one of two reasons:

1. The voltage at V_{BUCK} decreases and the buck converter runs out of headroom and causes LED current to

Feature Description (continued)

decrease as V_{BUCK} decreases.

2. Minimum on-time is reached which fixes the duty-cycle and therefore reduces the voltage at V_{BUCK}.

The transition from dimming with the DIM decoder to headroom or minimum on-time dimming is seamless. LED currents from full load to as low as 0.5 mA can be easily achieved.

7.3.10 Valley-Fill Circuit

V_{BUCK} supplies the power which drives the LED string. Diode D3 allows V_{BUCK} to remain high while V+ cycles on and off. V_{BUCK} has a relatively small hold capacitor C10 which reduces the voltage ripple when the valley fill capacitors are being charged. However, the network of diodes and capacitors shown between D3 and C10 make up a valley-fill circuit. The valley-fill circuit can be configured with two or three stages. The most common configuration is two stages. Figure 15 illustrates a two and three stage valley-fill circuit.

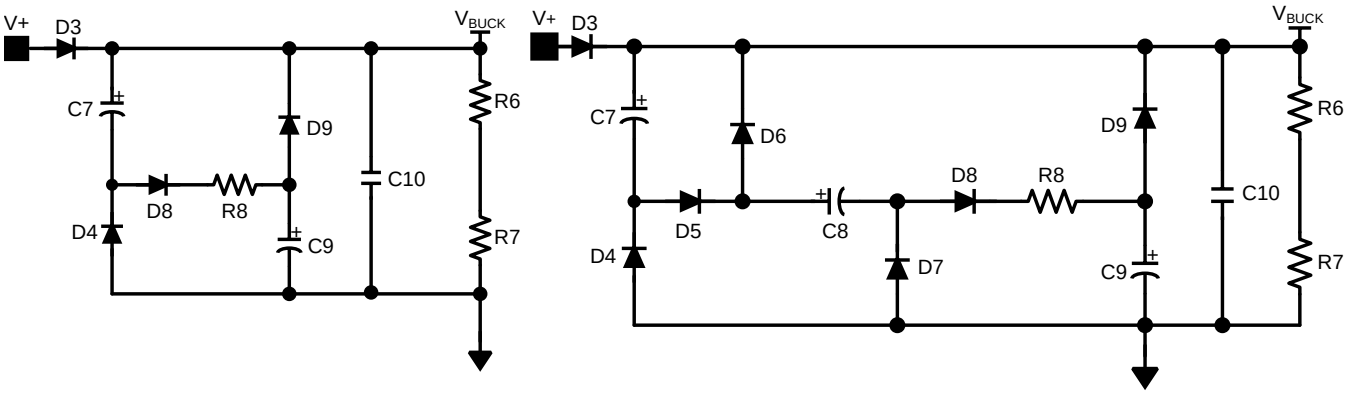


Figure 15. Two and Three Stage Valley Fill Circuit

The valley-fill circuit allows the buck regulator to draw power throughout a larger portion of the AC line. This allows the capacitance needed at V_{BUCK} to be lower than if there were no valley-fill circuit, and adds passive power factor correction (PFC) to the application. Besides better power factor correction, a valley-fill circuit allows the buck converter to operate while separate circuitry translates the dimming information. This allows for dimming that isn't subject to 120Hz flicker that can be perceived by the human eye.

7.3.11 Valley-Fill Operation

When the **input line is high**, power is derived directly through D3. The term **input line is high** can be explained as follows. The valley-fill circuit charges capacitors C7 and C9 in series (see Figure 16) when the input line is high.

Feature Description (continued)

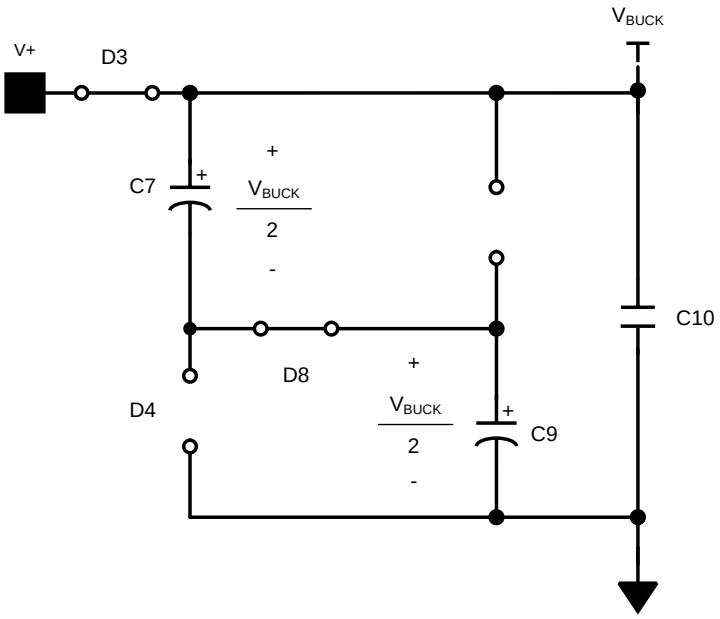


Figure 16. Two Stage Valley-Fill Circuit When AC Line is High

The peak voltage of a two stage valley-fill capacitor is:

$$V_{VF\text{-}CAP} = \frac{V_{AC\text{-}RMS}\sqrt{2}}{2} \tag{1}$$

As the AC line decreases from its peak value every cycle, there will be a point where the voltage magnitude of the AC line is equal to the voltage that each capacitor is charged. At this point diode D3 becomes reversed biased, and the capacitors are placed in parallel to each other (Figure 17), and V_{BUCK} equals the capacitor voltage.

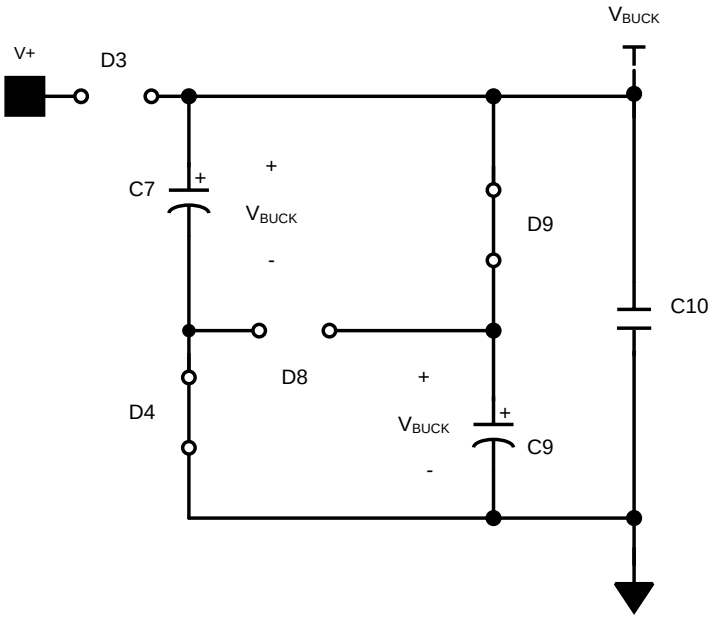


Figure 17. Two Stage Valley-Fill Circuit When AC Line is Low

Feature Description (continued)

A three stage valley-fill circuit performs exactly the same as two-stage valley-fill circuit except now three capacitors are now charged in series, and when the line voltage decreases to:

$$V_{VF\text{-}CAP} = \frac{V_{AC\text{-}RMS}\sqrt{2}}{3} \tag{2}$$

Diode D3 is reversed biased and three capacitors are in parallel to each other.

The valley-fill circuit can be optimized for power factor, voltage hold up and overall application size and cost. The LM3445 will operate with a single stage or a three stage valley-fill circuit as well. Resistor R8 functions as a current limiting resistor during start-up, and during the transition from series to parallel connection. Resistors R6 and R7 are 1-MΩ bleeder resistors, and may or may not be necessary for each application.

7.3.12 Buck Converter

The LM3445 is a buck controller that uses a proprietary constant off-time method to maintain constant current through a string of LEDs. While transistor Q2 is on, current ramps up through the inductor and LED string. A resistor R3 senses this current and this voltage is compared to the reference voltage at FLTR2. When this sensed voltage is equal to the reference voltage, transistor Q2 is turned off and diode D10 conducts the current through the inductor and LEDs. Capacitor C12 eliminates most of the ripple current seen in the inductor. Resistor R4, capacitor C11, and transistor Q3 provide a linear current ramp that sets the constant off-time for a given output voltage.

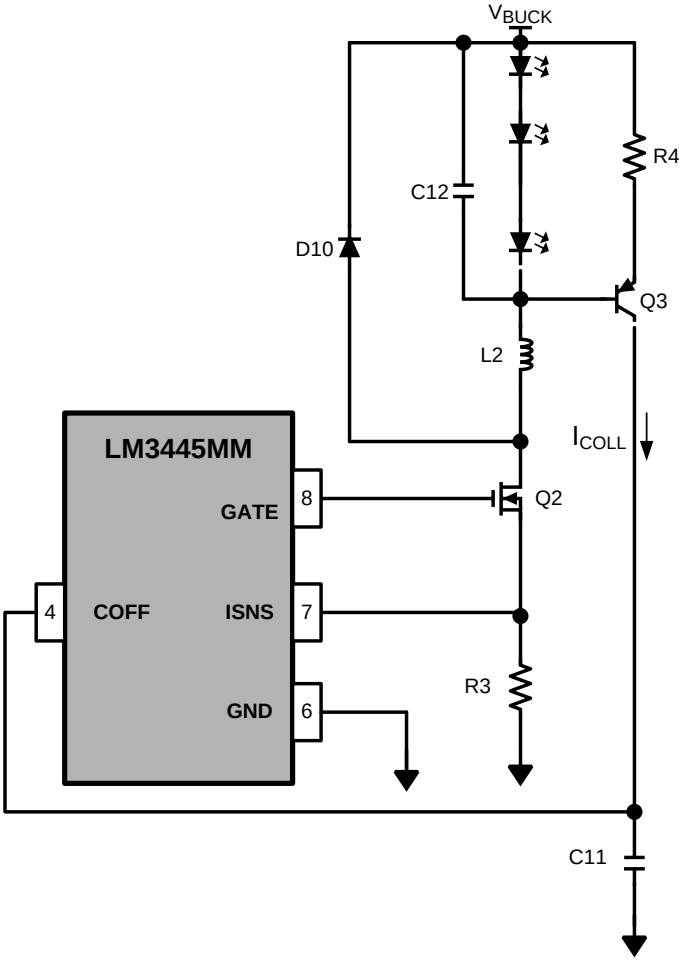


Figure 18. LM3445 Buck Regulation Circuit

Feature Description (continued)

7.3.13 Overview of Constant Off-Time Control

A buck converter's conversion ratio is defined using Equation 3.

$$\frac{V_O}{V_{IN}} = D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times f_{SW} \tag{3}$$

Constant off-time control architecture operates by simply defining the off-time and allowing the on-time, and therefore the switching frequency, to vary as either V_{IN} or V_O changes. The output voltage is equal to the LED string voltage (V_{LED}), and should not change significantly for a given application. The input voltage or V_{BUCK} in this analysis will vary as the input line varies. The length of the on-time is determined by the sensed inductor current through a resistor to a voltage reference at a comparator. During the on-time, denoted by t_{ON}, MOSFET switch Q2 is on causing the inductor current to increase. During the on-time, current flows from V_{BUCK}, through the LEDs, through L2, Q2, and finally through R3 to ground. At some point in time, the inductor current reaches a maximum ($I_{L2\text{-}PK}$) determined by the voltage sensed at R3 and the ISNS pin. This sensed voltage across R3 is compared against the voltage of dim decoder output, FLTR2, at which point Q2 is turned off by the controller.

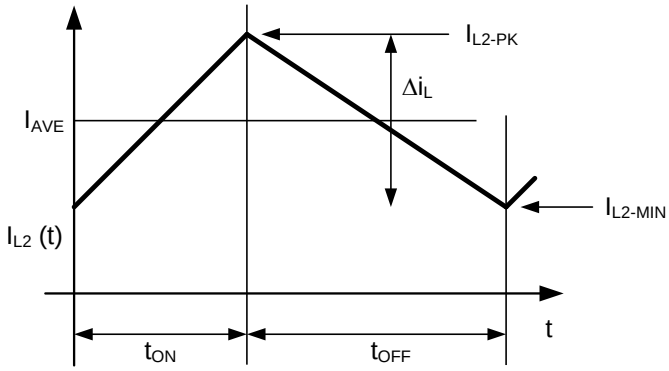


Figure 19. Inductor Current Waveform in CCM

During the off-period denoted by t_{OFF}, the current through L2 continues to flow through the LEDs via D10.

7.3.14 Master/Slave Operation

Multiple LM3445s can be configured so that large strings of LEDs can be controlled by a single TRIAC dimmer. By doing so, smooth consistent dimming for multiple LED circuits is achieved.

When the FLTR1 pin is tied above 4.9 V (typical), preferably to VCC, the ramp comparator is tri-stated, disabling the dim decoder. This allows one or more LM3445 devices or PWM LED driver devices (slaves) to be controlled by a single LM3445 (master) by connecting their DIM pins together.

7.3.15 Master/Slave Configuration

TI offers an LM3445 demonstration PCB for customer evaluation through our website. The following description and theory uses reference designators that follow our evaluation PCB. The LM3445 Master/Slave schematics are illustrated below (Figure 20 through Figure 22) for clarity. Each board contains a separate circuit for the Master and Slave function. Both the Master and Slave boards will need to be modified from their original stand alone function so that they can be coupled together. Only the Master LM3445 requires use of the Master/Slave circuit for any number of slaves.

7.3.16 Master Board Modifications

- Remove R10 and replace with a BAS40 diode
- Connect TP18 to TP14 (V_{CC})
- Connect TP17 (gate of Q5) to TP15 (gate of Q2)

7.3.17 Slave Board Modifications

- Remove R11 (disconnects BLDR)

Feature Description (continued)

- Tie TP14 (FLTR1) to V_{CC}

7.3.18 Master/Slave Interconnection

- Connect TP19 of Master to TP10 of Slave (Master VCC Control)
- Connect TP6 (DIM pin) of Master to TP6 (DIM pin) of Slave (Master DIM Control)

7.3.19 Master/Slave Theory of Operation

By placing two series diodes on the Master VCC circuit one forces the master VCC UVLO to become the dominant threshold. When Master VCC drops below UVLO, GATE stops switching and the RC timer (>200 µs) rises above the TL431 threshold (2.5 V) which in turn pulls down on the gate of the Slave pass device (Q1).

The valley-fill circuit could consist of one large circuit to power all LM3445 series connected, or each LM3445 circuit could have a separate valley-fill circuit located near the buck converter.

7.3.20 Master/Slave Connection Diagram

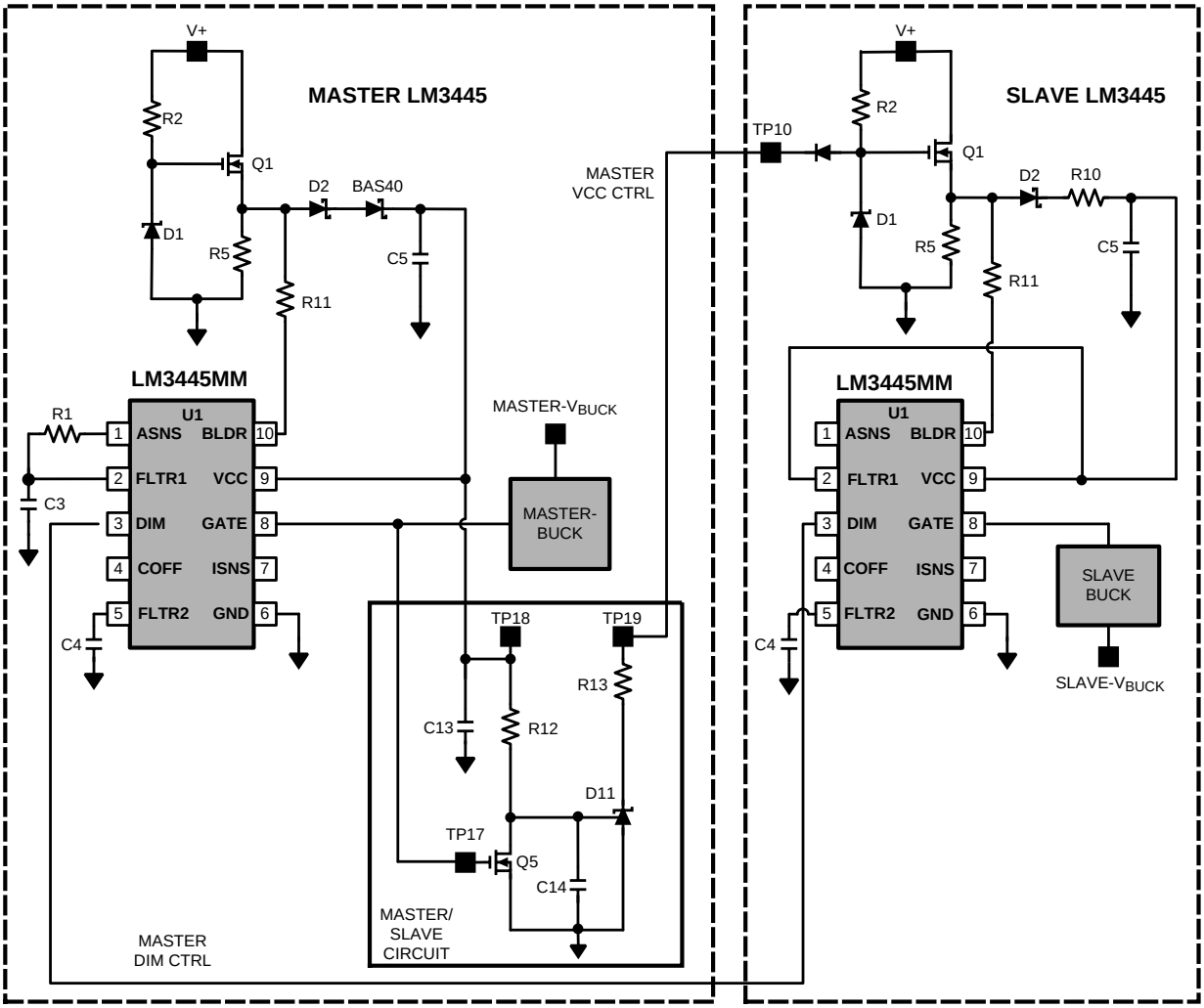


Figure 20. Master Slave Configuration

Feature Description (continued)

7.3.21 Master/Slave Block Diagrams

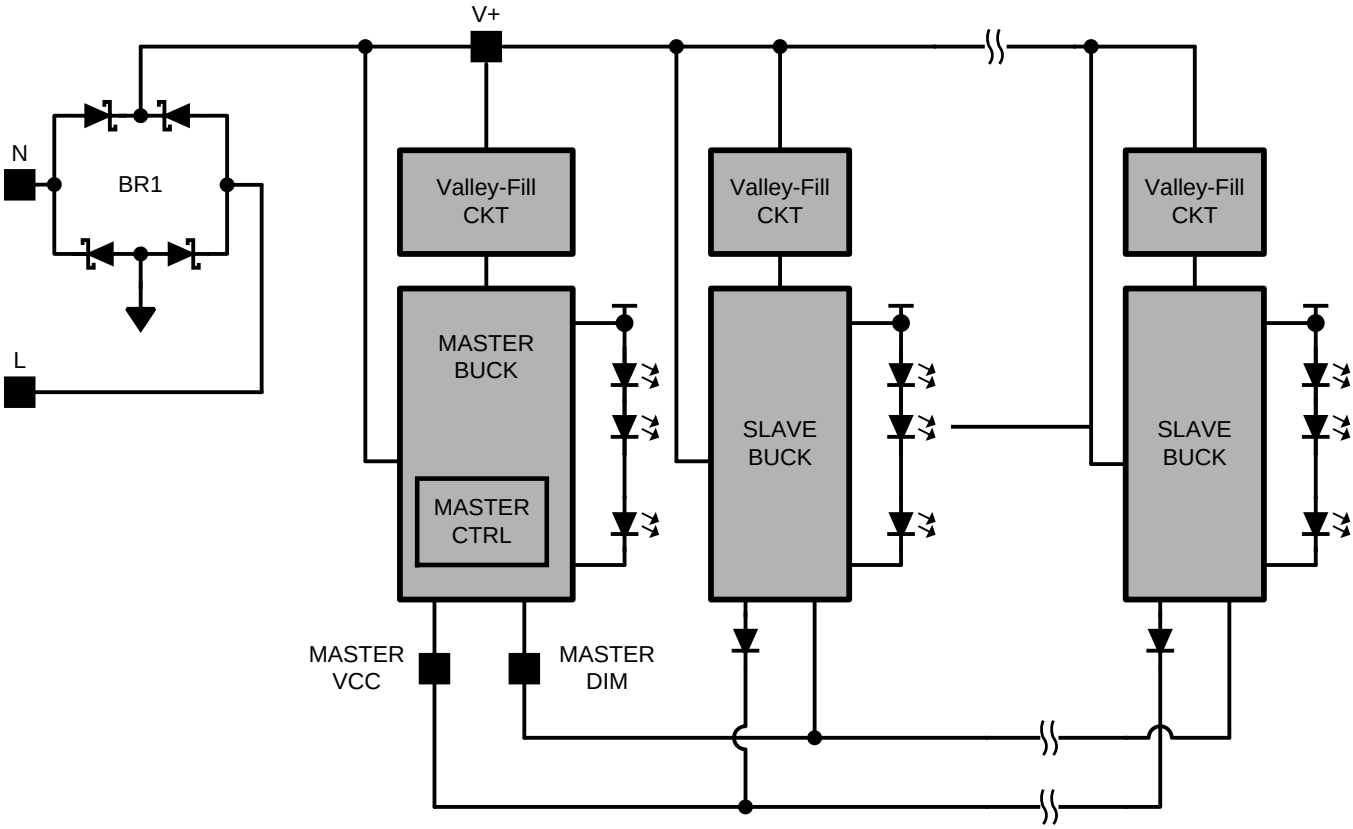


Figure 21. Master/Slave Configuration With Separate Valley-Fill Circuits

Feature Description (continued)

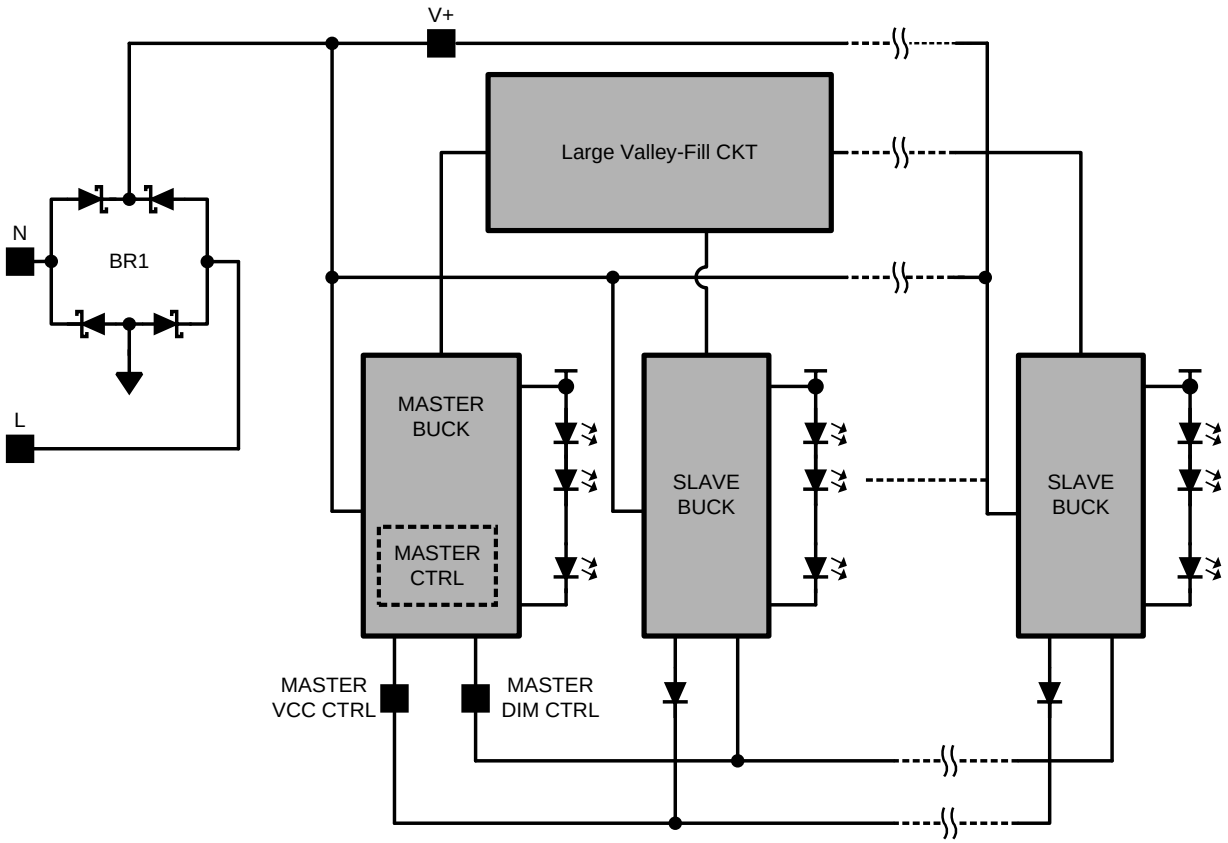


Figure 22. Master/Slave Configuration With One Valley-Fill Circuit

7.3.22 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 165°C. After thermal shutdown occurs, the output switch doesn't turn on until the junction temperature drops to approximately 145°C.

7.4 Device Functional Modes

This device does not have any additional functional modes.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Determining Duty-Cycle (D)

As shown in Equation 4, duty cycle (D) approximately equals:

$$\frac{V_{LED}}{V_{BUCK}} = D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times f_{SW} \tag{4}$$

With efficiency considered:

$$\frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}} = D \tag{5}$$

For simplicity, choose efficiency between 75% and 85%.

8.1.2 Calculating Off-Time

The Off-Time of the LM3445 is set by the user and remains fairly constant as long as the voltage of the LED stack remains constant. Calculating the off-time is the first step in determining the switching frequency of the converter, which is integral in determining some external component values.

PNP transistor Q3, resistor R4, and the LED string voltage define a charging current into capacitor C11. A constant current into a capacitor creates a linear charging characteristic, as shown in Equation 6.

$$i = C \frac{dv}{dt} \tag{6}$$

Resistor R4, capacitor C11 and the current through resistor R4 (i_{COLL}), which is approximately equal to V_{LED}/R4, are all fixed. Therefore, dv is fixed and linear, and dt (t_{OFF}) can now be calculated.

$$t_{OFF} = C11 \times 1.276V \times \left(\frac{R4}{V_{LED}}\right) \tag{7}$$

Equation 8 shows common equations for determining duty cycle and switching frequency in any buck converter.

$$f_{SW} = \frac{1}{t_{OFF} + t_{ON}}$$

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_{LED}}{V_{BUCK}}$$

$$D' = \frac{t_{OFF}}{t_{ON} + t_{OFF}} \tag{8}$$

Therefore:

$$f_{SW} = \frac{D}{t_{ON}}, \text{ and } f_{SW} = \frac{1 - D}{t_{OFF}} \tag{9}$$

With efficiency of the buck converter in mind, as shown in Equation 10.

$$\frac{V_{LED}}{V_{BUCK}} = \eta \times D \tag{10}$$

Substitute equations and rearrange:

Application Information (continued)

$$f_{SW} = \frac{\left(1 - \frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}}\right)}{t_{OFF}} \tag{11}$$

Off-time, and switching frequency can now be calculated using the equations above.

8.1.3 Setting the Switching Frequency

Selecting the switching frequency for nominal operating conditions is based on tradeoffs between efficiency (better at low frequency) and solution size and cost (smaller at high frequency).

The input voltage to the buck converter (V_{BUCK}) changes with both line variations and over the course of each half-cycle of the input line voltage. The voltage across the LED string will, however, remain constant, and therefore the off-time remains constant.

The on-time, and therefore the switching frequency, will vary as the V_{BUCK} voltage changes with line voltage. A good design practice is to choose a desired nominal switching frequency knowing that the switching frequency will decrease as the line voltage drops and increase as the line voltage increases (see Figure 23).

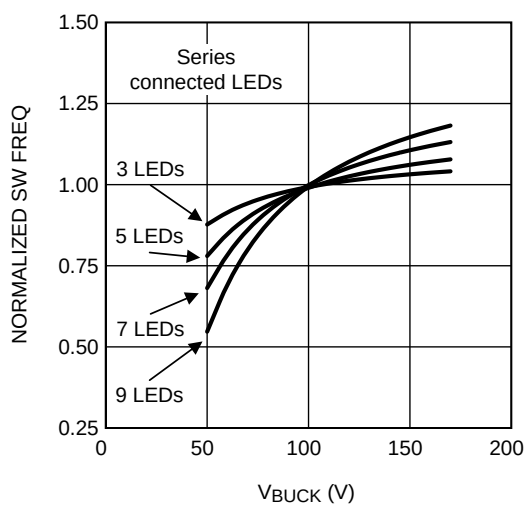


Figure 23. Graphical Illustration of Switching Frequency vs V_{BUCK}

The off-time of the LM3445 can be programmed for switching frequencies ranging from 30 kHz to over 1 MHz. A trade-off between efficiency and solution size must be considered when designing the LM3445 application.

The maximum switching frequency attainable is limited only by the minimum on-time requirement (200 ns).

Worst case scenario for minimum on time is when V_{BUCK} is at its maximum voltage (AC high line) and the LED string voltage (V_{LED}) is at its minimum value.

$$t_{ON(MIN)} = \left(\frac{1}{\eta} \times \frac{V_{LED(MIN)}}{V_{BUCK(MAX)}}\right)\frac{1}{f_{SW}} \tag{12}$$

The maximum voltage seen by the Buck Converter is:

$$V_{BUCK(MAX)} = V_{AC\text{-}RMS(MAX)} \times \sqrt{2} \tag{13}$$

Application Information (continued)

8.1.4 Inductor Selection

The controlled off-time architecture of the LM3445 regulates the average current through the inductor (L2), and therefore the LED string current. The input voltage to the buck converter (V_{BUCK}) changes with line variations and over the course of each half-cycle of the input line voltage. The voltage across the LED string is relatively constant, and therefore the current through R4 is constant. This current sets the off-time of the converter and therefore the output volt-second product (V_{LED} x off-time) remains constant. A constant volt-second product makes it possible to keep the ripple through the inductor constant as the voltage at V_{BUCK} varies.

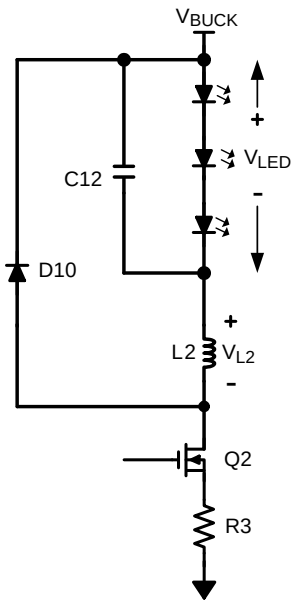


Figure 24. LM3445 External Components of the Buck Converter

The equation for an ideal inductor is shown in Equation 14.

$$\nu = L \frac{di}{dt} \tag{14}$$

Given a fixed inductor value, L, this equation states that the change in the inductor current over time is proportional to the voltage applied across the inductor.

During the on-time, the voltage applied across the inductor is,

$$V_{L(ON\text{-}TIME)} = V_{BUCK} - (V_{LED} + V_{DS(Q2)} + I_{L2} \times R3) \tag{15}$$

Since the voltage across the MOSFET switch (Q2) is relatively small, as is the voltage across sense resistor R3, we can simplify this to approximately,

$$V_{L(ON\text{-}TIME)} = V_{BUCK} - V_{LED} \tag{16}$$

During the off-time, the voltage seen by the inductor is approximately:

$$V_{L(OFF\text{-}TIME)} = V_{LED} \tag{17}$$

The value of $V_{L(OFF\text{-}TIME)}$ will be relatively constant, because the LED stack voltage will remain constant. If we rewrite the equation for an inductor inserting what we know about the circuit during the off-time, we get Equation 18.

$$V_{L(OFF\text{-}TIME)} = V_{LED} = L \times \frac{\Delta i}{\Delta t}$$

$$V_{L(OFF\text{-}TIME)} = V_{LED} = L \times \frac{(I_{(MAX)} - I_{(MIN)})}{\Delta t} \tag{18}$$

Re-arranging this gives us Equation 19.

Application Information (continued)

$$\Delta i \cong t_{OFF} \times \frac{V_{LED}}{L2} \tag{19}$$

From this we can see that the ripple current (Δi) is proportional to off-time (t_{OFF}) multiplied by a voltage which is dominated by V_{LED} divided by a constant (L2).

These equations can be rearranged to calculate the desired value for inductor L2.

$$L2 \cong t_{OFF} \times \frac{V_{LED}}{\Delta i} \tag{20}$$

Where:

$$t_{OFF} = \frac{\left(1 - \frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}}\right)}{f_{SW}} \tag{21}$$

Finally:

$$L2 = \frac{V_{LED}\left(1 - \frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}}\right)}{f_{SW} \times \Delta i} \tag{22}$$

See *Typical Application* to better understand the design process.

8.1.5 Setting the LED Current

The LM3445 constant off-time control loop regulates the peak inductor current (I_{L2}). The average inductor current equals the average LED current (I_{AVE}). Therefore the average LED current is regulated by regulating the peak inductor current.

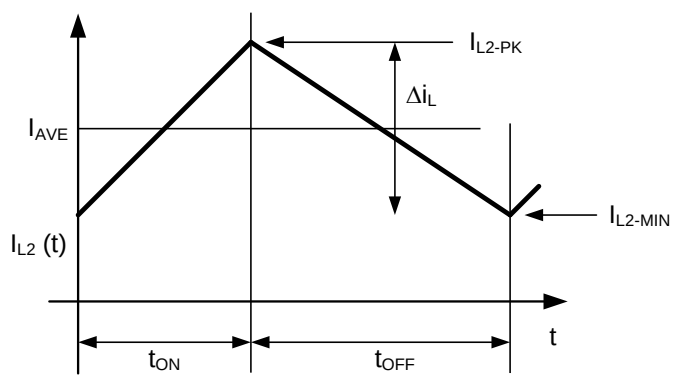


Figure 25. Inductor Current Waveform in CCM

Knowing the desired average LED current, I_{AVE} and the nominal inductor current ripple, Δi_L, the peak current for an application running in continuous conduction mode (CCM) is defined in Equation 23.

$$I_{L2\text{-}PK} = I_{AVE} + \frac{\Delta i_L}{2} \tag{23}$$

Or, the maximum, or undimmed, LED current would then be,

$$I_{AVE(UNDIM)} = I_{L2\text{-}PK(UNDIM)} - \frac{\Delta i_L}{2} \tag{24}$$

This is important to calculate because this peak current multiplied by the sense resistor R3 will determine when the internal comparator is tripped. The internal comparator turns the control MOSFET off once the peak sensed voltage reaches 750 mV, as shown in Equation 25.

$$I_{L\text{-}PK(UNDIM)} = \frac{750\ mV}{R3} \tag{25}$$

Application Information (continued)

Current Limit: Under normal circumstances, the trip voltage on the PWM comparator would be less than or equal to 750 mV, depending on the amount of dimming. However, if there is a short circuit or an excessive load on the output, higher than normal switch currents will cause a voltage above 1.27 V on the ISNS pin which will trip the I-LIM comparator. The I-LIM comparator will reset the RS latch, turning off Q2. It will also inhibit the Start Pulse Generator and the COFF comparator by holding the COFF pin low. A delay circuit will prevent the start of another cycle for 180 µs.

8.1.6 Valley Fill Capacitors

Determining voltage rating and capacitance value of the valley-fill capacitors:

Equation 26 shows the maximum voltage seen by the valley-fill capacitors is:

$$V_{VF\text{-}CAP} = \frac{V_{AC(MAX)}\sqrt{2}}{\#\text{stages}} \tag{26}$$

This is, of course, if the capacitors chosen have identical capacitance values and split the line voltage equally. Often a 20% difference in capacitance could be observed between like capacitors. Therefore a voltage rating margin of 25% to 50% should be considered.

8.1.6.1 Determining the Capacitance Value of the Valley-Fill Capacitors

The valley fill capacitors should be sized to supply energy to the buck converter (V_{BUCK}) when the input line is less than its peak divided by the number of stages used in the valley fill (t_X). The capacitance value should be calculated when the TRIAC is not firing, that is, when full LED current is being drawn by the LED string. The maximum power is delivered to the LED string at this time, and therefore the most capacitance is required.

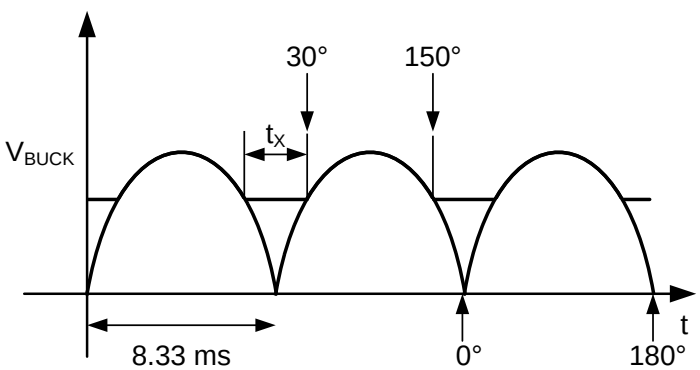


Figure 26. Two Stage Valley-Fill V_{BUCK} Voltage With No TRIAC Dimming

From the above illustration and the equation for current in a capacitor, i = C × dV/dt, the amount of capacitance needed at V_{BUCK} is calculated as follows:

At 60Hz, and a valley-fill circuit of two stages, the hold up time (t_X) required at V_{BUCK} is calculated as follows. The total angle of an AC half cycle is 180° and the total time of a half AC line cycle is 8.33 ms. When the angle of the AC waveform is at 30° and 150°, the voltage of the AC line is exactly ½ of its peak. With a two stage valley-fill circuit, this is the point where the LED string switches from power being derived from AC line to power being derived from the hold up capacitors (C7 and C9). 60° out of 180° of the cycle or 1/3 of the cycle the power is derived from the hold up capacitors (1/3 × 8.33 ms = 2.78 ms). This is equal to the hold up time (dt) from the above equation, and dv is the amount of voltage the circuit is allowed to droop. From the next section ("Determining Maximum Number of Series Connected LEDs Allowed") we know the minimum V_{BUCK} voltage will be about 45 V for a 90 V_{AC} to 135 V_{AC} line. At 90 V_{AC} low line operating condition input, ½ of the peak voltage is 64 V. Therefore, with some margin the voltage at V_{BUCK} can not droop more than about 15 V (dv). (i) is equal to (P_{OUT}/V_{BUCK}), where P_{OUT} is equal to (V_{LED} × I_{LED}). Total capacitance (C7 in parallel with C9) can now be calculated. See *Typical Application* for further calculations of the valley-fill capacitors.

Application Information (continued)

8.1.6.2 Determining Maximum Number of Series Connected LEDs Allowed

The LM3445 is an off-line buck topology LED driver. A buck converter topology requires that the input voltage (V_{BUCK}) of the output circuit must be greater than the voltage of the LED stack (V_{LED}) for proper regulation. One must determine what the minimum voltage observed by the buck converter will be before the maximum number of LEDs allowed can be determined. Two variables will have to be determined in order to accomplish this.

1. AC line operating voltage. This is usually 90 V_{AC} to 135 V_{AC} for North America. Although the LM3445 can operate at much lower and higher input voltages a range is needed to illustrate the design process.
2. How many stages are implemented in the valley-fill circuit (1, 2 or 3).

In this example the most common valley-fill circuit will be used (two stages).

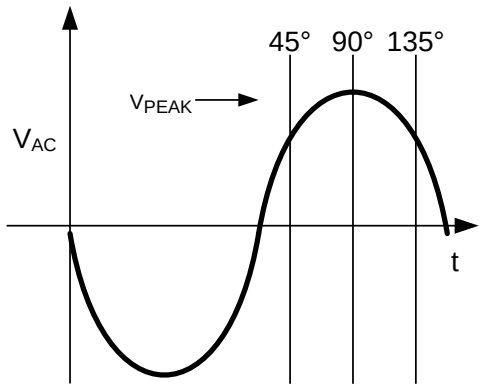


Figure 27. AC Line with Firing Angles

Figure 28 shows three TRIAC dimmed waveforms. One can easily see that the peak voltage (V_{PEAK}) from 0° to 90° will always be:

$$V_{AC\text{-}RMS\text{-}PK}\sqrt{2} \tag{27}$$

Once the TRIAC is firing at an angle greater than 90° the peak voltage will lower and equal to Equation 28.

$$V_{AC\text{-}RMS\text{-}PK}\sqrt{2} \text{ x } SIN(\theta) \tag{28}$$

The voltage at V_{BUCK} with a valley fill stage of two will look similar to the waveforms of Figure 29.

The purpose of the valley fill circuit is to allow the buck converter to pull power directly off of the AC line when the line voltage is greater than its peak voltage divided by two (two stage valley fill circuit). During this time, the capacitors within the valley fill circuit (C7 and C8) are charged up to the peak of the AC line voltage. Once the line drops below its peak divided by two, the two capacitors are placed in parallel and deliver power to the buck converter. One can now see that if the peak of the AC line voltage is lowered due to variations in the line voltage, or if the TRIAC is firing at an angle above 90°, the DC offset (V_{DC}) will lower. V_{DC} is the lowest value that voltage V_{BUCK} will encounter.

$$V_{BUCK(MIN)} = \frac{V_{AC\text{-}RMS(MIN)}\sqrt{2} \text{ x } SIN(\theta)}{\#stages} \tag{29}$$

Example:

Line voltage = 90 V_{AC} to 135 V_{AC}

Valley-Fill = two stage

$$V_{BUCK(MIN)} = \frac{90\sqrt{2} \text{ x } SIN(135^{o})}{2} = 45V \tag{30}$$

Application Information (continued)

Depending on what type and value of capacitors are used, some derating should be used for voltage droop when the capacitors are delivering power to the buck converter. When the TRIAC is firing at 135° the current through the LED string will be small. Therefore the droop should be small at this point and a 5% voltage droop should be a sufficient derating. With this derating, the lowest voltage the buck converter will see is about 42.5 V in this example.

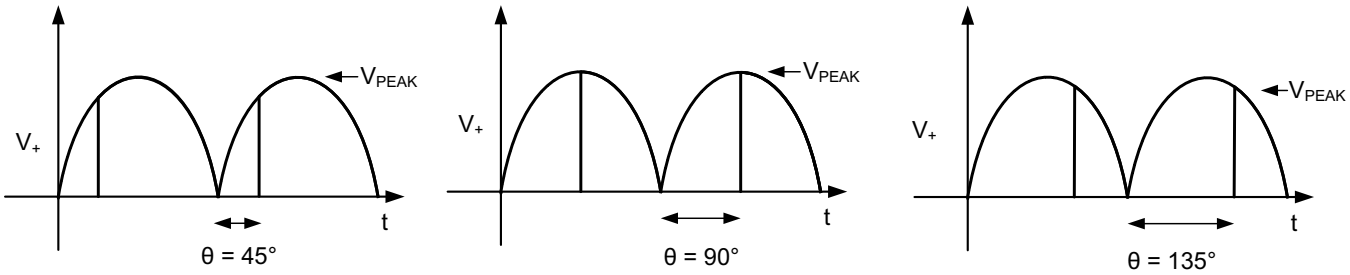


Figure 28. AC Line With Various Firing Angles

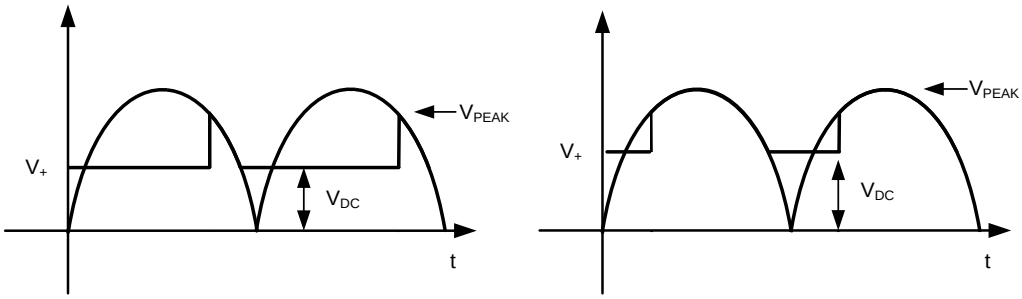


Figure 29. V_{BUCK} Waveforms With Various Firing Angles

To determine how many LEDs can be driven, take the minimum voltage the buck converter will see (42.5 V) and divide it by the worst case forward voltage drop of a single LED.

Example: 42.5 V / 3.7 V = 11.5 LEDs (11 LEDs with margin)

8.1.7 Output Capacitor

A capacitor placed in parallel with the LED or array of LEDs can be used to reduce the LED current ripple while keeping the same average current through both the inductor and the LED array. With a buck topology the output inductance (L2) can now be lowered, making the magnetics smaller and less expensive. With a well designed converter, you can assume that all of the ripple will be seen by the capacitor, and not the LEDs. One must ensure that the capacitor you choose can handle the RMS current of the inductor. See manufacture's data sheets to ensure compliance. Usually an X5R or X7R capacitor between 1 µF and 10 µF of the proper voltage rating will be sufficient.

8.1.8 Switching MOSFET

The main switching MOSFET should be chosen with efficiency and robustness in mind. The maximum voltage across the switching MOSFET will equal:

$$V_{DS(MAX)} = V_{AC\text{-}RMS(MAX)}\sqrt{2} \tag{31}$$

The average current rating should be greater than:

$$I_{DS\text{-}MAX} = I_{LED(\text{-}AVE)}(D_{MAX}) \tag{32}$$

Application Information (continued)

8.1.9 Re-Circulating Diode

The LM3445 Buck converter requires a re-circulating diode D10 (see the *Typical Application* circuit to carry the inductor current during the MOSFET Q2 off-time. The most efficient choice for D10 is a diode with a low forward drop and near-zero reverse recovery time that can withstand a reverse voltage of the maximum voltage seen at V_{BUCK}. For a common 110 V_{AC} ± 20% line, the reverse voltage could be as high as 190 V.

$$V_D \geq V_{AC\text{-}RMS(MAX)}\sqrt{2} \tag{33}$$

The current rating must be at least:

$$I_D = (1 - DMIN) \times Iledave \tag{34}$$

Or:

$$I_D = \left(1 - \frac{V_{LED(MIN)}}{V_{BUCK(MAX)}}\right) \times I_{LED(AVE)} \tag{35}$$

8.2 Typical Application

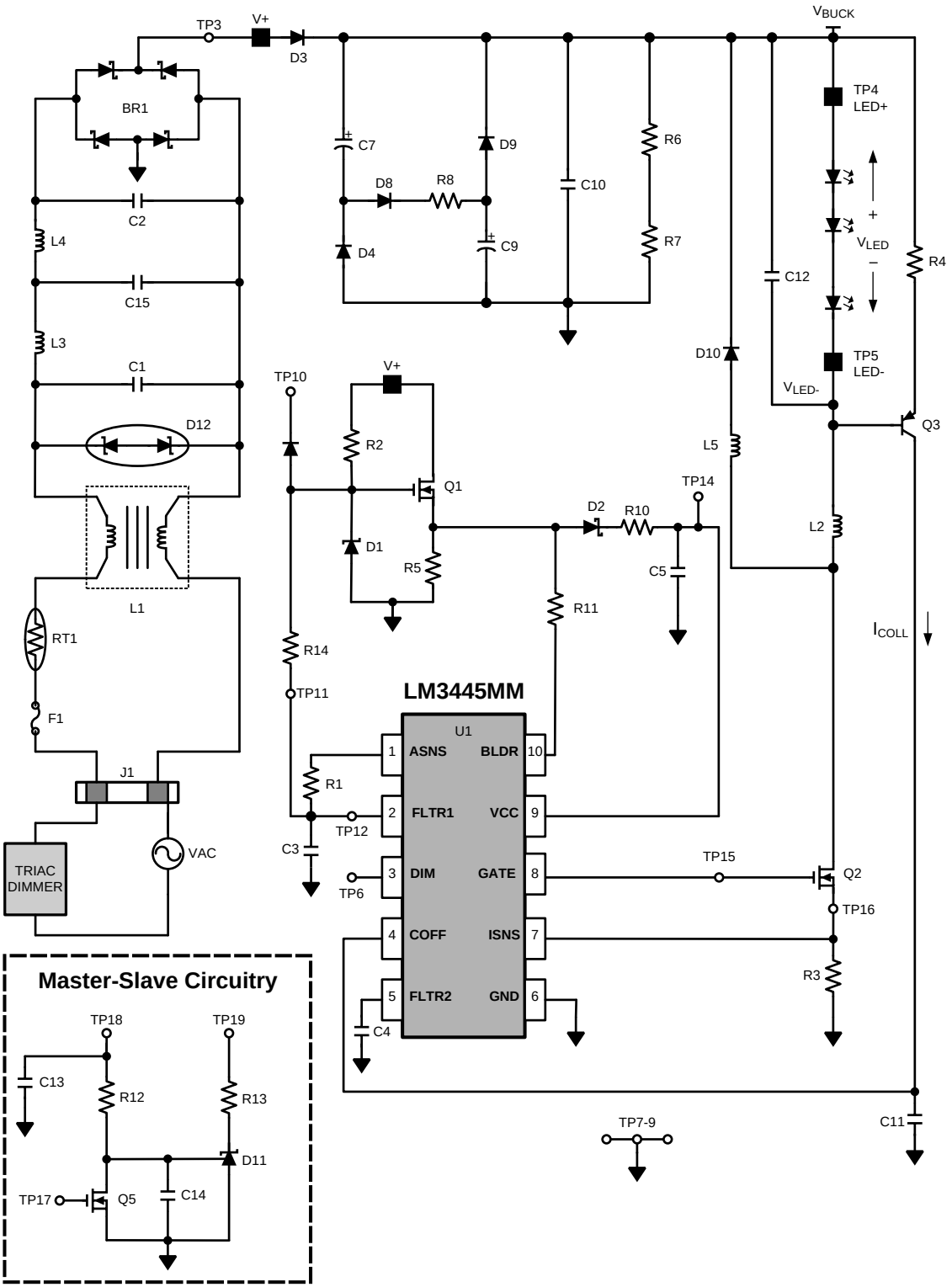


Figure 30. LM3445 Design Example 1 Input = 90 V_{AC} to 135 V_{AC}, V_{LED} = 7 × HB LED String Application at 400 MA

Typical Application (continued)

8.2.1 Design Requirements

Known:

1. Input voltage range (90 V_{AC} – 135 V_{AC})
2. Number of LEDs in series = 7
3. Forward voltage drop of a single LED = 3.6 V
4. LED stack voltage = (7 × 3.6V) = 25.2 V

Choose:

1. Nominal switching frequency, $f_{SW\text{-}TARGET}$ = 350 kHz
2. $I_{LED(AVE)}$ = 400 mA
3. Δi (usually 15% - 30% of $_{ILED(AVE)}$) = (0.30 × 400 mA) = 120 mA
4. Valley fill stages (1, 2, or 3) = 2
5. Assumed minimum efficiency = 80%

8.2.2 Detailed Design Procedure

The following design example illustrates the process of calculating external component values.

Calculate:

1. Calculate minimum voltage V_{BUCK} equals:

$$V_{BUCK(MIN)} = \frac{90\sqrt{2}\ \text{x SIN}(135^{o})}{2} = 45\text{V} \tag{36}$$

2. Calculate maximum voltage V_{BUCK} equals:

$$V_{BUCK(MAX)} = 135\sqrt{2} = 190\text{V} \tag{37}$$

3. Calculate t_{OFF} at V_{BUCK} nominal line voltage:

$$t_{OFF} = \frac{\left(1 - \frac{1}{0.8} \times \frac{25.2\text{V}}{115\sqrt{2}}\right)}{(250\ \text{kHz})} = 3.23\ \mu\text{s} \tag{38}$$

4. Calculate $t_{ON(MIN)}$ at high line to ensure that $t_{ON(MIN)}$ > 200 ns:

$$t_{ON\ (MIN)} = \frac{\left(\frac{1}{0.8} \times \frac{25.2\text{V}}{135\sqrt{2}}\right)}{\left(1 - \frac{1}{0.8} \times \frac{25.2\text{V}}{135\sqrt{2}}\right)} \times 3.23\ \mu\text{s} = 638\ \text{ns} \tag{39}$$

5. Calculate C11 and R4:
6. Choose current through R4: (between 50 µA and 100 µA) 70 µA

$$R4 = \frac{V_{LED}}{I_{COLL}} = 360\ \text{k}\Omega \tag{40}$$

7. Use a standard value of 365 kΩ
8. Calculate C11:

$$C11 = \left(\frac{V_{LED}}{R4}\right)\left(\frac{t_{OFF}}{1.276}\right) = 175\ \text{pF} \tag{41}$$

9. Use standard value of 120 pF
10. Calculate ripple current: 400 mA × 0.30 = 120 mA
11. Calculate inductor value at t_{OFF} = 3 µs:

$$L2 = \frac{25.2\text{V}\left(1 - \frac{1}{0.8} \times \frac{25.2\text{V}}{115\sqrt{2}}\right)}{(350\ \text{kHz x } 0.1\text{A})} = 580\ \mu\text{H} \tag{42}$$

12. Choose C10: 1 µF 200 V

Typical Application (continued)

13. Calculate valley-fill capacitor values: V_{AC} low line = 90 V_{AC}, V_{BUCK} minimum equals 60 V (no TRIAC dimming at maximum LED current). Set droop for 20 V maximum at full load and low line.

$$i = C \frac{dv}{dt}$$

where

- i equals P_{OUT} / V_{BUCK} (270 mA).
- dV equals 20 V.
- dt equals 2.77 ms.
- C_{TOTAL} equals 37 µF.

Therefore C7 = C9 = 22 µF. (43)

Table 1. Bill of Materials

QTY	REF DES	DESCRIPTION	MANUFACTURER	MANUFACTURER PN
1	U1	IC, CTRLR, DRVR-LED, VSSOP10	TI	LM3445MM
1	BR1	Bridge Rectifiier, SMT, 400 V, 800 mA	DiodesInc	HD04-T
1	L1	Common mode filter DIP4NS, 900 mA, 700 µH	Panasonic	ELF-11090E
1	L2	Inductor, SHLD, SMT, 1 A, 470 µH	Coilcraft	MSS1260-474-KLB
2	L3, L4	Diff mode inductor, 500 mA 1 mH	Coilcraft	MSS1260-105KL-KLB
1	L5	Bead Inductor, 160 Ω, 6A	Steward	HI1206T161R-10
3	C1, C2, C15	Cap, Film, X2Y2, 12.5 MM, 250 V_{AC}, 20%, 10 nF	Panasonic	ECQ-U2A103ML
1	C3	Cap, X7R, 0603, 16 V, 10%, 470 nF	MuRata	GRM188R71C474KA88D
1	C4	Cap, X7R, 0603, 16 V, 10%, 100 nF	MuRata	GRM188R71C104KA01D
2	C5, C6	Cap, X5R, 1210, 25 V, 10%, 22 µF	MuRata	GRM32ER61E226KE15L
2	C7, C9	Cap, AL, 200 V, 105C, 20%, 33 µF	UCC	EKXG201ELL330MK20S
1	C10	Cap, Film, 250 V, 5%, 10 nF	Epcos	B32521C3103J
1	C12	Cap, X7R, 1206, 50 V, 10%, 1.0 uF	Kemet	C1206F105K5RACTU
1	C11	Cap, C0G, 0603, 100 V, 5%, 120 pF	MuRata	GRM1885C2A121JA01D
1	C13	Cap, X7R, 0603, 50 V, 10%, 1.0 nF	Kemet	C0603C102K5RACTU
1	C14	Cap, X7R, 0603, 50 V, 10%, 22 nF	Kemet	C0603C223K5RACTU
1	D1	Diode, ZNR, SOT23, 15 V, 5%	OnSemi	BZX84C15LT1G
2	D2, D13	Diode, SCH, SOD123, 40 V, 120 mA	NXP	BAS40H
4	D3, D4, D8, D9	Diode, FR, SOD123, 200 V, 1A	Rohm	RF071M2S
1	D10	Diode, FR, SMB, 400 V, 1A	OnSemi	MURS140T3G
1	D11	IC, SHNT, ADJ, SOT23, 2.5 V, 0.5%	TI	TL431BIDBZR
1	D12	TVS, VBR = 209 V	LittleFuse	P6SMB220CA
1	R1	Resistor, 0603, 1%, 280 kΩ	Panasonic	ERJ-3EKF2803V
1	R2	Resistor, 1206, 1%, 100 kΩ	Panasonic	ERJ-8ENF1003V
1	R3	Resistor, 1210, 5%, 1.8 Ω	Panasonic	ERJ-14RQJ1R8U
1	R4	Resistor, 0603, 1%, 576 kΩ	Panasonic	ERJ-3EKF5763V
1	R5	Resistor, 1206, 1%, 1.00 kΩ	Panasonic	ERJ-8ENF1001V
2	R6, R7	Resistor, 0805, 1%, 1.00 MΩ	Rohm	MCR10EZHF1004
2	R8, R10	Resistor, 1206, 0.0 Ω	Yageo	RC1206JR-070RL
1	R9	Resistor, 1812, 0.0 Ω		
1	R11	Resistor, 0603, 0.0 Ω	Yageo	RC0603JR-070RL
1	R12	Resistor, 0603, 1%, 33.2 kΩ	Panasonic	ERJ-3EKF3322V
1	R13	Resistor, 0603, 1%, 2.0 kΩ	Panasonic	ERJ-3EKF2001V
1	R14	Resistor, 0805, 1%, 3.3 MΩ	Rohm	MCR10EZHF3304
1	RT1	Thermistor, 120 V, 1.1A, 50 Ω at 25°C	Thermometrics	CL-140

Typical Application (continued)

Table 1. Bill of Materials (continued)

QTY	REF DES	DESCRIPTION	MANUFACTURER	MANUFACTURER PN
2	Q1, Q2	XSTR, NFET, DPAK, 300 V, 4 A	Fairchild	FQD7N30TF
1	Q3	XSTR, PNP, SOT23, 300 V, 500 mA	Fairchild	MMBTA92
1	Q5	XSTR, NFET, SOT23, 100 V, 170 mA	Fairchild	BSS123
1	J1	Terminal Block 2 pos	Phoenix Contact	1715721
1	F1	Fuse, 125 V, 1,25 A	bel	SSQ 1.25

8.2.3 Application Curve

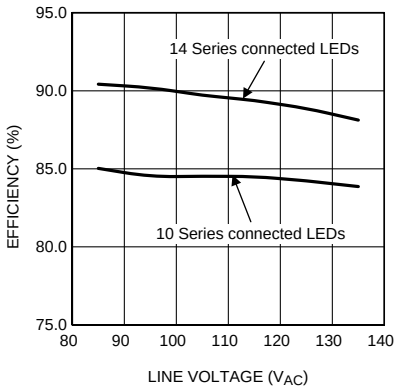


Figure 31. Efficiency versus Input Voltage

9 Power Supply Recommendations

Use any AC power supply capable of the maximum application requirements for voltage and total power.

10 Layout

10.1 Layout Guidelines

Keep the low power components for ASNS, FLTR1, FLTR2, and COFF close to the LM3445 with short traces. The ISNS trace should also be as short and direct as possible. Keep the high current switching paths generated by R3, Q2, L2, and D10 as short as possible to minimize generated switching noise and improve EMI.

10.2 Layout Example

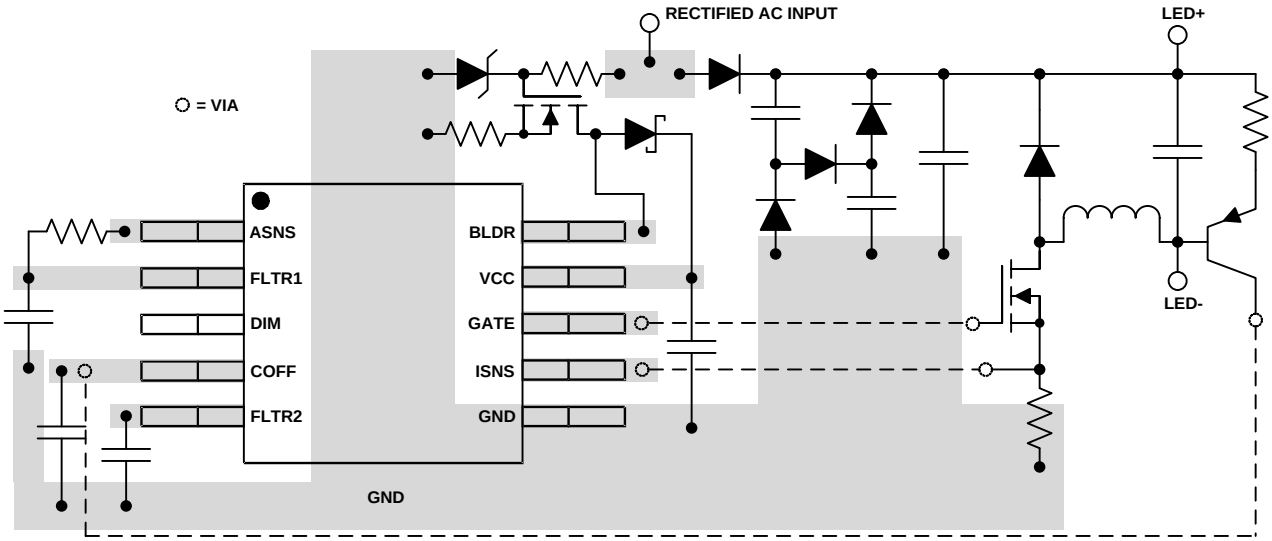


Figure 32. Layout Recommendation

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3445M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LM3445M	Samples
LM3445MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU NIPDAUAG | CU SN	Level-1-260C-UNLIM	-40 to 125	SULB	Samples
LM3445MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU NIPDAUAG | CU SN	Level-1-260C-UNLIM	-40 to 125	SULB	Samples
LM3445MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LM3445M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

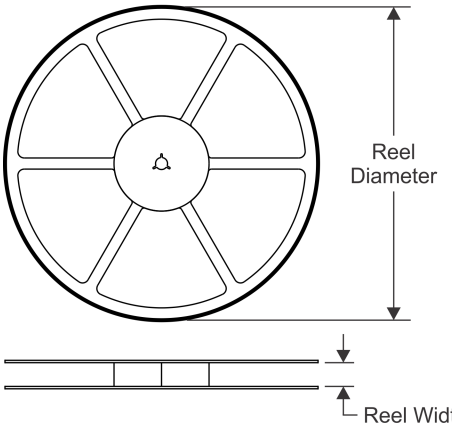
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

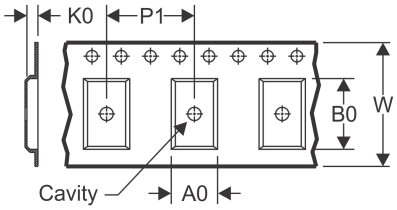
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

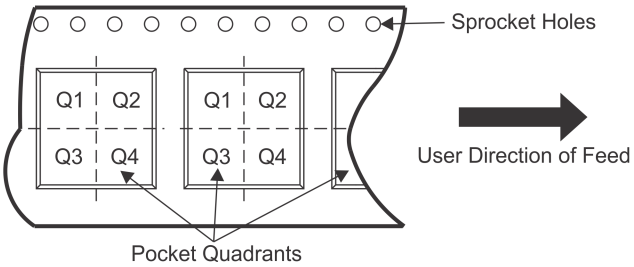


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

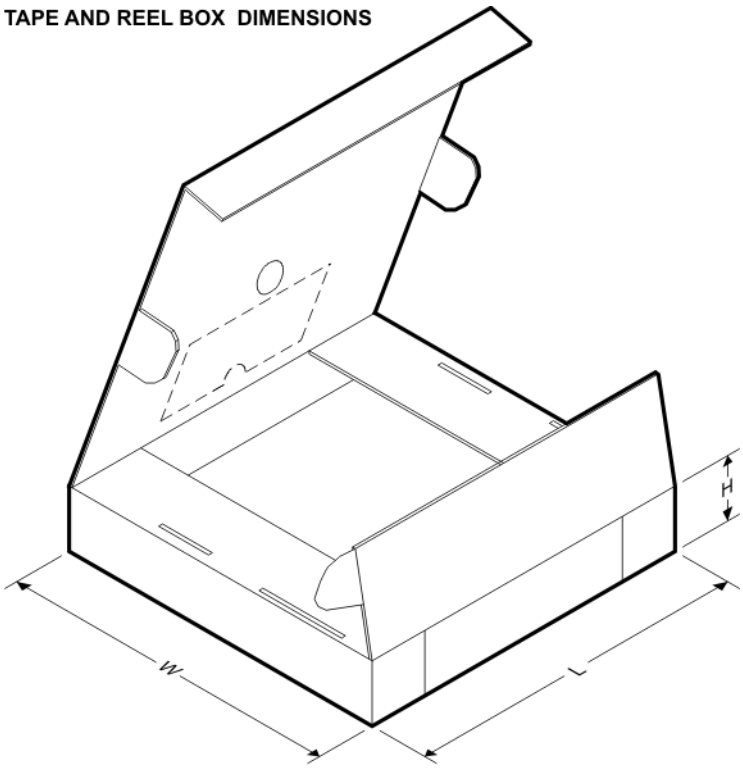
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

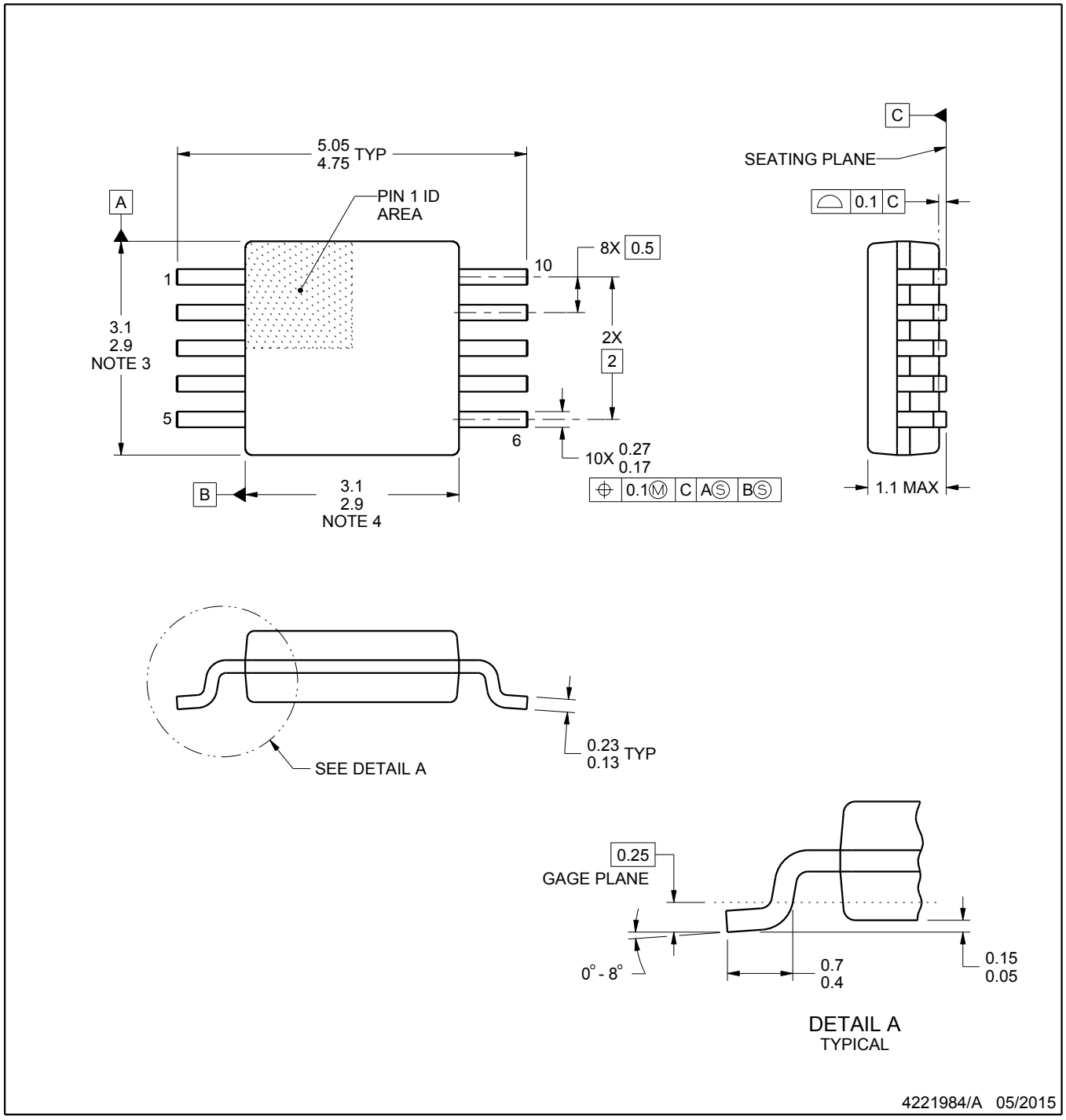
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3445MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3445MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3445MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



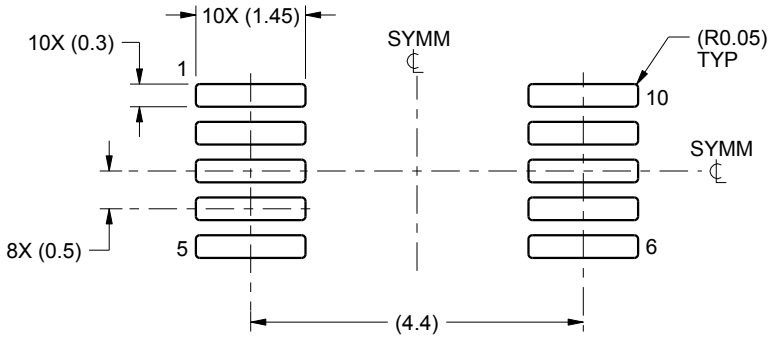
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3445MM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM3445MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM3445MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

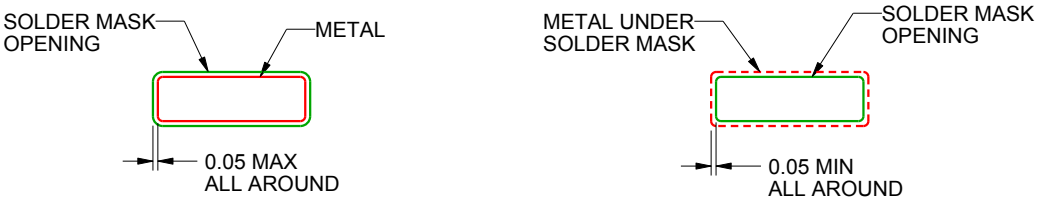


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

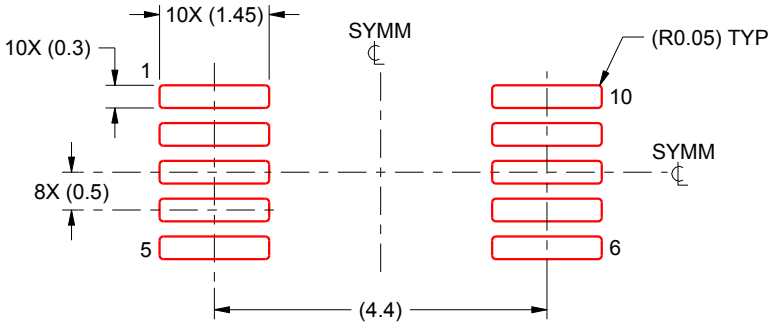
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



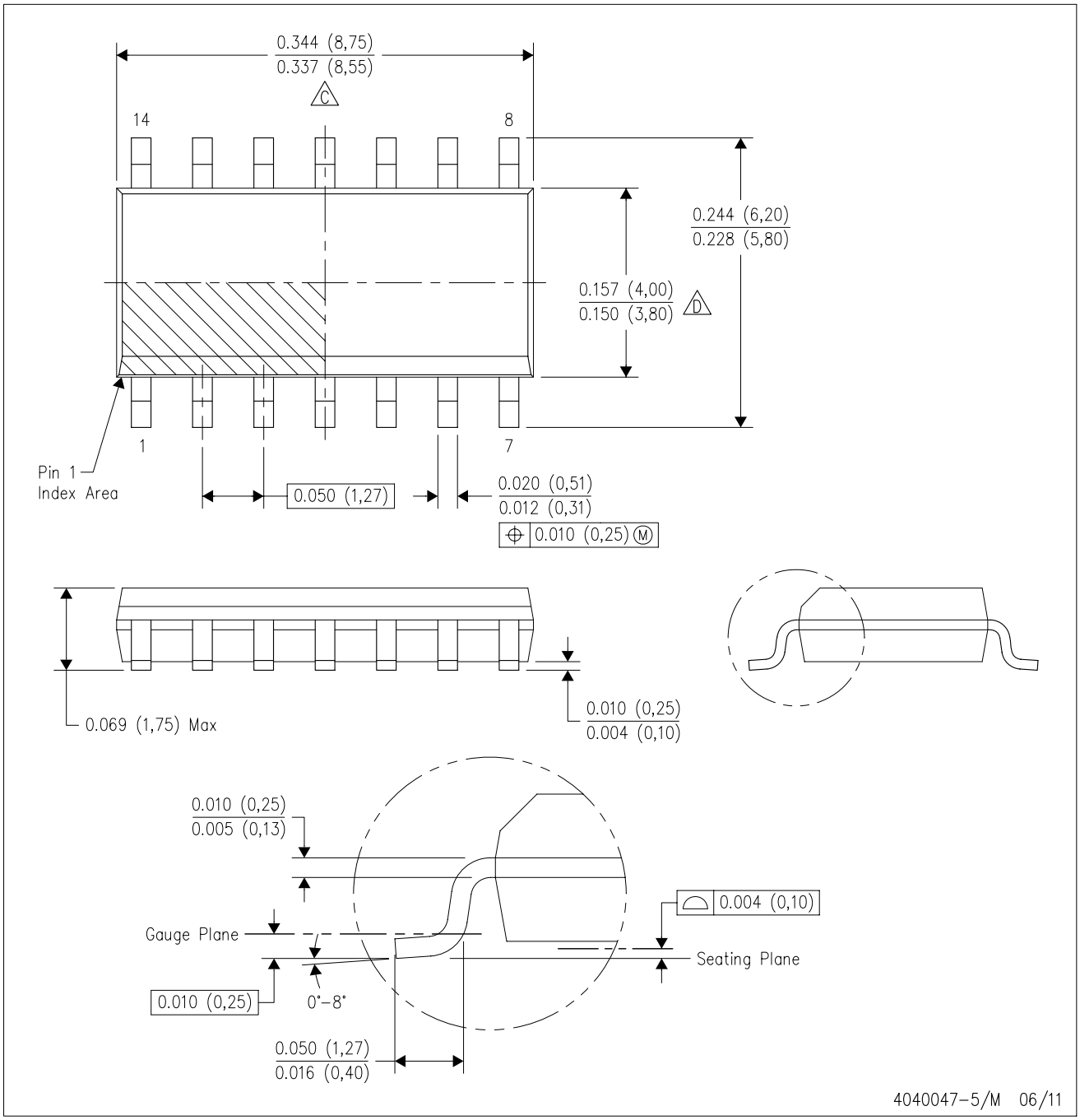
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

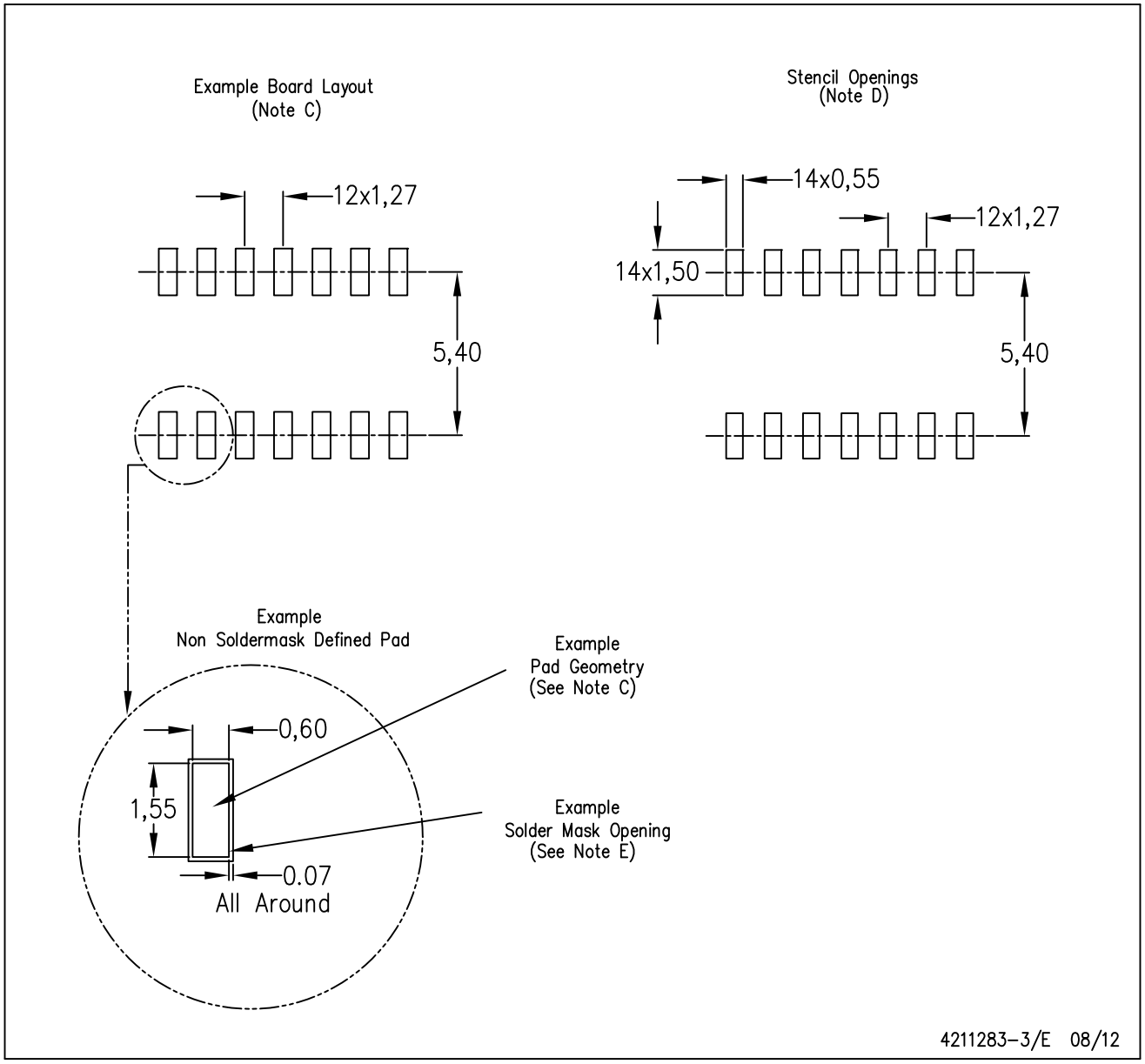
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.