THE DATASHEET OF

LM3444MM/NOPB

LM3444 AC-DC Offline LED Driver

1 Features

- Application Voltage Range: 80 V_{AC} to 277 V_{AC}
- Capable of Controlling LED Currents Greater than 1 A
- Adjustable Switching Frequency
- Low Quiescent Current
- Adaptive Programmable Off-Time Allows for Constant Ripple Current
- Thermal Shutdown
- No Flicker at 120 Hz
- Low-Profile 10-Pin VSSOP Package or 8-Lead SOIC Package
- Patented Drive Architecture

2 Applications

- Solid State Lighting
- Industrial and Commercial Lighting
- Residential Lighting

3 Description

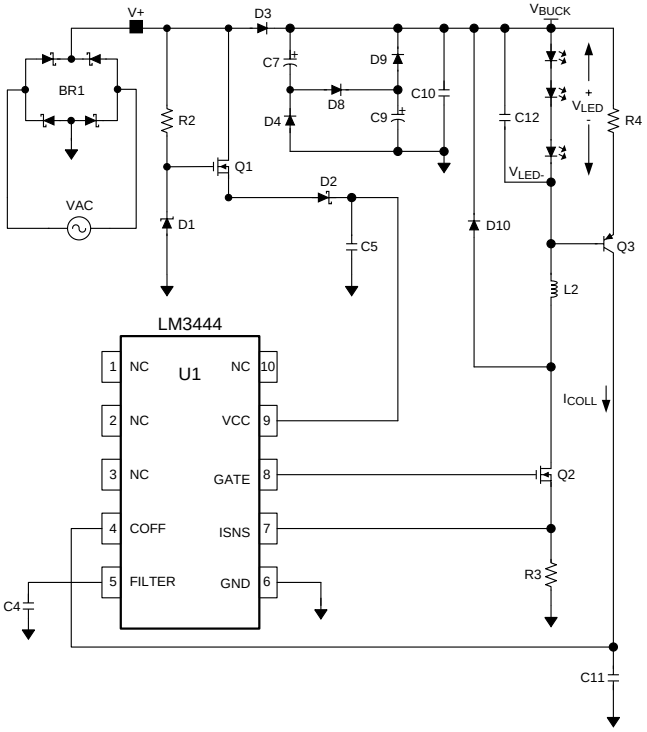
The LM3444 is an adaptive constant off-time AC/DC buck (step-down) constant current controller that provides a constant current for illuminating high power LEDs. The high-frequency capable architecture allows the use of small external passive components. A passive PFC circuit ensures good power factor by drawing current directly from the line for most of the cycle, and provides a constant positive voltage to the buck regulator. Additional features include thermal shutdown, current limit and V_{CC} undervoltage lockout. The LM3444 is available in a low profile 10-pin VSSOP package or an 8-lead SOIC package.

Device Information[1]

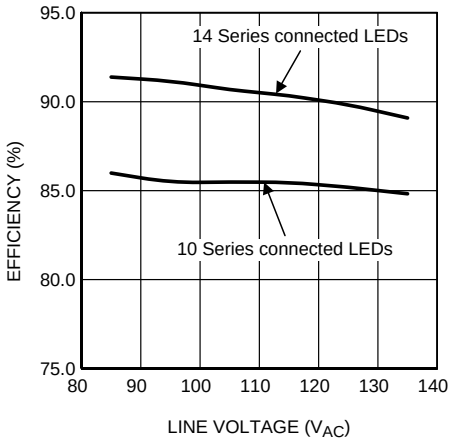
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3444	VSSOP (10)	3.00 mm × 3.00 mm
	SOIC (8)	3.91 mm × 4.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical LM3444 LED Driver Application Circuit



Efficiency vs Line Voltage



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2013) to Revision D **Page**

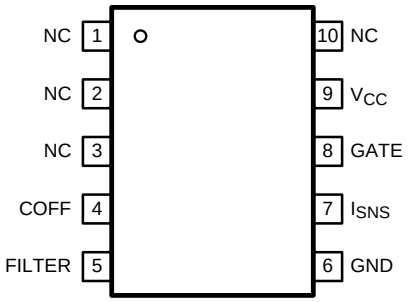
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision B (May 2013) to Revision C **Page**

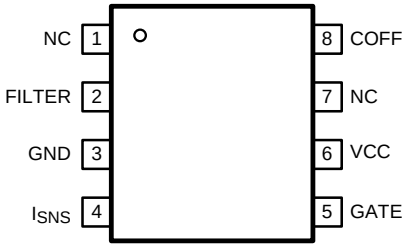
- Changed layout of National Data Sheet to TI format ... 23

5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



D Package
8-Lead SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	VSSOP	SOIC		
COFF	4	8	I	OFF time setting pin. A user set current and capacitor connected from the output to this pin sets the constant OFF time of the switching controller.
FILTER	5	2	I	Filter input. A low pass filter tied to this pin can filter a PWM dimming signal to supply a DC voltage to control the LED current. Can also be used as an analog dimming input. If not used for dimming connect a 0.1-µF capacitor from this pin to ground.
GATE	8	5	O	Power MOSFET driver pin. This output provides the gate drive for the power switching MOSFET of the buck controller.
GND	6	3	—	Circuit ground connection
ISNS	7	4	I	LED current sense pin. Connect a resistor from main switching MOSFET source, ISNS to GND to set the maximum LED current.
NC	1, 2, 3, 10	1, 7	—	No internal connection. Leave this pin open.
VCC	9	6	O	Input voltage pin. This pin provides the power for the internal control circuitry and gate driver.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
	V_{CC} and GATE to GND	–0.3	14	V
	ISNS to GND	–0.3	2.5	V
	FILTER and COFF to GND	–0.3	7	V
	COFF input current		60	mA
	Continuous power dissipation(3)	Internally limited		
T_J	Junction temperature		150	°C
	Maximum lead temperature (soldering)		260	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typical) and disengages at T_J = 145°C (typical).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}		8	13	V
T_J	Junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LM3444		UNIT
		DGS (VSSOP)	D (SOIC)	
		10 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163.8	111.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.4	58.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.6	51.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	11.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82.3	51.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

All typical limits are for T_J = 25°C and all maximum and minimum limits apply over the full operating temperature range (T_J = −40°C to 125°C). Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{CC} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} SUPPLY						
I_{VCC}	Operating supply current			1.58	2.25	mA
$V_{CC-UVLO}$	Rising threshold			7.4	7.7	V
	Falling threshold		6	6.4		
	Hysterisis			1		
COFF						
V_{COFF}	Time-out threshold		1.225	1.276	1.327	V
R_{COFF}	Off timer sinking impedance			33	60	Ω
t_{COFF}	Restart timer			180		µs
CURRENT LIMIT						
V_{ISNS}	ISNS limit threshold		1.174	1.269	1.364	V
t_{ISNS}	Leading edge blanking time			125		ns
	Current limit reset delay			180		µs
	ISNS limit to GATE delay	ISNS = 0 to 1.75-V step		33		ns
CURRENT SENSE COMPARATOR						
V_{FILTER}	FILTER open circuit voltage		720	750	780	mV
R_{FILTER}	FILTER impedance			1.12		MΩ
V_{OS}	Current sense comparator offset voltage		–4	0.1	4	mV
GATE DRIVE OUTPUT						
V_{DRVH}	GATE high saturation	I_{GATE} = 50 mA		0.24	0.5	V
V_{DRVL}	GATE low saturation	I_{GATE} = 100 mA		0.22	0.5	
I_{DRV}	Peak souce current	GATE = V_{CC}/2		–0.77		A
	Peak sink current	GATE = V_{CC}/2		0.88		
t_{DV}	Rise time	C_{load} = 1 nF		15		ns
	Fall time	C_{load} = 1 nF		15		
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature	See (1)		165		°C
	Thermal shutdown hysteresis			20		

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

6.6 Typical Characteristics

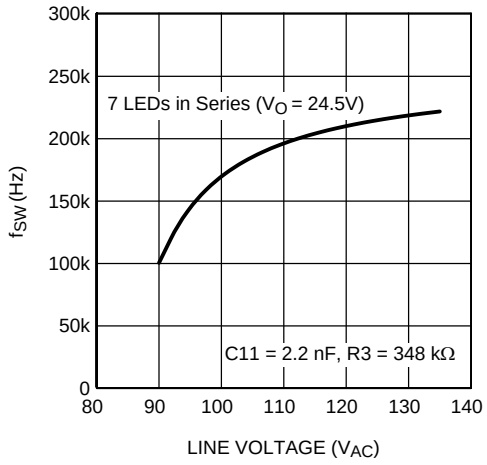


Figure 1. f_{SW} vs Input Line Voltage

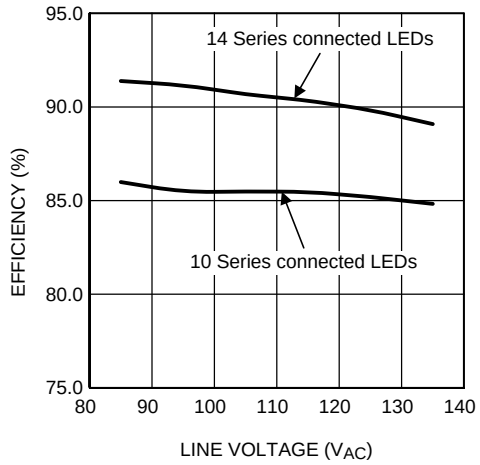


Figure 2. Efficiency vs Input Line Voltage

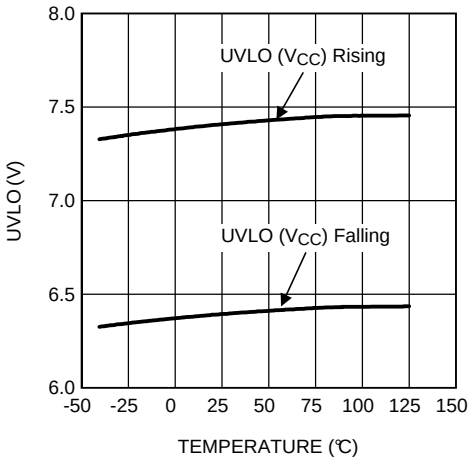


Figure 3. V_{CC} UVLO vs Temperature

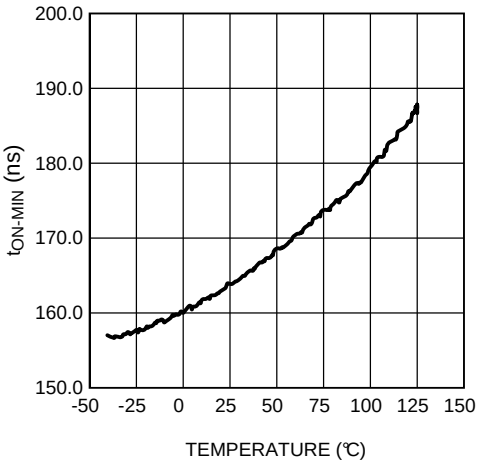


Figure 4. Minimum On-Time (t_{ON}) vs Temperature

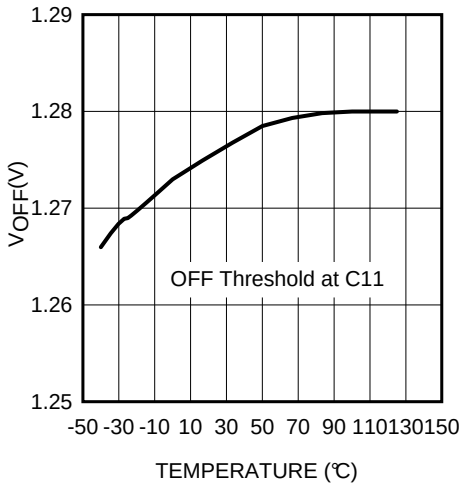


Figure 5. Off Threshold (C11) vs Temperature

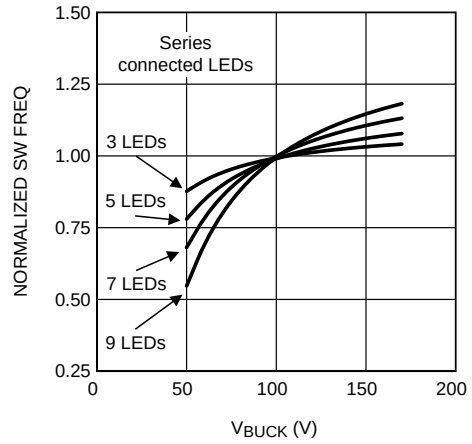


Figure 6. Normalized Variation in f_{SW} Over V_{BUCK} Voltage

Typical Characteristics (continued)

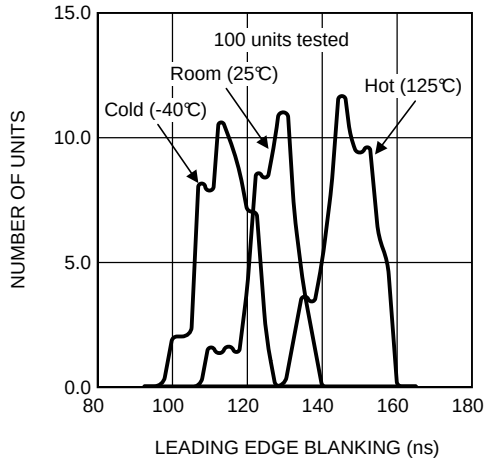


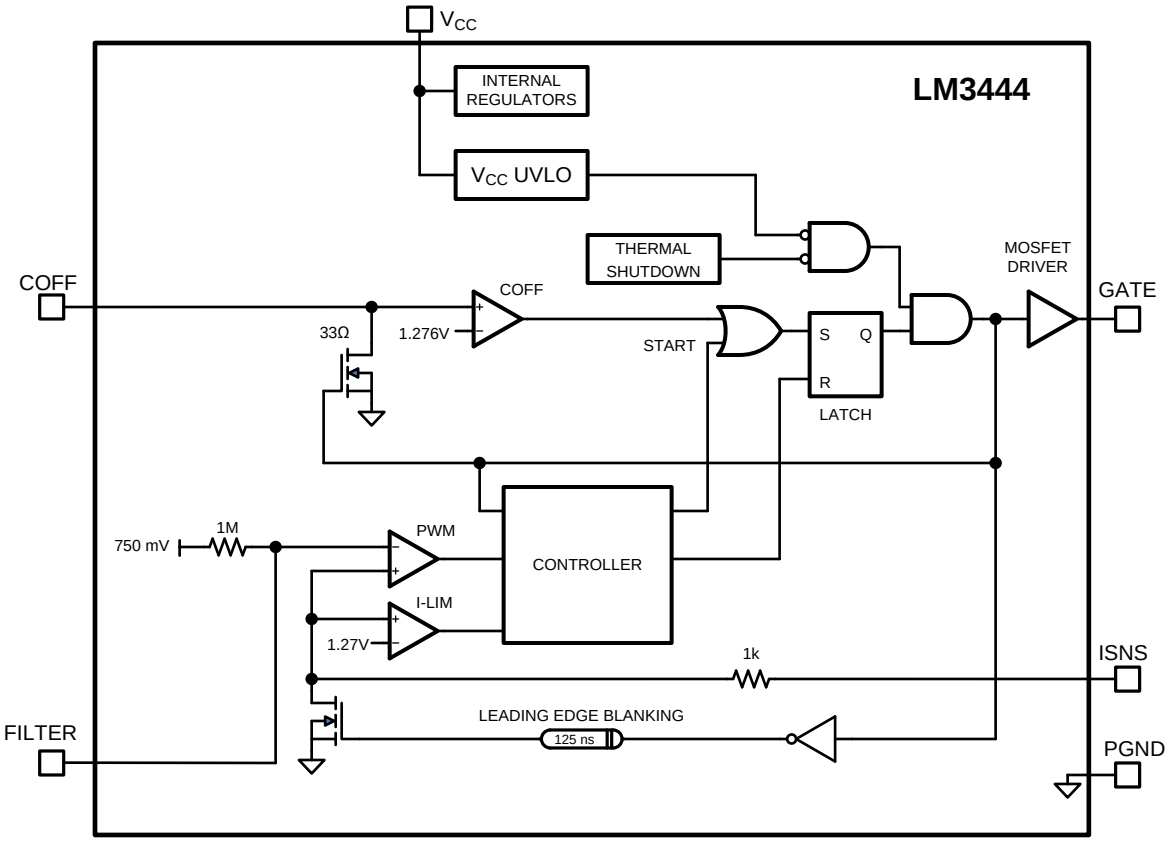
Figure 7. Leading Edge Blanking Variation Over Temperature

7 Detailed Description

7.1 Overview

The LM3444 device contains all the necessary circuitry to build a line-powered (mains powered) constant current LED driver.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Theory of Operation

For an image of the LM3444 along with basic external circuitry, see Figure 8.

Feature Description (continued)

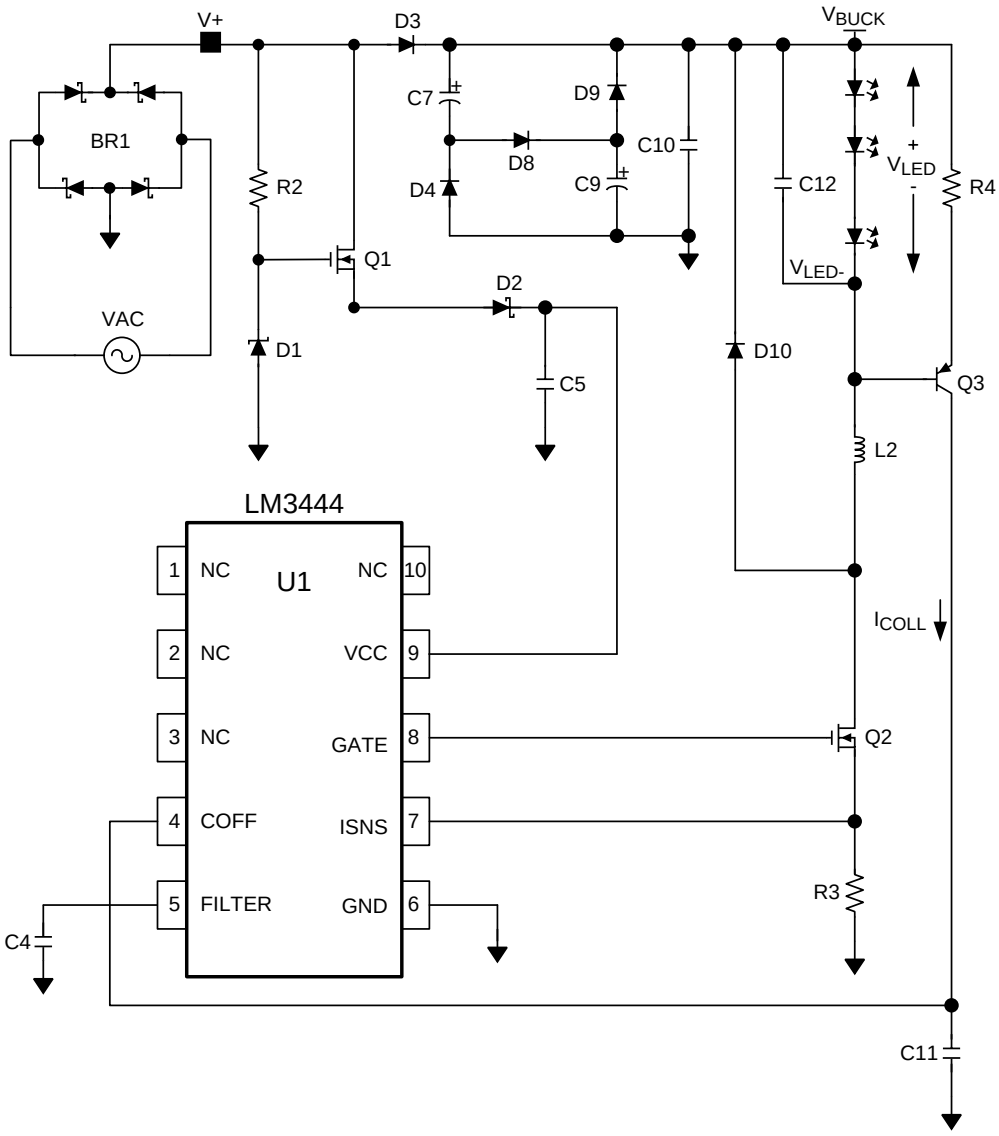


Figure 8. LM3444 Schematic

7.3.2 Valley-Fill Circuit

V_{BUCK} supplies the power which drives the LED string. Diode D3 allows V_{BUCK} to remain high while V+ cycles on and off. V_{BUCK} has a relatively small hold capacitor C10 which reduces the voltage ripple when the valley fill capacitors are being charged. However, the network of diodes and capacitors shown between D3 and C10 make up a valley-fill circuit. The valley-fill circuit can be configured with two or three stages. The most common configuration is two stages. Figure 9 illustrates a two- and three-stage valley-fill circuit.

Feature Description (continued)

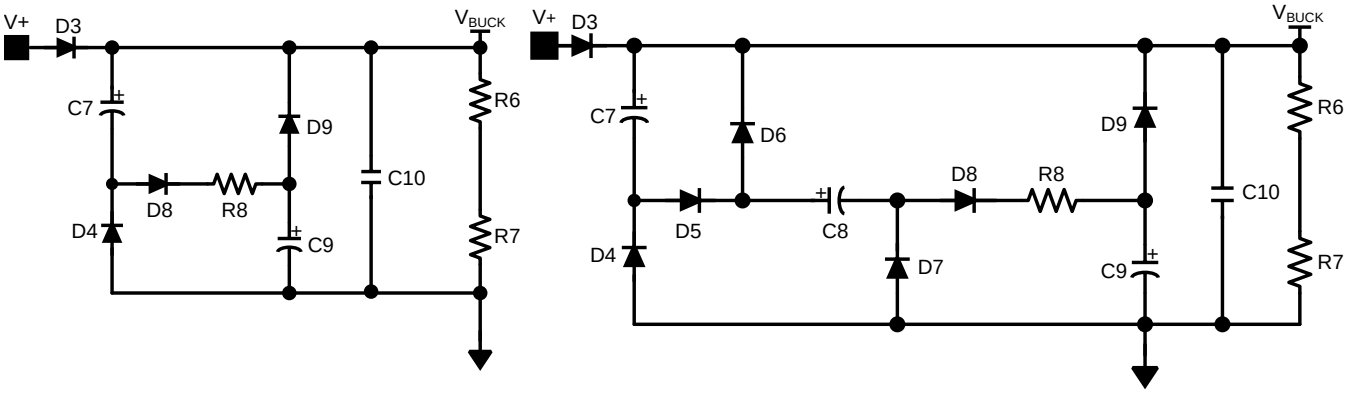


Figure 9. Two and Three Stage Valley Fill Circuit

The valley-fill circuit allows the buck regulator to draw power throughout a larger portion of the AC line. This allows the capacitance needed at V_{BUCK} to be lower than if there were no valley-fill circuit, and adds passive power factor correction (PFC) to the application.

7.3.3 Valley-Fill Operation

When the input line is high, power is derived directly through D3. The term *input line is high* is explained as follows. The valley-fill circuit charges capacitors C7 and C9 in series (Figure 10) when the input line is high.

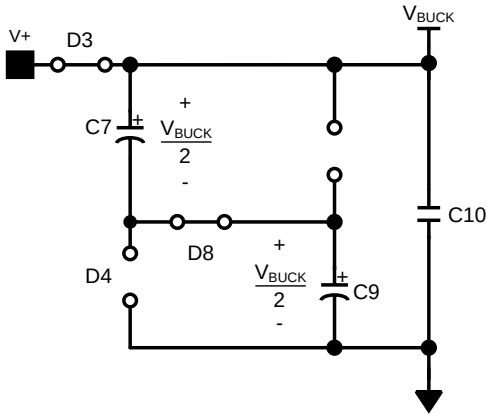


Figure 10. Two Stage Valley-Fill Circuit When AC Line is High

The peak voltage of a two-stage valley-fill capacitor is given by Equation 1.

$$V_{VF\text{-}CAP} = \frac{V_{AC\text{-}RMS}\sqrt{2}}{2} \quad (1)$$

As the AC line decreases from its peak value every cycle, there is a point where the voltage magnitude of the AC line is equal to the voltage that each capacitor is charged. At this point, diode D3 becomes reversed biased, and the capacitors are placed in parallel to each other (Figure 11), and V_{BUCK} equals the capacitor voltage.

Feature Description (continued)

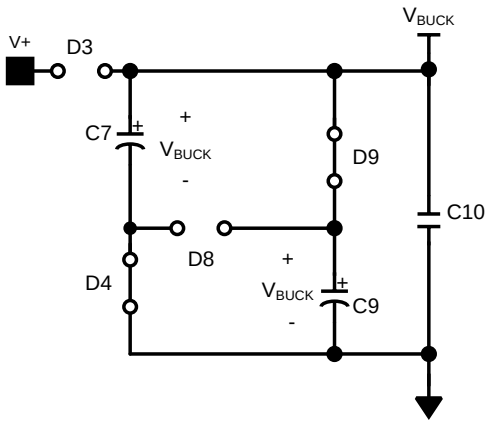


Figure 11. Two Stage Valley-Fill Circuit when AC Line is Low

A three stage valley-fill circuit performs exactly the same as two-stage valley-fill circuit, except now three capacitors are charged in series when the line voltage decreases, as shown in Equation 2:

$$V_{VF\text{-}CAP} = \frac{V_{AC\text{-}RMS}\sqrt{2}}{3} \quad (2)$$

Diode D3 is reverse-biased and three capacitors are in parallel to each other.

The valley-fill circuit can be optimized for power factor, voltage hold-up, and overall application size and cost. The LM3444 operates with a single-stage or a three-stage valley-fill circuit as well. Resistor R8 functions as a current limiting resistor during start-up, and during the transition from series to parallel connection. Resistors R6 and R7 are 1-MΩ bleeder resistors, and may or may not be necessary for each application.

7.3.4 Buck Converter

The LM3444 is a buck controller that uses a proprietary constant off-time method to maintain constant current through a string of LEDs. While transistor Q2 is on, current ramps up through the inductor and LED string. A resistor R3 senses this current and this voltage is compared to the reference voltage at FILTER. When this sensed voltage is equal to the reference voltage, transistor Q2 is turned off and diode D10 conducts the current through the inductor and LEDs. Capacitor C12 eliminates most of the ripple current seen in the inductor. Resistor R4, capacitor C11, and transistor Q3 provide a linear current ramp that sets the constant off-time for a given output voltage.

Feature Description (continued)

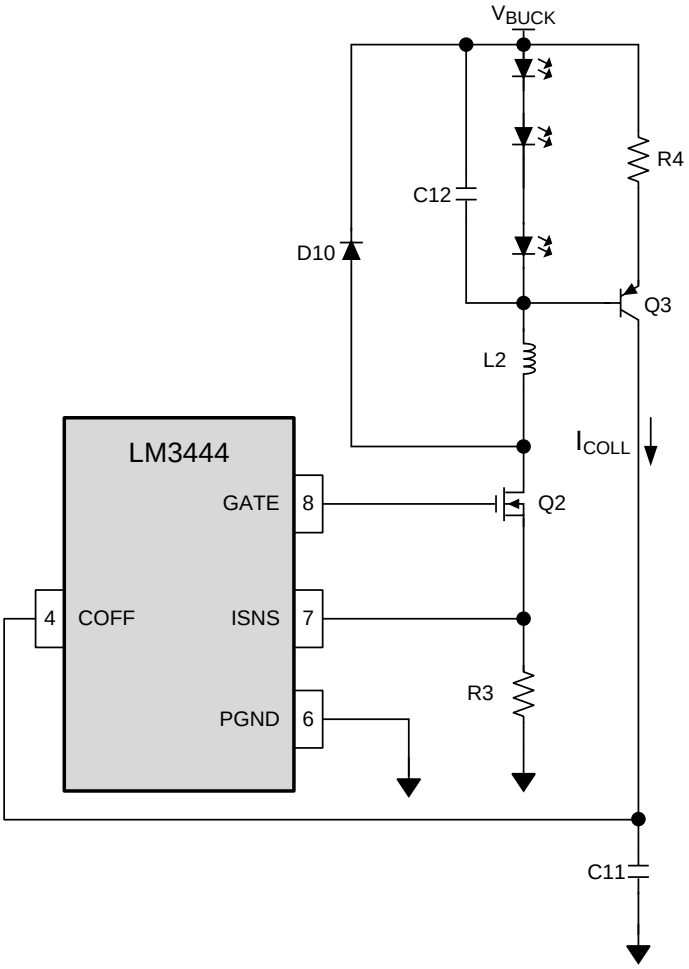


Figure 12. LM3444 Buck Regulation Circuit

7.3.5 Overview Of Constant Off-Time Control

The conversion ratio of a buck converter is defined as given by Equation 3.

$$\frac{V_O}{V_{IN}} = D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times f_{SW} \quad (3)$$

Constant off-time control architecture operates by simply defining the off-time and allowing the on-time, and therefore the switching frequency, to vary as either V_{IN} or V_O changes. The output voltage is equal to the LED string voltage (V_{LED}), and should not change significantly for a given application. The input voltage or V_{BUCK} in this analysis varies as the input line varies. The length of the on-time is determined by the sensed inductor current through a resistor to a voltage reference at a comparator. During the on-time, denoted by t_{ON}, MOSFET switch Q2 is on causing the inductor current to increase. During the on-time, current flows from V_{BUCK}, through the LEDs, through L2, Q2, and finally through R3 to ground. At some point in time, the inductor current reaches a maximum ($I_{L2\text{-}PK}$) determined by the voltage sensed at R3 and the ISNS pin. This sensed voltage across R3 is compared against the voltage of FILTER, at which point Q2 is turned off by the controller.

Feature Description (continued)

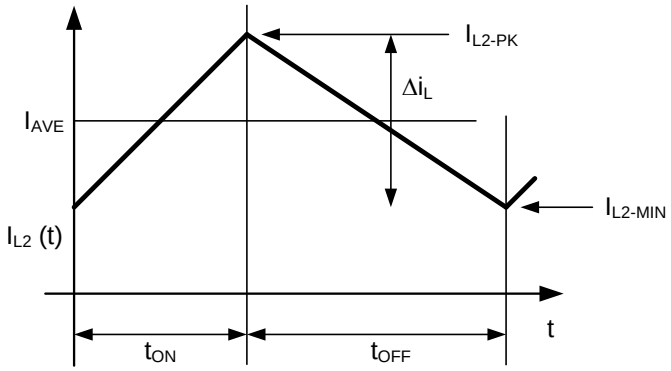


Figure 13. Inductor Current Waveform in CCM

During the off-period denoted by t_{OFF}, the current through L2 continues to flow through the LEDs through D10.

7.3.6 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 165°C. After thermal shutdown occurs, the output switch does not turn on until the junction temperature drops to approximately 145°C.

7.4 Device Functional Modes

This device does not have any additional functional modes.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Determining Duty-Cycle (D)

Equation 4 shows the duty-cycle (D).

$$\frac{V_{LED}}{V_{BUCK}} = D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times f_{SW} \tag{4}$$

Equation 5 shows the duty-cycle with efficiency considered.

$$\frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}} = D \tag{5}$$

For simplicity, choose efficiency from 75% to 85%.

8.1.2 Calculating Off-Time

The off-time of the LM3444 is set by the user and remains fairly constant as long as the voltage of the LED stack remains constant. Calculating the off-time is the first step in determining the switching frequency of the converter, which is integral in determining some external component values.

PNP transistor Q3, resistor R4, and the LED string voltage define a charging current into capacitor C11. A constant current into a capacitor creates a linear charging characteristic.

$$i = C\frac{dv}{dt} \tag{6}$$

Resistor R4, capacitor C11 and the current through resistor R4 (i_{COLL}), which is approximately equal to V_{LED}/R4, are all fixed. Therefore, dv is fixed and linear, and dt (t_{OFF}) can now be calculated as shown in Equation 7.

$$t_{OFF} = C11 \times 1.276V \times \left(\frac{R4}{V_{LED}}\right) \tag{7}$$

Common equations for determining duty-cycle and switching frequency in any buck converter are shown in Equation 8.

$$f_{SW} = \frac{1}{t_{OFF} + t_{ON}}$$

$$D = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_{LED}}{V_{BUCK}}$$

$$D' = \frac{t_{OFF}}{t_{ON} + t_{OFF}} \tag{8}$$

Therefore, Equation 9 shows:

$$f_{SW} = \frac{D}{t_{ON}}, \text{ and } f_{SW} = \frac{1 - D}{t_{OFF}} \tag{9}$$

Application Information (continued)

With efficiency of the buck converter in mind, Equation 10 shows:

$$\frac{V_{LED}}{V_{BUCK}} = \eta \times D \tag{10}$$

Substituting and rearranging the equations, Equation 11 shows:

$$f_{SW} = \frac{\left(1 - \frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}}\right)}{t_{OFF}} \tag{11}$$

Off-time and switching frequency can now be calculated using the previous equations.

8.1.3 Setting the Switching Frequency

Selecting the switching frequency for nominal operating conditions is based on tradeoffs between efficiency (better at low frequency) and solution size and cost (smaller at high frequency).

The input voltage to the buck converter (V_{BUCK}) changes with both line variations and over the course of each half-cycle of the input line voltage. The voltage across the LED string, however, remains constant, and therefore the off-time remains constant.

The on-time, and therefore the switching frequency, varies as the V_{BUCK} voltage changes with line voltage. A good design practice is to choose a desired nominal switching frequency knowing that the switching frequency decreases as the line voltage drops, and increases as the line voltage increases (Figure 14).

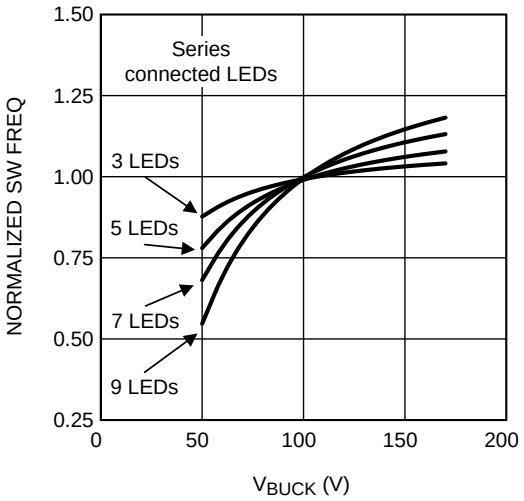


Figure 14. Graphical Illustration of Switching Frequency vs V_{BUCK}

The off-time of the LM3444 can be programmed for switching frequencies ranging from 30 kHz to over 1 MHz. A trade-off between efficiency and solution size must be considered when designing the LM3444 application.

The maximum switching frequency attainable is limited only by the minimum on-time requirement (200 ns).

Worst case scenario for minimum on time is when V_{BUCK} is at its maximum voltage (AC high line) and the LED string voltage (V_{LED}) is at its minimum value, as shown in Equation 12.

$$t_{ON(MIN)} = \left(\frac{1}{\eta} \times \frac{V_{LED(MIN)}}{V_{BUCK(MAX)}}\right) \frac{1}{f_{SW}} \tag{12}$$

Application Information (continued)

The maximum voltage seen by the Buck Converter is given by Equation 13.

$$V_{BUCK(MAX)} = V_{AC\text{-}RMS(MAX)} \times \sqrt{2} \quad (13)$$

8.1.4 Inductor Selection

The controlled off-time architecture of the LM3444 regulates the average current through the inductor (L2), and therefore the LED string current. The input voltage to the buck converter (V_{BUCK}) changes with line variations and over the course of each half-cycle of the input line voltage. The voltage across the LED string is relatively constant, and therefore the current through R4 is constant. This current sets the off-time of the converter and therefore the output volt-second product (V_{LED} × off-time) remains constant. A constant volt-second product makes it possible to keep the ripple through the inductor constant as the voltage at V_{BUCK} varies.

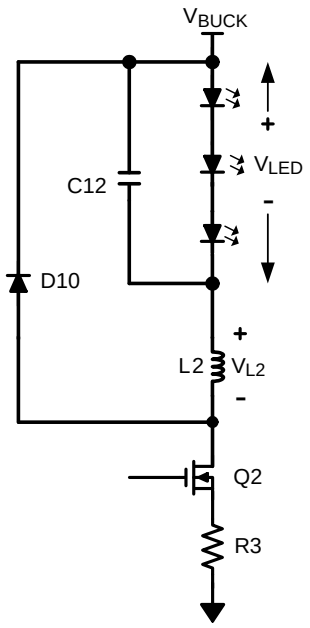


Figure 15. LM3444 External Components of the Buck Converter

Use Equation 14 to calculate an ideal inductor.

$$v = L\frac{di}{dt} \quad (14)$$

Given a fixed inductor value, L, Equation 14 states that the change in the inductor current over time is proportional to the voltage applied across the inductor.

During the on-time, the voltage applied across the inductor is given in Equation 15.

$$V_{L(ON\text{-}TIME)} = V_{BUCK} - (V_{LED} + V_{DS(Q2)} + I_{L2} \times R3) \quad (15)$$

Because the voltage across the MOSFET switch (Q2) is relatively small, as is the voltage across sense resistor R3, we can approximately simplify this as shown in Equation 16,

$$V_{L(ON\text{-}TIME)} = V_{BUCK} - V_{LED} \quad (16)$$

During the off-time, the voltage seen by the inductor is given by Equation 17.

$$V_{L(OFF\text{-}TIME)} = V_{LED} \quad (17)$$

Application Information (continued)

The value of $V_{L(OFF-TIME)}$ is relatively constant, because the LED stack voltage remains constant. If we rewrite the equation for an inductor inserting what we know about the circuit during the off-time, Equation 18 shows that we get:

$$V_{L(OFF-TIME)} = V_{LED} = L \times \frac{\Delta i}{\Delta t}$$

$$V_{L(OFF-TIME)} = V_{LED} = L \times \frac{(I_{(MAX)} - I_{(MIN)})}{\Delta t} \quad (18)$$

Rearranging this gives Equation 19.

$$\Delta i \cong t_{OFF} \times \frac{V_{LED}}{L2} \quad (19)$$

From this, we can see that the ripple current (Δi) is proportional to off-time (t_{OFF}) multiplied by a voltage, which is dominated by V_{LED} divided by a constant (L2).

These equations can be rearranged to calculate the desired value for inductor L2, as shown in Equation 20.

$$L2 \cong t_{OFF} \times \frac{V_{LED}}{\Delta i} \quad (20)$$

The off time can be calculated using Equation 21:

$$t_{OFF} = \frac{\left(1 - \frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}}\right)}{f_{SW}} \quad (21)$$

Substituting t_{off} in Equation 21 results in Equation 22:

$$L2 = \frac{V_{LED}\left(1 - \frac{1}{\eta} \times \frac{V_{LED}}{V_{BUCK}}\right)}{f_{SW} \times \Delta i} \quad (22)$$

See *Typical Application* to better understand the design process.

8.1.5 Setting the LED Current

The LM3444 constant off-time control loop regulates the peak inductor current (I_{L2}). The average inductor current equals the average LED current (I_{AVE}). Therefore the average LED current is regulated by regulating the peak inductor current.

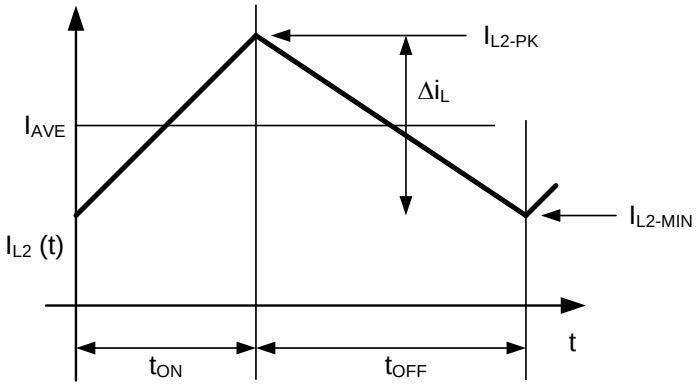


Figure 16. Inductor Current Waveform in CCM

Application Information (continued)

Knowing the desired average LED current, I_{AVE}, and the nominal inductor current ripple, Δi_L, the peak current for an application running in continuous conduction mode (CCM) is defined in Equation 23.

$$I_{L2\text{-}PK} = I_{AVE} + \frac{\Delta i_L}{2} \tag{23}$$

The LED current would then be calculated using Equation 24.

$$I_{AVE(UNDIM)} = I_{L2\text{-}PK(UNDIM)} - \frac{\Delta i_L}{2} \tag{24}$$

This is important to calculate because this peak current multiplied by the sense resistor R3 determines when the internal comparator is tripped. The internal comparator turns the control MOSFET off once the peak sensed voltage reaches 750 mV.

$$I_{L\text{-}PK(UNDIM)} = \frac{750\ mV}{R3} \tag{25}$$

Current Limit: The trip voltage on the PWM comparator is 750 mV. However, if there is a short circuit or an excessive load on the output, higher than normal switch currents cause a voltage greater than 1.27 V on the ISNS pin which trip the I-LIM comparator. The I-LIM comparator resets the RS latch, turning off Q2. It also inhibits the Start Pulse Generator and the COFF comparator by holding the COFF pin low. A delay circuit prevents the start of another cycle for 180 µs.

8.1.6 Valley Fill Capacitors

Determining voltage rating and capacitance value of the valley-fill capacitors:

The maximum voltage seen by the valley-fill capacitors is calculated by Equation 26.

$$V_{VF\text{-}CAP} = \frac{V_{AC(MAX)}\sqrt{2}}{\#stages} \tag{26}$$

This is, of course, if the capacitors chosen have identical capacitance values and split the line voltage equally. Often a 20% difference in capacitance could be observed between like capacitors. Therefore a voltage rating margin of 25% to 50% should be considered.

8.1.7 Determining the Capacitance Value of the Valley-Fill Capacitors

The valley-fill capacitors must be sized to supply energy to the buck converter (V_{BUCK}) when the input line is less than its peak divided by the number of stages used in the valley fill (t_X). The capacitance value must be calculated for the maximum LED current.

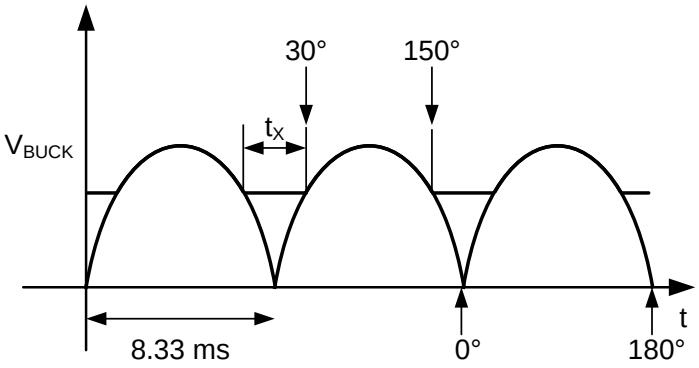


Figure 17. Two Stage Valley-Fill V_{BUCK} Voltage

Application Information (continued)

From Figure 17 and the equation for current in a capacitor, i = C × dV/dt, the amount of capacitance needed at V_{BUCK} is calculated as follows.

At 60 Hz, and a valley-fill circuit of two stages, the hold-up time (t_X) required at V_{BUCK} is calculated as follows. The total angle of an AC half cycle is 180° and the total time of a half AC line cycle is 8.33 ms. When the angle of the AC waveform is at 30° and 150°, the voltage of the AC line is exactly ½ of its peak. With a two-stage valley-fill circuit, this is the point where the LED string switches from power being derived from AC line to power being derived from the hold up capacitors (C7 and C9). 60° out of 180° of the cycle or 1/3 of the cycle the power is derived from the hold up capacitors (1/3 × 8.33 ms = 2.78 ms). This is equal to the hold up time (dt) from the previous equation, and dv is the amount of voltage the circuit is allowed to droop. From *Determining Maximum Number of Series Connected LEDs Allowed*, we know the minimum V_{BUCK} voltage is about 45 V for a 90-V_{AC} to 135-V_{AC} line. At 90-V_{AC} low-line operating condition input, ½ of the peak voltage is 64 V. Thus, with some margin, the voltage at V_{BUCK} can not droop more than about 15 V (dv). (i) is equal to (P_{OUT}/V_{BUCK}), where P_{OUT} is equal to ($V_{LED} \times I_{LED}$). Total capacitance (C7 in parallel with C9) can now be calculated. See *Typical Application* for further calculations of the valley-fill capacitors.

8.1.8 Determining Maximum Number of Series Connected LEDs Allowed

The LM3444 is an off-line buck topology LED driver. A buck converter topology requires that the input voltage (V_{BUCK}) of the output circuit must be greater than the voltage of the LED stack (V_{LED}) for proper regulation. One must determine what the minimum voltage observed by the buck converter is before the maximum number of LEDs allowed can be determined. The following two variables must be determined to accomplish this:

1. AC line operating voltage. This is usually 90 V_{AC} to 135 V_{AC} for North America. Although the LM3444 can operate at much lower and higher input voltages, a range is needed to illustrate the design process.
2. The number of stages implemented in the valley-fill circuit (1, 2, or 3).

In this example, the most common valley-fill circuit is used (two stages).

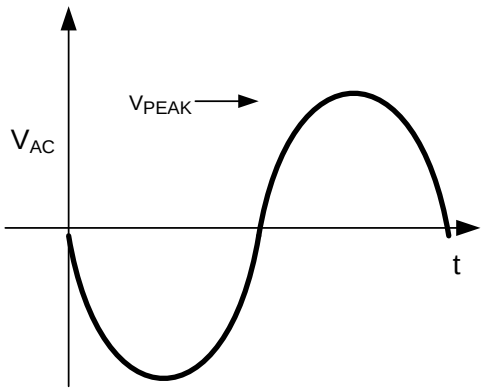


Figure 18. AC Line

Figure 18 shows the AC waveform. One can easily see that the peak voltage (V_{PEAK}) is always given by Equation 27.

$$V_{AC\text{-}RMS\text{-}PK}\sqrt{2} \tag{27}$$

The voltage at V_{BUCK} with a valley-fill stage of two looks similar to the waveforms in Figure 17.

The purpose of the valley-fill circuit is to allow the buck converter to pull power directly off of the AC line when the line voltage is greater than its peak voltage divided by two (two-stage valley-fill circuit). During this time, the capacitors within the valley fill circuit (C7 and C8) are charged up to the peak of the AC line voltage. Once the line drops below its peak divided by two, the two capacitors are placed in parallel and deliver power to the buck converter. One can now see that if the peak of the AC line voltage is lowered due to variations in the line voltage, the DC offset (V_{DC}) lowers. V_{DC} is the lowest value that voltage V_{BUCK} encounters.

Application Information (continued)

$$V_{BUCK(MIN)} = \frac{V_{AC\text{-}RMS(MIN)}\sqrt{2}\,x\ SIN(\theta)}{\#stages} \quad (28)$$

Example:

Line voltage = 90 V_{AC} to 135 V_{AC}

Valley-fill = two stage

$$V_{BUCK(MIN)} = \frac{90\sqrt{2}\ x\ SIN(135^{o})}{2} = 45V \quad (29)$$

Depending on what type and value of capacitors are used, some derating should be used for voltage droop when the capacitors are delivering power to the buck converter. With this derating, the lowest voltage the buck converter sees is about 42.5 V in this example.

To determine how many LEDs can be driven, take the minimum voltage the buck converter sees (42.5 V) and divide it by the worst-case forward voltage drop of a single LED.

Example: 42.5 V / 3.7 V = 11.5 LEDs (11 LEDs with margin)

8.1.9 Output Capacitor

A capacitor placed in parallel with the LED or array of LEDs can be used to reduce the LED current ripple while keeping the same average current through both the inductor and the LED array. With a buck topology, the output inductance (L2) can now be lowered, making the magnetics smaller and less expensive. With a well designed converter, you can assume that all of the ripple is seen by the capacitor, and not the LEDs. One must ensure that the capacitor you choose can handle the RMS current of the inductor. See the manufacturer data sheets to ensure compliance. Usually an X5R or X7R capacitor from 1 µF and 10 µF of the proper voltage rating is sufficient.

8.1.10 Switching MOSFET

The main switching MOSFET should be chosen with efficiency and robustness in mind. As shown in Equation 30, the maximum voltage across the switching MOSFET equals:

$$V_{DS(MAX)} = V_{AC\text{-}RMS(MAX)}\sqrt{2} \quad (30)$$

The average current rating should be greater than what is given in Equation 31.

$$I_{DS\text{-}MAX} = I_{LED(\text{-}AVE)}(D_{MAX}) \quad (31)$$

8.1.11 Recirculating Diode

The LM3444 buck converter requires a recirculating diode D10 (see Figure 8) to carry the inductor current during the MOSFET Q2 off-time. The most efficient choice for D10 is a diode with a low forward drop and near-zero reverse recovery time that can withstand a reverse voltage of the maximum voltage seen at V_{BUCK}. For a common 110 V_{AC} ± 20% line, the reverse voltage could be as high as 190 V, as shown in Equation 32.

$$V_D \geq V_{AC\text{-}RMS(MAX)}\sqrt{2} \quad (32)$$

As shown in Equation 33, the current rating must be at least:

$$I_D = (1 - D_{MIN}) \times I_{LED(AVE)} \quad (33)$$

Or as shown in Equation 34:

$$I_D = \left(1 - \frac{V_{LED(MIN)}}{V_{BUCK(MAX)}}\right) x\ I_{LED(AVE)} \quad (34)$$

8.2 Typical Application

The following design example illustrates the process of calculating external component values.

Typical Application (continued)

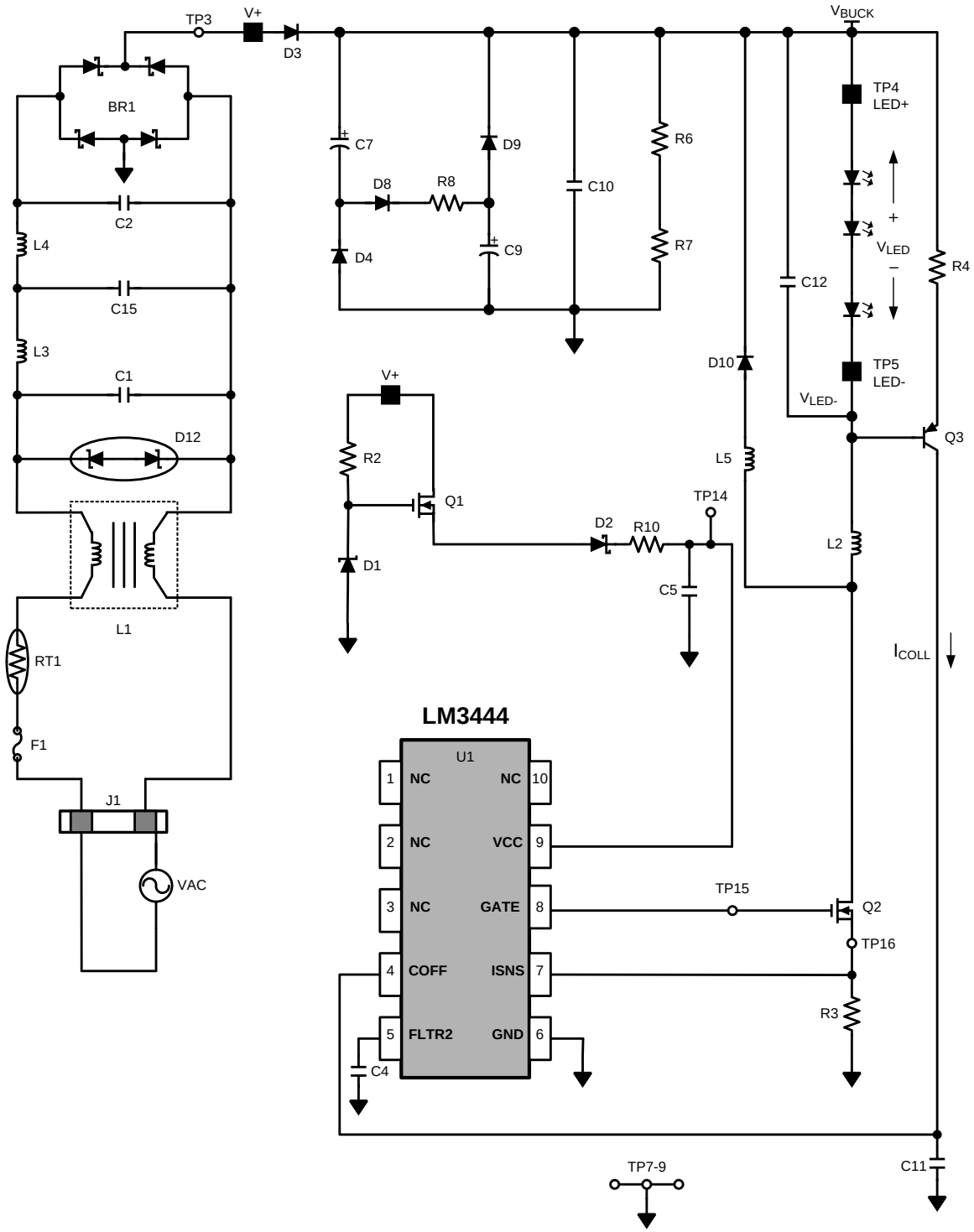


Figure 19. LM3444 Design Example 1 Input = 90 V_{AC} to 135 V_{AC} V_{LED} = 7 × HB LED String Application at 400 mA

Typical Application (continued)

8.2.1 Design Requirements

Known:

1. Input voltage range (90 V_{AC} to 135 V_{AC})
2. Number of LEDs in series = 7
3. Forward voltage drop of a single LED = 3.6 V
4. LED stack voltage = (7 × 3.6 V) = 25.2 V

Choose:

1. Nominal switching frequency, $f_{SW\text{-}TARGET}$ = 350 kHz
2. $I_{LED(AVE)}$ = 400 mA
3. Δi (usually 15% to 30% of $_{ILED(AVE)}$) = (0.30 × 400 mA) = 120 mA
4. Valley-fill stages (1, 2, or 3) = 2
5. Assumed minimum efficiency = 80%

8.2.2 Detailed Design Procedure

Calculate:

1. Calculate minimum voltage V_{BUCK}, as shown in Equation 35, which yields:

$$V_{BUCK(MIN)} = \frac{90\sqrt{2}\ \text{x SIN}(135^{o})}{2} = 45V \tag{35}$$

2. Calculate maximum voltage V_{BUCK}, as shown in Equation 36, which yields:

$$V_{BUCK(MAX)} = 135\sqrt{2} = 190V \tag{36}$$

3. Calculate t_{OFF} at V_{BUCK} nominal line voltage, as given by Equation 37.

$$t_{OFF} = \frac{\left(1 - \frac{1}{0.8} \times \frac{25.2V}{115\sqrt{2}}\right)}{(250\ \text{kHz})} = 3.23\ \mu s \tag{37}$$

4. Calculate $t_{ON(MIN)}$ at high line to ensure that $t_{ON(MIN)}$ > 200 ns, as given by Equation 38.

$$t_{ON\ (MIN)} = \frac{\left(\frac{1}{0.8} \times \frac{25.2V}{135\sqrt{2}}\right)}{\left(1 - \frac{1}{0.8} \times \frac{25.2V}{135\sqrt{2}}\right)} \times 3.23\ \mu s = 638\ ns \tag{38}$$

5. Calculate C11 and R4 in steps 6 through 9.
6. Choose current through R4 (from 50 µA to 100 µA): 70 µA as given by Equation 39.

$$R4 = \frac{V_{LED}}{I_{COLL}} = 360\ k\Omega \tag{39}$$

7. Use a standard value of 365 kΩ.
8. Calculate C11 as given by Equation 40.

$$C11 = \left(\frac{V_{LED}}{R4}\right)\left(\frac{t_{OFF}}{1.276}\right) = 175\ pF \tag{40}$$

9. Use standard value of 120 pF.
10. Calculate ripple current: 400 mA × 0.30 = 120 mA
11. Calculate inductor value at t_{OFF} = 3 µs as given by Equation 41.

Typical Application (continued)

$$L2 = \frac{25.2V\left(1 - \frac{1}{0.8} \times \frac{25.2V}{115\sqrt{2}}\right)}{(350\ kHz \times 0.1A)} = 580\ \mu H \quad (41)$$

12. Choose C10: 1 µF, 200 V
13. Calculate valley-fill capacitor values:

V_{AC} low line = 90 V_{AC}, V_{BUCK} minimum equals 60 V. Set droop for 20-V maximum at full load and low line as shown in Equation 42.

$$i = C\frac{dv}{dt} \quad (42)$$

where

- i equals P_{OUT}/V_{BUCK} (270 mA)
- dV equals 20 V
- dt equals 2.77 ms
- C_{TOTAL} equals 37 µF

Therefore, C7 = C9 = 22 µF

8.2.3 Application Curve

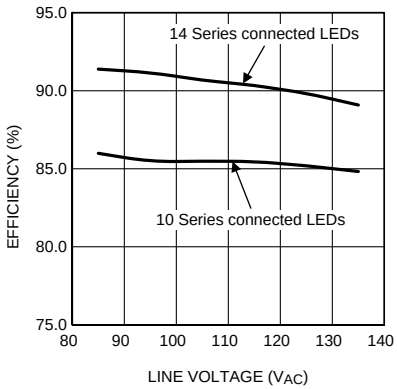


Figure 20. Efficiency vs Input Voltage

Table 1. Bill of Materials

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER
1	U1	IC, CTRLR, DRVR-LED, VSSOP	TI	LM3444MM
1	BR1	Bridge Rectifiier, SMT, 400 V, 800 mA	DiodesInc	HD04-T
1	L1	Common mode filter DIP4NS, 900 mA, 700 µH	Panasonic	ELF-11090E
1	L2	Inductor, SHLD, SMT, 1 A, 470 µH	Coilcraft	MSS1260-474-KLB
2	L3, L4	Diff mode inductor, 500 mA 1 mH	Coilcraft	MSS1260-105KL-KLB
1	L5	Bead Inductor, 160 Ω, 6 A	Steward	HI1206T161R-10
3	C1, C2, C15	Cap, Film, X2Y2, 12.5 MM, 250 V_{AC}, 20%, 10 nF	Panasonic	ECQ-U2A103ML
1	C4	Cap, X7R, 0603, 16 V, 10%, 100 nF	Murata	GRM188R71C104KA01D
2	C5, C6	Cap, X5R, 1210, 25 V, 10%, 22 µF	Murata	GRM32ER61E226KE15L
2	C7, C9	Cap, AL, 200 V, 105C, 20%, 33 µF	UCC	EKXG201ELL330MK20S
1	C10	Cap, Film, 250 V, 5%, 10 nF	Epcos	B32521C3103J
1	C12	Cap, X7R, 1206, 50 V, 10%, 1 µF	Kemet	C1206F105K5RACTU

Typical Application (continued)

Table 1. Bill of Materials (continued)

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	MANUFACTURER PART NUMBER
1	C11	Cap, C0G, 0603, 100 V, 5%, 120 pF	Murata	GRM1885C2A121JA01D
1	D1	Diode, ZNR, SOT23, 15 V, 5%	OnSemi	BZX84C15LT1G
2	D2, D13	Diode, SCH, SOD123, 40 V, 120 mA	NXP	BAS40H
4	D3, D4, D8, D9	Diode, FR, SOD123, 200 V, 1 A	Rohm	RF071M2S
1	D10	Diode, FR, SMB, 400 V, 1 A	OnSemi	MURS140T3G
1	D12	TVS, VBR = 144 V	Fairchild	SMBJ130CA
1	R2	Resistor, 1206, 1%, 100 kΩ	Panasonic	ERJ-8ENF1003V
1	R3	Resistor, 1210, 5%, 1.8Ω	Panasonic	ERJ-14RQJ1R8U
1	R4	Resistor, 0603, 1%, 576 kΩ	Panasonic	ERJ-3EKF5763V
2	R6, R7	Resistor, 0805, 1%, 1 MΩ	Rohm	MCR10EZHF1004
2	R8, R10	Resistor, 1206, 0 Ω	Yageo	RC1206JR-070RL
1	RT1	Thermistor, 120 V, 1.1 A, 50 Ω at 25°C	Thermometrics	CL-140
2	Q1, Q2	XSTR, NFET, DPAK, 300 V, 4 A	Fairchild	FQD7N30TF
1	Q3	XSTR, PNP, SOT23, 300 V, 500 mA	Fairchild	MMBTA92
1	J1	Terminal Block 2 pos	Phoenix Contact	1715721
1	F1	Fuse, 125 V, 1.25 A	bel	SSQ 1.25

9 Power Supply Recommendations

Use any AC power supply capable of the maximum application requirements for voltage and total power.

10 Layout

10.1 Layout Guidelines

Keep the low power components for FILTER and COFF close to the LM3444 with short traces. The ISNS trace should also be as short and direct as possible. Keep the high current switching paths generated by R3, Q2, L2, and D10 as short as possible to minimize generated switching noise and improve EMI.

10.2 Layout Example

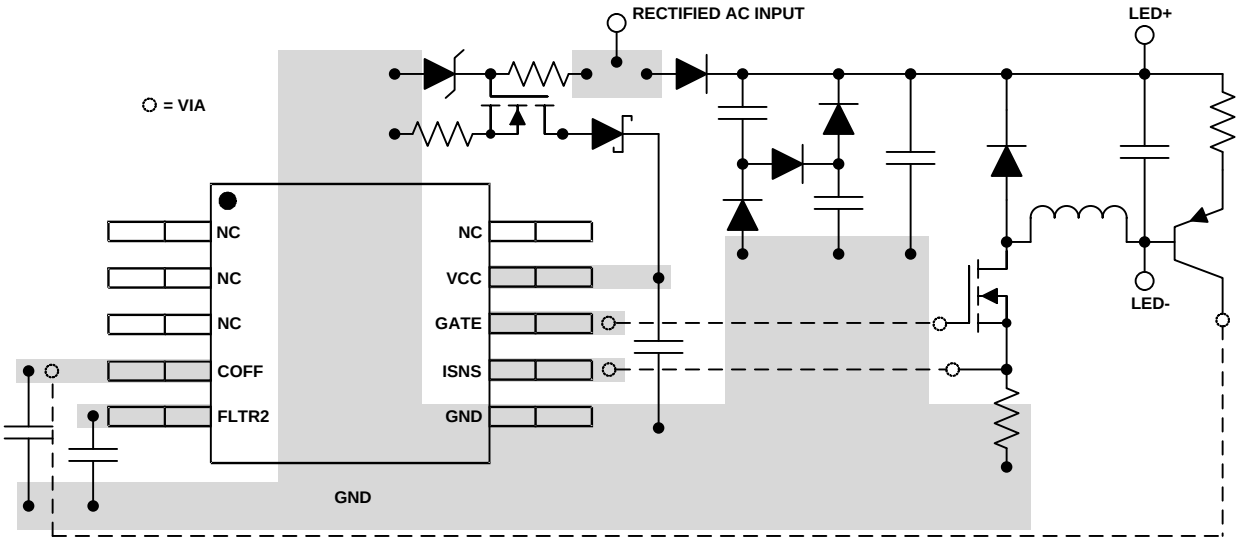


Figure 21. Layout Recommendation

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3444MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L3444 MA	Samples
LM3444MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L3444 MA	Samples
LM3444MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU NIPDAUAG | CU SN	Level-1-260C-UNLIM	-40 to 125	SZTB	Samples
LM3444MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU NIPDAUAG | CU SN	Level-1-260C-UNLIM	-40 to 125	SZTB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

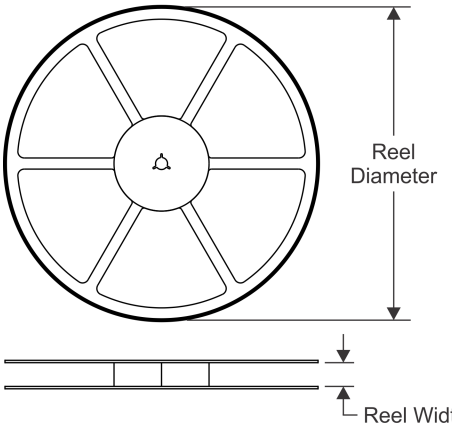
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

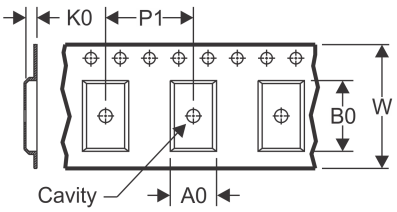
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

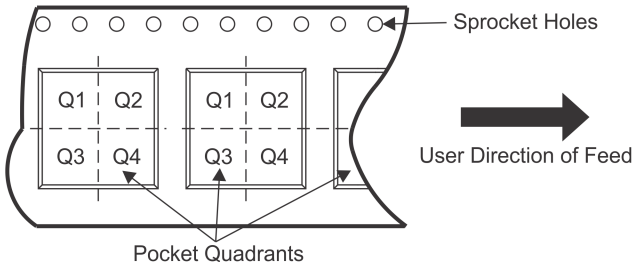


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

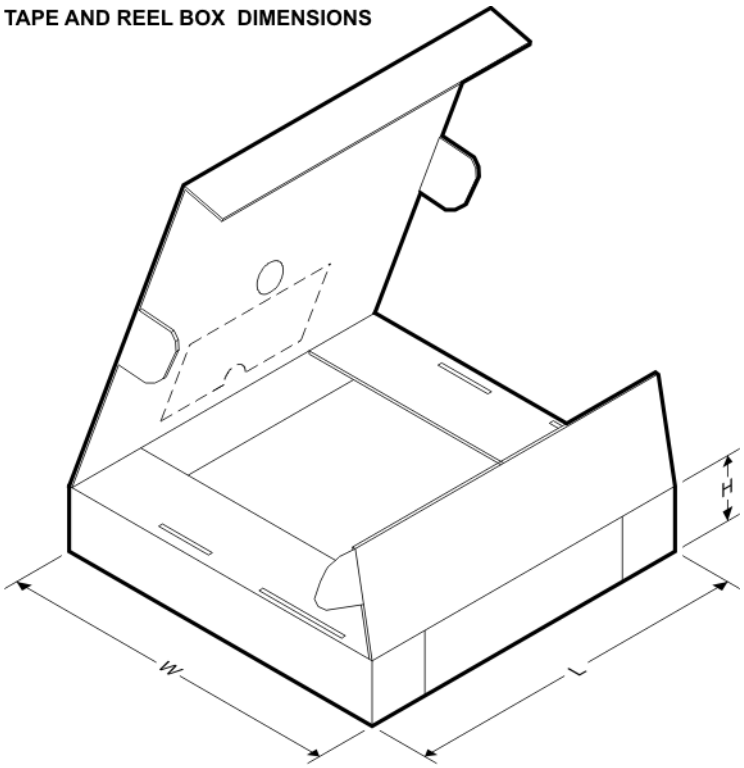
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

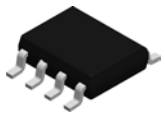
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3444MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM3444MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3444MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3444MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3444MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM3444MM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM3444MMX/NOPB	VSSOP	DGS	10	3500	364.0	364.0	27.0
LM3444MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

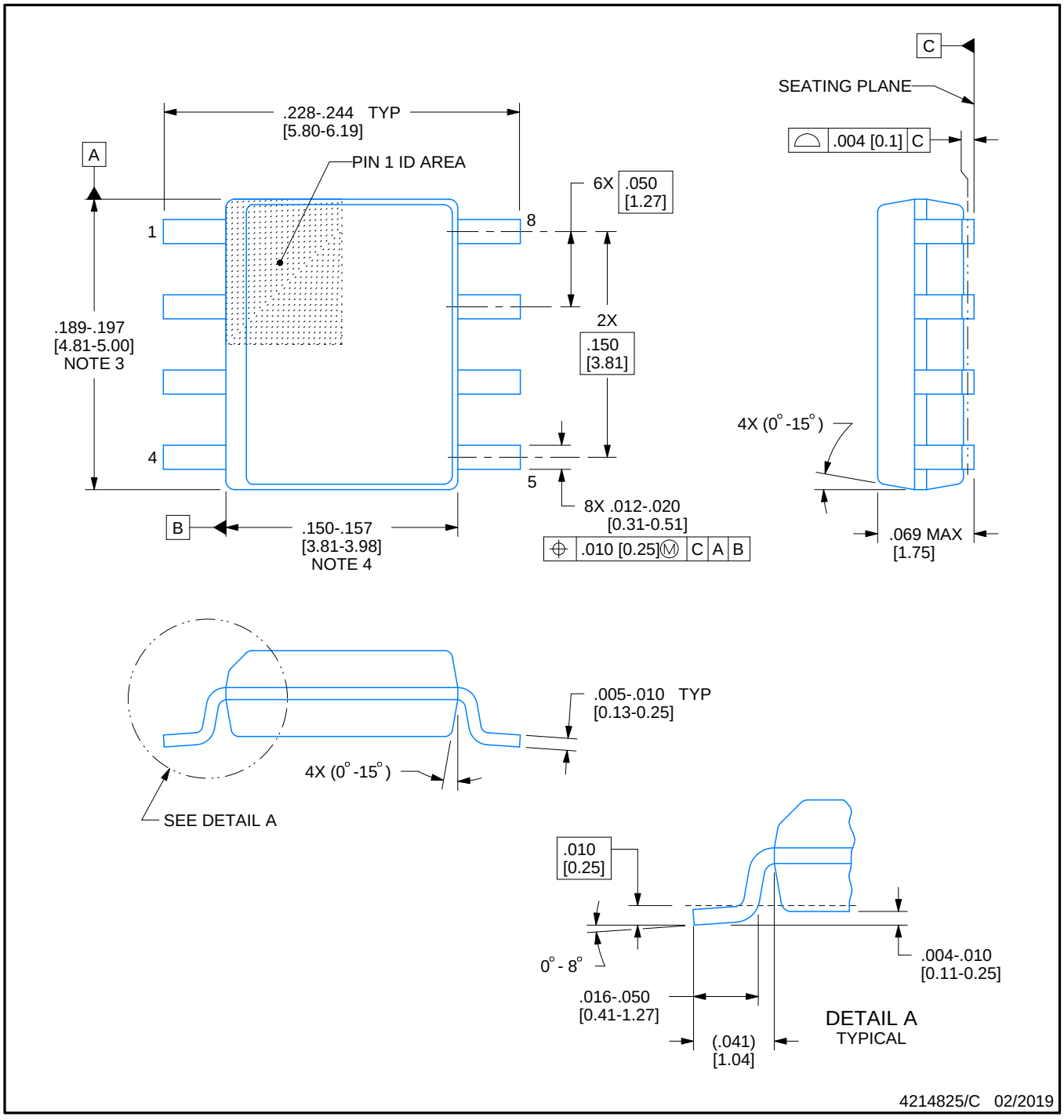


PACKAGE OUTLINE

D0008A

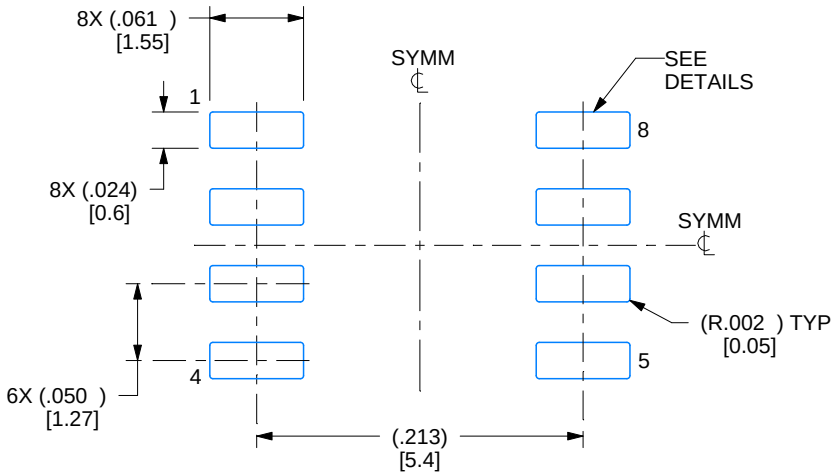
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

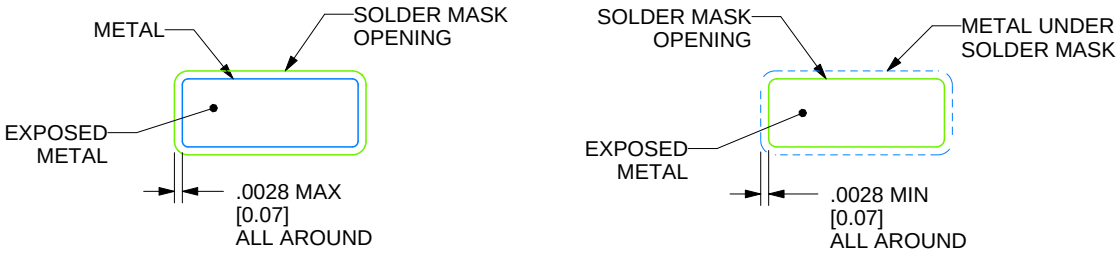


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

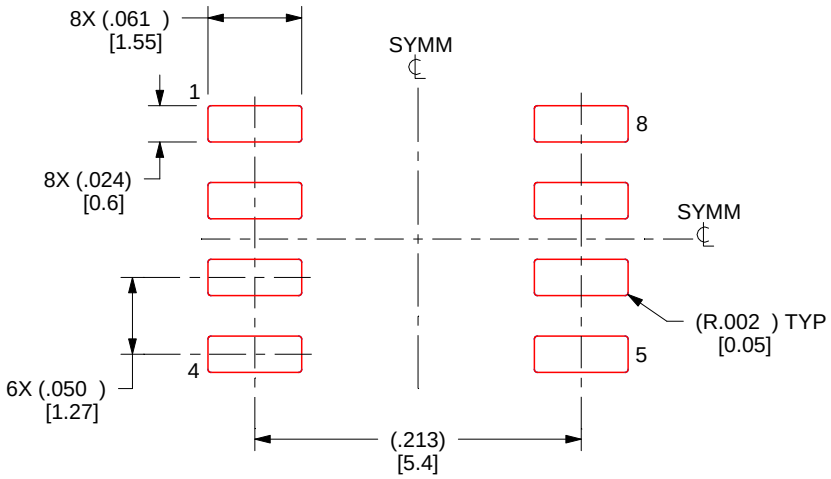
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

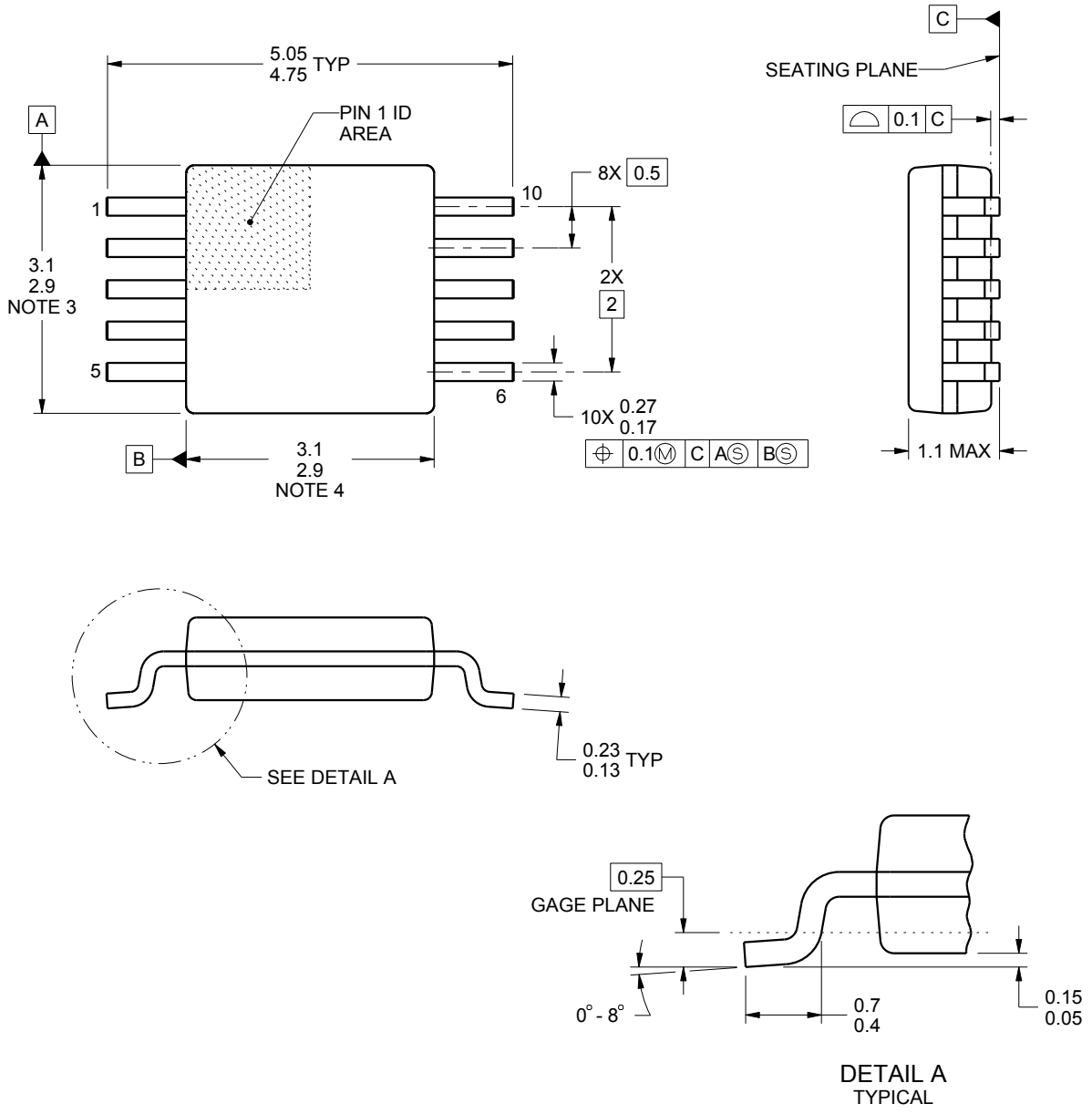
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0010A

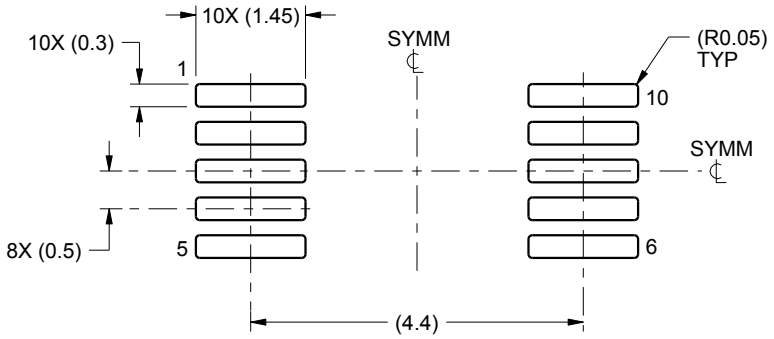
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

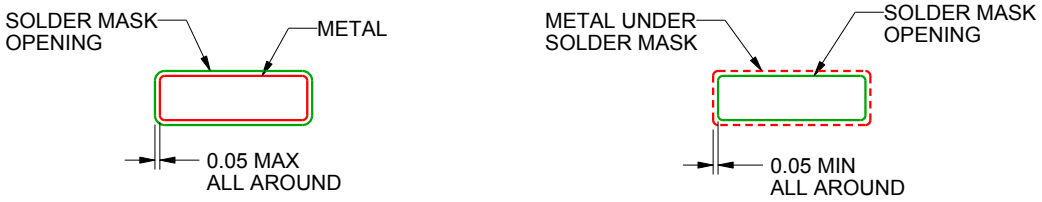


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

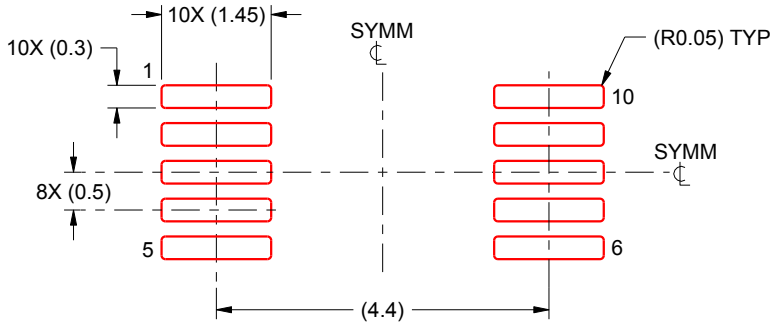


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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