# THE DATASHEET OF

# LM3424MH/NOPB

# LM3424/-Q1 Constant Current N-Channel Controller with Thermal Foldback for Driving LEDs

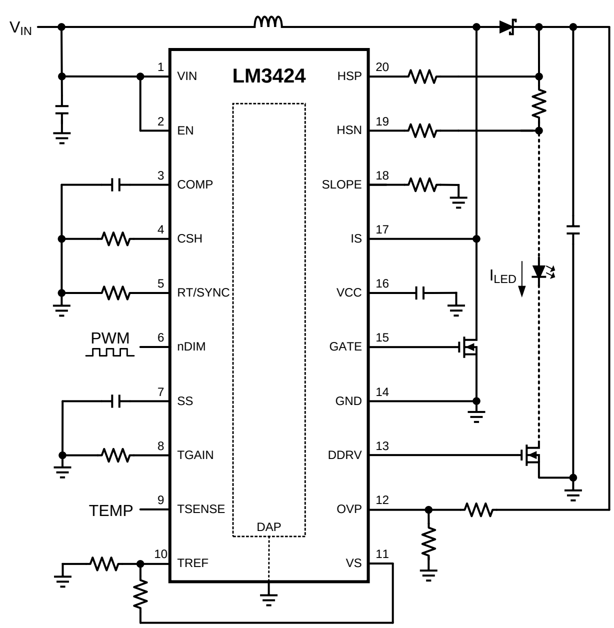
## 1 Features

- LM3424-Q1 is an Automotive Grade Product That is AEC-Q100 Grade 1 Qualified
- $V_{IN}$ Range from 4.5V to 75V
- High-Side Adjustable Current Sense
- 2-Ω, 1-A Peak MOSFET Gate Driver
- Input Undervoltage and Output Overvoltage Protection
- PWM and Analog Dimming
- Cycle-by-Cycle Current Limit
- Programmable Softstart and Slope Compensation
- Programmable, Synchronizable Switching Frequency
- Programmable Thermal Foldback
- Precision Voltage Reference
- Low Power Shutdown and Thermal Shutdown

## 2 Applications

- LED Drivers - Buck, Boost, Buck-Boost, and SEPIC
- Indoor and Outdoor Area SSL
- Automotive
- General Illumination
- Constant-Current Regulators

**Typical Boost Application Circuit**




## 3 Description

The LM3424 is a versatile high voltage N-channel MOSFET controller for LED drivers. It can be easily configured in buck, boost, buck-boost and SEPIC topologies. In addition, the LM3424 includes a thermal foldback feature for temperature management of the LEDs. This flexibility, along with an input voltage rating of 75 V, makes the LM3424 ideal for illuminating LEDs in a large family of applications.

Adjustable high-side current sense allows for tight regulation of the LED current with the highest efficiency possible. The LM3424 uses standard peak current-mode control providing inherent input voltage feed-forward compensation for better noise immunity. It is designed to provide accurate thermal foldback with a programmable foldback breakpoint and slope. In addition, a 2.45V reference is provided.

The LM3424 includes a high-voltage startup regulator that operates over a wide input range of 4.5 V to 75 V. The internal PWM controller is designed for adjustable switching frequencies of up to 2.0 MHz and external synchronization is possible. The controller is capable of high speed PWM dimming and analog dimming.

**Device Information[(1)]**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| LM3424 | HTSSOP (20) | 6.50 mm x 4.40 mm |
| LM3424-Q1 | | |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

## Table of Contents



## 4 Revision History

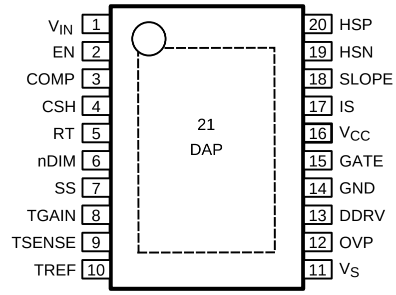
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision B (October 2009) to Revision C** **Page**

- Adjusted temperature range in Features section. ... 1
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed "Operating Temperature Range ($T_J$ = −40°C to +125°C)" to "Operating Temperature Range ($T_A$ = $T_J$ = −40°C to +125°C)" in Electrical Characterization table Condition statement ... 6

# 5 Pin Configuration and Functions

**PWP Package**
**20-Pin HTSSOP With PowerPAD™**
**Top View**




## Pin Functions

| PIN | | I/O | DESCRIPTION | |
|---|---|---|---|---|
| NO. | NAME | | | |
| 1 | $V_{IN}$ | I | Input Voltage | Bypass with 100 nF capacitor to GND as close to the device as possible. |
| 2 | EN | I | Enable | Connect to > 2.4V to enable the device or to < 0.8V for low power shutdown. |
| 3 | COMP | I | Compensation | Connect a capacitor to GND to compensate control loop. |
| 4 | CSH | I | Current Sense High | Connect a resistor to GND to set the signal current. Can also be used to analog dim as explained in the *Thermal Foldback and Analog Dimming* section. |
| 5 | RT | I | Resistor Timing | Connect a resistor to GND to set the switching frequency. Can also be used to synchronize to an external clock as explained in the *Switching Frequency* section. |
| 6 | nDIM | I | Dimming Input / Under-Voltage Protection | Connect a PWM signal for dimming as detailed in the *PWM Dimming* section and/or a resistor divider from $V_{IN}$ to program input under-voltage lockout. |
| 7 | SS | I | Soft-start | Connect a capacitor to GND to extend start-up time. |
| 8 | TGAIN | I | Temp Foldback Gain | Connect a resistor to GND to set the foldback slope. |
| 9 | TSENSE | I | Temp Sense Input | Connect a resistor/ thermistor divider from $V_S$ to sense the temperature as explained in the *Thermal Foldback and Analog Dimming* section. |
| 10 | TREF | I | Temp Foldback Reference | Connect a resistor divider from $V_S$ to set the foldback reference voltage. |
| 11 | $V_S$ | O | Voltage Reference | 2.45V reference for temperature foldback circuit and other external circuitry. |
| 12 | OVP | I | Over-Voltage Protection | Connect a resistor divider from $V_O$ to program output over-voltage lockout. |
| 13 | DDRV | O | Dimming Gate Drive Output | Connect to gate of dimming MOSFET. |
| 14 | GND | GND | Ground | Connect to DAP to provide proper system GND |
| 15 | GATE | O | Main Gate Drive Output | Connect to gate of main switching MOSFET. |
| 16 | $V_{CC}$ | O | Internal Regulator Output | Bypass with a 2.2 µF – 3.3 µF ceramic capacitor to GND. |
| 17 | IS | I | Main Switch Current Sense | Connect to the drain of the main N-channel MOSFET switch for $R_{DS-ON}$ sensing or to a sense resistor installed in the source of the same device. |
| 18 | SLOPE | I | Slope Compensation | Connect a resistor to GND to set slope of additional ramp. |
| 19 | HSN | I | LED Current Sense Negative | Connect through a series resistor to LED current sense resistor (negative). |
| 20 | HSP | I | LED Current Sense Positive | Connect through a series resistor to LED current sense resistor (positive). |
| DAP | DAP | GND | Thermal pad on bottom of IC | Connect to GND. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | $V_{IN}$, EN, nDIM | –0.3 | 76 | V |
| | OVP, HSP, HSN | –0.3 | 76 | |
| | IS | –0.3<br>–2 for 100 ns | 76 | |
| | $V_{CC}$ | –0.3 | 8 | |
| | $V_S$, TREF, TSENSE, TGAIN, COMP, CSH, RT, SLOPE, SS | –0.3 | 6 | |
| | GATE, DDRV | –0.3<br>–2.5 for 100 ns | $V_{CC}$<br>$V_{CC}$ + 2.5 for 100 ns | |
| | GND | –0.3<br>–2.5 for 100 ns | 0.3<br>2.5 for 100 ns | |
| Continuous current | $V_{IN}$, EN, nDIM | | –1 | mA |
| | OVP, HSP, HSN | | –100 | µA |
| | IS | | –1 | mA |
| | SS | –30 | 30 | µA |
| | GATE, DDRV | –1 | 1 | mA |
| Continuous power dissipation | | Internally Limited | | |
| Maximum Junction Temperature | | Internally Limited | | °C |
| Maximum lead temperature (Reflow and Solder)(3) | | | 260 | °C |
| Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Refer toTI's packaging website for more detailed information and mounting techniques. http://www.ti.com/analogpackaging

## 6.2 ESD Ratings—LM3424

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2500 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 ESD Ratings—LM3424-Q1

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2500 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1000 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.4 Recommended Operating Conditions

| | MIN | MAX | UNIT |
|---|---|---|---|
| Operating Ambient Temperature Range | –40 | 125 | °C |
| Input Voltage $V_{IN}$ | 4.5 | 75 | V |

## 6.5 Thermal Information

| THERMAL METRIC[1] | | LM3424, LM3424-Q1 PWP (HTSSOP) 20 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 36.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 21.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 18 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 17.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.6 Electrical Characteristics

MIN and MAX limits apply over the full Operating Temperature Range ($T_A = T_J = -40°C$ to 125°C) unless otherwise specified. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Unless otherwise stated the following condition applies: $T_J = 25°C$, $V_{IN} = 14$ V.

| PARAMETER | | TEST CONDITIONS | MIN(1) | TYP(2) | MAX(1) | UNIT |
|---|---|---|---|---|---|---|
| **STARTUP REGULATOR ($V_{CC}$)** | | | | | | |
| $V_{CC-REG}$ | $V_{CC}$ Regulation | $I_{CC}$ = 0 mA | 6.3 | 6.9 | 7.35 | V |
| $I_{CC-LIM}$ | $V_{CC}$ Current Limit | $V_{CC}$ = 0 V | 20 | 25 | | mA |
| $I_Q$ | Quiescent Current | EN = 3 V, Static | | 2 | 3 | mA |
| $I_{SD}$ | Shutdown Current | EN = 0 V, MAX: $T_J$ = 25°C | | 0.1 | 1 | µA |
| $V_{CC-UVLO}$ | $V_{CC}$ UVLO Threshold | $V_{CC}$ Increasing | | 4.17 | 4.50 | V |
| | | $V_{CC}$ Decreasing | 3.7 | 4.08 | | V |
| $V_{CC-HYS}$ | $V_{CC}$ UVLO Hysteresis | | | 0.1 | | V |
| **ENABLE (EN)** | | | | | | |
| $V_{EN-ST}$ | EN Startup Threshold | EN Increasing | | 1.75 | 2.4 | V |
| | | EN decreasing | 0.8 | 1.63 | | V |
| $V_{EN-HYS}$ | EN Startup Hysteresis | | | 0.1 | | V |
| $R_{EN}$ | EN Pull-down Resistance | | 0.45 | 0.82 | 1.30 | MΩ |
| **OVER-VOLTAGE PROTECTION (OVP)** | | | | | | |
| $V_{TH-OVP}$ | OVP OVLO Threshold | OVP Increasing | 1.185 | 1.24 | 1.285 | V |
| $I_{HYS-OVP}$ | OVP Hysteresis Source Current | OVP Active (high) | 13 | 20 | 27 | µA |
| **ERROR AMPLIFIER** | | | | | | |
| $V_{CSH}$ | CSH Reference Voltage | With Respect to GND | 1.21 | 1.235 | 1.26 | V |
| | Error Amplifier Input Bias Current | MIN, MAX: $T_J$ = 25°C | –0.6 | 0 | 0.6 | µA |
| | COMP Sink / Source Current | | 17 | 26 | 35 | µA |
| | Transconductance | | | 100 | | µA/V |
| | Linear Input Range | See(3) | | ±125 | | mV |
| | Transconductance Bandwidth | –6-dB Unloaded Response(3) | | 1 | | MHz |
| **OSCILLATOR (RT)** | | | | | | |
| $f_{SW}$ | Switching Frequency | $R_T$ = 36 kΩ | 164 | 207 | 250 | kHz |
| | | $R_T$ = 12 kΩ | 525 | 597 | 669 | kHz |
| $V_{RT-SYNC}$ | Sync Threshold | | | 3.5 | | V |
| **PWM COMPARATOR** | | | | | | |
| $V_{CP-BASE}$ | COMP to PWM Offset - No Slope Compensation | | 750 | 900 | 1050 | mV |
| **SLOPE COMPENSATION (SLOPE)** | | | | | | |
| $\Delta V_{CP}$ | Slope Compensation Amplitude | Additional COMP to PWM Offset - SLOPE sinking 100 µA | | 85 | | mV |
| **CURRENT LIMIT (IS)** | | | | | | |
| $V_{LIM}$ | Current Limit Threshold | | 215 | 245 | 275 | mV |
| | $V_{LIM}$ Delay to Output | | | 35 | 75 | ns |
| $t_{ON-MIN}$ | Leading Edge Blanking Time | | 140 | 240 | 340 | ns |
| **HIGH SIDE TRANSCONDUCTANCE AMPLIFIER** | | | | | | |
| | Input Bias Current | | | 10 | | µA |
| | Transconductance | | 20 | | | mA/V |
| | Input Offset Current | | –1.5 | 0 | 1.5 | µA |
| | Input Offset Voltage | | –5 | 0 | 5 | mV |

(1) All limits ensured at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) These electrical parameters are ensured by design, and are not verified by test.

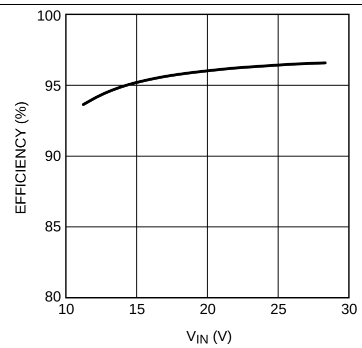
## Electrical Characteristics (continued)

MIN and MAX limits apply over the full Operating Temperature Range ($T_A = T_J = -40°C$ to 125°C) unless otherwise specified. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Unless otherwise stated the following condition applies: $T_J = 25°C$, $V_{IN} = 14$ V.

| PARAMETER | | TEST CONDITIONS | MIN[1] | TYP[2] | MAX[1] | UNIT |
|---|---|---|---|---|---|---|
| | Transconductance Bandwidth | $I_{CSH}$ = 100 µA[3] | | 500 | | kHz |
| **GATE DRIVER (GATE)** | | | | | | |
| $R_{SRC\text{-}GATE}$ | GATE Sourcing Resistance | GATE = High | | 2 | 6 | Ω |
| $R_{SNK\text{-}GATE}$ | GATE Sinking Resistance | GATE = Low | | 1.3 | 4.5 | Ω |
| **UNDERVOLTAGE LOCKOUT and DIM INPUT (nDIM)** | | | | | | |
| $V_{TH\text{-}nDIM}$ | nDIM / UVLO Threshold | | 1.185 | 1.240 | 1.285 | V |
| $I_{HYS\text{-}nDIM}$ | nDIM Hysteresis Current | | 13 | 20 | 27 | µA |
| **DIM DRIVER (DDRV)** | | | | | | |
| $R_{SRC\text{-}DDRV}$ | DDRV Sourcing Resistance | DDRV = High | | 13.5 | 30 | Ω |
| $R_{SNK\text{-}DDRV}$ | DDRV Sinking Resistance | DDRV = Low | | 3.5 | 10 | Ω |
| | nDIM rising to DDRV rising | | | 700 | | ns |
| | nDIM falling to DDRV falling | | | 360 | | ns |
| **SOFT-START (SS)** | | | | | | |
| $I_{SS}$ | Soft-start current | | | 10 | | µA |
| **THERMAL CONTROL** | | | | | | |
| $V_S$ | $V_S$ Voltage | $I_{VS}$ = 0A<br>$I_{VS}$ = 1 mA | 2.4 | 2.45 | 2.5 | V |
| | TREF input bias current | $V_{TREF}$ = 1.5 V<br>$V_{TSENSE}$ = 1.5 V | | 0.1 | | µA |
| | TSENSE Input Bias Current | $V_{TREF}$ = 1.5 V<br>$V_{TSENSE}$ = 1.5 V | | 0.1 | | µA |
| $I_{TGAIN\text{-}MAX}$ | TGAIN Maximum Sourcing Current | $V_{TGAIN}$ = 2 V | 200 | 600 | | µA |
| $I_{TF}$ | CSH Current with High-side Amplifier Disabled | $R_{TGAIN}$ = 10 kΩ; $V_{TREF}$ = 1.5 V<br>$V_{TSENSE}$ = 0.5 V | | 100 | | µA |
| | | $R_{TGAIN}$ = 10 kΩ; $V_{TREF}$ = 1.5 V<br>$V_{TSENSE}$ = 1.4 V | | 10 | | µA |
| | | $R_{TGAIN}$ = 10 kΩ; $V_{TREF}$ = 1.5 V<br>$V_{TSENSE}$ = 1.5 V | | 2 | | µA |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SD}$ | Thermal Shutdown Threshold | See[3] | | 165 | | °C |
| $T_{HYS}$ | Thermal Shutdown Hysteresis | See[3] | | 25 | | °C |

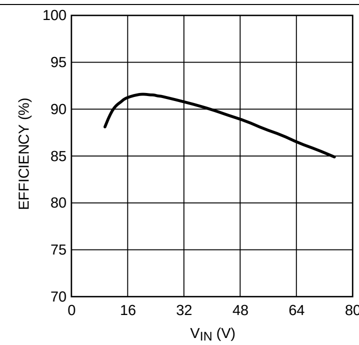
## 6.7 Typical Characteristics

$T_A$=25°C and $V_{IN}$ = 14 V unless otherwise specified. The measurements for Figure 1, Figure 3, andFigure 6 were made using the standard boost evaluation board from AN-1969 (SNVA397). The measurements for Figure 2, Figure 4, and Figure 5 were made using the standard buck-boost evaluation board from AN-1967 (SNVA398).



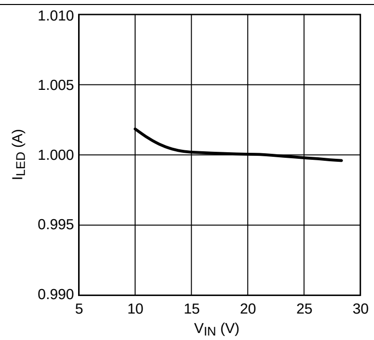

$V_O$ = 32 V (9 LEDs)

**Figure 1. Boost Efficiency vs Input Voltage**



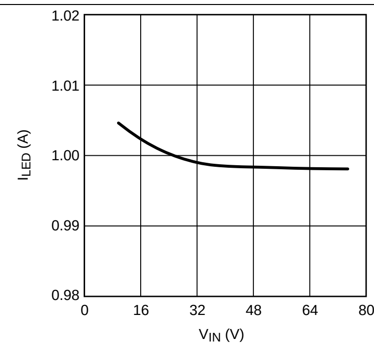

$V_O$ = 21 V (6 LEDs)

**Figure 2. Buck-Boost Efficiency vs. Input Voltage**



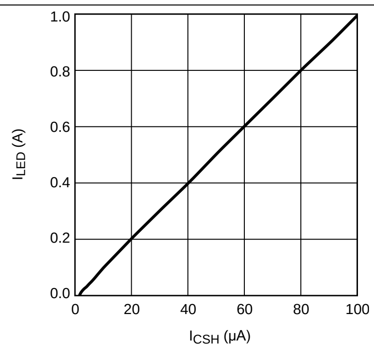

$V_O$ = 32 V (9 LEDs)

**Figure 3. Boost LED Current vs. Input Voltage**



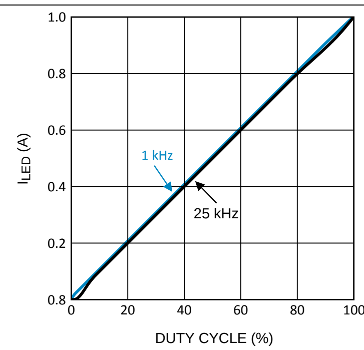

$V_O$ = 21 V (6 LEDs)

**Figure 4. Buck-Boost LED Current vs. Input Voltage**




$V_O$ = 21 V (6 LEDs) $V_{IN}$ = 24 V

**Figure 5. Analog Dimming**




$V_O$ = 32V (9 LEDs) $V_{IN}$ = 24 V

**Figure 6. PWM Dimming**

## Typical Characteristics (continued)

$T_A$=25°C and $V_{IN}$ = 14 V unless otherwise specified. The measurements for Figure 1, Figure 3, andFigure 6 were made using the standard boost evaluation board from AN-1969 (SNVA397). The measurements for Figure 2, Figure 4, and Figure 5 were made using the standard buck-boost evaluation board from AN-1967 (SNVA398).

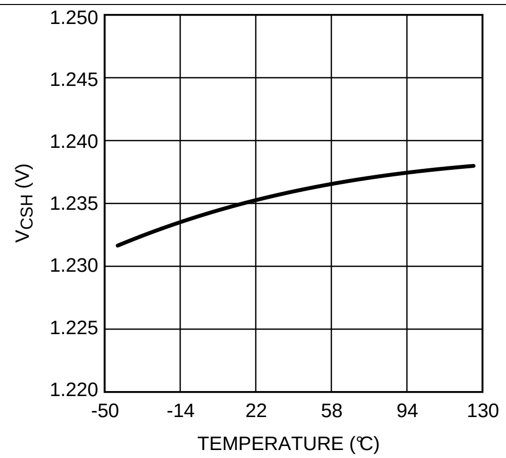



**Figure 7. $V_{CSH}$ vs. Junction Temperature**

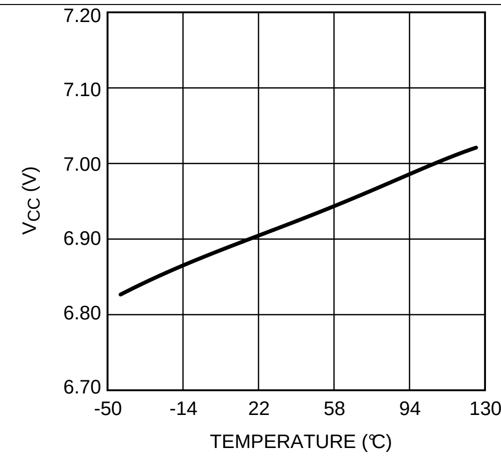



**Figure 8. $V_{CC}$ vs. Junction Temperature**

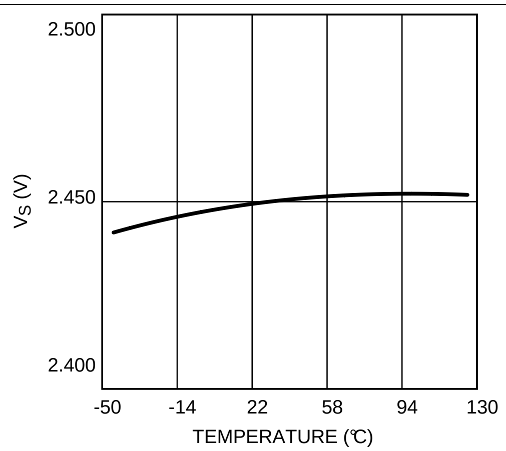



**Figure 9. $V_S$ vs. Junction Temperature**

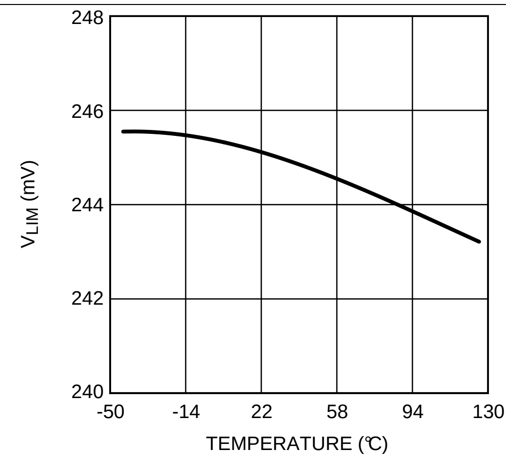



**Figure 10. $V_{LIM}$ vs. Junction Temperature**

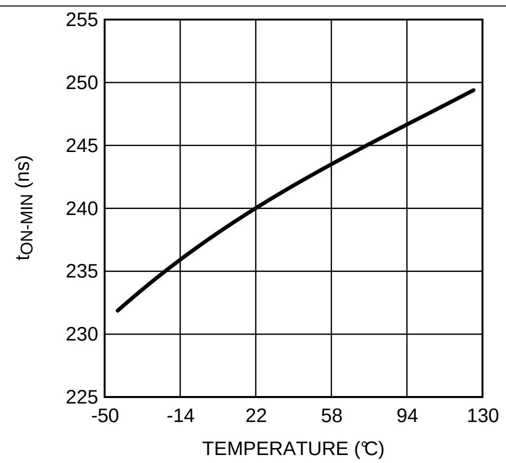



**Figure 11. Minimum On-Time vs. Junction Temperature**

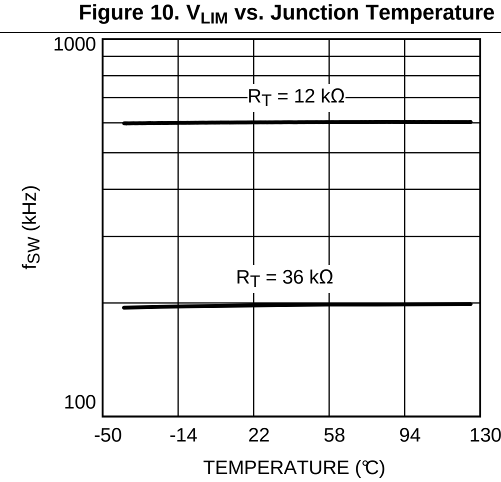



**Figure 12. Switching Frequency vs. Junction Temperature**

## Typical Characteristics (continued)

$T_A$=25°C and $V_{IN}$ = 14 V unless otherwise specified. The measurements for Figure 1, Figure 3, andFigure 6 were made using the standard boost evaluation board from AN-1969 (SNVA397). The measurements for Figure 2, Figure 4, and Figure 5 were made using the standard buck-boost evaluation board from AN-1967 (SNVA398).

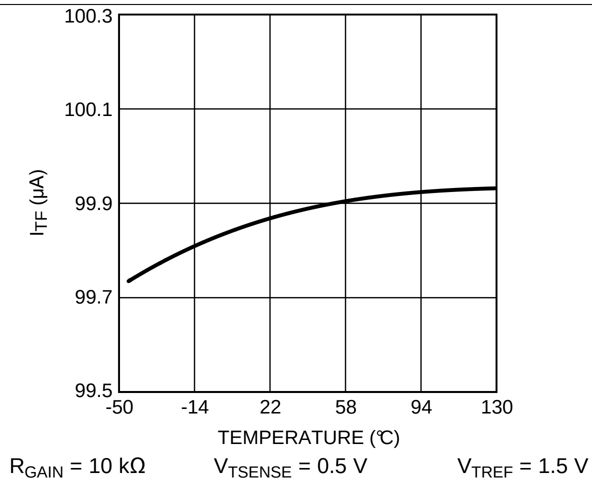



**Figure 13. $I_{TF}$ vs. Junction Temperature**

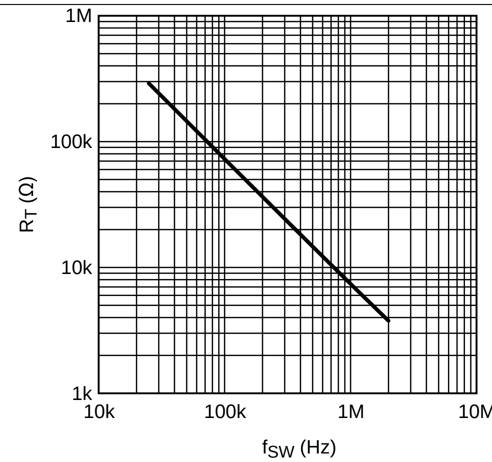



**Figure 14. Switching Frequency vs. Timing Resistance**

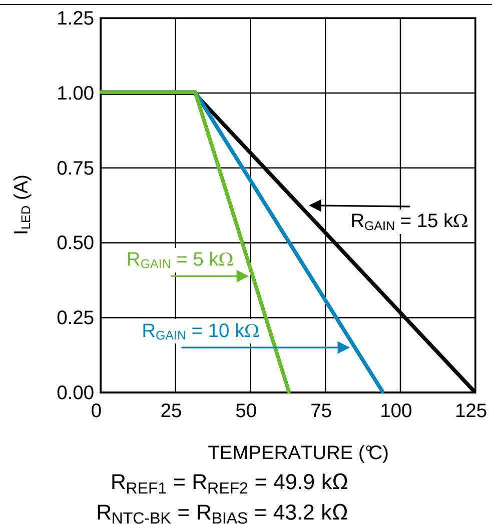



**Figure 15. Ideal Thermal Foldback with Varied Slope**

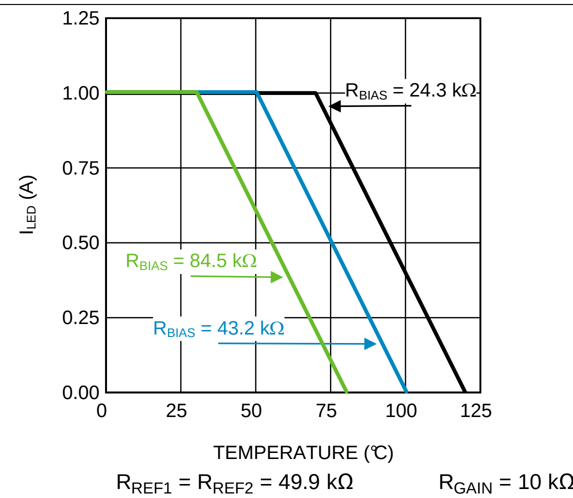


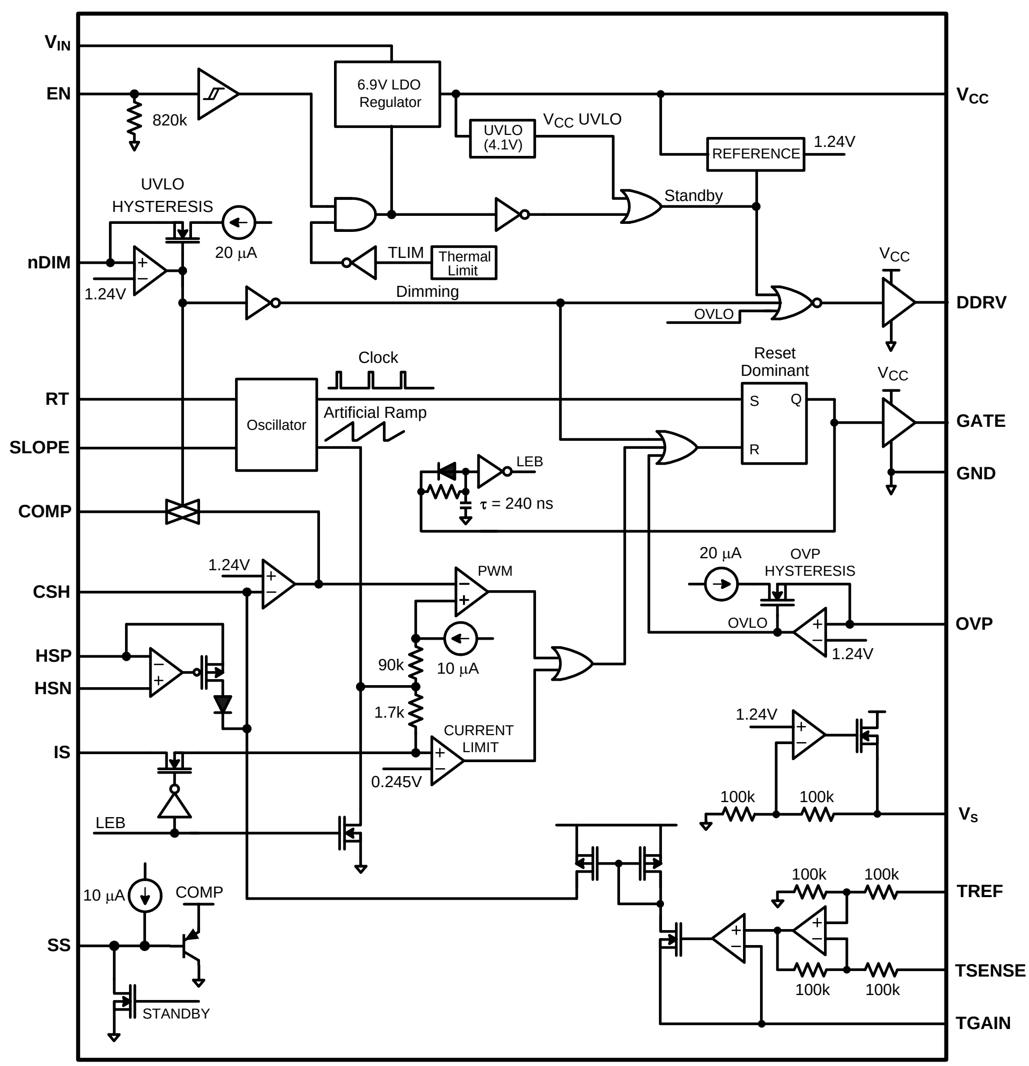

**Figure 16. Ideal Thermal Foldback with Varied Breakpoint**

# 7 Detailed Description

## 7.1 Overview

The LM3424 is an N-channel MOSFET (NFET) controller for buck, boost and buck-boost current regulators which are ideal for driving LED loads. The controller has wide input voltage range allowing for regulation of a variety of LED loads. The high-side differential current sense, with low adjustable threshold voltage, provides an excellent method for regulating output current while maintaining high system efficiency. The LM3424 uses peak current mode control providing good noise immunity and an inherent cycle-by-cycle current limit. The adjustable current sense threshold provides the capability to amplitude (analog) dim the LED current and the thermal foldback circuitry allows for precise temperature management of the LEDs. The output enable/disable function coupled with an internal dimming drive circuit provides high speed PWM dimming through the use of an external MOSFET placed at the LED load. When designing, the maximum attainable LED current is not internally limited because the LM3424 is a controller. Instead it is a function of the system operating point, component choices, and switching frequency allowing the LM3424 to easily provide constant currents up to 5A. This simple controller contains all the features necessary to implement a high efficiency versatile LED driver.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Current Regulators

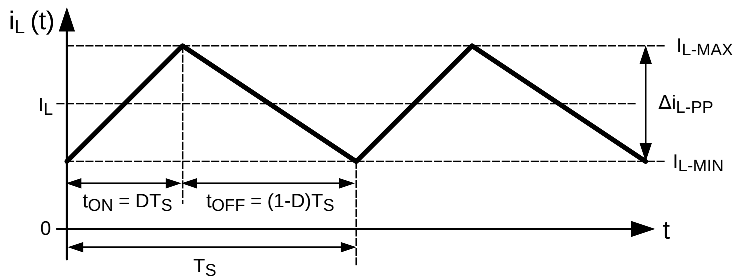



**Figure 17. Ideal CCM Regulator Inductor Current $i_L(t)$**

Current regulators can be designed to accomplish three basic functions: buck, boost, and buck-boost. All three topologies in their most basic form contain a main switching MOSFET, a recirculating diode, an inductor and capacitors. The LM3424 is designed to drive a ground referenced NFET which is perfect for a standard boost regulator. Buck and buck-boost regulators, on the other hand, usually have a high-side switch. When driving an LED load, a ground referenced load is often not necessary, therefore a ground referenced switch can be used to drive a floating load instead. The LM3424 can then be used to drive all three basic topologies as shown in the *Basic Topology Schematics* section. Other topologies such as the SEPIC and flyback converter (both derivatives of the buck-boost) can be implemented as well.

Looking at the buck-boost design, the basic operation of a current regulator can be analyzed. During the time that the NFET (Q1) is turned on ($t_{ON}$), the input voltage source stores energy in the inductor (L1) while the output capacitor ($C_O$) provides energy to the LED load. When Q1 is turned off ($t_{OFF}$), the re-circulating diode (D1) becomes forward biased and L1 provides energy to both $C_O$ and the LED load. Figure 17 shows the inductor current ($i_L(t)$) waveform for a regulator operating in CCM.

The average output LED current ($I_{LED}$) is proportional to the average inductor current ($I_L$) , therefore if $I_L$ is tightly controlled, $I_{LED}$ will be well regulated. As the system changes input voltage or output voltage, the ideal duty cycle (D) is varied to regulate $I_L$ and ultimately $I_{LED}$. For any current regulator, D is a function of the conversion ratio:

Buck

$$D = \frac{V_O}{V_{IN}} \tag{1}$$

Boost

$$D = \frac{V_O - V_{IN}}{V_O} \tag{2}$$

Buck-Boost

$$D = \frac{V_O}{V_O + V_{IN}} \tag{3}$$

### 7.3.2 Peak Current Mode Control

Peak current mode control is used by the LM3424 to regulate the average LED current through an array of HBLEDs. This method of control uses a series resistor in the LED path to sense LED current and can use either a series resistor in the MOSFET path or the MOSFET $R_{DS-ON}$ for both cycle-by-cycle current limit and input voltage feed forward. The controller has a fixed switching frequency set by an internal programmable oscillator which means current mode instability can occur at duty cycles higher than 50%. To mitigate this standard problem, an artificial ramp is added to the control signal internally. The slope of this ramp is programmable to allow for a wider range of component choices for a given design. A detailed explanation of this control method is presented in the following sections.

## Feature Description (continued)

### 7.3.3 Average LED Current

To first understand how the LM3424 regulates LED current, the thermal foldback functionality will be ignored. Figure 18 shows the physical implementation of the LED current sense circuitry assuming the thermal foldback circuitry is a simple current source which, for now, will be set to zero ($I_{TF}$ = 0A). The LM3424 uses an external current sense resistor ($R_{SNS}$) placed in series with the LED load to convert the LED current ($I_{LED}$) into a voltage ($V_{SNS}$). The HSP and HSN pins are the inputs to the high-side sense amplifier which are forced to be equal potential ($V_{HSP}$=$V_{HSN}$) through negative feedback. Because of this, the $V_{SNS}$ voltage is forced across $R_{HSP}$ which generates a current that is summed with the thermal foldback current ($I_{TF}$) to generate the signal current ($I_{CSH}$) which flows out of the CSH pin and through the $R_{CSH}$ resistor. The error amplifier will regulate the CSH pin to 1.24V and assuming $I_{TF}$ = 0A, $I_{CSH}$ can be calculated:

$$I_{CSH} = \frac{V_{SNS}}{R_{HSP}} \tag{4}$$

This means $V_{SNS}$ will be regulated as follows:

$$V_{SNS} = 1.24V \times \frac{R_{HSP}}{R_{CSH}} \tag{5}$$

$I_{LED}$ can then be calculated:

$$I_{LED} = \frac{V_{SNS}}{R_{SNS}} = \frac{1.24V}{R_{SNS}} \times \frac{R_{HSP}}{R_{CSH}} \tag{6}$$

The selection of the three resistors ($R_{SNS}$, $R_{CSH}$, and $R_{HSP}$) is not arbitrary. For matching and noise performance, the suggested signal current $I_{CSH}$ is approximately 100 µA. This current does not flow in the LEDs and will not affect either the off-state LED current or the regulated LED current. $I_{CSH}$ can be above or below this value, but the high-side amplifier offset characteristics may be affected slightly. In addition, to minimize the effect of the high-side amplifier voltage offset on LED current accuracy, the minimum $V_{SNS}$ is suggested to be 50 mV. Finally, a resistor ($R_{HSN}$ = $R_{HSP}$) should be placed in series with the HSN pin to cancel out the effects of the input bias current (~10 µA) of both inputs of the high-side sense amplifier.

Note that he CSH pin can also be used as a low-side current sense input regulated to 1.24V. The high-side sense amplifier is disabled if HSP and HSN are tied to GND.

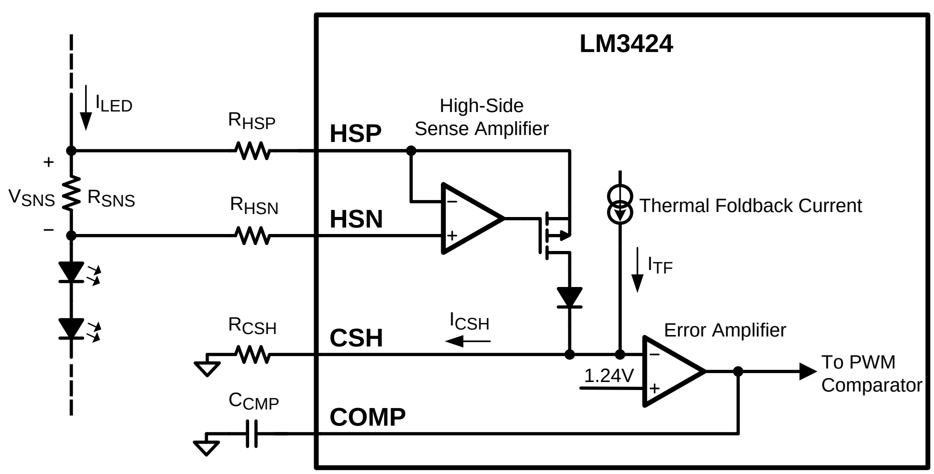



**Figure 18. LED Current Sense Circuitry**

### 7.3.4 Thermal Foldback and Analog Dimming

Thermal foldback is necessary in many applications due to the extreme temperatures created in LED environments. In general, two functions are necessary: a temperature breakpoint ($T_{BK}$) after which the nominal operating current needs to be reduced, and a slope corresponding to the amount of LED current decrease per temperature increase as shown in Figure 19. The LM3424 allows the user to program both the breakpoint and slope of the thermal foldback profile.

## Feature Description (continued)

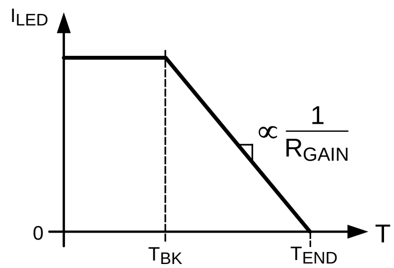



**Figure 19. Ideal Thermal Foldback Profile**

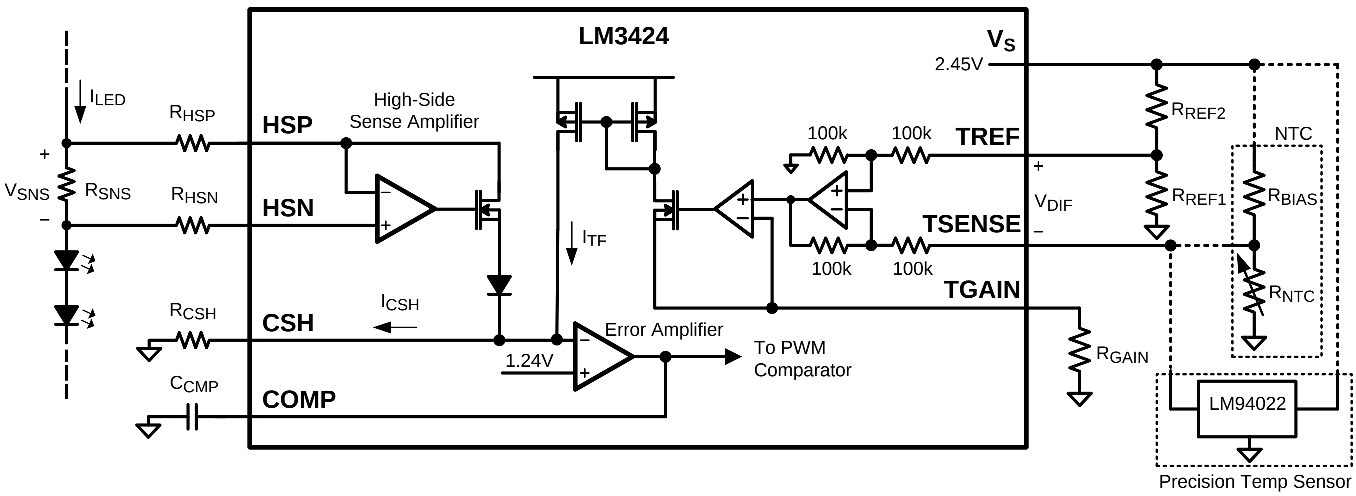



**Figure 20. Thermal Foldback Circuitry**

Foldback is accomplished by adding current ($I_{TF}$) to the CSH summing node. As more current is added, less current is needed from the high side amplifier and correspondingly, the LED current is regulated to a lower value. The final temperature ($T_{END}$) is reached when $I_{TF}$ = $I_{CSH}$ causing no current to be needed from the high-side amplifier, yielding $I_{LED}$ = 0A.

Figure 20 shows how the thermal foldback circuitry is physically implemented in the system. $I_{TF}$ is set by placing a differential voltage ($V_{DIF} = V_{TREF} – V_{TSENSE}$) across TSENSE and TREF. $V_{TREF}$ can be set with a simple resistor divider ($R_{REF1}$ and $R_{REF2}$) supplied from the $V_S$ voltage reference (typical 2.45V). $V_{TSENSE}$ is set with a temperature dependant voltage (as temperature increases, voltage should decrease).

An NTC thermistor is the most cost effective device used to sense temperature. As the temperature of the thermistor increases, its resistance decreases (albeit non-linearly). Usually, the NTC manufacturer's datasheet will detail the resistance-temperature characteristic of the thermistor. The thermistor will have a different resistance ($R_{NTC}$) at each temperature. The nominal resistance of an NTC is the resistance when the temperature is 25°C ($R_{25}$) and in many datasheets this will be given a multiplier of 1. Then the resistance at a higher temperature will have a multiplier less than 1 (that is, $R_{85}$ multiplier is 0.161 therefore $R_{85}$ = 0.161 x $R_{25}$). Given a desired $T_{BK}$ and $T_{END}$, the corresponding resistances at those temperatures ($R_{NTC-BK}$ and $R_{NTC-END}$) can be found.

Using the NTC method, a resistor divider from $V_S$ can be implemented with a resistor connected between $V_S$ and TSENSE and the NTC thermistor placed at the desired location and connected from TSENSE to GND. This will ensure that the desired temperature-voltage characteristic occurs at TSENSE.

If a linear decrease over the foldback range is necessary, a precision temperature sensor such as the LM94022 can be used instead as shown in Figure 20. Either method can be used to set $V_{TSENSE}$ according to the temperature. However, for the rest of this datasheet, the NTC method will be used for thermal foldback calculations.

## Feature Description (continued)

During operation, if $V_{DIF}$ < 0V, then the sensed temperature is less than $T_{BK}$ and the differential sense amplifier will regulate its output to zero forcing $I_{TF}$ = 0. This maintains the nominal LED current and no foldback is observed.

At $T_{BK}$, $V_{DIF}$ = 0V exactly and $I_{TF}$ is still zero. Looking at the manufacturer's datasheet for the NTC thermistor, $R_{NTC-BK}$ can be obtained for the desired $T_{BK}$ and the voltage relationship at the breakpoint ($V_{TSENSE-BK} = V_{TREF}$) can be defined:

$$\frac{R_{REF1}}{R_{REF1} + R_{REF2}} = \frac{R_{NTC-BK}}{R_{NTC-BK} + R_{BIAS}} \quad (7)$$

A general rule of thumb is to set $R_{REF1} = R_{REF2}$ simplifying the breakpoint relationship to $R_{BIAS} = R_{NTC-BK}$.

If $V_{DIF}$ > 0V (temperature is above $T_{BK}$), then the amplifier will regulate its output equal to the input forcing $V_{DIF}$ across the resistor ($R_{GAIN}$) connected from TGAIN to GND. $R_{GAIN}$ ultimately sets the slope of the LED current decrease with respect to increasing temperature by changing $I_{TF}$:

$$I_{TF} = \frac{V_{TREF} - V_{TSENSE}}{R_{GAIN}} \quad (8)$$

If an analog temperature sensor such as the LM94022 is used, then $R_{BIAS}$ and the NTC are not necessary and $V_{TSENSE}$ will be the direct voltage output of the sensor.

Since the NTC is not usually local to the controller, a bypass capacitor ($C_{NTC}$) is suggested from TSENSE to GND. If a capacitor is used at TSENSE, then a capacitor ($C_{REF}$) of equal or greater value should be placed from TREF to GND in order to ensure the controller does not start-up in foldback. Alternatively, a smaller $C_{REF}$ can be used to create a fade-up function at start-up (see *Application Information*).

Thermal foldback is simply analog dimming according to a specific profile, therefore any method of controlling the differential voltage between TREF and TSENSE can be use to analog dim the LED current. The corresponding LED current for any $V_{DIF}$ > 0V is defined:

$$I_{LED} = (I_{CSH} - I_{TF}) \times \left(\frac{R_{HSP}}{R_{SNS}}\right) \quad (9)$$

The CSH pin can also be used to analog dim the LED current by adjusting the current sense voltage ($V_{SNS}$), similar to thermal foldback. There are several different methods to adjust $V_{SNS}$ using the CSH pin:

1. External variable resistance: Adjust a potentiometer placed in series with $R_{CSH}$ to vary $V_{SNS}$.
2. External variable current source: Source current (0 µA to $I_{CSH}$) into the CSH pin to adjust $V_{SNS}$.

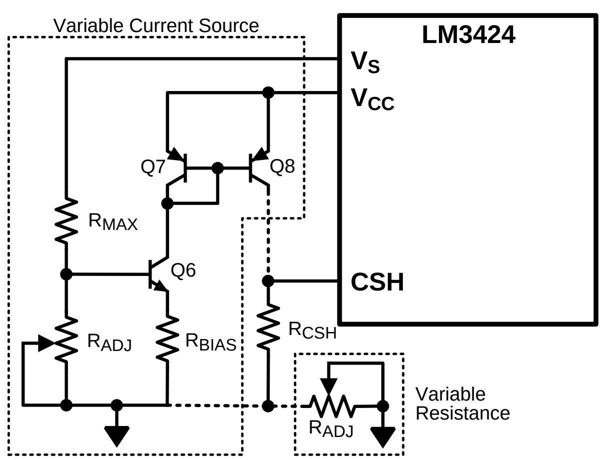



**Figure 21. Analog Dimming Circuitry**

## Feature Description (continued)

In general, analog dimming applications require a lower switching frequency to minimize the effect of the leading edge blanking circuit. As the LED current is reduced, the output voltage and the duty cycle decreases. Eventually, the minimum on-time is reached. The lower the switching frequency, the wider the linear dimming range. Figure 21 shows how both CSH methods are physically implemented.

Method 1 uses an external potentiometer in the CSH path which is a simple addition to the existing circuitry. However, the LEDs cannot dim completely because there is always some resistance causing signal current to flow. This method is also susceptible to noise coupling at the CSH pin since the potentiometer increases the size of the signal current loop.

Method 2 provides a complete dimming range and better noise performance, though it is more complex. Like thermal foldback, it simply sources current into the CSH pin, decreasing the amount of signal current that is necessary. This method consists of a PNP current mirror and a bias network consisting of an NPN, 2 resistors and a potentiometer ($R_{ADJ}$), where $R_{ADJ}$ controls the amount of current sourced into the CSH pin. A higher resistance value will source more current into the CSH pin causing less regulated signal current through $R_{HSP}$, effectively dimming the LEDs. Q7 and Q8 should be a dual pair PNP for best matching and performance. The additional current ($I_{ADD}$) sourced into the CSH pin can be calculated:

$$I_{ADD} = \frac{\left(\frac{R_{ADJ} \times V_{REF}}{R_{ADJ} + R_{MAX}}\right) - V_{BE\text{-}Q6}}{R_{BIAS}} \quad (10)$$

The corresponding $I_{LED}$ for a specific $I_{ADD}$ is:

$$I_{LED} = (I_{CSH} - I_{ADD}) \times \left(\frac{R_{HSP}}{R_{SNS}}\right) \quad (11)$$

### 7.3.5 Current Sense and Current Limit

The LM3424 achieves peak current mode control using a comparator that monitors the main MOSFET (Q1) transistor current, comparing it with the COMP pin voltage as shown in Figure 22. Further, it incorporates a cycle-by-cycle over-current protection function. Current limit is accomplished by a redundant internal current sense comparator. If the voltage at the current sense comparator input (IS) exceeds 245 mV (typical), the on cycle is immediately terminated. The IS input pin has an internal N-channel MOSFET which pulls it down at the conclusion of every cycle. The discharge device remains on an additional 240 ns (typical) after the beginning of a new cycle to blank the leading edge spike on the current sense signal. The leading edge blanking (LEB) determines the minimum achievable on-time ($t_{ON\text{-}MIN}$).

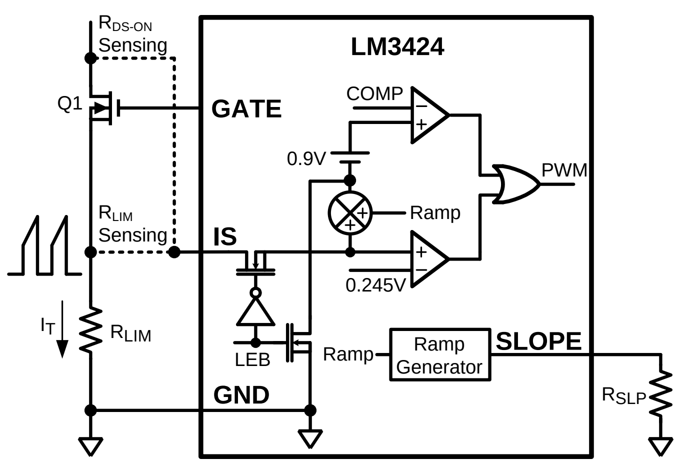



**Figure 22. Current Sense / Current Limit Circuitry**

## Feature Description (continued)

There are two possible methods to sense the transistor current. The $R_{DS\text{-}ON}$ of the main power MOSFET can be used as the current sense resistance because the IS pin was designed to withstand the high voltages present on the drain when the MOSFET is in the off state. Alternatively, a sense resistor located in the source of the MOSFET may be used for current sensing, however a low inductance (ESL) type is suggested. The cycle-by-cycle current limit ($I_{LIM}$) can be calculated using either method as the limiting resistance ($R_{LIM}$):

$$I_{LIM} = \frac{245\ \text{mV}}{R_{LIM}} \tag{12}$$

In general, the external series resistor allows for more design flexibility, however it is important to ensure all of the noise sensitive low power ground connections are connected together local to the controller and a single connection is made to GND.

### 7.3.6 Slope Compensation

The LM3424 has programmable slope compensation in order to provide stability over a wide range of operating conditions. Without slope compensation, a well-known condition called current mode instability (or sub-harmonic oscillation) can result if there is a perturbation of the MOSFET current sense voltage at the IS pin, due to noise or a some type of transient.

Through a mathematical / geometrical analysis of the inductor current ($I_L$) and the corresponding control current ($I_C$, it can be shown that if D < 0.5, the effect of the perturbation will decrease each switching cycle and the system will remain stable. However, if D > 0.5 then the perturbation will grow as shown in Figure 23, eventually causing a "period doubling" effect where the effect of the perturbation remains, yielding current mode instability.

Looking at Figure 22, the positive PWM comparator input is the IS voltage, a mirror of $I_L$ during $t_{ON}$, plus a typical 900 mV offset. The negative input of the PWM comparator is the COMP pin which is proportional to $I_C$, the threshold at which the main MOSFET (Q1) is turned off.

The LM3424 mitigates current mode instability by implementing an aritifical ramp (commonly called slope compensation) which is summed with the sensed MOSFET current at the IS pin as shown in Figure 22. This combined signal is compared to the COMP pin to generate the PWM signal. An increase in the ramp that is added to the sense voltage will increase the maximum achievable duty cycle. It should be noted that as the artificial ramp is increased more and more, the control method approaches standard voltage mode control and the benefits of current mode control are reduced.

To program the slope compensation, an external resistor, $R_{SLP}$, is connected from SLOPE to GND. This sets the slope of the artificial ramp that is added to the MOSFET current sense voltage. A smaller $R_{SLP}$ value will increase the slope of the added ramp. A simple calculation is suggested to ensure any duty cycle is attainable while preventing the addition of excessive ramp. This method requires the artifical ramp slope ($M_A$) to be equal to half the inductor slope during $t_{OFF}$:

$$M_A = \frac{7.5 \times 10^{12}}{R_T \times R_{SLP} \times R_{LIM}} = \frac{V_O}{2 \times L1} \tag{13}$$

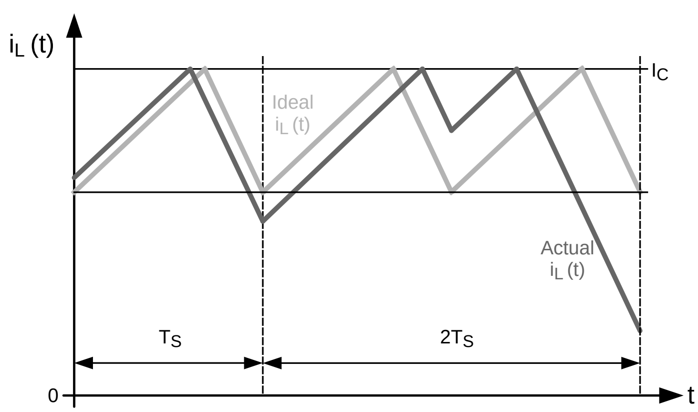



**Figure 23. "Period Doubling" due to Current Mode Instability**

## Feature Description (continued)

### 7.3.7 Control Loop Compensation

The LM3424 control loop is modeled like any current mode controller. Using a first order approximation, the uncompensated loop can be modeled as a single pole created by the output capacitor and, in the boost and buck-boost topologies, a right half plane zero created by the inductor, where both have a dependence on the LED string dynamic resistance. There is also a high frequency pole in the model, however it is near the switching frequency and plays no part in the compensation design process therefore it will be neglected. Since ceramic capacitance is recommended for use with LED drivers due to long lifetimes and high ripple current rating, the ESR of the output capacitor can also be neglected in the loop analysis. Finally, there is a DC gain of the uncompensated loop which is dependent on internal controller gains and the external sensing network.

A buck-boost regulator will be used as an example case. See the *Application Information* section for compensation of all topologies.

The uncompensated loop gain for a buck-boost regulator is given by the following equation:

$$T_U = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)} \tag{14}$$

Where the uncompensated DC loop gain of the system is described as:

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{(1+D) \times R_{HSP} \times R_{LIM}} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} \tag{15}$$

And the output pole ($\omega_{P1}$) is approximated:

$$\omega_{P1} = \frac{1+D}{r_D \times C_O} \tag{16}$$

And the right half plane zero ($\omega_{Z1}$) is:

$$\omega_{Z1} = \frac{r_D \times D'^2}{D \times L1} \tag{17}$$

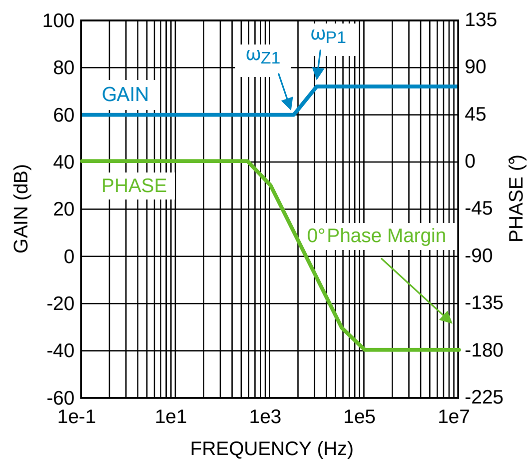



**Figure 24. Uncompensated Loop Gain Frequency Response**

## Feature Description (continued)

Figure 24 shows the uncompensated loop gain in a worst-case scenario when the RHP zero is below the output pole. This occurs at high duty cycles when the regulator is trying to boost the output voltage significantly. The RHP zero adds 20dB/decade of gain while loosing 45°/decade of phase which places the crossover frequency (when the gain is zero dB) extremely high because the gain only starts falling again due to the high frequency pole (not modeled or shown in figure). The phase will be below -180° at the crossover frequency which means there is no phase margin (180° + phase at crossover frequency) causing system instability. Even if the output pole is below the RHP zero, the phase will still reach -180° before the crossover frequency in most cases yielding instability.

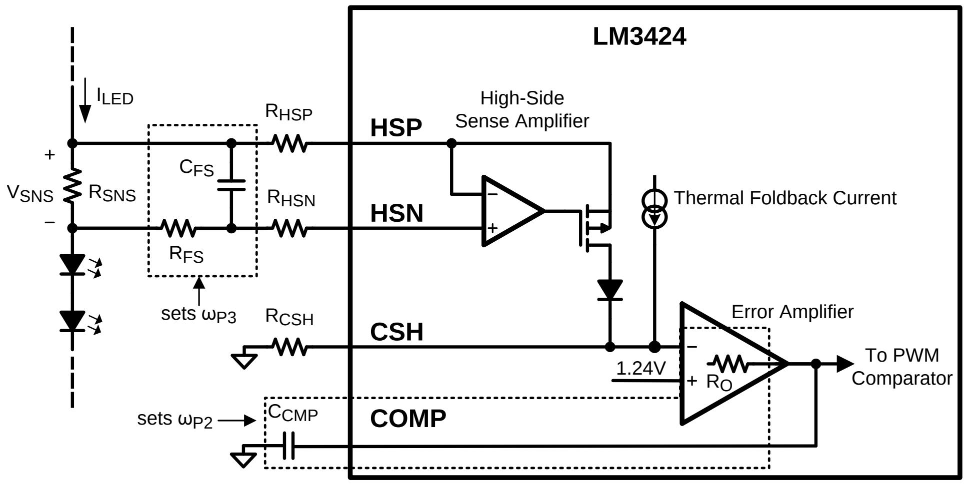



**Figure 25. Compensation Circuitry**

To mitigate this problem, a compensator should be designed to give adequate phase margin (above 45°) at the crossover frequency. A simple compensator using a single capacitor at the COMP pin ($C_{CMP}$) will add a dominant pole to the system, which will ensure adequate phase margin if placed low enough. At high duty cycles (as shown in Figure 24), the RHP zero places extreme limits on the achievable bandwidth with this type of compensation. However, because an LED driver is essentially free of output transients (except catastrophic failures open or short), the dominant pole approach, even with reduced bandwidth, is usually the best approach. The dominant compensation pole ($\omega_{P2}$) is determined by $C_{CMP}$ and the output resistance ($R_O$) of the error amplifier (typically 5 MΩ):

$$\omega_{P2} = \frac{1}{5 \times 10^6 \Omega \times C_{CMP}} \tag{18}$$

It may also be necessary to add one final pole at least one decade above the crossover frequency to attenuate switching noise and, in some cases, provide better gain margin. This pole can be placed across $R_{SNS}$ to filter the ESL of the sense resistor at the same time. Figure 25 shows how the compensation is physically implemented in the system.

The high frequency pole ($\omega_{P3}$) can be calculated:

$$\omega_{P3} = \frac{1}{R_{FS} \times C_{FS}} \tag{19}$$

The total system transfer function becomes:

$$T = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right) \times \left(1 + \frac{s}{\omega_{P2}}\right) \times \left(1 + \frac{s}{\omega_{P3}}\right)} \tag{20}$$

The resulting compensated loop gain frequency response shown in Figure 26 indicates that the system has adequate phase margin (above 45°) if the dominant compensation pole is placed low enough, ensuring stability:

## Feature Description (continued)

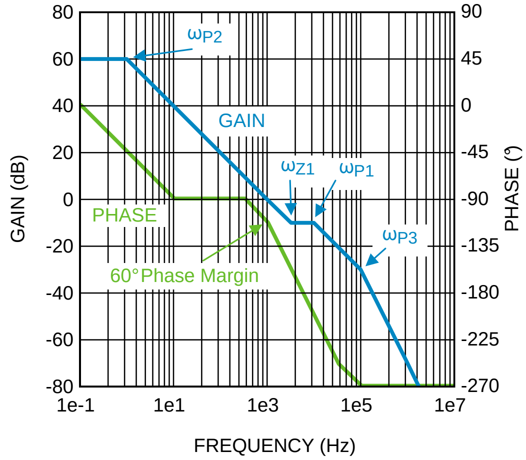



**Figure 26. Compensated Loop Gain Frequency Response**

### 7.3.8 Start-Up Regulator and Soft-Start

The LM3424 includes a high voltage, low dropout bias regulator. When power is applied, the regulator is enabled and sources current into an external capacitor ($C_{BYP}$) connected to the $V_{CC}$ pin. The recommended bypass capacitance for the $V_{CC}$ regulator is 2.2 µF to 3.3 µF. The output of the $V_{CC}$ regulator is monitored by an internal UVLO circuit that protects the device from attempting to operate with insufficient supply voltage and the supply is also internally current limited.

The LM3424 also has programmable soft-start, set by an external capacitor ($C_{SS}$), connected from SS to GND. For $C_{SS}$ to affect start-up, $C_{REF} > C_{NTC}$ must be maintained so that the converter does not start in foldback mode. Figure 27 shows the typical start-up waveforms for the LM3424 assuming $C_{REF} > C_{NTC}$.

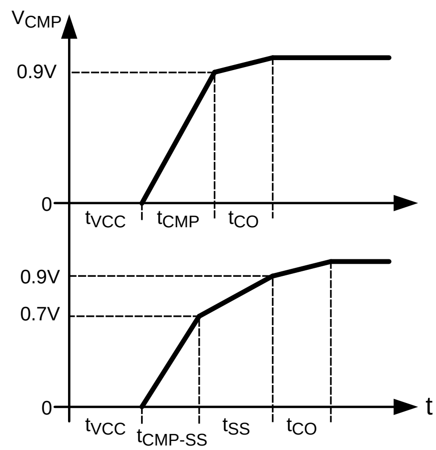



**Figure 27. Start-up Waveforms**

First, $C_{BYP}$ is charged to be above $V_{CC}$ UVLO threshold (~4.2V). The $C_{VCC}$ charging time ($t_{VCC}$) can be estimated as:

$$t_{VCC} = \frac{4.2V}{25\ mA} \times C_{BYP} = 168\Omega \times C_{BYP} \tag{21}$$

Assuming there is no $C_{SS}$ or if $C_{SS}$ is less than 40% of $C_{CMP}$ , $C_{CMP}$ is then charged to 0.9V over the charging time ($t_{CMP}$) which can be estimated as:

$$t_{CMP} = \frac{0.9V}{25\ \mu A} \times C_{CMP} = 36\ k\Omega \times C_{CMP} \tag{22}$$

## Feature Description (continued)

Once $C_{CMP}$ = 0.9V, the part starts switching to charge $C_O$ until the LED current is in regulation. The $C_O$ charging time ($t_{CO}$) can be roughly estimated as:

$$t_{CO} = C_O \times \frac{V_O}{I_{LED}} \tag{23}$$

If $C_{SS}$ is greater than 40% of $C_{CMP}$, the compensation capacitor will only charge to 0.7V over a smaller $C_{CMP}$ charging time ($t_{CMP\text{-}SS}$) which can be estimated as:

$$t_{CMP\text{-}SS} = \frac{0.70\text{V}}{25\,\mu\text{A}} \times C_{CMP} = 28\,\text{k}\Omega \times C_{CMP} \tag{24}$$

Then COMP will clamp to SS, forcing COMP to rise (the last 200 mV before switching begins) according to the $C_{SS}$ charging time ($t_{SS}$) which can be estimated as:

$$t_{SS} = \frac{0.2\text{V}}{10\,\mu\text{A}} \times C_{SS} = 20\ \text{k}\Omega \times C_{SS} \tag{25}$$

The system start-up time ($t_{SU}$ or $t_{SU\text{-}SS}$) is defined as:

$C_{SS}$ < 0.4 x $C_{CMP}$

$$t_{SU} = t_{VCC} + t_{CMP} + t_{CO} \tag{26}$$

$C_{SS}$ > 0.4 x $C_{CMP}$

$$t_{SU\text{-}SS} = t_{VCC} + t_{CMP\text{-}SS} + t_{SS} + t_{CO} \tag{27}$$

As a general rule of thumb, standard smooth startup operation can be achieved with $C_{SS}$ = $C_{CMP}$.

### 7.3.9 Overvoltage Lockout (OVLO)

The LM3424 can be configured to detect an output (or input) over-voltage condition via the OVP pin. The pin features a precision 1.24V threshold with 20 µA (typical) of hysteresis current as shown in Figure 28. When the OVLO threshold is exceeded, the GATE pin is immediately pulled low and a 20 µA current source provides hysteresis to the lower threshold of the OVLO hysteretic band.

If the LEDs are referenced to a potential other than ground (floating), as in the buck-boost and buck configuration, the output voltage ($V_O$) should be sensed and translated to ground by using a single PNP as shown in Figure 29.

The over-voltage turn-off threshold ($V_{TURN\text{-}OFF}$) is defined:

Ground Referenced

$$V_{TURN\text{-}OFF} = 1.24\text{V} \times \left(\frac{R_{OV1} + R_{OV2}}{R_{OV1}}\right) \tag{28}$$

Floating

$$V_{TURN\text{-}OFF} = 1.24\text{V} \times \left(\frac{0.5 \times R_{OV1} + R_{OV2}}{R_{OV1}}\right) \tag{29}$$

In the ground referenced configuration, the voltage across $R_{OV2}$ is $V_O$ - 1.24 V whereas in the floating configuration it is $V_O$ - 620 mV where 620 mV approximates $V_{BE}$ of the PNP.

The over-voltage hysteresis ($V_{HYSO}$) is defined:

$$V_{HYSO} = 20\,\mu\text{A} \times R_{OV2} \tag{30}$$

## Feature Description (continued)

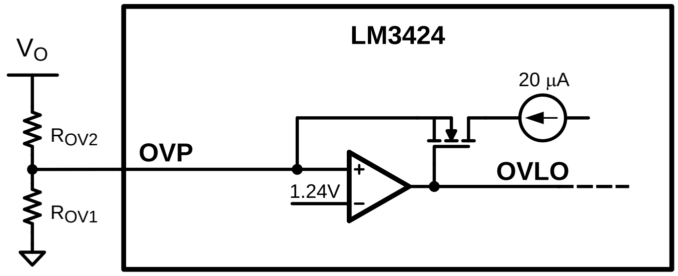



**Figure 28. Over-Voltage Protection Circuitry**

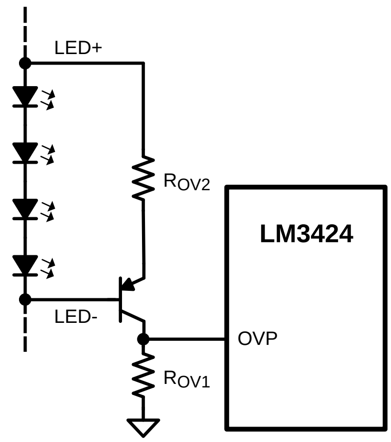



**Figure 29. Floating Output OVP Circuitry**

### 7.3.10 Input Undervoltage Lockout (UVLO)

The nDIM pin is a dual-function input that features an accurate 1.24V threshold with programmable hysteresis as shown in Figure 30. This pin functions as both the PWM dimming input for the LEDs and as a $V_{IN}$ UVLO. When the pin voltage rises and exceeds the 1.24V threshold, 20 µA (typical) of current is driven out of the nDIM pin into the resistor divider providing programmable hysteresis.

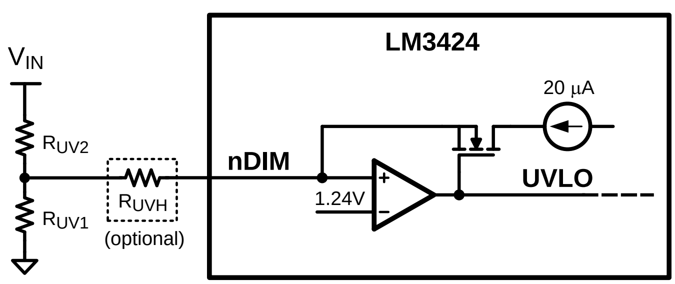



**Figure 30. UVLO Circuit**

When using the nDIM pin for UVLO and PWM dimming concurrently, the UVLO circuit can have an extra series resistor to set the hysteresis. This allows the standard resistor divider to have smaller resistor values minimizing PWM delays due to a pull-down MOSFET at the nDIM pin (see *PWM Dimming* section). In general, at least 3V of hysteresis is preferable when PWM dimming, if operating near the UVLO threshold.

The turn-on threshold ($V_{TURN-ON}$) is defined as follows:

$$V_{TURN-ON} = 1.24V \times \left( \frac{R_{UV1} + R_{UV2}}{R_{UV1}} \right) \tag{31}$$

## Feature Description (continued)

The hysteresis ($V_{HYS}$) is defined as follows:

#### *7.3.10.1 UVLO Only*

$$V_{HYS} = 20\,\mu A \times R_{UV2} \tag{32}$$

#### *7.3.10.2 PWM Dimming and UVLO*

$$V_{HYS} = 20\,\mu A \times \left(R_{UV2} + \frac{R_{UVH} \times (R_{UV1} + R_{UV2})}{R_{UV1}}\right) \tag{33}$$

### 7.3.11 PWM Dimming

The active low nDIM pin can be driven with a PWM signal which controls the main NFET and the dimming FET (dimFET). The brightness of the LEDs can be varied by modulating the duty cycle of this signal. LED brightness is approximately proportional to the PWM signal duty cycle, (that is, 30% duty cycle at approximately 30% LED brightness). This function can be ignored if PWM dimming is not required by using nDIM solely as a $V_{IN}$ UVLO input as described in the *Input Undervoltage Lockout (UVLO)* section or by tying it directly to $V_{CC}$ or $V_{IN}$.

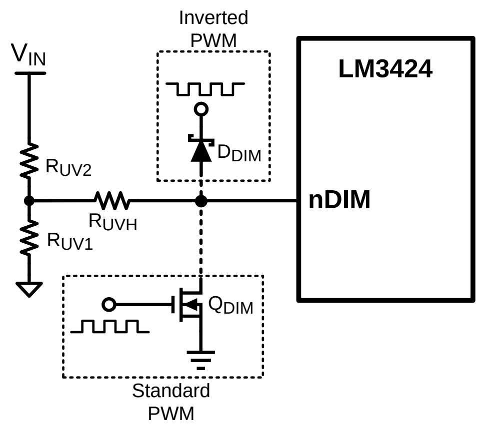



**Figure 31. PWM Dimming Circuit**

Figure 31 shows how the PWM signal is applied to nDIM:

1. Connect the dimming MOSFET ($Q_{DIM}$) with the drain to the nDIM pin and the source to GND. Apply an external logic-level PWM signal to the gate of $Q_{DIM}$.
2. Connect the anode of a Schottky diode ($D_{DIM}$) to the nDIM pin. Apply an inverted external logic-level PWM signal to the cathode of the same diode.

The DDRV pin is a PWM output that follows the nDIM PWM input signal. When the nDIM pin rises, the DDRV pin rises and the PWM latch reset signal is removed allowing the main MOSFET Q1 to turn on at the beginning of the next clock set pulse. In boost and buck-boost topologies, the DDRV pin is used to control a N-channel MOSFET placed in series with the LED load, while it would control a P-channel MOSFET in parallel with the load for a buck topology.

The series dimFET will open the LED load, when nDIM is low, effectively speeding up the rise and fall times of the LED current. Without any dimFET, the rise and fall times are limited by the inductor slew rate and dimming frequencies above 1 kHz are impractical. Using the series dimFET, dimming frequencies up to 30 kHz are achievable. With a parallel dimFET (buck topology), even higher dimming frequencies are achievable.

When using the PWM functionality in a boost regulator, the PWM signal drives a ground referenced FET. However, with buck-boost and buck topologies, level shifting circuitry is necessary to translate the PWM dim signal to the floating dimFET as shown in Figure 32 and Figure 33.

## Feature Description (continued)

When using a series dimFET to PWM dim the LED current, more output capacitance is always better. A general rule of thumb is to use a minimum of 40 µF when PWM dimming. For most applications, this will provide adequate energy storage at the output when the dimFET turns off and opens the LED load. Then when the dimFET is turned back on, the capacitance helps source current into the load, improving the LED current rise time.

A minimum on-time must be maintained in order for PWM dimming to operate in the linear region of its transfer function. Because the controller is disabled during dimming, the PWM pulse must be long enough such that the energy intercepted from the input is greater than or equal to the energy being put into the LEDs. For boost and buck-boost regulators, the minimum dimming pulse length in seconds ($t_{PULSE}$) is:

$$t_{PULSE} = \frac{2 \times I_{LED} \times V_O \times L1}{V_{IN}^2} \tag{34}$$

Even maintaining a dimming pulse greater than $t_{PULSE}$, preserving linearity at low dimming duty cycles is difficult. Several modifications are suggested for applications requiring low dimming duty cycles. Since nDIM rising releases the latch but does not trigger the on-time specifically, there will be an effective jitter on the rising edge of the LED current. This jitter can be easily removed by tying the PWM input signal through the synchronization network at the RT pin (shown in Figure 35), forcing the on-time to synchronize with the nDIM pulse.

The second helpful modification is to remove the $C_{FS}$ capacitor and $R_{FS}$ resistor, eliminating the high frequency compensation pole. This should not affect stability, but it will speed up the response of the CSH pin, specifically at the rising edge of the LED current when PWM dimming, thus improving the achievable linearity at low dimming duty cycles.

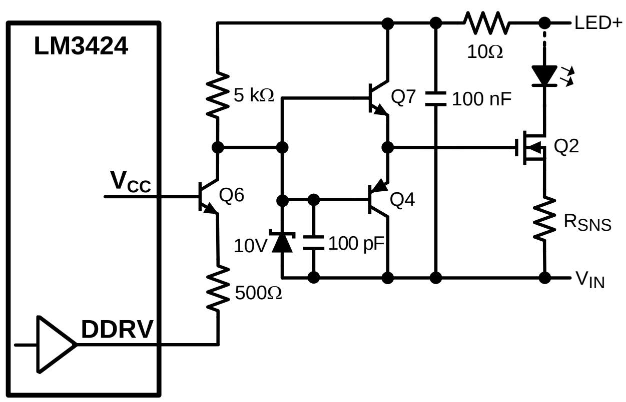



**Figure 32. Buck-boost Level-Shifted PWM Circuit**

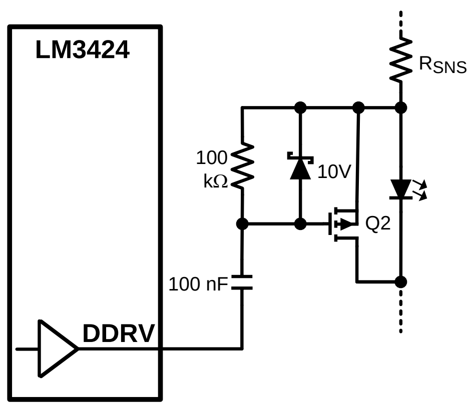



**Figure 33. Buck Level-Shifted PWM Circuit**

## Feature Description (continued)

### 7.3.12 Thermal Shutdown

The LM3424 includes thermal shutdown. If the die temperature reaches approximately 165°C the device will shut down (GATE pin low), until it reaches approximately 140°C where it turns on again.

## 7.4 Device Functional Modes

There are no additional device functional modes for this part.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

### 8.1.1 Inductor

The inductor (L1) is the main energy storage device in a switching regulator. Depending on the topology, energy is stored in the inductor and transfered to the load in different ways (as an example, buck-boost operation is detailed in the *Current Regulators* section). The size of the inductor, the voltage across it, and the length of the switching subinterval ($t_{ON}$ or $t_{OFF}$) determines the inductor current ripple ($\Delta i_{L-PP}$). In the design process, L1 is chosen to provide a desired $\Delta i_{L-PP}$. For a buck regulator the inductor has a direct connection to the load, which is good for a current regulator. This requires little to no output capacitance therefore $\Delta i_{L-PP}$ is basically equal to the LED ripple current $\Delta i_{LED-PP}$. However, for boost and buck-boost regulators, there is always an output capacitor which reduces $\Delta i_{LED-PP}$, therefore the inductor ripple can be larger than in the buck regulator case where output capacitance is minimal or completely absent.

In general, $\Delta i_{LED-PP}$ is recommended by manufacturers to be less than 40% of the average LED current ($I_{LED}$). Therefore, for the buck regulator with no output capacitance, $\Delta i_{L-PP}$ should also be less than 40% of $I_{LED}$. For the boost and buck-boost topologies, $\Delta i_{L-PP}$ can be much higher depending on the output capacitance value. However, $\Delta i_{L-PP}$ is suggested to be less than 100% of the average inductor current ($I_L$) to limit the RMS inductor current.

L1 is also suggested to have an RMS current rating at least 25% higher than the calculated minimum allowable RMS inductor current ($I_{L-RMS}$).

### 8.1.2 LED Dynamic Resistance

When the load is a string of LEDs, the output load resistance is the LED string dynamic resistance plus $R_{SNS}$. LEDs are PN junction diodes, and their dynamic resistance shifts as their forward current changes. Dividing the forward voltage of a single LED ($V_{LED}$) by the forward current ($I_{LED}$) leads to an incorrect calculation of the dynamic resistance of a single LED ($r_{LED}$). The result can be 5 to 10 times higher than the true $r_{LED}$ value.

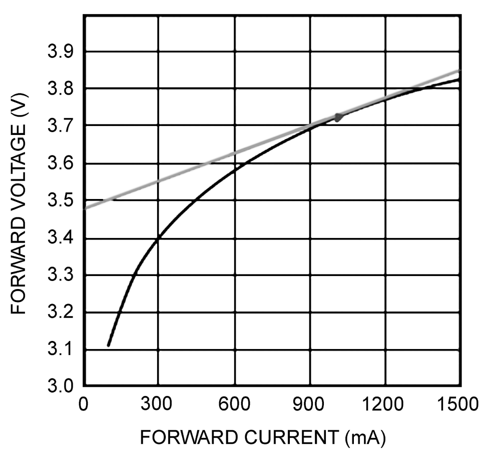



**Figure 34. Dynamic Resistance**

Obtaining $r_{LED}$ is accomplished by referring to the manufacturer's LED I-V characteristic. It can be calculated as the slope at the nominal operating point as shown in Figure 34. For any application with more than 2 series LEDs, $R_{SNS}$ can be neglected allowing $r_D$ to be approximated as the number of LEDs multiplied by $r_{LED}$.

## Application Information (continued)

### 8.1.3 Output Capacitor

For boost and buck-boost regulators, the output capacitor ($C_O$) provides energy to the load when the recirculating diode (D1) is reverse biased during the first switching subinterval. An output capacitor in a buck topology will simply reduce the LED current ripple ($\Delta i_{LED\text{-}PP}$) below the inductor current ripple ($\Delta i_{L\text{-}PP}$). In all cases, $C_O$ is sized to provide a desired $\Delta i_{LED\text{-}PP}$. As mentioned in the *Inductor* section, $\Delta i_{LED\text{-}PP}$ is recommended by manufacturers to be less than 40% of the average LED current ($I_{LED}$).

$C_O$ should be carefully chosen to account for derating due to temperature and operating voltage. It must also have the necessary RMS current rating. Ceramic capacitors are the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dieletric rating is suggested.

### 8.1.4 Input Capacitors

The input capacitance ($C_{IN}$) provides energy during the discontinuous portions of the switching period. For buck and buck-boost regulators, $C_{IN}$ provides energy during $t_{ON}$ and during $t_{OFF}$, the input voltage source charges up $C_{IN}$ with the average input current ($I_{IN}$). For boost regulators, $C_{IN}$ only needs to provide the ripple current due to the direct connection to the inductor. $C_{IN}$ is selected given the maximum input voltage ripple ($\Delta v_{IN\text{-}PP}$) which can be tolerated. $\Delta v_{IN\text{-}PP}$ is suggested to be less than 10% of the input voltage ($V_{IN}$).

An input capacitance at least 100% greater than the calculated $C_{IN}$ value is recommended to account for derating due to temperature and operating voltage. When PWM dimming, even more capacitance can be helpful to minimize the large current draw from the input voltage source during the rising transistion of the LED current waveform.

The chosen input capacitors must also have the necessary RMS current rating. Ceramic capacitors are again the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dieletric rating is suggested.

For most applications, it is recommended to bypass the $V_{IN}$ pin with an 0.1 µF ceramic capacitor placed as close as possible to the pin. In situations where the bulk input capacitance may be far from the LM3424 device, a 10 Ω series resistor can be placed between the bulk input capacitance and the bypass capacitor, creating a 150 kHz filter to eliminate undesired high frequency noise.

### 8.1.5 Main MOSFET and Dimming MOSFET

The LM3424 requires an external NFET (Q1) as the main power MOSFET for the switching regulator. Q1 is recommended to have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node. In practice, all switching regulators have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. The current rating is recommended to be at least 10% higher than the average transistor current. The power rating is then verified by calculating the power loss given the RMS transistor current and the NFET on-resistance ($R_{DS\text{-}ON}$).

When PWM dimming, the LM3424 requires another MOSFET (Q2) placed in series (or parallel for a buck regulator) with the LED load. This MOSFET should have a voltage rating greater than the output voltage ($V_O$) and a current rating at least 10% higher than the nominal LED current ($I_{LED}$) . The power rating is simply $V_O$ multiplied by $R_{DS\text{-}ON}$, assuming 100% dimming duty cycle (continuous operation) will occur.

In general, the NFETs should be chosen to minimize total gate charge ($Q_g$) when $f_{SW}$ is high and minimize $R_{DS\text{-}ON}$ otherwise. This will minimize the dominant power losses in the system. Frequently, higher current NFETs in larger packages are chosen for better thermal performance.

### 8.1.6 Re-Circulating Diode

A re-circulating diode (D1) is required to carry the inductor current during $t_{OFF}$. The most efficient choice for D1 is a Schottky diode due to low forward voltage drop and near-zero reverse recovery time. Similar to Q1, D1 is recommended to have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node and a current rating at least 10% higher than the average diode current. The power rating is verified by calculating the power loss through the diode. This is accomplished by checking the typical diode forward voltage from the I-V curve on the product datasheet and multiplying by the average diode current. In general, higher current diodes have a lower forward voltage and come in better performing packages minimizing both power losses and temperature rise.

## Application Information (continued)

### 8.1.7 Switching Frequency

The switching frequency of the LM3424 is programmed using an external resistor ($R_T$) connected from the RT pin to GND as shown in Figure 35.

Alternatively, an external PWM signal can be applied to the RT pin through a filter ($R_{FLT}$ and $C_{FLT}$) and an AC coupling capacitor ($C_{AC}$) to synchronize the part to an external clock as shown in Figure 35. If the external PWM signal is applied at a frequency higher than the base frequency set by the $R_T$ resistor, the internal oscillator is bypassed and the switching frequency becomes the synchronized frequency. The external synchronization signal should have a pulse width of 100ns, an amplitude between 3V and 6V, and be AC coupled to the RT pin with a ceramic capacitor ($C_{AC}$ = 100pF). A 10MHz RC filter ($R_{FLT}$ = 150Ω and $C_{FLT}$ = 100 pF) should be placed between the PWM signal and $C_{AC}$ to eliminate unwanted high frequency noise from coupling into the RT pin.

The switching frequency is defined:

$$f_{SW} = \frac{1}{1.4 \times 10^{-10} \times R_T - 1.95 \times 10^{-8}} \quad (35)$$

See the *Typical Characteristics* section for a plot of $R_T$ vs. $f_{SW}$.

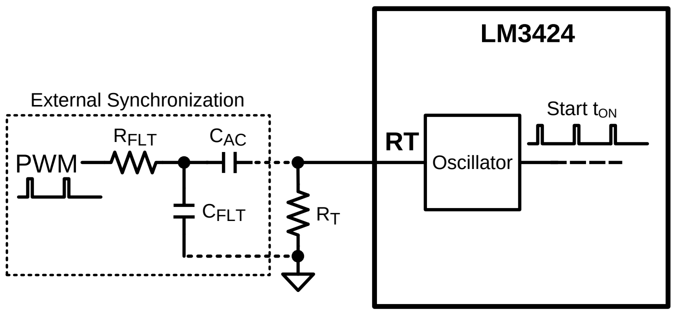



**Figure 35. Timing Circuitry**

## 8.2 Typical Applications

### 8.2.1 Basic Topology Schematics

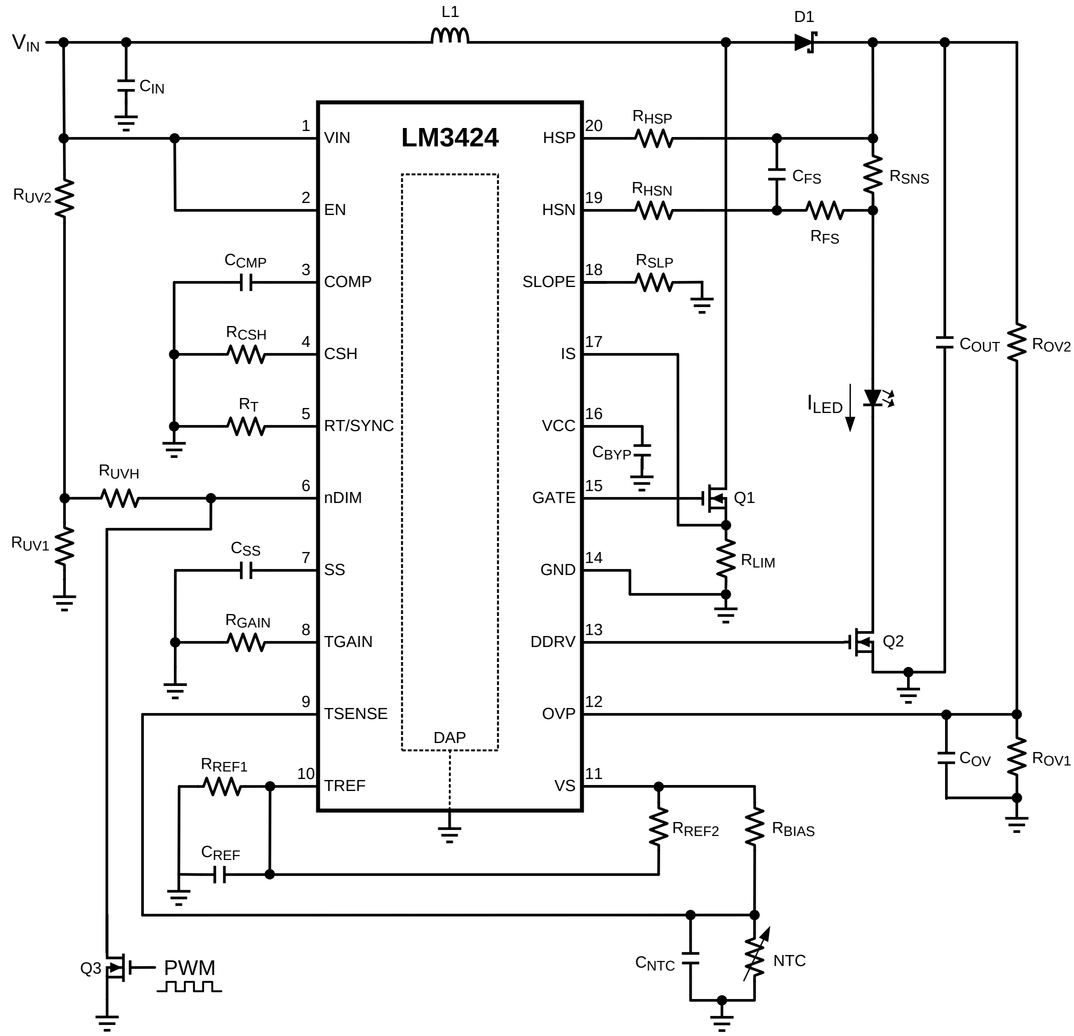



**Figure 36. Boost Regulator ($V_{IN}$ < $V_O$)**

## Typical Applications (continued)

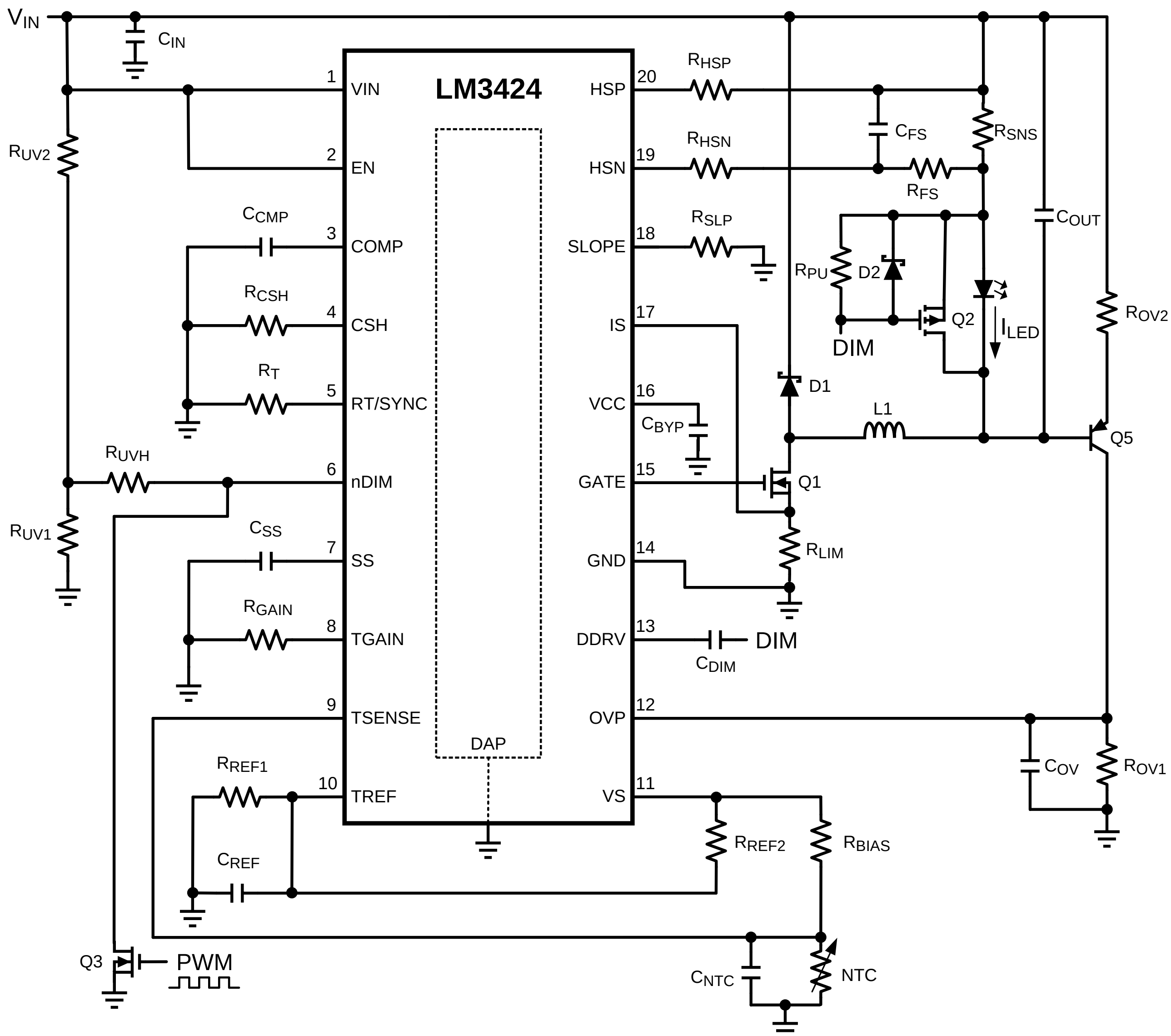



**Figure 37. Buck Regulator ($V_{IN} > V_O$)**

## Typical Applications (continued)

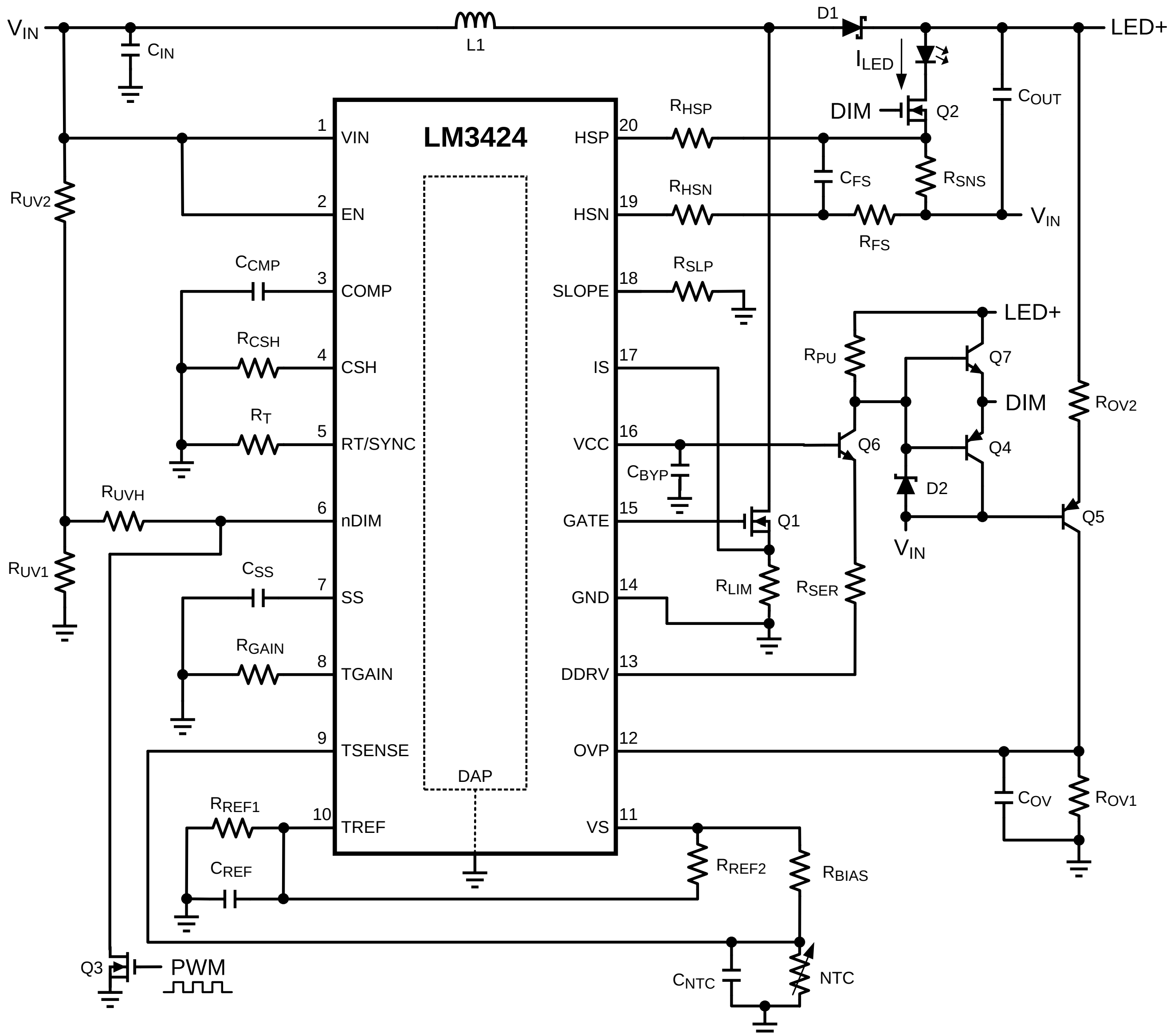



**Figure 38. Buck-Boost Regulator**

#### 8.2.1.1 Design Requirements

Number of series LEDs: N

Single LED forward voltage: $V_{LED}$

Single LED dynamic resistance: $r_{LED}$

Nominal input voltage: $V_{IN}$

Input voltage range: $V_{IN-MAX}$, $V_{IN-MIN}$

Switching frequency: $f_{SW}$

Current sense voltage: $V_{SNS}$

Average LED current: $I_{LED}$

## Typical Applications (continued)

Inductor current ripple: $\Delta i_{L-PP}$

LED current ripple: $\Delta i_{LED-PP}$

Peak current limit: $I_{LIM}$

Input voltage ripple: $\Delta v_{IN-PP}$

Output OVLO characteristics: $V_{TURN-OFF}$, $V_{HYSO}$

Input UVLO characteristics: $V_{TURN-ON}$, $V_{HYS}$

Thermal foldback characteristics: $T_{BK}$, $T_{END}$

Total start-up time: $t_{TSU}$

### *8.2.1.2 Detailed Design Procedure*

#### 8.2.1.2.1 Operating Point

Given the number of series LEDs (N), the forward voltage ($V_{LED}$) and dynamic resistance ($r_{LED}$) for a single LED, solve for the nominal output voltage ($V_O$) and the nominal LED string dynamic resistance ($r_D$):

$$V_O = N \times V_{LED} \quad (36)$$

$$r_D = N \times r_{LED} \quad (37)$$

Solve for the ideal nominal duty cycle (D):

Buck

$$D = \frac{V_O}{V_{IN}} \quad (38)$$

Boost

$$D = \frac{V_O - V_{IN}}{V_O} \quad (39)$$

Buck-Boost

$$D = \frac{V_O}{V_O + V_{IN}} \quad (40)$$

Using the same equations, find the minimum duty cycle ($D_{MIN}$) using maximum input voltage ($V_{IN-MAX}$) and the maximum duty cycle ($D_{MAX}$) using the minimum input voltage ($V_{IN-MIN}$). Also, remember that D' = 1 - D.

#### 8.2.1.2.2 Switching Frequency

Set the switching frequency ($f_{SW}$) by solving for $R_T$:

$$R_T = \frac{1 + 1.95\text{x}10^{-8} \text{ x } f_{SW}}{1.40\text{x}10^{-10} \text{ x } f_{SW}} \quad (41)$$

#### 8.2.1.2.3 Average LED Current

For all topologies, set the average LED current ($I_{LED}$) knowing the desired current sense voltage ($V_{SNS}$) and solving for $R_{SNS}$:

$$R_{SNS} = \frac{V_{SNS}}{I_{LED}} \quad (42)$$

If the calculated $R_{SNS}$ is too far from a desired standard value, then $V_{SNS}$ will have to be adjusted to obtain a standard value.

Setup the suggested signal current of 100 µA by assuming $R_{CSH}$ = 12.4 kΩ and solving for $R_{HSP}$:

$$R_{HSP} = \frac{I_{LED} \text{ x } R_{CSH} \text{ x } R_{SNS}}{1.24\text{V}} \quad (43)$$

## Typical Applications (continued)

If the calculated $R_{HSP}$ is too far from a desired standard value, then $R_{CSH}$ can be adjusted to obtain a standard value.

#### 8.2.1.2.4 Thermal Foldback

For all topologies, set the thermal foldback breakpoint ($T_{BK}$) by finding corresponding $R_{NTC\text{-}BK}$ from manufacturer's datasheet and solving for $R_{BIAS}$:

$$R_{BIAS} = R_{NTC\text{-}BK} \times \frac{R_{REF2}}{R_{REF1}} \tag{44}$$

The easiest approach is to set $R_{REF1} = R_{REF2}$, therefore setting $R_{BIAS} = R_{NTC\text{-}BK}$ will properly set $T_{BK}$. Remember, capacitance is recommended at the TSENSE and TREF pins, so ensure $C_{REF} > C_{NTC}$ to prevent start-up in foldback.

Then set the thermal foldback endpoint ($T_{END}$) by finding the corresponding $R_{NTC\text{-}END}$ from manufacturer's datasheet and solving for $R_{GAIN}$:

$$R_{GAIN} = \frac{\left(\frac{R_{REF1}}{R_{REF1} + R_{REF2}} - \frac{R_{NTC\text{-}END}}{R_{NTC\text{-}END} + R_{BIAS}}\right) \times 2.45\text{V}}{I_{CSH}} \tag{45}$$

#### 8.2.1.2.5 Inductor Ripple Current

Set the nominal inductor ripple current ($\Delta i_{L\text{-}PP}$) by solving for the appropriate inductor (L1):

Buck

$$L1 = \frac{(V_{IN} - V_O) \times D}{\Delta i_{L\text{-}PP} \times f_{SW}} \tag{46}$$

Boost and Buck-boost

$$L1 = \frac{V_{IN} \times D}{\Delta i_{L\text{-}PP} \times f_{SW}} \tag{47}$$

To set the worst case inductor ripple current, use $V_{IN\text{-}MAX}$ and $D_{MIN}$ when solving for L1.

The minimum allowable inductor RMS current rating ($I_{L\text{-}RMS}$) can be calculated as:

Buck

$$I_{L\text{-}RMS} = I_{LED} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{L\text{-}PP}}{I_{LED}}\right)^2} \tag{48}$$

Boost and Buck-Boost

$$I_{L\text{-}RMS} = \frac{I_{LED}}{D'} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{L\text{-}PP} \times D'}{I_{LED}}\right)^2} \tag{49}$$

#### 8.2.1.2.6 LED Ripple Current

Set the nominal LED ripple current ($\Delta i_{LED\text{-}PP}$), by solving for the output capacitance ($C_O$):

Buck

$$C_O = \frac{\Delta i_{L\text{-}PP}}{8 \times f_{SW} \times r_D \times \Delta i_{LED\text{-}PP}} \tag{50}$$

Boost and Buck-Boost

$$C_O = \frac{I_{LED} \times D}{r_D \times \Delta i_{LED\text{-}PP} \times f_{SW}} \tag{51}$$

## Typical Applications (continued)

To set the worst case LED ripple current, use $D_{MAX}$ when solving for $C_O$. Remember, when PWM dimming it is recommended to use a minimum of 40 µF of output capacitance to improve performance.

The minimum allowable RMS output capacitor current rating ($I_{CO-RMS}$) can be approximated:

Buck

$$I_{CO-RMS} = \frac{\Delta i_{LED-PP}}{\sqrt{12}} \tag{52}$$

Boost and Buck-Boost

$$I_{CO-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1-D_{MAX}}} \tag{53}$$

#### 8.2.1.2.7 Peak Current Limit

Set the peak current limit ($I_{LIM}$) by solving for the transistor path sense resistor ($R_{LIM}$):

$$R_{LIM} = \frac{245\ \text{mV}}{I_{LIM}} \tag{54}$$

#### 8.2.1.2.8 Slope Compensation

For all topologies, the preferred method to set slope compensation is to ensure any duty cycle is attainable for the nominal $V_O$ and chosen L by solving for $R_{SLP}$:

$$R_{SLP} \quad \frac{1.5\text{x}10^{13} \text{ x } L1}{V_O \text{x} R_T \text{x} R_{LIM}} \tag{55}$$

#### 8.2.1.2.9 Loop Compensation

Using a simple first order peak current mode control model, neglecting any output capacitor ESR dynamics, the necessary loop compensation can be determined.

First, the uncompensated loop gain ($T_U$) of the regulator can be approximated:

Buck

$$T_U = T_{U0} \times \frac{1}{\left(1 + \frac{s}{\omega_{P1}}\right)} \tag{56}$$

Boost and Buck-Boost

$$T_U = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)} \tag{57}$$

Where the pole ($\omega_{P1}$) is approximated:

Buck

$$\omega_{P1} = \frac{1}{r_D \times C_O} \tag{58}$$

Boost

$$\omega_{P1} = \frac{2}{r_D \times C_O} \tag{59}$$

Buck-Boost

## Typical Applications (continued)

$$\omega_{P1} = \frac{1+D}{r_D \times C_O} \tag{60}$$

And the RHP zero ($\omega_{Z1}$) is approximated:

Boost

$$\omega_{Z1} = \frac{r_D \times D'^2}{L1} \tag{61}$$

Buck-Boost

$$\omega_{Z1} = \frac{r_D \times D'^2}{D \times L1} \tag{62}$$

And the uncompensated DC loop gain ($T_{U0}$) is approximated:

Buck

$$T_{U0} = \frac{500V \times R_{CSH} \times R_{SNS}}{R_{HSP} \times R_{LIM}} = \frac{620V}{I_{LED} \times R_{LIM}} \tag{63}$$

Boost

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{2 \times R_{HSP} \times R_{LIM}} = \frac{D' \times 310V}{I_{LED} \times R_{LIM}} \tag{64}$$

Buck-Boost

$$T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{(1+D) \times R_{HSP} \times R_{LIM}} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} \tag{65}$$

For all topologies, the primary method of compensation is to place a low frequency dominant pole ($\omega_{P2}$) which will ensure that there is ample phase margin at the crossover frequency. This is accomplished by placing a capacitor ($C_{CMP}$) from the COMP pin to GND, which is calculated according to the lower value of the pole and the RHP zero of the system (shown as a minimizing function):

$$\omega_{P2} = \frac{\min(\omega_{P1}, \omega_{Z1})}{5 \times T_{U0}} \tag{66}$$

$$C_{CMP} = \frac{1}{\omega_{P2} \times 5 \text{x} 10^6} \tag{67}$$

If analog dimming is used, $C_{CMP}$ should be approximately 4x larger to maintain stability as the LEDs are dimmed to zero.

A high frequency compensation pole ($\omega_{P3}$) can be used to attenuate switching noise and provide better gain margin. Assuming $R_{FS}$ = 10Ω, $C_{FS}$ is calculated according to the higher value of the pole and the RHP zero of the system (shown as a maximizing function):

$$\omega_{P3} = \max(\omega_{P1}, \omega_{Z1}) \times 10 \tag{68}$$

$$C_{FS} = \frac{1}{10 \times \omega_{P3}} \tag{69}$$

The total system loop gain (T) can then be written as:

Buck

$$T = T_{U0} \times \frac{1}{\left(1+\frac{s}{\omega_{P1}}\right) \times \left(1+\frac{s}{\omega_{P2}}\right) \times \left(1+\frac{s}{\omega_{P3}}\right)} \tag{70}$$

Boost and Buck-Boost

## Typical Applications (continued)

$$T = T_{U0} \times \frac{\left(1 - \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right) \times \left(1 + \frac{s}{\omega_{P2}}\right) \times \left(1 + \frac{s}{\omega_{P3}}\right)} \quad (71)$$

#### 8.2.1.2.10 Input Capacitance

Set the nominal input voltage ripple ($\Delta v_{IN-PP}$) by solving for the required capacitance ($C_{IN}$):

Buck

$$C_{IN} = \frac{I_{LED} \times (1 - D) \times D}{\Delta V_{IN-PP} \times f_{SW}} \quad (72)$$

Boost

$$C_{IN} = \frac{\Delta i_{L-PP}}{8 \times \Delta V_{IN-PP} \times f_{SW}} \quad (73)$$

Buck-Boost

$$C_{IN} = \frac{I_{LED} \times D}{\Delta V_{IN-PP} \times f_{SW}} \quad (74)$$

Use $D_{MAX}$ to set the worst case input voltage ripple, when solving for $C_{IN}$ in a buck-boost regulator and $D_{MID}$ = 0.5 when solving for $C_{IN}$ in a buck regulator.

The minimum allowable RMS input current rating ($I_{CIN-RMS}$) can be approximated:

Buck

$$I_{CIN-RMS} = I_{LED} \times \sqrt{D_{MID} \times (1 - D_{MID})} \quad (75)$$

Boost

$$I_{CIN-RMS} = \frac{\Delta i_{L-PP}}{\sqrt{12}} \quad (76)$$

Buck-Boost

$$I_{CIN-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \quad (77)$$

#### 8.2.1.2.11 NFET

The NFET voltage rating should be at least 15% higher than the maximum NFET drain-to-source voltage ($V_{T-MAX}$):

Buck

$$V_{T-MAX} = V_{IN-MAX} \quad (78)$$

Boost

$$V_{T-MAX} = V_O \quad (79)$$

Buck-Boost

$$V_{T-MAX} = V_{IN-MAX} + V_O \quad (80)$$

The current rating should be at least 10% higher than the maximum average NFET current ($I_{T-MAX}$):

Buck

$$I_{T-MAX} = D_{MAX} \times I_{LED} \quad (81)$$

Boost and Buck-Boost

## Typical Applications (continued)

$$I_{T\text{-}MAX} = \frac{D_{MAX}}{1 - D_{MAX}} \times I_{LED} \quad (82)$$

Approximate the nominal RMS transistor current ($I_{T\text{-}RMS}$) :

Buck

$$I_{T\text{-}RMS} = I_{LED} \times \sqrt{D} \quad (83)$$

Boost and Buck-Boost

$$I_{T\text{-}RMS} = \frac{I_{LED}}{D'} \times \sqrt{D} \quad (84)$$

Given an NFET with on-resistance ($R_{DS\text{-}ON}$), solve for the nominal power dissipation ($P_T$):

$$P_T = {I_{T\text{-}RMS}}^2 \times R_{DSON} \quad (85)$$

#### 8.2.1.2.12 Diode

The Schottky diode voltage rating should be at least 15% higher than the maximum blocking voltage ($V_{RD\text{-}MAX}$):

Buck

$$V_{RD\text{-}MAX} = V_{IN\text{-}MAX} \quad (86)$$

Boost

$$V_{RD\text{-}MAX} = V_O \quad (87)$$

Buck-Boost

$$V_{RD\text{-}MAX} = V_{IN\text{-}MAX} + V_O \quad (88)$$

The current rating should be at least 10% higher than the maximum average diode current ($I_{D\text{-}MAX}$):

Buck

$$I_{D\text{-}MAX} = (1 - D_{MIN}) \times I_{LED} \quad (89)$$

Boost and Buck-Boost

$$I_{D\text{-}MAX} = I_{LED} \quad (90)$$

Replace $D_{MAX}$ with D in the $I_{D\text{-}MAX}$ equation to solve for the average diode current ($I_D$). Given a diode with forward voltage ($V_{FD}$), solve for the nominal power dissipation ($P_D$):

$$P_D = I_D \times V_{FD} \quad (91)$$

#### 8.2.1.2.13 Output OVLO

For boost and buck-boost regulators, output OVLO is programmed with the turn-off threshold voltage ($V_{TURN\text{-}OFF}$) and the desired hysteresis ($V_{HYSO}$). To set $V_{HYSO}$, solve for $R_{OV2}$:

$$R_{OV2} = \frac{V_{HYSO}}{20\,\mu A} \quad (92)$$

To set $V_{TURN\text{-}OFF}$, solve for $R_{OV1}$:

Boost

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN\text{-}OFF} - 1.24V} \quad (93)$$

Buck-Boost

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN\text{-}OFF} - 620\ mV} \quad (94)$$

## Typical Applications (continued)

A small filter capacitor ($C_{OVP}$ = 47 pF) should be added from the OVP pin to ground to reduce coupled switching noise.

#### 8.2.1.2.14 Input UVLO

For all topologies, input UVLO is programmed with the turn-on threshold voltage ($V_{TURN-ON}$) and the desired hysteresis ($V_{HYS}$).

**Method 1:** If no PWM dimming is required, a two resistor network can be used. To set $V_{HYS}$, solve for $R_{UV2}$:

$$R_{UV2} = \frac{V_{HYS}}{20\,\mu A} \tag{95}$$

To set $V_{TURN-ON}$, solve for $R_{UV1}$:

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN-ON} - 1.24V} \tag{96}$$

**Method 2:** If PWM dimming is required, a three resistor network is suggested. To set $V_{TURN-ON}$, assume $R_{UV2}$ = 10 kΩ and solve for $R_{UV1}$ as in Method 1. To set $V_{HYS}$, solve for $R_{UVH}$:

$$R_{UVH} = \frac{R_{UV1} \times (V_{HYS} - 20\,\mu A \times R_{UV2})}{20\,\mu A \times (R_{UV1} + R_{UV2})} \tag{97}$$

#### 8.2.1.2.15 Soft-Start

For all topologies, if soft-start is desired, find the start-up time without $C_{SS}$ ($t_{SU}$):

$$t_{SU} = t_{VCC} + t_{CMP} + t_{CO} \tag{98}$$

Then, if the desired total start-up time ($t_{TSU}$) is larger than $t_{SU}$, solve for the base start-up time ($t_{SU-SS-BASE}$), assuming that a $C_{SS}$ greater than 40% of $C_{CMP}$ will be used:

$$t_{SU-SS-BASE} = 168\Omega \times C_{BYP} + 28\,k\Omega \times C_{CMP} + \frac{V_O}{I_{LED}} \times C_O \tag{99}$$

Then solve for $C_{SS}$:

$$C_{SS} = \frac{10\,\mu A}{0.2V} \times (t_{TSU} - t_{SU-SS-BASE}) \tag{100}$$

#### 8.2.1.2.16 PWM Dimming Method

PWM dimming can be performed several ways:

**Method 1:** Connect the dimming MOSFET ($Q_3$) with the drain to the nDIM pin and the source to GND. Apply an external PWM signal to the gate of $Q_{DIM}$. A pull down resistor may be necessary to properly turn off $Q_3$.

**Method 2:** Connect the anode of a Schottky diode to the nDIM pin. Apply an external inverted PWM signal to the cathode of the same diode.

The DDRV pin should be connected to the gate of the dimFET with or without level-shifting circuitry as described in the *PWM Dimming* section. The dimFET should be rated to handle the average LED current and the nominal output voltage.

#### 8.2.1.2.17 Analog Dimming Method

Analog dimming can be performed several ways:

**Method 1:** Place a potentiometer in place of the thermistor in the thermal foldback circuit shown in the *Thermal Foldback and Analog Dimming* section.

**Method 2:** Place a potentiometer in series with the $R_{CSH}$ resistor to dim the LED current from the nominal $I_{LED}$ to near zero.

**Method 3:** Connect a controlled current source as detailed in the *Thermal Foldback and Analog Dimming* section to the CSH pin. Increasing the current sourced into the CSH node will decrease the LEDs from the nominal $I_{LED}$ to zero current in the same manner as the thermal foldback circuit.

## Typical Applications (continued)

### 8.2.2 Buck-Boost Application

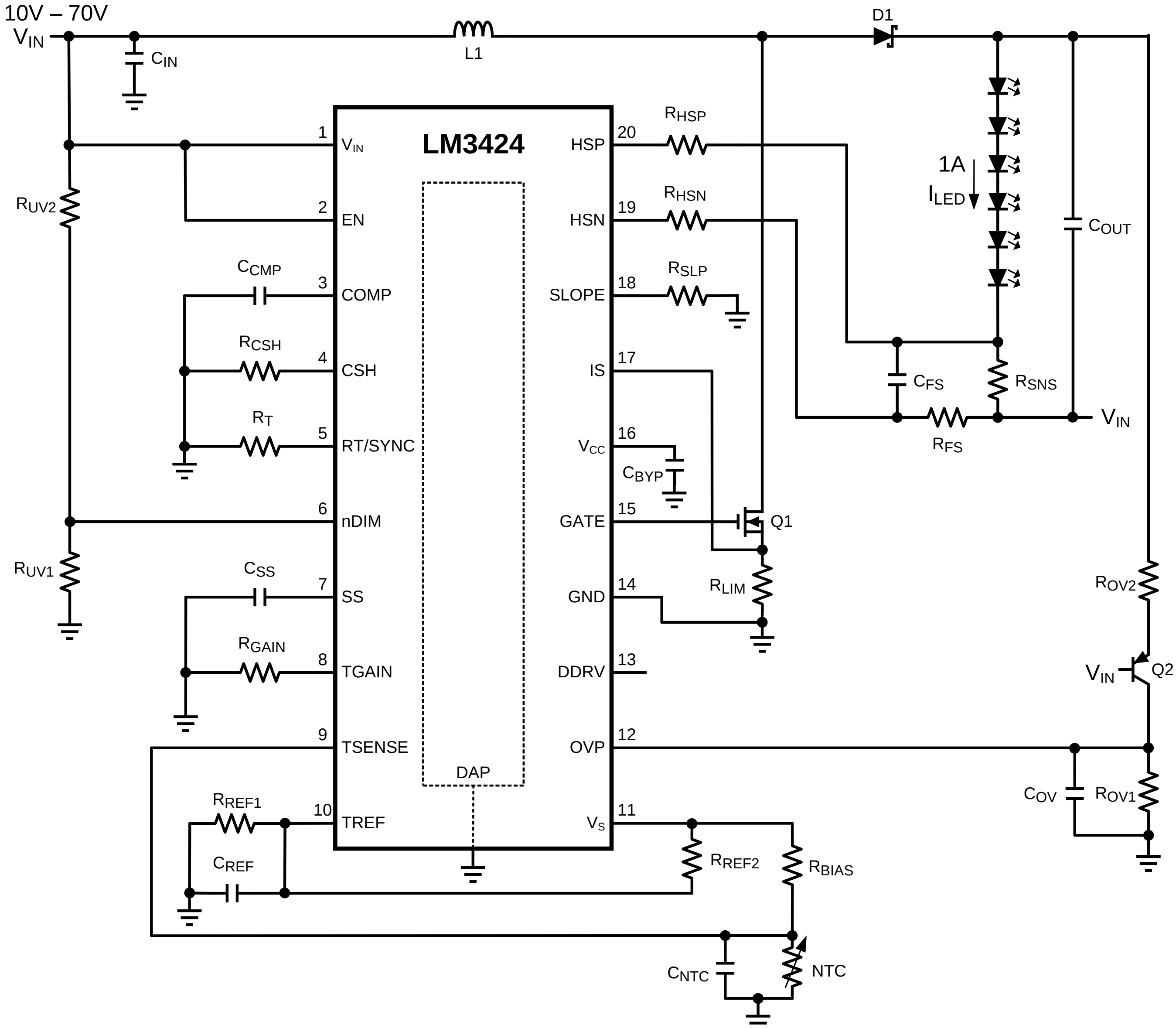



**Figure 39. Buck-Boost Application**

#### *8.2.2.1 Design Requirements*

N = 6

$V_{LED}$ = 3.5V

$r_{LED}$ = 325 mΩ

$V_{IN}$ = 24V

$V_{IN-MIN}$ = 10V

$V_{IN-MAX}$ = 70V

$f_{SW}$ = 500 kHz

$V_{SNS}$ = 100 mV

## Typical Applications (continued)

$I_{LED}$ = 1A

$\Delta i_{L-PP}$ = 700 mA

$\Delta i_{LED-PP}$ = 12 mA

$\Delta v_{IN-PP}$ = 100 mV

$I_{LIM}$ = 6A

$V_{TURN-ON}$ = 10V

$V_{HYS}$ = 3V

$V_{TURN-OFF}$ = 40V

$V_{HYSO}$ = 10V

$T_{BK}$ = 70°C

$T_{END}$= 120°C

$t_{TSU}$ = 30 ms

### *8.2.2.2 Detailed Design Procedure*

#### 8.2.2.2.1 Operating Point

Solve for $V_O$ and $r_D$:

$$V_O = N \times V_{LED} = 6 \times 3.5V = 21V \quad (101)$$

$$r_D = N \times r_{LED} = 6 \times 325\ m\Omega = 1.95\Omega \quad (102)$$

Solve for D, D', $D_{MAX}$, and $D_{MIN}$:

$$D = \frac{V_O}{V_O + V_{IN}} = \frac{21V}{21V + 24V} = 0.467 \quad (103)$$

$$D' = 1 - D = 1 - 0.467 = 0.533 \quad (104)$$

$$D_{MIN} = \frac{V_O}{V_O + V_{IN-MAX}} = \frac{21V}{21V + 70V} = 0.231 \quad (105)$$

$$D_{MAX} = \frac{V_O}{V_O + V_{IN-MIN}} = \frac{21V}{21V + 10V} = 0.677 \quad (106)$$

#### 8.2.2.2.2 Switching Frequency

Solve for $R_T$:

$$R_T = \frac{1 + 1.95 \times 10^{-8} \times f_{SW}}{1.4 \times 10^{-10} \times f_{SW}} = \frac{1 + 1.95 \times 10^{-8} \times 500\ kHz}{1.4 \times 10^{-10} \times 500\ kHz} = 14.4\ k\Omega \quad (107)$$

The closest standard resistor is 14.3 kΩ therefore $f_{SW}$ is:

$$f_{SW} = \frac{1}{1.4 \times 10^{-10} \times R_T - 1.95 \times 10^{-8}}$$

$$f_{SW} = \frac{1}{1.4 \times 10^{-10} \times 14.3\ k\Omega - 1.95 \times 10^{-8}} = 504\ kHz \quad (108)$$

The chosen component from step 2 is:

$$\boxed{R_T = 14.3\ k\Omega} \quad (109)$$

#### 8.2.2.2.3 Average LED Current

Solve for $R_{SNS}$:

## Typical Applications (continued)

$$R_{SNS} = \frac{V_{SNS}}{I_{LED}} = \frac{100\ mV}{1A} = 0.1\Omega \tag{110}$$

Assume $R_{CSH}$ = 12.4 kΩ and solve for $R_{HSP}$:

$$R_{HSP} = \frac{I_{LED}\ x\ R_{CSH}\ x\ R_{SNS}}{1.24V} = \frac{1A\ x\ 12.4\ k\Omega\ x\ 0.1\Omega}{1.24V} = 1.0\ k\Omega \tag{111}$$

The closest standard resistor for $R_{SNS}$ is actually 0.1Ω and for $R_{HSP}$ is actually 1 kΩ therefore $I_{LED}$ is:

$$I_{LED} = \frac{1.24V\ x\ R_{HSP}}{R_{SNS}\ x\ R_{CSH}} = \frac{1.24V\ x\ 1.0\ k\Omega}{0.1\Omega\ x\ 12.4\ k\Omega} = 1.0A \tag{112}$$

The chosen components from step 3 are:

$$\boxed{\begin{array}{l} R_{SNS} = 0.1\Omega \\ R_{CSH} = 12.4\ k\Omega \\ R_{HSP} = R_{HSN} = 1k\Omega \end{array}} \tag{113}$$

#### 8.2.2.2.4 Thermal Foldback

Find the resistances corresponding to $T_{BK}$ and $T_{END}$ ($R_{NTC\text{-}BK}$ = 24.3 kΩ and $R_{NTC\text{-}END}$ = 7.15 kΩ) from the manufacturer's datasheet. Assuming $R_{REF1}$ = $R_{REF2}$ = 49.9 kΩ, then $R_{BIAS}$ = $R_{NTC\text{-}BK}$= 24.3 kΩ.

Solve for $R_{GAIN}$:

$$R_{GAIN} = \frac{\left(\frac{R_{REF1}}{R_{REF1} + R_{REF2}} - \frac{R_{NTC\text{-}END}}{R_{NTC\text{-}END} + R_{BIAS}}\right) x\ 2.45V}{I_{CSH}}$$

$$R_{GAIN} = \frac{\left(\frac{1}{2} - \frac{7.15\ k\Omega}{7.15\ k\Omega + 24.3k\Omega}\right) x\ 2.45V}{100\ \mu A} = 6.68\ k\Omega \tag{114}$$

The chosen components from step 4 are:

$$\boxed{\begin{array}{l} R_{GAIN} = 6.81\ k\Omega \\ R_{BIAS} = 24.3\ k\Omega \\ R_{REF1} = R_{REF2} = 49.9\ k\Omega \end{array}} \tag{115}$$

#### 8.2.2.2.5 Inductor Ripple Current

Solve for L1:

$$L1 = \frac{V_{IN}\ x\ D}{\Delta i_{L\text{-}PP}\ x\ f_{SW}} = \frac{24V\ x\ 0.467}{700\ mA\ x\ 504\ kHz} = 32\ \mu H \tag{116}$$

The closest standard inductor is 33 µH therefore $\Delta i_{L\text{-}PP}$ is:

$$\Delta i_{L\text{-}PP} = \frac{V_{IN}\ x\ D}{L1\ x\ f_{SW}} = \frac{24V\ x\ 0.467}{33\ \mu H\ x\ 504\ kHz} = 674\ mA \tag{117}$$

Determine minimum allowable RMS current rating:

$$I_{L\text{-}RMS} = \frac{I_{LED}}{D'}\ x \sqrt{1 + \frac{1}{12}\ x \left(\frac{\Delta i_{L\text{-}PP}\ x\ D'}{I_{LED}}\right)^2}$$

$$I_{L\text{-}RMS} = \frac{1A}{0.533}\ x \sqrt{1 + \frac{1}{12}\ x \left(\frac{674\ mA\ x\ 0.533}{1A}\right)^2} = 1.89A \tag{118}$$

The chosen component from step 5 is:

## Typical Applications (continued)

$$\boxed{L1 = 33\,\mu H} \quad (119)$$

#### 8.2.2.2.6 Output Capacitance

Solve for $C_O$:

$$C_O = \frac{I_{LED} \times D}{r_D \times \Delta i_{LED\text{-}PP} \times f_{SW}}$$

$$C_O = \frac{1A \times 0.467}{1.95\Omega \times 12\ mA \times 504\ kHz} = 39.6\,\mu F \quad (120)$$

The closest capacitance totals 40 µF therefore $\Delta i_{LED\text{-}PP}$ is:

$$\Delta i_{LED\text{-}PP} = \frac{I_{LED} \times D}{r_D \times C_O \times f_{SW}}$$

$$\Delta i_{LED\text{-}PP} = \frac{1A \times 0.467}{1.95\Omega \times 40\,\mu F \times 504\ kHz} = 12\ mA \quad (121)$$

Determine minimum allowable RMS current rating:

$$I_{CO\text{-}RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 1A \times \sqrt{\frac{0.677}{1 - 0.677}} = 1.45A \quad (122)$$

The chosen components from step 6 are:

$$\boxed{C_O = 4 \times 10\,\mu F} \quad (123)$$

#### 8.2.2.2.7 Peak Current Limit

Solve for $R_{LIM}$:

$$R_{LIM} = \frac{245\ mV}{I_{LIM}} = \frac{245\ mV}{6A} = 0.041\Omega \quad (124)$$

The closest standard resistor is 0.04 Ω therefore $I_{LIM}$ is:

$$I_{LIM} = \frac{245\ mV}{R_{LIM}} = \frac{245\ mV}{0.04\Omega} = 6.13A \quad (125)$$

The chosen component from step 7 is:

$$\boxed{R_{LIM} = 0.04\Omega} \quad (126)$$

#### 8.2.2.2.8 Slope Compensation

Solve for $R_{SLP}$:

$$R_{SLP} = \frac{1.5 \times 10^{13} \times L1}{V_O \times R_T \times R_{LIM}}$$

$$R_{SLP} = \frac{1.5e^{13} \times 33\,\mu H}{21\ V \times 14.3\ k\Omega \times 0.04\ \Omega} = 41.2\ k\Omega \quad (127)$$

The chosen component from step 8 is:

$$\boxed{R_{SLP} = 41.2\ k\Omega} \quad (128)$$

#### 8.2.2.2.9 Loop Compensation

$\omega_{P1}$ is approximated:

$$\omega_{P1} = \frac{1 + D}{r_D \times C_O} = \frac{1.467}{1.95\Omega \times 40\,\mu F} = 19k\frac{rad}{sec} \quad (129)$$

## Typical Applications (continued)

$\omega_{Z1}$ is approximated:

$$\omega_{Z1} = \frac{r_D \times D'^2}{D \times L1} = \frac{1.95\Omega \times 0.533^2}{0.467 \times 33\mu H} = 36k\frac{rad}{sec} \tag{130}$$

$T_{U0}$ is approximated:

$$T_{U0} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} = \frac{0.533 \times 620V}{1.467 \times 1A \times 0.04\Omega} = 5630 \tag{131}$$

To ensure stability, calculate $\omega_{P2}$:

$$\omega_{P2} = \frac{\min(\omega_{P1}, \omega_{Z1})}{5 \times T_{U0}} = \frac{\omega_{P1}}{5 \times 5630} = \frac{19k\frac{rad}{sec}}{5 \times 5630} = 0.675\frac{rad}{sec} \tag{132}$$

Solve for $C_{CMP}$:

$$C_{CMP} = \frac{1}{\omega_{P2} \times 5 \times 10^6\Omega} = \frac{1}{0.675\frac{rad}{sec} \times 5 \times 10^6\Omega} = 0.30\mu F \tag{133}$$

To attenuate switching noise, calculate $\omega_{P3}$:

$$\omega_{P3} = (\max \omega_{P1}, \omega_{Z1}) \times 10 = \omega_{Z1} \times 10$$

$$\omega_{P3} = 36k\frac{rad}{sec} \times 10 = 360k\frac{rad}{sec} \tag{134}$$

Assume $R_{FS}$ = 10Ω and solve for $C_{FS}$:

$$C_{FS} = \frac{1}{10\Omega \times \omega_{P3}} = \frac{1}{10\Omega \times 360k\frac{rad}{sec}} = 0.28\ \mu F \tag{135}$$

The chosen components from step 9 are:

$$\boxed{\begin{array}{l} C_{CMP} = 0.33\ \mu F \\ R_{FS} = 10\Omega \\ C_{FS} = 0.27\mu F \end{array}} \tag{136}$$

#### 8.2.2.2.10 Input Capacitance

Solve for the minimum $C_{IN}$:

$$C_{IN} = \frac{I_{LED} \times D}{\Delta v_{IN\text{-}PP} \times f_{SW}} = \frac{1A \times 0.467}{100\ mV \times 504\ kHz} = 9.27\ \mu F \tag{137}$$

To minimize power supply interaction a 200% larger capacitance of approximately 20 µF is used, therefore the actual $\Delta v_{IN\text{-}PP}$ is much lower. Since high voltage ceramic capacitor selection is limited, four 4.7 µF X7R capacitors are chosen.

Determine minimum allowable RMS current rating:

$$I_{IN\text{-}RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 1A \times \sqrt{\frac{0.677}{1 - 0.677}} = 1.45A \tag{138}$$

The chosen components from step 10 are:

$$\boxed{C_{IN} = 4 \times 4.7\ \mu F} \tag{139}$$

#### 8.2.2.2.11 NFET

Determine minimum Q1 voltage rating and current rating:

$$V_{T\text{-}MAX} = V_{IN\text{-}MAX} + V_O = 70V + 21V = 91V \tag{140}$$

## Typical Applications (continued)

$$I_{T\text{-}MAX} = \frac{0.677}{1 - 0.677} \times 1A = 2.1A \quad (141)$$

A 100V NFET is chosen with a current rating of 32A due to the low $R_{DS\text{-}ON}$ = 50 mΩ. Determine $I_{T\text{-}RMS}$ and $P_T$:

$$I_{T\text{-}RMS} = \frac{I_{LED}}{D'} \times \sqrt{D} = \frac{1A}{0.533} \times \sqrt{0.467} = 1.28A \quad (142)$$

$$P_T = I_{T\text{-}RMS}^2 \times R_{DSON} = 1.28A^2 \times 50\,m\Omega = 82\,mW \quad (143)$$

The chosen component from step 11 is:

$$\boxed{Q1 \rightarrow 32A,\ 100V,\ DPAK} \quad (144)$$

#### 8.2.2.2.12 Diode

Determine minimum D1 voltage rating and current rating:

$$V_{RD\text{-}MAX} = V_{IN\text{-}MAX} + V_O = 70V + 21V = 91V \quad (145)$$

$$I_{D\text{-}MAX} = I_{LED} = 1A \quad (146)$$

A 100V diode is chosen with a current rating of 12A and $V_{DF}$ = 600 mV. Determine $P_D$:

$$P_D = I_D \times V_{FD} = 1A \times 600\,mV = 600\,mW \quad (147)$$

The chosen component from step 12 is:

$$\boxed{D1 \rightarrow 12A,\ 100V,\ DPAK} \quad (148)$$

#### 8.2.2.2.13 Input UVLO

Solve for $R_{UV2}$:

$$R_{UV2} = \frac{V_{HYS}}{20\,\mu A} = \frac{3V}{20\,\mu A} = 150\,k\Omega \quad (149)$$

The closest standard resistor is 150 kΩ therefore $V_{HYS}$ is:

$$V_{HYS} = R_{UV2} \times 20\,\mu A = 150\,k\Omega \times 20\,\mu A = 3V \quad (150)$$

Solve for $R_{UV1}$:

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN\text{-}ON} - 1.24V} = \frac{1.24V \times 150\,k\Omega}{10V - 1.24V} = 21.2\,k\Omega \quad (151)$$

The closest standard resistor is 21 kΩ making $V_{TURN\text{-}ON}$:

$$V_{TURN\text{-}ON} = \frac{1.24V \times (R_{UV1} + R_{UV2})}{R_{UV1}}$$

$$V_{TURN\text{-}ON} = \frac{1.24V \times (21\,k\Omega + 150\,k\Omega)}{21\,k\Omega} = 10.1V \quad (152)$$

The chosen components from step 13 are:

$$\boxed{\begin{array}{l} R_{UV1} = 21\,k\Omega \\ R_{UV2} = 150\,k\Omega \end{array}} \quad (153)$$

#### 8.2.2.2.14 Output OVLO

Solve for $R_{OV2}$:

$$R_{OV2} = \frac{V_{HYSO}}{20\,\mu A} = \frac{10V}{20\,\mu A} = 500\,k\Omega \quad (154)$$

The closest standard resistor is 499 kΩ therefore $V_{HYSO}$ is:

## Typical Applications (continued)

$$V_{HYSO} = R_{OV2} \times 20\mu A = 499\,k\Omega \times 20\mu A = 9.98V \tag{155}$$

Solve for $R_{OV1}$:

$$R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN\text{-}OFF} - 0.62V} = \frac{1.24V \times 499\,k\Omega}{40V - 0.62V} = 15.7\,k\Omega \tag{156}$$

The closest standard resistor is 15.8 kΩ making $V_{TURN\text{-}OFF}$:

$$V_{TURN\text{-}OFF} = \frac{1.24V \times (0.5 \times R_{OV1} + R_{OV2})}{R_{OV1}}$$

$$V_{TURN\text{-}OFF} = \frac{1.24V \times (0.5 \times 15.8\,k\Omega + 499\,k\Omega)}{15.8\,k\Omega} = 39.8V \tag{157}$$

The chosen components from step 14 are:

$$\boxed{\begin{array}{l} R_{OV1} = 15.8\,k\Omega \\ R_{OV2} = 499\,k\Omega \end{array}} \tag{158}$$

#### 8.2.2.2.15 Soft-Start

Solve for $t_{SU}$:

$$t_{SU} = 168\Omega \times C_{BYP} + 36\,k\Omega \times C_{CMP} + \frac{V_O}{I_{LED}} \times C_O$$

$$t_{SU} = 168\Omega \times 2.2\,\mu F + 36\,k\Omega \times 0.33\,\mu F + \frac{21V}{1A} \times 40\,\mu F$$

$$t_{SU} = 13.1\text{ ms} \tag{159}$$

If $t_{SU}$ is less than $t_{TSU}$, solve for $t_{SU\text{-}SS\text{-}BASE}$:

$$t_{SU\text{-}SS\text{-}BASE} = 168\Omega \times C_{BYP} + 28\,k\Omega \times C_{CMP} + \frac{V_O}{I_{LED}} \times C_O$$

$$t_{SU\text{-}SS\text{-}BASE} = 168\Omega \times 2.2\,\mu F + 28\,k\Omega \times 0.33\,\mu F + \frac{21V}{1A} \times 40\,\mu F$$

$$t_{SU\text{-}SS\text{-}BASE} = 10.5\text{ ms} \tag{160}$$

Solve for $C_{SS}$:

$$C_{SS} = \frac{(t_{TSU} - t_{SU\text{-}SS\text{-}BASE})}{20\,k\Omega} = \frac{(30\text{ ms} - 10.5\text{ ms})}{20\,k\Omega} = 975\text{ nF} \tag{161}$$

The chosen component from step 15 is:

$$\boxed{C_{SS} = 1\mu F} \tag{162}$$

**Table 1. Bill of Materials**

| QTY | PART ID | PART VALUE | MANUFACTURER | PART NUMBER |
|---|---|---|---|---|
| 1 | LM3424 | Boost controller | TI | LM3424MH |
| 1 | $C_{BYP}$ | 2.2 µF X7R 10% 16V | MURATA | GRM21BR71C225KA12L |
| 2 | $C_{CMP}$, $C_{NTC}$ | 0.33 µF X7R 10% 25V | MURATA | GRM21BR71E334KA01L |
| 1 | $C_{FS}$ | 0.27 µF X7R 10% 25V | MURATA | GRM21BR71E274KA01L |
| 4 | $C_{IN}$ | 4.7 µF X7R 10% 100V | TDK | C5750X7R2A475K |
| 4 | $C_O$ | 10 µF X7R 10% 50V | TDK | C4532X7R1H106K |
| 1 | $C_{OV}$ | 47 pF COG/NPO 5% 50V | AVX | 08055A470JAT2A |
| 1 | $C_{REF}$, $C_{SS}$ | 1 µF X7R 10% 25V | MURATA | GRM21BR71E105KA01L |

## Typical Applications (continued)

**Table 1. Bill of Materials (continued)**

| QTY | PART ID | PART VALUE | MANUFACTURER | PART NUMBER |
|---|---|---|---|---|
| 1 | D1 | Schottky 100V 12A | VISHAY | 12CWQ10FNPBF |
| 1 | L1 | 33 µH 20% 6.3A | COILCRAFT | MSS1278-333MLB |
| 1 | Q1 | NMOS 100V 32A | FAIRCHILD | FDD3682 |
| 1 | Q2 | PNP 150V 600 mA | FAIRCHILD | MMBT5401 |
| 1 | $R_{BIAS}$ | 24.3 kΩ 1% | VISHAY | CRCW080524K3FKEA |
| 1 | $R_{CSH}$ | 12.4 kΩ 1% | VISHAY | CRCW080512K4FKEA |
| 1 | $R_{FS}$ | 10Ω 1% | VISHAY | CRCW080510R0FKEA |
| 1 | $R_{GAIN}$ | 6.81 kΩ 1% | VISHAY | CRCW08056K81FKEA |
| 2 | $R_{HSP}$, $R_{HSN}$ | 1.0 kΩ 1% | VISHAY | CRCW08051K00FKEA |
| 1 | $R_{LIM}$ | 0.04Ω 1% 1W | VISHAY | WSL2512R0400FEA |
| 1 | $R_{OV1}$ | 15.8 kΩ 1% | VISHAY | CRCW080515K8FKEA |
| 1 | $R_{OV2}$ | 499 kΩ 1% | VISHAY | CRCW0805499KFKEA |
| 2 | $R_{REF1}$, $R_{REF2}$ | 49.9 kΩ 1% | VISHAY | CRCW080549K9FKEA |
| 1 | $R_{SLP}$ | 16.5 kΩ 1% | VISHAY | CRCW080516K5FKEA |
| 1 | $R_{SNS}$ | 0.1Ω 1% 1W | VISHAY | WSL2512R1000FEA |
| 1 | $R_T$ | 14.3 kΩ 1% | VISHAY | CRCW080514K3FKEA |
| 1 | $R_{UV1}$ | 21 kΩ 1% | VISHAY | CRCW080521K0FKEA |
| 1 | $R_{UV2}$ | 150 kΩ 1% | VISHAY | CRCW0805150KFKEA |
| 1 | NTC | Thermistor 100 kΩ 5% | TDK | NTCG204H154J |

### *8.2.2.3 Application Curve*

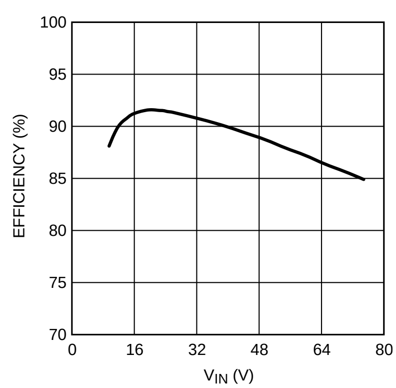



**Figure 40. Efficiency vs. Input Voltage**

### 8.2.3 Boost Application

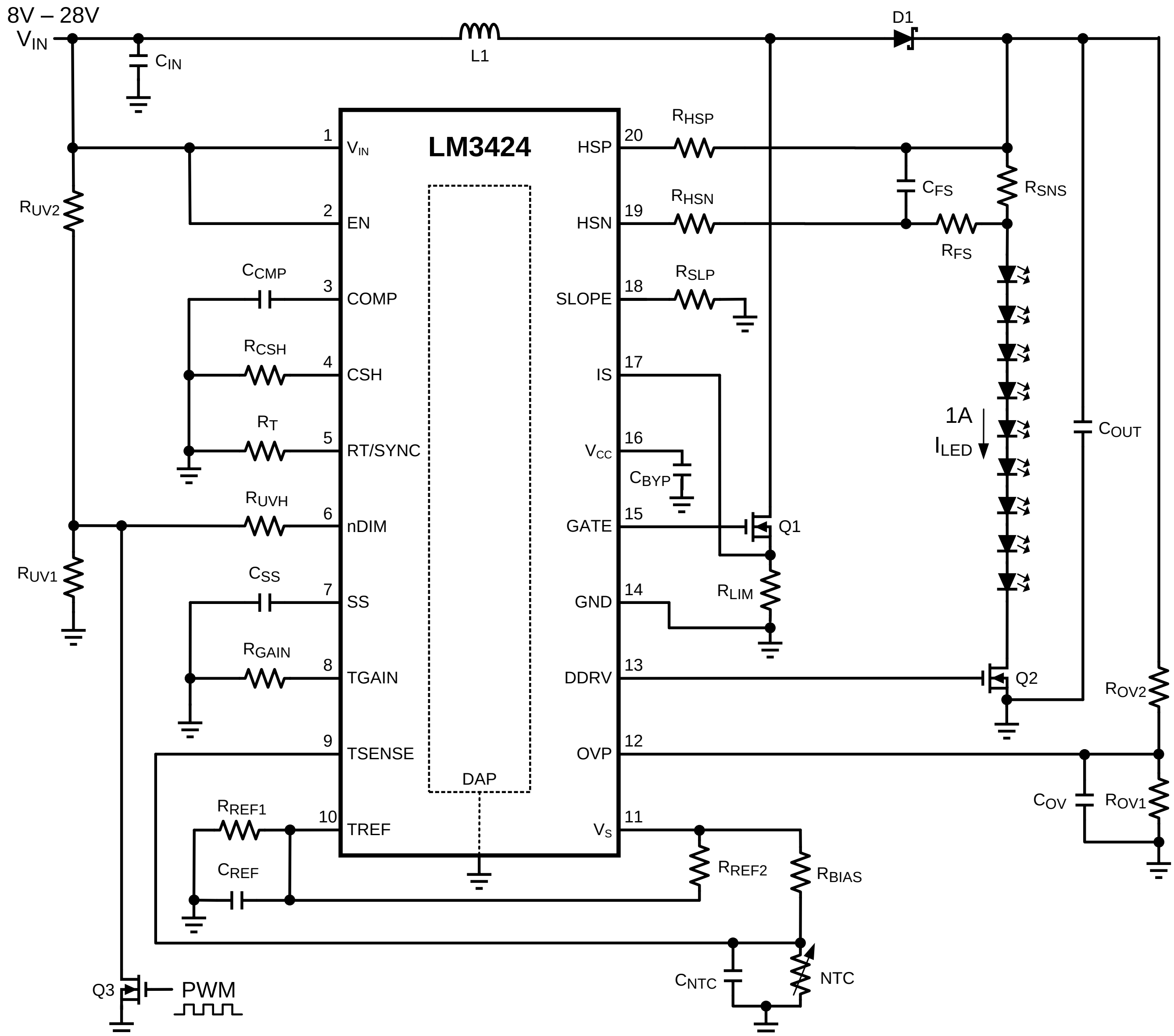



**Figure 41. Boost Application**

#### *8.2.3.1 Design Requirements*

- Input: 8 V to 28 V
- Output: 9 LEDs at 1A
- 65°C - 100°C Thermal Foldback
- PWM Dimming up to 30 kHz
- 700 kHz Switching Frequency

### 8.2.3.2 Detailed Design Procedure

**Table 2. Bill of Materials**

| QTY | PART ID | PART VALUE | MANUFACTURER | PART NUMBER |
|---|---|---|---|---|
| 1 | LM3424 | Boost controller | TI | LM3424MH |
| 1 | $C_{BYP}$ | 2.2 µF X7R 10% 16V | MURATA | GRM21BR71C225KA12L |
| 1 | $C_{CMP}$ | 0.1 µF X7R 10% 25V | MURATA | GRM21BR71E104KA01L |
| 0 | $C_{FS}$ | DNP | | |
| 4 | $C_{IN}$ | 4.7 µF X7R 10% 100V | TDK | C5750X7R2A475K |
| 4 | $C_{OUT}$ | 10 µF X7R 10% 50V | TDK | C4532X7R1H106K |
| 1 | $C_{OV}$ | 47 pF COG/NPO 5% 50V | AVX | 08055A470JAT2A |
| 2 | $C_{NTC}$, $C_{SS}$ | 0.27 µF X7R 10% 25V | MURATA | GRM21BR71E274KA01L |
| 1 | $C_{REF}$ | 1 µF X7R 10% 25V | MURATA | GRM21BR71E105KA01L |
| 1 | D1 | Schottky 60V 5A | COMCHIP | CDBC560-G |
| 1 | L1 | 33 µH 20% 6.3A | COILCRAFT | MSS1278-333MLB |
| 2 | Q1, Q2 | NMOS 60V 8A | VISHAY | SI4436DY |
| 1 | Q3 | NMOS 60V 115mA | ON-SEMI | 2N7002ET1G |
| 1 | $R_{BIAS}$ | 19.6 kΩ 1% | VISHAY | CRCW080519K6FKEA |
| 2 | $R_{CSH}$, $R_{OV1}$ | 12.4 kΩ 1% | VISHAY | CRCW080512K4FKEA |
| 1 | $R_{FS}$ | 0Ω 1% | VISHAY | CRCW08050000Z0EA |
| 1 | $R_{GAIN}$ | 6.49 kΩ 1% | VISHAY | CRCW08056K49FKEA |
| 2 | $R_{HSP}$, $R_{HSN}$ | 1.0 kΩ 1% | VISHAY | CRCW08051K00FKEA |
| 1 | $R_{LIM}$ | 0.06Ω 1% 1W | VISHAY | WSL2512R0600FEA |
| 1 | $R_{OV2}$ | 499 kΩ 1% | VISHAY | CRCW0805499KFKEA |
| 2 | $R_{REF1}$, $R_{REF2}$ | 49.9 kΩ 1% | VISHAY | CRCW080549K9FKEA |
| 1 | $R_{SNS}$ | 0.1Ω 1% 1W | VISHAY | WSL2512R1000FEA |
| 2 | $R_{SLP}$, $R_{UV2}$ | 10.0 kΩ 1% | VISHAY | CRCW080510K0FKEA |
| 1 | $R_T$ | 14.3 kΩ 1% | VISHAY | CRCW080514K3FKEA |
| 1 | $R_{UV1}$ | 1.82 kΩ 1% | VISHAY | CRCW08051K82FKEA |
| 1 | $R_{UVH}$ | 17.8 kΩ 1% | VISHAY | CRCW080517K8FKEA |
| 1 | NTC | Thermistor 100 kΩ 5% | TDK | NTCG204H154J |

### 8.2.4 Buck-Boost Application

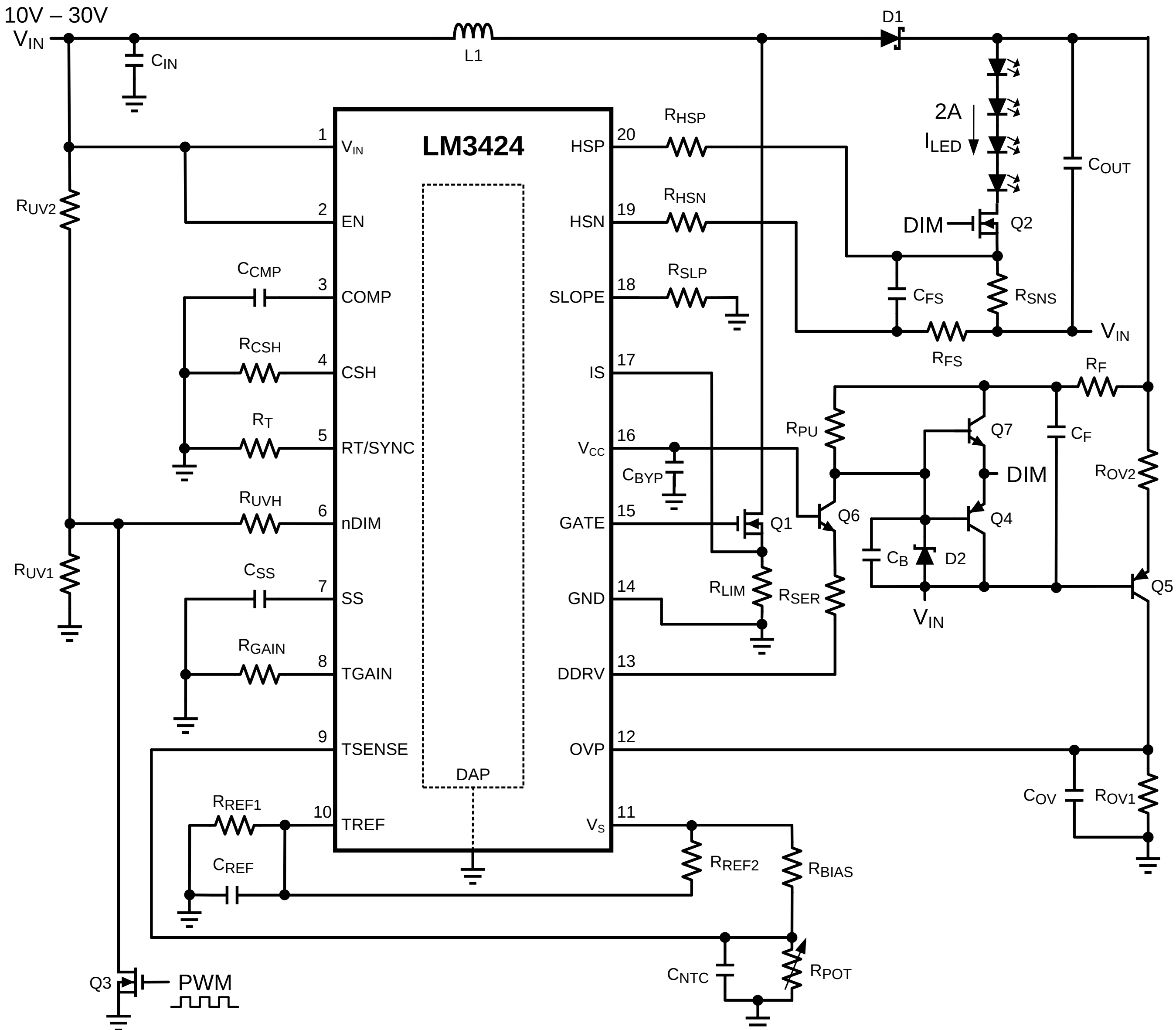



**Figure 42. Buck-Boost Application**

#### *8.2.4.1 Design Requirements*

- Input: 10V to 30V
- Output: 4 LEDs at 2A
- PWM Dimming up to 10 kHz
- Analog Dimming
- 600-kHz Switching Frequency

### *8.2.4.2 Detailed Design Procedures*

**Table 3. Bill of Materials**

| QTY | PART ID | PART VALUE | MANUFACTURER | PART NUMBER |
|---|---|---|---|---|
| 1 | LM3424 | Boost controller | TI | LM3424MH |
| 1 | $C_B$ | 100 pF COG/NPO 5% 50V | MURATA | GRM2165C1H101JA01D |
| 1 | $C_{BYP}$ | 2.2 µF X7R 10% 16V | MURATA | GRM21BR71C225KA12L |
| 3 | $C_{CMP}$, $C_{REF}$, $C_{SS}$ | 1 µF X7R 10% 25V | MURATA | GRM21BR71E105KA01L |
| 1 | $C_F$ | 0.1 µF X7R 10% 25V | MURATA | GRM21BR71E104KA01L |
| 0 | $C_{FS}$ | DNP | | |
| 4 | $C_{IN}$ | 6.8 µF X7R 10% 50V | TDK | C5750X7R1H685K |
| 1 | $C_{NTC}$ | 0.47 µF X7R 10% 25V | MURATA | GRM21BR71E474KA01L |
| 4 | $C_{OUT}$ | 10 µF X7R 10% 50V | TDK | C4532X7R1H106K |
| 1 | $C_{OV}$ | 47 pF COG/NPO 5% 50V | AVX | 08055A470JAT2A |
| 1 | D1 | Schottky 100V 12A | VISHAY | 12CWQ10FNPBF |
| 1 | D2 | Zener 10V 500mA | ON-SEMI | BZX84C10LT1G |
| 1 | L1 | 22 µH 20% 7.2A | COILCRAFT | MSS1278-223MLB |
| 2 | Q1, Q2 | NMOS 60V 8A | VISHAY | SI4436DY |
| 1 | Q3 | NMOS 60V 260mA | ON-SEMI | 2N7002ET1G |
| 1 | Q4 | PNP 40V 200 mA | FAIRCHILD | MMBT5087 |
| 1 | Q5 | PNP 150V 600 mA | FAIRCHILD | MMBT5401 |
| 1 | Q6 | NPN 300V 600 mA | FAIRCHILD | MMBTA42 |
| 1 | Q7 | NPN 40V 200 mA | FAIRCHILD | MMBT6428 |
| 3 | $R_{BIAS}$, $R_{REF1}$, $R_{REF2}$ | 49.9 kΩ 1% | VISHAY | CRCW080549K9FKEA |
| 2 | $R_{CSH}$, $R_T$ | 12.4 kΩ 1% | VISHAY | CRCW080512K4FKEA |
| 1 | $R_F$ | 10Ω 1% | VISHAY | CRCW080510R0FKEA |
| 1 | $R_{FS}$ | 0Ω 1% | VISHAY | CRCW08050000Z0EA |
| 2 | $R_{GAIN}$, $R_{UV2}$ | 10.0 kΩ 1% | VISHAY | CRCW080510K0FKEA |
| 2 | $R_{HSP}$, $R_{HSN}$ | 1.0 kΩ 1% | VISHAY | CRCW08051K00FKEA |
| 1 | $R_{LIM}$ | 0.04Ω 1% 1W | VISHAY | WSL2512R0400FEA |
| 1 | $R_{OV1}$ | 18.2 kΩ 1% | VISHAY | CRCW080518K2FKEA |
| 1 | $R_{OV2}$ | 499 kΩ 1% | VISHAY | CRCW0805499KFKEA |
| 1 | $R_{POT}$ | 50 kΩ potentiometer | BOURNS | 3352P-1-503 |
| 1 | $R_{PU}$ | 4.99 kΩ 1% | VISHAY | CRCW08054K99FKEA |
| 1 | $R_{SER}$ | 499Ω 1% | VISHAY | CRCW0805499RFKEA |
| 1 | $R_{SLP}$ | 34.0 kΩ 1% | VISHAY | CRCW080534K0FKEA |
| 1 | $R_{SNS}$ | 0.05Ω 1% 1W | VISHAY | WSL2512R0500FEA |
| 1 | $R_{UV1}$ | 1.43 kΩ 1% | VISHAY | CRCW08051K43FKEA |
| 1 | $R_{UVH}$ | 17.4 kΩ 1% | VISHAY | CRCW080517K4FKEA |

### 8.2.5 Boost Application

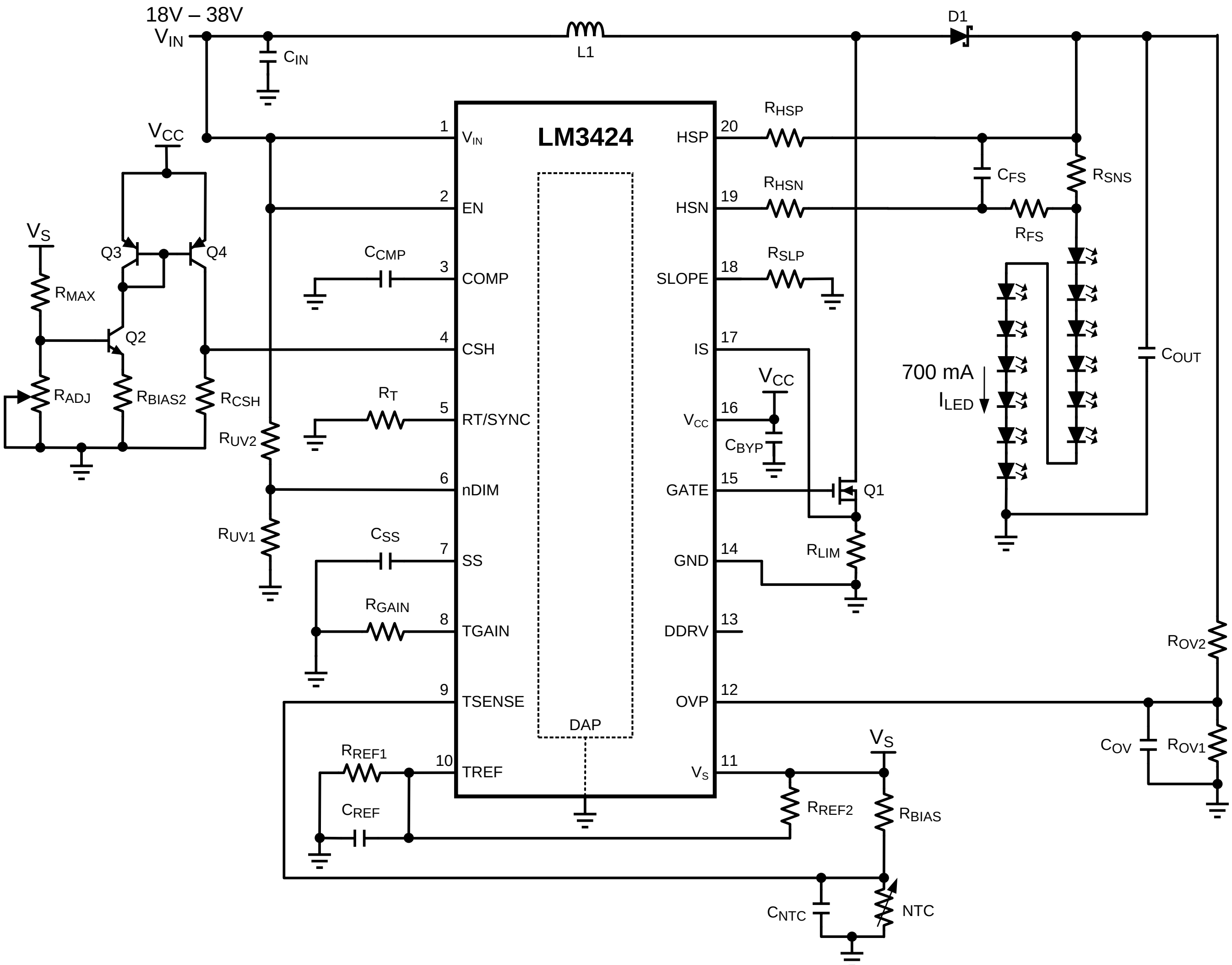



**Figure 43. Boost Application**

#### *8.2.5.1 Design Requirements*

- Input: 18V to 38V
- Output: 12 LEDs at 700mA
- 85°C - 125°C Thermal Foldback
- Analog Dimming
- 700 kHz Switching Frequency

### 8.2.5.2 Detailed Design Procedure

**Table 4. Bill of Materials**

| QTY | PART ID | PART VALUE | MANUFACTURER | PART NUMBER |
|---|---|---|---|---|
| 1 | LM3424 | Boost controller | TI | LM3424MH |
| 1 | $C_{BYP}$ | 2.2 µF X7R 10% 16V | MURATA | GRM21BR71C225KA12L |
| 3 | $C_{CMP}$, $C_{REF}$, $C_{SS}$ | 1 µF X7R 10% 25V | MURATA | GRM21BR71E105KA01L |
| 1 | $C_{NTC}$ | 0.33 µF X7R 10% 25V | MURATA | GRM21BR71E334KA01L |
| 1 | $C_{FS}$ | 0.1 µF X7R 10% 25V | MURATA | GRM21BR71E104KA01L |
| 4 | $C_{IN}$ | 4.7 µF X7R 10% 100V | TDK | C5750X7R2A475K |
| 4 | $C_{OUT}$ | 10 µF X7R 10% 50V | TDK | C4532X7R1H106K |
| 1 | $C_{OV}$ | 47 pF COG/NPO 5% 50V | AVX | 08055A470JAT2A |
| 1 | D1 | Schottky 60V 5A | COMCHIP | CDBC560-G |
| 1 | L1 | 47 µH 20% 5.3A | COILCRAFT | MSS1278-473MLB |
| 1 | Q1 | NMOS 60V 8A | VISHAY | SI4436DY |
| 1 | Q2 | NPN 40V 200 mA | FAIRCHILD | MMBT3904 |
| 1 | Q3, Q4 (dual pack) | Dual PNP 40V 200mA | FAIRCHILD | FFB3906 |
| 1 | $R_{ADJ}$ | 100 kΩ potentiometer | BOURNS | 3352P-1-104 |
| 1 | $R_{BIAS}$ | 9.76 kΩ 1% | VISHAY | CRCW08059K76FKEA |
| 1 | $R_{BIAS2}$ | 17.4 kΩ 1% | VISHAY | CRCW080517K4FKEA |
| 3 | $R_{CSH}$, $R_{OV1}$, $R_{UV1}$ | 12.4 kΩ 1% | VISHAY | CRCW080512K4FKEA |
| 1 | $R_{FS}$ | 10Ω 1% | VISHAY | CRCW080510R0FKEA |
| 1 | $R_{GAIN}$ | 6.55 kΩ 1% | VISHAY | CRCW08056K55FKEA |
| 3 | $R_{HSP}$, $R_{HSN}$, $R_{MAX}$ | 1.0 kΩ 1% | VISHAY | CRCW08051K00FKEA |
| 1 | $R_{LIM}$ | 0.06Ω 1% 1W | VISHAY | WSL2512R0600FEA |
| 1 | $R_{OV2}$ | 499 kΩ 1% | VISHAY | CRCW0805499KFKEA |
| 2 | $R_{REF1}$, $R_{REF2}$ | 49.9 kΩ 1% | VISHAY | CRCW080549K9FKEA |
| 2 | $R_{SLP}$, $R_T$ | 10.0 kΩ 1% | VISHAY | CRCW080510K0FKEA |
| 1 | $R_{SNS}$ | 0.15Ω 1% 1W | VISHAY | WSL2512R1500FEA |
| 1 | $R_{UV2}$ | 100 kΩ 1% | VISHAY | CRCW0805100KFKEA |
| 1 | NTC | Thermistor 100 kΩ 5% | TDK | NTCG204H154J |

### 8.2.6 Buck-Boost Application

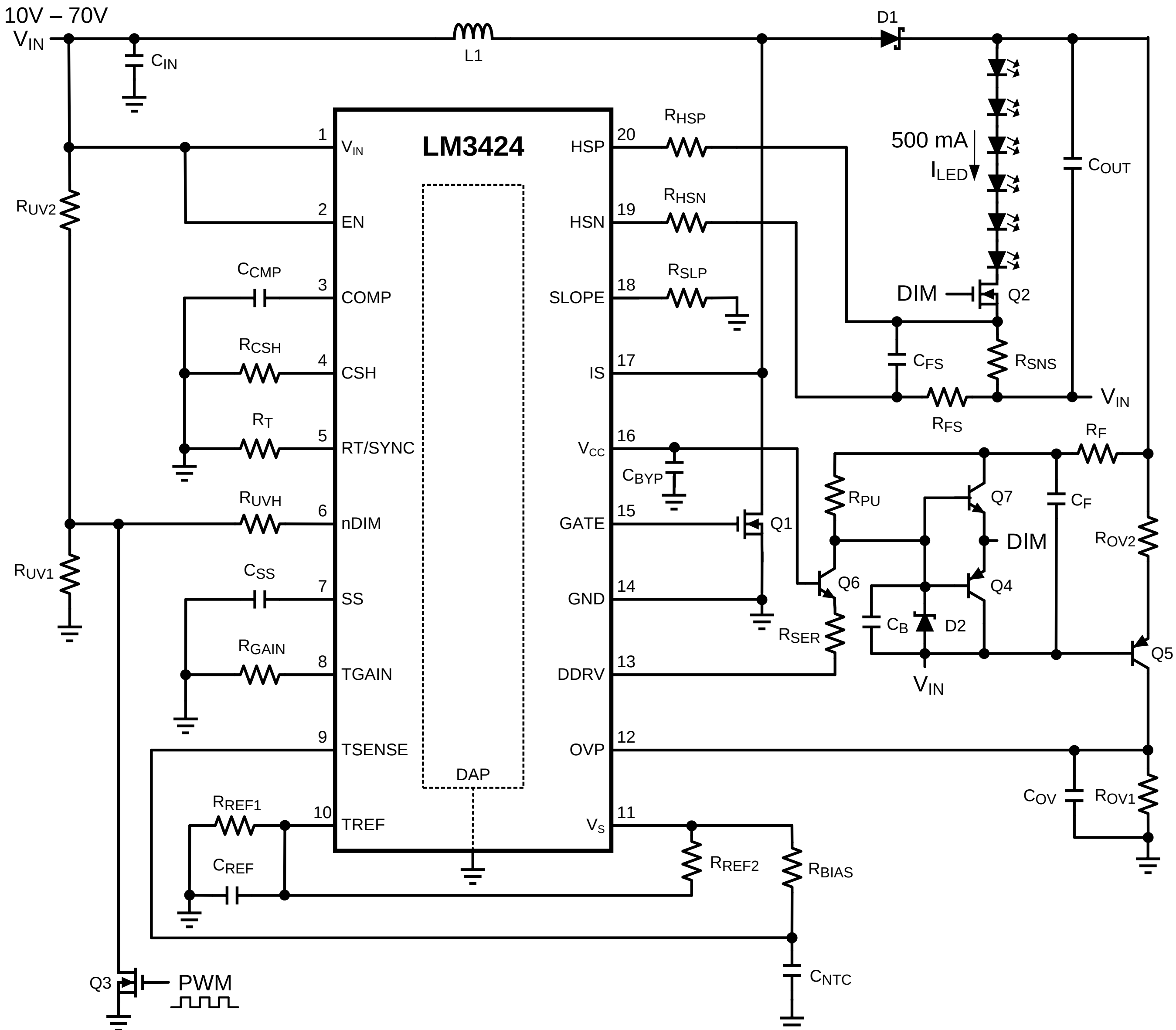



**Figure 44. Buck-Boost Application**

#### *8.2.6.1 Design Requirements*

- Input: 10 V to 70 V
- Output: 6 LEDs at 500 mA
- PWM Dimming up to 10 kHz
- 5-s Fade-up
- MOSFET $R_{DS\text{-}ON}$ Sensing
- 700-kHz Switching Frequency

### 8.2.6.2 Detailed Design Procedure

**Table 5. Bill of Materials**

| QTY | PART ID | PART VALUE | MANUFACTURER | PART NUMBER |
|---|---|---|---|---|
| 1 | LM3424 | Boost controller | TI | LM3424MH |
| 1 | $C_B$ | 100 pF COG/NPO 5% 50V | MURATA | GRM2165C1H101JA01D |
| 1 | $C_{BYP}$ | 2.2 µF X7R 10% 16V | MURATA | GRM21BR71C225KA12L |
| 2 | $C_{CMP}$, $C_{SS}$ | 1 µF X7R 10% 25V | MURATA | GRM21BR71E105KA01L |
| 1 | $C_{REF}$ | 0.01 µF X7R 10% 25V | MURATA | GRM21BR71E103KA01L |
| 1 | $C_F$ | 0.1 µF X7R 10% 25V | MURATA | GRM21BR71E104KA01L |
| 0 | $C_{FS}$ | DNP | | |
| 4 | $C_{IN}$ | 4.7 µF X7R 10% 100V | TDK | C5750X7R2A475K |
| 1 | $C_{NTC}$ | 10 µF X7R 10% 10V | MURATA | GRM21BR71A106KE51L |
| 4 | $C_{OUT}$ | 10 µF X7R 10% 50V | TDK | C4532X7R1H106K |
| 1 | $C_{OV}$ | 47 pF COG/NPO 5% 50V | AVX | 08055A470JAT2A |
| 1 | D1 | Schottky 100V 12A | VISHAY | 12CWQ10FNPBF |
| 1 | D2 | Zener 10V 500mA | ON-SEMI | BZX84C10LT1G |
| 1 | L1 | 68 µH 20% 4.3A | COILCRAFT | MSS1278-683MLB |
| 2 | Q1, Q2 | NMOS 100V 32A | FAIRCHILD | FDD3682 |
| 1 | Q3 | NMOS 60V 260mA | ON-SEMI | 2N7002ET1G |
| 1 | Q4 | PNP 40V 200mA | FAIRCHILD | MMBT5087 |
| 1 | Q5 | PNP 150V 600 mA | FAIRCHILD | MMBT5401 |
| 1 | Q6 | NPN 300V 600mA | FAIRCHILD | MMBTA42 |
| 1 | Q7 | NPN 40V 200mA | FAIRCHILD | MMBT6428 |
| 3 | $R_{BIAS}$, $R_{REF1}$, $R_{REF2}$ | 49.9 kΩ 1% | VISHAY | CRCW080549K9FKEA |
| 1 | $R_{CSH}$ | 12.4 kΩ 1% | VISHAY | CRCW080512K4FKEA |
| 1 | $R_{FS}$ | 0Ω 1% | VISHAY | CRCW08050000Z0EA |
| 3 | $R_{GAIN}$, $R_T$, $R_{UV2}$ | 10.0 kΩ 1% | VISHAY | CRCW080510K0FKEA |
| 2 | $R_{HSP}$, $R_{HSN}$ | 1.0 kΩ 1% | VISHAY | CRCW08051K00FKEA |
| 1 | $R_{OV1}$ | 15.8 kΩ 1% | VISHAY | CRCW080515K8FKEA |
| 1 | $R_{OV2}$ | 499 kΩ 1% | VISHAY | CRCW0805499KFKEA |
| 1 | $R_{PU}$ | 4.99 kΩ 1% | VISHAY | CRCW08054K99FKEA |
| 1 | $R_{SER}$ | 499Ω 1% | VISHAY | CRCW0805499RFKEA |
| 1 | $R_{SNS}$ | 0.2Ω 1% 1W | VISHAY | WSL2512R2000FEA |
| 1 | $R_{SLP}$ | 24.3 kΩ 1% | VISHAY | CRCW080524K3FKEA |
| 1 | $R_{UV1}$ | 1.43 kΩ 1% | VISHAY | CRCW08051K43FKEA |
| 1 | $R_{UVH}$ | 17.4 kΩ 1% | VISHAY | CRCW080517K4FKEA |

### 8.2.7 Buck Application

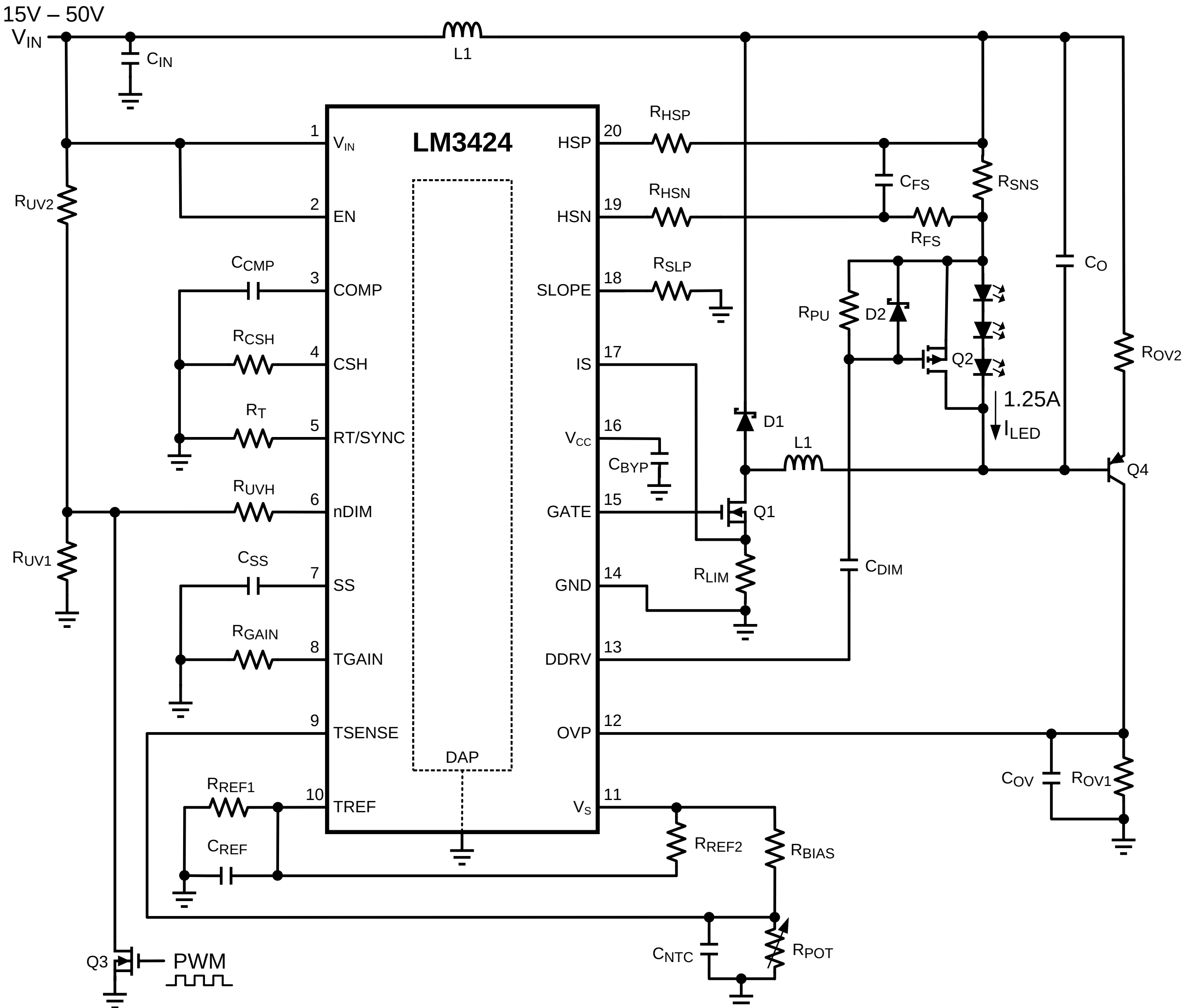



**Figure 45. Buck Application**

#### *8.2.7.1 Design Requirements*

- Input: 15 V to 50 V
- Output: 3 LEDS AT 1.25 A
- PWM Dimming up to 50 kHz
- Analog Dimming
- 700-kHz Switching Frequency

#### 8.2.7.2 Detailed Design Procedure

**Table 6. Bill of Materials**

| QTY | PART ID | PART VALUE | MANUFACTURER | PART NUMBER |
|---|---|---|---|---|
| 1 | LM3424 | Boost controller | TI | LM3424MH |
| 1 | $C_{BYP}$ | 2.2 µF X7R 10% 16V | MURATA | GRM21BR71C225KA12L |
| 2 | $C_{CMP}$, $C_{DIM}$ | 0.1 µF X7R 10% 25V | MURATA | GRM21BR71E104KA01L |
| 0 | $C_{FS}$ | DNP | | |
| 1 | $C_{NTC}$ | 0.33 µF X7R 10% 25V | MURATA | GRM21BR71E334KA01L |
| 4 | $C_{IN}$ | 4.7 µF X7R 10% 100V | TDK | C5750X7R2A475K |
| 0 | $C_{OUT}$ | DNP | | |
| 1 | $C_{OV}$ | 47 pF COG/NPO 5% 50V | AVX | 08055A470JAT2A |
| 1 | $C_{REF}$, $C_{SS}$ | 1 µF X7R 10% 25V | MURATA | GRM21BR71E105KA01L |
| 1 | D1 | Schottky 100V 12A | VISHAY | 12CWQ10FNPBF |
| 1 | D2 | Zener 10V 500mA | ON-SEMI | BZX84C10LT1G |
| 1 | L1 | 22 µH 20% 7.3A | COILCRAFT | MSS1278-223MLB |
| 1 | Q1 | NMOS 60V 8A | VISHAY | SI4436DY |
| 1 | Q2 | PMOS 30V 6.2A | VISHAY | SI3483DV |
| 1 | Q3 | NMOS 60V 115mA | ON-SEMI | 2N7002ET1G |
| 1 | Q4 | PNP 150V 600 mA | FAIRCHILD | MMBT5401 |
| 3 | $R_{BIAS}$, $R_{REF1}$, $R_{REF2}$ | 49.9 kΩ 1% | VISHAY | CRCW080549K9FKEA |
| 1 | $R_{CSH}$ | 12.4 kΩ 1% | VISHAY | CRCW080512K4FKEA |
| 1 | $R_{FS}$ | 0Ω 1% | VISHAY | CRCW08050000OZEA |
| 1 | $R_{GAIN}$, $R_T$ | 10.0 kΩ 1% | VISHAY | CRCW080510K0FKEA |
| 2 | $R_{HSP}$, $R_{HSN}$ | 1.0 kΩ 1% | VISHAY | CRCW08051K00FKEA |
| 1 | $R_{LIM}$ | 0.04Ω 1% 1W | VISHAY | WSL2512R0400FEA |
| 1 | $R_{OV1}$ | 21.5 kΩ 1% | VISHAY | CRCW080521K5FKEA |
| 1 | $R_{OV2}$ | 499 kΩ 1% | VISHAY | CRCW0805499KFKEA |
| 1 | $R_{POT}$ | 50 kΩ potentiometer | BOURNS | 3352P-1-503 |
| 2 | $R_{PU}$, $R_{UV2}$ | 100 kΩ 1% | VISHAY | CRCW0805100KFKEA |
| 1 | $R_{SLP}$ | 36.5 kΩ 1% | VISHAY | CRCW080536K5FKEA |
| 1 | $R_{SNS}$ | 0.08Ω 1% 1W | VISHAY | WSL2512R0800FEA |
| 1 | $R_{UV1}$ | 11.5 kΩ 1% | VISHAY | CRCW080511K5FKEA |

### 8.2.8 Buck-Boost Application

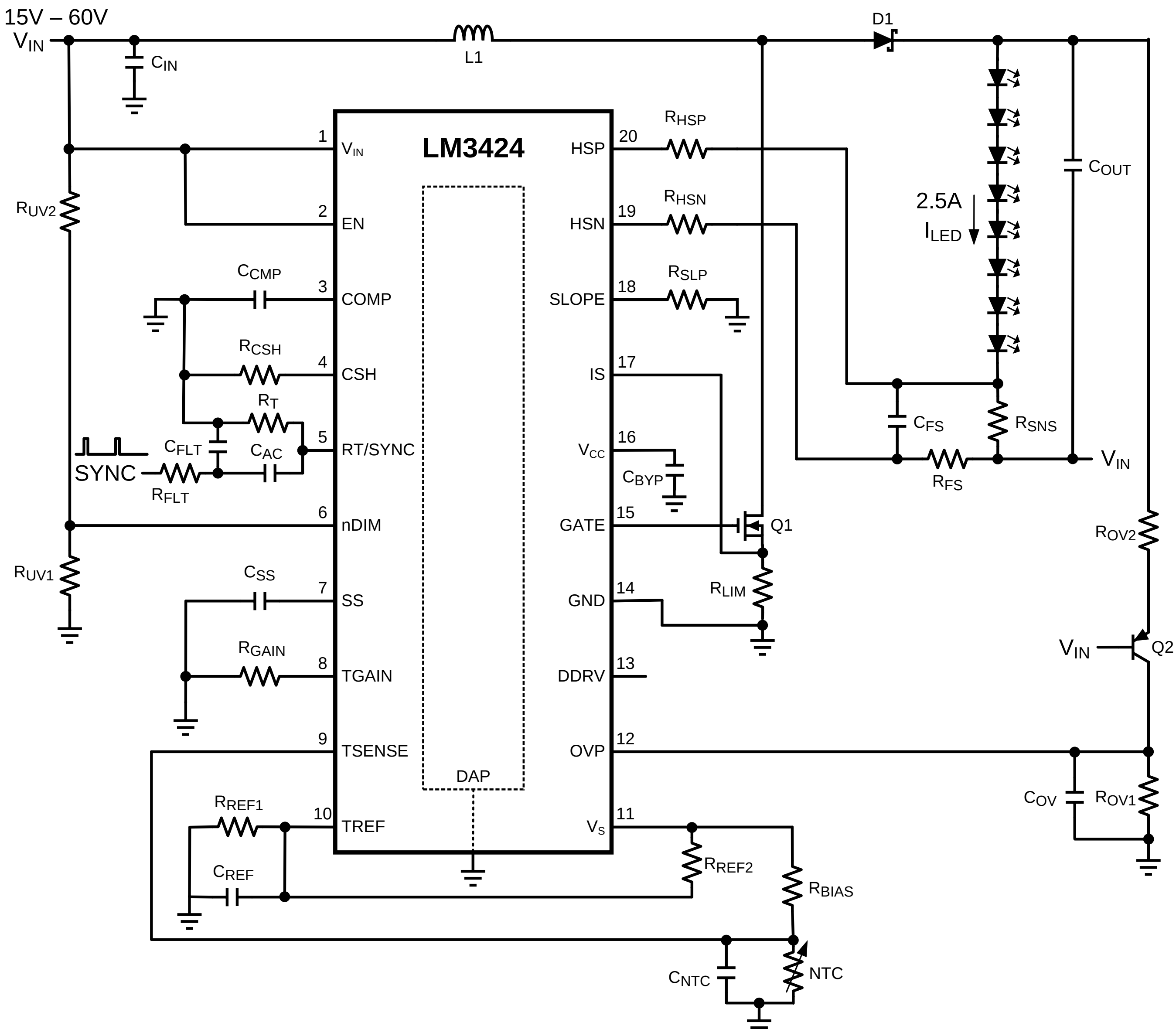



**Figure 46. Buck-Boost Application**

#### *8.2.8.1 Design Requirements*

- Input: 15 V to 60 V
- Output: 8 LEDs at 2.5 A
- 80°C to 110°C Thermal Foldback
- 500-kHz Switching Frequency
- External Synchronization > 500 kHz

### 8.2.8.2 Detailed Design Procedure

**Table 7. Bill of Materials**

| QTY | PART ID | PART VALUE | MANUFACTURER | PART NUMBER |
|---|---|---|---|---|
| 1 | LM3424 | Boost controller | TI | LM3424MH |
| 2 | $C_{AC}$, $C_{FLT}$ | 100 pF COG/NPO 5% 50V | MURATA | GRM2165C1H101JA01D |
| 1 | $C_{BYP}$ | 2.2 µF X7R 10% 16V | MURATA | GRM21BR71C225KA12L |
| 3 | $C_{CMP}$, $C_{NTC}$, $C_{SS}$ | 0.33 µF X7R 10% 25V | MURATA | GRM21BR71E334KA01L |
| 1 | $C_{FS}$ | 0.1 µF X7R 10% 25V | MURATA | GRM21BR71E104KA01L |
| 4 | $C_{IN}$ | 4.7 µF X7R 10% 100V | TDK | C5750X7R2A475K |
| 4 | $C_{OUT}$ | 10 µF X7R 10% 50V | TDK | C4532X7R1H106K |
| 1 | $C_{OV}$ | 47 pF COG/NPO 5% 50V | AVX | 08055A470JAT2A |
| 1 | $C_{REF}$ | 1 µF X7R 10% 25V | MURATA | GRM21BR71E105KA01L |
| 1 | D1 | Schottky 100V 12A | VISHAY | 12CWQ10FNPBF |
| 1 | L1 | 22 µH 20% 7.2A | COILCRAFT | MSS1278-223MLB |
| 1 | Q1 | NMOS 100V 32A | FAIRCHILD | FDD3682 |
| 1 | Q2 | PNP 150V 600 mA | FAIRCHILD | MMBT5401 |
| 1 | $R_{BIAS}$ | 11.5 kΩ 1% | VISHAY | CRCW080511K5FKEA |
| 2 | $R_{CSH}$, $R_{OV1}$ | 12.4 kΩ 1% | VISHAY | CRCW080512K4FKEA |
| 1 | $R_{FS}$ | 10Ω 1% | VISHAY | CRCW080510R0FKEA |
| 1 | $R_{FLT}$ | 150Ω 1% | VISHAY | CRCW0805150RFKEA |
| 1 | $R_{GAIN}$ | 5.49 kΩ 1% | VISHAY | CRCW08055K49FKEA |
| 2 | $R_{HSP}$, $R_{HSN}$ | 1.0 kΩ 1% | VISHAY | CRCW08051K00FKEA |
| 2 | $R_{LIM}$, $R_{SNS}$ | 0.04Ω 1% 1W | VISHAY | WSL2512R0400FEA |
| 1 | $R_{OV1}$ | 15.8 kΩ 1% | VISHAY | CRCW080515K8FKEA |
| 1 | $R_{OV2}$ | 499 kΩ 1% | VISHAY | CRCW0805499KFKEA |
| 2 | $R_{REF1}$, $R_{REF2}$ | 49.9 kΩ 1% | VISHAY | CRCW080549K9FKEA |
| 1 | $R_{SLP}$ | 20.5 kΩ 1% | VISHAY | CRCW080520K5FKEA |
| 1 | $R_T$ | 14.3 kΩ 1% | VISHAY | CRCW080514K3FKEA |
| 1 | $R_{UV1}$ | 13.7 kΩ 1% | VISHAY | CRCW080513K7FKEA |
| 1 | $R_{UV2}$ | 150 kΩ 1% | VISHAY | CRCW0805150KFKEA |
| 1 | NTC | Thermistor 100 kΩ 5% | TDK | NTCG204H154J |

### 8.2.9 SEPIC Application

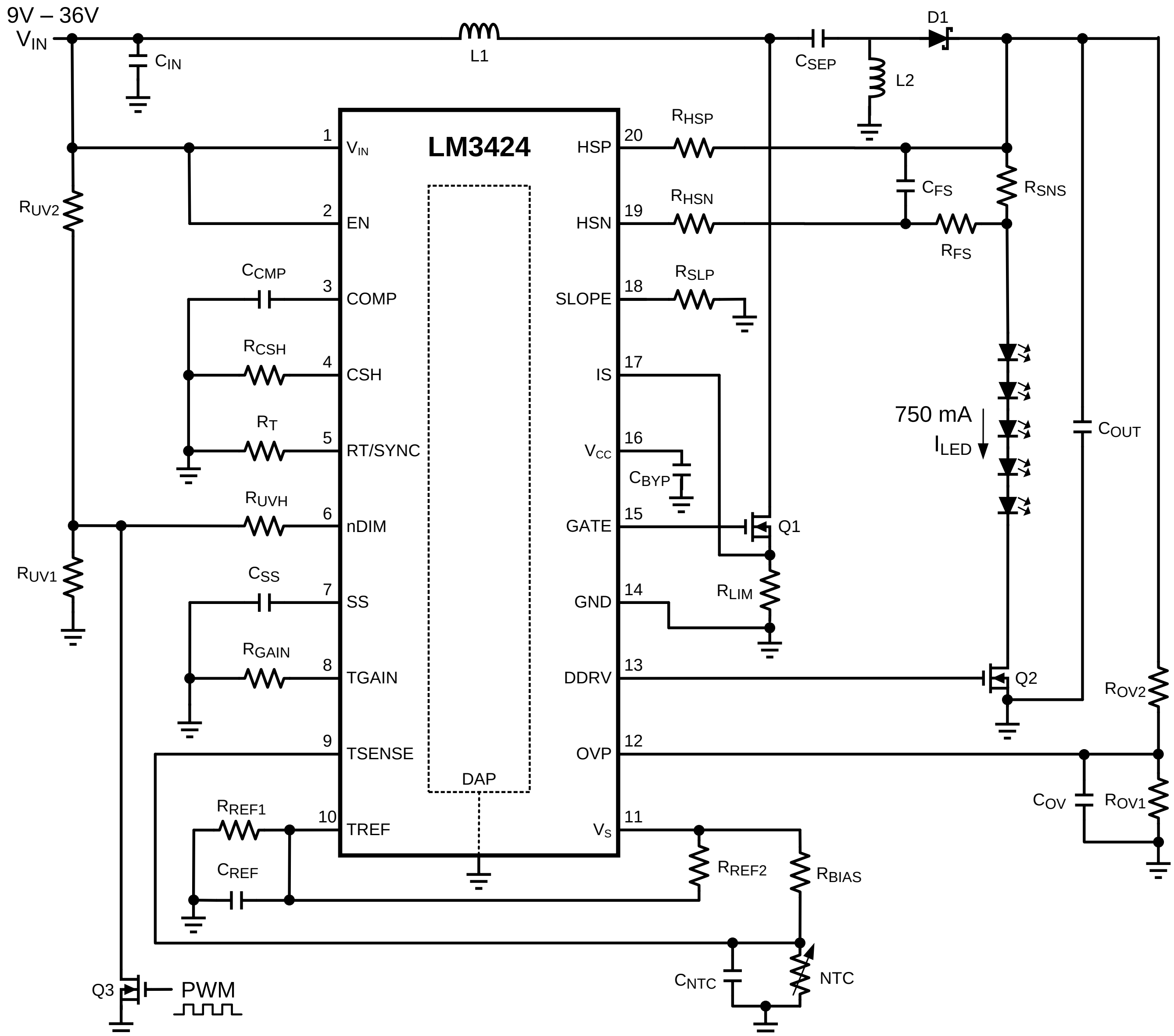



**Figure 47. SEPIC Application**

#### *8.2.9.1 Design Requirements*

- Input: 9 V to 36 V
- Output: 5 LEDs at 750 mA
- 60°C to 120°C Thermal Foldback
- PWM Dimming up to 30 kHz
- 500-kHz Switching Frequency

### 8.2.9.2 Detailed Design Procedure

**Table 8. Bill of Materials**

| QTY | PART ID | PART VALUE | MANUFACTURER | PART NUMBER |
|---|---|---|---|---|
| 1 | LM3424 | Boost controller | TI | LM3424MH |
| 1 | $C_{BYP}$ | 2.2 µF X7R 10% 16V | MURATA | GRM21BR71C225KA12L |
| 3 | $C_{CMP}$, $C_{NTC}$, $C_{SS}$ | 0.47 µF X7R 10% 25V | MURATA | GRM21BR71E474KA01L |
| 0 | $C_{FS}$ | DNP | | |
| 4 | $C_{IN}$ | 4.7 µF X7R 10% 100V | TDK | C5750X7R2A475K |
| 4 | $C_{OUT}$ | 10 µF X7R 10% 50V | TDK | C4532X7R1H106K |
| 1 | $C_{SEP}$ | 1.0 µF X7R 10% 100V | TDK | C4532X7R2A105K |
| 1 | $C_{OV}$ | 47 pF COG/NPO 5% 50V | AVX | 08055A470JAT2A |
| 1 | $C_{REF}$ | 1 µF X7R 10% 25V | MURATA | GRM21BR71E105KA01L |
| 1 | D1 | Schottky 60V 5A | COMCHIP | CDBC560-G |
| 2 | L1, L2 | 68 µH 20% 4.3A | COILCRAFT | DO3340P-683 |
| 2 | Q1, Q2 | NMOS 60V 8A | VISHAY | SI4436DY |
| 1 | Q3 | NMOS 60V 115 mA | ON-SEMI | 2N7002ET1G |
| 1 | $R_{BIAS}$ | 23.7 kΩ 1% | VISHAY | CRCW080523K7FKEA |
| 1 | $R_{CSH}$ | 12.4 kΩ 1% | VISHAY | CRCW080512K4FKEA |
| 1 | $R_{FS}$ | 0Ω 1% | VISHAY | CRCW08050000OZEA |
| 1 | $R_{GAIN}$ | 9.31 kΩ 1% | VISHAY | CRCW08059K31FKEA |
| 2 | $R_{HSP}$, $R_{HSN}$ | 750Ω 1% | VISHAY | CRCW0805750RFKEA |
| 1 | $R_{LIM}$ | 0.04Ω 1% 1W | VISHAY | WSL2512R0400FEA |
| 1 | $R_{OV1}$ | 15.8 kΩ 1% | VISHAY | CRCW080515K8FKEA |
| 1 | $R_{OV2}$ | 499 kΩ 1% | VISHAY | CRCW0805499KFKEA |
| 2 | $R_{REF1}$, $R_{REF2}$ | 49.9 kΩ 1% | VISHAY | CRCW080549K9FKEA |
| 1 | $R_{SLP}$ | 20.0 kΩ 1% | VISHAY | CRCW080520K0FKEA |
| 1 | $R_{SNS}$ | 0.1Ω 1% 1W | VISHAY | WSL2512R1000FEA |
| 1 | $R_{T}$ | 14.3 kΩ 1% | VISHAY | CRCW080514K3FKEA |
| 1 | $R_{UV1}$ | 1.62 kΩ 1% | VISHAY | CRCW08051K62FKEA |
| 1 | $R_{UV2}$ | 10.0 kΩ 1% | VISHAY | CRCW080510K0FKEA |
| 1 | $R_{UVH}$ | 16.9 kΩ 1% | VISHAY | CRCW080516K9FKEA |
| 1 | NTC | Thermistor 100 kΩ 5% | TDK | NTCG204H154J |

# 9 Power Supply Recommendations

## 9.1 Input Supply Current Limit

It is important to set the output current limit of your input supply to an appropriate value to avoid delays in your converter analysis and optimization. If not set high enough, current limit can be tripped during start up or when your converter output power is increased, causing a foldback or shut-down condition. It is a common oversight when powering up a converter for the first time.

# 10 Layout

## 10.1 Layout Guidelines

The performance of any switching regulator depends as much upon the layout of the PCB as the component selection. Following a few simple guidelines will maximimize noise rejection and minimize the generation of EMI within the circuit.

Discontinuous currents are the most likely to generate EMI, therefore care should be taken when routing these paths. The main path for discontinuous current in the LM3424 buck regulator contains the input capacitor ($C_{IN}$), the recirculating diode (D1), the N-channel MOSFET (Q1), and the sense resistor ($R_{LIM}$). In the LM3424 boost regulator, the discontinuous current flows through the output capacitor ($C_O$), D1, Q1, and $R_{LIM}$. In the buck-boost regulator both loops are discontinuous and should be carefully layed out. These loops should be kept as small as possible and the connections between all the components should be short and thick to minimize parasitic inductance. In particular, the switch node (where L1, D1, and Q1 connect) should be just large enough to connect the components. To minimize excessive heating, large copper pours can be placed adjacent to the short current path of the switch node.

The RT, COMP, CSH, IS, TSENSE, TREF, HSP, and HSN pins are all high-impedance inputs which couple external noise easily, therefore the loops containing these nodes should be minimized whenever possible.

In some applications the LED or LED array can be far away (several inches or more) from the LM3424, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the regulator, the output capacitor should be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.

## 10.2 Layout Example

Note critical paths and component placement:

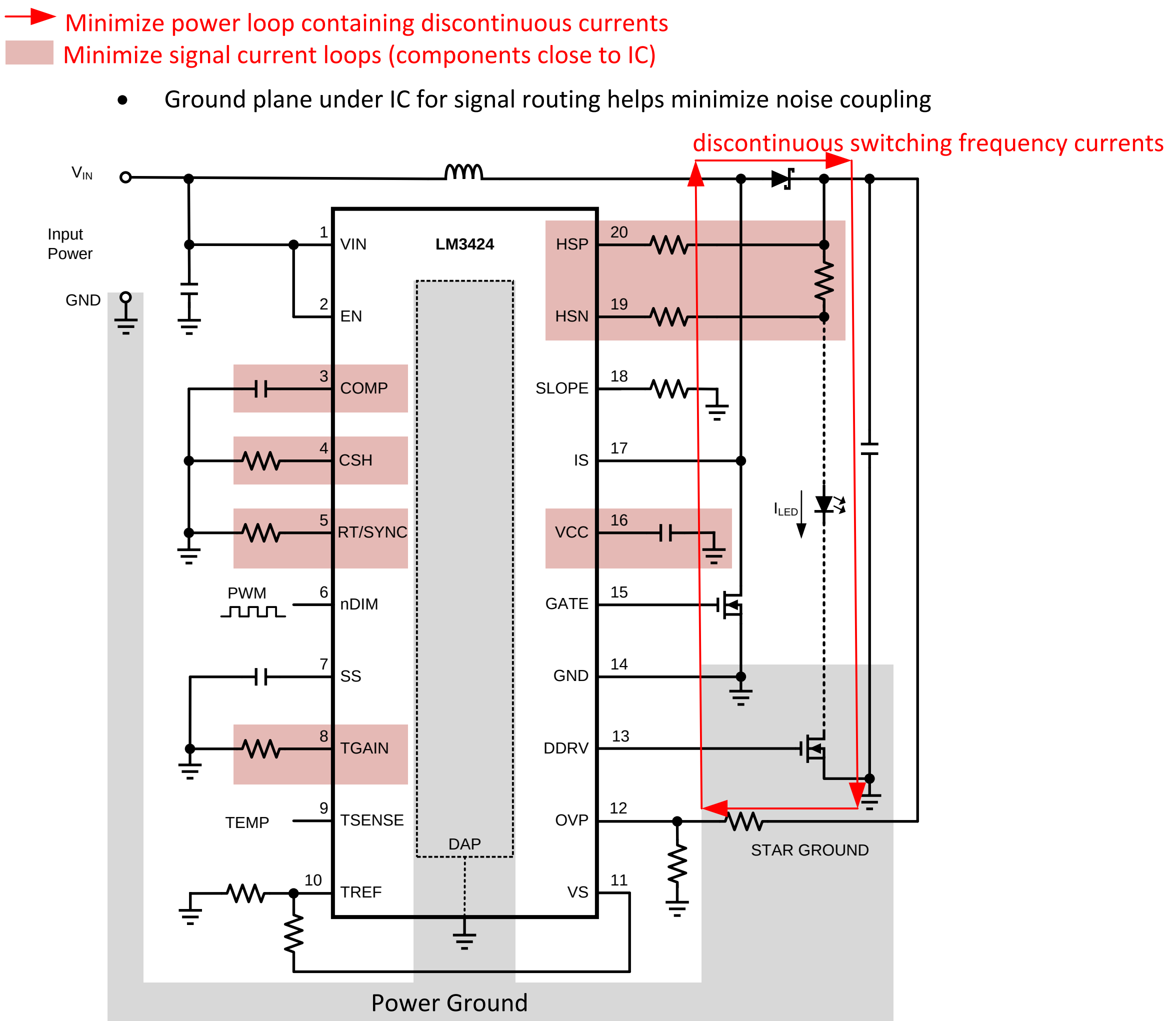



**Figure 48. Layout Recommendation**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Third-Party Products Disclaimer

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## 11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 9. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| LM3424 | Click here | Click here | Click here | Click here | Click here |
| LM3424-Q1 | Click here | Click here | Click here | Click here | Click here |

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
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## 11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3424MH/NOPB | ACTIVE | HTSSOP | PWP | 20 | 73 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LM3424 MH | Samples |
| LM3424MHX/NOPB | ACTIVE | HTSSOP | PWP | 20 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LM3424 MH | Samples |
| LM3424QMH/NOPB | ACTIVE | HTSSOP | PWP | 20 | 73 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LM3424 QMH | Samples |
| LM3424QMHX/NOPB | ACTIVE | HTSSOP | PWP | 20 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LM3424 QMH | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF LM3424, LM3424-Q1 :**

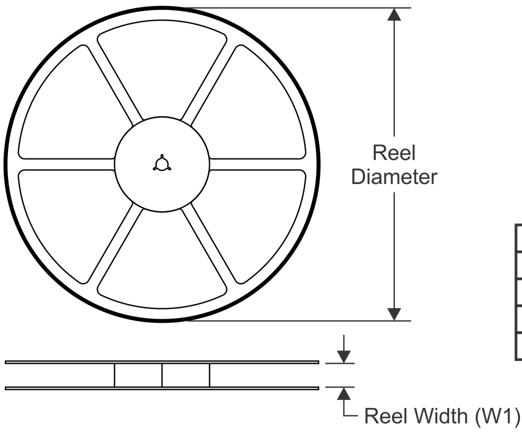
- Catalog: LM3424
- Automotive: LM3424-Q1

NOTE: Qualified Version Definitions:

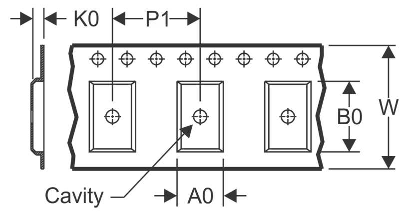
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

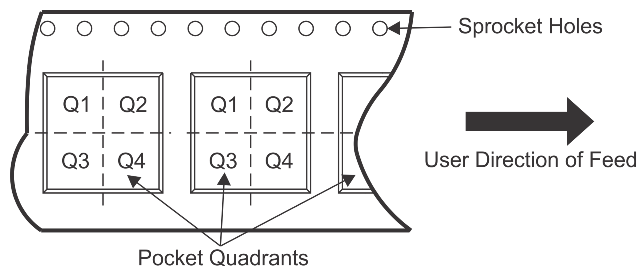



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

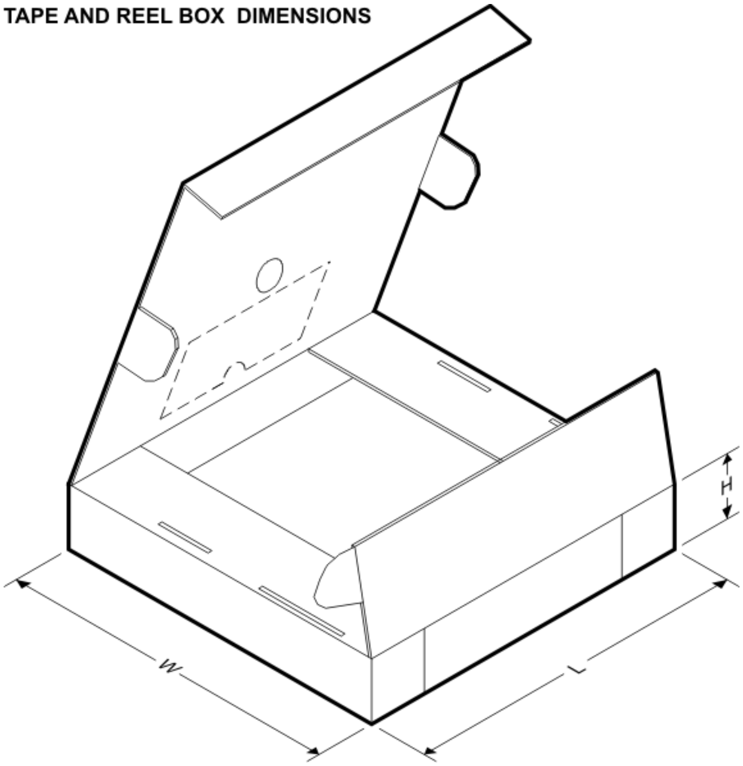
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3424MHX/NOPB | HTSSOP | PWP | 20 | 2500 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| LM3424QMHX/NOPB | HTSSOP | PWP | 20 | 2500 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

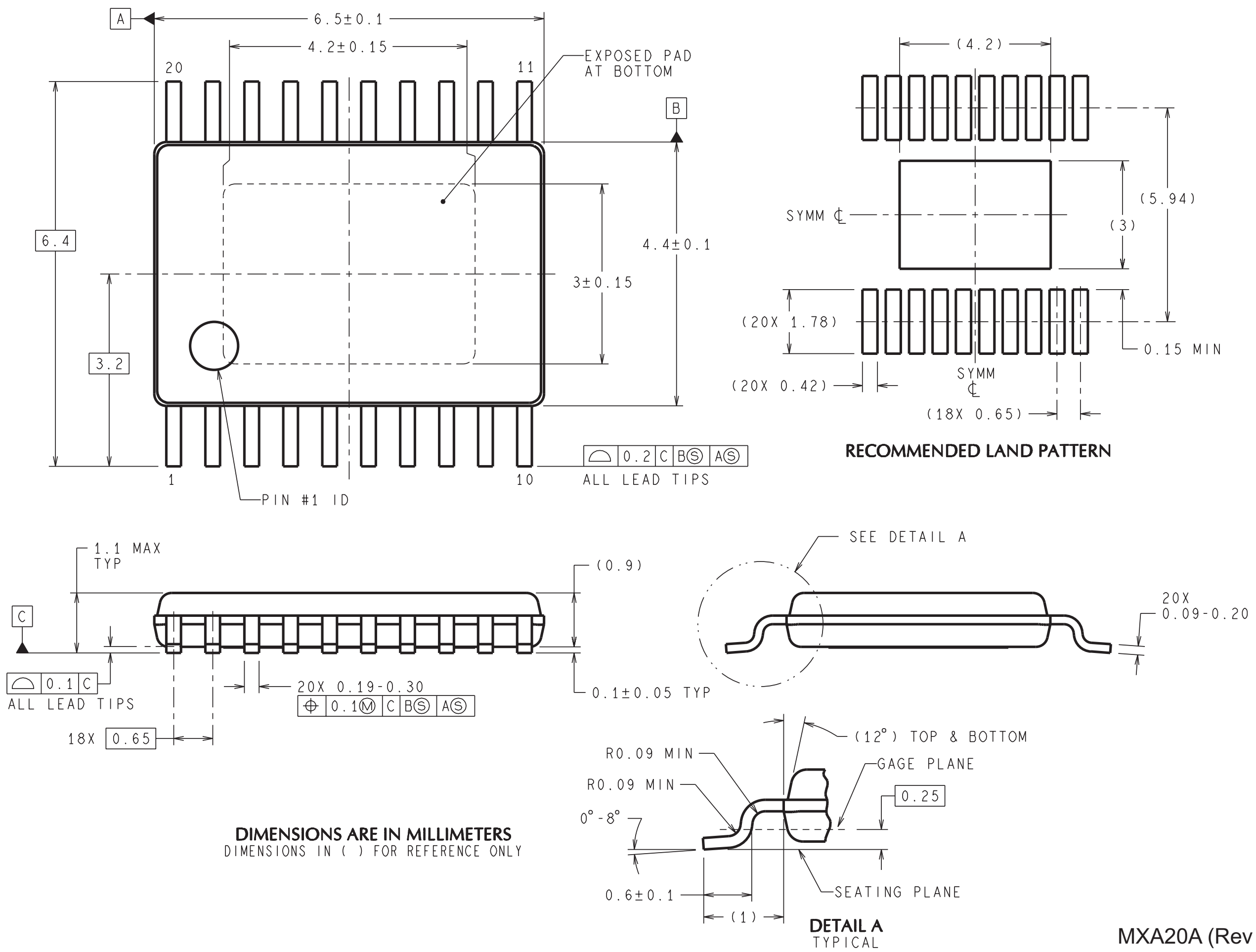
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM3424MHX/NOPB | HTSSOP | PWP | 20 | 2500 | 367.0 | 367.0 | 35.0 |
| LM3424QMHX/NOPB | HTSSOP | PWP | 20 | 2500 | 367.0 | 367.0 | 35.0 |

# PWP0020A

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