



**THE DATASHEET OF  
LM2903AVQPWRQ1**



## LM2903-Q1 Automotive Dual Differential Comparators

### 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 0:  $-40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  Ambient Operating Temperature Range (LM2903E-Q1)
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  Ambient Operating Temperature Range (LM2903-Q1)
  - Device HBM ESD Classification Level H1C
  - Device CDM ESD Classification Level C4B
- ESD Protection Exceeds 1000 V Per MIL-STD-883, Method 3015; Exceeds 100 V Using Machine Model ( $C = 200\text{ pF}$ ,  $R = 0\ \Omega$ )
- Single Supply or Dual Supplies
- Low Supply-Current Drain Independent of Supply Voltage 0.4 mA Typ Per Comparator
- Low Input Bias Current 25 nA Typ
- Low Input Offset Current 5 nA Typ
- Low Input Offset Voltage 2 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage  $\pm 36\text{ V}$
- Low Output Saturation Voltage
- Output Compatible With TTL, MOS, and CMOS

### 2 Applications

- Automotive
  - HEV/EV and Power Train
  - Infotainment and Cluster
  - Body Control Module
- Industrial
- Power supervision
- Oscillator
- Peak Detector
- Logic Voltage Translation

### 3 Description

This device consists of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is possible, as long as the difference between the two supplies is 2 V to 36 V, and VCC is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

The LM2903-Q1 is Qualified for the AEC-Q100 Grade 1 temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . The LM2903E-Q1 is Qualified for the AEC-Q100 Grade 0 temperature range of  $-40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ .

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2903-Q1	VSSOP(8)	3.00 mm x 3.00 mm
	SOIC (8)	4.90 mm x 3.91 mm
	TSSOP (8)	3.00 mm x 4.40 mm
LM2903E-Q1	TSSOP (8)	3.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Simplified Schematic



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## 4 Revision History

### Changes from Revision F (May 2018) to Revision G

Page

•	Changed previous Q1 graphs to match new format .....	<b>6</b>
•	Added LM2903E-Q1 specific graphs.....	<b>6</b>

### Changes from Revision E (June 2014) to Revision F

Page

•	Added LM2903E-Q1 to datasheet.....	<b>1</b>
•	Added Pin Functions table. ....	<b>3</b>
•	Changed Thermal Information Table .....	<b>4</b>

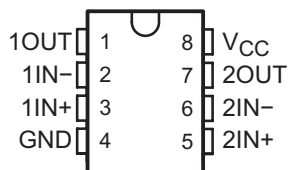
### Changes from Revision D (April 2008) to Revision E

Page

•	Added AEC-Q100 info to Features. ....	<b>1</b>
•	Added Applications. ....	<b>1</b>
•	Added Device Information table. ....	<b>1</b>
•	Added Handling Ratings table. ....	<b>4</b>
•	Added T <sub>J</sub> and ESD ratings to Abs Max table. ....	<b>4</b>
•	Updated Recommended Operating Conditions table. ....	<b>4</b>
•	Added Thermal Information table. ....	<b>4</b>
•	Updated Electrical Characteristics table. ....	<b>5</b>

## 5 Pin Configuration and Functions

**D, DGK OR PW PACKAGE  
Top View**



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
1OUT	1	Output	Comparator 1's output pin
1IN-	2	Input	Comparator 1's negative input pin
1IN+	3	Input	Comparator 1's positive input pin
GND	4	Input	Ground
2IN+	5	Input	Comparator 2's positive input pin
2IN-	6	Input	Comparator 2's negative input pin
2OUT	7	Output	Comparator 2's output pin
V <sub>CC</sub>	8	Input	Supply Pin

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>		36	V
V <sub>CC</sub>	Supply voltage, LM2903E-Q1 Only <sup>(2)</sup>		32	V
V <sub>ID</sub>	Differential input voltage <sup>(3)</sup>	-36	36	V
V <sub>I</sub>	Input voltage range (either input)	-0.3	36	V
V <sub>O</sub>	Output voltage		36	V
I <sub>O</sub>	Output current		20	mA
	Duration of output short-circuit to ground		Unlimited	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to GND.
- (3) Differential voltages are at IN+ with respect to IN-.

## LM2903-Q1

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### 6.2 Handling Ratings

			MIN	MAX	UNIT
$T_{stg}$	Storage temperature range	LM2903-Q1 Only	-65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	0	1000	V
		Charged device model (CDM), per AEC Q100-011	0	750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions, LM2903-Q1

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CC}$ (non-V devices)		2		30	V
$V_{CC}$ (V devices)		2		32	V
$T_J$	Junction Temperature	-40		125	°C

### 6.4 Recommended Operating Conditions, LM2903E-Q1

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CC}$		2		30	V
$T_J$	Junction Temperature	-40		150	°C

### 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LM2903E-Q1	LM2903-Q1	LM2903-Q1	LM2903-Q1	UNIT
		PW	DGK	PW	D	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	178.9	199.4	186.6	126.0	°C/W
$R_{\theta JCTop}$	Junction-to-case (top) thermal resistance	70.7	120.8	79.6	74.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	108.9	90.2	116.5	66.4	
$\Psi_{JT}$	Junction-to-top characterization parameter	11.9	21.5	17.7	25.4	
$\Psi_{JB}$	Junction-to-board characterization parameter	107.3	119.1	114.9	65.9	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

## 6.6 Electrical Characteristics

at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^{(1)}$	MIN TYP MAX			UNIT
			MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_O = 1.4\text{ V}$ , $V_{IC} = V_{IC(min)}$ , $V_{CC} = 5\text{ V to MAX}^{(2)}$	Non-A devices	25°C	2	7	mV
			Full range		15	
		A-suffix devices	25°C	1	2	
			Full range		4	
$I_{IO}$ Input offset current	$V_O = 1.4\text{ V}$	25°C	5	50	nA	
		Full range		200		
$I_{IB}$ Input bias current	$V_O = 1.4\text{ V}$	25°C	-25	-250	nA	
		Full range		-500		
$V_{ICR}$ Common-mode input voltage range <sup>(3)</sup>		25°C	0 to $V_{CC}-1.5$		V	
		Full range	0 to $V_{CC}-2$			
$A_{VD}$ Large-signal differential-voltage amplification	$V_{CC} = 15\text{ V}$ , $V_O = 1.4\text{ V to }11.4\text{ V}$ , $R_L \geq 15\text{ k}\Omega\text{ to }V_{CC}$	25°C	25	100	V/mV	
$I_{OH}$ High-level output current	$V_{OH} = 5\text{ V}$ $V_{OH} = V_{CC}\text{ MAX}^{(2)}$	$V_{ID} = 1\text{ V}$	25°C	0.1	50	nA
			Full range		1	$\mu\text{A}$
$V_{OL}$ Low-level output voltage	$I_{OL} = 4\text{ mA}$ ,	$V_{ID} = -1\text{ V}$	25°C	150	400	mV
			Full range		700	
$I_{OL}$ Low-level output current	$V_{OL} = 1.5\text{ V}$ ,	$V_{ID} = -1\text{ V}$	25°C	6		mA
$I_{CC}$ Supply current	$R_L = \infty$	$V_{CC} = 5\text{ V}$	25°C	0.8	1	mA
		$V_{CC} = \text{MAX}^{(2)}$	Full range		2.5	

(1) Full range (MIN or MAX) for LM2903-Q1 is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  and  $-40^\circ\text{C}$  to  $150^\circ\text{C}$  for the LM2903E-Q1. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

(2)  $V_{CC}\text{ MAX} = 30\text{ V}$  for non-V devices and  $32\text{ V}$  for V-suffix devices.

(3) The voltage at either input or common-mode should not be allowed to go negative by more than  $0.3\text{ V}$ . The upper end of the common-mode voltage range is  $V_{CC} + 1.5\text{ V}$  for the inverting input ( $-$ ), and the non-inverting input ( $+$ ) can exceed the  $V_{CC}$  level; the comparator provides a proper output state. Either or both inputs can go to  $30\text{ V}$  ( $32\text{ V}$  for V-suffix devices) without damage.

## 6.7 Switching Characteristics

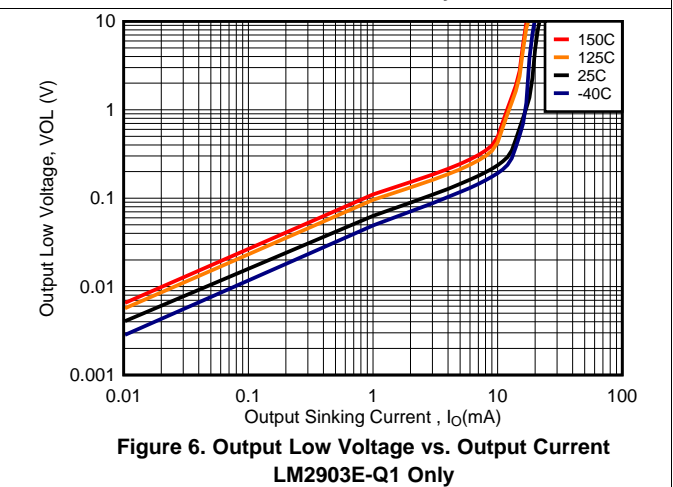
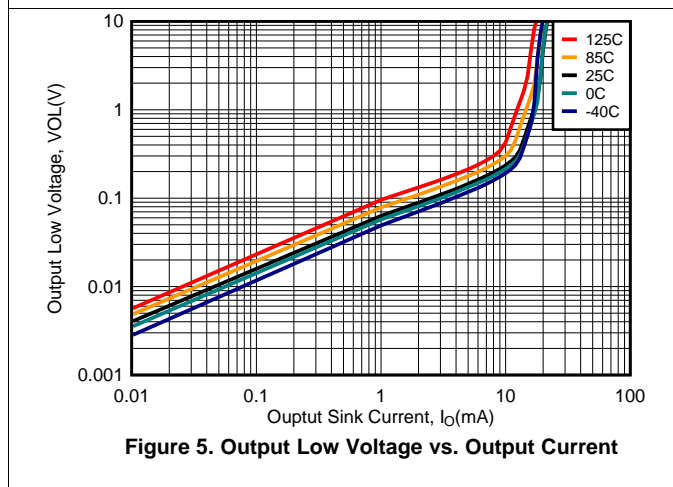
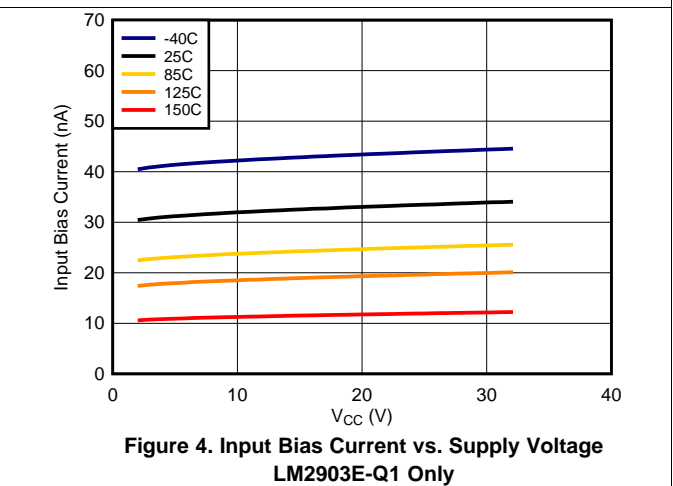
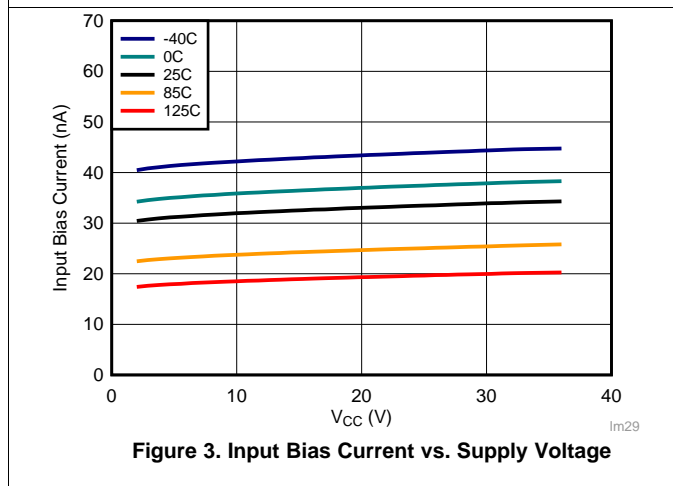
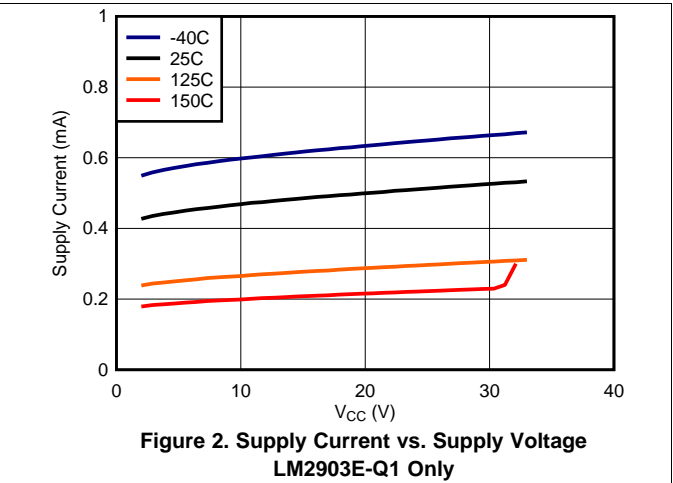
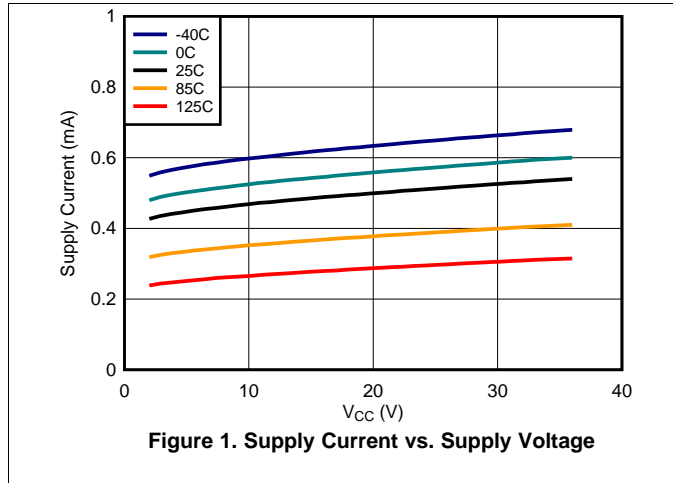
 $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ 

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	$R_L$ connected to $5\text{ V}$ through $5.1\text{ k}\Omega$ ,	100-mV input step with 5-mV overdrive	1.3	$\mu\text{s}$
	$C_L = 15\text{ pF}^{(1)(2)}$	TTL-level input step	0.3	

(1)  $C_L$  includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses  $1.4\text{ V}$ .

### 6.8 Typical Characteristics



## 7 Detailed Description

### 7.1 Overview

The LM2903-Q1 family is a dual comparator with the ability to operate up to 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to its very wide supply voltages range (2 V to 36 V), low I<sub>q</sub> and fast response.

This device is AEC-Q100 qualified and can operate over a wide temperature range of –40°C to 125°C (LM2903-Q1) or –40°C to 150°C (LM2903E-Q1).

The open-drain output allows the user to configure the output's logic low voltage (V<sub>OL</sub>) and can be utilized to enable the comparator to be used in AND functionality.

### 7.2 Functional Block Diagram

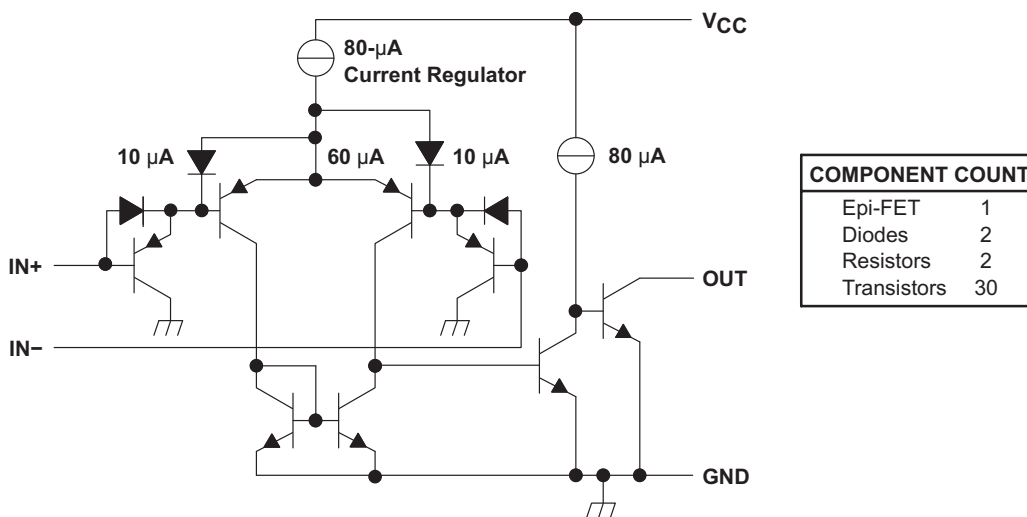


Figure 7. Schematic (Each Comparator)

### 7.3 Feature Description

LM2903-Q1 family consists of a PNP darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing LM2903-Q1 to accurately function from ground to V<sub>CC</sub>–1.5V differential input. This enables much head room for modern day supplies of 3.3 V and 5.0 V.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN will sink current when the positive input voltage is higher than the negative input voltage and the offset voltage. The V<sub>OL</sub> is resistive and will scale with the output current. Please see Figure 3 in the *Typical Characteristics* section for V<sub>OL</sub> values with respect to the output current.

### 7.4 Device Functional Modes

#### 7.4.1 Voltage Comparison

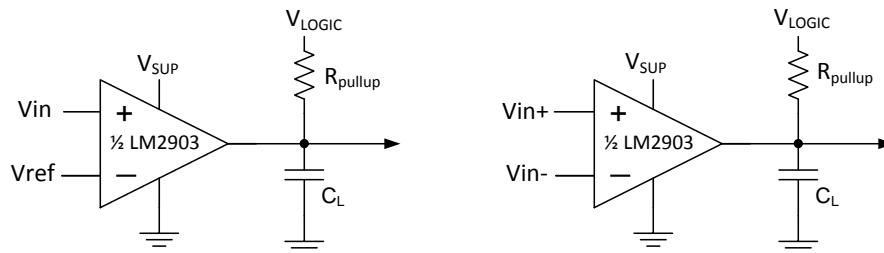
The LM2903-Q1 family operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pull-up) based on the input differential polarity.

## 8 Application and Implementation

### 8.1 Application Information

LM2903-Q1 will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes LM2903Q1 optimal for level shifting to a higher or lower voltage.

### 8.2 Typical Application



**Figure 8. Single-ended and Differential Comparator Configurations**

#### 8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

**Table 1. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to $V_{sup}-1.5$ V
Supply Voltage	2 V to 36 V
Logic Supply Voltage	2 V to 36 V
Output Current ( $R_{PULLUP}$ )	1 $\mu$ A to 20 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance ( $C_L$ )	15 pF

#### 8.2.2 Detailed Design Procedure

When using LM2903-Q1 family in a general comparator application, determine the following:

- Input Voltage Range
- Minimum Overdrive Voltage
- Output and Drive Current
- Response Time

##### 8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range ( $V_{ICR}$ ) must be taken in to account. If temperature operation is above or below 25°C the  $V_{ICR}$  can range from 0 V to  $V_{CC}-2.0$  V. This limits the input voltage range to as high as  $V_{CC}-2.0$  V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

Below is a list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common mode range:
  - a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
  - b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting

2. When IN- is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common mode and IN- is within common mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common mode, the output is low and the output transistor is sinking current

**8.2.2.2 Minimum Overdrive Voltage**

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage ( $V_{IO}$ ). In order to make an accurate comparison the Overdrive Voltage ( $V_{OD}$ ) should be higher than the input offset voltage ( $V_{IO}$ ). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. Figure 9 and Figure 10 show positive and negative response times with respect to overdrive voltage.

**8.2.2.3 Output and Drive Current**

Output current is determined by the load/pull-up resistance and logic/pull-up voltage. The output current will produce a output low voltage ( $V_{OL}$ ) from the comparator. In which  $V_{OL}$  is proportional to the output current. Use Figure 5 to determine  $V_{OL}$  based on the output current.

The output current can also effect the transient response. More will be explained in the next section.

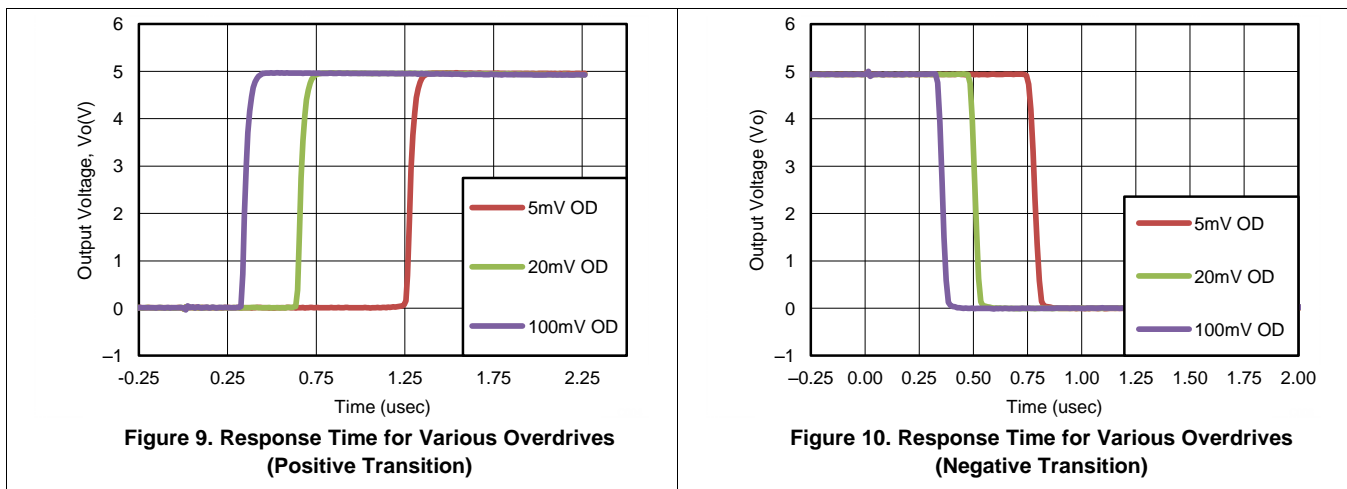
**8.2.2.4 Response Time**

The transient response can be determined by the load capacitance ( $C_L$ ), load/pull-up resistance ( $R_{PULLUP}$ ) and equivalent collector-emitter resistance ( $R_{CE}$ ).

- The positive response time ( $\tau_P$ ) is approximately  $\tau_P \sim R_{PULLUP} \times C_L$
- The negative response time ( $\tau_N$ ) is approximately  $\tau_N \sim R_{CE} \times C_L$ 
  - $R_{CE}$  can be determine by taking the slope of Figure 5 in it's linear region at the desired temperature, or by dividing the  $V_{OL}$  by  $I_{out}$

**8.2.3 Application Curves**

The following curves were generated with 5 V on  $V_{CC}$  and  $V_{Logic}$ ,  $R_{PULLUP} = 5.1 \text{ k}\Omega$ , and 50 pF scope probe.



## 9 Power Supply Recommendations

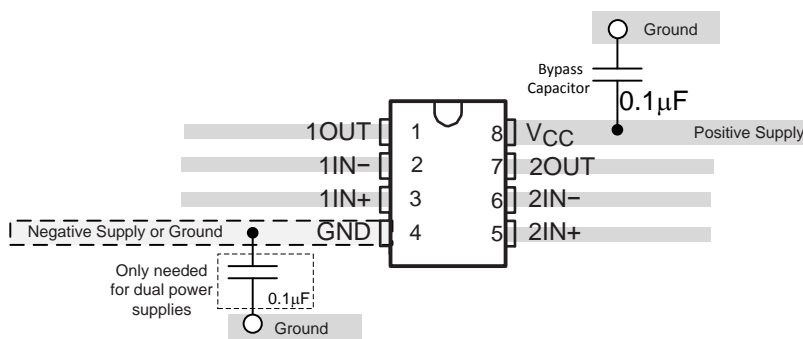
For fast response and comparison applications with noisy or AC inputs, it is recommended to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can eat into the comparator's input common mode range and create an inaccurate comparison.

## 10 Layout

### 10.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches, which can affect the high level input common mode voltage range. In order to achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

### 10.2 Layout Example



**Figure 11. LM2903Q1 Layout Example**

## 11 Device and Documentation Support

### 11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM2903-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
LM2903E-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2903AVQDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ	<a href="#">Samples</a>
LM2903AVQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ	<a href="#">Samples</a>
LM2903AVQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ	<a href="#">Samples</a>
LM2903AVQPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903AVQ	<a href="#">Samples</a>
LM2903EPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	2903Q0	<a href="#">Samples</a>
LM2903QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	KACQ	<a href="#">Samples</a>
LM2903QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1	<a href="#">Samples</a>
LM2903QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1	<a href="#">Samples</a>
LM2903QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1	<a href="#">Samples</a>
LM2903QPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q1	<a href="#">Samples</a>
LM2903VQDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ1	<a href="#">Samples</a>
LM2903VQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ1	<a href="#">Samples</a>
LM2903VQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ	<a href="#">Samples</a>
LM2903VQPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903VQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF LM2903-Q1 :**

- Catalog: [LM2903](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2903AVQDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903AVQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903EPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903QPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2903AVQDRQ1	SOIC	D	8	2500	340.5	338.1	20.6
LM2903AVQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903AVQPWRQ1	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903EPWRQ1	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2903QPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903QPWRQ1	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903VQPWRG4Q1	TSSOP	PW	8	2000	367.0	367.0	35.0
LM2903VQPWRQ1	TSSOP	PW	8	2000	367.0	367.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW0008A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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