



THE DATASHEET OF LM2755TMX



LM2755 Charge Pump LED Controller with I²C-Compatible Interface in DSBGA Package

Check for Samples: [LM2755](#)

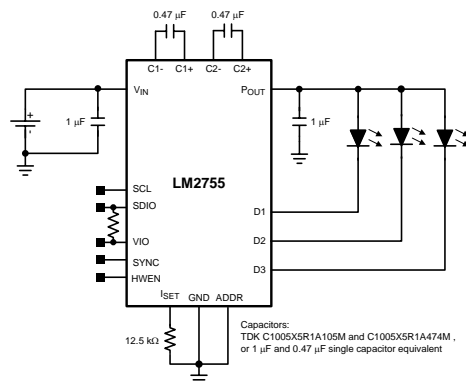
FEATURES

- **90% Peak Efficiency**
- **Total solution size < 13mm²**
- **No Inductor Required: Only 4 Inexpensive Ceramic Caps**
- **3 Independently Controlled Constant Current Outputs**
- **Programmable Trapezoidal Dimming Waveform on Each Output**
- **Programmable Timing Control Via Internal Registers and External Clock Synchronization Input**
- **32 Exponential Dimming Steps with 800:1 Dimming Ratio**
- **Programmable Brightness Control via I²C-Compatible Interface**
- **Hardware Enable Pin**
- **Wide Input Voltage Range: 2.7V to 5.5V**
- **Tiny 18-bump Thin DSBGA : 1.8mm x 1.6mm x 0.6mm**

APPLICATIONS

- **Indicator LEDs**
- **Keypad LED Backlight**
- **Display LED Backlight**
- **Fun-light LEDs**

TYPICAL APPLICATION CIRCUIT


Figure 1. Typical Application Circuit

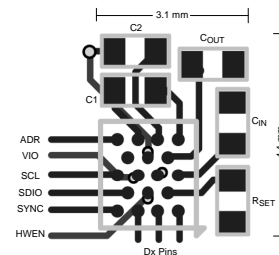
DESCRIPTION

The LM2755 is a charge-pump-based, constant current LED driver capable of driving 3 LEDs with a total output current up to 90mA. The diode current waveforms of each LED can be trapezoidal with timing and level parameters (rise time, fall time, high level, low level, delay, high time, low time) programmed via an I²C-compatible interface. The 32 brightness levels found on the LM2755 are exponentially spaced (as opposed to linearly spaced) to better match the response of the human eye to changing brightness levels.

The device requires only four small and low-cost ceramic capacitors. The LM2755 provides excellent efficiency without the use of an inductor by operating the charge pump in a gain of 3/2 or in a gain of 1. Maximum efficiency is achieved over the input voltage range by actively selecting the proper gain based on the LED forward voltage requirements.

The pre-regulation scheme used by the LM2755 is optimized to ensure low conducted noise on the input. An internal soft-start circuitry eliminates high inrush current at start-up. The LM2755 consumes 3µA (typ.) of supply current in shut-down.

The LM2755 is available in Texas Instruments' tiny 18-bump thin DSBGA package.


Figure 2. Minimum Solution Size


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Connection Diagram

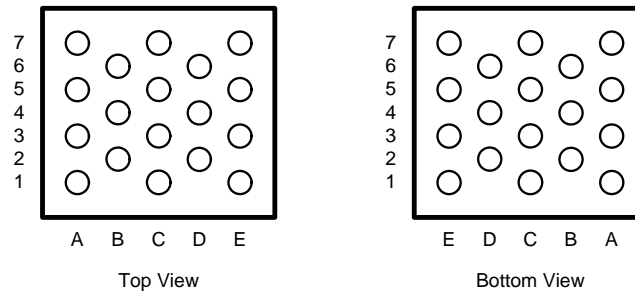


Figure 3. 18-Bump Thin DSBGA Package
1.615mm × 1.807mm × 0.6mm
(See Package Number YFQ0018AAA)

PIN DESCRIPTIONS

Pin #s	Pin Names	Pin Descriptions
A1	ID1	LED Driver 1
A3	ID2	LED Driver 2
A5	ID3	LED Driver 3
A7	SYNC	External clock synchronization input
B2	ISET	LED Driver Current Set Pin
B4	HWEN	Hardware EN Pin. Low '0' = RESET, High '1' = Normal Operation
B6	SDIO	Serial data Input/Output pin
C1	V _{IN}	Input Voltage Connection
C3	GND	Ground Connection.
C5	VIO	Serial Bus Voltage Level Input
C7	SCL	Serial Clock Pin
D2	P _{OUT}	Charge Pump Output
D4	C2-	Flying Capacitor Connect
D6	GND	Ground connection
E1	C1+	Flying Capacitor Connect
E3	C2+	Flying Capacitor Connect
E5	C1-	Flying Capacitor Connect
E7	ADDR	Chip Address Select Input. VIN = 0x67. Ground = 0x18.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS (1)(2)(3)

V _{IN} pin voltage	-0.3V to 6.0V
SCL, SDIO, VIO, ADDR, SYNC pin voltages	-0.3V to (V _{IN} +0.3V) w/ 6.0V max
I _{Dx} Pin Voltages	-0.3V to (V _{POUT} +0.3V) w/ 6.0V max
Continuous Power Dissipation (4)	Internally Limited
Junction Temperature (T _{J-MAX})	150°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering)	(5)
ESD Rating ⁽⁶⁾ Human Body Model	2.5kV

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply verified performance limits. For verified performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) All voltages are with respect to the potential at the GND pin.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160°C (typ.) and disengages at T_J = 155°C (typ.).
- (5) For detailed soldering specifications and information, please refer to STET Application Note 1112: DSBGA Wafer Level Chip Scale Package (AN-1112 [SNVA009](#)).
- (6) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. (MIL-STD-883 3015.7)

OPERATING RATINGS (1)(2)

Input Voltage Range	2.7V to 5.5V
Junction Temperature (T _J) Range	-30°C to 105°C
Ambient Temperature (T _A) Range ⁽³⁾	-30°C to +85°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply verified performance limits. For verified performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) All voltages are with respect to the potential at the GND pin.
- (3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX-OP} = 105°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

THERMAL PROPERTIES

Junction-to-Ambient Thermal Resistance (θ _{JA}), YFQ0018 Package (1)	56°C/W
--------------------------------------------------------------------------------	--------

- (1) Junction-to-ambient thermal resistance is highly dependent on application and board layout. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. For more information, please refer to Texas Instruments STET Application Note 1112: DSBGA Wafer Level Chip Scale Package (AN-1112 [SNVA009](#)).

ELECTRICAL CHARACTERISTICS ⁽¹⁾⁽²⁾

Limits in standard typeface are for $T_J = 25^\circ\text{C}$, and limits in boldface type apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = 3.6\text{V}$; $V_{D1} = 0.4\text{V}$; $V_{D2} = 0.4\text{V}$; $V_{D3} = 0.4\text{V}$; $R_{SET} = 12.5\text{k}\Omega$; D1, D2, and D3 = Fullscale Current; EN1, EN2, and EN3 Bits = "1"; CLK bit = '0'; $C_1 = C_2 = 0.47\mu\text{F}$, $C_{IN} = C_{OUT} = 1\mu\text{F}$; Specifications related to output current(s) and current setting pins (I_{DX} and I_{SET}) apply to D1, D2 and D3. ⁽³⁾

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DX}	Output Current Regulation	$3.0\text{V} \leq V_{IN} \leq 5.5\text{V}$	18.7	20.7	22.7	mA
I_{MATCH}	Output Current Matching	$3.0\text{V} \leq V_{IN} \leq 5.5\text{V}$ ⁽⁴⁾		1		%
I_Q	Quiescent Supply Current	Gain = 3/2 $D_{1-3} = \text{OPEN}$, $R_{SET} = \text{OPEN}$		1.0	1.3	mA
I_{SD}	Shutdown Supply Current	$3.0\text{V} \leq V_{IN} \leq 5.5\text{V}$ EN1 = EN2 = EN3 = 0		5	9.5	μA
V_{SET}	I_{SET} Pin Voltage	$3.0\text{V} \leq V_{IN} \leq 5.5\text{V}$		1.25		V
I_{DX} / I_{SET}	Output Current to Current Set Ratio	⁽⁵⁾		200		
V_{DXTH}	V_{DX} 1x to 3/2x Gain Transition Threshold	V_{D1} and/or V_{D2} and/or V_{D3} Falling		350		mV
V_{HR}	Current Source Headroom Voltage Requirement ⁽⁶⁾	$I_{DX} = 95\% \times I_{DX}(\text{nom.})$ ($I_{DX}(\text{nom.}) \approx 20\text{mA}$) Gain = 3/2		200		mV
f_{SW}	Switching Frequency		0.975	1.25	1.525	MHz
t_{START}	Start-up Time	$P_{OUT} = 90\%$ steady state		300		μs
f_{PWM}	Internal Diode Current PWM Frequency			20		kHz
f_{SYNC}	Maximum External Sync Frequency			1.0		MHz
V_{HWEN}	HWEN Voltage Thresholds	$2.7\text{V} \leq V_{IN} \leq 5.5\text{V}$	Reset	0	0.5	V
			Normal Operation	1.23	VIN	
I²C-Compatible Interface Voltage Specifications (SCL, SDIO, VIO)						
V_{IO}	Serial Bus Voltage Level	$2.7\text{V} \leq V_{IN} \leq 5.5\text{V}$ ⁽⁷⁾	1.44		VIN	V
V_{IL}	Input Logic Low "0"	$2.7\text{V} \leq V_{IN} \leq 5.5\text{V}$, $V_{IO} = 3.0\text{V}$	0		0.35 × VIN	V
V_{IH}	Input Logic High "1"	$2.7\text{V} \leq V_{IN} \leq 5.5\text{V}$, $V_{IO} = 3.0\text{V}$	0.65 × VIN		VIO	V
V_{OL}	Output Logic Low "0"	$I_{LOAD} = 3\text{mA}$			400	mV
I²C-Compatible Interface Timing Specifications (SCL, SDIO, VIO) ⁽⁸⁾						
t_1	SCL (Clock Period)		2.5			μs
t_2	Data In Setup Time to SCL High		100			ns
t_3	Data Out stable After SCL Low		0			ns
t_4	SDIO Low Setup Time to SCL Low (Start)		100			ns

- All voltages are with respect to the potential at the GND pin.
- Min and Max limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
- C_{IN} , C_{POUT} , C_1 , and C_2 : Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
- For the current sinks on a part, the following are determined: the maximum sink current in the group (MAX), the minimum sink current in the group (MIN), and the average sink current of the group (AVG). Two matching numbers are calculated: $(\text{MAX}-\text{AVG})/\text{AVG}$ and $(\text{AVG}-\text{MIN})/\text{AVG}$. The larger number of the two (worst case) is considered the matching figure. The typical specification provided is the most likely norm of the matching figure for all parts
- The maximum total output current for the LM2755 should be limited to 90mA. The total output current can be split among any of the three banks ($I_{D1} = I_{D2} = I_{D3} = 30\text{mA Max.}$). Under maximum output current conditions, special attention must be given to input voltage and LED forward voltage to ensure proper current regulation. See [MAXIMUM OUTPUT CURRENT](#), [MAXIMUM LED VOLTAGE](#), and [MINIMUM INPUT VOLTAGE](#) of the datasheet for more information.
- For each I_{DX} output pin, headroom voltage is the voltage across the internal current sink connected to that pin. For $V_{HR} = V_{OUT} - V_{Dxx}$. If headroom voltage requirement is not met, LED current regulation will be compromised.
- SCL and SDIO signals are referenced to VIO and GND for minimum VIO voltage testing.
- SCL and SDIO should be glitch-free in order for proper brightness control to be realized.

ELECTRICAL CHARACTERISTICS ⁽¹⁾⁽²⁾ (continued)

Limits in standard typeface are for $T_J = 25^\circ\text{C}$, and limits in boldface type apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = 3.6\text{V}$; $V_{D1} = 0.4\text{V}$; $V_{D2} = 0.4\text{V}$; $V_{D3} = 0.4\text{V}$; $R_{SET} = 12.5\text{k}\Omega$; D1, D2, and D3 = Fullscale Current; EN1, EN2, and EN3 Bits = "1"; CLK bit = '0'; $C1 = C2 = 0.47\mu\text{F}$; $C_{IN} = C_{OUT} = 1\mu\text{F}$; Specifications related to output current(s) and current setting pins (I_{DX} and I_{SET}) apply to D1, D2 and D3. ⁽³⁾

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_5	SDIO High Hold Time After SCL High (Stop)		100			ns

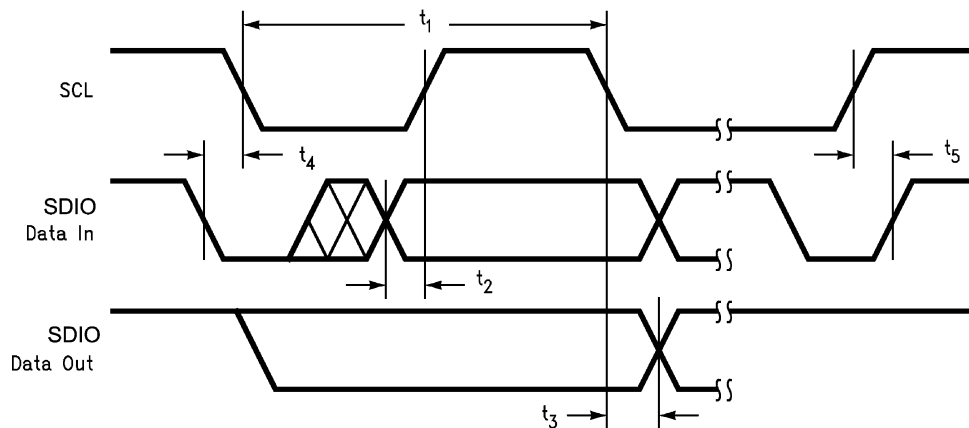


Figure 4. I²C Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: $T_A = 25^\circ\text{C}$; $V_{IN} = 3.6\text{V}$; $V_{HWEN} = V_{IN}$; $V_{D1} = V_{D2} = V_{D3} = 3.6\text{V}$; $R_{SET} = 12.5\text{k}\Omega$; $C_1=C_2= 0.47\mu\text{F}$, $C_{IN} = C_{VOUT} = 1\mu\text{F}$; $\text{ENA} = \text{ENB} = \text{ENC} = '1'$.

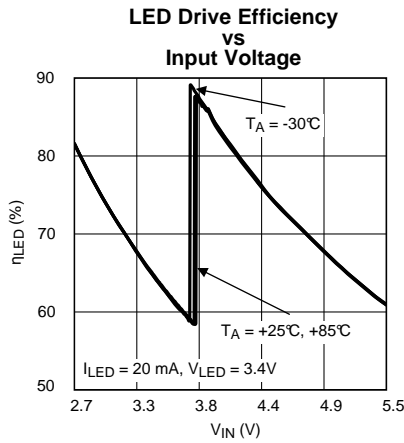


Figure 5.

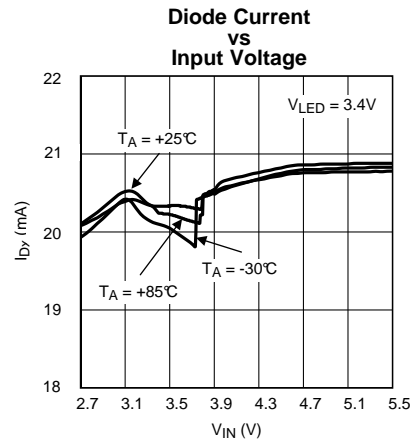


Figure 6.

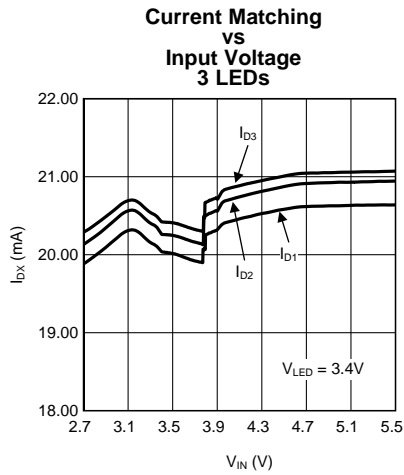


Figure 7.

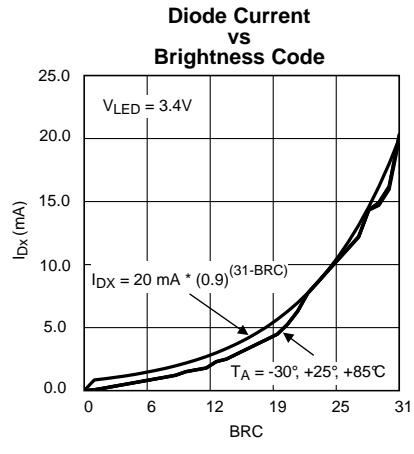


Figure 8.

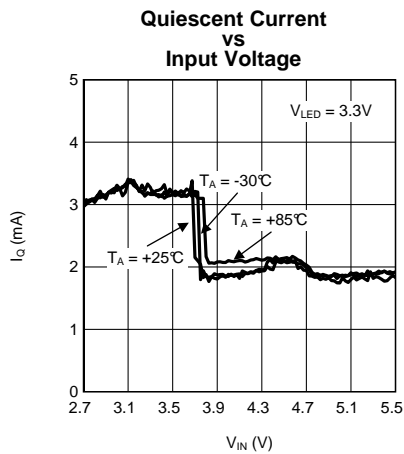


Figure 9.

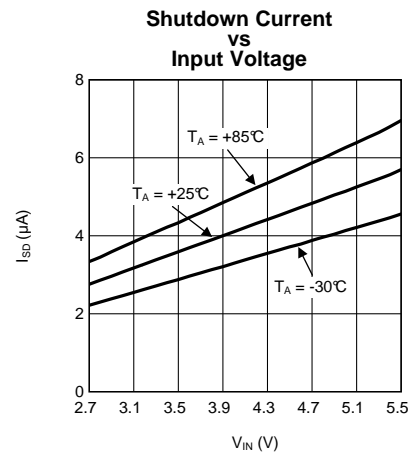


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_A = 25^\circ\text{C}$; $V_{IN} = 3.6\text{V}$; $V_{HWEN} = V_{IN}$; $V_{D1} = V_{D2} = V_{D3} = 3.6\text{V}$; $R_{SET} = 12.5\text{k}\Omega$; $C_1=C_2= 0.47\mu\text{F}$, $C_{IN} = C_{VOUT} = 1\mu\text{F}$; $\text{ENA} = \text{ENB} = \text{ENC} = '1'$.

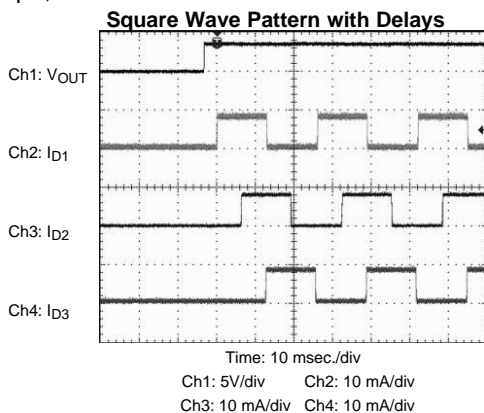


Figure 11.

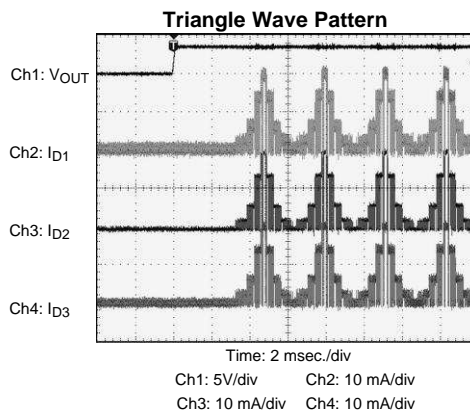


Figure 12.

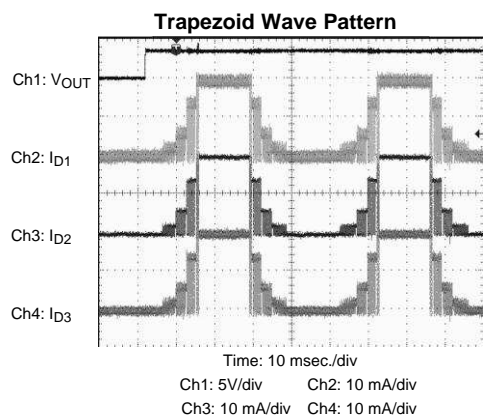


Figure 13.

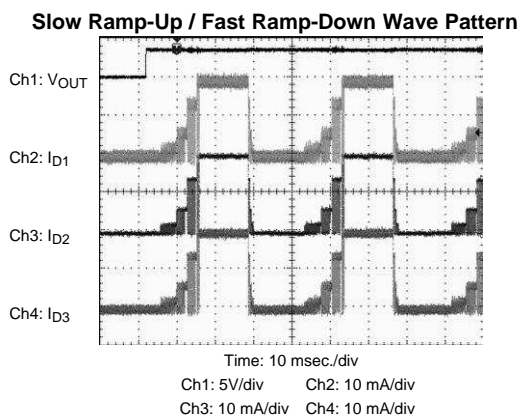
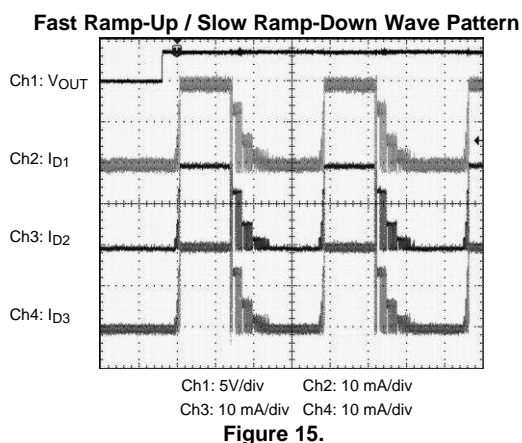


Figure 14.



BLOCK DIAGRAM

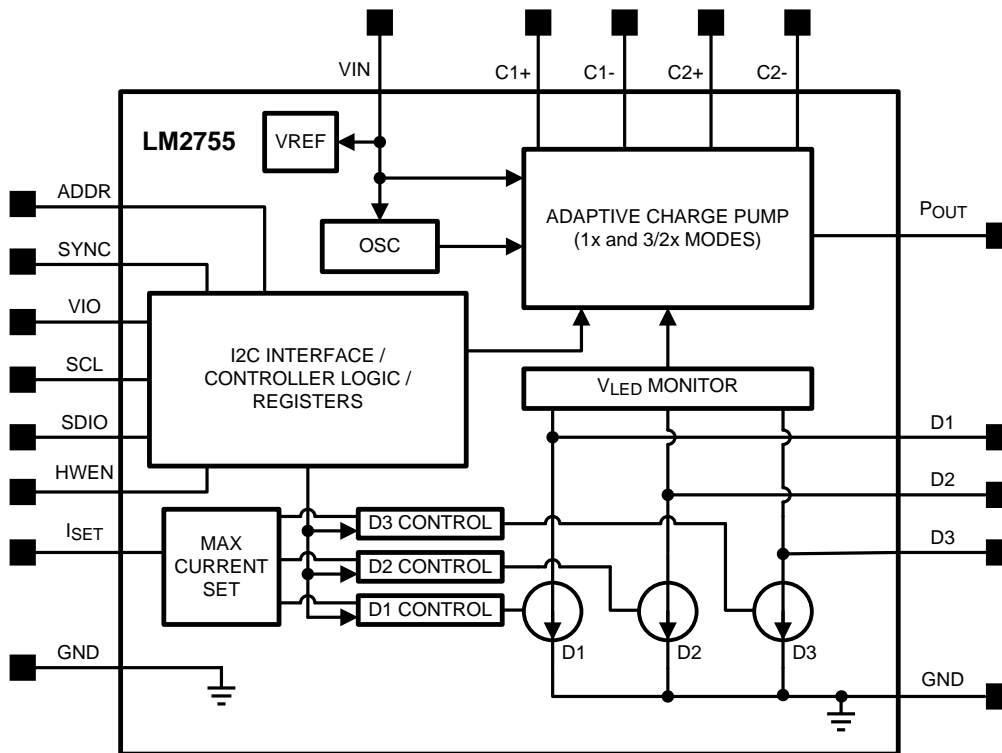


Figure 16. Block Diagram

CIRCUIT COMPONENTS

CHARGE PUMP

The input to the 3/2x - 1x charge pump is connected to the V_{IN} pin, and the regulated output of the charge pump is connected to the P_{OUT} pin. The recommended input voltage range of the LM2755 is 3.0V to 5.5V. The device's regulated charge pump has both open loop and closed loop modes of operation. When the device is in open loop, the voltage at V_{OUT} is equal to the gain times the voltage at the input. When the device is in closed loop, the voltage at V_{OUT} is regulated to 4.6V (typ.). The charge pump gain transitions are actively selected to maintain regulation based on LED forward voltage and load requirements. This allows the charge pump to stay in the most efficient gain (1x) over as much of the input voltage range as possible, reducing the power consumed from the battery.

LED FORWARD VOLTAGE MONITORING

The LM2755 has the ability to switch converter gains (1x or 3/2x) based on the forward voltage of the LED load. This ability to switch gains maximizes efficiency for a given load. Forward voltage monitoring occurs on all diode pins. At higher input voltages, the LM2755 will operate in pass mode, allowing the P_{OUT} voltage to track the input voltage. As the input voltage drops, the voltage on the Dx pins will also drop ($V_{DX} = V_{P_{OUT}} - V_{LEDx}$). Once any of the active Dx pins reaches a voltage approximately equal to 350mV, the charge pump will then switch to the gain of 3/2x. This switch-over ensures that the current through the LEDs never becomes pinched off due to a lack of headroom on the current sources.

Only active Dx pins will be monitored. For example, if only D1 is enabled, the LEDs connected to D2 and D3 will not affect the gain transition point. If all Dx pins are enabled, all diodes will be monitored, and the gain transition will be based upon the diode with the highest forward voltage.

HWEN PIN

The LM2755 has a hardware enable/reset pin (HWEN) that allows the device to be disabled by an external controller without requiring an I²C write command. Under normal operation, the HWEN pin should be held high (logic '1') to prevent an unwanted reset. When the HWEN is driven low (logic '0'), all internal control registers reset to the default states and the part becomes disabled. Please see [Electrical Characteristics](#) for required voltage thresholds.

SYNC PIN

The SYNC pin allows the LM2755 to use an external clock to generate the timing within. This allows the LM2755's current-sinks to pulse-width modulate (PWM) and transition at a user controlled frequency. The PWM frequency and the step-time increment can be set by feeding a clock signal into the SYNC pin and enabling bit 6 in the General Purpose register (See [Electrical Characteristics](#) for more details.). The maximum frequency allowed to ensure current level accuracy is 1MHz. This external clock is divided down by 32x to create the minimum time-step and PWM frequency. For a 1MHz external clock, the PWM frequency becomes 31.25KHz, and the minimum step time becomes 32µseconds. If not used, it is recommended that the SYNC pin be tied to ground.

ADDR PIN

The ADDR pin allows the user to choose between two different I²C chip addresses for the LM2755. Tying the ADDR pin high sets the chip address to hex 67 (0x67 or 67h), while tying the ADDR pin low sets the chip address to hex 18 (0x18 or 18h). This feature allows multiple LM2755's to be used within a system in addition to providing flexibility in the event another chip in the system has a chip address similar to the default LM2755 address (0x18).

I²C-Compatible Interface

DATA VALIDITY

The data on SDIO line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

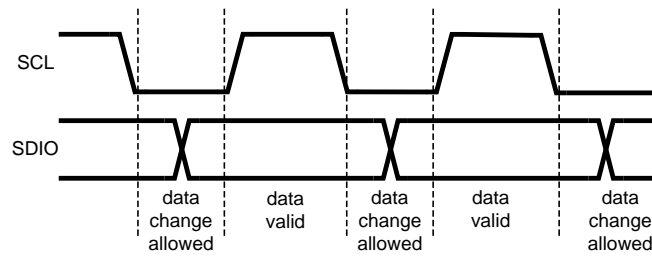


Figure 17. Data Validity Diagram

A pull-up resistor between V_{IO} and SDIO must be greater than $[(V_{IO} - V_{OL}) / 3\text{mA}]$ to meet the V_{OL} requirement on SDIO. Using a larger pull-up resistor results in lower switching current with slower edges, while using a smaller pull-up results in higher switching currents with faster edges.

START AND STOP CONDITIONS

START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as SDIO signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDIO transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise. The data on SDIO line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when CLK is LOW.

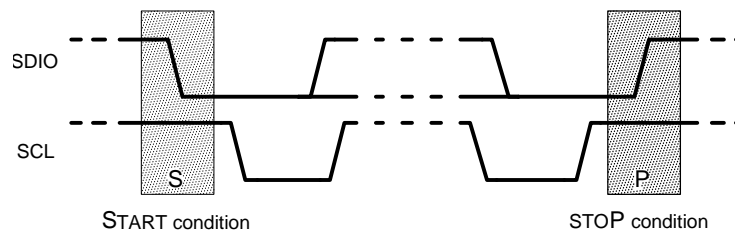
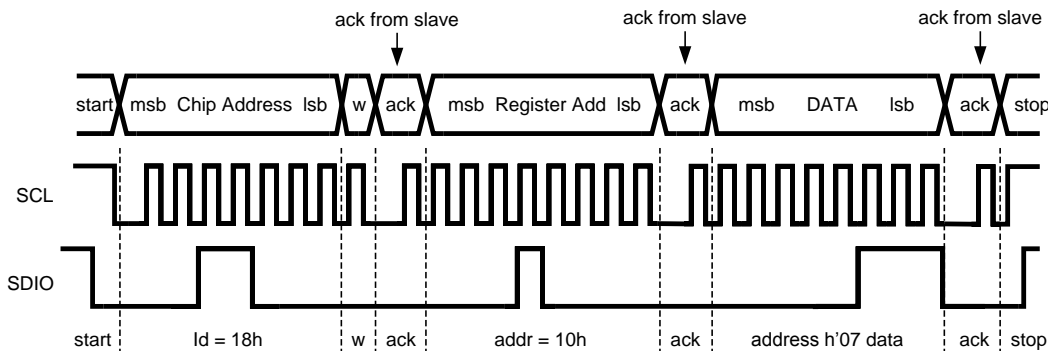


Figure 18. Start and Stop Conditions

TRANSFERRING DATA

Every byte put on the SDIO line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDIO line (HIGH) during the acknowledge clock pulse. The LM2755 pulls down the SDIO line during the 9th clock pulse, signifying an acknowledge. The LM2755 generates an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM2755 address is 18h is ADDR if tied low and 67h if ADDR is tied high. For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.



w = write (SDIO = "0")
 r = read (SDIO = "1")
 ack = acknowledge (SDIO pulled down by either master or slave)
 rs = repeated start
 id = chip address, 18h if ADDR = '0' or 67h if ADDR = '1' for LM2755

Figure 19. Write Cycle

I²C-COMPATIBLE CHIP ADDRESS

The chip address for LM2755 is 0011000 (0x18) when ADDR = '0' or 1100111(0x67) when ADDR = '1'.

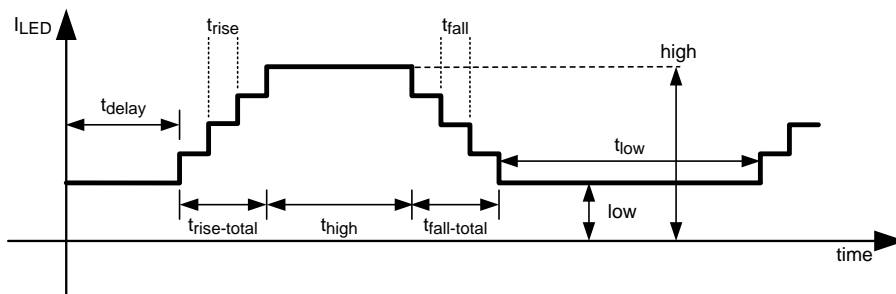


Figure 20. Dimming Waveform

Internal Registers

Table 1. Internal Registers of LM2755

Register Name	Internal Hex Address	Power On Value
General Purpose	x10	0000 0000
Time Step: n _{STEP}	x20	1000 1000
D1 High Level: n _{ID1H}	xA9	1110 0000
D1 Low Level: n _{ID1L}	xA8	1110 0000
D1 Delay: n _{delay1}	xA1	0000 0000
D1 Ramp-Up Step Time: n _{rise1}	xA5	0000 0000 ⁽¹⁾
D1 Time High: n _{high1}	xA3	0000 0000
D1 Ramp-Down Step Time: n _{fall1}	xA4	0000 0000 ⁽¹⁾
D1 Timing: n _{low1}	xA2	0000 0000
D2 High Level: n _{ID2H}	xB9	1110 0000
D2 Low Level: n _{ID2L}	xB8	1110 0000
D2 Delay: n _{delay2}	xB1	0000 0000
D2 Ramp-Up Step Time: n _{rise2}	xB5	0000 0000 ⁽¹⁾

(1) n_{riseix} or n_{fallix} = 0 or 1 are not valid and should not be used

Table 1. Internal Registers of LM2755 (continued)

Register Name	Internal Hex Address	Power On Value
D2 Time High: n_{high2}	xB3	0000 0000
D2 Ramp-Down Step Time: n_{fall2}	xB4	0000 0000 ⁽¹⁾
D2 Timing: n_{low2}	xB2	0000 0000
D3 High Level: n_{ID3H}	xC9	1110 0000
D3 Low Level: n_{ID3L}	xC8	1110 0000
D3 Delay: n_{delay3}	xC1	0000 0000
D3 Ramp-Up Step Time: n_{rise3}	xC5	0000 0000 ⁽¹⁾
D3 Time High: n_{high3}	xC3	0000 0000
D3 Ramp-Down Step Time: n_{fall3}	xC4	0000 0000 ⁽¹⁾
D3 Timing: n_{low3}	xC2	0000 0000

GENERAL PURPOSE REGISTER DESCRIPTION

- Bit 0: enable output D1 with high current level.
- Bit 1: enable output D2 with high current level.
- Bit 2: enable output D3 with high current level.
- Bit 3: enable dimming waveform on output D1.
- Bit 4: enable dimming waveform on output D2.
- Bit 5: enable dimming waveform on output D3.
- Bit 6: enable external clock. '1' = External Clock Sync, '0' = Internal Clock Used
- Bit 7: If Bit 7 = 0 the charge pump is powered on before any dimming waveform is enabled. It is recommended that Bit7 be set to a '0' if an external clock is used. If Bit 7 = 1 the dimming waveform can be enabled before charge pump is powered on.

Application Information

SETTING FULL-SCALE LED CURRENT

The current through the LEDs connected to D1, D2 and D3 can be set to a desired level simply by connecting an appropriately sized resistor (R_{SET}) between the ISET pin of the LM2755 and GND. The LED currents are proportional to the current that flows through the ISET pin and are a factor of 200 times greater than the I_{SET} currents. The feedback loop of the internal amplifier sets the voltage of the ISET pin to 1.25V (typ.). The statement above is simplified in the equation below:

$$I_{Dx (Full-Scale)} = 200 \times (V_{ISET} / R_{SET}) \quad (1)$$

Please refer to [I²C-Compatible Interface](#) for detailed instructions on how to adjust the brightness control registers.

BRIGHTNESS LEVEL CONTROL

Once the desired R_{SET} value has been chosen, the LM2755 can internally dim the LEDs by modulating the currents with an internally set 20kHz PWM signal. The PWM duty cycle percentage is independently set for each LED through the I²C-compatible interface. The 32 brightness levels follow an exponentially increasing pattern rather than a linearly increasing one in order to better match the human eye's response to changing brightness. The brightness level response is modeled in the following equations.:

$$I_{Dx LOW} = (0.9)^{(31-n_{IDxL})} \times I_{Dx Fullscale} \quad (2)$$

$$I_{Dx HIGH} = (0.9)^{(31-n_{IDxH})} \times I_{Dx Fullscale} \quad (3)$$

n_{IDxH} and n_{IDxL} are numbers between 0 and 31 stored in the Brightness Level registers. When the waveform enable bits are set to '1', n_{IDxH} and n_{IDxL} are the brightness level boundaries. These equations apply to all Dx outputs and their corresponding registers. A '0' code in the Brightness Control register sets the current to an "off-state" (0mA).

TIME STEP CONTROL

Bit 0 to Bit 2: The value of these 3 bits is equal to N, which is used in the timing control equations ($0 \leq N \leq 7$). The minimum internal time step (N=0) is 50µs. Setting the time-step to N=7 results in a maximum time step of 6.4msec.

$$t_{STEP} = 50\mu\text{sec} \times 2^{N_{STEP}} \text{ if the internal clock is used.} \quad (4)$$

$$t_{STEP} = 2^{N_{STEP}} \times (32 \div f_{SYNC}) \text{ if the external clock on the SYNC pin is used.} \quad (5)$$

Bit 3 to Bit 7: Not used

DELAY CONTROL

The LM2755 allows the programmed current waveform on each diode pin to independently start with a delay upon enabling the waveform dimming bits in the general purpose register. There are 256 delay levels available. The delay time is set by the following equation:

$$\text{For } n_{STEP} = 0, \quad (6)$$

$$t_{delayx} = t_{STEP} \times (n_{delayx} + n_{risex}) \quad (7)$$

$$\text{By default, } n_{delayx} = 0 \text{ with a range of } 0 \leq n_{delayx} \leq 255. \quad (8)$$

$$\text{For } 1 \leq n_{STEP} \leq 7, t_{delayx} = t_{STEP} \times [(n_{delayx}-1) + (n_{risex}-1)]$$

where

- $1 \leq n_{delayx} \leq 255$.
- If $n_{delayx} = 0$, $t_{delayx} = 0\text{s}$.
- n_{delayx} is stored in the Dx Delay registers. (9)

TIMING CONTROL

n_{risex} , n_{fallx} , n_{highx} , n_{lowx} are numbers between 0 and 255, stored in the timing control registers. The durations of the rise, high, fall and low times are given by:

$$\text{For } n_{STEP} = 0, \quad (10)$$

$$t_{rise/fall} = t_{STEP} \times (n_{IDxH} - n_{IDxL} - 1) \times n_{risex/fallx} \quad (11)$$

where

- $2 \leq n_{risex/fallx} \leq 255$
- **n_{risex} or $n_{fallx} = 0$ or 1 are not valid and should not be used** (12)

$$\text{For } 1 \leq n_{STEP} \leq 7, \quad (13)$$

$$t_{rise/fall} = t_{STEP} \times (n_{IDxH} - n_{IDxL} - 1) \times (n_{risex/fallx} - 1)$$

where

- $2 \leq n_{risex/fallx} \leq 255$
- **n_{risex} or $n_{fallx} = 0$ or 1 are not valid and should not be used** (14)

$$\text{For } n_{STEP} = 0, \quad (15)$$

$$t_{highx} = t_{STEP} \times (n_{highx} + n_{fallx}) \quad t_{lowx} = t_{STEP} \times (n_{lowx} + n_{risex})$$

where

- $1 \leq n_{highx/lowx} \leq 255$
- For $n_{highx/lowx} = 0$, t_{high} or $t_{low} = t_{STEP}$ (16)

$$\text{For } 1 \leq n_{STEP} \leq 7, \quad (17)$$

$$t_{highx} = t_{STEP} \times ((n_{highx} - 1) + (n_{fallx} - 1)) \quad (18)$$

$$t_{lowx} = t_{STEP} \times ((n_{lowx} - 1) + (n_{risex} - 1))$$

where

- $2 \leq n_{highx/lowx} \leq 255$
- For $n_{highx/lowx} = 0$ or 1, $t_{highx} = t_{STEP} \times (n_{fallx} - 1)$
- $t_{lowx} = t_{STEP} \times (n_{risex} - 1)$ (19)

SYNC PIN TIMING CONTROL

It is possible to replace the internal clock with an external one placed on the external SYNC pin. Writing a '1' to bit 6 in the General Purpose register switches the system clock from being internally generated to externally generated. The frequency of the PWM modulating signal becomes:

$$f_{\text{PWM}} = f_{\text{SYNC}} / 32 \quad (20)$$

The maximum recommended SYNC frequency is 1MHz. This frequency yields a PWM frequency of 31.25KHz and the minimum step time of 32μsec.

MAXIMUM OUTPUT CURRENT, MAXIMUM LED VOLTAGE, MINIMUM INPUT VOLTAGE

The LM2755 can drive 3 LEDs at 30mA each (D1, D2, D3) from an input voltage as low as 3.2V, as long as the LEDs have a forward voltage of 3.6V or less (room temperature).

The statement above is a simple example of the LED drive capability of the LM2755. The statement contains the key application parameters that are required to validate an LED-drive design using the LM2755: LED current (I_{LEDx}), number of active LEDs (N_x), LED forward voltage (V_{LED}), and minimum input voltage ($V_{\text{IN-MIN}}$).

The equation below can be used to estimate the maximum output current capability of the LM2755:

$$I_{\text{LED_MAX}} = [(1.5 \times V_{\text{IN}}) - V_{\text{LED}} - (I_{\text{ADDITIONAL}} \times R_{\text{OUT}})] \div [(N_x \times R_{\text{OUT}}) + k_{\text{HRx}}] \quad (21)$$

$$I_{\text{LED_MAX}} = [(1.5 \times V_{\text{IN}}) - V_{\text{LED}} - (I_{\text{ADDITIONAL}} \times 2.4\Omega)] \div [(N_x \times 2.4\Omega) + k_{\text{HRx}}] \quad (22)$$

- $I_{\text{ADDITIONAL}}$ is the additional current that could be delivered to the other LED Groups. (22)

R_{OUT} : Output resistance. This parameter models the internal losses of the charge pump that result in voltage droop at the pump output V_{OUT} . Since the magnitude of the voltage droop is proportional to the total output current of the charge pump, the loss parameter is modeled as a resistance. The output resistance of the LM2755 is typically 2.4Ω ($V_{\text{IN}} = 3.6\text{V}$, $T_A = 25^\circ\text{C}$). In equation form:

$$V_{\text{OUT}} = (1.5 \times V_{\text{IN}}) - [(I_{\text{LED1}} + I_{\text{LED2}} + I_{\text{LED3}}) \times R_{\text{OUT}}] \quad (23)$$

k_{HR} – Headroom constant. This parameter models the minimum voltage required to be present across the current sinks for them to regulate properly. This minimum voltage is proportional to the programmed LED current, so the constant has units of mV/mA. The typical k_{HR} of the LM2755 is 3.25mV/mA. In equation form:

$$(V_{\text{VOUT}} - V_{\text{LEDx}}) > k_{\text{HRx}} \times I_{\text{LEDx}} \quad (24)$$

$$\text{Typical Headroom Constant Values } k_{\text{HR1}} = k_{\text{HR2}} = k_{\text{HR3}} = 10 \text{ mV/mA} \quad (25)$$

The " $I_{\text{LED-MAX}}$ " Equation 21 is obtained from combining the " R_{OUT} " Equation 23 with the " k_{HRx} " Equation 24 and solving for I_{LEDx} . Maximum LED current is highly dependent on minimum input voltage and LED forward voltage. Output current capability can be increased by raising the minimum input voltage of the application, or by selecting an LED with a lower forward voltage. Excessive power dissipation may also limit output current capability of an application.

Total Output Current Capability

The maximum output current that can be drawn from the LM2755 is 90mA. Each driver group has a maximum allotted current per Dx sink that must not be exceeded.

Table 2.

DRIVER TYPE	MAXIMUM Dx CURRENT
Dx	30mA per Dx Pin

The 90mA load can be distributed in many different configurations. Special care must be taken when running the LM2755 at the maximum output current to ensure proper functionality.

POWER EFFICIENCY

Efficiency of LED drivers is commonly taken to be the ratio of power consumed by the LEDs (P_{LED}) to the power drawn at the input of the part (P_{IN}). With a 3/2x - 1x charge pump, the input current is equal to the charge pump gain times the output current (total LED current). The efficiency of the LM2755 can be predicted as follow:

$$P_{\text{LEDTOTAL}} = (V_{\text{LEDA}} \times N_A \times I_{\text{LEDA}}) + (V_{\text{LEDB}} \times N_B \times I_{\text{LEDB}}) + (V_{\text{LEDC}} \times I_{\text{LEDC}}) \quad (26)$$

$$P_{\text{IN}} = V_{\text{IN}} \times I_{\text{IN}} \quad (27)$$

$$P_{\text{IN}} = V_{\text{IN}} \times (\text{GAIN} \times I_{\text{LEDTOTAL}} + I_{\text{Q}}) \quad (28)$$

$$E = (P_{LEDTOTAL} \div P_{IN}) \quad (29)$$

The LED voltage is the main contributor to the charge-pump gain selection process. Use of low forward-voltage LEDs (3.0V to 3.5V) will allow the LM2755 to stay in the gain of 1x for a higher percentage of the lithium-ion battery voltage range when compared to the use of higher forward voltage LEDs (3.5V to 4.0V). See [LED FORWARD VOLTAGE MONITORING](#) for a more detailed description of the gain selection and transition process.

For an advanced analysis, it is recommended that power consumed by the circuit ($V_{IN} \times I_{IN}$) for a given load be evaluated rather than power efficiency.

POWER DISSIPATION

The power dissipation (P_{DISS}) and junction temperature (T_J) can be approximated with the equations below. P_{IN} is the power generated by the 3/2x - 1x charge pump, P_{LED} is the power consumed by the LEDs, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance for the DSBGA 18-bump package. V_{IN} is the input voltage to the LM2755, V_{LED} is the nominal LED forward voltage, N is the number of LEDs and I_{LED} is the programmed LED current.

$$P_{DISS} = P_{IN} - P_{LED1} - P_{LED2} - P_{LED3} \quad (30)$$

$$P_{DISS} = (GAIN \times V_{IN} \times I_{D1} + D2 + D3) - (V_{LED1} \times I_{LED1}) - (V_{LED2} \times I_{LED2}) - (V_{LED3} \times I_{LED3}) \quad (31)$$

$$T_J = T_A + (P_{DISS} \times \theta_{JA}) \quad (32)$$

The junction temperature rating takes precedence over the ambient temperature rating. The LM2755 may be operated outside the ambient temperature rating, as long as the junction temperature of the device does not exceed the maximum operating rating of 105°C. The maximum ambient temperature rating must be derated in applications where high power dissipation and/or poor thermal resistance causes the junction temperature to exceed 105°C.

THERMAL PROTECTION

Internal thermal protection circuitry disables the LM2755 when the junction temperature exceeds 160°C (typ.). This feature protects the device from being damaged by high die temperatures that might otherwise result from excessive power dissipation. The device will recover and operate normally when the junction temperature falls below 155°C (typ.). It is important that the board layout provide good thermal conduction to keep the junction temperature within the specified operating ratings.

CAPACITOR SELECTION

The LM2755 requires 4 external capacitors for proper operation ($C_{IN} = C_{OUT} = 1\mu F$, $C_1 = C_2 = 0.47\mu F$). Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive and have very low equivalent series resistance (ESR <20mΩ typ.). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors are not recommended for use with the LM2755 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LM2755. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over -55°C to 125°C; X5R: ±15% over -55°C to 85°C).

Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the LM2755. Capacitors with these temperature characteristics typically have wide capacitance tolerance (+80%, -20%) and vary significantly over temperature (Y5V: +22%, -82% over -30°C to +85°C range; Z5U: +22%, -56% over +10°C to +85°C range). Under some conditions, a nominal 1μF Y5V or Z5U capacitor could have a capacitance of only 0.1μF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM2755.

The recommended voltage rating for the capacitors is 10V to account for DC bias capacitance losses.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM2755TM/NOPB	ACTIVE	DSBGA	YFQ	18	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D32	Samples
LM2755TMX/NOPB	ACTIVE	DSBGA	YFQ	18	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	D32	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

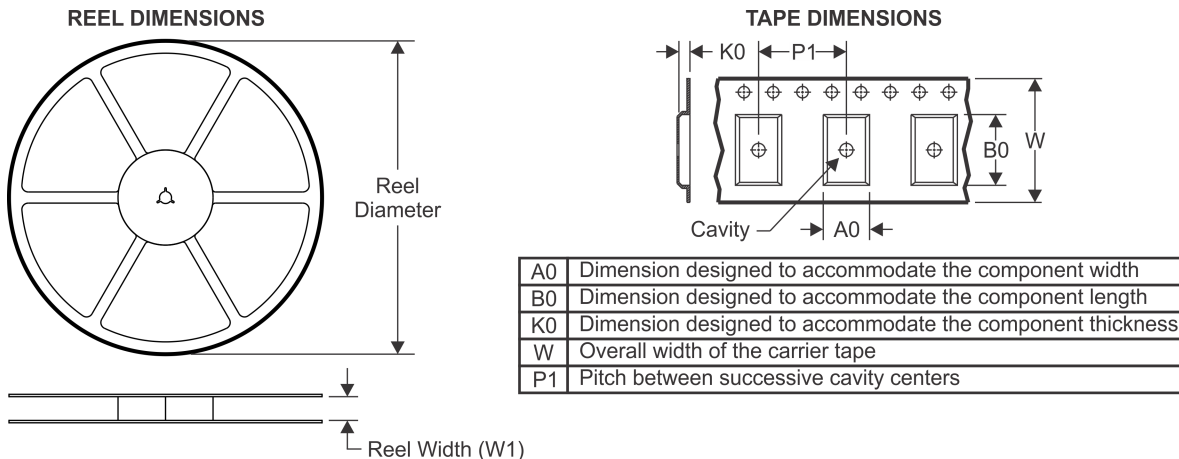
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2755TM/NOPB	DSBGA	YFQ	18	250	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1
LM2755TMX/NOPB	DSBGA	YFQ	18	3000	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2755TM/NOPB	DSBGA	YFQ	18	250	210.0	185.0	35.0
LM2755TMX/NOPB	DSBGA	YFQ	18	3000	210.0	185.0	35.0

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View LM2755TMX](#) on WIN SOURCE

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management