THE DATASHEET OF

LM10CN/NOPB

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LM10 Operational Amplifier and Voltage Reference

1 Features

- Input Offset Voltage: 2 mV (Maximum)
- Input Offset Current: 0.7 nA (Maximum)
- Input Bias Current: 20 nA (Maximum)
- Reference Regulation: 0.1% (Maximum)
- Offset Voltage Drift: 2 µV/°C
- Reference Drift: 0.002%/°C

2 Applications

- Remote Amplifiers
- Battery-Level Indicators
- Thermocouple Transmitters
- Voltage and Current regulators

3 Description

The LM10 series are monolithic linear ICs consisting of a precision reference, an adjustable reference buffer and an independent, high-quality operational amplifier.

The unit can operate from a total supply voltage as low as 1.1 V or as high as 40 V, drawing only 270 µA. A complementary output stage swings within 15 mV of the supply terminals or will deliver ±20-mA output current with ±0.4-V saturation. Reference output can be as low as 200 mV.

The circuit is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-purpose applications.

The device is capable of operating in a floating mode, independent of fixed supplies. It can function as a remote comparator, signal conditioner, SCR controller or transmitter for analog signals, delivering the processed signal on the same line used to supply power. It is also suited for operation in a wide range of voltage and current regulator applications, from low voltages to several hundred volts, providing greater precision than existing ICs.

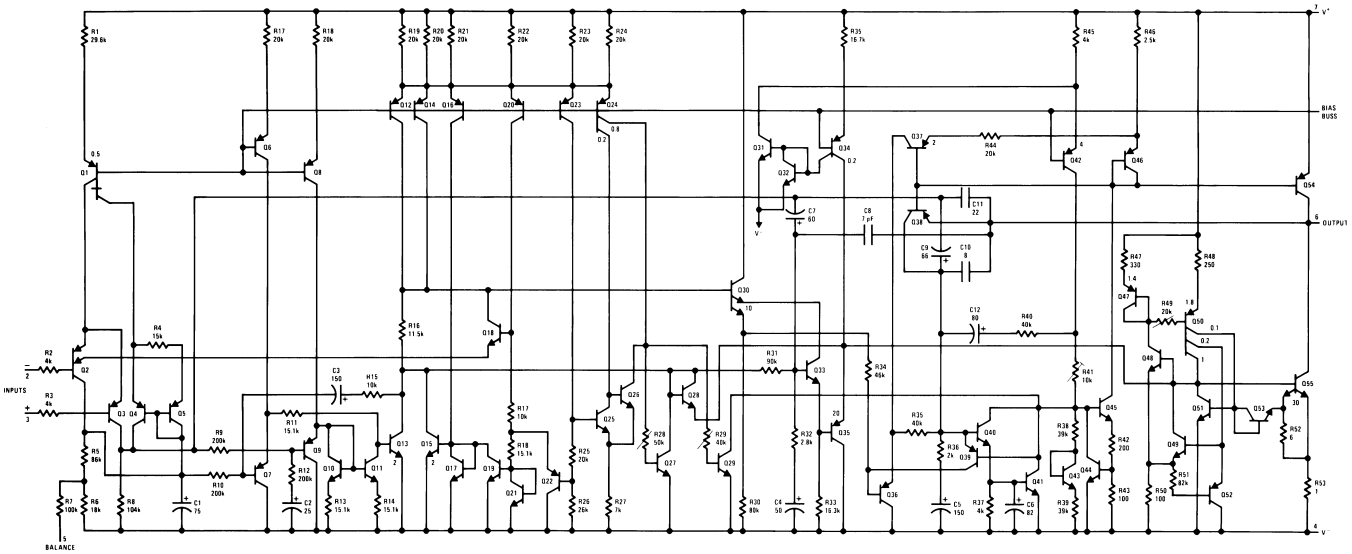
This series is available in the three standard temperature ranges, with the commercial part having relaxed limits. In addition, a low-voltage specification (suffix L) is available in the limited temperature ranges at a cost savings.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM10	SOIC (14)	8.992 mm × 7.498 mm
	SDIP (8)	8.255 mm × 8.255 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Operational Amplifier Schematic



(Pin numbers are for 8-pin packages)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 Recommended Operating Conditions ... 4
6.3 Thermal Information ... 4
6.4 Electrical Characteristics LM10/LM10B ... 5
6.5 Electrical Characteristics, LM10C ... 6
6.6 Electrical Characteristics, LM10BL ... 8
6.7 Electrical Characteristics, LM10CL ... 9
6.8 Typical Characteristics ... 11
7 Detailed Description ... 17
7.1 Overview ... 17
7.2 Functional Block Diagram ... 17
7.3 Feature Description ... 17
7.4 Device Functional Modes ... 17
8 Application and Implementation ... 18
8.1 Application Information ... 18
8.2 Typical Application ... 18
8.3 System Examples ... 19
9 Power Supply Recommendations ... 27
10 Layout ... 27
10.1 Layout Guidelines ... 27
10.2 Layout Example ... 27
11 Device and Documentation Support ... 28
11.1 Device Support ... 28
11.2 Documentation Support ... 28
11.3 Community Resources ... 28
11.4 Trademarks ... 29
11.5 Electrostatic Discharge Caution ... 29
11.6 Glossary ... 29
12 Mechanical, Packaging, and Orderable Information ... 29

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (March 2013) to Revision D **Page**

- Changed layout of National Data Sheet to TI format ... 26

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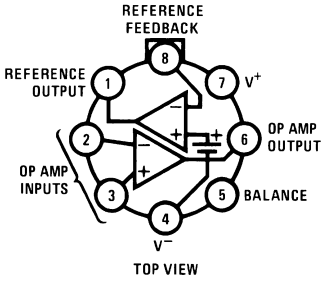
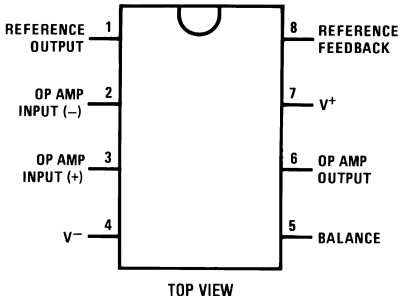
5 Pin Configuration and Functions

NEV Package
8-Pin SDIP
Top View



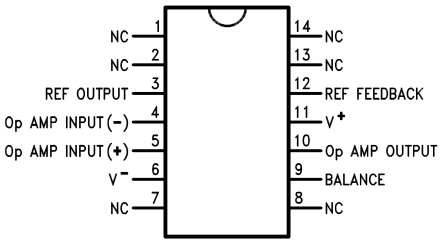
P Package
8-Pin PDIP
Top View



Pin Functions — 8-Pin SDIP or PDIP

PIN		I/O	DESCRIPTION
NAME	NO.		
Balance	5	I	Used for offset nulling
Op Amp Input (+)	3	I	Noninverting input of operational amplifier
Op Amp Input (–)	2	I	Inverting input of operational amplifier
Op Amp Output	6	O	Output terminal of operational amplifier
Reference Feedback	8	I	Feedback terminal of reference
Reference Output	1	O	Output terminal of reference
V+	7	I	Positive supply voltage
V–	4	I	Negative supply voltage

NPA Package
14-Pin SOIC
Top View



Pin Functions — 14-Pin SOIC

PIN		I/O	DESCRIPTION
NAME	NO.		
Balance	9	I	Used for offset nulling
NC	1, 2, 7, 8, 14, 13	—	No connection
Op Amp Input (–)	4	I	Inverting input of operational amplifier
Op Amp Input (+)	5	I	Noninverting input of operational amplifier
Op Amp Output	10	O	Output terminal of operational amplifier
Reference Feedback	12	I	Feedback terminal of reference
Reference Output	3	O	Output terminal of reference
V+	11	I	Positive supply voltage
V–	6	I	Negative supply voltage

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6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)(3)

			MIN	MAX	UNIT
Total supply voltage	LM10/LM10B/LM10C			45	V
	LM10BL/LM10CL			7	V
Differential input voltage(4)	LM10/LM10B/LM10C			±40	V
	LM10BL/LM10CL			±7	V
Power dissipation(5)			Internally limited		
Output short-circuit duration(6)			Continuous		
Lead temperature	TO	Soldering (10 seconds)		300	°C
	DIP	Soldering (10 seconds)		260	°C
		Vapor phase (60 seconds)		215	°C
		Infrared (15 seconds)		220	°C
Maximum junction temperature	LM10			150	°C
	LM10B			100	°C
	LM10C			85	°C
Storage temperature, T_{stg}			−55	150	°C

(1) Refer to RETS10X for LM10H military specifications.
(2) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) The Input voltage can exceed the supply voltages provided that the voltage from the input to any other terminal does not exceed the maximum differential input voltage and excess dissipation is accounted for when $V_{IN} < V^-$.
(5) The maximum, operating-junction temperature is 150°C for the LM10, 100°C for the LM10B(L) and 85°C for the LM10C(L). At elevated temperatures, devices must be derated based on package thermal resistance.
(6) Internal thermal limiting prevents excessive heating that could result in sudden failure, but the IC can be subjected to accelerated stress with a shorted output and worst-case conditions.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply input voltage range (V–) – (V+)	1.2		40	V
V_{CM}	Common-mode voltage	(V–)		(V+) – 0.85	V
V_{REF}	Reference voltage		0.2		V
I_{REF}	Reference current	0		1	mA

6.3 Thermal Information

THERMAL METRIC(1)		LM10			UNIT
		NEV (SDIP)	NPA (SOIC)	P (PDIP)	
		8 PINS	14 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	90	87	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.4 Electrical Characteristics LM10/LM10B

T_J=25°C unless otherwise specified(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage	T_J=25°C		0.3	2	mV
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))			3	mV
Input offset current(2)	T_J=25°C		0.25	0.7	nA
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))			1.5	nA
Input bias current	T_J=25°C		10	20	nA
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))			30	nA
Input resistance	T_J=25°C	250	500		kΩ
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))	150			kΩ
Large signal voltage gain	V_S = ±20 V, I_{OUT} = 0	120	400		V/mV
	V_{OUT} = ±19.95 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	80			V/mV
	V_S = ±20 V, V_{OUT} = ±19.4 V	50	130		V/mV
	I_{OUT} = ±20 mA, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	20			V/mV
	I_{OUT} = ±15 mA, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	20			V/mV
	V_S = ±0.6 V, I_{OUT} = ±2 mA	1.5	3		V/mV
	V_S = ±0.65 V, I_{OUT} = ±2 mA, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	1.5	3		V/mV
	V_{OUT} = ±0.4 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	0.5			V/mV
	V_{OUT} = ±0.3 V, V_{CM} = −0.4 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	0.5			V/mV
Shunt gain(3)	1.2 V ≤ V_{OUT} ≤ 40 V, R_L = 1.1 kΩ	14	33		V/mV
	1.3 V ≤ V_{OUT} ≤ 40 V, R_L = 1.1 kΩ, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	14	33		V/mV
	0.1 mA ≤ I_{OUT} ≤ 5 mA, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	6			V/mV
	1.5 V ≤ V^+ ≤ 40 V, R_L = 250 Ω	8	25		V/mV
	0.1 mA ≤ I_{OUT} ≤ 20 mA, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	4			V/mV
Common-mode rejection	−20 V ≤ V_{CM} ≤ 19.15 V	93	102		dB
	−20 V ≤ V_{CM} ≤ 19 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	93	102		dB
	V_S = ±20 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	87			dB
Supply-voltage rejection	−0.2 V ≥ V^- ≥ −39 V	90	96		dB
	V^+ = 1 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	84			dB
	V^+ = 1.1 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	84			dB
	1 V ≤ V^+ ≤ 39.8 V	96	106		dB
	1.1 V ≤ V^+ ≤ 39.8 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	96	106		dB
	V^- = −0.2 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	90			dB
Offset voltage drift			2		µV/°C
Offset current drift			2		pA/°C
Bias current drift	T_C < 100°C		60		pA/°C
Line regulation	1.2 V ≤ V_S ≤ 40 V		0.001	0.003	%/V
	1.3 V ≤ V_S ≤ 40 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))		0.001	0.003	%/V
	0 ≤ I_{REF} ≤ 1 mA, V_{REF} = 200 mV, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))			0.006	%/V
Load regulation	0 ≤ I_{REF} ≤ 1 mA		0.01%	0.1%	
	$V^+ - V_{REF}$ ≥ 1 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))			0.15%	
	$V^+ - V_{REF}$ ≥ 1.1 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))			0.15%	

(1) These specifications apply for $V^- \le V_{CM} \le V^+ - 0.85$ V, 1 V ($T_{MIN} \le T_J \le T_{MAX}$), 1.2 V, 1.3 V ($T_{MIN} \le T_J \le T_{MAX}$) < $V_S \le V_{MAX}$, V_{REF} = 0.2 V and 0 ≤ I_{REF} ≤ 1 mA, unless otherwise specified: V_{MAX} = 40 V for the standard part and 6.5 V for the low voltage part. The full-temperature-range operation is −55°C to 125°C for the LM10, −25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients ($\tau_1 \approx 20$ ms), die heating ($\tau_2 \approx 0.2$ s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

(2) For T_J > 90°C, I_{OS} may exceed 1.5 nA for $V_{CM} = V^-$. With T_J = 125°C and $V^- \le V_{CM} \le V^- + 0.1$ V, $I_{OS} \le 5$ nA.

(3) This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see *System Examples*). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

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Electrical Characteristics LM10/LM10B (continued)

T_J=25°C unless otherwise specified(1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Amplifier gain	0.2 V ≤ V_{REF} ≤ 35 V	T_J=25°C	50	75		V/mV
		T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))	23			V/mV
Feedback sense voltage	T_J=25°C		195	200	205	mV
	T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))		194		206	mV
Feedback current	T_J=25°C			20	50	nA
	T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))				65	nA
Reference drift				0.002		%/°C
Supply current	T_J=25°C			270	400	µA
	T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))				500	µA
Supply current change	1.2 V ≤ V_S ≤ 40 V	T_J=25°C		15		µA
		T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))			75	µA
	1.3 V ≤ V_S ≤ 40 V	T_J=25°C		15		µA
		T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))			75	µA

6.5 Electrical Characteristics, LM10C

T_J=25°C unless otherwise specified(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage	T_J=25°C		0.5	4	mV
	T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))			5	mV
Input offset current(2)	T_J=25°C		0.4	2	nA
	T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))			3	nA
Input bias current	T_J=25°C		12	30	nA
	T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))			40	nA
Input resistance	T_J=25°C	150	400		kΩ
	T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))	115			kΩ
Large signal voltage gain	V_S = ±20 V, I_{OUT} = 0	80	400		V/mV
	V_{OUT} = ±19.95 V, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))	50			V/mV
	V_S = ±20 V, V_{OUT} = ±19.4 V	25	130		V/mV
	I_{OUT} = ±20 mA, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))	15			V/mV
	I_{OUT} = ±15 mA, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))	15			V/mV
	V_S = ±0.6 V, I_{OUT} = ±2 mA	1	3		V/mV
	V_S = 0.65 V, I_{OUT} = ±2 mA, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))	1	3		V/mV
	V_{OUT} = ±0.4 V, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))	0.75			V/mV
	V_{OUT} = ±0.3 V, V_{CM} = −0.4 V, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))	0.75			V/mV
Shunt gain(3)	1.2 V ≤ V_{OUT} ≤ 40 V, R_L = 1.1 kΩ	10	33		V/mV
	1.3 V ≤ V_{OUT} ≤ 40 V, R_L = 1.1 kΩ, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))	10	33		V/mV
	0.1 mA ≤ I_{OUT} ≤ 5 mA, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))	6			V/mV
	1.5 V ≤ V^+ ≤ 40 V, R_L = 250 Ω	6	25		V/mV
	0.1 mA ≤ I_{OUT} ≤ 20 mA, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))	4			V/mV

(1) These specifications apply for V^- ≤ V_{CM} ≤ V^+− 0.85 V, 1 V (T_{MIN} ≤ T_J ≤ T_{MAX}), 1.2 V, 1.3 V (T_{MIN} ≤ T_J ≤ T_{MAX}) < V_S ≤ V_{MAX}, V_{REF} = 0.2 V and 0 ≤ I_{REF} ≤ 1 mA, unless otherwise specified: V_{MAX} = 40 V for the standard part and 6.5 V for the low voltage part. The full-temperature-range operation is −55°C to 125°C for the LM10, −25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients (τ_1 ≈ 20 ms), die heating (τ_2 ≈ 0.2 s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

(2) For T_J > 90°C, I_{OS} may exceed 1.5 nA for V_{CM} = V^-. With T_J = 125°C and V^- ≤ V_{CM} ≤ V^- + 0.1 V, I_{OS} ≤ 5 nA.

(3) This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see *System Examples*). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

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Electrical Characteristics, LM10C (continued)

T_J=25°C unless otherwise specified(1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Common-mode rejection	−20 V ≤ V_{CM} ≤ 19.15 V		90	102		dB
	−20 V ≤ V_{CM} ≤ 19 V		90	102		dB
	V_S = ±20 V, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))		87			dB
Supply-voltage rejection	−0.2 V ≥ V^- ≥ −39 V		87	96		dB
	V^+ = 1 V, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))		84			dB
	V^+ = 1.1 V, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))		84			dB
	1 V ≤ V^+ ≤ 39.8 V		93	106		dB
	1.1 V ≤ V^+ ≤ 39.8 V, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))		93	106		dB
	V^- = −0.2 V, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))		90			dB
Offset voltage drift				5		µV/°C
Offset current drift				5		pA/°C
Bias current drift	T_C < 100°C			90		pA/°C
Line regulation	1.2 V ≤ V_S ≤ 40 V			0.001	0.008	%/V
	1.3 V ≤ V_S ≤ 40 V, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))			0.001	0.008	%/V
	0 ≤ I_{REF} ≤ 1 mA, V_{REF} = 200 mV, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))				0.01	%/V
Load regulation	0 ≤ I_{REF} ≤ 1 mA			0.01%	0.15%	
	V^+ − V_{REF} ≥ 1 V, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))				0.2%	
	V^+ − V_{REF}≥ 1.1 V, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))				0.2%	
Amplifier gain	0.2 V ≤ V_{REF} ≤ 35 V	T_J=25°C	25	70		V/mV
		T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))	15			V/mV
Feedback sense voltage	T_J=25°C		190	200	210	mV
	T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))		189		211	mV
Feedback current	T_J=25°C			22	75	nA
	T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))				90	nA
Reference drift				0.003		%/°C
Supply current	T_J=25°C			300	500	µA
	T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))				570	µA
Supply current change	1.2 V ≤ V_S ≤ 40 V	T_J=25°C		15		µA
		T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))			75	
	1.3 V ≤ V_S ≤ 40 V	T_J=25°C		15		µA
		T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))			75	

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6.6 Electrical Characteristics, LM10BL

T_J=25°C unless otherwise specified.(1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage	T_J=25°C			0.3	2	mV
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))				3	mV
Input offset current(2)	T_J=25°C			0.1	0.7	nA
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))				1.5	nA
Input bias current	T_J=25°C			10	20	nA
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))				30	nA
Input resistance	T_J=25°C		250	500		kΩ
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))		150			kΩ
Large signal voltage gain	V_S = ±3.25 V, I_{OUT} = 0		60	300		V/mV
	V_{OUT} = ±3.2 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))		40			V/mV
	V_S = ±3.25 V, I_{OUT} = 10 mA		10	25		V/mV
	V_{OUT} = ±2.75 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))		4			V/mV
	V_S = ±0.6 V, I_{OUT} = ±2 mA		1.5	3		V/mV
	V_S = 0.65 V, I_{OUT} = ±2 mA, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))		1.5	3		V/mV
	V_{OUT} = ±0.4 V, V_{CM} = −0.4 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))		0.5			V/mV
	V_{OUT} = ±0.3 V, V_{CM} = −0.4 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))		0.5			V/mV
Shunt gain(3)	1.5 V ≤ V^+ ≤ 6.5 V, R_L = 500 Ω		8	30		V/mV
	0.1 mA ≤ I_{OUT} ≤ 10 mA, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))		4			V/mV
Common-mode rejection	−3.25 V ≤ V_{CM} ≤ 2.4 V		89	102		dB
	−3.25 V ≤ V_{CM} ≤ 2.25 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))					
	V_S = ±3.25 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))		83			dB
Supply-voltage rejection	−0.2 V ≥ V^- ≥ −5.4 V		86	96		dB
	V^+ = 1 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))		80			dB
	V^+ = 1.2 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))		80			dB
	1 V ≤ V^+ ≤ 6.3 V		94	106		dB
	1.1 V ≤ V^+ ≤ 6.3 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))		94	106		dB
	V^-=0.2 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))		88			dB
Offset voltage drift				2		µV/°C
Offset current drift				2		pA/°C
Bias current drift				60		pA/°C
Line regulation	1.2 V ≤ V_S ≤ 6.5 V			0.001	0.01	%/V
	1.3 V ≤ V_S ≤ 6.5 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))			0.001	0.01	%/V
	0 ≤ I_{REF} ≤ 0.5 mA, V_{REF} = 200 mV, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))				0.02	%/V
Load regulation	0 ≤ I_{REF} ≤ 0.5 mA			0.01%	0.1%	
	$V^+ - V_{REF}$ ≥ 1 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))				0.15%	
	$V^+ - V_{REF}$ ≥ 1.1 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))				0.15%	
Amplifier gain	0.2 V ≤ V_{REF} ≤ 5.5 V	T_J=25°C	30	70		V/mV
		$T_{MIN} \le T_J \le T_{MAX}$ (see (1))	20			V/mV
Feedback sense voltage	T_J=25°C		195	200	205	mV
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))		194		206	mV

(1) These specifications apply for $V^- \le V_{CM} \le V^+ - 0.85$ V, 1 V ($T_{MIN} \le T_J \le T_{MAX}$), 1.2 V, 1.3 V ($T_{MIN} \le T_J \le T_{MAX}$) < $V_S \le V_{MAX}$, V_{REF} = 0.2 V and 0 ≤ I_{REF} ≤ 1 mA, unless otherwise specified: V_{MAX} = 40 V for the standard part and 6.5 V for the low voltage part. The full-temperature-range operation is −55°C to 125°C for the LM10, −25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients (τ_1 ≈ 20 ms), die heating (τ_2 ≈ 0.2 s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

(2) For T_J > 90°C, I_{OS} may exceed 1.5 nA for $V_{CM} = V^-$. With T_J=125°C and $V^- \le V_{CM} \le V^-$ + 0.1 V, I_{OS} ≤ 5 nA.

(3) This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see *System Examples*). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

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Electrical Characteristics, LM10BL (continued)

T_J=25°C unless otherwise specified.(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Feedback current	T_J=25°C		20	50	nA
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))			65	nA
Reference drift			0.002		%/°C
Supply current	T_J=25°C		260	400	µA
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))			500	µA

6.7 Electrical Characteristics, LM10CL

T_J=25°C unless otherwise specified.(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage	T_J=25°C		0.5	4	mV
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))			5	mV
Input offset current(2)	T_J=25°C		0.2	2	nA
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))			3	nA
Input bias current	T_J=25°C		12	30	nA
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))			40	nA
Input resistance	T_J=25°C	150	400		kΩ
	$T_{MIN} \le T_J \le T_{MAX}$ (see (1))	115			kΩ
Large signal voltage gain	V_S = ±3.25 V, I_{OUT} = 0	40	300		V/mV
	V_{OUT} = ±3.2 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	25			V/mV
	V_S = ±3.25 V, I_{OUT} = 10 mA	5	25		V/mV
	V_{OUT} = ±2.75 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	3			V/mV
	V_S = ±0.6 V, I_{OUT} = ±2 mA	1	3		V/mV
	V_S = 0.65 V, I_{OUT} = ±2 mA, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	1	3		V/mV
	V_{OUT} = ±0.4 V, V_{CM} = −0.4 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	0.75			V/mV
	V_{OUT} = ±0.3 V, V_{CM} = −0.4 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	0.75			V/mV
Shunt gain(3)	1.5 V ≤ V^+ ≤ 6.5 V, R_L= 500 Ω	6	30		V/mV
	0.1 mA ≤ I_{OUT} ≤ 10 mA, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	4			V/mV
Common-mode rejection	−3.25 V ≤ V_{CM} ≤ 2.4 V	80	102		dB
	−3.25 V ≤ V_{CM} ≤ 2.25 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	80	102		dB
	V_S = ±3.25 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	74			dB
Supply-voltage rejection	−0.2 V ≥ V^- ≥ −5.4 V	80	96		dB
	V^+ = 1 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	74			dB
	V^+ = 1.2 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	74			dB
	1 V ≤ V^+ ≤ 6.3 V	80	106		dB
	1.1 V ≤ V^+ ≤ 6.3 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	80	106		dB
	V^- = 0.2 V, $T_{MIN} \le T_J \le T_{MAX}$ (see (1))	74			dB
Offset voltage drift			5		µV/°C
Offset current drift			5		pA/°C
Bias current drift			90		pA/°C

(1) These specifications apply for V^- ≤ V_{CM} ≤ V^+− 0.85 V, 1 V ($T_{MIN} \le T_J \le T_{MAX}$), 1.2 V, 1.3 V ($T_{MIN} \le T_J \le T_{MAX}$) < $V_S \le V_{MAX}$, V_{REF} = 0.2 V and 0 ≤ I_{REF} ≤ 1 mA, unless otherwise specified: V_{MAX} = 40 V for the standard part and 6.5 V for the low voltage part. The full-temperature-range operation is −55°C to 125°C for the LM10, −25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients (τ_1 ≈ 20 ms), die heating (τ_2 ≈ 0.2 s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

(2) For T_J > 90°C, I_{OS} may exceed 1.5 nA for V_{CM} = V^-. With T_J = 125°C and V^- ≤ V_{CM} ≤ V^- + 0.1 V, I_{OS} ≤ 5 nA.

(3) This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see *System Examples*). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

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Electrical Characteristics, LM10CL (continued)

T_J=25°C unless otherwise specified.(1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Line regulation	1.2 V ≤ V_S ≤ 6.5 V			0.001	0.02	%/V
	1.3 V ≤ V_S ≤ 6.5 V, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))			0.001	0.02	%/V
	0 ≤ I_{REF} ≤ 0.5 mA, V_{REF} = 200 mV, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))				0.03	%/V
Load regulation	0 ≤ I_{REF} ≤ 0.5 mA			0.01%	0.15%	
	$V^+ - V_{REF}$ ≥ 1 V, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))				0.2%	
	$V^+ - V_{REF}$ ≥ 1.1 V, T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))				0.2%	
Amplifier gain	0.2 V ≤ V_{REF} ≤ 5.5 V	T_J=25°C	20	70		V/mV
		T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))	15			V/mV
Feedback sense voltage	T_J=25°C		190	200	210	mV
	T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))		189		211	mV
Feedback current	T_J=25°C			22	75	nA
	T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))				90	nA
Reference drift				0.003		%/°C
Supply current	T_J=25°C			280	500	µA
	T_{MIN} ≤ T_J ≤ T_{MAX} (see (1))				570	µA

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6.8 Typical Characteristics

6.8.1 Typical Characteristics (Op Amp)

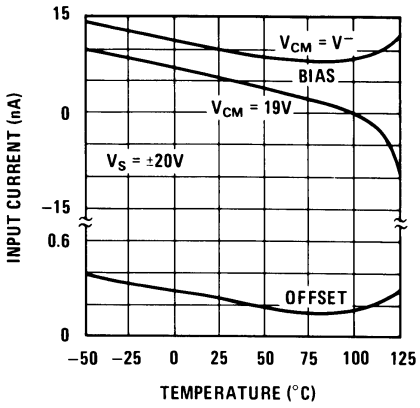

Figure 1. Input Current

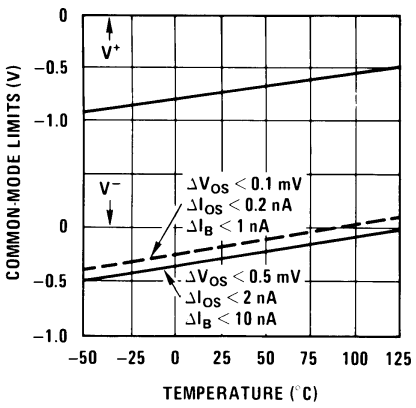

Figure 2. Common-Mode Limits

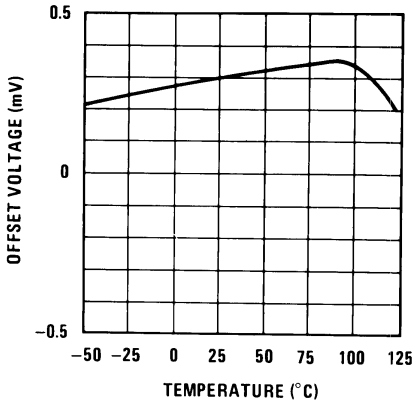

Figure 3. Output Voltage Drift

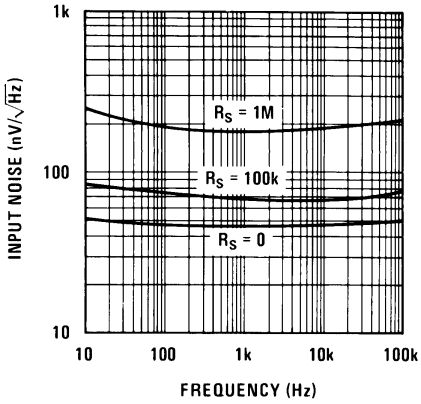

Figure 4. Input Noise Voltage

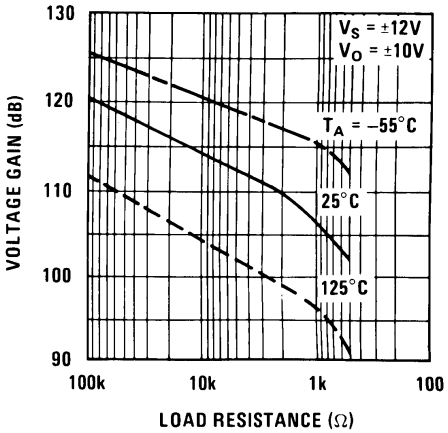

Figure 5. DC Voltage Gain

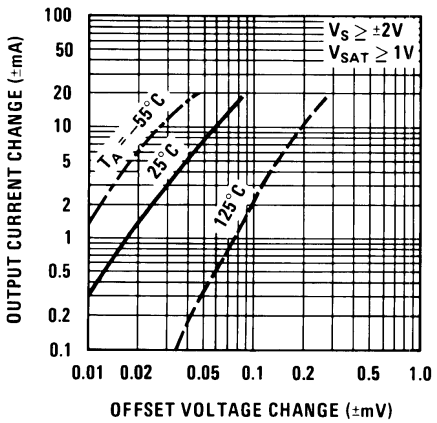

Figure 6. Transconductance

Typical Characteristics (Op Amp) (continued)

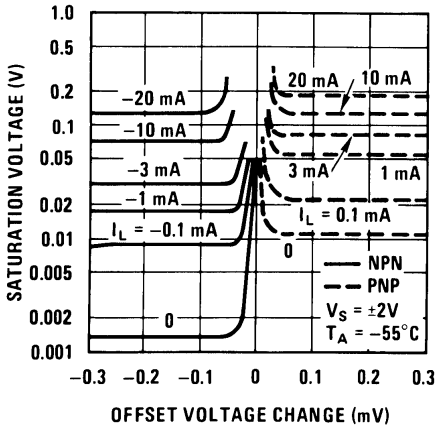

Figure 7. Output Saturation Characteristics

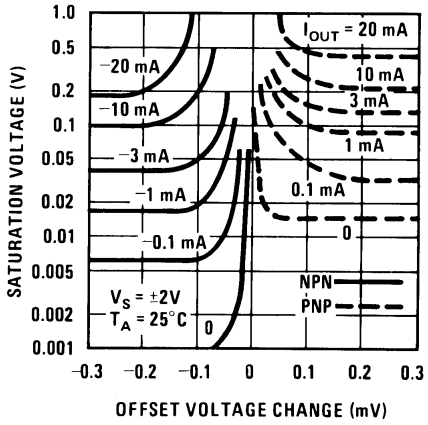

Figure 8. Output Saturation Characteristics

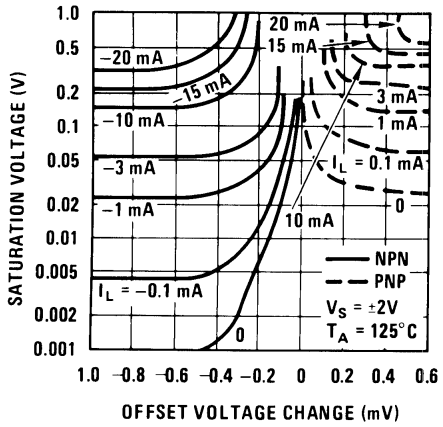

Figure 9. Output Saturation Characteristics

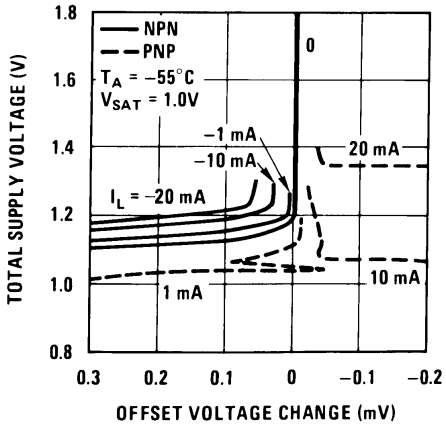

Figure 10. Minimum Supply Voltage

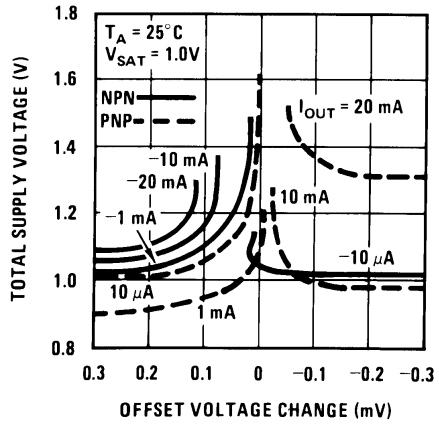

Figure 11. Minimum Supply Voltage

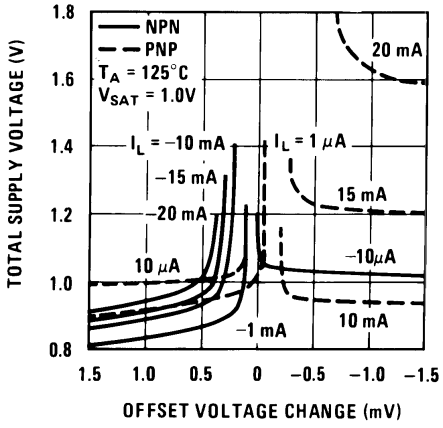

Figure 12. Minimum Supply Voltage

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Typical Characteristics (Op Amp) (continued)

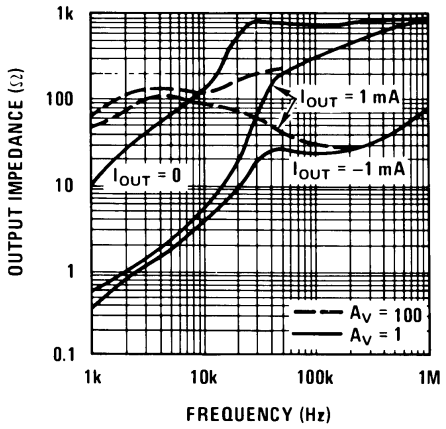

Figure 13. Output Impedance

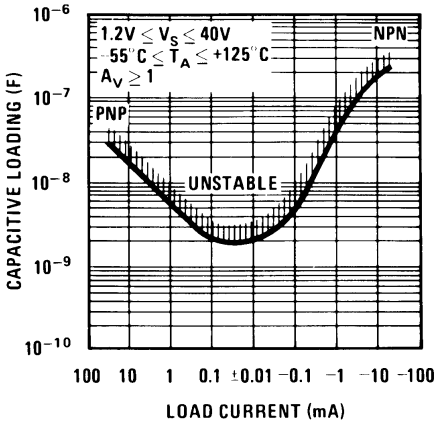

Figure 14. Typical Stability Range

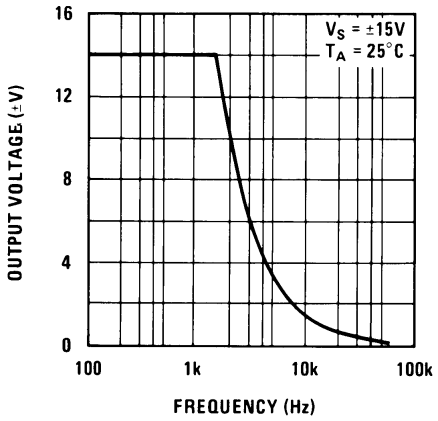

Figure 15. Large Signal Response

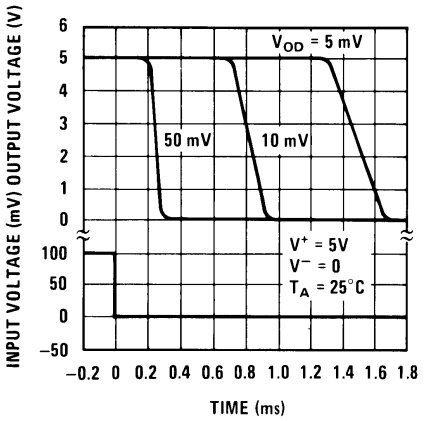

Figure 16. Comparator Response Time For Various Input Overdrives

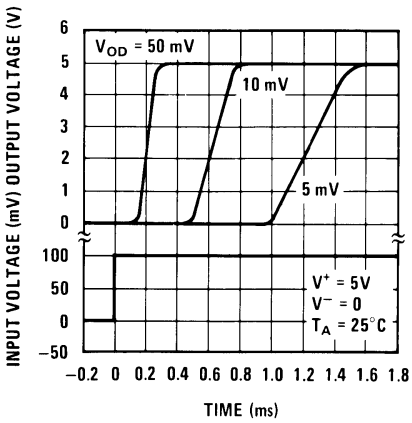

Figure 17. Comparator Response Time For Various Input Overdrives

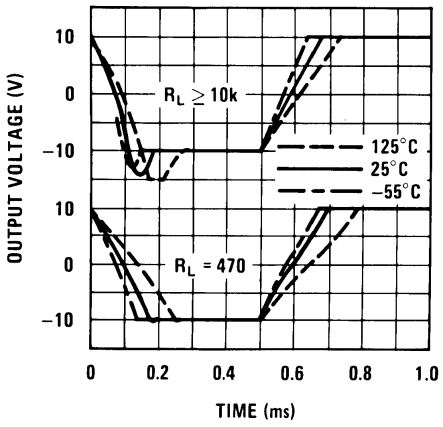

Figure 18. Follower Pulse Response

Typical Characteristics (Op Amp) (continued)

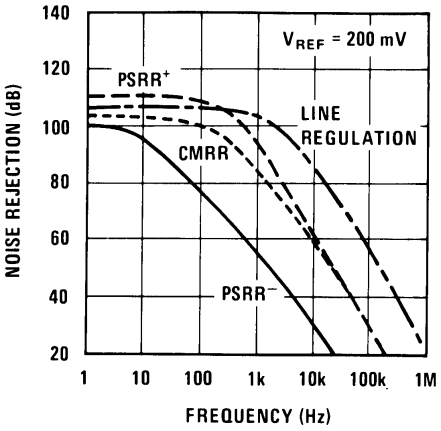

Figure 19. Noise Rejection

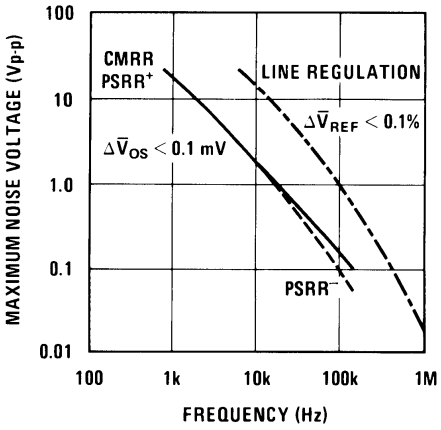

Figure 20. Rejection Slew Limiting

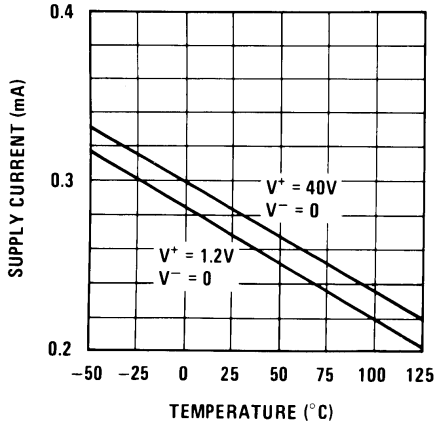

Figure 21. Supply Current

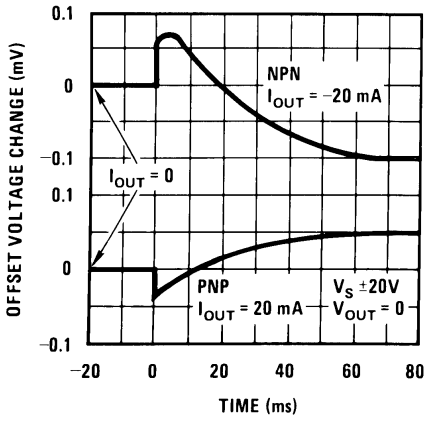

Figure 22. Thermal Gradient Feedback

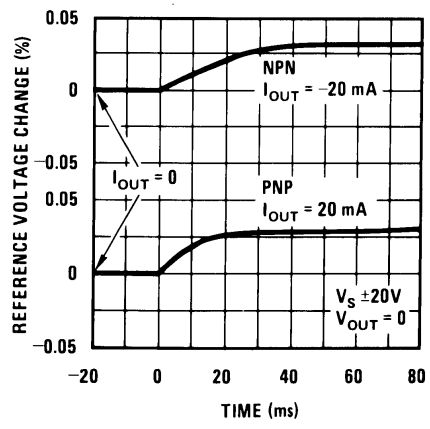

Figure 23. Thermal Gradient Cross-Coupling

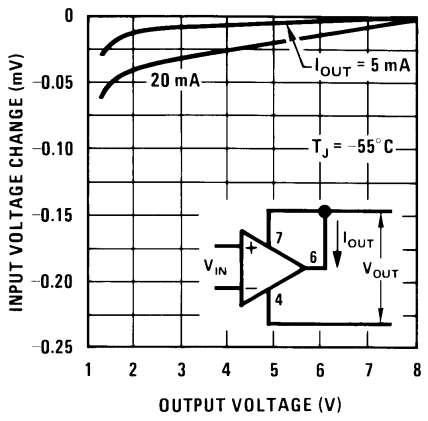

Figure 24. Shunt Gain

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Typical Characteristics (Op Amp) (continued)

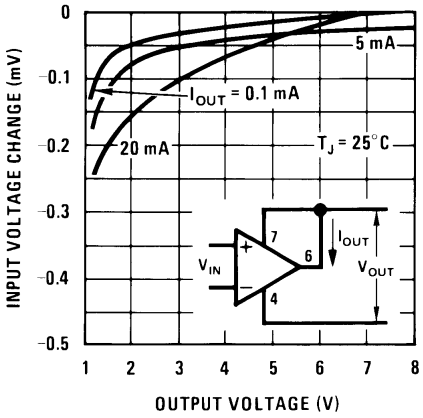

Figure 25. Shunt Gain

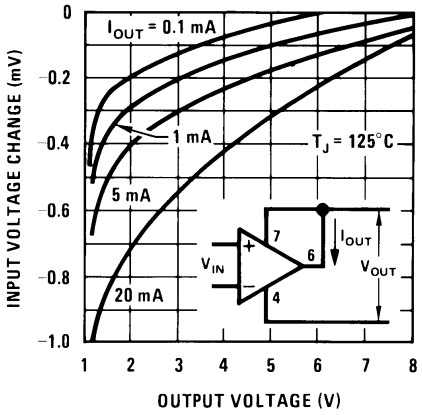

Figure 26. Shunt Gain

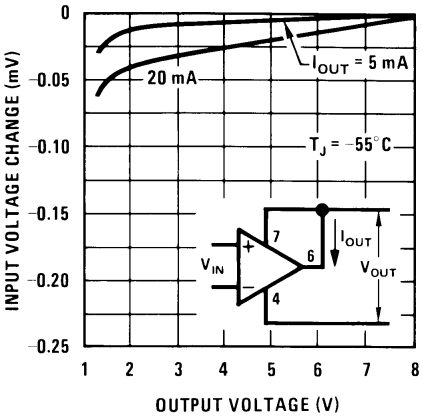

Figure 27. Shunt Gain

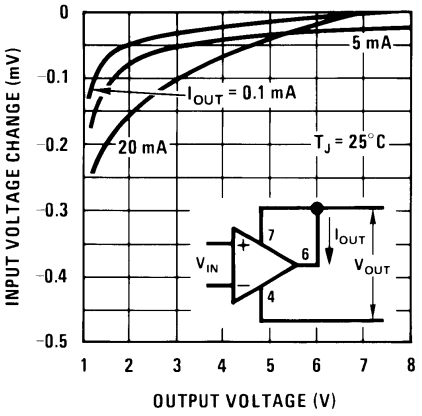

Figure 28. Shunt Gain

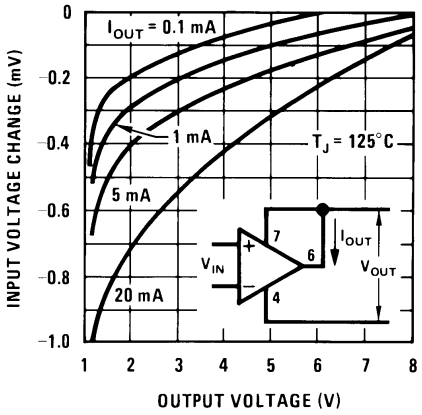

Figure 29. Shunt Gain

6.8.2 Typical Characteristics (Reference)

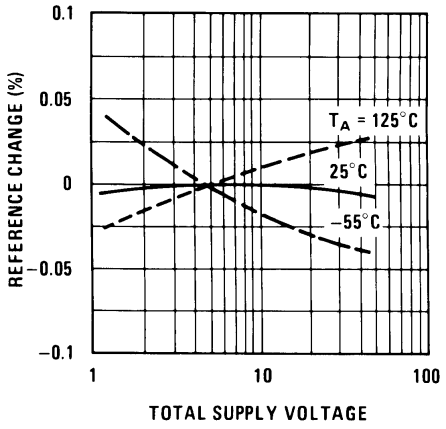

Figure 30. Line Regulation

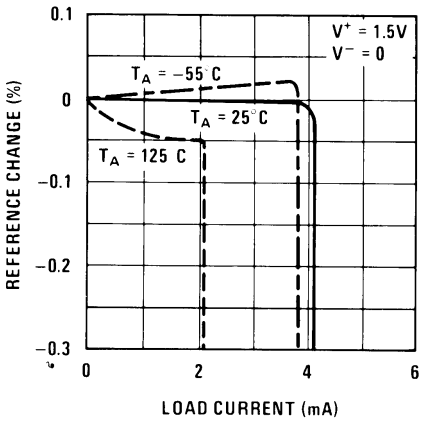

Figure 31. Load Regulation

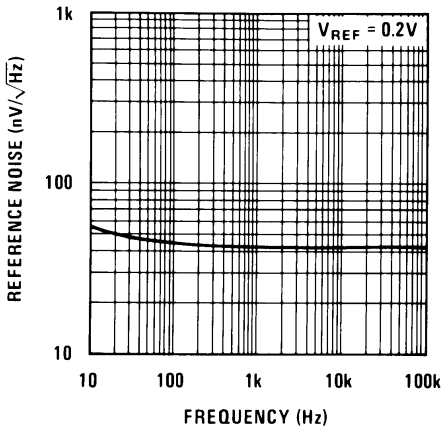

Figure 32. Reference Noise Voltage

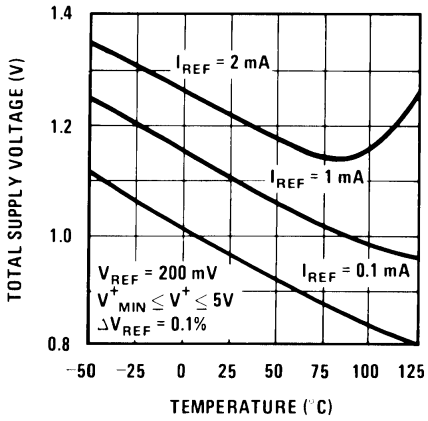

Figure 33. Minimum Supply Voltage

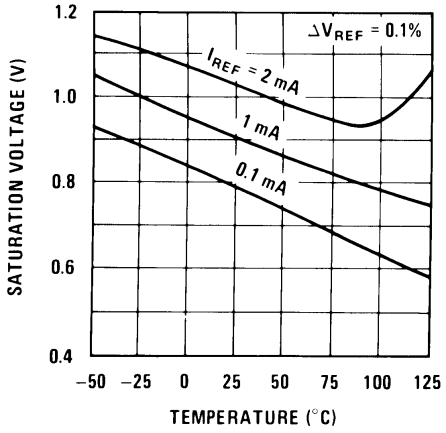

Figure 34. Output Saturation

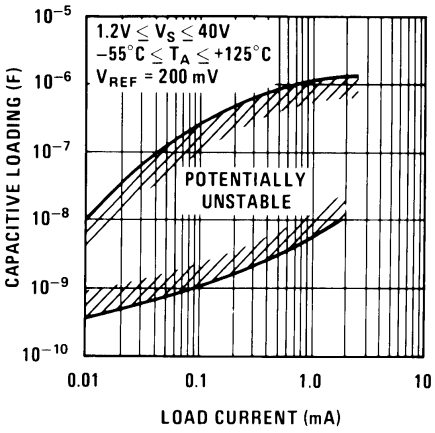

Figure 35. Typical Stability Range

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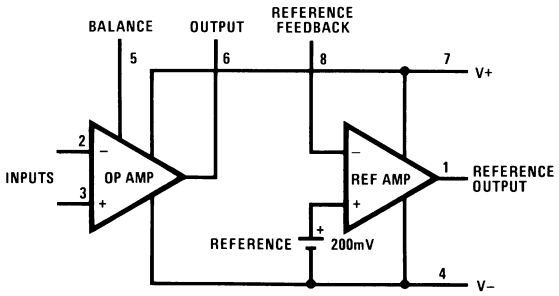
7 Detailed Description

7.1 Overview

The LM10 is a dual-operational amplifier combined with a voltage reference capable of a single-supply operation down to 1.1 V. It provides high overall performance, making it ideal for many general-purpose applications. The circuit can also operate in a floating mode, powered by residual voltage, independent of fixed supplies and it is well-protected from temperature drift.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The LM10 is specified for operation from 1.2 V to 40 V. Many of the specifications apply from –55ºC to 125ºC. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in electrical characteristics tables under *Specifications* and in the *Typical Characteristics* section.

7.3.2 Common-Mode Voltage Range

The input common-mode voltage range of the LM10 extends from the negative rail to 0.85 V less than the positive rail.

7.3.3 Operational Amplifier

The minimum operating voltage is reduced to nearly one volt and the current gain is less affected by temperature, resulting in a fairly flat bias current over temperature.

7.3.4 Voltage Reference

Second-order nonlinearities are compensated for which eliminates the bowed characteristics of conventional designs, resulting in better temperature stability.

7.4 Device Functional Modes

7.4.1 Floating Mode

To use the device in a floating mode, the operational amplifier output is shorted to V+ which disables the PNP portion of the output stage. Thus, with a positive input signal, neither halves of the output conducts and the current between the supply terminals is equal to the quiescent supply current. With negative input signals, the NPN portion of the output begins to turn on, reaching the short circuit current for a few hundred microvolts overdrive.

7.4.2 Linear Operation

This device can also operate linearly while in the floating mode. An example of this is shown in the *Typical Application* section.

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8 Application and Implementation

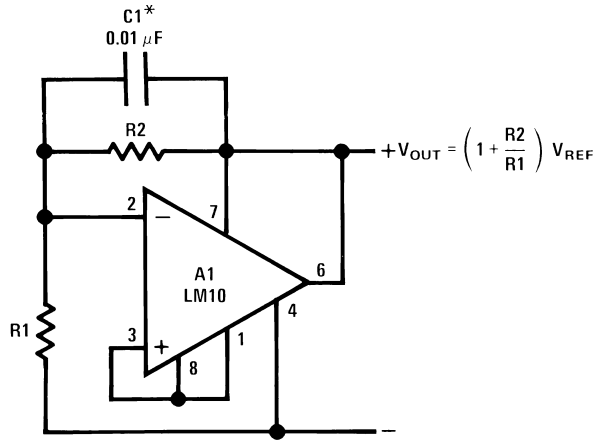
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

With heavy amplifier loading to V^-, resistance drops in the V^- lead can adversely affect reference regulation. Lead resistance can approach 1 Ω. Therefore, the common to the reference circuitry should be connected as close as possible to the package.

8.2 Typical Application



* required for capacitive loading

Figure 36. Shunt Voltage Regulator

8.2.1 Design Requirements

Table 1 lists the design parameters for this example.

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Ambient Temperature Range	–55ºC to 125ºC
Supply Voltage Range	1.2 V to 40 V
Common-Mode Input Range	(V–) to (V+) – 0.85 V

8.2.2 Detailed Design Procedure

Given that the transfer function of this circuit is:

$$V_{OUT} = (1 + \frac{R_2}{R_1}) V_{REF} \quad (1)$$

the output can be set between 0.2 V and the breakdown voltage of the IC by selecting an appropriate value for R2. The circuit regulates for input voltages within a saturation drop of the output (typically 0.4 V at 20 mA and 0.15 V at 5 mA). The regulator is protected from shorts or overloads by current limiting and thermal shutdown.

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Typical regulation is about 0.05% load and 0.003%/V line. A substantial improvement in regulation can be effected by connecting the operational amplifier as a follower and setting the reference to the desired output voltage. This has the disadvantage that the minimum input-output differential is increased to a little more than a diode drop. If the operational amplifier were connected for a gain of 2, the output could again saturate. But this requires an additional pair of precision resistors.

The regulator in Figure 36 could be made adjustable to zero by connecting the operational amplifier to a potentiometer on the reference output. This has the disadvantage that the regulation at the lower voltage settings is not as good as it might otherwise be.

8.2.3 Application Curve

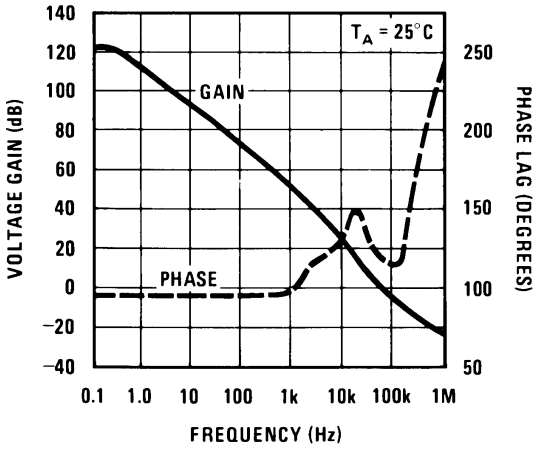


Figure 37. Frequency Response

8.3 System Examples

Circuit descriptions available in application note AN-211 (SNOA638).

8.3.1 Operational Amplifier Offset Adjustment

(Pin numbers are for 8-pin packages)

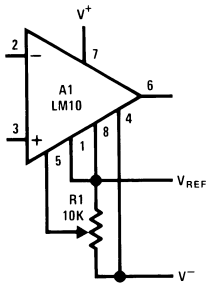


Figure 38. Standard

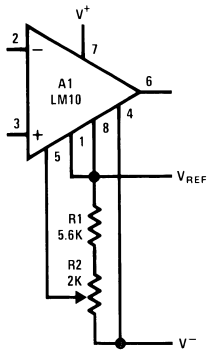


Figure 39. Limited Range

System Examples (continued)

(Pin numbers are for 8-pin packages)

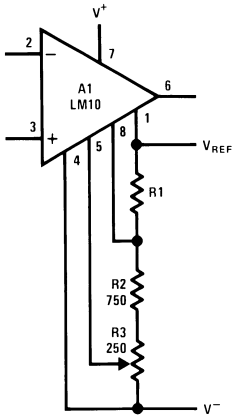


Figure 40. Limited Range With Boosted Reference

8.3.2 Positive Regulators

(Pin numbers are for 8-pin packages)

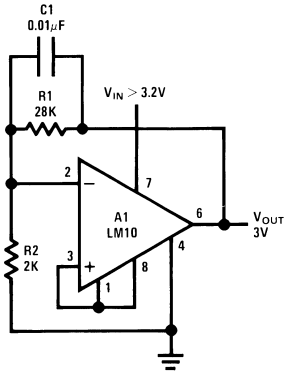


Figure 41. Low Voltage

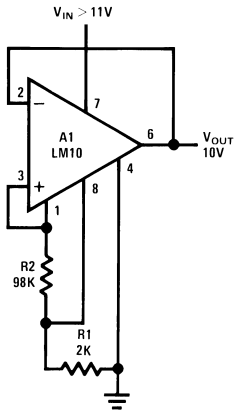
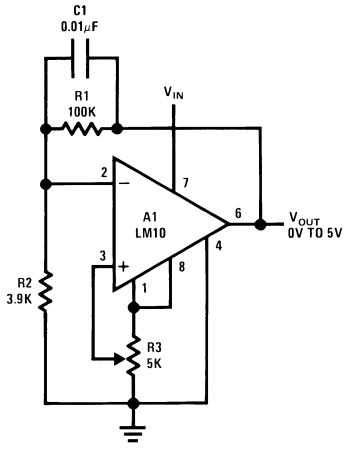


Figure 42. Best Regulation



Use only electrolytic output capacitors.

Figure 43. Zero Output

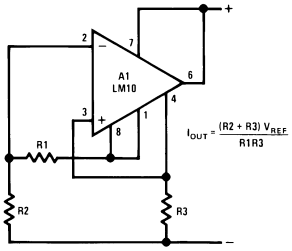


Figure 44. Current Regulator

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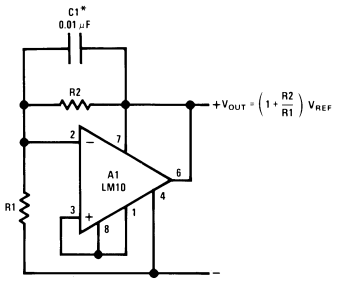
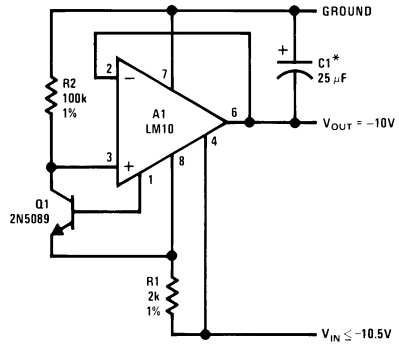
System Examples (continued)

(Pin numbers are for 8-pin packages)



Required For Capacitive Loading

Figure 45. Shunt Regulator



*Electrolytic

Figure 46. Negative Regulator

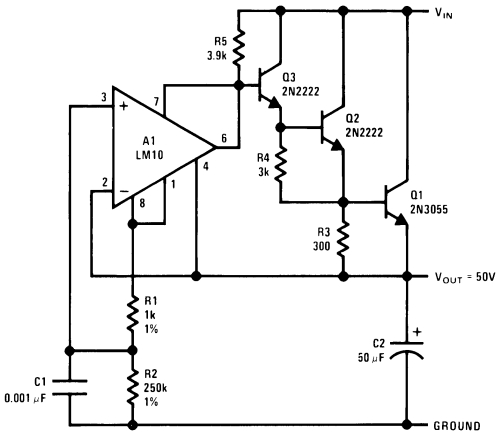
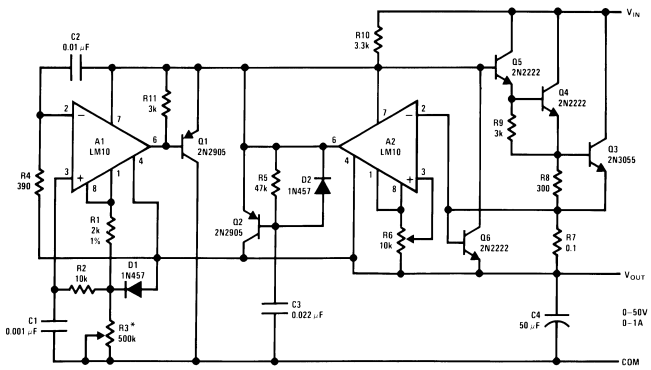
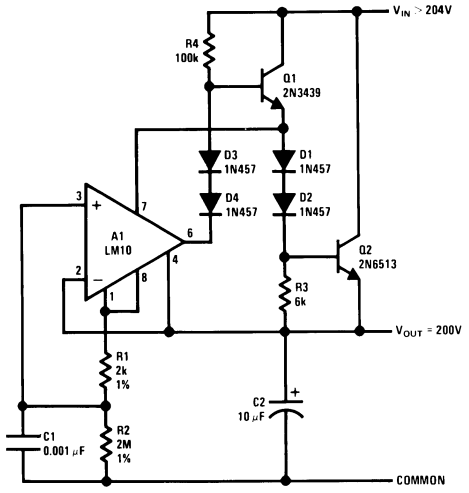


Figure 47. Precision Regulator



*V_{OUT}=10^{-4} R3

Figure 48. Laboratory Power Supply



$$V_{OUT} = \frac{R2}{R1} V_{REF}$$

Figure 49. HV Regulator

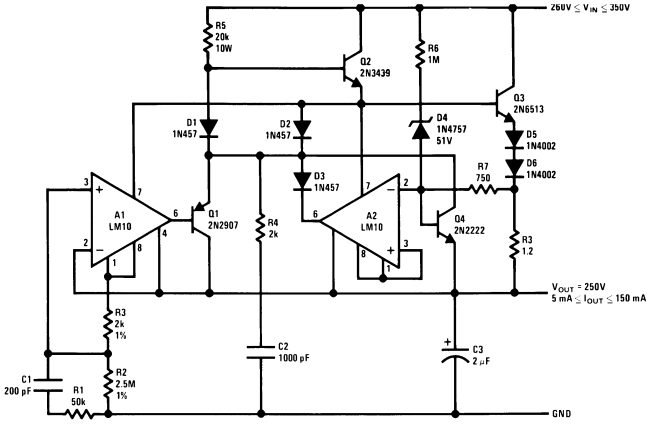
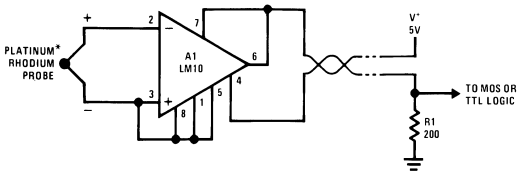


Figure 50. Protected HV Regulator

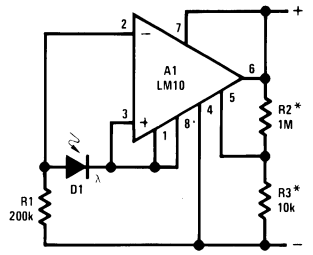
System Examples (continued)

(Pin numbers are for 8-pin packages)



*800°C Threshold Is Established By Connecting Balance To V_{REF}.

Figure 51. Flame Detector



*Provides Hysteresis

Figure 52. Light Level Sensor

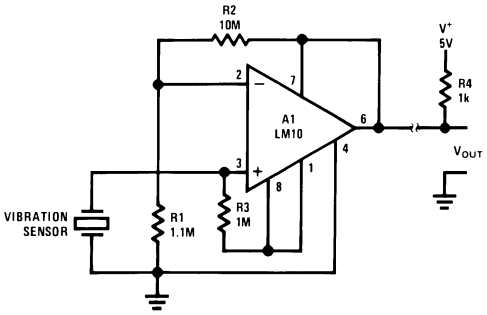


Figure 53. Remote Amplifier

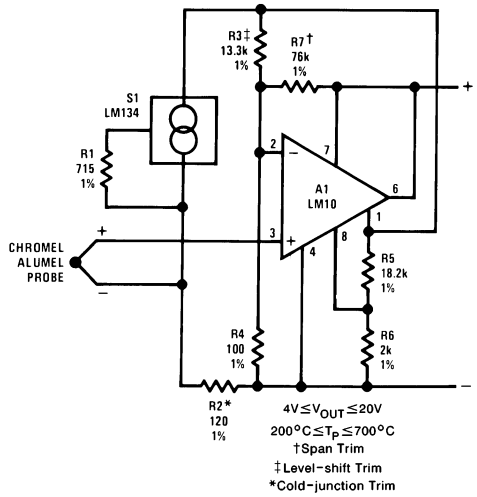


Figure 54. Remote Thermocouple Amplifier

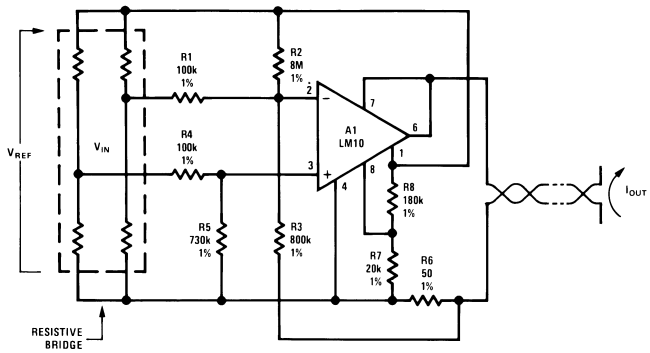
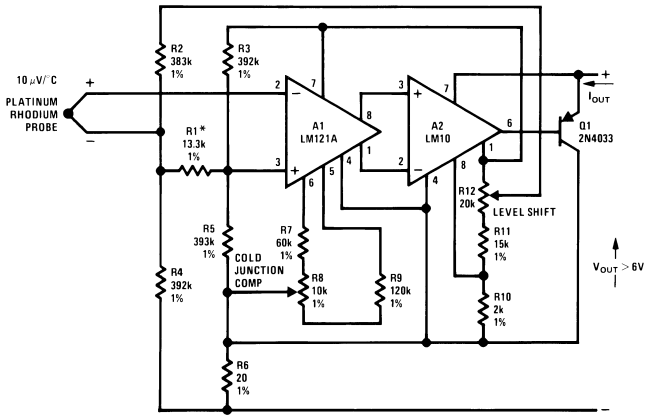


Figure 55. Transmitter for Bridge Sensor



10 mA≤I_{OUT}≤50 mA
500°C≤T_P≤1500°C
*Gain Trim

Figure 56. Precision Thermocouple Transmitter

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System Examples (continued)

(Pin numbers are for 8-pin packages)

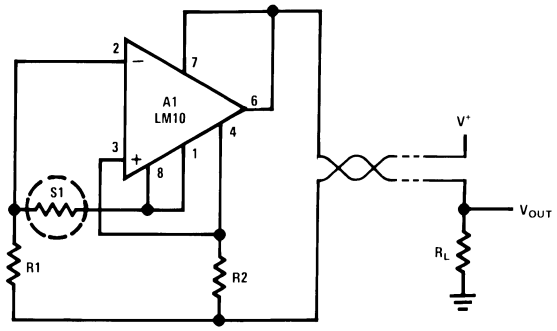
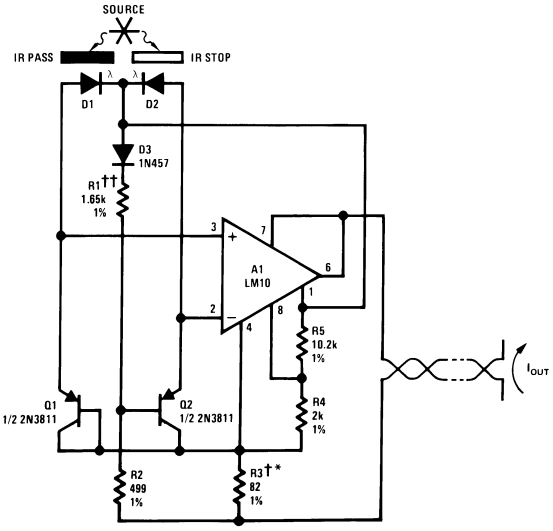


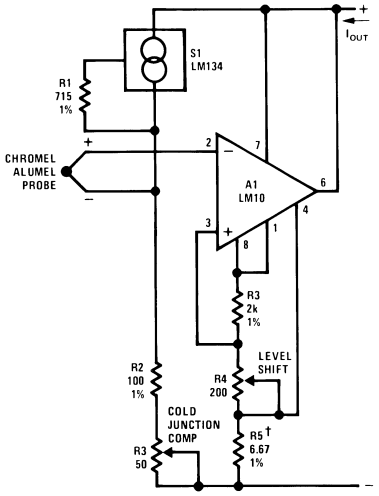
Figure 57. Resistance Thermometer Transmitter



††Level-shift Trim
*Scale Factor Trim
†Copper Wire Wound
1 mA≤I_{OUT}≤5 mA

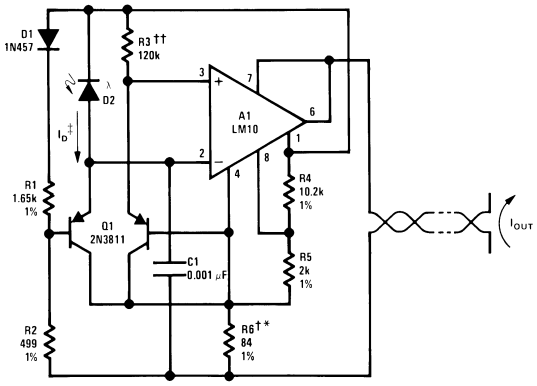
$$0.01 \leq \frac{I_{D2}}{I_{D1}} \leq 100$$

Figure 58. Optical Pyrometer



200°C≤T_p≤700°C
1 mA≤I_{OUT}≤5 mA
†Gain Trim

Figure 59. Thermocouple Transmitter



1 mA≤I_{OUT}≤5 mA
‡50 μA≤I_D≤500 μA
††Center Scale Trim
†Scale Factor Trim
*Copper Wire Wound

Figure 60. Logarithmic Light Sensor

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System Examples (continued)

(Pin numbers are for 8-pin packages)

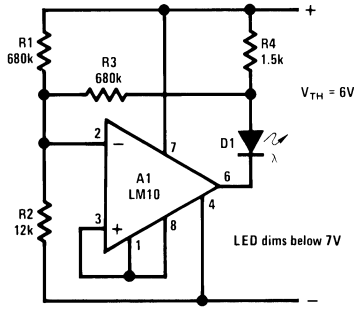


Figure 61. Battery-level Indicator

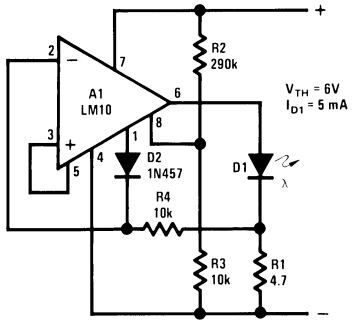
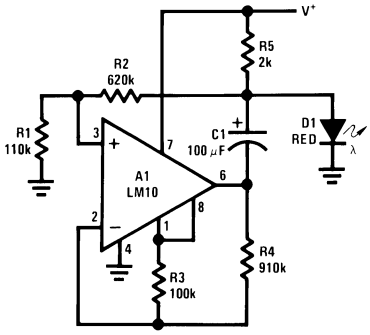
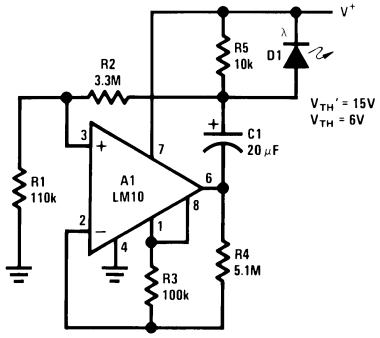


Figure 62. Battery-threshold Indicator



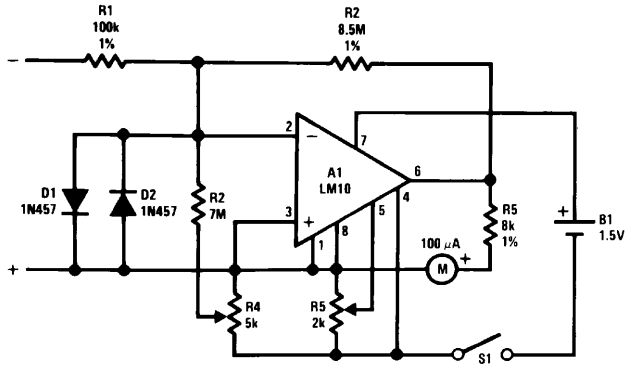
Flashes Above 1.2V
Rate Increases With
Voltage

Figure 63. Single-cell Voltage Monitor



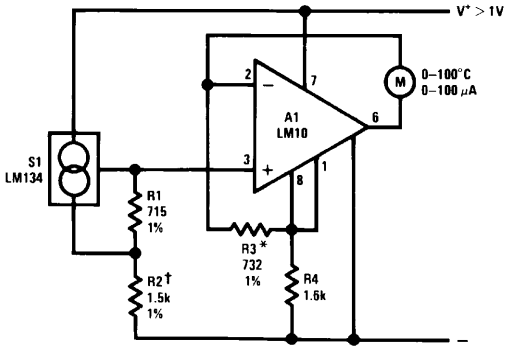
Flash Rate Increases
Above 6V and Below 15V

Figure 64. Double-ended Voltage Monitor



INPUT
10 mV, 100nA
FULL-SCALE

Figure 65. Meter Amplifier



*Trim For Span
†Trim For Zero

Figure 66. Thermometer

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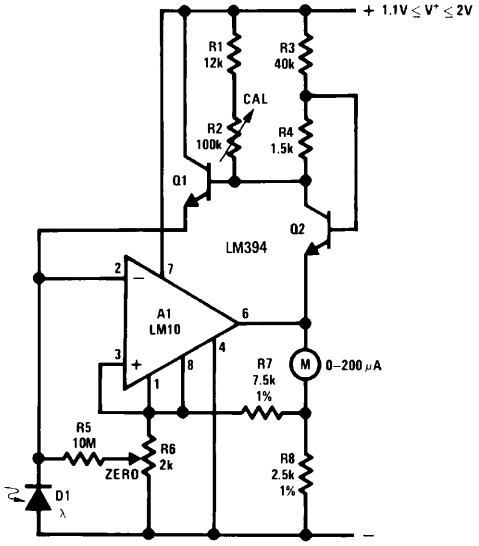
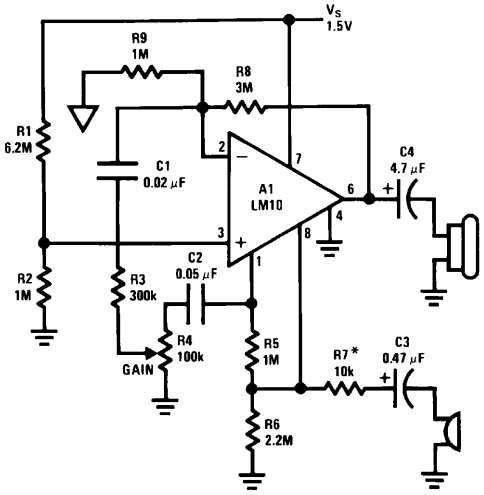
System Examples (continued)

(Pin numbers are for 8-pin packages)



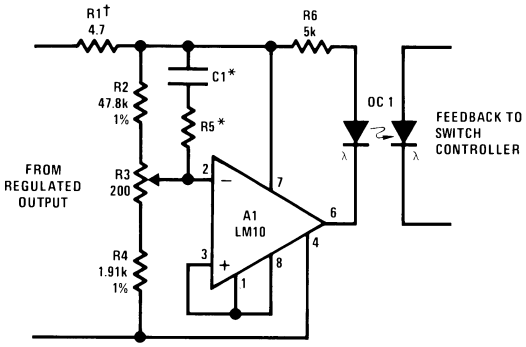
$1 \leq \lambda/\lambda_0 \leq 10^5$

Figure 67. Light Meter



Z_{OUT}~680Ω @ 5 kHz
$A_V \leq 1k$
f_1~100 Hz
f_2~5 kHz
R_L~500
*Max Gain Trim

Figure 68. Microphone Amplifier



†Controls "Loop Gain"
*Optional Frequency Shaping

Figure 69. Isolated Voltage Sensor

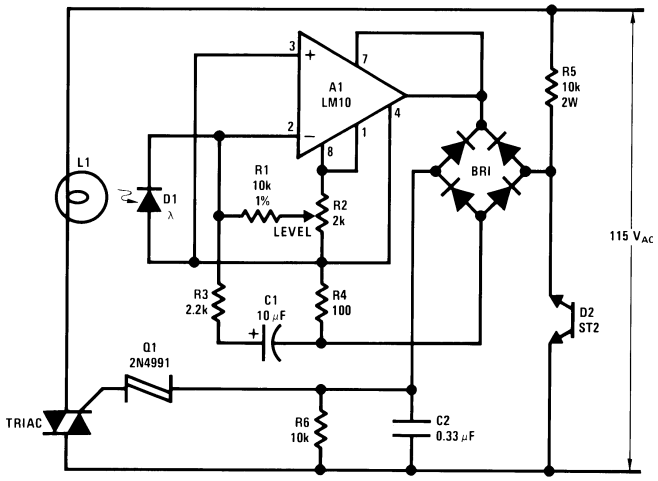


Figure 70. Light-Level Controller

System Examples (continued)

(Pin numbers are for 8-pin packages)

8.3.3 Reference and Internal Regulator

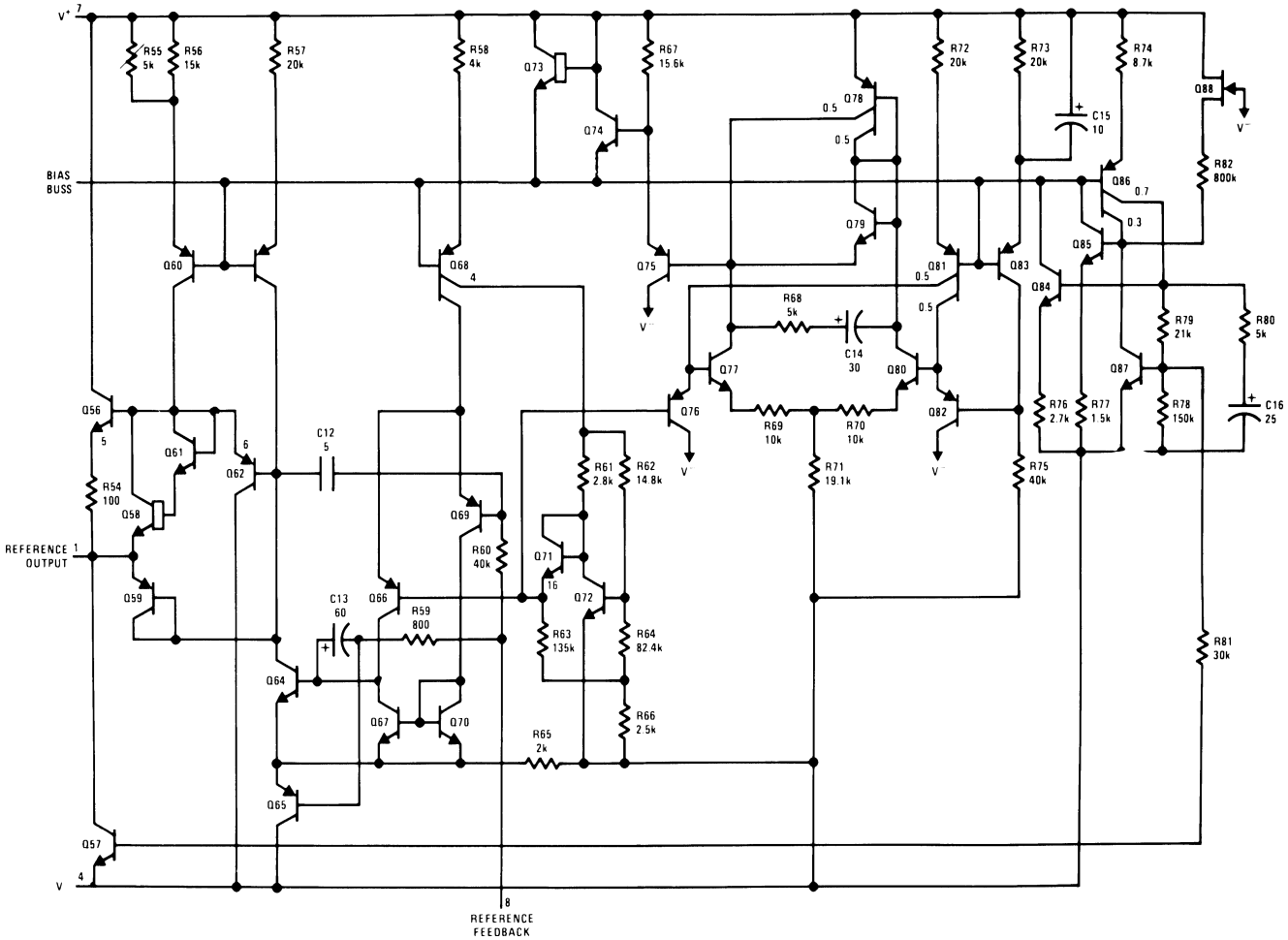


Figure 71. Reference and Internal Regulator

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9 Power Supply Recommendations

The LM10 is specified for operation from 1.2 V to 40 V unless otherwise stated. Many specifications apply from –55ºC to 125ºC. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Specifications* section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, good printed-circuit board (PCB) layout practices are recommended. Low-loss, 0.1-uF bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

10.2 Layout Example

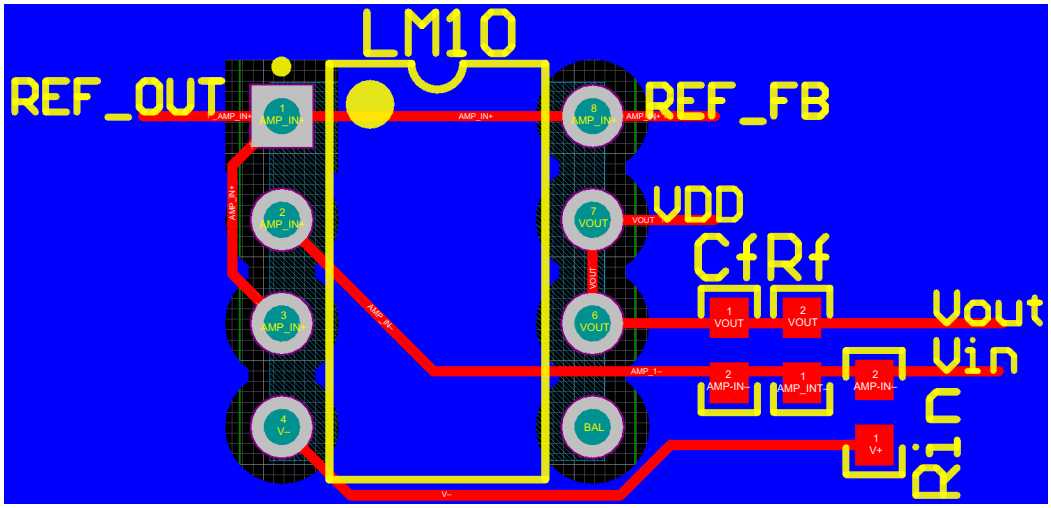

Figure 72. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

11.1.1.1 Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the unloaded output is in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Shunt gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it with the output tied to the V^+ terminal of the IC. The load and power source are connected between the V^+ and V^- terminals, and input common-mode is referred to the V^- terminal.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Line regulation: The average change in reference output voltage over the specified supply voltage range.

Load regulation: The change in reference output voltage from no load to that load specified.

Feedback sense voltage: The voltage, referred to V^-, on the reference feedback terminal while operating in regulation.

Reference amplifier gain: The ratio of the specified reference output change to the change in feedback sense voltage required to produce it.

Feedback current: The absolute value of the current at the feedback terminal when operating in regulation.

Supply current: The current required from the power source to operate the amplifier and reference with their outputs unloaded and operating in the linear range.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

AN-211 New Op Amp Ideas, SNOA638

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM10BH	ACTIVE	TO-CAN	LMG	8	500	TBD	Call TI	Call TI	-40 to 85	(LM10BH, LM10BH)	Samples
LM10BH/NOPB	ACTIVE	TO-CAN	LMG	8	500	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	-40 to 85	(LM10BH, LM10BH)	Samples
LM10CH	ACTIVE	TO-CAN	LMG	8	500	TBD	Call TI	Call TI	0 to 70	(LM10CH, LM10CH)	Samples
LM10CH/NOPB	ACTIVE	TO-CAN	LMG	8	500	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	0 to 70	(LM10CH, LM10CH)	Samples
LM10CLN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM10CLN	Samples
LM10CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM 10CN	Samples
LM10CWM	NRND	SOIC	NPA	14	50	TBD	Call TI	Call TI	0 to 70	LM10CWM	
LM10CWM/NOPB	ACTIVE	SOIC	NPA	14	50	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	LM10CWM	Samples
LM10CWMX/NOPB	ACTIVE	SOIC	NPA	14	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	LM10CWM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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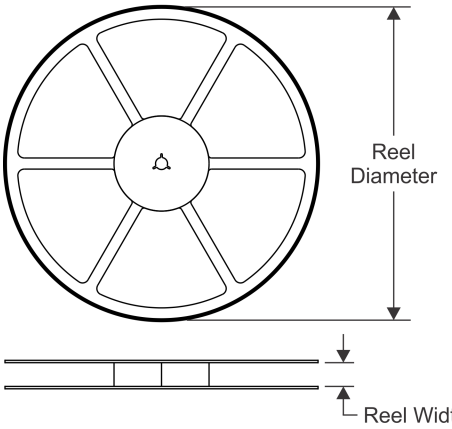
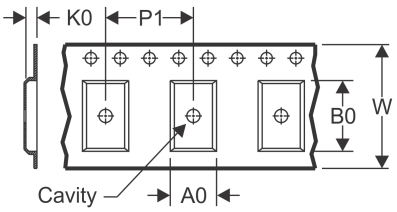
TAPE AND REEL INFORMATION

REEL DIMENSIONS

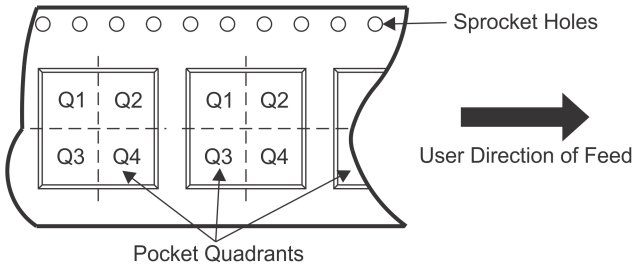


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

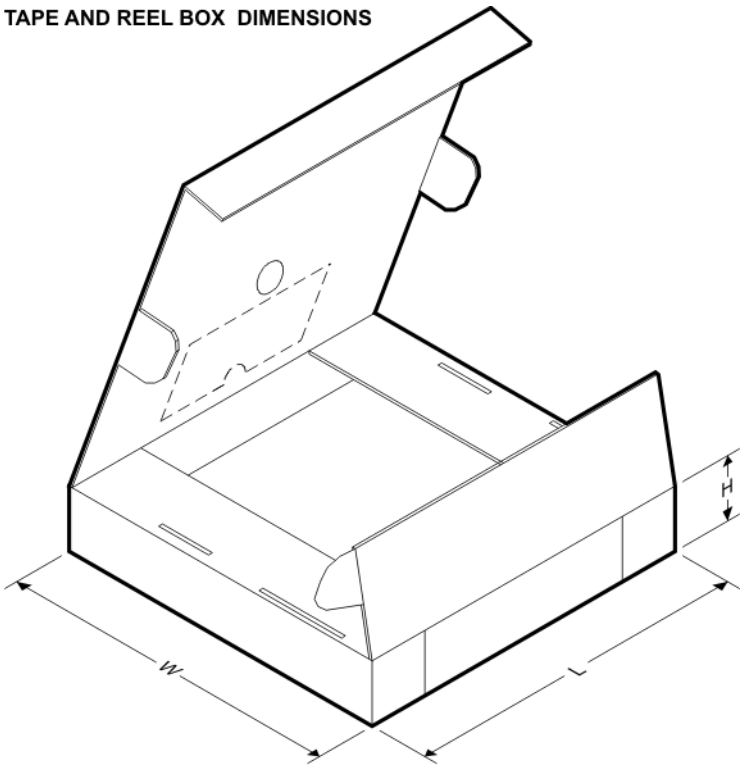
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM10CWMX/NOPB	SOIC	NPA	14	1000	330.0	16.4	10.9	9.5	3.2	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

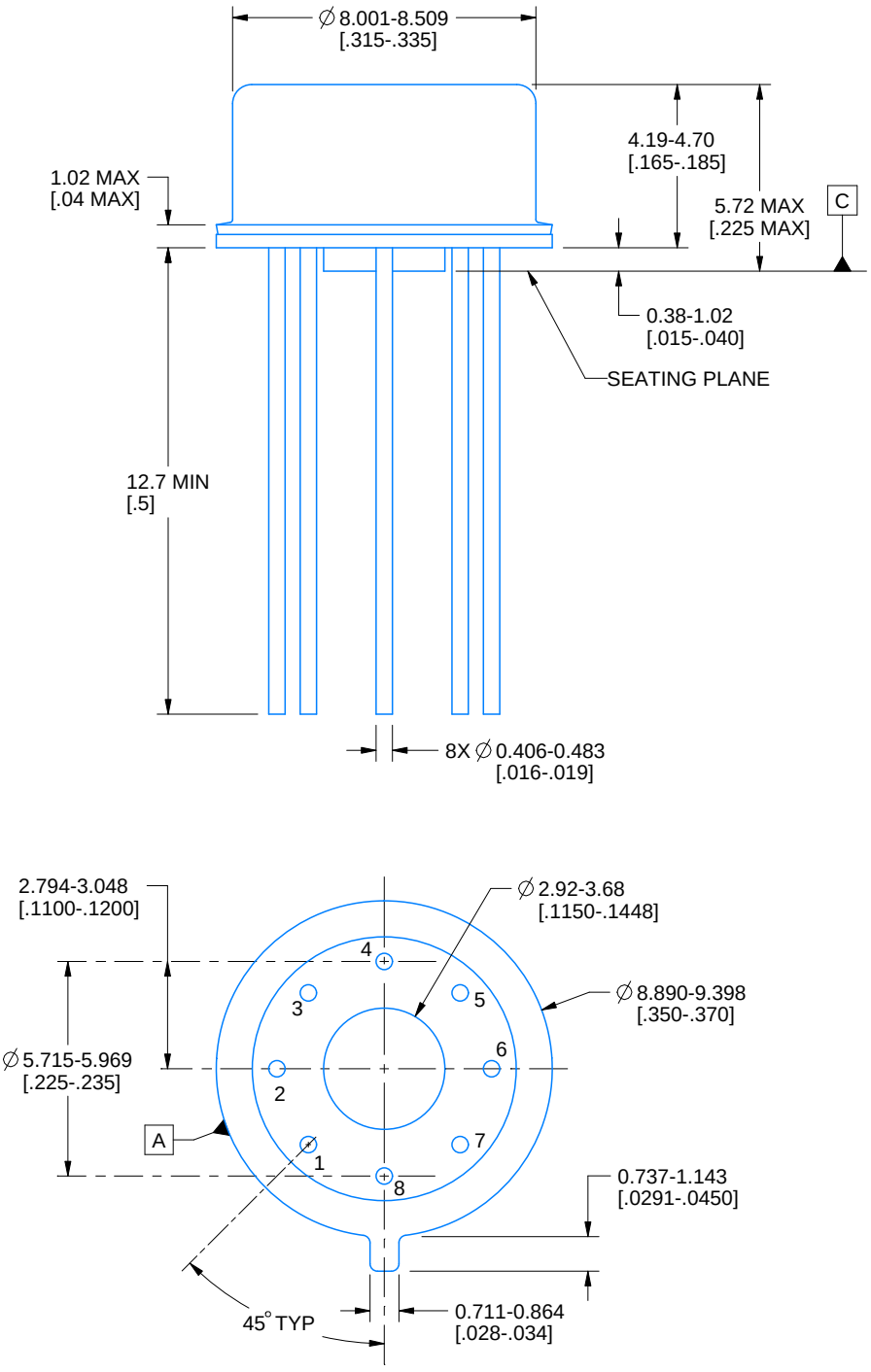
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM10CWMX/NOPB	SOIC	NPA	14	1000	367.0	367.0	38.0

PACKAGE OUTLINE

LMG0008A

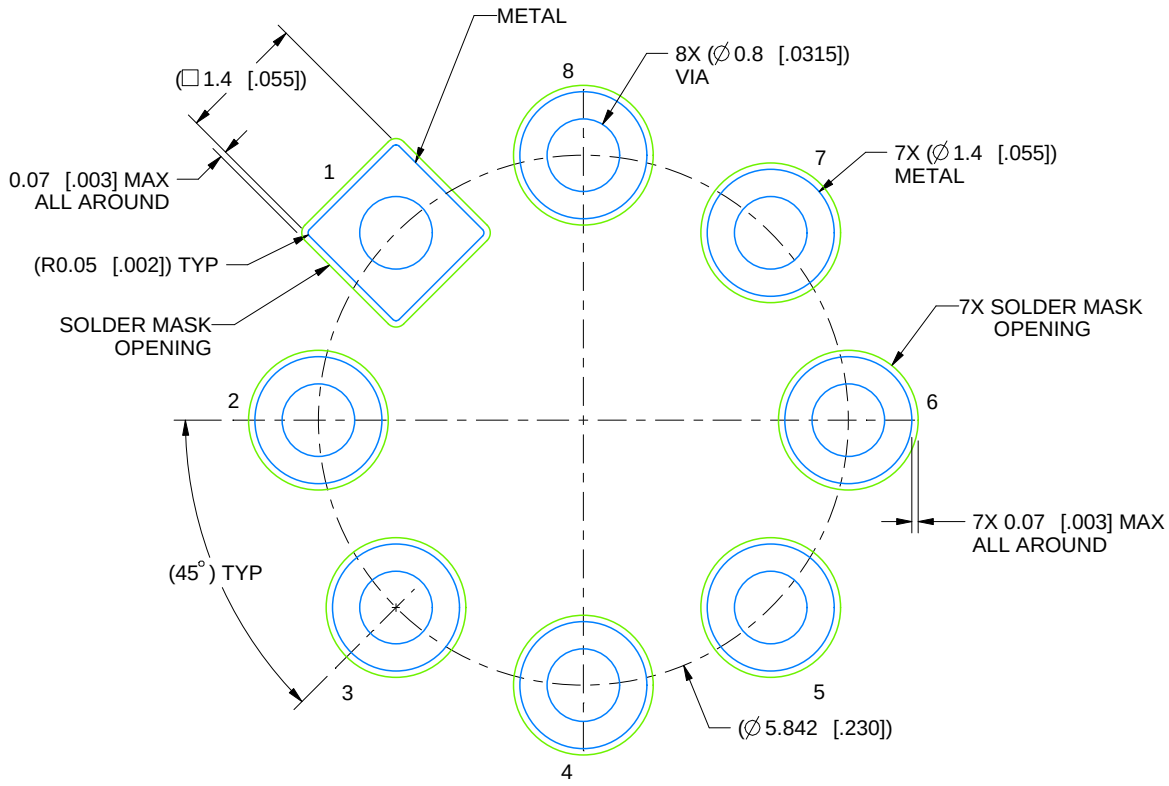
TO-CAN - 5.72 mm max height

METAL CYLINDRICAL PACKAGE



NOTES:

1. All linear dimensions are in millimeters [inches]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



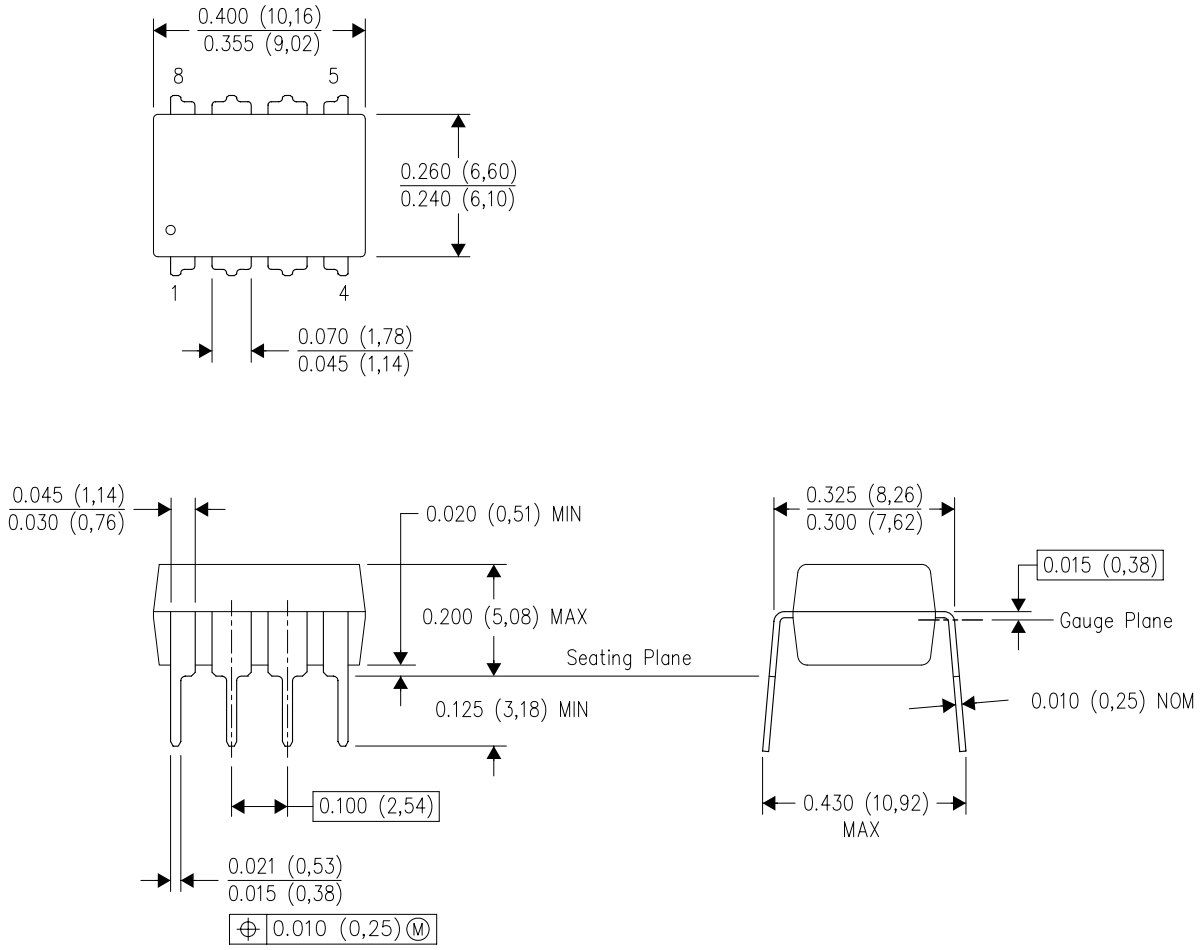
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4224369/B 08/2018

REVISIONS

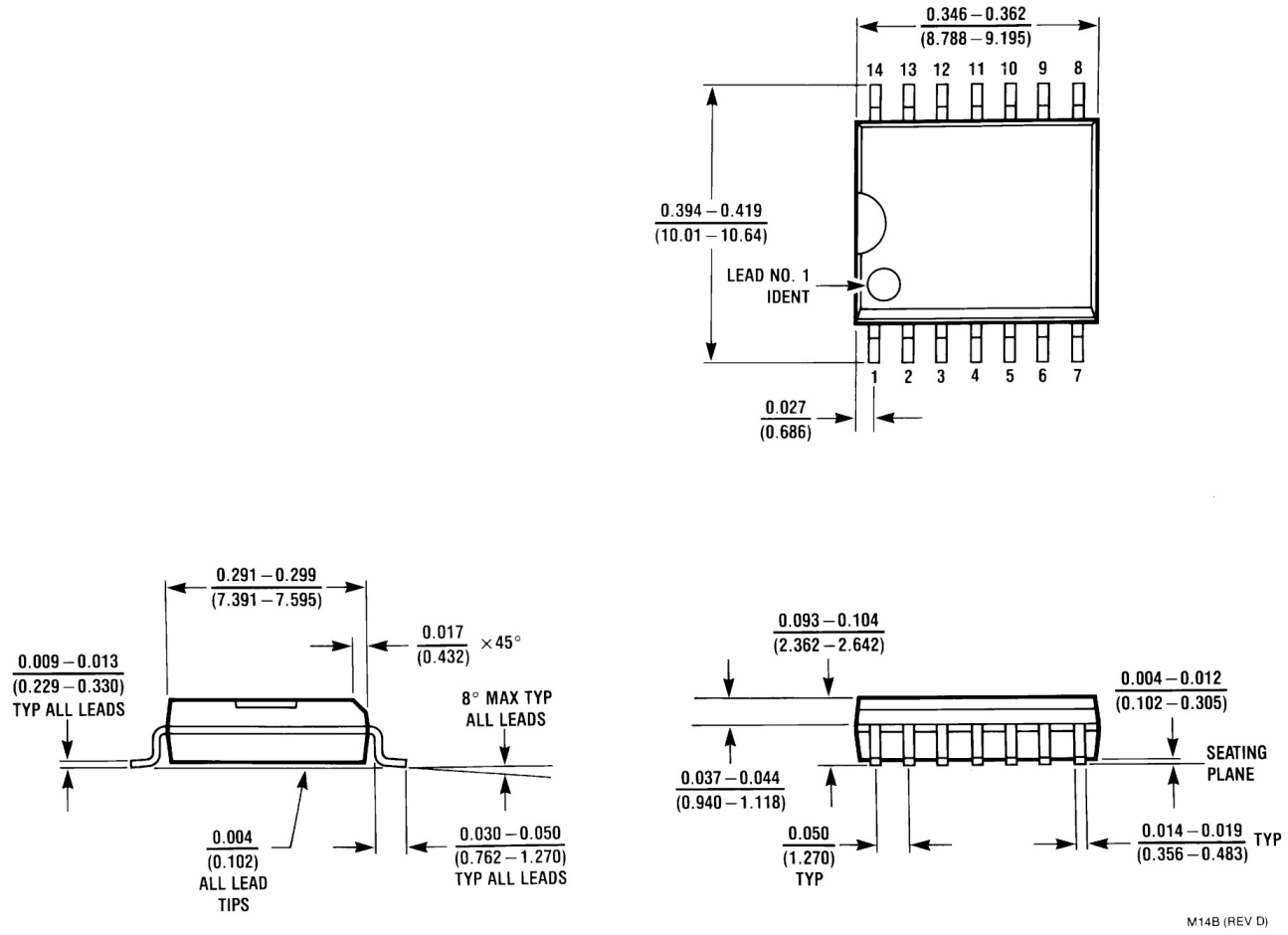
REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2174627	07/10/2018	V. DASIKA / K. SINCERBOX
B	CHANGE TO DUAL DIMENSIONING MM [INCH] FORMAT	2175848	08/17/2018	V. DASIKA / K. SINCERBOX

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

NPA0014B


0.346 – 0.362
(8.788 – 9.195)
14 13 12 11 10 9 8
0.394 – 0.419
(10.01 – 10.64)
LEAD NO. 1
IDENT
1 2 3 4 5 6 7
0.027
(0.686)
0.291 – 0.299
(7.391 – 7.595)
0.017
(0.432)
×45°
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
8° MAX TYP
ALL LEADS
0.004
(0.102)
ALL LEAD
TIPS
0.030 – 0.050
(0.762 – 1.270)
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
SEATING
PLANE
0.037 – 0.044
(0.940 – 1.118)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.483)
TYP
M14B (REV D)

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