THE DATASHEET OF

LM10500SQ-0.8/NOPB

LM10500 5A Step-Down Energy Management Unit (EMU) With PowerWise™ Adaptive Voltage Scaling (AVS)

Check for Samples: LM10500

FEATURES

- **Closed-Loop Adaptive Voltage Scaling (AVS)**
- **PWI 1.0 / PWI 2.0 Compatible**
- **Resistor-Programmable switching frequency**
- **Frequency Synchronization**
- **Precision Enable**
- **Internal Soft-Start to Reduce In-Rush Current**
- **Power Good (PWROK)**
- **Under-Voltage Lock Out (UVLO)**
- **Over-Voltage Protection (OVP)**
- **Cycle-by-cycle current limiting (OCP)**
- **Thermal Shutdown**

KEY SPECIFICATIONS

- **3.0 V to 18.0 V Input Voltage Range**
- **1.5% Feedback Voltage Accuracy**
- **0.6 Vto 1.0 V AVS Feedback Voltage Range**
- **0.8 Vto 5.0 V Startup V_{OUT} Range (Using Resistor-Divider)**
- **AVS Typical Power Saving 40% Over Fixed Voltage**
- **300 kHz to 1.5 MHz Switching Frequency Range**
- **WQFN-28 Package (5 mm x 5 mm x 0.8 mm, 0.5 mm pitch)**

APPLICATIONS

- **Point-of-Load Regulation**
- **Servers and Networking Cards**
- **Storage Devices**
- **Set-Top-Box Processors**
- **Medical and Industrial Processors**

DESCRIPTION

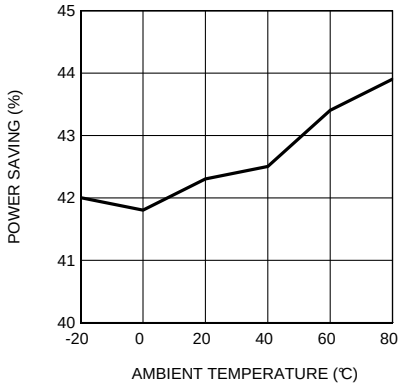
The LM10500 is a 5A Energy Management Unit (EMU) that actively reduces system-level power consumption by utilizing a continuous, real-time, closed-loop Adaptive Voltage Scaling (AVS) scheme. The LM10500 operates cooperatively with PowerWise™ AVS compatible ASICs, SoCs, and processors to optimize supply voltages adaptively over process and temperature variations. The device is controlled via PowerWise Interface (PWI) 1.0 or PWI 2.0 high-speed serial interface.

A typical power saving of 40% can be achieved when LM10500 is used with AVS compatible ASICs, SoCs, and processors.

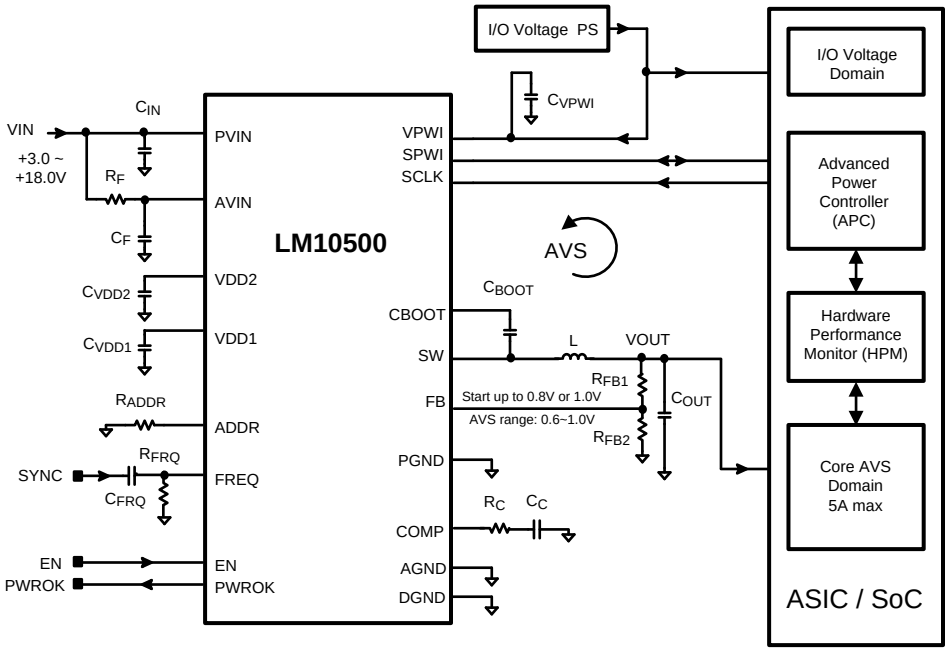
Adaptive Voltage Scaling Technology

PowerWise Adaptive Voltage Scaling (AVS) technology is an advanced closed-loop technology for reducing active and standby energy consumption of digital processing engines and ASICs. Hardware Performance Monitor (HPM) is designed into the digital engine together with an Advanced Power Controller (APC) to monitor the performance of the silicon based on process and temperature variation. Information is fed back to an Energy Management Unit (EMU) which then sets the voltage precisely according to the processor's needs. The AVS technology enables optimum power delivery to the processors, ASICs, and SoCs, which maximizes overall system energy savings. AVS technology is process and architecture independent.

Figure 1. Typical Power Saving Using AVS And The LM10500 Compared To Fixed Voltage Scheme



Typical Application Circuit



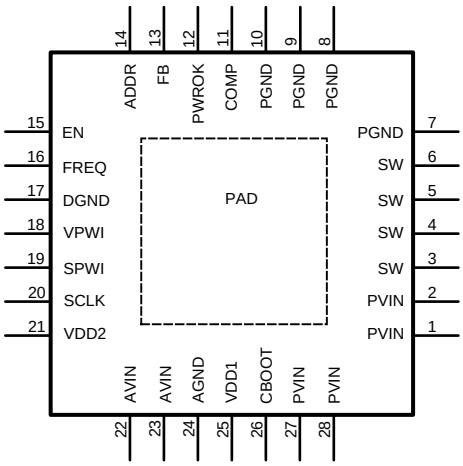


Figure 2. WQFN-28 Package, Exposed Pad
See package Number RSG0028B

PIN DESCRIPTIONS

Pin #	Name	Type (1)	Function
1,2,27,28	PVIN	P	Input voltage to the power switches integrated in the device.
3,4,5,6	SW	P	Switch node output of the power switches. It should be connected to the external inductor.
7,8,9,10	PGND	G	Power ground for the internal power switches.
11	COMP	A	Compensation pin to connect to external compensation network.
12	PWROK	OD	Power Good or PWI Power OK, open drain output. If high, indicates the output voltage is regulated within tolerance. A pull-up resistor (10 kΩ to 100 kΩ) is recommended for most applications.
13	FB	A	Voltage Feedback pin. This pin can be connected to the output voltage directly or through a resistor divider to set the output voltage range. Range of FB pin voltage is PWI 1.0 or PWI 2.0 programmable between 0.6V and 1.0V.
14	ADDR	A	PWI Address Selection pin. An external resistor should be connected from this pin to ground to set the PWI 1.0 or PWI 2.0 address. The voltage on this pin is only read once by the internal register when the device is powered up.
15	EN	I	Precision enable pin. An external divider can be used to set the device turn-on threshold. If not used, the EN pin should be connected to AVIN.
16	FREQ/SYNC	A	Frequency setting or external clock synchronization pin. This pin can be connected to a resistor to ground to set the internal oscillator frequency. It also can be connected to an external clock source via a capacitor, so that the switching action of the device is synchronized to the external clock.
17	DGND	G	Digital ground for VPWI and digital interface: SPWI and SCLK.
18	VPWI	P	PowerWise Interface (PWI) supply input, 1.8 V-10% to 3.3V+10%. A bypass capacitor of 1µF is recommended on this pin.
19	SPWI	I/O	PowerWise Interface (PWI) bi-directional data pin. This pin is internally pulled down to ground.
20	SCLK	I	PowerWise Interface (PWI) clock input. This pin is internally pulled down to ground.
21	VDD2	P	2.5V output of internal regulator. This pin is only for bypassing the internal LDO. Loading this pin is not recommended.
22,23	AVIN	P	Analog power input. It powers the internal 2.5V and 5.0V LDOs, which provide bias current and internal driver power. It can be connected to PVIN through a low pass RC filter, or can be supplied by a separate rail.
24	AGND	G	Analog ground for the internal bias circuitry.
25	VDD1	P	5.0V output of internal regulator. This pin is only for bypassing the internal LDO. Loading this pin is not recommended.
26	CBOOT	A	Bootstrap pin to drive the high side switch. A bootstrap capacitor should be connected between this pin to the SW pin.
PAD	PAD		Exposed pad at the back of the device. The PAD should be connected to ground, but cannot be used as primary ground connection. Use multiple vias under the PAD for optimal thermal performance.

(1) P: Power, A: Analog, I: Digital Input, I/O: Digital Input/Output, G: Ground, OD: Open Drain

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

PVIN, AVIN, SW, EN, PWROK to AGND	-0.3 V to +20 V
CBOOT to AGND	-0.3 V to +25 V
CBOOT to SW	-0.3 V to +5.5 V
VDD1, VPWI, FB, COMP, ADDR, FREQ, SCLK, SPWI to AGND	-0.3 V to +6 V
VDD2 to AGND	-0.3 V to +3 V
AGND to PGND	-0.3 V to +0.3 V
Junction Temperature (T_{J-MAX})	150 °C
Storage Temperature Range	-65 °C to 150 °C
Maximum Continuous Power Dissipation P_{D-MAX} (3)	Internally limited
Maximum Lead Temperature Leadfree compatible (4)	+260 °C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications
(3) The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula $P = (T_J – T_A)/\theta_{JA}$, where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high power dissipation exists, special care must be paid to thermal dissipation issues in PC board design. Internal thermal shutdown circuitry protects the device from permanent damage.
(4) For detailed soldering specifications, please refer to *Application Note 1187: Leadless Leadframe Package (LLP) (AN-1187)* SNOA401.

ESD Ratings (1)

All Pins, Human Body Model (HBM)	±2 kV

(1) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7)

Operating Ratings

PVIN to PGND, AGND	3 V to 18 V
AVIN to PGND, AGND	3 V to 18 V

Thermal Properties

Junction Temperature	−40 °C to +125 °C
Ambient Temperature (1)	−40 °C to +85 °C
Junction-to-Ambient Thermal Resistance (θ_{JA}) (2)	32.4 °C/W

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$) and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (\theta_{JA} \times P_{D\text{-}MAX})$.

(2) Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer standard JEDEC thermal test board or 4LJEDEC, 4" x 3" in size, with a 3 by 3 array of thermal vias. The board has two embedded copper layers which cover roughly the same size as the board. The copper thickness for the four layers, starting from the top one, is 2 oz./1oz./1oz./2 oz. For WQFN, thermal vias are placed between the die attach pad in the 1st. copper layer and 2nd. copper layer. Detailed description of the board can be found in JESD 51-7. Ambient temperature in the simulation is 22°C, still air. Power dissipation is 1W. The value of θ_{JA} of this product can vary significantly depending on PCB material, layout, and environmental conditions. In applications with high power dissipation (e.g. high V_{OUT}, high I_{OUT}), special care must be paid to thermal dissipation issues. For more information on these topics, please refer to *Application Note AN-1187: Leadless Leadframe Package (LLP)* SNOA401.

General Electrical Characteristics (1) (2)

Specifications with standard typeface are for T_J = 25 °C, and those in **boldface type** apply over the full Operating Temperature Range (T_J = −40 °C to 125 °C). Unless otherwise specified, $V_{PVIN} = V_{AVIN}$ = 12 V, V_{OUT} = 1.2 V.

Symbol	Parameter	Remarks	Min	Typ	Max	Unit
$V_{FB\text{-}default}$	Feedback Pin Factory Default Voltage. All Registers in Default States	LM10500SQ-0.8	**0.788**	0.8	**0.812**	V
		LM10500SQ-1.0	**0.985**	1.0	**1.015**	
$V_{FB\text{-}range\text{-}top}$	Maximum Feedback Voltage	Voltage Code = R0 – R9 = 7FH		1.0		
$V_{FB\text{-}range\text{-}bottom}$	Minimum Feedback Voltage	Voltage Code = R0 – R9 = 00H		0.6		
Resolution	Bit Length of The Feedback Voltage DAC	V_{FB} = 0.6 V to 1 V		7		bit
DNL	Differential Non-Linearity of V_{FB} DAC	V_{FB} = 0.6 V to 1 V			**0.5**	LSB
INL	Integrated Non-Linearity of V_{FB} DAC	V_{FB} = 0.6 V to 1 V			**1**	LSB
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	I_{OUT} = 0.1 A to 5 A		0.02		%/A
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 3.0 V to 18 V		0.01		%/V
$R_{DS\text{-}ON\text{-}HS}$	High Side Switch On-Time Resistance	$I_{DS\text{-}HS}$ = 5 A		44		mΩ
$R_{DS\text{-}ON\text{-}LS}$	Low Side Switch On-Time Resistance	$I_{DS\text{-}LS}$ = 5 A		22		
$I_{CL\text{-}HS}$	High Side Switch Current Limit	High-Side FET	**5.9**	7	**7.87**	A
$I_{CL\text{-}LS}$	Low Side Switch Current Limit	Low-Side FET (3)	**5.9**	8	**10.2**	
$I_{NEG\text{-}CL\text{-}LS}$	Low Side Switch Negative Current Limit	Low-Side FET	**-7**	-4.1	**-1.64**	
I_{SD}	Shutdown Quiescent Current, AVIN is Connected to PVIN, V_{EN} = 0	$V_{AVIN} = V_{PVIN}$ = 5 V		0.1	**2**	µA
		$V_{AVIN} = V_{PVIN}$ = 18 V		1	**4.1**	
I_q	Quiescent Current With Switcher On, No Load, DCM Operation	$V_{AVIN} = V_{PVIN}$ = 18 V		9	**9.7**	mA
I_{FB}	Feedback Pin Input Bias Current	V_{FB} = 1.0 V		1		nA

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.

(3) The low side switch current limit is ensured to be higher than the high side switch current limit.

General Electrical Characteristics (1) (2) (continued)

Specifications with standard typeface are for T_J = 25 °C, and those in **boldface type** apply over the full Operating Temperature Range (T_J = −40 °C to 125 °C). Unless otherwise specified, V_{PVIN} = V_{AVIN} = 12 V, V_{OUT} = 1.2 V.

Symbol	Parameter	Remarks	Min	Typ	Max	Unit
Gm	Error Amplifier Transconductance	V_{FB} = 1.0 V, V_{COMP} = 0.5 V		2400		µA/V
A_{VOL}	Error Amplifier Voltage Gain			65		dB
V_{IH-OVP}	OVP Tripping Threshold	Output voltage rising threshold, % of V_{OUT}	**103.5**	109.5	**115**	%
$V_{HYST-OVP}$	OVP Hysteresis Window	% of V_{OUT}		-4.3		
$V_{UVLO-HI-AVIN}$	AVIN UVLO Rising Threshold		**2.84**	2.93	**2.987**	V
$V_{UVLO-LO-AVIN}$	AVIN UVLO FallingThreshold		**2.66**	2.73	**2.83**	V
$V_{UVLO-HYS-AVIN}$	AVIN UVLO Hysteresis Window			195		mV
V_{VDD1}	Internal LDO1 Output Voltage	Measured At VDD1 Pin, 1 kΩ Load		4.88		V
$C_{OUT-VDD1}$	Recommended Bypass Capacitance to VDD1 Pin	Ceramic Capacitor		1		µF
$I_{Short-VDD1}$	VDD1 Pin Short Circuit Current			31		mA
V_{VDD2}	Internal LDO2 Output Voltage	Measured At VDD2 Pin, 1 kΩ Load		2.47		V
$C_{OUT-VDD2}$	Recommended Bypass Capacitance to VDD2 Pin	Ceramic Capacitor		100		nF
$I_{Short-VDD2}$	VDD2 Pin Short Circuit Current			47		mA
$VF_{CBOOT-d}$	CBOOT Diode Forward Voltage	Measured Between VDD1 and CBOOT @ 10 mA		0.76		V
I_{CBOOT}	CBOOT Leakage Current	V_{CBOOT} = 5.5 V, V_{EN} = 0 V		0.65		µA
$T_{Startup-Delay}$	Soft Start Delay Time	Measured From EN Rising Edge to The Beginning of Internal Soft-Start Ramp		160		µs
$T_{Soft-Start}$	Internal Soft-Start Ramping Time	From 10% to 90% V_{FB}, V_{FB} = 0.8 V	**1.9**	3.4	**5.3**	ms
		From 10% to 90% V_{FB}, V_{FB} = 1.0 V	**2.4**	4.3	**6.2**	
OSCILLATOR						
$F_{OSC-nom}$	Nominal Switching Frequency	R_{FRQ} = 61.9 kΩ 0.025%	**695**	750	**795**	kHz
$F_{OSC-MAX}$	Maximum Switching Frequency	R_{FRQ} = 28.4 kΩ		1500		
$F_{OSC-MIN}$	Minimum Switching Frequency	R_{FRQ} = 167.5 kΩ		300		
$T_{OFF-MIN}$	Switch Node Minimum OFF Time	f_S = 1.5 MHz, V_{PVIN} = 3.3 V, V_{FB} = 1.0 V, Resistor Divider Ratio = 3.3		50		ns
T_{ON-MIN}	Switch Node Minimum ON Time	f_S = 1.5 MHz, V_{FB} = 0.6 V, Resistor Divider Ratio = 1		70		
LOGIC						
V_{IH-EN}	EN Pin Rising Threshold		**1.1**	1.2	**1.3**	V
$V_{HYST-EN}$	EN Pin Hysteresis Window		**130**	200	**302**	mV
I_{EN-IN}	EN Pin Input Current	V_{EN} = 12 V		18	**23**	µA
$V_{IH-UV-PWROK}$	PWROK UV Rising Threshold	% of V_{OUT}	**87.5**	93	**97.5**	%
$V_{HYST-UV-PWROK}$	PWROK UV Hysteresis Window			-4.2		

General Electrical Characteristics (1) (2) (continued)

Specifications with standard typeface are for T_J = 25 °C, and those in **boldface type** apply over the full Operating Temperature Range (T_J = −40 °C to 125 °C). Unless otherwise specified, V_{PVIN} = V_{AVIN} = 12 V, V_{OUT} = 1.2 V.

Symbol	Parameter	Remarks	Min	Typ	Max	Unit
$I_{OL-\ PWROK}$	PWROK Sink Current	V_{OL} = 0.2 V		3		mA
$I_{OH-\ PWROK}$	PWROK Leakage Current	V_{OH} = 18 V			**460**	nA
PWI I/O: SPWI, SCLK. The VPWI pin is powered from an external source, VPWI range = 1.8V-10% to 3.3V+10%						
VPWI Slew Rate	VPWI Pin Voltage Ramping Rate	See(4)			**500**	µs
V_{IH}	Logic Input High	% of VPWI	**80**			%
V_{IL}	Logic Input Low	% of VPWI			**20**	%
I_{IH}	Input Leakage Current, Pin Driven High (VPWI)	SPWI, SCLK Pins Have Internal Pulldowns			**+5**	µA
I_{IL}	Input Leakage Current, Pin Driven Low		**-1**			
V_{OH}	Logic Output High	Sourcing 1mA, % of VPWI	**80**			%
V_{OL}	Logic Output Low	Sinking 1mA, % of VPWI			**10**	
R_{PD-PWI}	Pull-down resistance for PWI signals	SPWI, SCLK	**0.5**	1	**2**	MΩ
$F_{SCLK-MAX}$	Maximum PWI SCLK Frequency	SCLK		15		MHz
TD	SPWI Data Change Time to Valid Value	% of SCLK Cycle, F_{SCLK} ≤ 15 MHz(5)			**27**	%
TS	SPWI Data Setup Time	% of SCLK Cycle, F_{SCLK} ≤ 15 MHz(5)	**14**			
TH	SPWI Data Hold Time	% of SCLK Cycle, F_{SCLK} ≤ 15 MHz(5)	**39**			
TXZ	SPWI Data Drive Release Time	% of SCLK Cycle, F_{SCLK} ≤ 15 MHz(5)			**27**	
THERMAL SHUTDOWN						
TSD	Thermal Shutdown	See(6)		160		°C
TSD-HYS	Thermal Shutdown Hysteresis	See(6)		10		°C

(4) Recommend not to exceed 500 µs ramp time.
(5) Ensured by design. For more details, please refer to *PWI 1.0 Specifications* or *PWI 2.0 Specifications*.
(6) Ensured by design.

Typical Performance Characteristics

Unless otherwise specified: V_{PVIN} = V_{AVIN} = 12V, V_{OUT} = 1.2V, L=2.2µH, C_{OUT} = 220µF, fs = 300kHz.

Efficiency
fs = 300 kHz, V_{OUT} = 1.2 V, FPWM = 0

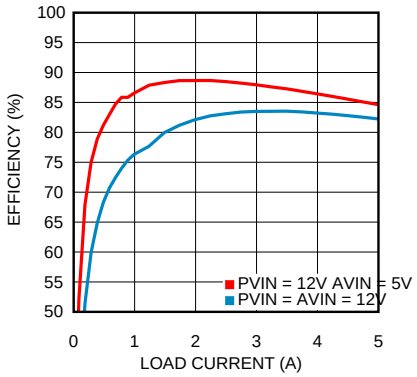


Figure 3.

Efficiency
fs = 300 kHz, V_{OUT} = 3.3 V, FPWM = 0

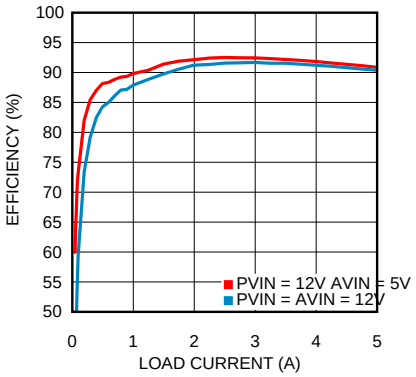


Figure 4.

Efficiency
fs = 300 kHz, P_{VIN} = A_{VIN} = 5 V, FPWM = 0

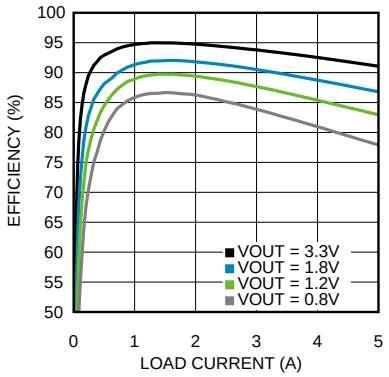


Figure 5.

Efficiency
fs = 300 kHz, P_{VIN} = A_{VIN} = 12 V, FPWM = 0

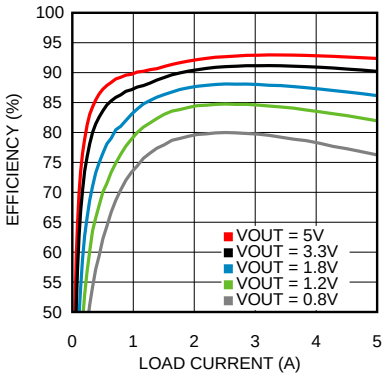


Figure 6.

Efficiency
fs = 500 kHz, P_{VIN} = A_{VIN} = 5 V, FPWM = 0

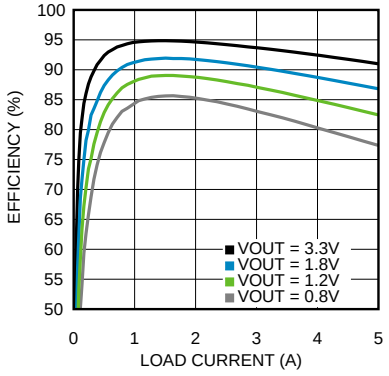


Figure 7.

Efficiency
fs = 500 kHz, P_{VIN} = A_{VIN} = 12 V, FPWM = 0

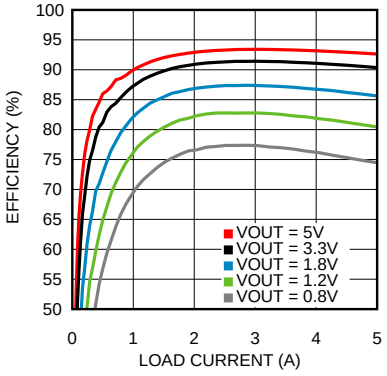


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified: V_{PVIN} = V_{AVIN} = 12V, V_{OUT} = 1.2V, L=2.2µH, C_{OUT} = 220µF, fs = 300kHz.

Load Regulation (%)

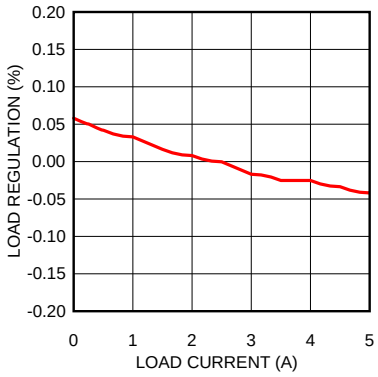


Figure 9.

Line Regulation (%)

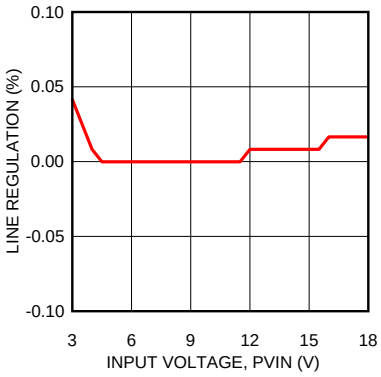


Figure 10.

V_{OUT}(%) Regulation vs. Temperature

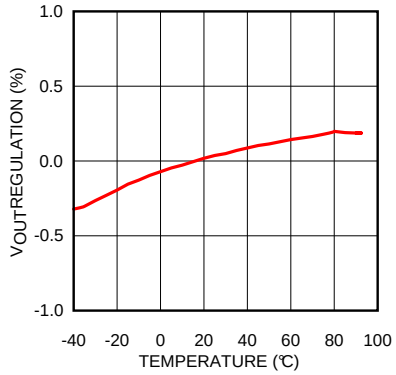


Figure 11.

Quiescent Current When I_{OUT} = 0, FPWM = 0

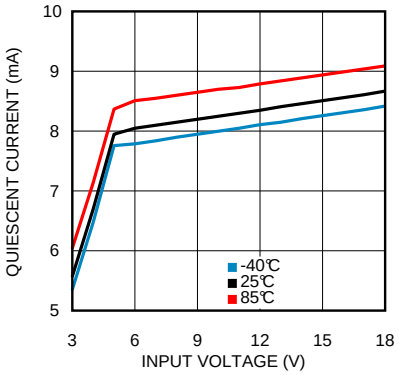


Figure 12.

High-Side and Low-Side R_{DSON} vs. Temperature

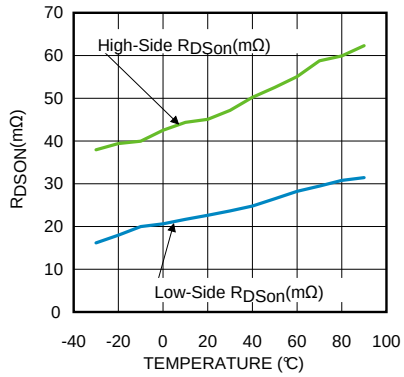


Figure 13.

Switching Frequency vs. R_{FRQ}

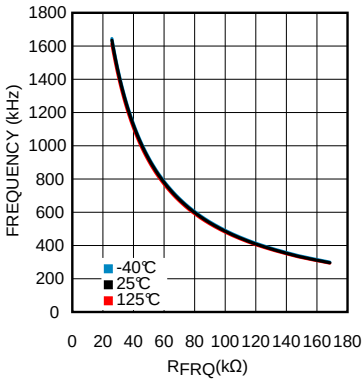


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified: $V_{PVIN} = V_{AVIN} = 12V$, $V_{OUT} = 1.2V$, L=2.2µH, $C_{OUT} = 220µF$, fs = 300kHz.

Soft Start With 5 A Load, Triggered By EN Rising Edge

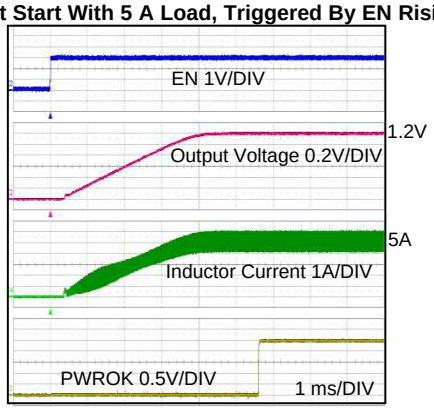


Figure 15.

Soft Start With No Load, Triggered By EN Rising Edge

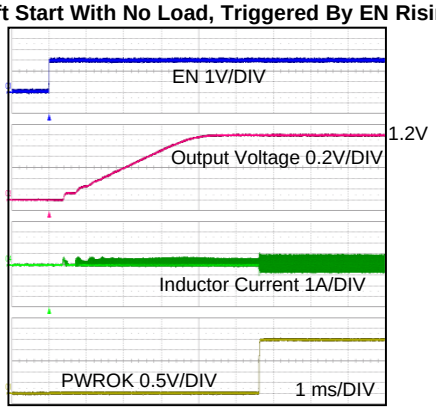


Figure 16.

Soft Start With 0.5V Pre-bias Voltage, DCM Operation, Triggered By PWI 'Wakeup' Command

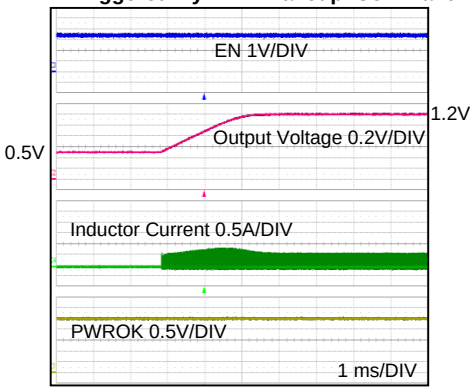


Figure 17.

Soft Start With 0.5V Pre-bias Voltage, CCM Operation, Triggered By PWI 'Wakeup' Command

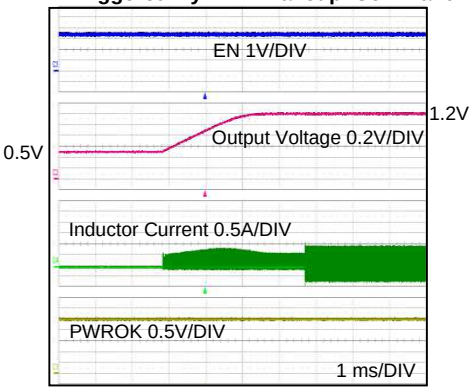


Figure 18.

Switching Waveform With 5 A Load

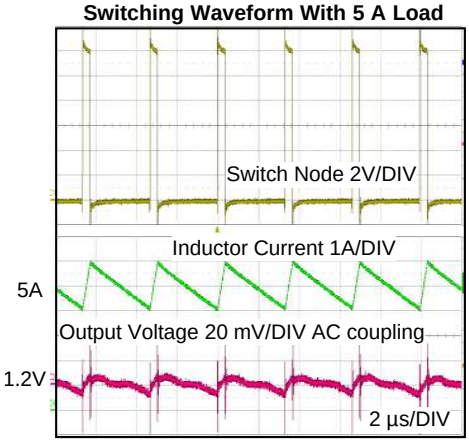


Figure 19.

Load Transient Between 0.1 A And 5 A

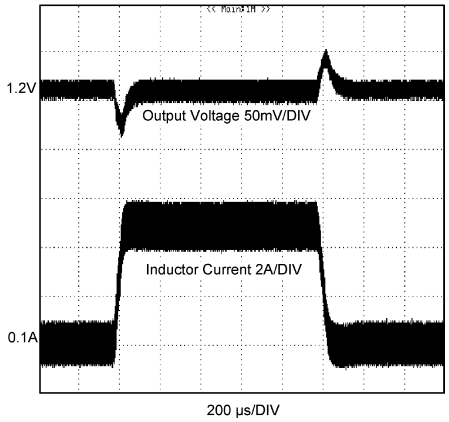


Figure 20.

LM10500 PWI REGISTER MAPS

SUMMARY

The PWI standard supports thirty-two 8-bit registers on the PWI slave. Table 1 summarizes these registers and shows default register bit values after reset. The following sub-sections provide additional details on the use of each individual register. Please refer to http://www.pwistandard.com/ for more detailed PWI 1.0 and PWI 2.0 specifications.

Table 1. Slave Base Register Summary

Register Address	Register Name	Register Usage	Type	Default Value(1)								
				7	6	5	4	3	2	1	0	HEX
0x0	R0	Core Voltage(2)	R/W	0	1	1	1	1	1	1	1	7F
0x1-0x3	R1-R3	Unused	N/A	-	-	-	-	-	-	-	-	
0x4	R4	PWI Version Number / Device Capability	R/O	-	-	-	-	-	-	**0**	**1**	01 PWI 1.0
										1	**0**	02 PWI 2.0
0x5 - 0x8	R5 - R8	Unused	N/A	-	-	-	-	-	-	-	-	N/A
0x9	R9	Core Voltage Offset(3)	R/W	-	1	0	0	0	0	0	0	40 Startup voltage 0.8V
				-	0	0	0	0	0	0	0	00 Startup voltage 1.0V
0xA	R10	Switcher Control(4)	R/W	-	-	-	-	-	1	1	1	07
0xB	R11	Unused	N/A	-	-	-	-	-	-	-	-	N/A
0xC-0xF	R12-R15	Reserved	N/A	-	-	-	-	-	-	-	-	N/A
0x10-0x1F	R16-R31	Not Implemented	N/A	-	-	-	-	-	-	-	-	N/A

(1) "-" denotes unused bits. A write into unused bit position will be ignored. A read will produce '0' when register is partially used and a "No response frame" when register is completely unused. A bit in BOLD denotes a register bit that is read-only. A read will result in the indicated value and a write will be ignored. Please refer to PWI specification version 1.0/2.0 for further information.
(2) Factory configurable to **0x7F**, 0x5F, 0x3F, or 0x1F.
(3) Factory configurable to **0x00**, 0x20, **0x40**, or 0x60.
(4) Manufacture default is Force PWM enabled.

Slave Extended Registers are not implemented in the LM10500.

Table 2. Slave Extended Register Summary

Register Address	Register Name	Register Usage	Type	Reset Default Value								
				7	6	5	4	3	2	1	0	HEX
0x00-0xFF	ER0-ER255	Not implemented	N/A	-	-	-	-	-	-	-	-	N/A

PWI Register Bit Definition

Bit definitions of R0, R4, R9 and R10 are listed in the tables below.

Table 3. R0 - Core Voltage Register

Bit	Field Name	Description or Comment	
7	Sign	This bit is fixed to 0.	
6:0	Voltage code	PWI 1.0/2.0 programmable from 7h'00 to 7h'7F. Default R0 = 7FH. Core voltage is determined by the Voltage Code = R0 − R9.	
		Voltage Code [6:0]	Core voltage with no external resistor divider (V)
		7h'00	0.6
		7h'xx	Linear scaling from 0.6 to 1.0, 3.15 mV / LSB
		7h'7F	1.0

R0 is restored to its default value when LM10500 wakes up from SLEEP state.

Table 4. R4 - PWI Version Number/Device Capability Register

Bit	Field Name	Description or Comment	
7:2	Reserved	Unused	
1:0	Version	Read only. Writing transactions to this register will be ignored. Read transaction will return:	
		2b′01	PWI version 1.0
		2b′10	PWI version 2.0

See PowerWise interface Selection section for configuring the device to PWI 1.0 or 2.0.

Table 5. R9 - Core Voltage Offset Register

Bit	Field Name	Description
7	Reserved	Unused
6:0	Core Voltage Offset code	The core voltage is determined by the Voltage Code = R0 − R9. R9 is intended for supporting APC1 or APC2 startup voltages that are less than top of the range (0x7F). In LM10500SQ-0.8 and LM10500SQX-0.8, default R9 = 40H In LM10500SQ-1.0 and LM10500SQX-1.0, default R9 = 00H

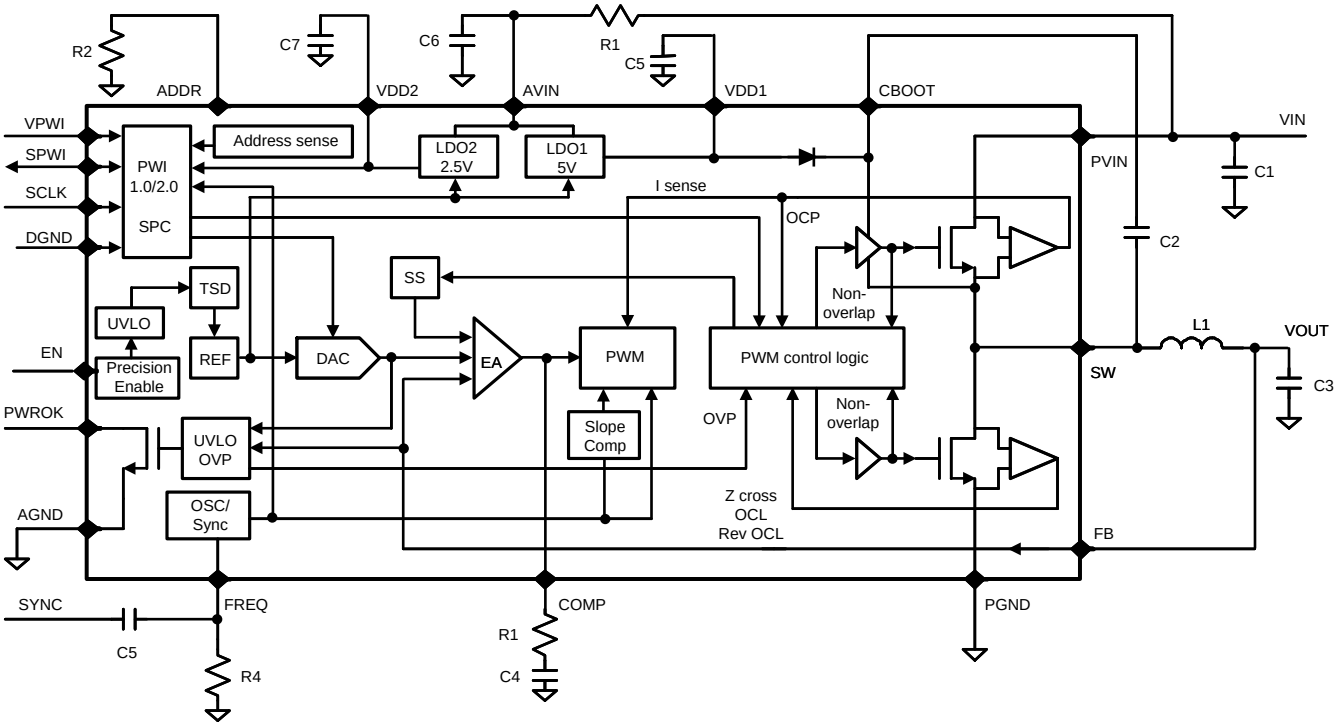
R9 is NOT restored to its default value when LM10500 wakes up from SLEEP state.

Table 6. R10 - Regulator Control Register

Bit	Field Name	Description
7:3	Reserved	Unused
2	Force PWM (FPWM)	1: Force switcher to operate in Continuous Conduction Mode (CCM) regardless of load 0: Switcher will operate in Discontinuous Conduction Mode (DCM) at light load
1	Voltage Down Slew Control Enable	1: Enable stepping slew rate control for large voltage code down step 0: Disable stepping slew rate control for down step
0	Voltage Up Slew Control Enable	1: Enable stepping slew rate control for large voltage code up step 0: Disable stepping slew rate control for up step

R10 is NOT restored to its default value when LM10500 wakes up from SLEEP state.

Block Diagram



Operation Description

LM10500 is a PowerWise Interface (PWI) 1.0 and 2.0 compliant energy management unit (EMU). It operates cooperatively with ASIC and FPGA cores using Advanced Power Controller (APC) to provide Adaptive or Dynamic Voltage Scaling (AVS or DVS) which drastically reduces power consumption compared to conventional power delivery methods. The device consists of PWI registers, logic, and a switching DC/DC buck converter to supply the AVS or DVS voltage domain. Please refer to http://www.pwistandard.com/ for more detailed PWI 1.0 and PWI 2.0 specifications.

SWITCHING REGULATOR

The LM10500 employs a buck type (step-down) architecture. It utilizes many advanced features to achieve excellent voltage regulation and efficiency. This easy-to-use regulator features two integrated switches and is capable of supplying up to 5 A of continuous output current. The regulator utilizes peak current mode control with slope compensation scaled with switching frequency to optimize stability and transient response over the entire output voltage and switching frequency range. Peak current mode control also provides inherent line feed-forward, cycle-by-cycle current limiting and easy loop compensation. The switching frequency can be adjusted between 300 kHz and 1.5 MHz. The device can operate with a small external L-C filter and still provide very low output voltage ripple. The precision internal voltage reference allows the output to be set as low as 0.6 V. Using an external compensation circuit, the regulator bandwidth can be selected based on the switching frequency to provide fast load transient response. The switching regulator is specially designed for high efficiency operation throughout the load range. Synchronous rectification yields high efficiency for low voltage and heavy load current situations, while optional Discontinuous Conduction Mode (DCM) operation extends high efficiency conversion to lower load currents. Fault protection features include: high-side and low-side switch current limiting, negative current limiting on the low-side switch, over voltage protection and thermal shutdown. The device is available in the WQFN-28 package featuring an exposed pad to aid thermal dissipation. The LM10500 can be used in numerous applications to efficiently step-down from a wide range of rails: 3 V to 18 V.

POWERWISE INTERFACE

The LM10500 is programmable via the low-power, 2-wire PowerWise Interface (PWI). This serial interface controls the various voltages and states of the regulator in the device. The switching regulator voltage at the feedback pin can be set between 0.6 V and 1.0 V in 127 steps (linear scaling, 3.15 mV per step). This high-resolution voltage control enables accurate temperature and process compensation in AVS.

The LM10500 supports the full command set as described in PWI 1.0 / 2.0 specifications:

- Core Voltage Adjust
- Reset
- Sleep
- Shutdown
- Wake-up
- Register Read
- Register Write
- Authenticate
- Synchronize

DEVICE OPERATIONAL STATES

This device has four operating states: STARTUP, ACTIVE, SHUTDOWN and SLEEP.

The STARTUP state is the default state after PWI Reset Command. The STARTUP state is entered from any other state if the EN pin is pulled to logic zero, or the PWI Reset Command is issued. When EN pin is in logic low, the regulator is off, and PWROK output is '0'. The DC-DC regulator will be enabled when the EN pin is pulled high. After the internal soft start, the device enters the ACTIVE state.

In the ACTIVE state, the voltage regulator is in normal operation and the PWROK output is '1'. Immediately after soft start, the output voltage is at the default level. The output voltage can then be scaled by programming the corresponding PWI control registers. If a PWI Shutdown Command is issued, the device will enter the SHUTDOWN state. Or if a PWI Sleep Command is issued, it will enter the SLEEP state.

In the SLEEP state, the voltage regulator is off, but the PWROK output is still '1'. The PWI registers can be programmed in the SLEEP state. The device can be activated from the SLEEP state to the ACTIVE state by the PWI Wake-Up Command. The register R0 will be reset to its default value (7FH) and all other register contents will remain unchanged. The device will enter the SHUTDOWN state by the PWI Shutdown Command.

In the SHUTDOWN state, the voltage regulator is off and PWROK signal is '0' as well. The device will exit the SHUTDOWN state to the STARTUP state if the EN pin is pulled low or a Reset Command is issued.

The diagram below summarized the four states and transitions. This figure assumes that the supply voltage to the regulator IC is in the valid range.

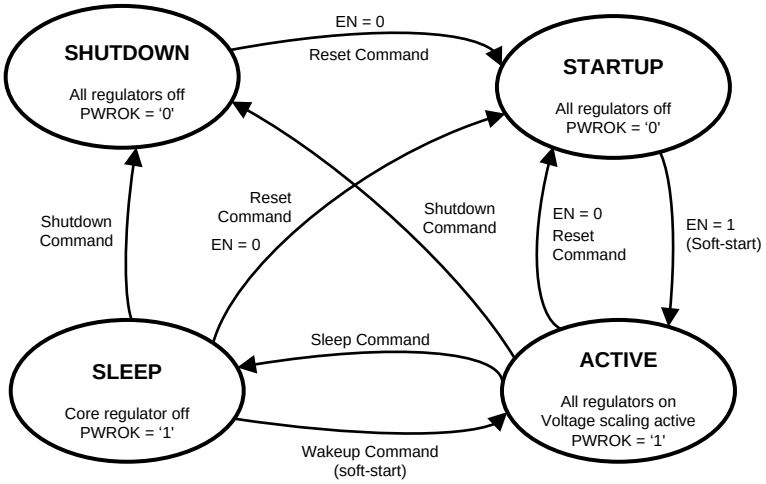


Figure 21. The LM10500 PWI Operating States

VOLTAGE SCALING

The device is designed to be used in a voltage scaling (AVS or DVS) enabled system to lower the power dissipation of SoCs or ASICs. By scaling the supply voltage with process variations, temperature variations, aging or the clock frequency, dramatic power savings can be achieved. Two types of voltage scaling are supported, dynamic voltage scaling (DVS) and adaptive voltage scaling (AVS). DVS systems switch between pre-characterized voltages which are paired to clock frequencies used for frequency scaling in the ASIC. AVS systems track the ASIC's performance and optimize the supply voltage adaptively to the required performance. AVS is a closed loop system that provides process and temperature compensation such that for any given process, temperature, or clock frequency, the minimum supply voltage that can achieve desired performance is delivered.

The output voltage of the switching regulator is programmed via the Core Voltage Adjust command sent by APC. PWI commands adjust the content of the PWI registers to adjust the AVS reference voltage (output of the internal DAC). The programmable reference voltage range is between 0.6 V and 1.0 V. The output voltage is the same as the AVS reference voltage when the FB pin is connected to the output voltage directly, otherwise, it will be scaled up by the output resistor divider. Please refer to the Design Guide section for design guidelines.

DIGITALLY ASSISTED VOLTAGE SCALING

The switching regulator in the LM10500 is designed to work in a voltage scaling system. This requires that the regulator has a well-controlled large signal transient response. The device delivers fast, controlled voltage scaling transients with the help of a digital state machine. The state machine automatically optimizes large signal transients providing minimal over / undershoot and maintaining settling times less than 100 µsec. This is an important characteristic for voltage scaling systems that rely on minimal undershoot to set voltages as low as possible to save more energy.

When a large voltage up or down step is requested by the PWI command, the straight forward way is to change the AVS voltage reference to the final value right away, as shown by the dash line in the figure below. The control loop will regulate the output voltage to follow the reference. Also, the inductor current needs to charge or discharge the output capacitors. The output voltage will have overshoot or undershoot and the inductor current will also show large current spikes.

In the LM10500, the large single step in AVS voltage reference is divided in a binary manner, as shown in by the solid line in the figure. By doing so, the large-signal voltage scaling response is smoothed out over time and the transients show almost no overshoot / undershoot. The slew rate control for voltage up and down steps can be enabled or disabled independently by register R10.

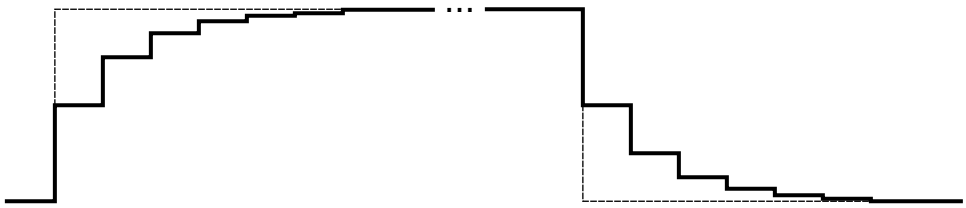


Figure 22. AVS Reference Voltage Large Step With Slew Rate Control (Solid Line) And Without Slew Rate Control (Dash Line)

PEAK CURRENT MODE CONTROL

In most applications, the peak current mode control architecture used in the LM10500 only requires two external components to achieve a stable design. The external compensation allows the user to set the crossover frequency and phase margin, thus optimizing the transient performance of the device. For duty cycles above 50%, all current mode control buck converters require the addition of an artificial ramp to avoid sub-harmonic oscillation. This linear ramp is commonly referred to as slope compensation. The amount of slope compensation in the LM10500 will automatically change depending on the switching frequency: higher the switching frequency, larger the slope compensation. This allows smaller inductors to be used with higher switching frequency to increase power density.

SWITCHING FREQUENCY SETTING AND SYNCHRONIZATION

The switching regulator in the LM10500 device can operate at frequencies ranging from 300 kHz to 1.5 MHz. The switching frequency can be set / controlled in two ways. One is by selecting an external resistor R_{FRQ} attached to the FREQ pin to set the internal oscillator frequency, which controls the switching frequency. An external 100 pF capacitor, C_{FRQ}, should also be connected from the FREQ pin to the analog ground as a noise filter, as shown in Figure 23.

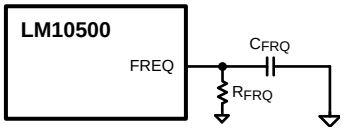


Figure 23. Switching Frequency Set By An External Resistor

The other way is to synchronize the switching action to an external clock or other fixed frequency signal in the range of 300 kHz to 1.5 MHz. The external clock should be applied through a 100 pF coupling capacitor, C_{FRQ}, as shown in Figure 24:

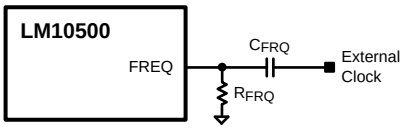


Figure 24. Switching Frequency Synchronized To External Clock

The recommendations for the external clock include peak-to-peak voltage above 1.5 V, duty cycle between 20% and 80%, and the edge rate faster than 100 ns. Circuits that use an external clock should still have a resistor, R_{FRQ}, connected from the FREQ pin to the analog ground. The external clock frequency should be within −10% to +50% of the frequency set by R_{FRQ}. This allows the regulator to continue operating at approximately the same switching frequency if the external clock fails and the coupling capacitor on the clock side is grounded or pulled to logic high.

If the external clock fails low, timeout circuits will prevent the high-side FET from staying off for longer than 1.5 times the switching period (switching period = 1 / switching frequency). At the end of this timeout period, the regulator will begin to switch at the frequency set by R_{FRQ}.

If the external clock fails high, timeout circuits will again prevent the high-side FET from staying off longer than 1.5 times the switching period. After this timeout period, the internal oscillator takes over and switches at a fixed 1 MHz until the voltage on the FREQ pin has decayed to approximately 0.6V. This decay follows the time constant of C_{FRQ} and R_{FRQ}, and once it is completed, the regulator will switch at the frequency set by R_{FRQ}.

LIGHT LOAD OPERATION

The LM10500 offers increased efficiency at light loads when the FPWM bit (bit 2 in PWI register R10) is '0', where Discontinuous Conduction Mode (DCM) is enabled. When the load current is reduced to a point where half of the inductor ripple current is greater than the load current, the device will enter DCM, thus preventing negative inductor current. The point at which this occurs is the critical conduction boundary and can be calculated by the following equation:

$$I_{BOUNDARY} = \frac{V_{OUT} \times (1 - D)}{2Lf_S} \quad (1)$$

where D is the duty cycle of the high side switch, equal to (high side switch on time / switching period). Please refer to CALCULATING THE DUTY CYCLE under Design Guide for more details. Several diagrams are shown in Figure 25 illustrating Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), and the boundary condition.

It can be seen that in DCM, whenever the inductor current reaches zero, the SW node will become high impedance. Ringing will occur on this pin as a result of the LC tank circuit formed by the inductor and the effective parasitic capacitance at the switch node. If this ringing is of concern, an additional RC snubber circuit can be added from the switch node to the power ground. At very light loads, usually below 100 mA, several pulses may be skipped in between switching cycles, effectively reducing the switching frequency and further improving light-load efficiency.

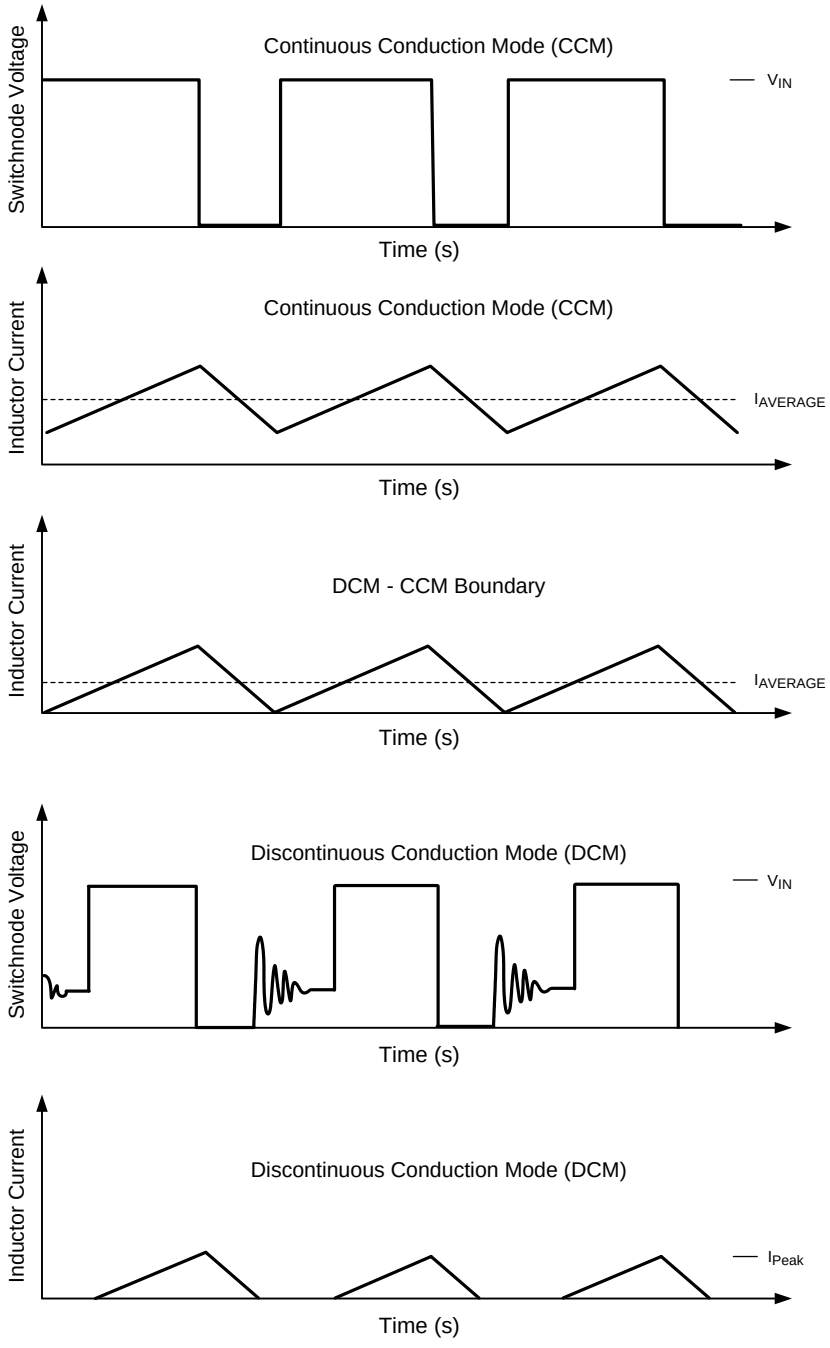


Figure 25. CCM and DCM Operation

FPWM OPERATION (FPWM BIT)

The regulator in the LM10500 can be programmed to operate in Continuous Conduction Mode (CCM) regardless of load, by setting the FPWM bit (bit 2 of PWI register R10) to '1'. When FPWM=1, the inductor current can be negative when load current is lower than critical conduction boundary (refer to LIGHT LOAD OPERATION section for more details). A negative current limit is implemented in the LM10500. If the inductor current goes below the limit, the low side switch will be turned off. When FPWM = 0, the regulator will operate in Discontinuous Conduction Mode (DCM) at light load, where inductor current will not be negative. At light load, DCM provides higher power conversion efficiency, while CCM operation provides smaller output voltage ripple and better transients.

The FPWM bit can be configured on the fly. However, when the load current is lower than the critical conduction boundary, an small over- or under-shoot may appear when toggling the FPWM bit. The reason is that duty cycle is different in CCM and DCM for a certain output voltage and load condition. When toggling the FPWM bit, the feedback loop needs time to adjust the duty cycle to the new value, resulting a small spike on V_{OUT}. If the FPWM bit is toggled when the current is above the critical conduction boundary, there will be NO spike at all. It is recommended to toggle the FPWM bit when the load current is above the critical conduction boundary, or when the device is in . The same reason explains a small voltage undershoot seen after soft start with light load and FPWM = 1. The regulator operates in diode emulation mode during soft start, the same behavior as in DCM. After desired V_{OUT} is reached, PWROK is released to high and the regulator will operate in CCM. The transition will result a small undershoot if load current is below the critical conduction boundary. The undershoot will NOT appear if FPWM = 0, or load current is above the critical conduction boundary.

PRECISION ENABLE

The enable (EN) pin allows the output of the device to be enabled or disabled by an external control signal. This pin is a precision analog input that enables the device when the voltage exceeds 1.2 V (typical). The EN pin has 200 mV (typical) of hysteresis and will disable the output when the enable voltage falls below 1.0 V (typical). If the EN pin is not used, it should be pulled up to AVIN via a 10 kΩ to 100 kΩ resistor. Since the enable pin has a precise turn on threshold, it can be used along with an external resistor divider network from AVIN or an external voltage to configure the device to turn on at a precise voltage. The precision enable circuitry will remain active even when the device is disabled. The turn on voltage with a divider can be found by:

$$V_{EN\text{-}EXT} = 1.2 \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) \quad (2)$$

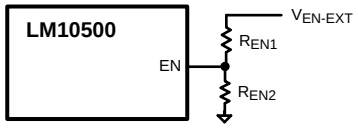


Figure 26. Use External Resistor To Set The EN Threshold

DEVICE SHUTDOWN AND ENABLE

The device output can be turned off by turning off AVIN, pulling the EN pin low, or issuing a PWI Shutdown Command with supply power ON and EN pin high.

To enable the device, EN pin must be high with the presence of AVIN and PVIN. Once enabled, the device engages the internal soft start and output voltage goes to its default value. The soft start feature allows the regulator output to gradually reach the steady state operating point, thus reducing stresses on the input supply and controlling start up current. Soft start begins when at the rising edge of EN with AVIN above UVLO level. It is important to make sure PVIN is high when soft start begins. The LM10500 allows AVIN to be higher than PVIN, or PVIN higher than AVIN, as long as both of them are within their operating voltage ranges.

When using PWI to issue a Shutdown Command, the PWI will be disabled along with the regulator in the device. To restart the part, EN pin must be toggled (high → low → high). The part will then begin soft start and output voltage will ramp to its default value. Please refer to the DEVICE OPERATIONAL STATES for more details.

The EN pin provides flexibility for system control. In larger systems, it can be advantageous to enable/disable a subsystem independently. The EN pin also allows the system controller to issue a global reset command to all the subsystems.

Figure 27 illustrates a shutdown and enable sequence of the LM10500.

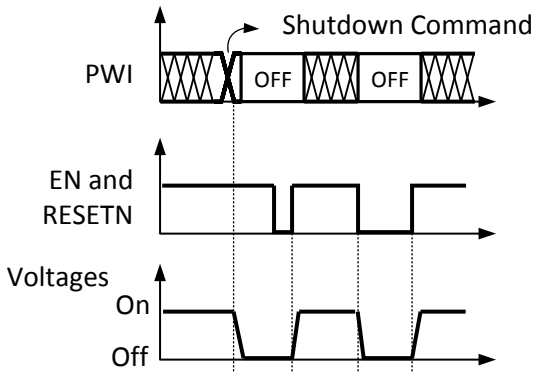


Figure 27. Shutdown And Enable Methods

UVLO

The LM10500 has a built-in Under-Voltage Lock-Out (UVLO) protection circuit that prevents the device from switching until the AVIN voltage reaches 2.93V (typical). The UVLO threshold has typically 195 mV of hysteresis that keeps the device from responding to power-on glitches during startup.

SOFT-START AND PRE-BIAS STARTUP CAPABILITY

Soft start of the LM10500 is controlled internally. It typically takes 4.3 ms to finish the soft start sequence in LM10500SQ-1.0 and 3.4 ms in LM10500SQ-0.8. PWROK will be high after soft start is finished.

The LM10500 is in a pre-biased state when the device starts up with an output voltage greater than zero. This often occurs in many multi-rail applications such as when powering an FPGA, ASIC, or DSP. In these applications the output can be pre-biased through parasitic conduction paths from one supply rail to another. Even though the LM10500 is a synchronous converter it will not pull the output low when a pre-bias condition exists. During start up the LM10500 will be in diode emulation mode: the low side switch is turned off when inductor current zero crossing is detected. After soft start, the operation mode programmed in PWI register R10 (FPWM = 0 or 1) is resumed.

PEAK CURRENT PROTECTION AND NEGATIVE CURRENT LIMITING

The switching regulator in the LM10500 detects the peak inductor current and limits it to the value of 7A typical. To determine the average current limit from the peak current limit, the inductor size, input and output voltages, and the switching frequency must be known. The average current limit can be found by:

$$I_{ave\text{-}limit} = I_{peak\text{-}limit} - \frac{(1-D)V_{OUT}}{2Lf_S} \quad (3)$$

When the peak inductor current sensed from the high-side switch reaches the current limit threshold, an over-current event is triggered and the internal high-side switch is turned off and the low-side FET is turned on, allowing the inductor current to ramp down until the next switching cycle. When the high-side over-current condition persists, the output voltage of the device will drop due to the reduced high side switch ON time.

In cases such as short circuit or when the high-side switch minimum on time conditions are reached, the high-side switch current limiting may not be sufficient to limit the inductor current. The LM10500 features an additional low-side switch current limit to prevent the inductor current from running away. The low-side switch current limit is set higher than the high-side current limit: 8 A typical. When the low-side switch current is higher than the limit level, PWM pulses will be skipped until the low-side over current event is not detected during the entire low-side switch conduction time. Normal PWM switching subsequently occurs when the condition is removed.

High-side and low-side current protections result in a current limit that does not aggressively fold back for brief over-current events, while at the same time providing frequency and voltage fold back protection during hard short circuit conditions.

The low-side switch also has negative current limit, -4.1 A typical. If the negative current limit is triggered, the low-side switch will be turned off. The negative current will be forced to go through the high-side switch body diode and it will quickly reduce to zero. The switch node will have a voltage pulse at (PVIN + 0.7 V) level due to the turning on of the high-side switch diode.

PWROK AND OVER-/UNDER-VOLTAGE HANDLING

The PWROK pin is an open-drain output. It should be pulled high with an external resistor (10 kΩ to 1 MΩ recommended). The PWROK pin will be high when the FB voltage is within −7% to +9.5% (typical) of the AVS reference voltage. Otherwise, an internal pull-down device will pull the PWROK pin low, as defined in the PWI specification.

The LM10500 has built-in under- and over-voltage comparators that control the high-side and low-side switches. Whenever there is an excursion in output voltage above the set Over Voltage Protection (OVP) threshold, +9.5% typical, the device will terminate high-side ON pulse if present, turn on the low-side switch, and pull the PWROK pin low. The low-side switch will remain ON until either the FB voltage falls back into regulation or the inductor current zero-cross is detected which in turn tri-states the switches. OVP is disabled during soft start to prevent false triggering.

If the output reaches the Under Voltage Protection (UVP) threshold, −7% typical, the device will continue switching and the PWROK pin will be pulled low. To avoid false tripping during transient glitches, the PWROK pin has 16 µs of built in deglitch time to both rising and falling edges.

INTERNAL REGULATORS

The LM10500 contains two internal Low DropOut (LDO) regulators to produce internal driving and bias voltage rails from AVIN. One LDO produces 5.0 V to power the internal MOSFET drivers, the other produces 2.5 V to power the internal bias circuitry. The 5.0 V LDO should be bypassed to analog ground through VDD1 pin with an external ceramic capacitor (1 µF recommended). The 2.5 V LDO should be bypassed to analog ground through VDD2 pin with an external ceramic capacitor (0.1 µF recommended). Good bypassing is necessary to supply the large transient currents required by the power MOSFET gate drivers.

Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation within the LDOs. Connecting a load to the VDD1 or VDD2 pin is not recommended since it will degrade their driving capability to the internal circuitry, further pushing the LDOs into their RMS current ratings, and increasing power dissipation and die temperature.

The LM10500 allows AVIN to be as low as 3 V which makes the voltage at the VDD1 LDO lower than 5 V. Low supply voltage at the MOSFET drivers will increase on-time resistance of the high-side and low-side MOSFETs and reduce efficiency of the regulator. When AVIN is between 3 V to 5 V, the best practice is to short the VDD1 pin to AVIN to avoid the voltage drop on the internal LDO. However, the device can be damaged if the VDD1 pin is pulled to a voltage higher than 5.5 V.

For efficiency considerations, it would be the best to use AVIN = 5 V if possible. When AVIN is above 5 V, reduced efficiency can be observed at light load due to the power loss on the LDOs. When AVIN is close to 3 V, increased MOSFET on-time resistance can reduce efficiency at high load current operations.

MINIMUM ON-TIME CONSIDERATIONS

Minimum on-time, T_{ON-MIN}, is the smallest duration of time that the high-side MOSFET can be on. This time is typically 70 ns in the LM10500. In CCM operation, the minimum on-time limit imposes a minimum duty cycle of

$$D_{MIN} = f_S \times T_{ON-MIN} \quad (4)$$

With a given output voltage, minimum on-time limits the switching regulator when operating with high input voltage and high switching frequency at the same time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint. With a given switching frequency and desired output voltage, the maximum allowed PVIN can be approximated by

$$V_{PVIN\text{-}max} = \frac{V_{OUT}}{f_S} \times \frac{1}{T_{ON\text{-}MIN}} \quad (5)$$

Similarly, if the input rail is fixed, the maximum switching frequency without imposing minimum on-time can be found by

$$f_{S\text{-}max} = \frac{V_{OUT}}{V_{PVIN\text{-}max}} \times \frac{1}{T_{ON\text{-}MIN}} \quad (6)$$

In rare cases, steady-state operation at minimum duty cycle is unavoidable. If the regulator is operating with FPWM = 1, the output voltage will increase with supply voltage or switching frequency, until OVP is triggered. OVP response will skip PWM cycles until output voltage drops back to the regulation band (below 105% of the regulated V_{OUT}). V_{OUT} will be regulated slightly above target with bigger ripple. This is a safe operating condition in most AVS applications. If FPWM = 0, DCM mode is allowed. The regulator will automatically skip PWM cycles to keep V_{OUT} in regulation, similar to light load DCM operation.

THERMAL PROTECTION

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that maximum junction temperature is exceeded. When activated, typically at 160 °C, the LM10500 tri-states the high-side and low-side power switches and resets soft-start. After the junction temperature cools down to approximately 150 °C, the regulator starts up again using normal startup routine. This feature is provided to prevent catastrophic failures from accidental device overheating.

Design Guide

This section walks the designer through the steps necessary to select the external components to build a fully functional PWI energy management unit (EMU). As with any DC-DC converter, numerous tradeoffs are possible to optimize the design for efficiency, size, and performance. These will be taken into account and highlighted throughout this discussion. To facilitate component selection discussions, the typical application circuit below may be used as a reference. Unless otherwise indicated, all formulas assume units of Amps (A) for current, Farads (F) for capacitance, Henries (H) for inductance, Volts (V) for voltages and Hertz (Hz) for frequencies.

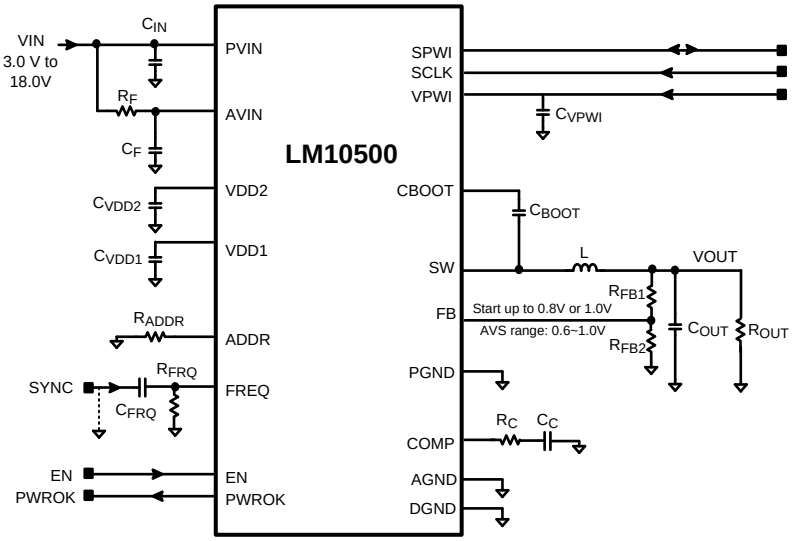


Figure 28. LM10500 Typical Application Circuit

PROGRAMMING THE OUTPUT VOLTAGE

The output voltage of LM10500 can be adjusted in two ways: V_{FB} is run-time programmable by PWI command through PWI interface, and a resistor divider can be used on the board to scale the (V_{OUT} / V_{FB}) ratio.

The FB pin can be connected to V_{OUT} directly or through a resistor divider. With external resistor divider, the output voltage can be scaled up from V_{FB}. Figure 29 shows the connection of the divider to the FB pin.

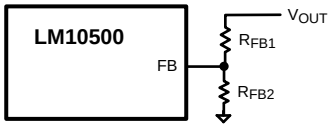


Figure 29. Setting the Output Voltage By Resistor Divider

The output voltage can be found by:

$$V_{OUT}=(1+\frac{R_{FB1}}{R_{FB2}})\times V_{FB} \quad (7)$$

V_{FB} power up voltage is 0.8 V in LM10500SQ-0.8 and 1.0 V in LM10500SQ-1.0. The output voltage programming range is scaled up by a factor of (1 + R_{FB1} / R_{FB2}). For example, if the desired power up voltage is 1.2 V, R_{FB1} = 2 kΩ, R_{FB2} = 10 kΩ can be used with LM10500SQ-1.0. The output voltage programming range becomes 0.72 V to 1.2 V. The maximum allowed output voltage is 5 V in the LM10500.

Unlike non-AVS power supplies, the reference voltage V_{FB} in the LM10500 is programmable by the PWI registers. The range of the AVS reference voltage is from 0.6 V to 1.0 V, corresponding linearly to voltage code 0x0 to 0x7F. The voltage code is determined by the codes in PWI register R0 (Core voltage register) and R9 (core voltage offset) as:

$$\text{Voltage Code} = \begin{cases} \text{R0 - R9}, & \text{R0 - R9} \geq 0 \\ 0, & \text{R0 - R9} < 0 \end{cases}$$

Voltage Code = (R0 - R9) [6:0]	Reference Voltage (V)
0x00	0.6
0x00 < code < 0x7F	Linear scaling from 0.6 to 1.0, 3.15 mV/LSB
0x7F	1.0

The R0 default code after power up is always 0x7F. The difference between LM10500SQ-0.8 and LM10500SQ-1.0 is shown in the table below. The default AVS reference voltage is usually the maximum reference voltage used in AVS operation to ensure safe operation for all conditions at start up.

	R0 default	R9 default	V_{FB} default	V_{FB} range
LM10500SQ-0.8	0x7F	0x40	0.8V	0.6 to 1.0V
LM10500SQ-1.0	0x7F	0x00	1.0V	0.6 to 1.0V

CALCULATING THE DUTY CYCLE

The first value to calculate for any buck converter is the duty cycle. In an ideal (no loss) buck converter, the ideal duty cycle can be found by:

$$D_{ideal} = \frac{V_{OUT}}{V_{PVIN}} \quad (8)$$

In applications with low output voltage (<1.2 V) and high load current (>3 A), which is typical in AVS operation, the losses should not be ignored when calculating the duty cycle. Considering the effect of conduction losses associated with the MOSFETs and inductor, the duty cycle can be approximated by:

$$D=\frac{V_{OUT}+I_{OUT}\left(R_{dson\text{-}LS}+DCR\right)}{V_{PVIN}+I_{OUT}\left(R_{dson\text{-}LS}-R_{dson\text{-}HS}\right)} \quad (9)$$

$R_{dson\text{-}HS}$ and $R_{dson\text{-}LS}$ are the ON-time parasitic resistances of the high-side and low-side MOSFETs, respectively. R_{dcr} is the equivalent DC resistance of the inductor used in the output filter. Other parasitics, such as PCB trace resistance, can be included in R_{DCR} if desired. I_{OUT} is the load current. It is also equal to the average inductor current. The duty cycle will increase slightly with the increase of load current.

SUPPLY POWER AND INPUT CAPACITORS

PVIN is the supply voltage for the regulator's power conversion. It is the supply that delivers the output power to the load. The input capacitors on PVIN rail supply the large AC switching current drawn by the switching action of the internal MOSFETs. The input current of a buck converter is discontinuous and the ripple current supplied by the input capacitors can be quite large. The input capacitors must be rated to handle this current, as well as the voltage. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS\_CIN} = I_{OUT}\sqrt{\frac{V_{OUT}\left(V_{IN}-V_{OUT}\right)}{P_{VIN}}}\ (A) \quad (10)$$

The power dissipation in the input capacitors can be found by:

$$P_{D\_CIN} = I^2_{RIM\_CIN}R_{ESR\_CIN}(W) \quad (11)$$

where R_{ESR_CIN} is the ESR of the input capacitor.

This equation has a maximum at $P_{VIN} = 2\times V_{OUT}$, where $I_{RMS} \cong I_{OUT}/2$ and D=50%. This simple worst-case condition is commonly used for design purposes because even significant deviations from the worst case duty cycle operating point do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low-input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes. A 1µF ceramic bypass capacitor is also recommended directly adjacent the PVIN and PGND pins. Please refer to the PCB LAYOUT CONSIDERATIONS section provided later in this document.

AVIN FILTER AND VPWI BYPASS

AVIN is the supply voltage for the internal control circuitry and the MOSFET drivers. An RC filter should be added to prevent any switching noise on PVIN from interfering with the internal analog circuitry connected to AVIN. These can be seen on the schematic as components R_F and C_F. There is a practical limit to the size of the resistor R_F as the AVIN pin will draw a short 60 mA burst of current during startup, and if R_F is too large the resulting voltage drop can trigger the UVLO comparator. A recommended 1 µF C_F capacitor coupled with a 1Ω resistor provides approximately 10 dB of attenuation at the 500 kHz switching frequency.

VPWI is the supply voltage to the PWI interface. The VPW voltage range is 1.8 V to 3.3 V, allowing ±10% voltage variation. It is recommended that VPWI voltage ramp up time is less than 500 µs. A 1 µF bypass capacitor is recommended to bypass the VPWI pin to ground.

SWITCHING FREQUENCY

The LM10500 supports a wide range of switching frequencies: 300 kHz to 1.5 MHz. The choice of switching frequency is usually a compromise between conversion efficiency and the size of the circuit. Lower switching frequency implies reduced switching losses (including gate charge losses, switch transition losses, etc.) and usually result in a higher overall efficiency. However, higher switching frequency allows use of smaller LC output filters and hence a more compact design. Lower inductance also helps transient response (higher large signal slew rate of inductor current), and reduces the DCR loss. The optimal switching frequency is usually a trade-off in a given application and thus meeds to be determined on a case-by-case basis. It is related to the input voltage, output voltage, most frequent load current level(s), external component choices, and circuit size requirement.

The choice of switching frequency may also be limited if an operating condition triggers T_{ON-MIN} or $T_{OFF-MIN}$. Please refer to the aforementioned MINIMUM ON-TIME CONSIDERATIONS section.

The following equation or figure can be used to calculate the resistance to obtain a desired frequency of operation: .

$$f_S[kHz] = 31000 \times R_{FRQ}^{-0.9}[k\Omega] \quad (12)$$

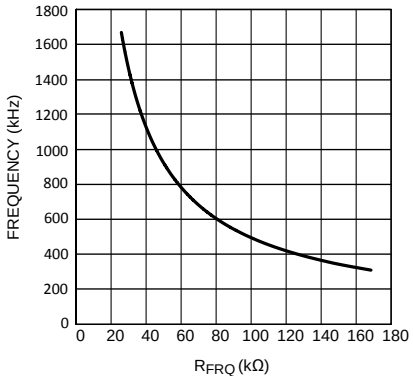


Figure 30. External Resistor Selection To Set The Switching Frequency

INDUCTOR

A general recommendation for the filter inductor in an LM10500 application is to keep a peak-to-peak ripple current between 20% and 40% of the maximum DC load current of 5A.

The peak-to-peak current ripple can be calculated by:

$$\Delta i_{Lp-p} = \frac{(1 - D) \times V_{OUT}}{f_S \times L} \approx \frac{V_{OUT}}{f_S \times L}\left(1 - \frac{V_{OUT}}{V_{PVIN}}\right) \quad (13)$$

The current ripple is larger with smaller inductance and/or lower switching frequency. It is recommended to choose L such that:

$$\frac{(1 - D) \times V_{OUT}}{f_S \times 0.4 \times I_{L(MAX)}} \le L \le \frac{(1 - D) \times V_{OUT}}{f_S \times 0.2 \times I_{L(MAX)}} \quad (14)$$

The inductor should be rated to handle the maximum load current plus the ripple current:

$$I_{L(MAX)} = I_{LOAD(MAX)} + i_{Lp-p(MAX)}/2 \quad (15)$$

An inductor with saturation current higher than the over current protection limit is a safe choice.

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. But too low of an inductance can generate too large of an inductor current ripple such that over current protection at the full load could be falsely triggered. It also generates more conduction loss, since the RMS current is slightly higher relative that with lower current ripple at the same DC current. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak current mode control, it is not recommended to have too small of an inductor current ripple, so that the peak current comparator has enough signal-to-noise ratio.

Once the inductance is determined, the type of inductor must be selected. Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. The ‘hard’ saturation results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

OUTPUT CAPACITOR

The device is designed to be used with a wide variety of LC filters. It is generally desired to use as little output capacitance as possible to keep cost and size down. The output capacitor(s), C_{OUT}, should be chosen with care since it directly affects the steady state output voltage ripple, loop stability and the voltage over/undershoot during load current transients.

The output voltage ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\text{-}ESR} = \Delta i_{Lp\text{-}p} \times ESR \tag{16}$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\text{-}C} = \frac{\Delta i_{Lp\text{-}p}}{8 f_S C_{OUT}} \tag{17}$$

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of the two peaks:

$$\Delta V_{OUT} < \Delta i_{Lp\text{-}p} \times \left(\frac{1}{8 f_S C_{OUT}} + ESR \right) \tag{18}$$

Figure 31 shows an illustration of two ripple components.

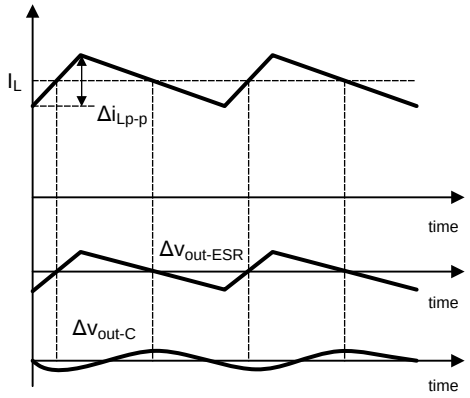


Figure 31. Two Components of V_{OUT} Ripple

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rates. When a fast large load transient happens, output capacitors provide the required charge before the inductor current can slew to the appropriate level. The initial output voltage step is equal to the load current step multiplied by the ESR. V_{OUT} continues to droop until the control loop response increases or decreases the inductor current to supply the load. To maintain a small over- or undershoot during a transient, small ESR and large capacitance are desired. But these also come with higher cost and size. Thus, the motivation is to seek a fast control loop response to reduce the output voltage deviation.

One or more ceramic capacitors are generally recommended because they have very low ESR and remain capacitive up to high frequencies. The capacitor dielectric should be X5R, X7R, or comparable material to maintain proper tolerance. Other types of capacitors also can be used, particularly if large bulk capacitance is needed (such as tantalum, POSCAP and OSCON). Such capacitors have lower ESR zero {1/(2π*ESR*×*C*)} frequency than ceramic capacitors. The lower ESR zero frequency can influence the control loop, particularly if it occurs close to the desired crossover frequency. If high switching frequency and high crossover frequency are desired, an all ceramic design would be more appropriate.

EFFICIENCY CONSIDERATIONS

The efficiency of a switching regulator is defined as the output power divided by the input power times 100%. Efficiency also can be found by

$$\eta = 1 - \frac{\text{Total Power Loss}}{\text{Input Power}} \quad (19)$$

It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in the LM10500-based converters: 1) conduction losses, 2) switching and gate driving losses, 3) bias losses.

Conduction losses are the I^2R losses on parasitic resistances in the path of the output current, including ON-time resistances of the internal switches (R_{DS-ON}), equivalent inductor DC resistance R_{dcr}, and PC board trace resistances R_{trace}. The conduction loss can be approximated by:

$$W_{cond-loss}=I^2_{OUT}(D\times R_{DS-ON-HS}+(1-D)\times R_{DS-ON-LS}+DCR+R_{trace}) \quad (20)$$

The total conduction loss can be reduced by reducing these parasitic resistances. For example, the LM10500 is designed to have low R_{DS-ON} internal MOSFET switches. The inductor DCR should be small. The traces that conduct the current should be wide, thick and as short as possible. The conduction losses affect the efficiency more at heavier load.

Switching losses include all the losses generated by the switching action of two power MOSFETs. Each time the switch node swings from low to high or vice versa, charges are applied or removed from the parasitic capacitance from the SW node to GND. Each time a power MOSFET gate is switched from low to high and to low again, a packet of charge moves from VDD1 to ground. Further more, each time a power MOSFET is turned on or off, a transition loss is generated relative to the overlapping area of voltage and current. MOSFET parasitic diodes generate reverse recovery loss and dead time conduction loss. RMS currents through the input and output capacitor ESR also generates loss. All of these losses should be evaluated and carefully considered to design a high efficiency switching power converter. Since these losses only occur during 'switching', reducing the switching frequency always help to reduce the switching loss. The resultant improvement in efficiency is more pronounced at lighter load.

AVIN provides MOSFET driving voltage and control circuit bias voltage. One part of loss on AVIN is from providing the current to the drivers, equals to V_{AVIN} x i_{drive}. The other portion of AVIN power loss is the bias current through VDD2, equals to V_{AVIN} x i_{bias}. i_{drive} does not change for AVIN above 5.0 V. If AVIN is below 5.0V, i_{drive} will reduce slightly, but R_{DS-ON} of the switches will increase and reduce efficiency more. i_{bias} is constant with AVIN between 3.0 V and 18.0 V. Powering AVIN from a 5 V system rail provides an optimal tradeoff between bias power loss and switching loss (R_{DS-ON} loss).

LOAD CURRENT DE-RATING AT HIGHER DUTY CYCLE OPERATION

The LM10500 is optimized for lower duty cycle operation, e.g. high input to output voltage ratio. The high-side MOSFET is designed to be half the size of the low-side MOSFET, thus optimizing the relative levels of switching loss in the high-side switch and the conduction loss in the low-side switch. The continuous current rating in the low-side switch is the maximum load current of 5 A, while the high-side switch is rated at 2.5 A. If the LM10500 is operating with duty cycle higher than 50%, the maximum output current should be derated.

$$I_{OUT-max} = 5 \times \min[\,(1.5 - D)\,,\,1] \quad (21)$$

Derating of maximum load current when D > 50% is also illustrated in Figure 32:

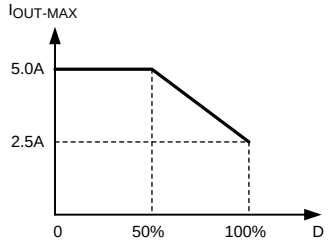


Figure 32. LM10500 Maximum Load Current Derating When D > 50%

CONTROL LOOP COMPENSATION

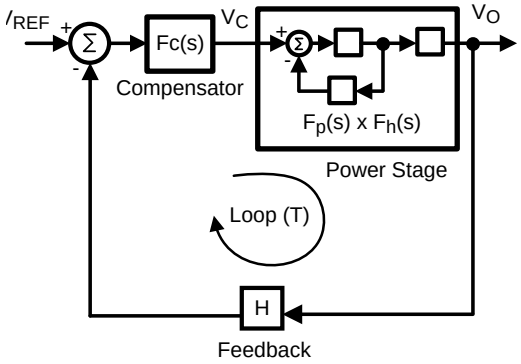


Figure 33. Control Block Diagram Of A Current Mode Controlled Buck Converter

The LM10500 employs a current mode controller and therefore the control block diagram representation involves two feedback loops (see Figure 33). The inner feedback loop derives its feedback from the sensed inductor current, while the outer loop monitors the output voltage. This section will not provide a rigorous analysis of current mode control, but rather a simplified yet relatively accurate method to determine the control loop compensation network.

The LM10500 compensation components from COMP pin to AGND are shown in Figure 34. The purpose of the compensator block is to stabilize the control loop and achieve high performance in terms of the transient response, audio susceptibility and output impedance. The LM10500 will typically require only a single resistor R_c and capacitor C_{c1} for compensation. However, depending on the location of the power stage ESR zero, a second (small) capacitor, C_{c2}, may be required between COMP and AGND to create a high-frequency pole.

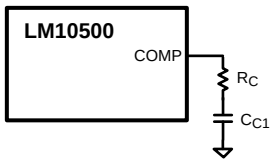


Figure 34. LM10500 Compensation Network

The overall loop transfer function is a product of the power stage transfer function, internal amplifier gains and the feedback network transfer function, and can be express by

$$T = Gain_0 F_p(s) F_h(s) F_{comp}(s) \quad (22)$$

where Gain0 includes all the DC gains in the loop, $F_p(s)$ represents the power stage pole and zero (including the inner current loop), $F_h(s)$ represents the sampling effect in such a switch-mode converter and $F_{comp}(s)$ is the transfer function of the external compensator. Figure 35 shows an asymptotic approximation plot of the loop gain.

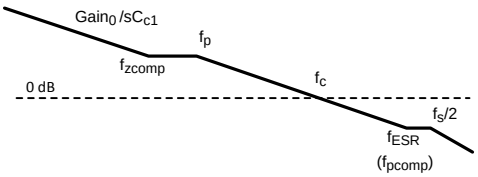


Figure 35. LM10500 Loop Gain Asymptote Approximation

The loop gain determines both static and dynamic performance of the converter. The power stage response is fixed by the selection of the power components and the compensator is therefore designed around the power stage response to achieve the desired loop response. The goal is to design a control loop with high crossover frequency (or loop bandwidth) and adequate phase margin under all operation conditions.

SELECT COMPENSATION COMPONENTS

To select the compensation components, a desired crossover frequency, f_c, needs to be selected. It is recommended to select $f_c \leq 1/6\ f_S$(switching frequency). The effect of $F_h(s)$ can be ignored in this range to simplify the design. The capacitor ESR zero is also assumed to be at least 3 times higher than f_c. The compensation resistor can be found by

$$R_c \approx \frac{1}{Gain_0} \times \frac{f_c}{f_p} = \frac{V_{OUT}}{V_{FB}} \times 302 \times f_c \times C_{OUT} \tag{23}$$

C_{c1} does not affect the crossover frequency f_c, but it sets the compensator zero f_{zcomp} and affects the phase margin of the loop. For a fast design, C_{c1} = 10 nF gives adequate performance in most LM10500 applications. Larger C_{c1} gives larger phase margin but in the expense of longer transient response settling time. Lower C_{c1} gives higher gain at lower frequency thus faster transient response. It is recommended to set the compensation zero no higher than $f_c/3$ to ensure enough phase margin, implying

$$C_{c1} \geq \frac{3}{2\pi R_c f_c} \tag{24}$$

PLOTTING THE LOOP GAIN

The include the effect of $F_h(s)$ and ESR zero, the complete loop gain can be plotted using a software tool, such as Matlab, Mathcad, or Excel. The components in the loop gain can by found as follows. The constant $Gain_0$ in the loop, as shown in Figure 35, can be found by

$$Gain_0 = \frac{V_{FB}}{V_{OUT}} \times \frac{R_{OUT}}{1 + \frac{R_{OUT}}{f_s L}(m_c D' - 0.5)} \times 0.0208 \tag{25}$$

where f_s is the switching frequency; m_c can be found by

$$m_c = 1 + \frac{4 \times f_S \times L}{V_{IN} - V_{OUT}} \tag{26}$$

and

$$D' = 1 - D \tag{27}$$

Minimum R_{OUT} should be used in the calculation:

$$R_{OUT} = V_{OUT}/I_{OUT} \tag{28}$$

$F_p(s)$ can be expressed by:

$$F_p(s) = \frac{1 + sC_{OUT} * ESR}{1 + \frac{s}{2\pi f_p}} \tag{29}$$

where the power stage pole considering the slope compensation effect is:

$$f_p = \frac{1}{2\pi C_{OUT}} \left(\frac{1}{R_{OUT}} + \frac{1}{f_s L} (m_c D' - 0.5) \right) \tag{30}$$

The high frequency behavior $F_h(s)$ can be expressed by:

$$F_h(s) = \frac{1}{1 + \frac{s}{w_n Q_p} + \frac{s^2}{w_n^2}} \tag{31}$$

where

$$w_n = \pi f_s \text{ and } Q_p = \frac{1}{\pi(m_c D' - 0.5)} \tag{32}$$

The compensation network transfer function is:

$$F_{comp}(s) = R_c + \frac{1}{sC_{c1}} \quad (33)$$

With above equations, the loop gain

$$T = Gain_0 F_p(s) F_h(s) F_{comp}(s) \quad (34)$$

can be plotted and more accurate loop performance metrics (crossover frequency and phase margin) can be found.

HIGH-FREQUENCY CONSIDERATIONS

$F_h(s)$ represents the additional magnitude and phase drop around $f_s/2$ caused by the switching behavior of the current mode converter. $F_h(s)$ contains a pair of double poles with quality factor Q_p at half of the switching frequency. It is a good idea to check that Q_p is between 0.15 and 2, ideally around 0.6. If Q_p is too high, the resonant peaking at $f_s/2$ could become severe and coincide with subharmonic oscillations in the duty cycle and inductor current. If Q_p is too low, the two complex poles split, the converter begins to act like a voltage mode controlled converter and the compensation scheme used above should be changed.

$F_p(s)$ also contains the ESR zero of the output capacitors:

$$f_{ESR} = \frac{1}{2\pi C_{OUT} ESR} \quad (35)$$

In a typical ceramic capacitor design, f_{ESR} is at least three times higher than the desired crossover frequency f_c. If f_{ESR} is lower tha $f_s/2$, an additional capacitor C_{c2} can be added between the COMP pin and AGND to give a high-frequency pole.

$$C_{c2} = \frac{1}{2\pi R_c f_{ESR}} \quad (36)$$

C_{C2} should be and usually is much smaller than C_{C1} to avoid affecting the compensation zero.

BOOTSTRAP CAPACITOR

A ceramic capacitor is needed between the CBOOT pin to the SW node to supply the gate drive charge when the high-side switch is turning ON. The capacitance should be large enough to supply the charge without significant voltage drop. A 0.1 µF bootstrap capacitor is recommended in LM10500 applications.

POWERWISE INTERFACE ADDRESS SELECTION

External 1% resistor connecting between the ADDR pin to AGND sets the PWI address.

PWI Standard	Description	Typ	Unit
$R_{PWI1.0}$	Address selection resistor for PWI-1.0	≤20	kΩ
$R_{PWI2.0\text{-}0}$	Address selection resistor for PWI-2.0, address 0	40.2	kΩ
$R_{PWI2.0\text{-}1}$	Address selection resistor for PWI-2.0, address 1	60.4	kΩ
$R_{PWI2.0\text{-}2}$	Address selection resistor for PWI-2.0, address 2	80.6	kΩ
$R_{PWI2.0\text{-}3}$	Address selection resistor for PWI-2.0, address 3	100	kΩ

The external resistance is only sensed one time when the part is powered up. If the address selection resistor is modified after power up, it won't take effect until a power cycling is performed.

VDD1 AND VDD2 BYPASS CAPACITORS

VDD1 and VDD2 pins are internal LDO outputs. As previously mentioned, the two LDOs are used for internal circuits only and should not be substantially loaded.

Bypass capacitors are needed to stabilize the LDOs. Ceramic capacitors within a specified range should be used to meet stability requirements. The dielectric should be X5R, X7R, or better and rated for the required operating temperature range. Use the following table to choose suitable LDO bypass capacitor.

	Output voltage NOMINAL (V)	Output Capacitance Range (recommended typical value)
VDD1	4.88	1 µF ± 20% 16V
VDD2	2.47	0.1 µF ± 20% 10V

PCB LAYOUT CONSIDERATIONS

PC board layout is an important part of DC/DC converter design. Poor PC board layout can disrupt the performance of a DC/DC converter and surrounding circuitry by contributing to EMI, noise coupling, ground bounce, and resistive voltage loss in the traces, and thermal problems. Erroneous signals can reach the DC-DC converter, possibly resulting in poor regulation or in instability.

Good PCB layout for an LM10500-based converter can be implemented by following a few simple design rules.

1. Provide adequate device heat sinking by utilizing the PAD of the IC as the primary thermal path. Use a 3 by 3 array of 10 mil thermal vias to connect the PAD to the system ground plane heat sink. The vias should be evenly distributed under the PAD. Use a four-layer board with the copper thickness for the four layers, starting from the top one, 2 oz / 1 oz / 1 oz / 2 oz. Four layer boards with enough copper thickness provides low current conduction impedance and proper shielding.
2. It is imperative that the input capacitors be located as close as possible to the PVIN pins; the inductor should be placed as close as possible to the SW pins and the output capacitors. This is to minimize the area of switching current loops to reduce EMI, and reduce the resistive loss on the high current path. The copper area of the switch node should be thick and short to provide a good conduction path for the switch node current to the inductor. Make input and output power bus connections as wide and short as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. Use copper plates/planes on the top layer to connect the multiple PVIN pins together and PGND pins together.
3. All bypass capacitors should be placed as close as possible to the corresponding pin and ground. Based on the LM10500 pinout, a 1 µF to 10 µF capacitor can be placed right by pins 1, 2 and pin 7, across the SW node trace, as an addition to the bulk input capacitors. Using a size 1206 or larger capacitor allows enough copper width for the switch node to be routed underneath the capacitor for good conduction (see evaluation board layout in application node AN-2080).
4. It is recommended to use one of the middle layers as a solid ground plane. Ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and DGND pins should be connected to the ground plane using vias right next to the bypass capacitors. DGND should also be connected to the source where VPWI is provided. PGND pins are connected to the source of the internal low-side switch. They should be connected directly to the grounds of the input and output capacitors. The PGND net contains noise at switching frequency and may bounce due to load variations. PGND trace, as well as PVIN and SW traces, should be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and should be used for sensitive routes.
5. To reduce noise sensitivity of the output voltage feedback path, it is important to place the resistor divider close to the FB pin, rather than close to the load. The FB pin is the input to the error amplifier, so it is a high impedance node and very sensitive to noise. Placing the resistor divider closer to the FB pin reduces the trace length of FB signal and reduces noise coupling. The output node is a low impedance node, so the trace from Vout to the resistor divider can be long if short path is not available. The COMP is also a noise sensitive node and the compensation components should be located as close as possible to the IC.
6. If voltage accuracy at the load is important, make sure voltage sense is made at the load. Doing so will correct for voltage drops along the traces and provide the best output accuracy. The voltage sense trace from the load to the feedback resistor divider should be routed away from the SW node path and the inductor to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high value resistors are used to set the output voltage. It is recommended to route the voltage sense trace and place the resistor divider on a different layer than the inductor and SW node path such that there is a ground plane in between the feedback trace and inductor/SW node polygon. This provides further shielding for the voltage feedback path from EMI noise.
7. The 0.1 µF boot capacitor connected between the CBOOT pin and the SW node should be placed as close as possible to the CBOOT pin and SW pins.
8. The frequency set resistor and its associated capacitor should be placed as close as possible to the FREQ pin.
9. The PWI address set resistor should be place as close as possible to the ADDR pin.

10. The traces to SCLK and SPWI pins should be routed parallel to each other and as short as possible. If this is a multi-master and/or multi-slave system, care should be taken in matching the trace lengths of all segments of the PWI bus. Additionally, the designer must ensure that the electrical characteristics of interconnect do not violate the restrictions in the PowerWise Interface 1.0 / 2.0 specifications.

THERMAL CONSIDERATIONS

The thermal characteristics of the LM10500 are specified using the parameter θ_{JA}, which relates junction temperature to ambient temperature in a particular application. Although the value of θ_{JA} is dependant on many variables, it still can be used to approximate the operating junction temperature of the device. To obtain an estimate of the device junction temperature, one may use the following relationship:

$$T_J = P_D \theta_{JA} + T_A \quad (37)$$

where

- T_J = Junction temperature in °C
- $P_D = P_{IN} \times (1 - \text{Efficiency}) - 1.1 \times I_{OUT} \times DCR$
- P_{IN} = Input power in Watts ($P_{IN} = V_{IN} \times I_{IN}$)
- I_{OUT} = Output load current
- DCR = Inductor DC parasitic resistance.
- θ_{JA} = Junction-to-ambient thermal resistance of the LM10500 in °C/W
- T_A = Ambient temperature in °C

It is important to always keep the LM10500 operating junction temperature (T_J) below 125 °C to ensure reliable operation. If the junction temperature exceeds 160 °C, the device will cycle in and out of thermal shutdown. If thermal shutdown occurs, it is a sign of inadequate heat-sinking and/or excessive power dissipation in the device. PC Board heat-sinking can be improved by using more thermal vias, a larger board, or more heat-spreading layers within the board.

Application Example

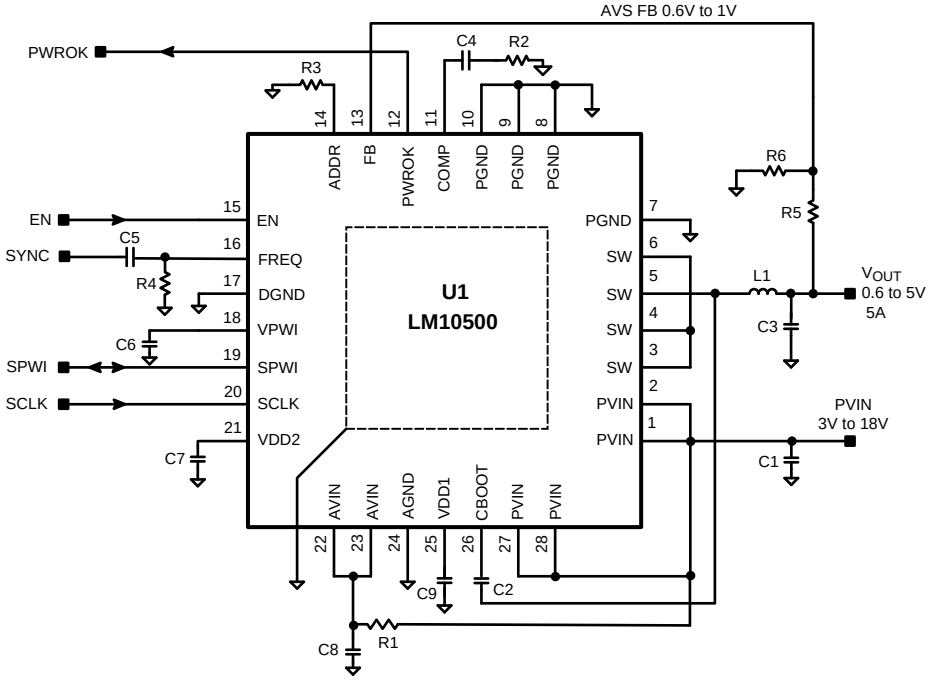


Figure 36. Application Circuit Example

Bill Of Materials

The table below shows BOMs for a V_{OUT} = 0.8 V design and for a V_{OUT} = 1.2 V design. In both applications, PVIN = AVIN = 12 V, fs = 300 kHz, $I_{OUT-MAX}$ = 5 A, and PWI 1.0 are used. For information on the LM10500 evaluation boards, please refer to AN-2080.

Table 7. Bill of Materials for LM10500 0.8 V and 1.2 V Applications

Designator	For 0.8V design	For 1.2V design	Manufacture	Qty
U1	LM10500SQ-0.8	LM10500SQ-1.0	TI	1
C1	TANT 47µF 25V	TANT 47µF 25V	KEMET	1
	CERAMIC 10µF 50V X7S	CERAMIC 10µF 50V X7S	TAIYO YUDEN	1
	CERAMIC 1.0 µF 35V X5R	CERAMIC 1.0 µF 35V X5R	TAIYO YUDEN	1
C2, C7	CERAMIC 0.1 µF 50V X7R	CERAMIC 0.1 µF 50V X7R	TAIYO YUDEN	2
C3	CERAMIC 47 µF10V X5R	CERAMIC 47 µF10V X5R	MURATA	1
	220 µF POLYMER 6.3V	220 µF POLYMER 6.3V	PANASONIC	1
C4	CERAMIC 10000 pF 25V	CERAMIC 10000 pF 25V	TDK	1
C5	CERAMIC 100 pF 100V	CERAMIC 100 pF 100V	PANASONIC	1
C6, C8, C9	CERAMIC 1.0 µF 35V X5R	CERAMIC 1.0 µF 35V X5R	TAIYO YUDEN	3
L1	1.2 µH SMD INDUCTOR	2.2 µH SMD INDUCTOR	COILCRAFT	1
R1	1Ω 0603 1%	1Ω 0603 1%	YAGEO	1
R2	1.75 KΩ 0603 1%	2kΩ 0603 1%	YAGEO	1
R3	0 Ω 0603 1%	0 Ω 0603 1%	YAGEO	1
R4	169 KΩ 0603 1%	169 kΩ 0603 1%	YAGEO	1
R5	0 RΩ 0603 1%	2kΩ 0603 1%	YAGEO	1
R6	open	10.0 kΩ 0603 1%	YAGEO	1

PCB Layout Example

An example of an LM10500 PCB layout is shown in Figure 37. Only the top layer and the silk screen are shown. For more details, please refer to application note AN-2080 SNVA453.

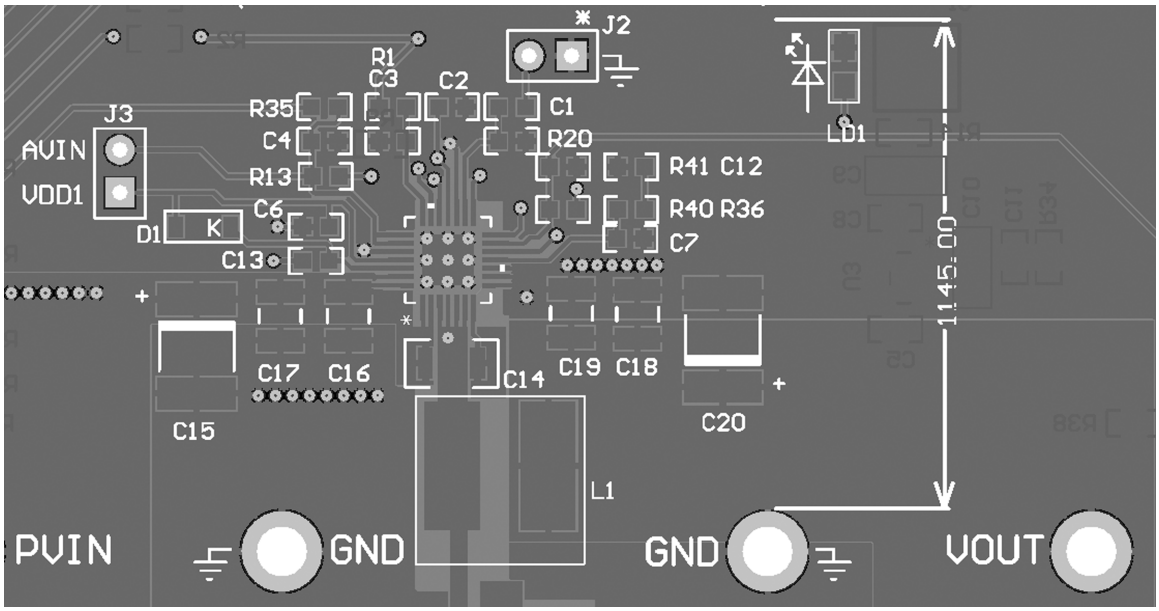


Figure 37. PCB Layout Example: Top Layer and Silk Screen

REVISION HISTORY

Changes from Revision F (March 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	33

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM10500SQ-0.8/NOPB	ACTIVE	WQFN	RSG	28	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2A-260C-4 WEEK	-40 to 85	1050008	Samples
LM10500SQ-1.0/NOPB	ACTIVE	WQFN	RSG	28	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2A-260C-4 WEEK	-40 to 85	1050010	Samples
LM10500SQE-0.8/NOPB	ACTIVE	WQFN	RSG	28	250	Green (RoHS & no Sb/Br)	CU SN	Level-2A-260C-4 WEEK		1050008	Samples
LM10500SQE-1.0/NOPB	ACTIVE	WQFN	RSG	28	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		1050010	Samples
LM10500SQX-0.8/NOPB	ACTIVE	WQFN	RSG	28	4500	Green (RoHS & no Sb/Br)	CU SN	Level-2A-260C-4 WEEK	-40 to 85	1050008	Samples
LM10500SQX-1.0/NOPB	ACTIVE	WQFN	RSG	28	4500	Green (RoHS & no Sb/Br)	CU SN	Level-2A-260C-4 WEEK	-40 to 85	1050010	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

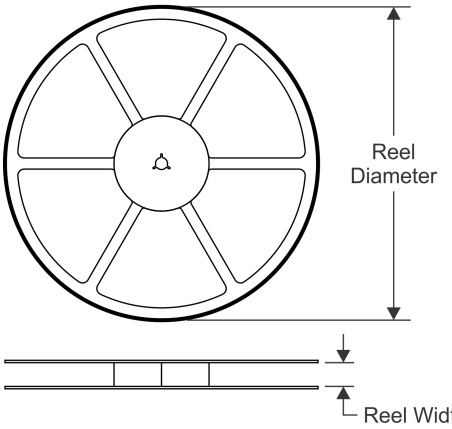
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

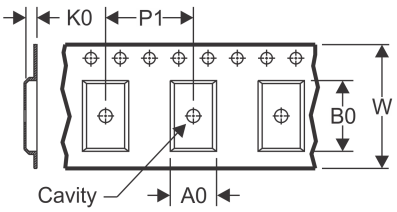
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

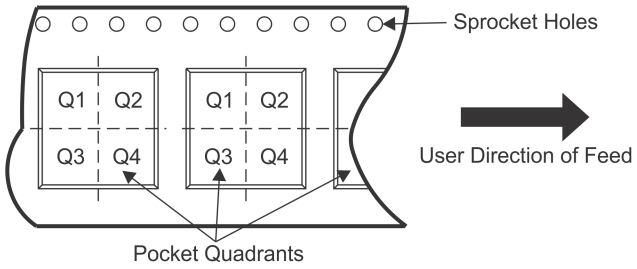


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

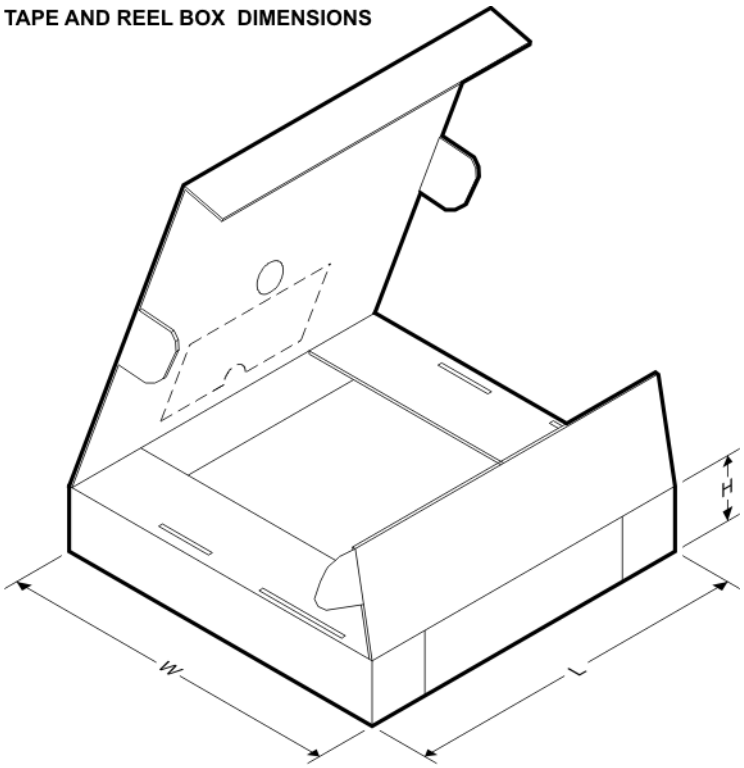
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM10500SQ-0.8/NOPB	WQFN	RSG	28	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM10500SQ-1.0/NOPB	WQFN	RSG	28	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM10500SQE-0.8/NOPB	WQFN	RSG	28	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM10500SQE-1.0/NOPB	WQFN	RSG	28	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM10500SQX-0.8/NOPB	WQFN	RSG	28	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LM10500SQX-1.0/NOPB	WQFN	RSG	28	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM10500SQ-0.8/NOPB	WQFN	RSG	28	1000	210.0	185.0	35.0
LM10500SQ-1.0/NOPB	WQFN	RSG	28	1000	210.0	185.0	35.0
LM10500SQE-0.8/NOPB	WQFN	RSG	28	250	210.0	185.0	35.0
LM10500SQE-1.0/NOPB	WQFN	RSG	28	250	210.0	185.0	35.0
LM10500SQX-0.8/NOPB	WQFN	RSG	28	4500	367.0	367.0	35.0
LM10500SQX-1.0/NOPB	WQFN	RSG	28	4500	367.0	367.0	35.0

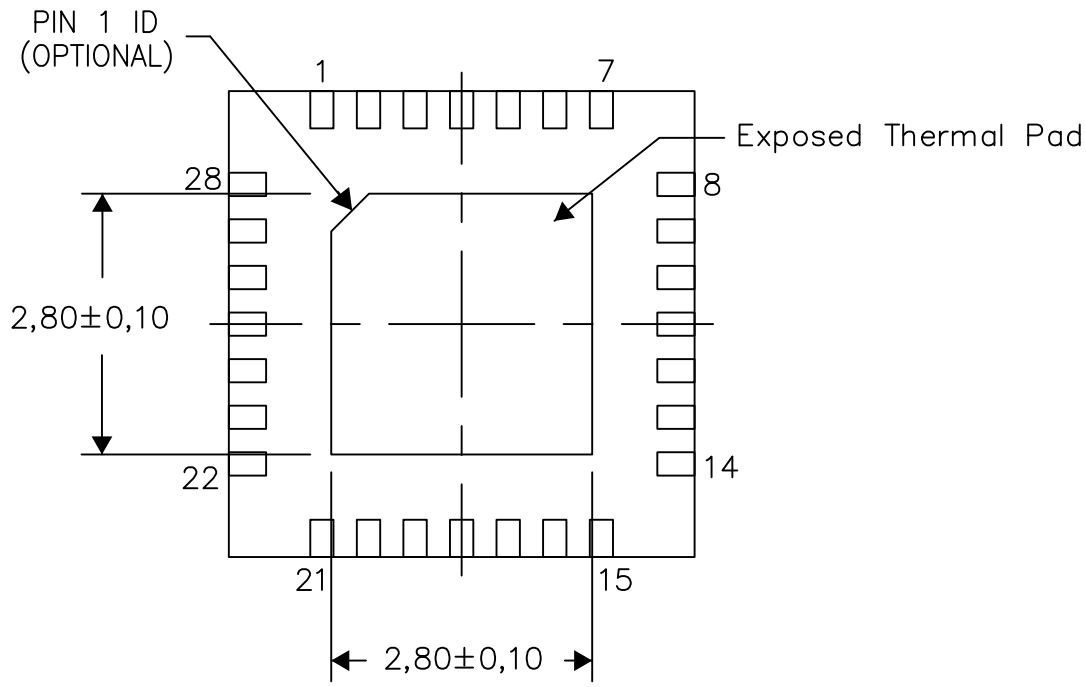
RSG (S–PWQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4221534–3/B 04/15

NOTE: All linear dimensions are in millimeters

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