



CCB LC72720YVS

CMOS IC

Single-Chip RDS Signal-Processing System IC

ON Semiconductor®

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Overview

The LC72720YVS is a single-chip system IC that implement the signal processing required by the European Broadcasting Union RDS (Radio Data System) standard and by the US NRSC (National Radio System Committee) RBDS (Radio Broadcast Data System) standard. This IC include band-pass filter, demodulator, synchronization, and error correction circuits as well as data buffer RAM on chip and perform effective error correction using a soft-decision error correction technique.

Functions

- Band-pass filter : switched capacitor filter (SCF)
- Demodulator : RDS data clock regeneration and demodulated data reliability information
- Synchronization : Block synchronization detection
(with variable backward and forward protection conditions)
- Error correction : Soft-decision/hard-decision error correction
- Buffer RAM : Adequate for 24 blocks of data (about 500ms) and flag memory
- Data I/O : CCB interface (power on reset)

Features

- Error correction capability improved by soft-decision error correction
- The load on the control microprocessor can be reduced by storing decoded data in the on-chip data buffer RAM.
- Two synchronization detection circuits provide continuous and stable detection of the synchronization.
- Data can be read out starting with the backward-protection block data after a synchronization reset.
- Fully adjustment free

Specifications

- Operating power-supply voltage : 3.0 to 3.6V
- Operating temperature : -40 to +85°C
- Package : SSOP30(275mil)

- CCB is ON Semiconductor® 's original format. All addresses are managed by ON Semiconductor® for this format.

- CCB is a registered trademark of Semiconductor Components Industries, LLC.

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Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{\text{SSD}} = V_{\text{SSA}} = 0\text{V}$

| Parameter | Symbol | Pin Name | Ratings | Unit |
|-----------------------------|---------|---|------------------|------------------|
| Maximum supply voltage | Vddmax | Vddd, Vdda | -0.3 to +7.0 | V |
| Maximum input voltage | Vin1max | CL, DI, CE, SYR, T1, T2, T3, T4, T5, T6, T7, SYNC | -0.3 to +7.0 | V |
| | Vin2max | XIN | -0.3 to Vddd+0.3 | V |
| | Vin3max | MPXIN, CIN | -0.3 to Vdda+0.3 | V |
| Maximum output voltage | Vo1max | DO, SYNC, RDS-ID, T3, T4, T5, T6, T7 | -0.3 to +7.0 | V |
| | Vo2max | XOUT | -0.3 to Vddd+0.3 | V |
| | Vo3max | FLOUT | -0.3 to Vdda+0.3 | V |
| Maximum output current | Io1max | DO, T3, T4, T5, T6, T7 | +6.0 | mA |
| | Io2max | XOUT, FLOUT | +3.0 | mA |
| | Io3max | SYNC, RDS-ID | +20.0 | mA |
| Allowable power dissipation | Pdmax | ($T_a \leq 85^\circ\text{C}$) | 150 | mW |
| Operating temperature | Topr | | -40 to +85 | $^\circ\text{C}$ |
| Storage temperature | Tstg | | -55 to +125 | $^\circ\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ranges at $T_a = -40$ to 85°C , $V_{\text{SSD}} = V_{\text{SSA}} = 0\text{V}$

| Parameter | Symbol | Pin Name | Conditions | Ratings | | | Unit |
|---|------------------|--------------------------------------|--|---------|-------|-----------|---------------|
| | | | | min | typ | max | |
| Supply voltage | Vdd1 | Vddd, Vdda | | 3.0 | | 3.6 | V |
| | Vdd2 | Vddd | Serial data hold voltage | 2.0 | | | V |
| Input high-level voltage | V_{IH} | CL, DI, CE, SYR, T1, T2 | | 0.7Vddd | | 6.5 | V |
| Input low-level voltage | V_{IL} | CL, DI, CE, SYR, T1, T2 | | 0 | | 0.3Vddd | V |
| Output voltage | V_{O} | DO, SYNC, RDS-ID, T3, T4, T5, T6, T7 | | | | 6.5 | V |
| Input amplitude | V_{IN1} | MPXIN | $f=57 \pm 2\text{kHz}$ | | | 50 | mVrms |
| | V_{IN2} | | 100% modulation composite | 100 | | | mVrms |
| | V_{XIN} | XIN | | 400 | | 1500 | mVrms |
| Guaranteed crystal Oscillator frequencies | XTAL | XIN, XOUT | $C_L \leq 120\Omega$ (XS=0) | | 4.332 | | MHz |
| | | | $C_L \leq 70\Omega$ (XS=1) | | 8.664 | | MHz |
| Crystal oscillator frequency deviation | TXtal | XIN, XOUT | $f_0=4.332\text{MHz}$, 8.664MHz | | | ± 100 | ppm |
| Data setup time | tSU | DI, CL | | 0.75 | | | μs |
| Data hold time | tHD | DI, CL | | 0.75 | | | μs |
| Clock low level time | tCL | CL | | 0.75 | | | μs |
| Clock high level time | tCH | CL | | 0.75 | | | μs |
| CE wait time | tEL | CE, CL | | 0.75 | | | μs |
| CE setup time | tES | CE, CL | | 0.75 | | | μs |
| CE hold time | tEH | CE, CL | | 0.75 | | | μs |
| CE high-level time | tCE | CE | | | | 20 | ms |
| Data latch change time | tLC | | | | | 1.15 | μs |
| Data output time | tDC | DO, CL | Differs depending on the value of the pull-up resistor used. | | | 0.46 | μs |
| | tDH | DO, CE | | | | 0.46 | μs |

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Electrical Characteristics at $T_a = -40$ to 85°C , $V_{SSD} = V_{SSA} = 0\text{V}$

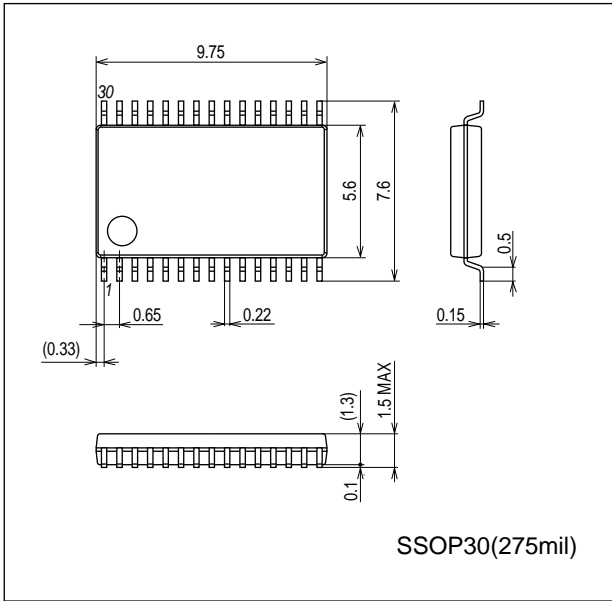
| Parameter | Symbol | Pin Name | Conditions | Ratings | | | Unit |
|------------------------------|-------------|--------------------------------------|--------------------------------------|---------|--------------|-----------|---------------|
| | | | | min | typ | max | |
| Input resistance | R_{MPXIN} | MPXIN-Vssa | $f=0$ to 100kHz | | 23 | | $k\Omega$ |
| Internal feedback resistance | R_f | XIN | | | 1.5 | | $M\Omega$ |
| Center frequency | f_c | FLOUT | | 56.5 | 57.0 | 57.5 | kHz |
| -3dB band width | BW-3dB | FLOUT | | 2.5 | 3.0 | 3.5 | kHz |
| Gain | Gain | MPXIN-FLOUT | $f=57\text{kHz}$ | 28 | 31 | 34 | dB |
| Stop band Attenuation | Att1 | FLOUT | $\Delta f = \pm 7\text{kHz}$ | 30 | | | dB |
| | Att2 | FLOUT | $f < 45\text{kHz}, f > 70\text{kHz}$ | 40 | | | dB |
| | Att3 | FLOUT | $f < 20\text{kHz}$ | 50 | | | dB |
| Group delay deviation | G-Delay | FLOUT | $f = 57 \pm 1.2\text{kHz}$ | | | ± 2.0 | μs |
| Reference voltage output | V_{ref} | V_{ref} | $V_{DDA} = 5.0\text{V}$ | | 1.65 | | V |
| Hysteresis | V_{HIS} | CL, DI, CE, SYR, T1, T2 | | | $0.1V_{DDD}$ | | V |
| Output low-level voltage | V_{OL1} | DO, T3, T4, T5, T6, T7 | $I = 2\text{mA}$ | | | 0.5 | V |
| | V_{OL2} | SYNC, RDS-ID | $I = 8\text{mA}$ | | | 0.5 | V |
| Input high-level current | I_{IH1} | CL, DI, CE, SYR, T1, T2 | $V_I = V_{DDD}$ | | | 5.0 | μA |
| | I_{IH2} | XIN | $V_I = V_{DDD}$ | 0.9 | | 4.0 | μA |
| Input low-level current | I_{IL1} | CL, DI, CE, SYR, T1, T2 | $V_I = 0\text{V}$ | | | 5.0 | μA |
| | I_{IL2} | XIN | $V_I = 0\text{V}$ | 0.9 | | 4.0 | μA |
| Output off leakage current | I_{OFF} | DO, SYNC, RDS-ID, T3, T4, T5, T6, T7 | $V_O = 6.5\text{V}$ | | | 5.0 | μA |
| Current drain | I_{DD} | V_{DDD}, V_{DDA} | $V_{DDD} = V_{DDA} = 3.3\text{V}$ | | 6 | | mA |

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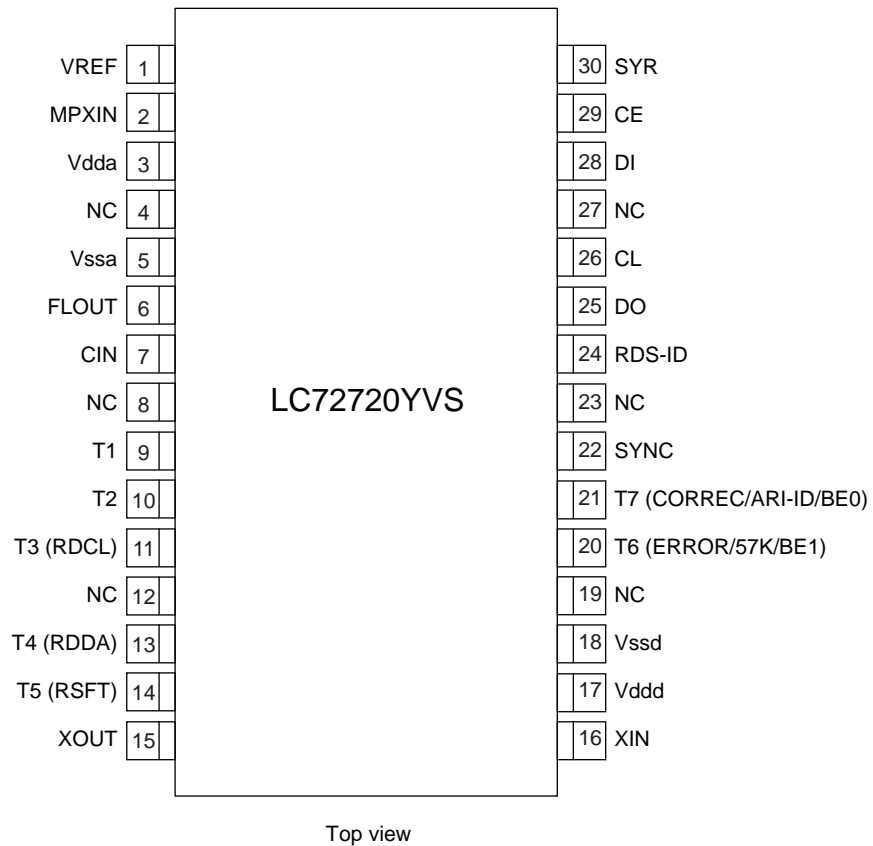
Package Dimensions

unit : mm (typ)

3191C

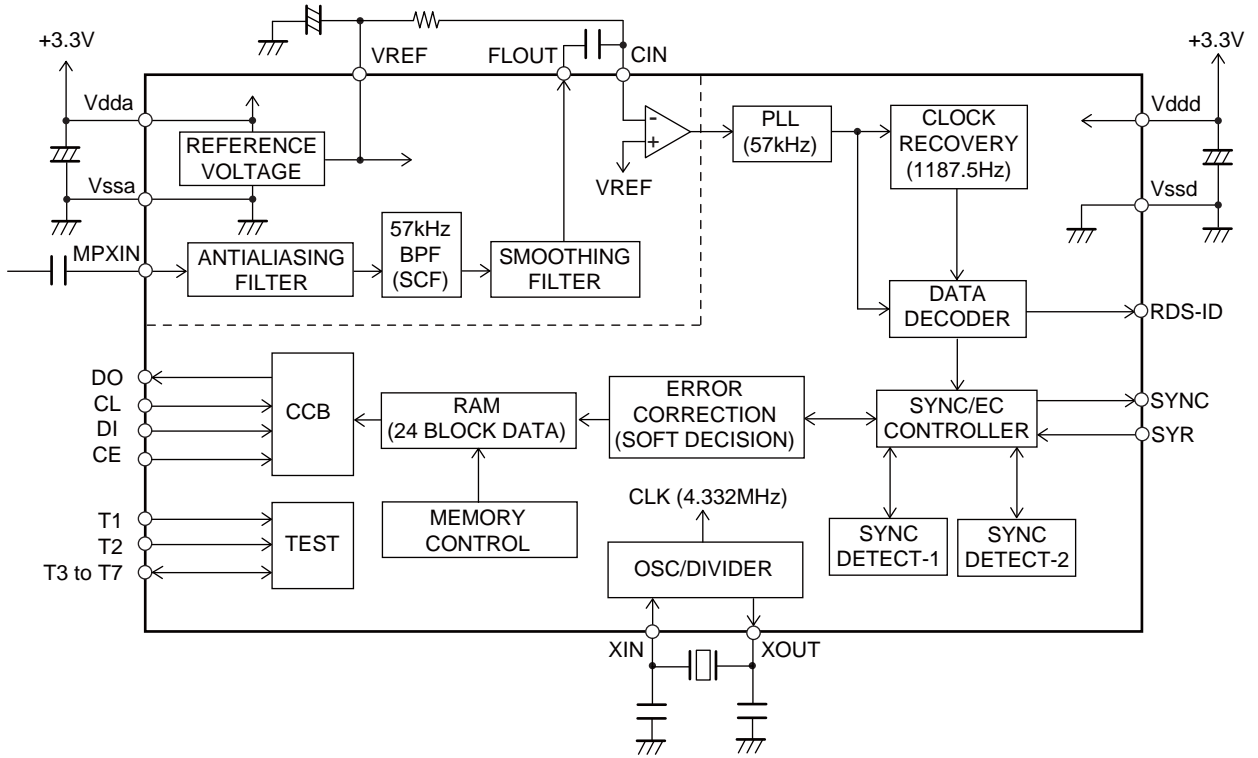


Pin Assignment



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Block Diagram



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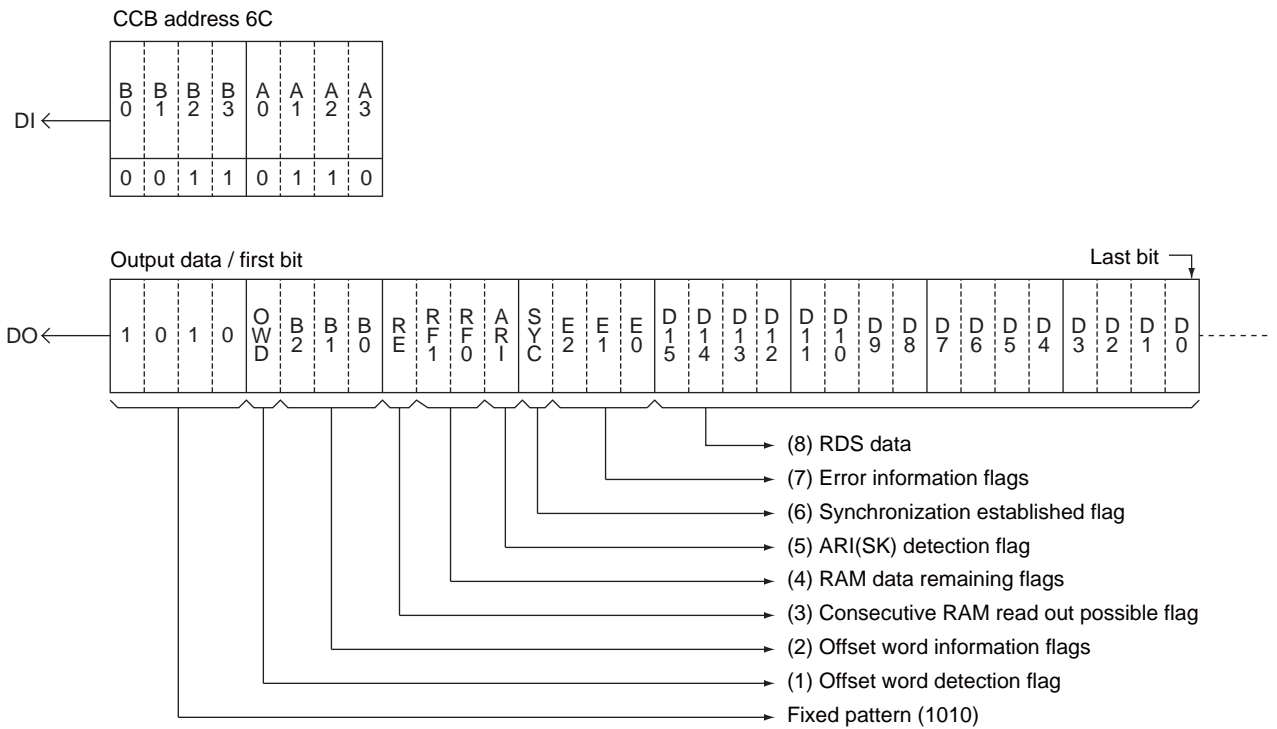
Pin Functions

| Pin No. | Pin name | Function | I/O | Pin circuit |
|---------|---------------------------|---|--------|-------------|
| 1 | VREF | Reference voltage output (Vdda/2) | Output | |
| 2 | MPXIN | Baseband (multiplexed) signal input | Input | |
| 6 | FLOUT | Subcarrier output (filter output) | Output | |
| 7 | CIN | Subcarrier input (comparator input) | Input | |
| 3 | Vdda | Analog system power supply (+3.3V) | - | - |
| 5 | Vssa | Analog system ground | - | - |
| 15 | XOUT | Crystal oscillator output (4.332/8.664MHz) | Output | |
| 16 | XIN | Crystal oscillator input (external reference signal input) | Input | |
| 9 | T1 | Test input (This pin must always be connected to ground.) | Input | |
| 10 | T2 | Test input (standby control) 0:Normal operation, 1:Standby state (crystal oscillator stopped) | | |
| 11 | T3(RDCL) | Test I/O (RDS clock output) | I/O* | |
| 13 | T4(RDDA) | Test I/O (RDS data output) | | |
| 14 | T5(RSFT) | Test I/O (soft-decision control data output) | | |
| 20 | T6 (ERROR/57K/BE1) | Test I/O (error status, regenerated carrier, error block count) | | |
| 21 | T7 (CORREC/ARI-ID/BE0) | Test I/O (error correction status, SK detection, error block count) | | |
| 22 | SYNC | Block synchronization detection output | Output | |
| 24 | RDS-ID | RDS detection output | | |
| 25 | DO | Data output | Input | |
| 26 | CL | Clock input | | |
| 28 | DI | Data input | | |
| 29 | CE | Chip enable | | |
| 30 | SYR | Synchronization and RAM address reset (active high) | | |
| 17 | Vddd | Digital system power supply (+3.3V) | - | - |
| 18 | Vssd | Digital system ground | - | - |

Note : * Normally function as an output pin. Used as an I/O pin in test mode, which is not available to user applications. Pin 4, 8, 12, 19, 23, 27 are NC (NO CONNECT) Pins.

CCB output data format

1. Each block of output data consists of 32 bits (4 bytes), of which 2 bytes are RDS data and 2 bytes are flag data.
2. Any number of 32-bits output data blocks can be output consecutively.
3. When there is no data that can be read out in the internal memory, the system outputs blocks of all-zero data consecutively.
4. If data readout is interrupted, the next read operation starts with the 32-bit data block whose readout was interrupted.
However, if only the last bit is remaining to be read, it will not be possible to re-read that whole block.
5. The check bits (10 bits) are not output.
6. The data valid (OWD) must not be referred to.
7. When the first leading bits are not "1010", the read in data is in invalid, and read operation is cancelled.



(1) Offset word detection flag (1bit) : OWD

| OWD | Offset word detection |
|-----|--|
| 1 | Detected |
| 0 | Not detected (protection function operating) |

(2) Offset word information flag (3bit) : B0 to B2

| B ₂ | B ₁ | B ₀ | Offset word |
|----------------|----------------|----------------|-------------|
| 0 | 0 | 0 | A |
| 0 | 0 | 1 | B |
| 0 | 1 | 0 | C |
| 0 | 1 | 1 | C' |
| 1 | 0 | 0 | D |
| 1 | 0 | 1 | E |
| 1 | 1 | 0 | Unused |
| 1 | 1 | 1 | Unused |

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(3) Consecutive RAM read out possible flag (1bit) : RE

| RE | RAM data information |
|----|---|
| 1 | The next data to be read out is in RAM |
| 0 | This data item is the last item in RAM, and the next data is not present. |

(4) RAM data remaining flag (2bits) : RF0,RF1

| RF1 | RF0 | Remaining data in RAM (number of blocks) |
|-----|-----|--|
| 0 | 0 | 1 to 7 |
| 0 | 1 | 8 to 15 |
| 1 | 0 | 16 to 23 |
| 1 | 1 | 24 |

Caution : This value is only meaningful when RE is 1. When RE is 0, there is no data in RAM, even if RF is 00.
If a synchronization reset was applied using SYR, then the backward protection block data that was written to memory is also counted in this value.

(5) ARI(SK) detection flag (1bit) : ARI

| ARI | SK signal |
|-----|--------------|
| 1 | Detected |
| 0 | Not detected |

(6) Synchronization established flag (1bit) : SYC

| SYC | Synchronization detection |
|-----|---------------------------|
| 1 | Synchronized |
| 0 | Not synchronized |

Caution : This flag indicates the synchronization state of the circuit at the point when the data block being output was received.
On the other hand, the SYNC pin (pin18) output indicates the current synchronization state of the circuit.

(7) Error information flags (3bits) : E0 to E2

| E 2 | E 1 | E 0 | Number of bits corrected |
|--------|--------|--------|--------------------------|
| 0 | 0 | 0 | 0 (no errors) |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | Correction not possible |
| 1 | 1 | 1 | Unused |

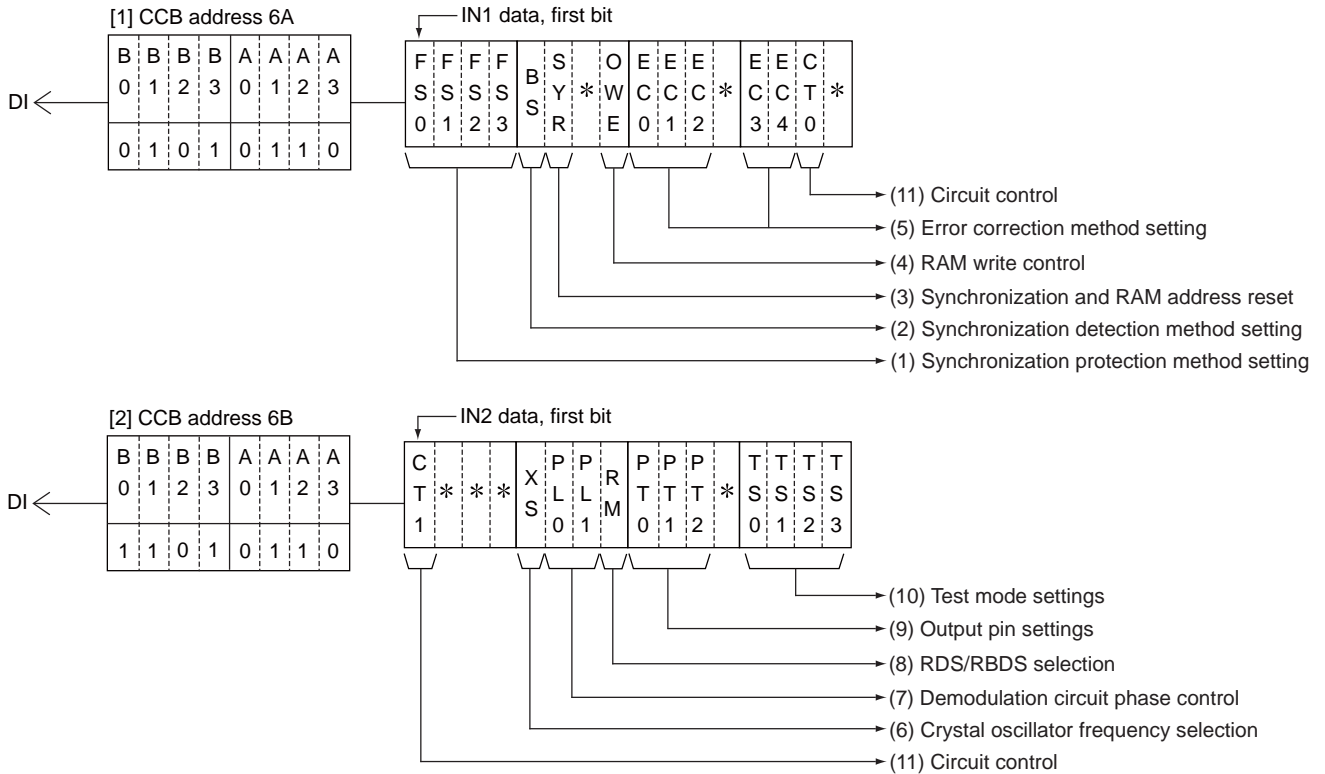
Caution : If the number of errors exceeds the value of the EC0 to EC2 setting (see the section on the CCB input format), the error information flags will be set to the "Correction not possible" value.

(8) RDS data (16bits) : D0 to D15

This data is output with the MSB first and the LSB last.

Caution : When error correction was not possible, the input data is output without change.

CCB Input data format



Caution : The bits labeled with an asterisk must be set to 0.

(1) Synchronization protection (forward protection) method setting (4bits) : FS0 to FS3

FS3 = 0 : If offset words in the correct order could not be detected continuously during the number of blocks specified by FS0 to FS2, take that to be a lost synchronization state.

FS3 = 1 : If blocks with uncorrectable errors were received consecutively during the number of blocks specified by FS0 to FS2, take that to be a lost synchronization state.

| F | F | F | Condition for detecting lost synchronization |
|---|---|---|---|
| S | S | S | |
| 0 | 1 | 2 | |
| 0 | 0 | 0 | If 3 consecutive blocks matching the FS3 condition are received. |
| 1 | 0 | 0 | If 4 consecutive blocks matching the FS3 condition are received. |
| 0 | 1 | 0 | If 5 consecutive blocks matching the FS3 condition are received. |
| 1 | 1 | 0 | If 6 consecutive blocks matching the FS3 condition are received. |
| 0 | 0 | 1 | If 8 consecutive blocks matching the FS3 condition are received. |
| 1 | 0 | 1 | If 10 consecutive blocks matching the FS3 condition are received. |
| 0 | 1 | 1 | If 12 consecutive blocks matching the FS3 condition are received. |
| 1 | 1 | 1 | If 16 consecutive blocks matching the FS3 condition are received. |

Initial value : FS0 = 0, FS1 = 1, FS2 = 0, FS3 = 0

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(2) Synchronization detection method setting (1bit) : BS

| BS | Synchronization detection conditions |
|----|--|
| 0 | If during 3 blocks, 2 blocks of offset words were detected in the correct order. |
| 1 | If the offset words were detected in the correct order in 2 consecutive blocks. |

Initial value : BS = 0

(3) Synchronization and RAM address reset (1bit) : SYR

| SYR | Synchronization detection circuit | RAM |
|-----|--|--|
| 0 | Normal operation (reset cleared) | Normal write (See the description of the OWE bit) |
| 1 | Forced to the unsynchronized state (synchronization reset) | After the reset is cleared, start writing from the data prior to the establishment of synchronization, i.e. the data in backward protection. |

Initial value : SYR = 0

- Caution :
1. To apply a synchronization reset, set SYR to 1 temporarily using CCB, and then set it back to 0 again using CCB. The circuit will start synchronization capture operation at the point SYR is set to 0.
 2. The SYR pin (pin30) also provides an identical reset control operation. Applications can use either method. However, the control method that is not used must be set to 0 at all times. Any pulse with a width of over 250 ns will suffice.
 3. A reset must be applied immediately after the reception channel is changed. If a reset is not applied, reception data from the previous channel may remain in on-chip memory.
 4. Data read out after a synchronization reset is read out starting with the backward protection block data preceding the establishment of synchronization.

(4) RAM write control (1bit) : OWE

| OWE | RAM write conditions |
|-----|--|
| 0 | Only data for which synchronization had been established is written. |
| 1 | Data for which synchronization not has been established (unsynchronized data) is also written. (However, this applies when SYR = 0.) |

Initial value : OWE = 0

(5) Error correction method setting (5bits) : EC0 to EC4

| E C 0 | E C 1 | E C 2 | Number of bits corrected |
|-------------|-------------|-------------|--------------------------|
| 0 | 0 | 0 | 0 (error detection only) |
| 1 | 0 | 0 | 1 or fewer bits |
| 0 | 1 | 0 | 2 or fewer bits |
| 1 | 1 | 0 | 3 or fewer bits |
| 0 | 0 | 1 | 4 or fewer bits |
| 1 | 0 | 1 | 5 or fewer bits |
| 0 | 1 | 1 | Illegal value |
| 1 | 1 | 1 | Illegal value |

| E C 3 | E C 4 | Soft-decision setting |
|-------------|-------------|-----------------------|
| 0 | 0 | MODE0 Hard decision |
| 1 | 0 | MODE1 Soft decision A |
| 0 | 1 | MODE2 Soft decision B |
| 1 | 1 | Illegal value |

Initial values : EC0 = 0, EC1 = 1, EC2 = 0, EC3 = 0, EC4 = 1

- Caution :
1. If soft-decision A or soft-decision B is specified, soft-decision control will be performed even if the number of bits corrected is set to 0 (error detection only). With these settings, data will be output for blocks with no errors.
 2. As opposed to soft-decision B, the soft-decision A setting suppresses soft decision error correction.

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(6) Crystal oscillator frequency selection (1bit) : XS

XS = 0 : 4.332MHz (Initial value : XS = 0)
 XS = 1 : 8.664MHz

(7) Demodulation circuit phase control (2bits) : PL0, PL1

| PL0 | PL1 | Demodulation circuit phase control |
|-----|-----|---|
| 0 | 0/1 | < Normal operation > when ARI presence or absence is unclear. |
| 1 | 0 | If the circuit determines that the ARI signal is absent : 90° phase |
| | 1 | If the circuit determines that the ARI signal is present : 0° phase |

Initial values : PL0 = 0, PL1 = 1

Caution : 1. When PL0 is 0 (normal operation), the IC detects the presence or absence of the ARI signal and reproduces the RDS data by automatically controlling the demodulation phase with respect to the reproduced carrier. However, the initial phase following a synchronization reset is set by PL1.

2. If PL0 is set to 1, the demodulation circuit phase is locked according to the PL1 setting at either 90° (PL1 = 0) or 0° (PL1 = 1), allowing RDS data to be reproduced. When ARI is not present, PL1 should be set to 0, since the RDS data is reproduced by detecting at a phase of 90° with respect to the reproduced carrier. When ARI is present, PL1 should be set to 1, since detection is at 0°. In cases where the ARI presence is known in advance, more stable reproduction can be achieved by fixing the demodulation phase in this manner.

(8) RDS/RBDS(MMBS) selection (1bit) : RM

| RM | RBDS | Decoding method |
|----|----------|--|
| 0 | None | Only RDS data is decoded correctly (Offset word E is not detected.) |
| 1 | Provided | RDS and MMBS data is decoded correctly (Offset word E is also detected.) |

Initial value : RM=0

(9) Output pin settings (3bits) : PT0 to PT2

These bits control the T3, T4, T5, T6, T7, SYNC, and RDS-ID pins

| MODE | P | P | P | T3 | T4 | T5 | T6 | | | T7 | | |
|------|---|---|---|------|------|------|-------|-----|-----|--------|--------|-----|
| | T | T | T | | | | ERROR | 57K | BE1 | CORREC | ARI-ID | BE0 |
| | 0 | 1 | 2 | RDCL | RDDA | RSFT | | | | | | |
| 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — |
| 1 | 1 | 0 | 0 | ○ | ○ | ○ | — | — | — | — | — | — |
| 2 | 0 | 1 | 0 | ○ | ○ | ○ | — | ○ | — | — | ○ | — |
| 3 | 1 | 1 | 0 | ○ | ○ | ○ | ○ | — | — | ○ | — | — |
| 4 | 0 | 0 | 1 | — | — | — | — | — | ○ | — | — | ○ |
| 5 | 1 | 0 | 1 | ● | ○ | ○ | — | — | — | — | — | — |
| 6 | 0 | 1 | 1 | ● | ○ | ○ | — | ● | — | — | ● | — |
| 7 | 1 | 1 | 1 | ● | ○ | ○ | ● | — | — | ● | — | — |

— : open, ○, ● : Output enabled (● = reverse polarity)

Initial value : PT0 = 1, PT1 = 1, PT2 = 0 (Mode 3)

Caution : 1. When PT2 is set to 1, the polarity of the T3(RDCL), T6(ERROR/57K), T7(CORREC/ARI-ID), SYNC, and RDS-ID pins changes to active high.

2. The output pins (T3 to T7, SYNC, and RDS-ID) are all open-drain pins, and require external pull-up resistors to output data.

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| Item | Pin T3 (RDCL) |
|---------|--|
| PT2 = 0 | Data(RDDA and RSFT) changes on this pin's rising edge |
| PT2 = 1 | Data(RDDA and RSFT) changes on this pin's falling edge |

| Mode2 (PT2 = 0) | Pin T7 (ARI-ID) |
|-----------------|-----------------|
| No SK | High (1) |
| SK present | Low (0) |

| Mode3 (PT2 = 0) | Pin T6 (ERROR) | Pin T7 (CORREC) |
|-------------------------|----------------|-----------------|
| Correction not possible | Low (0) | Low (0) |
| Errors corrected | High (1) | Low (0) |
| No errors | High (1) | High (1) |

| Mode = 4 | Pin T6 (BE1) | Pin T7 (BE0) |
|----------------------------|--------------|--------------|
| Number of error blocks (B) | | |
| B=0 | Low (0) | Low (0) |
| $1 \leq B \leq 20$ | Low (0) | High (1) |
| $20 < B \leq 40$ | High (1) | Low (0) |
| $40 < B \leq 48$ | High (1) | High (1) |

These pins indicate the number of blocks in a set of 48 blocks that had errors before correction. The output polarity of these pins is fixed at the values listed in the table.

| Mode (PT2 = 0) | The SYNC pin |
|----------------|---|
| 0 to 2 | When synchronized : Low (0), When unsynchronized: High (1) |
| 3 | When synchronized : Goes high for a fixed period (421 μ s) at the start of a block and then goes low. When unsynchronized : High (1) |

Caution : The output indicates the synchronization state for the previous block.

| When PT2 = 0 | The RDS-ID pin |
|--------------|----------------|
| No RDS | High (1) |
| RDS present | Low (0) |

- (10) Test mode settings (4bits) : TS0 to TS3
Initial values : TS0 = 0, TS1 = 0, TS2 = 0, TS3 = 0
(Applications must set these bits to the above values.)

Notes : The T1 and T2 pins (pins 9 and 10) are related to test mode as follows.

| Pin T1 | Pin T2 | IC operation | Notes |
|--------|--------|---|--------------------------------|
| 0 | 0 | Normal operating mode | These states are user settable |
| 0 | 1 | Standby mode (crystal oscillator stopped) | |
| 1 | 0/1 | IC test mode | Users cannot use this state |

The T1 pin must be tied to V_{SS} (0V).

- (11) Circuit control (2 bits) : CT0 and CT1

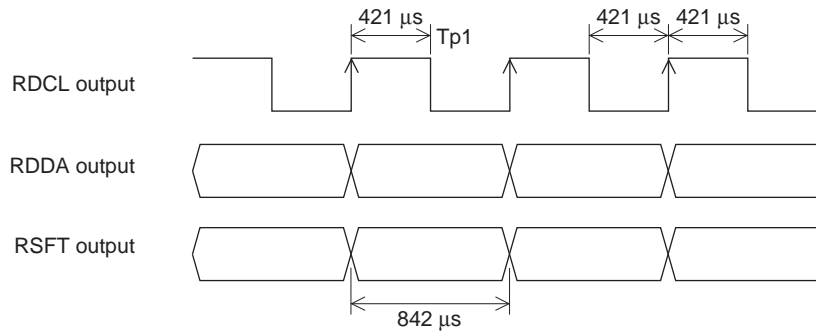
| | Item | Control |
|-----|----------------------------|---|
| CT0 | RSFT control | When set to 1, soft-decision control data (RSFT) is easier to generate. |
| CT1 | RDS-ID detection condition | When set to 1, the RDS-ID detection conditions are made more restrictive. |

Initial value : CT0 = 0, CT1 = 0

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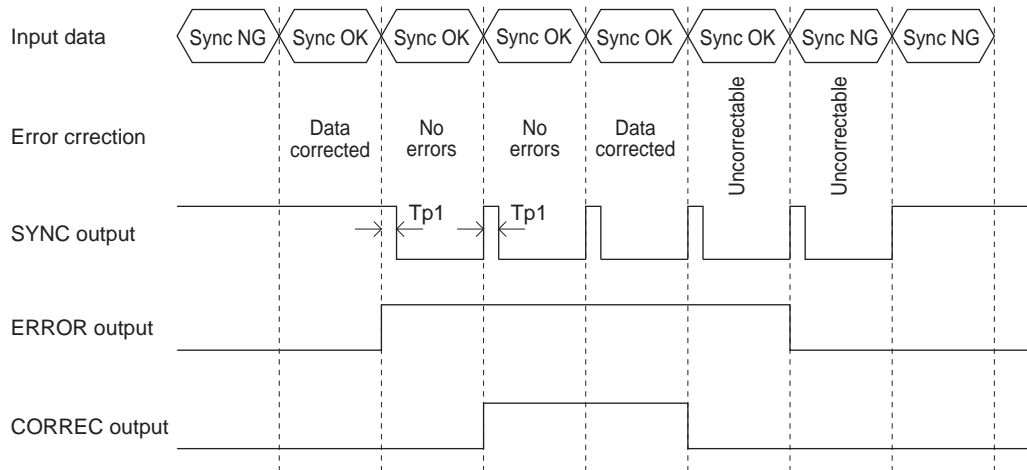
RDCL / RDDA / RSFT and ERROR / CORREC / SYNC output timing

(1) Timing 1



Note : When $PT2 = 0$, RDDA and RSFT must be acquired on the falling edge of RDCL.

(2) Timing 2 (mode 3, $PT2 = 0$)

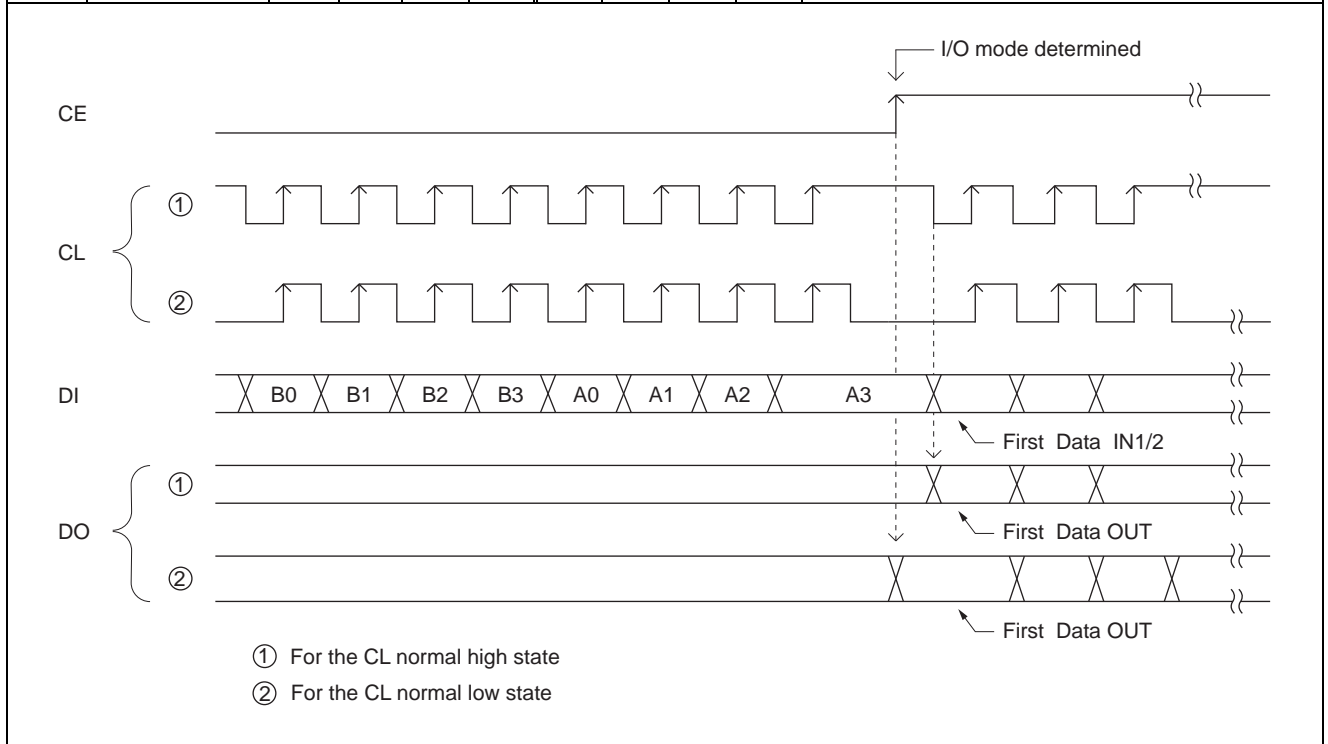


LC72720YVS

Serial Data Input and Output Methods

Data is input and output using the CCB (Computer Control Bus), which is Our audio IC serial bus format. This IC adopts an 8-bit address CCB format.

| | I/O mode | Address | | | | | | | | Comment |
|-----|----------|---------|----|----|----|-------|----|----|----|---|
| | | (LSB) | | | | (MSB) | | | | |
| | | B0 | B1 | B2 | B3 | A0 | A1 | A2 | A3 | |
| [1] | IN1 (6A) | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | <ul style="list-style-type: none"> Control data input mode, also referred to as "serial data input" mode. 16bit data input mode |
| [2] | IN2 (6B) | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | |
| [3] | OUT (6C) | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | <ul style="list-style-type: none"> Data output mode The data for multiple blocks can be output sequentially in this mode. |

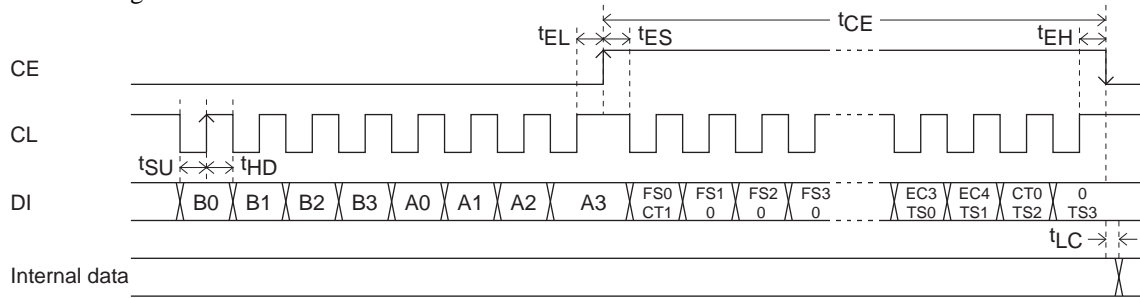


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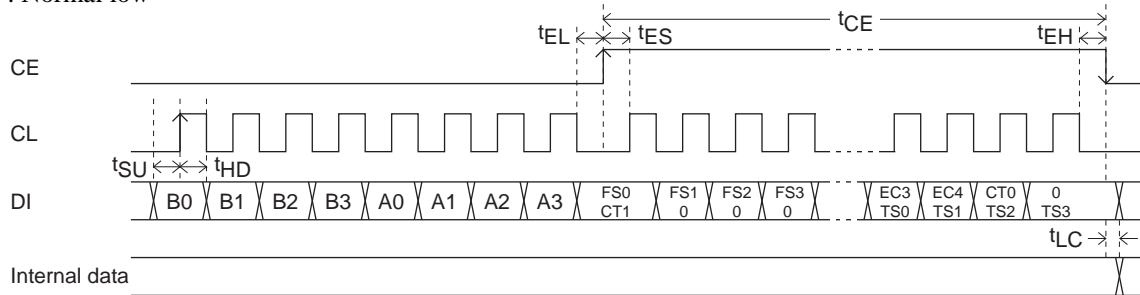
(1) Serial data input (IN1 / IN2)

$t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} \geq 0.75\mu s$ $t_{LC} < 1.15\mu s$ $t_{CE} < 20 ms$

① CL : Normal high



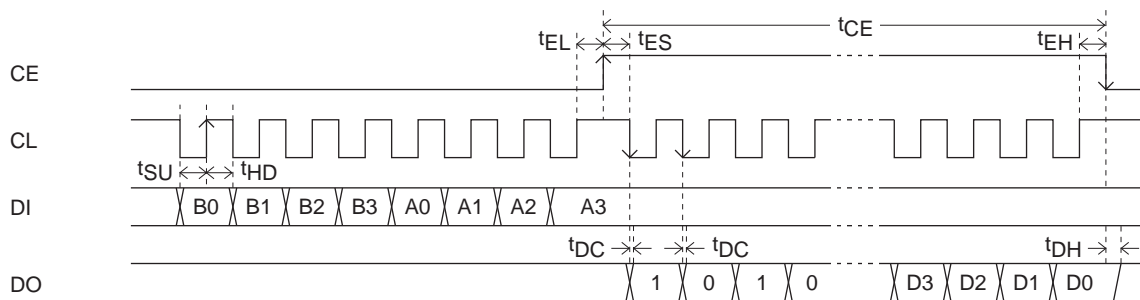
② CL : Normal low



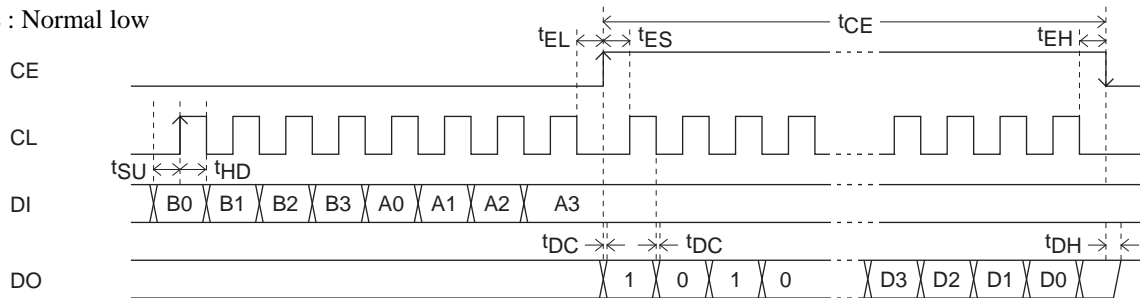
(2) Serial data output (OUT)

$t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} \geq 0.75\mu s$ $t_{DC}, t_{DH} < 0.46\mu s$ $t_{CE} < 20 ms$

① CL : Normal high



② CL : Normal low



Cautions : 1. Since the DO pin is an n-channel open-drain output, the transition times (t_{DC} , t_{DH}) will differ with the value of the pull-up resistor used.

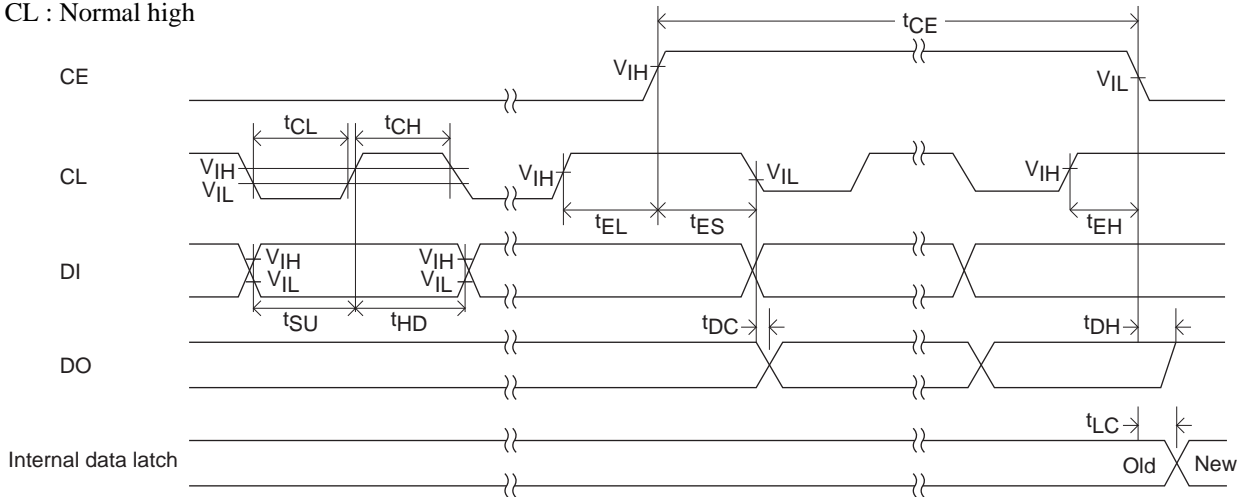
2. The CE, CL, DI, and DO pins can be connected to the corresponding pins on other ICs that use the CCB interface. (However, we recommend connecting the DO and CE pins separately if the number of available microcontroller ports allows it.)

3. Serial data I/O becomes possible after the crystal oscillator starts oscillation.

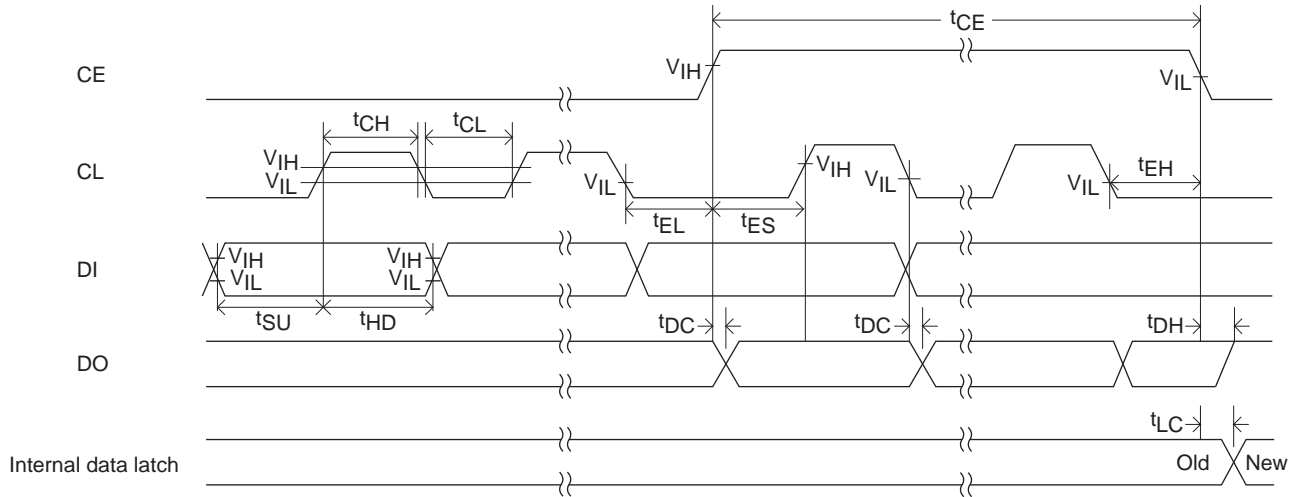
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(3) Serial data timing

① CL : Normal high



② CL : Normal low

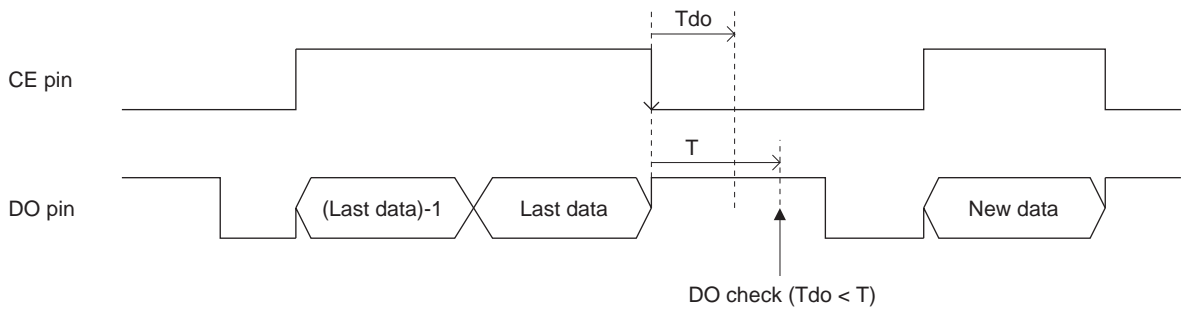


| Parameter | Symbol | Conditions | min | typ | max | Unit |
|----------------------------|----------|------------|------|-----|------|---------------|
| Data setup time | t_{SU} | DI, CL | 0.75 | | | μs |
| Data hold time | t_{HD} | DI, CL | 0.75 | | | μs |
| Clock low level time | t_{CL} | CL | 0.75 | | | μs |
| Clock high level time | t_{CH} | CL | 0.75 | | | μs |
| CE wait time | t_{EL} | CE, CL | 0.75 | | | μs |
| CE setup time | t_{ES} | CE, CL | 0.75 | | | μs |
| CE hold time | t_{EH} | CE, CL | 0.75 | | | μs |
| CE high level time | t_{CE} | CE | | | 20 | ms |
| Data latch transition time | t_{LC} | | | | 1.15 | μs |
| Data output time | t_{DC} | DO, CL | | | 0.46 | μs |
| | t_{DH} | DO, CE | | | 0.46 | μs |

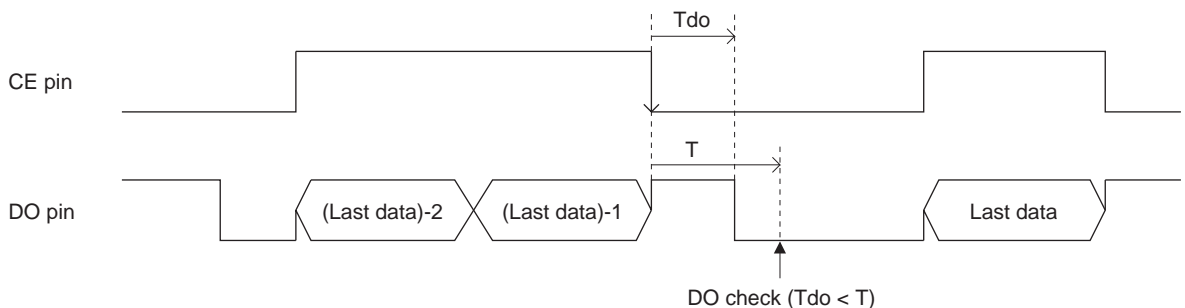
DO pin operation

This IC incorporates a RAM data buffer that can hold up to 24 blocks of data. At the point when one block of data is written to this RAM, the IC issues a read request by switching the DO pin from high to low. The DO pin always goes high for a fixed period ($T_{do} = 265 \mu s$) after a readout and CE goes low. When all the data in the data buffer has been read out, the DO pin is held in the high state until a new block of data has been written to the RAM. If there is data that has not yet been read remaining in the data buffer, the DO pin goes low after the T_{do} time has elapsed. After a synchronization reset, the DO pin is held high until synchronization is established. It goes low at the point the IC synchronizes.

- ① When the DO pin is high following the 265 μs period (T_{do}) after data is read out. Here, the buffer is in the empty state, i.e. the state where new data has not been written. After this, when the DO pin goes low, applications are guaranteed to be able to read out that data without it being overwritten by new data if they start a readout operation within 480 ms of DO going low.



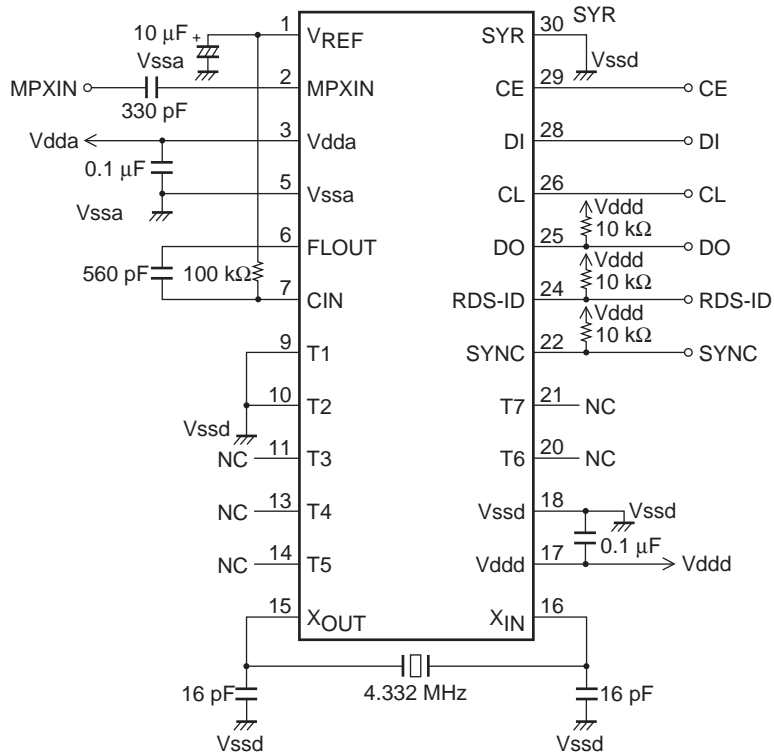
- ② When DO goes low 265 μs after data is read out. Here, there is data that has not been read out remaining in the data buffer. In this case, applications are guaranteed to be able to read out that data without it being overwritten by new data if they start a readout operation within 20 ms of DO going low. (Note that this is the worst case condition.)



- Notes :
1. Although an application can determine whether or not there is data remaining in the buffer by checking the DO level with the above timing, checking the RE and RF flags in the serial data is a preferable method.
 2. Applications are not limited to reading out one block of data at a time, but rather can read out multiple blocks of data continuously as described above. When using this method, if an application references the RE and RF flags in the data while reading out data, it can determine the amount of data remaining. However, the length of the period for data readout (the period the CE pin remains high) must be kept under 20 ms.
 3. If the DO pin is shared with other ICs that use the CCB interface, the application must identify which IC issued the readout request. One method is to read out data from the LC72720YVS and either check whether meaningful data has been read (if the LC72720YVS is not requesting a read, data consisting of all zeros will be read out) or check whether the DO level goes low within the 256 μs following the completion of the read (if the DO pin goes low, then the request was from another IC).

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Sample Application circuit





- Caution :
1. Determine the value of the DO pin pull-up resistor based on the required serial data transfer speed.
 2. A 100-kΩ bias resistor must be connected between the CIN pin and the VREF pin. Note that this resistor is planned to be included internally to the IC in later versions of this product.
 3. If the SYR pin is unused, it must be connected to ground.

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