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LAN9730/LAN9730i

High-Speed Inter-Chip (HSIC) USB 2.0 to 10/100 Ethernet Controller

PRODUCT FEATURES

Data Brief

Highlights

- Single Chip HSIC USB 2.0 to 10/100 Ethernet Controller
- Integrated 10/100 Ethernet MAC with Full-Duplex Support
- Integrated 10/100 Ethernet PHY with HP Auto-MDIX Support
- Integrated USB 2.0 Hi-Speed Device Controller
- Integrated HSIC Interface
- Implements Reduced Power Operating Modes

Target Applications

- Embedded Systems
- Set-Top Boxes
- PVRs
- CE Devices
- Networked Printers
- USB Port Replicators
- Test Instrumentation
- Industrial

Key Features

- USB Device Controller
  - Fully compliant with Hi-Speed Universal Serial Bus Specification, revision 2.0
  - Supports HS (480 Mbps) mode
  - Four Endpoints supported
  - Supports vendor specific commands
  - Integrated HSIC Interface
  - Remote wakeup supported
- High-Performance 10/100 Ethernet Controller
  - Fully compliant with IEEE 802.3/802.3u
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full- and half-duplex support
  - Full- and half-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Loop-back modes
  - TCP/UDP/IP/ICMP checksum offload support
  - Flexible address filtering modes
    - One 48-bit perfect address
    - 64 hash-filtered multicast addresses
    - Pass all multicast
    - Promiscuous mode
    - Inverse filtering
    - Pass all incoming with status report
  - Wakeup packet support
  - Integrated Ethernet PHY
    - Auto-negotiation
    - Automatic polarity detection and correction
    - HP Auto-MDIX support
    - Link status change wake-up detection
  - Support for three status LEDs
  - External MII and Turbo MII support HomePNA® and HomePlug® PHY
- Power and I/Os
  - Various low power modes
  - Supports PCI-like PME wake when USB Host disabled
  - 11 GPIOs
  - Supports bus-powered and self-powered operation
  - Integrated power-on reset circuit
  - Single external 3.3 V I/O supply
    - Optional internal core regulator
- Miscellaneous Features
  - EEPROM controller
  - Supports custom operation without EEPROM
  - IEEE 1149.1 (JTAG) boundary scan
  - Requires single 25 MHz crystal
- Software
  - Windows® 7/XP/Vista driver
  - Linux® driver
  - Win CE driver
  - MAC® OS driver
  - EEPROM utility
- Packaging
  - 56-pin QFN (8x8 mm) lead-free, RoHS compliant
- Environmental
  - Commercial Temperature Range (0°C to +70°C)
  - Industrial Temperature Range (-40°C to +85°C)

PRODUCT PREVIEW

Order Numbers:

LAN9730-ABZJ (Tray) for 56-pin, QFN lead-free RoHS compliant package (0 to +70°C temp)

LAN9730i-ABZJ (Tray) for 56-pin, QFN lead-free RoHS compliant package (-40 to +85°C temp)

LAN9730-ABZJ-TR (Tape & Reel) for 56-pin, QFN lead-free RoHS compliant package (0 to +70°C temp)

LAN9730i-ABZJ-TR (Tape & Reel) for 56-pin, QFN lead-free RoHS compliant package (-40 to +85°C temp)

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000 or 1 (800) 443-SEMI

General Description

The LAN9730/LAN9730i is a high performance solution for USB to 10/100 Ethernet port bridging. With applications ranging from embedded systems, set-top boxes, and PVRs, to USB port replicators, and test instrumentation, the device is targeted as a high-performance, low-cost USB/Ethernet connectivity solution.

The LAN9730/LAN9730i contains an integrated 10/100 Ethernet PHY, HSIC interface, Hi-Speed USB 2.0 device controller, 10/100 Ethernet MAC, TAP controller, EEPROM controller, and a FIFO controller with a total of 30 kB of internal packet buffering.

The internal USB 2.0 device controller is compliant with the USB 2.0 Hi-Speed standard. The HSIC interface is compliant with the High-Speed Interchip USB Electrical Specification Revision 1.0. High-Speed Inter-Chip (HSIC) is a digital interconnect bus that enables the use of USB technology as a low-power chip-to-chip interconnect at speeds up to 480 Mb/s. The device implements Control, Interrupt, Bulk-in and Bulk-out USB Endpoints.

The Ethernet controller supports auto-negotiation, auto-polarity correction, HP Auto-MDIX, and is compliant with the IEEE 802.3 and 802.3u standards. An external MII interface provides support for an external Fast Ethernet PHY, HomePNA, and HomePlug functionality.

Multiple power management features are provided, including various low-power modes, and Magic Packet, Wake On LAN and Link Status Change wake events. These wake events can be programmed to initiate a USB remote wakeup. A PCI-like PME wake is also supported when the Host controller is disabled.

An internal EEPROM controller exists to load various USB configuration information and the device MAC address. The integrated IEEE 1149.1 compliant TAP controller provides boundary scan via JTAG.

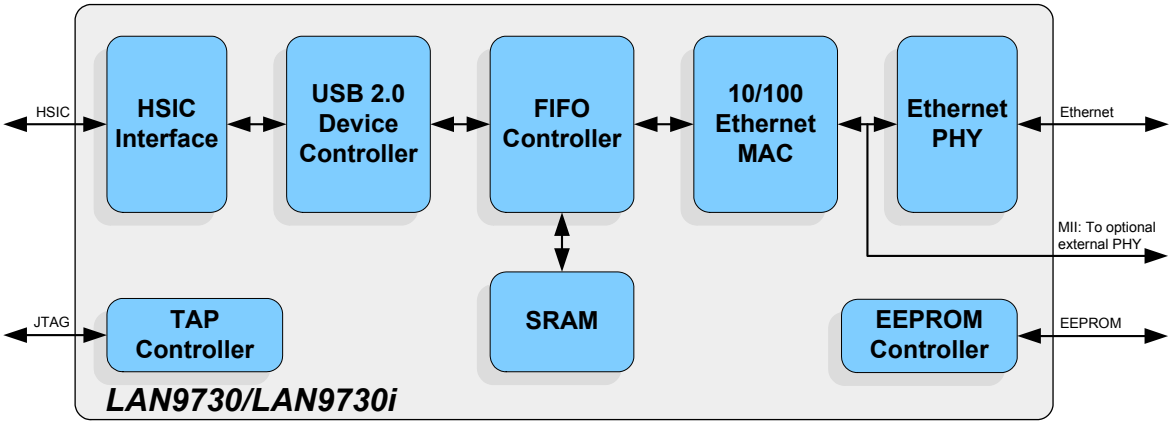


Figure 1 LAN9730/LAN9730i Block Diagram

Package Outline

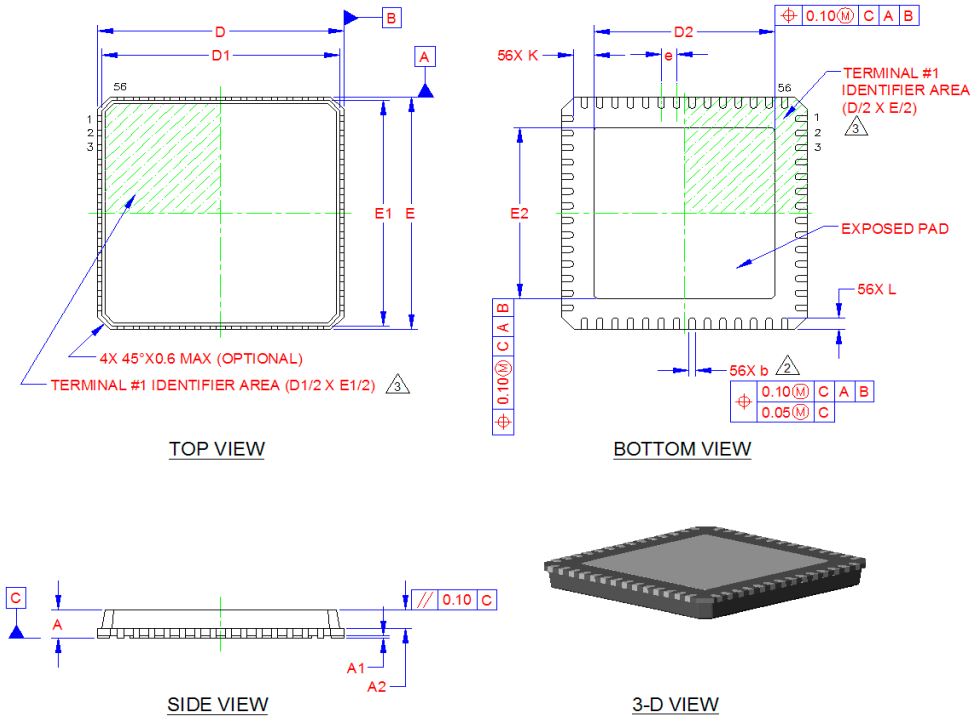


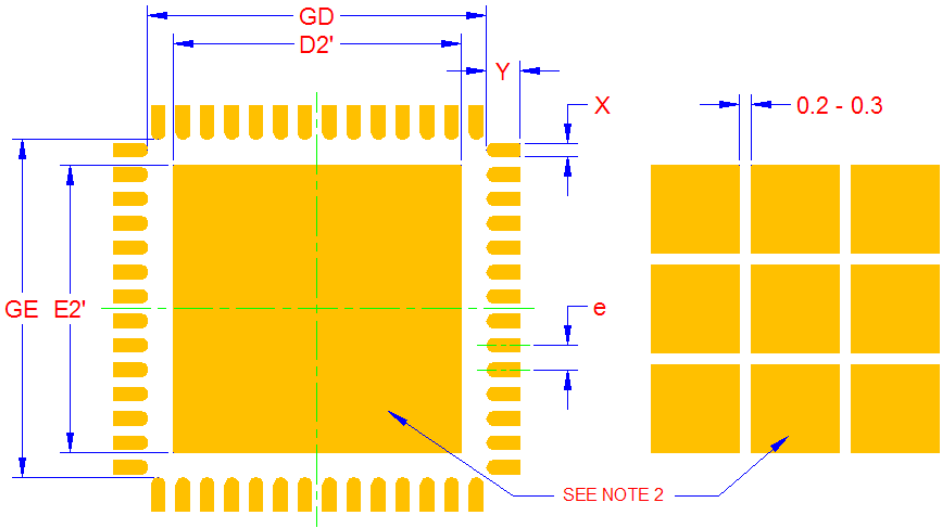
Figure 2 56-Pin QFN Package Definition

Table 1 56-Pin QFN Dimensions

	MIN	NOMINAL	MAX	REMARKS
A	0.70	0.85	1.00	Overall Package Height
A1	0.00	0.02	0.05	Standoff
A2	-	-	0.90	Mold Cap Thickness
D/E	7.85	8.00	8.15	X/Y Body Size
D1/E1	7.55	7.75	7.95	X/Y Mold Cap Size
D2/E2	5.80	5.90	6.00	X/Y Exposed Pad Size
L	0.30	0.40	0.50	Terminal Length
b	0.18	0.25	0.30	Terminal Width
K	0.55	-	-	Center Pad to Pin Clearance
e	0.50 BSC			Terminal Pitch

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Position tolerance of each terminal and exposed pad is +/-0.05 mm at maximum material condition. Dimension “b” applies to plated terminals and is measured between 0.15 and 0.30 mm from the terminal tip.
3. The pin 1 identifier may vary, but is always located within the zone indicated.



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	6.93	-	7.05
D2'/E2'	-	5.90	5.90
X	-	0.28	0.28
Y	-	0.69	0.69
e		0.50	

NOTES:
1. THE USER MAY MODIFY THE PCB LAND PATTERN DESIGN AND DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY
2. EXPOSED SOLDERABLE COPPER AREA OF THE CENTER PAD CAN BE EITHER SOLID OR SEGMENTED
3. MAXIMUM THERMAL AND ELECTRICAL PACKAGE PERFORMANCE IS ACHIEVED WHEN AN ARRAY OF SOLID VIAS IS INCORPORATED IN THE CENTER LAND PATTERN

PCB LAND PATTERN

Figure 3 56-QFN Recommended PCB Land Pattern

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