

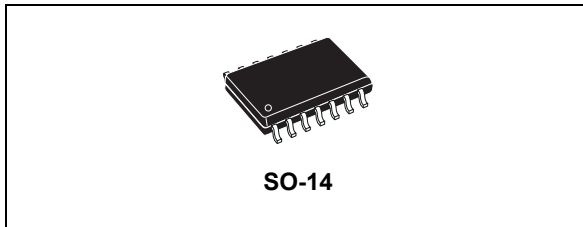


# THE DATASHEET OF L6386ADTR



## High voltage high and low-side driver

Datasheet - production data



### Description

The L6386AD is a high voltage gate driver, manufactured with the BCD™ “offline” technology, and able to drive simultaneously one high and one low-side power MOSFET or IGBT device. The high-side (floating) section is able to work with voltage rail up to 600 V. Both device outputs can independently sink and source 650 mA and 400 mA respectively and can be simultaneously driven high in order to drive asymmetrical half-bridge configurations.

The L6386AD device provides two input pins, two output pins and an enable pin (SD), and guarantees the outputs switch in phase with inputs. The logic inputs are CMOS/TTL compatible to ease the interfacing with controlling devices.

The L6386AD integrates a comparator (inverting input internally referenced to 0.5 V) that can be used to protect the device against fault events, like overcurrent. The DIAG output is a diagnostic pin, driven by the comparator, and used to signal a fault event occurrence to the controlling device.

The bootstrap diode is integrated in the driver allowing a more compact and reliable solution.

The L6386AD device features the UVLO protection on both supply voltages ( $V_{CC}$  and  $V_{BOOT}$ ) ensuring greater protection against voltage drops on the supply lines.

The device is available in a SO-14 package, in tube, and tape and reel packaging.

### Features

- High voltage rail up to 600 V
- $dV/dt$  immunity  $\pm 50$  V/nsec in full temperature range
- Driver current capability
  - 400 mA source
  - 650 mA sink
- Switching times 50/30 nsec rise/fall with 1 nF load
- CMOS/TTL Schmitt trigger inputs with hysteresis and pull-down
- Undervoltage lockout on lower and upper driving section
- Integrated bootstrap diode
- Outputs in phase with inputs

### Applications

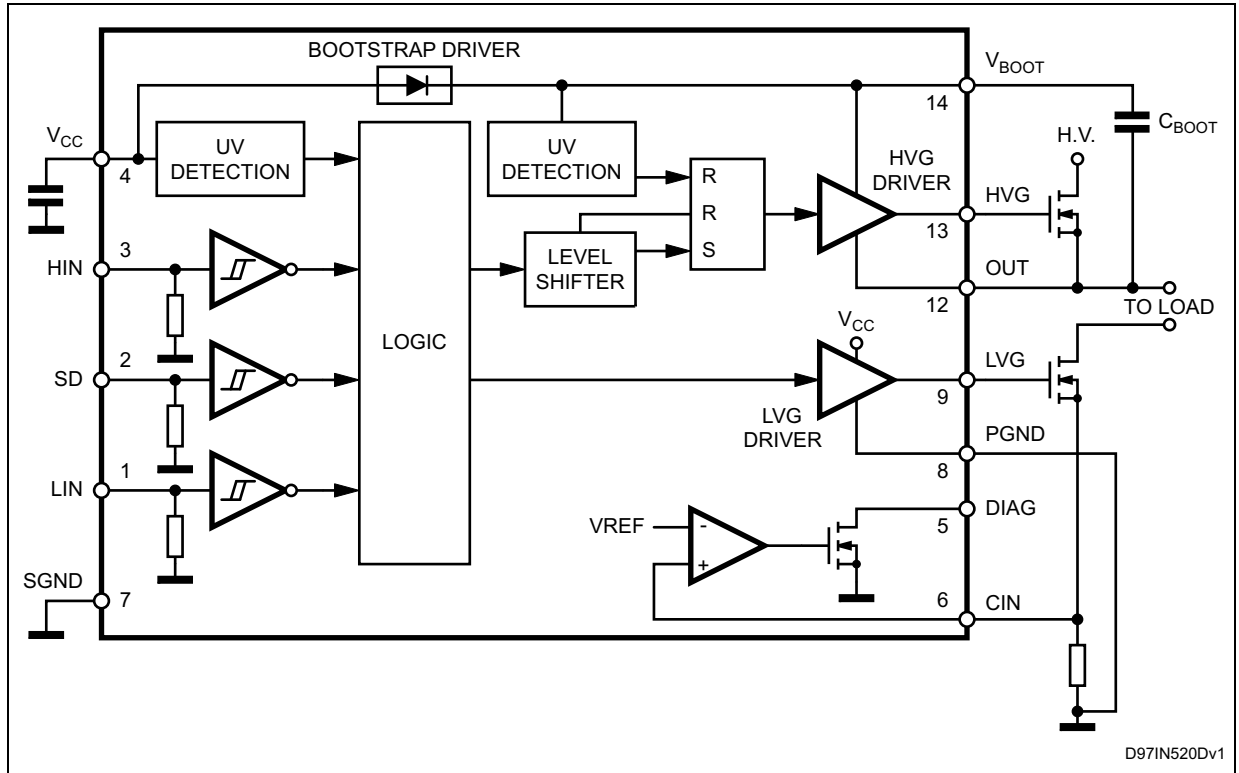
- Home appliances
- Induction heating
- Industrial applications and drives
- Motor drivers
  - SR motors,
  - DC, AC, PMDC and PMAC motors
- Asymmetrical half-bridge topologies
- HVAC
- Lighting applications
- Factory automation
- Power supply systems

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# 1 Block diagram

Figure 1. Block diagram



## 2 Electrical data

### 2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>OUT</sub>	Output voltage	-3 to V <sub>BOOT</sub> - 18	V
V <sub>CC</sub>	Supply voltage	- 0.3 to +18	V
V <sub>BOOT</sub>	Floating supply voltage	-1 to 618	V
V <sub>hvg</sub>	High-side gate output voltage	- 1 to V <sub>BOOT</sub>	V
V <sub>lvg</sub>	Low-side gate output voltage	-0.3 to V <sub>CC</sub> +0.3	V
V <sub>i</sub>	Logic input voltage	-0.3 to V <sub>CC</sub> +0.3	V
V <sub>DIAG</sub>	Open drain forced voltage	-0.3 to V <sub>CC</sub> +0.3	V
V <sub>CIN</sub>	Comparator input voltage	-0.3 to 10 V	V
dV <sub>out</sub> /dt	Allowed output slew rate	50	V/ns
P <sub>tot</sub>	Total power dissipation (T <sub>J</sub> = 85 °C)	750	mW
T <sub>j</sub>	Junction temperature	150	°C
T <sub>stg</sub>	Storage temperature	-50 to 150	°C

### 2.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	SO-14	Unit
R <sub>th(JA)</sub>	Thermal resistance junction to ambient	165	°C/W

### 2.3 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
V <sub>OUT</sub>	12	Output voltage		(1)		580	V
V <sub>BS</sub> <sup>(2)</sup>	14	Floating supply voltage		(1)		17	V
f <sub>sw</sub>		Switching frequency	HVG, LVG load C <sub>L</sub> = 1 nF			400	kHz
V <sub>CC</sub>	4	Supply voltage				17	V
T <sub>J</sub>		Junction temperature		-45		125	°C

1. If the condition V<sub>BOOT</sub> - V<sub>OUT</sub> < 18 V is guaranteed, V<sub>OUT</sub> can range from -3 to 580 V.

2. V<sub>BS</sub> = V<sub>BOOT</sub> - V<sub>OUT</sub>.

## 2.4 Pin connection

Figure 2. Pin connection (top view)

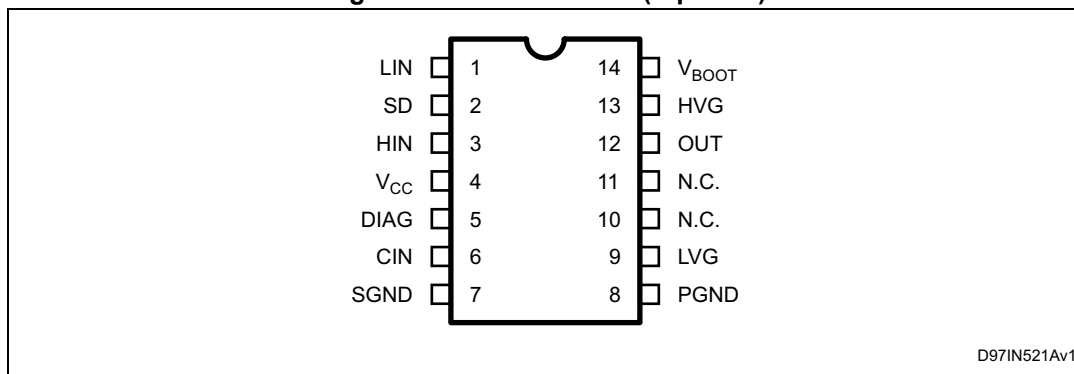


Table 4. Pin description

No.	Pin	Type	Function
1	LIN	I	Low-side driver logic input
2	SD <sup>(1)</sup>	I	Shutdown logic input
3	HIN	I	High-side driver logic input
4	V <sub>CC</sub>	P	Low voltage supply
5	DIAG	O	Open drain diagnostic output
6	CIN	I	Comparator input
7	SGND	P	Ground
8	PGND	P	Power ground
9	LVG <sup>(1)</sup>	O	Low-side driver output
10, 11	N.C.		Not connected
12	OUT	P	High-side driver floating driver
13	HVG <sup>(1)</sup>	O	High-side driver output
14	V <sub>BOOT</sub>	P	Bootstrapped supply voltage

1. The circuit guarantees 0.3 V maximum on the pin (at  $I_{\text{sink}} = 10 \text{ mA}$ ), with  $V_{\text{CC}} > 3 \text{ V}$ . This allows to omit the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver assures low impedance also in SD condition.

### 3 Electrical characteristics

#### 3.1 AC operation

Table 5. AC operation electrical characteristics ( $V_{CC} = 15\text{ V}$ ;  $T_J = 25\text{ }^\circ\text{C}$ )

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{on}$	1, 3 vs. 9, 13	High/low-side driver turn-on propagation delay	$V_{OUT} = 0\text{ V}$		110	150	ns
$t_{off}$		High/low-side driver turn-off propagation delay			110	150	ns
$t_{sd}$	2 vs. 9, 13	Shutdown to high/low-side propagation delay			105	150	
$t_r$	9, 13	Rise time	$C_L = 1000\text{ pF}$		50		ns
$t_f$		Fall time	$C_L = 1000\text{ pF}$		30		ns

#### 3.2 DC operation

Table 6. DC operation electrical characteristics ( $V_{CC} = 15\text{ V}$ ;  $T_J = 25\text{ }^\circ\text{C}$ )

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Low supply voltage section</b>							
$V_{CCth1}$	4	$V_{CC}$ UV turn-on threshold		9.1	9.6	10.1	V
$V_{CCth2}$		$V_{CC}$ UV turn-off threshold		7.9	8.3	8.8	V
$V_{CCchys}$		$V_{CC}$ UV hysteresis			1.3		V
$I_{QCCU}$		Undervoltage quiescent supply current	$V_{CC} \leq 9\text{ V}$		200		$\mu\text{A}$
$I_{QCC}$		Quiescent current	$V_{CC} = 15\text{ V}$		250	320	$\mu\text{A}$
<b>Bootstrapped supply section</b>							
$V_{BTh1}$	14	$V_{BOOT}$ UV turn-on threshold		8.5	9.5	10.5	V
$V_{BTh2}$		$V_{BOOT}$ UV turn-off threshold		7.2	8.2	9.2	V
$V_{BHys}$		$V_{BOOT}$ UV hysteresis			1.3		V
$I_{QBOOT}$		$V_{BOOT}$ quiescent current	HVG ON			200	$\mu\text{A}$
$I_{LK}$		High voltage leakage current	$V_{hvg} = V_{OUT} = V_{BOOT} = 600\text{ V}$			10	$\mu\text{A}$
$R_{DS(on)}$		Bootstrap driver on-resistance <sup>(1)</sup>	$V_{CC} \geq 12.5\text{ V}$ $V_{IN} = 0\text{ V}$		125		$\Omega$
<b>Driving buffers section</b>							
$I_{so}$	9, 13	High/low-side source short-circuit current	$V_{IN} = V_{ih}$ ( $t_p < 10\text{ }\mu\text{s}$ )	300	400		mA
$I_{si}$	9, 13	High/low-side sink short-circuit current	$V_{IN} = V_{il}$ ( $t_p < 10\text{ }\mu\text{s}$ )	500	650		mA

Table 6. DC operation electrical characteristics (continued) ( $V_{CC} = 15\text{ V}$ ;  $T_J = 25\text{ }^\circ\text{C}$ )

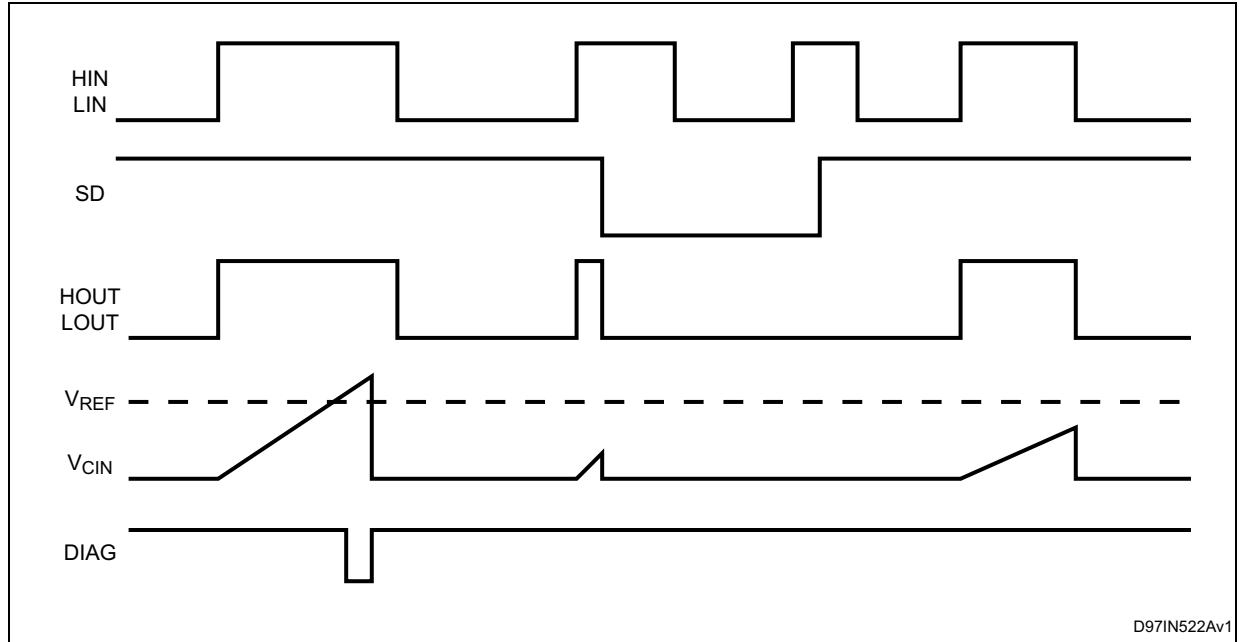
Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
<b>Logic inputs</b>							
$V_{il}$	1, 2, 3	Low level logic voltage				1.5	V
$V_{ih}$		High level logic voltage		3.6			V
$I_{ih}$		High level logic input current	$V_{IN} = 15\text{ V}$		50	70	$\mu\text{A}$
$I_{il}$		Low level logic input current	$V_{IN} = 0\text{ V}$			1	$\mu\text{A}$
<b>Sense comparator</b>							
$V_{io}$		Input offset voltage		-10		10	mV
$I_{io}$	6	Input bias current	$V_{CIN} \geq 0.5$		0.2		$\mu\text{A}$
$V_{ol}$	2	Open drain low level output voltage	$I_{od} = -2.5\text{ mA}$			0.8	V
$V_{ref}$		Comparator reference voltage		0.46	0.50	0.54	V

1.  $R_{DS(on)}$  is tested in the following way:

$$R_{DS(on)} = \frac{(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})}{I_1(V_{CC}, V_{BOOT1}) - I_2(V_{CC}, V_{BOOT2})}$$

where  $I_1$  is the pin 14 current when  $V_{BOOT} = V_{BOOT1}$ ,  $I_2$  when  $V_{BOOT} = V_{BOOT2}$ .

### 3.3 Timing diagram

Figure 3. Input/output timing diagram<sup>(1)</sup>

1. If the SD is set low, each output remains in the shutdown condition also after the rising edge of the SD, until the first rising edge of the input signal occurs.

## 4 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 4 a*). In the L6386AD device a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in *Figure 4 b*. An internal charge pump (*Figure 4 b*) provides the DMOS driving voltage. The diode connected in series to the DMOS has been added to avoid undesirable turn-on.

### C<sub>BOOT</sub> selection and charging

To choose the proper C<sub>BOOT</sub> value, the external MOSFET can be seen as an equivalent capacitor. This capacitor C<sub>EXT</sub> is related to the MOSFET total gate charge:

**Equation 1**

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C<sub>EXT</sub> and C<sub>BOOT</sub> is proportional to the cyclical voltage loss. It has to be:

$$C_{BOOT} \gg \gg C_{EXT}$$

E.g.: if Q<sub>gate</sub> is 30 nC and V<sub>gate</sub> is 10 V, C<sub>EXT</sub> is 3 nF. With C<sub>BOOT</sub> = 100 nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the C<sub>BOOT</sub> selection has to take into account also the leakage losses.

E.g.: HVG steady state consumption is lower than 200 μA, so if HVG T<sub>ON</sub> is 5 ms, C<sub>BOOT</sub> has to supply 1 μC to C<sub>EXT</sub>. This charge on a 1 μF capacitor means a voltage drop of 1 V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has a great leakage current).

This structure can work only if V<sub>OUT</sub> is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T<sub>charge</sub>) of the C<sub>BOOT</sub> is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R<sub>DS(on)</sub> (typical value: 125 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken into account.

The following equation is useful to compute the drop on the bootstrap DMOS:

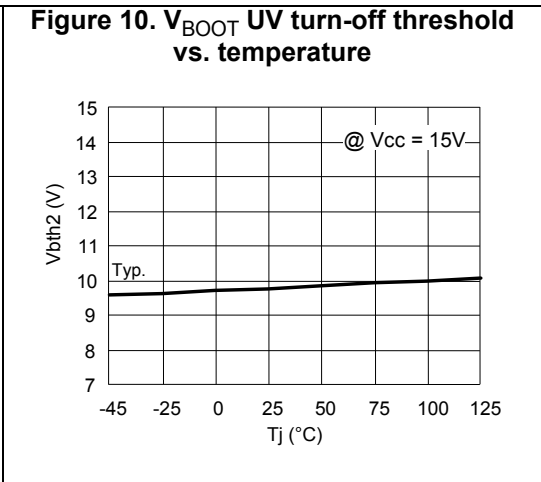
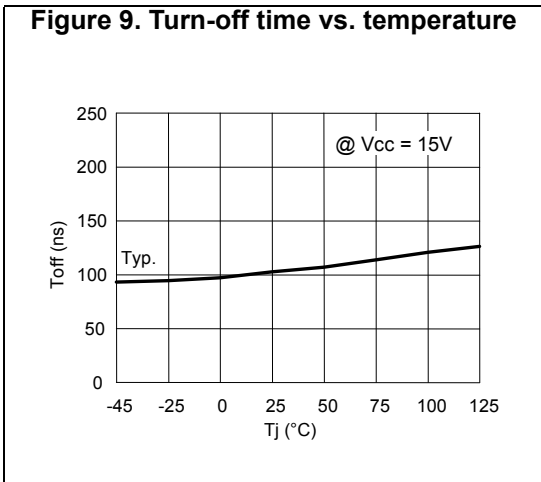
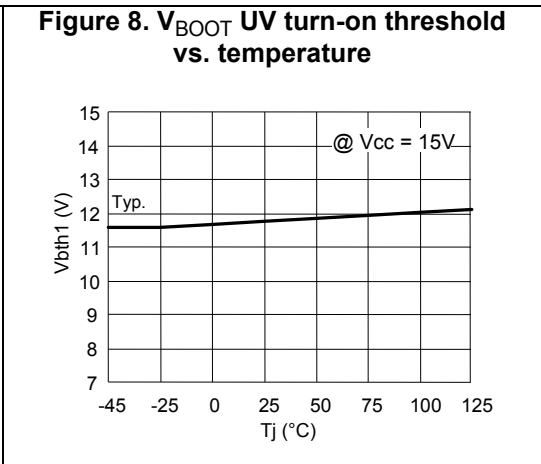
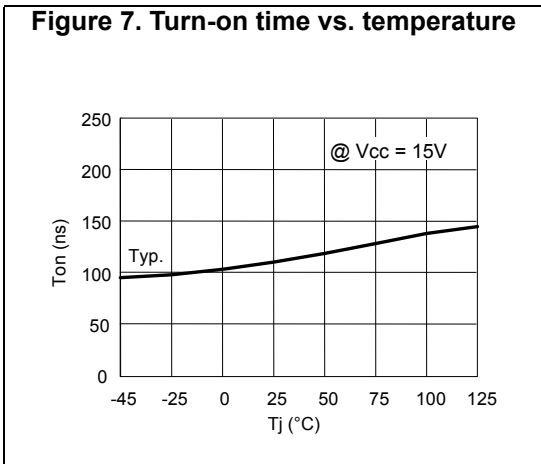
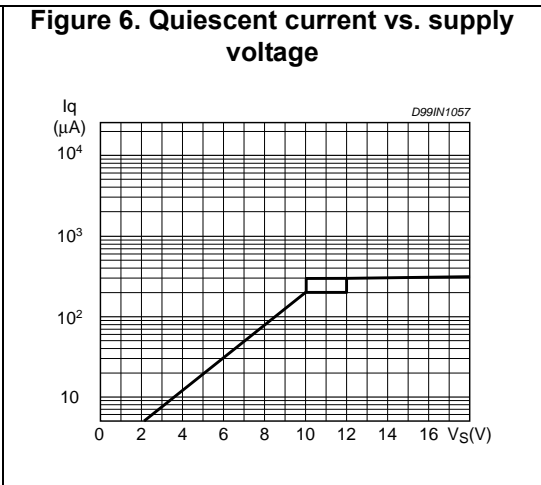
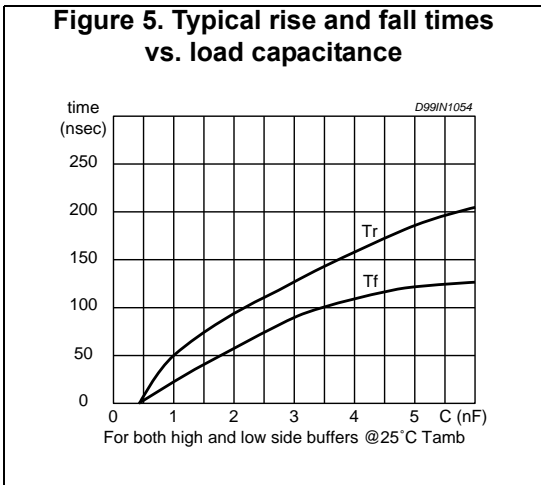
**Equation 2**

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

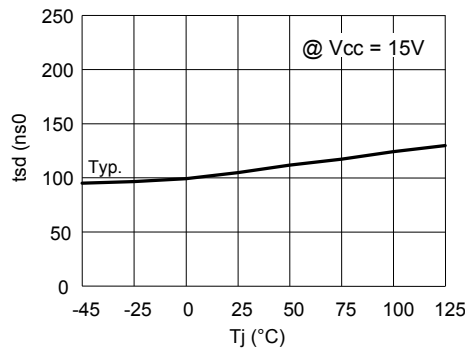
where Q<sub>gate</sub> is the gate charge of the external power MOSFET, R<sub>dson</sub> is the on-resistance of the bootstrap DMOS, and T<sub>charge</sub> is the charging time of the bootstrap capacitor.



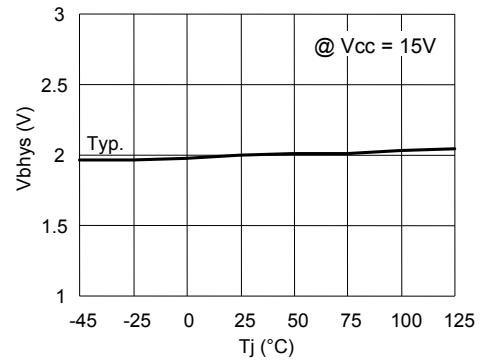
# 5 Typical characteristic



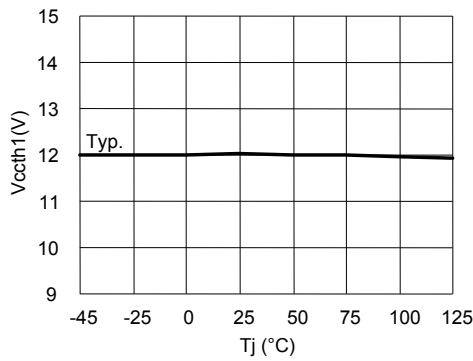
**Figure 11. Shutdown time vs. temperature**



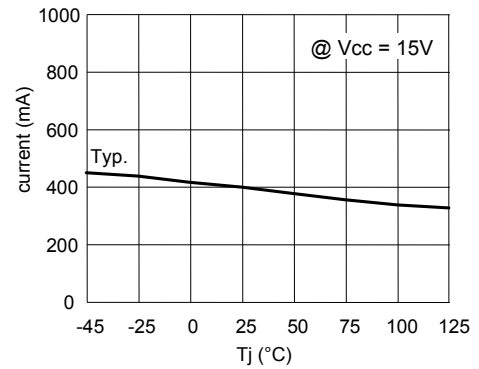
**Figure 12. V<sub>BOOT</sub> UV hysteresis**



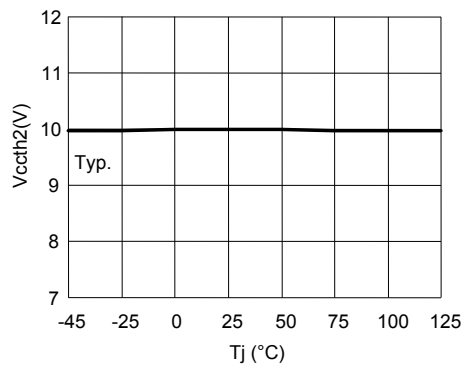
**Figure 13. V<sub>CC</sub> UV turn-on threshold vs. temperature**



**Figure 14. Output source current vs. temperature**



**Figure 15. V<sub>CC</sub> UV turn-off threshold vs. temperature**



**Figure 16. Output sink current vs. temperature**

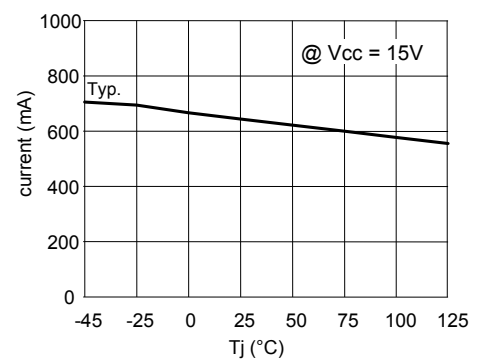
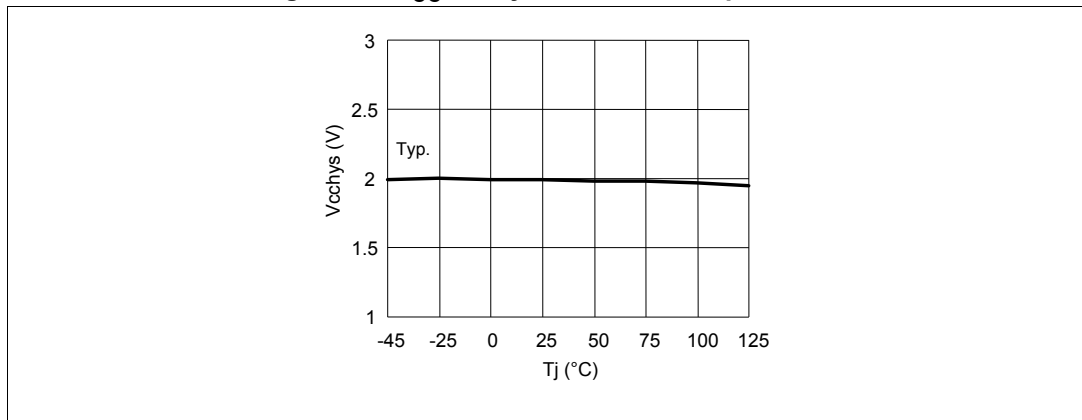


Figure 17.  $V_{CC}$  UV hysteresis vs. temperature



## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 6.1 SO-14 package information

Figure 18. SO-14 package outline

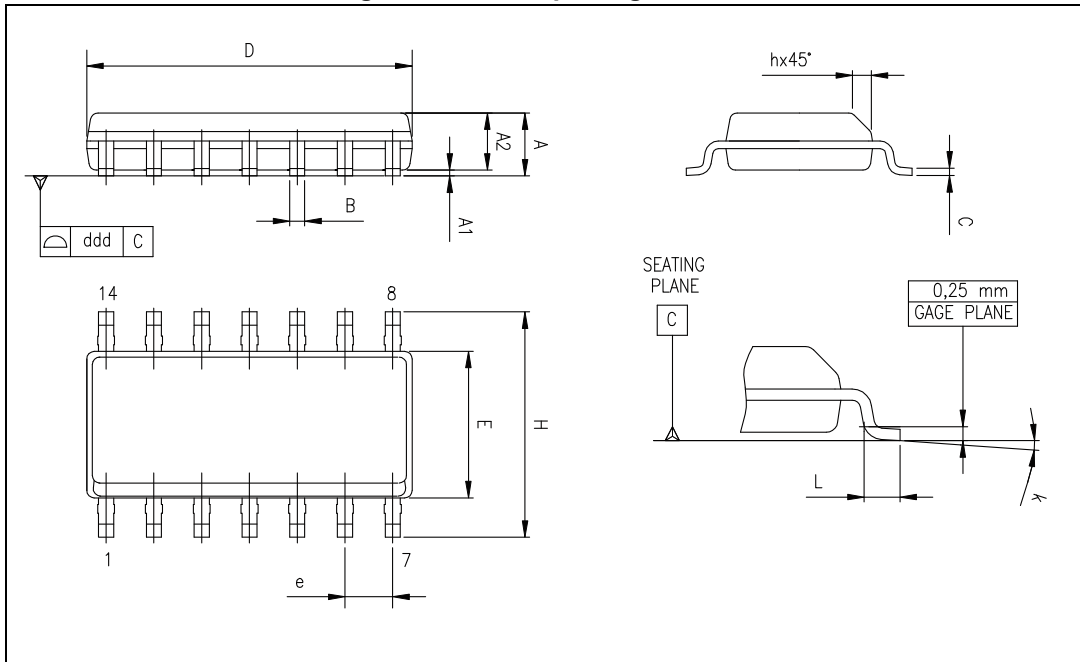


Table 7. SO-14 package mechanical data

Symbol	Dimensions (mm)			Dimensions (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.30	0.004		0.012
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.01
D <sup>(1)</sup>	8.55		8.75	0.337		0.344
E	3.80		4.0	0.150		0.157
e		1.27			0.050	
H	5.8		6.20	0.228		0.244
h	0.25		0.50	0.01		0.02
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. "D" dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

## 7 Order codes

**Table 8. Device summary**

<b>Order codes</b>	<b>Package</b>	<b>Packaging</b>
L6386AD	SO-14	Tube
L6386AD013TR	SO-14	Tape and reel

## 8 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
14-Jul-2008	1	First release
20-Jun-2014	2	<p>Added <a href="#">Section : Applications on page 1</a>.</p> <p>Updated <a href="#">Section : Description on page 1</a> (replaced by new description).</p> <p>Updated <a href="#">Table 1: Device summary on page 1</a> (moved “Table 9 Order codes” from page 15 to page 1, renamed title of <a href="#">Table 1</a>).</p> <p>Updated <a href="#">Figure 1: Block diagram on page 3</a> (moved to page 3, added <a href="#">Section 1: Block diagram on page 3</a>).</p> <p>Updated <a href="#">Section 2.1: Absolute maximum ratings on page 4</a> (removed note below <a href="#">Table 1: Absolute maximum ratings</a>).</p> <p>Updated <a href="#">Table 4: Pin description on page 5</a> (updated “Type” of several pins).</p> <p>Numbered <a href="#">Equation 1 on page 8</a>, <a href="#">Equation 2 on page 8</a> and <a href="#">Equation 3 on page 9</a>.</p> <p>Updated <a href="#">Section 6: Package information on page 13</a> (updated ECOPACK text, updated/added titles, reversed order of <a href="#">Figure 18</a> and <a href="#">Table 7</a> (numbered <a href="#">Table 7</a>), removed 3D package figure, minor modifications].</p> <p>Minor modifications throughout document.</p>
29-Mar-2016	3	<p>Updated <a href="#">Section : Description on page 1</a> (updated text and replaced “power MOS” by “power MOSFET”).</p> <p>Updated <a href="#">Table 1 on page 4</a>, <a href="#">Table 3 on page 4</a>, <a href="#">Table 4 on page 5</a> to <a href="#">Table 6 on page 6</a> (updated “Symbol”, “Parameter”, “Pin”, and “Test condition”, and note 1. below <a href="#">Table 6</a> (replaced “V<sub>BOOTx</sub>” by “V<sub>BOOTx</sub>”).</p> <p>Updated <a href="#">Figure 3 on page 7</a> (replaced by new figure, added note 1.).</p> <p>Moved <a href="#">Table 8 on page 15</a> (moved from page 1 to page 15, added title of <a href="#">Section 7: Order codes on page 15</a>).</p> <p>Minor modifications throughout document.</p>

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