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KSZ8721CLA2TR

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KS8721CL

3.3V Single Power Supply 10/100BASE-TX/FX MII Physical Layer Transceiver

Rev. 1.2

General Description

The KS8721CL is a 10BASE-T, 100BASE-TX, and 100BASE-FX physical layer transceiver providing MII/RMII interfaces to MACs and switches. Using a unique mixed-signal design that extends signaling distance while reducing power consumption, the KS8721CL represents Micrel's fourth generation single-port Fast Ethernet PHY.

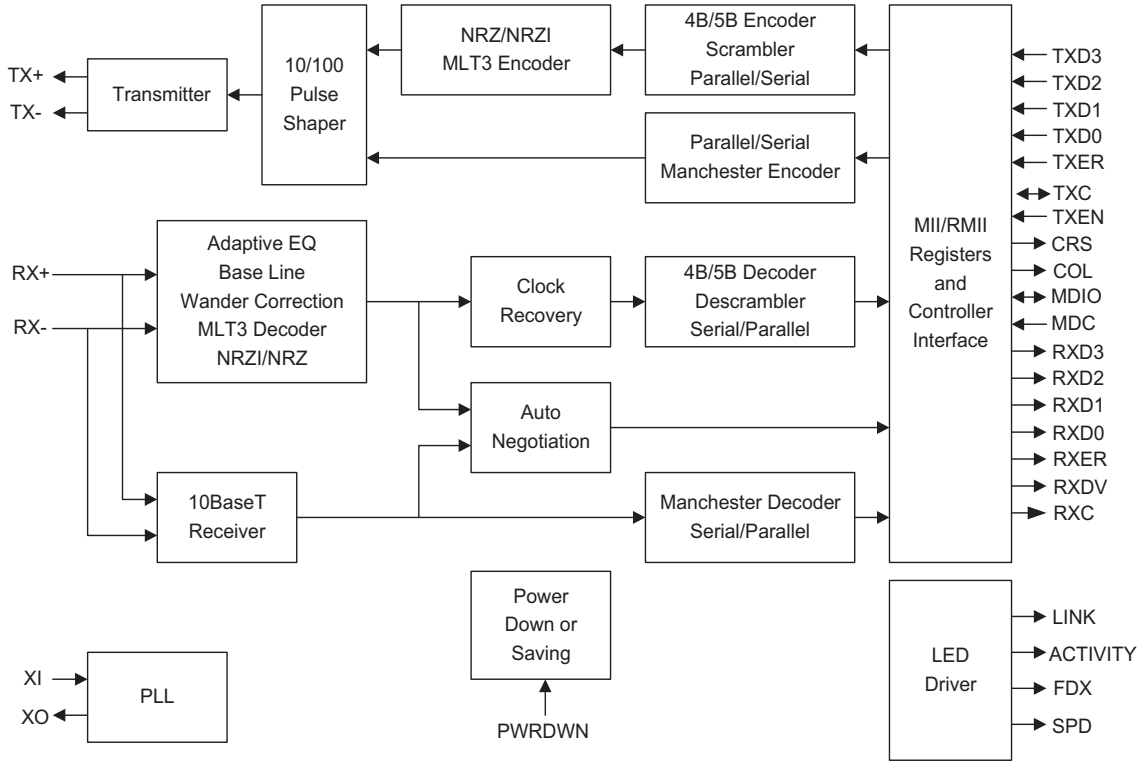
The KS8721CL contains 10BASE-T physical medium attachment (PMA), physical medium dependent (PMD), and physical coding sub-layer (PCS) functions. It also has on-chip 10BASE-T output filtering. This eliminates the need for external filters and allows a single set of line magnetics to be used to meet requirements for both 100BASE-TX and 10BASE-T.

The KS8721CL automatically configures itself for 100Mbps or 10Mbps and full- or half-duplex operation, using an on-chip auto-negotiation algorithm. It is the ideal physical layer transceiver for 100BASE-TX/10BASE-T applications.

Features

- Single chip 100BASE-TX/100BASE-FX/10BASE-T physical layer solution
- 2.5V CMOS design; 2.5/3.3V tolerance on I/O
- 3.3V single power supply with built-in voltage regulator; Power consumption <340mW (including output driver current)
- Fully compliant to IEEE 802.3u standard
- Supports MII and Reduced MII (RMII)
- Supports 10BASE-T, 100BASE-TX, and 100BASE-FX with far-end-fault (FEF) detection
- Supports power-down and power-saving modes
- Configurable through MII serial management ports or via external control pins
- Supports auto-negotiation and manual selection for 10/100Mbps speed and full-/half-duplex modes
- On-chip, built-in, analog front-end filtering for both 100BASE-TX and 10BASE-T
- Available in Lead-free and Industrial Temperature packages.

Functional Diagram



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Features (continued)

- LED outputs for link, activity, full-/half-duplex, and speed
- Supports back-to-back, FX to TX for media converter applications
- Supports MDI/MDI-X auto-crossover
- Commercial temperature range: 0°C to +70°C
- Industrial temperature range: –40°C to +85°C
- Available in 48-pin LQFP

Ordering Information

Part Number	Temp. Range	Package	Lead Finish
KS8721CL	0°C to +70°C	48-Pin LQFP	Standard
KSZ8721CL	0°C to +70°C	48-Pin LQFP	Lead-free

Revision History

Revision	Date	Summary of Changes
0.90	7/20/04	Created.
1.0	10/08/04	Updated series resistance for crystal specification to 40Ω.
1.1	1/27/05	MDIO resistor value changes to 4.7kΩ. Added note on strapping option pins. Updated bits 1b.0 - 1b.7 to self-clearing. Updated Electrical characteristics. Updated reference schematic for strapping option configuration to 3.3V. Updated bits 1f.4-1f.2 to reserved. Added aditional magnetics to qualified transformer table. Added reset reference circuit.
1.2	3/16/05	Added RMII timing. Corrected LED signal references to collision. Removed KS8721CLI from ordering information.

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Pin Description

Pin Number	Pin Name	Type[1]	Pin Function
1	MDIO	I/O	Management Independent Interface (MII) Data I/O. This pin requires an external 4.7K pull-up resistor.
2	MDC	I	MII Clock Input. This pin is synchronous to the MDIO.
3	RXD3/ PHYAD	Ipd/O	MII Receive Data Output. RXD [3..0], these bits are synchronous with RXCLK. When RXDV is asserted, RXD [3..0] presents valid data to MAC through the MII. RXD [3..0] is invalid when RXDV is de-asserted. During reset, the pull-up/pull-down value is latched as PHYADDR [1]. See “Strapping Options” section for details.
4	RXD2/ PHYAD2	Ipd/O	MII Receive Data Output. During reset, the pull-up/pull-down value is latched as PHYADDR[2]. See “Strapping Options” section for details.
5	RXD1/ PHYAD3	Ipd/O	MII Receive Data Output. During reset, the pull-up/pull-down value is latched as PHYADDR [3]. See “Strapping Options” section for details.
6	RXD0/ PHYAD4	Ipd/O	MII Receive Data Output. During reset, the pull-up/pull-down value is latched as PHYADDR [4]. See “Strapping Options” section for details.
7	VDDIO	P	Digital IO 2.5 /3.3V tolerant power supply. 3.3V power Input of voltage regulator. See “Circuit Design Ref. for Power Supply" section for details.
8	GND	GND	Ground.
9	RXDV/ CRSDV/ PCS_LPBK	Ipd/O	MII Receive Data Valid Output. During reset, the pull-up/pull-down value is latched as PCS_LPBK. See “Strapping Options” section for details.
10	RXC	O	MII Receive Clock Output. Operating at 25MHz = 100Mbps, 2.5MHz = 10Mbps.
11	RXER/ISO	Ipd/O	MII Receive Error Output. During reset, the pull-up/pull-down value is latched as ISOLATE during reset. See “Strapping Options” section for details.
12	GND	GND	Ground.
13	VDDC	P	Digital core 2.5V only power supply. See “Circuit Design Ref. for Power Supply" section for details.
14	TXER	Ipd	MII Transmit Error Input.
15	TXC/ REFCLK	I/O	MII Transmit Clock Output. Input for crystal or an external 50MHz clock. When REFCLK pin is used for REF clock interface, pull up XI to VDDPLL 2.5V via 10kΩ resistor and leave XO pin unconnected.
16	TXEN	Ipd	MII Transmit Enable Input.
17	TXD0	Ipd	MII Transmit Data Input.
18	TXD1	Ipd	MII Transmit Data Input.

Notes:

1. P = Power supply.
   GND = Ground.
   I = Input.
   I/O = Bidirectional.
   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu = Input w/ internal pull-up.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   O = Output.

Pin Number	Pin Name	Type[1]	Pin Function
19	TXD2	Ipd	MII Transmit Data Input.
20	TXD3	Ipd	MII Transmit Data Input.
21	COL/RMII	Ipd/O	MII Collision Detect Output. During reset, the pull-up/pull-down value is latched as RMII select. See “Strapping Options” section for details.
22	CRS/ RMII_BTB	Ipd/O	MII Carrier Sense Output. During reset, the pull-up/pull-down value is latched as RMII back-to-back mode when RMII mode is selected. See “Strapping Options” section for details.
23	GND	GND	Ground.
24	VDDIO	P	Digital IO 2.5/3.3V tolerant power supply. 3.3V power input of voltage regulator. See “Circuit Design Ref. for Power Supply” section for details.
25	INT#/ PHYAD0	Ipu/O	Management Interface (MII) Interrupt Out. Interrupt level set by Register 1f, bit 9. During reset, latched as PHYAD[0]. See “Strapping Options” section for details.
26	LED0/TEST PHYAD0	Ipu/O	Link LED Output. The external pull-down enable test mode and only used for the factory test. Active low. **Link** / **Pin State** / **LED Definition** No Link / H / “Off” Link / L / “On”
27	LED1/ SPD100/ nFEF	Ipu/O	Speed LED Output. Latched as SPEED (Register 0, bit 13) during power-up/ reset. See “Strapping Options” section for details. Active low. **Speed** / **Pin State** / **LED Definition** 10BT / H / “Off” 100BT / L / “On”
28	LED2/	Ipu/O	Full-duplex LED Output. Latched as DUPLEX (register 0h, bit 8) during power-up/ reset. See “Strapping DUPLEX Options” section for details. Active low. **Duplex** / **Pin State** / **LED Definition** Half / H / “Off” Full / L / “On”
29	LED3/ NWAYEN	Ipu/O	LED Output. Latched as ANEG_EN (register 0h, bit 12) during power-up/ reset. See “Strapping Options” section for details. **Activity** / **Pin State** / **LED Definition** Activity / – / “Toggle”
30	PD#	Ipu	Power Down. 1 = Normal operation, 0 = Power-down. Active low.

Notes:

1. P = Power supply.
   GND = Ground.
   I = Input.
   I/O = Bidirectional.
   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu = Input w/ internal pull-up.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   O = Output.

Pin Number	Pin Name	Type[1]	Pin Function
31	VDDRX	P	Analog 2.5V power supply. See “Circuit Design Ref. for Power Supply” section for details.
32	RX-	I	Receive Input. Differential receive input pins for 100FX, 100BASE-TX, or 10BASE-T.
33	RX+	I	Receive Input: Differential receive input pin for 100FX, 100BASE-TX, or 10BASE-T.
34	FXSD/FXEN	Ipd/O	Fiber Mode Enable / Signal Detect in Fiber Mode. If FXEN = 0, FX mode is disable. The default is “0”. See “100BT FX Mode” section for more details.
35	GND	GND	Ground.
36	GND	GND	Ground.
37	REXT	I	External resistor (6.49kW) connects to REXT and GND.
38	VDDRCV	P	Analog 2.5V power supply. 2.5V power output of voltage regulator. See “Circuit Design Ref. for Power Supply” section for details.
39	GND	GND	Ground.
40	TX-	O	Transmit Outputs: Differential transmit output for 100FX, 100BASE-TX, or 10BASE-T.
41	TX+	O	Transmit Outputs: Differential transmit output for 100FX, 100BASE-TX, or 10BASE-T.
42	VDDTX	P	Transmitter 2.5V power supply. See “Circuit Design Ref. for Power Supply” section for details.
43	GND	GND	Ground.
44	GND	GND	Ground.
45	XO	O	XTAL feedback: Used with XI for Xtal application.
46	XI	I	Crystal Oscillator Input: Input for a crystal or an external 25MHz clock. If an oscillator is used, XI connects to a 3.3V tolerant oscillator, and X2 is a no-connect.
47	VDDPLL	P	Analog PLL 2.5V power supply. See “Circuit Design Ref. for Power Supply” section for details.
48	RST#	Ipu	Chip Reset. Active low, minimum of 50µs pulse is required.

Notes:

1. P = Power supply.
   GND = Ground.
   I = Input.
   I/O = Bidirectional.
   Ipd = Input w/ internal pull-down.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu = Input w/ internal pull-up.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   O = Output.

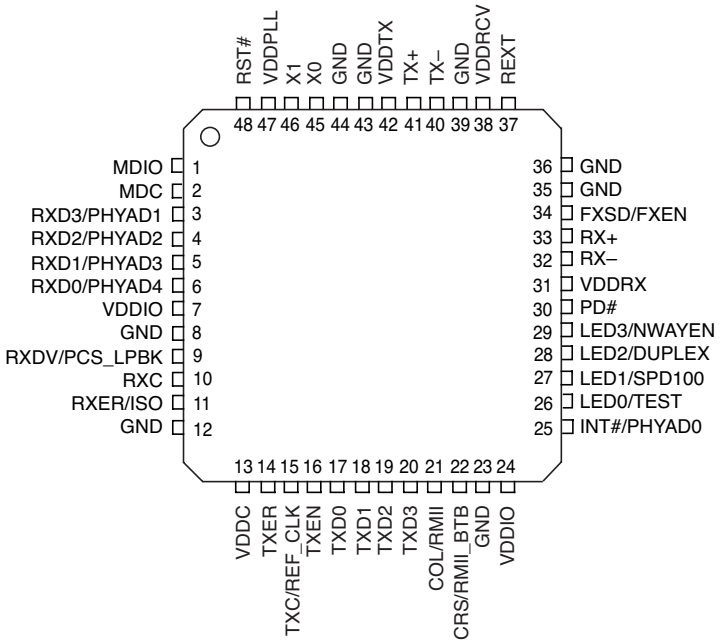
Strapping Options[1]

Pin Number	Pin Name	Type[2]	Description
6,5, 4,3	PHYAD[4:1]/ RXD[0:3]	Ipd/O	PHY Address latched at power-up/reset. The default PHY address is 00001.
25	PHYAD0/ INT#	Ipu/O	
9[3]	PCS_LPBK/ RXDV	Ipd/O	Enables PCS_LPBK mode at power-up/reset. PD (default) = Disable, PU = Enable.
11[3]	ISO/RXER	Ipd/O	Enables ISOLATE mode at power-up/reset. PD (default) = Disable, PU = Enable.
21[3]	RMII/COL	Ipd/O	Enables RMII mode at power-up/reset. PD (default) = Disable, PU = Enable.
22[3]	RMII_BTB CRS	Ipd/O	Enable RMII back-to-back mode at power-up/reset. PD (default) = Disable, PU = Enable.
27	SPD100/ No FEF/ LED1	Ipu/O	Latched into Register 0h bit 13 during power-up/reset. PD = 10Mbps, PU (default) = 100Mbps. If SPD100 is asserted during power-up/reset, this pin is also latched as the Speed Support in register 4h. (If FXEN is pulled up, the latched value 0 means no Far_End _Fault.)
28	DUPLEX/ LED2	Ipu/O	Latched into Register 0h bit 8 during power-up/reset. PD = Half-duplex, PU (default) = Full-duplex. If Duplex is pulled up during reset, this pin is also latched as the Duplex support in register 4h.
29	NWAYEN/ LED3	Ipu/O	Nway (auto-negotiation) Enable. Latched into Register 0h bit 12 during power-up/ reset. PD = Disable Auto-Negotiation, PU (default) = Enable Auto-Negotiation.
30	PD#	Ipu	Power-Down Enable. PU (default) = Normal operation, PD = Power-Down mode.

Notes:

1. Strap-in is latched during power-up or reset.
2. Ipu = Input w/ internal pull-up.
   Ipd/O = Input w/ internal pull-down during reset, output pin otherwise.
   Ipu/O = Input w/ internal pull-up during reset, output pin otherwise.
   See “Reference Circuit” section for pull-up/pull-down and float information.
3. Some devices may drive MII pins that are designated as output (PHY) on power up, resulting in incorrect strapping values latched in at reset. It is recommended that an external pull-down via 1kΩ resistor be used in their applications to augment the 8721's internal pull-down.

Pin Configuration



48-Pin LQFP (LQ)

Introduction

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission. The circuitry starts with a parallel to serial conversion that converts the 25MHz, 4-bit nibbles into a 125MHz serial bit stream. The incoming data is clocked in at the positive edge of the TXC signal. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 6.49kΩ resistor for the 1:1 transformer ratio. Its typical rise/fall time of 4ns complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output driver is also incorporated into the 100BASE-TX driver.

100BASE-TX Receive

The 100BASE-TX receive function performs adaptive equalization, DC restoration, MLT-3 to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion are a function of the length of the cable, the equalizer has to adjust its characteristic to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics. It then tunes itself for optimization. This is an ongoing process and can self-adjust for environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effects of base line wander and improve dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. Finally, the NRZ serial data is converted to 4-bit parallel 4B nibbles. A synchronized 25MHz RXC is generated so that the 4B nibbles are clocked out at the negative edge of RCK25 and is valid for the receiver at the positive edge. When no valid data is present, the clock recovery circuit is locked to the 25MHz reference clock and both TXC and RXC clocks continue to run.

PLL Clock Synthesizer

The KS8721CL generates 125MHz, 25MHz, and 20MHz clocks for system timing. An internal crystal oscillator circuit provides the reference clock for the synthesizer.

Scrambler/De-scrambler (100BASE-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce electromagnetic interference (EMI) and baseline wander.

10BASE-T Transmit

When TXEN (transmit enable) goes high, data encoding and transmission begins. The KS8721CL continues to encode and transmit data as long as TXEN remains high. The data transmission ends when TXEN goes low. The last transition occurs at the boundary of the bit cell if the last bit is zero, or at the center of the bit cell if the last bit is one. The output driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.5V amplitude. The harmonic contents are at least 27dB below the fundamental when driven by an all-ones, Manchester-encoded signal.

10BASE-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300mV or with short pulse widths in order to prevent noise at the RX+ or RX- input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KS8721CL decodes a data frame. This activates the carrier sense (CRS) and RXDV signals and makes the receive data (RXD) available. The receive clock is maintained active during idle periods in between data reception.

SQE and Jabber Function (10BASE-T only)

In 10BASE-T operation, a short pulse is put out on the COL pin after each packet is transmitted. This is required as a test of the 10BASE-T transmit/receive path and is called an SQE test. The 10BASE-T transmitter is disabled and COL goes high if TXEN is high for more than 20ms (Jabbering). If TXEN then goes low for more than 250ms, the 10BASE-T transmitter is re-enabled and COL goes low.

Auto-Negotiation

The KS8721CL performs auto-negotiation by hardware strapping option (pin 29) or software (Register 0.12). It automatically chooses its mode of operation by advertising its abilities and comparing them with those received from its link partner whenever

auto-negotiation is enabled. It can also be configured to advertise 100BASE-TX or 10BASE-T in either full- or half-duplex mode (please refer to “Auto-Negotiation”). Auto-negotiation is disabled in the FX mode.

During auto-negotiation, the contents of Register 4, coded in fast link pulse (FLP), are sent to its link partner under the conditions of power-on, link-loss, or restart. At the same time, the KS8721CL monitors incoming data to determine its mode of operation. The parallel detection circuit is enabled as soon as either 10BASE-T normal link pulse (NLP) or 100BASE-TX idle is detected. The operation mode is configured based on the following priority:

Priority 1: 100BASE-TX, full-duplex

Priority 2: 100BASE-TX, half-duplex

Priority 3: 10BASE-T, full-duplex

Priority 4: 10BASE-T, half-duplex

When the KS8721CL receives a burst of FLP from its link partner with three identical link code words (ignoring acknowledge bit), it will store these code words in Register 5 and wait for the next three identical code words. Once the KS8721CL detects the second code words, it then configures itself according to the above-mentioned priority. In addition, the KS8721CL also checks for 100BASE-TX idle or 10BASE-T NLP symbols. If either is detected, the KS8721CL automatically configures to match the detected operating speed.

MII Management Interface

The KS8721CL supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the KS8721CL. The MDIO interface consists of the following:

- A physical connection including a data line (MDIO), a clock line (MDC), and an optional interrupt line (INTRPT).
- A specific protocol that runs across the above-mentioned physical connection that allows one controller to communicate with multiple KS8721CL devices. Each KS8721CL is assigned an MII address between 0 and 31 by the PHYAD inputs.
- An internal addressable set of fourteen 16-bit MDIO registers. Registers [0:6] are required and their functions are specified by the IEEE 802.3 specifications. Additional registers are provided for expanded functionality.

The INTPRT pin functions as a management data interrupt in the MII. An active Low or High in this pin indicates a status change on the KS8721CL based on 1fh.9 level control. Register bits at 1bh[15:8] are the interrupt enable bits. Register bits at 1bh[7:0] are the interrupt condition bits. This interrupt is cleared by reading Register 1bh.

MII Data Interface

The data interface consists of separate channels for transmitting data from a 10/100 802.3 compliant Media Access Controller (MAC) to the KS8721CL, and for receiving data from the line. Normal data transmission is implemented in 4B nibble mode (4-bit wide nibbles).

Transmit Clock (TXC): The transmit clock is normally generated by the KS8721CL from an external 25MHz reference source at the X1 input. The transmit data and control signals must always be synchronized to the TXC by the MAC. The KS8721CL normally samples these signals on the rising edge of the TXC.

Receive Clock (RXC): For 100BASE-TX links, the receive clock is continuously recovered from the line. If the link goes down, and auto-negotiation is disabled, the receive clock operates off the master input clock (X1 or TXC). For 10BASE-T links, the receive clock is recovered from the line while carrier is active, and operates from the master input clock when the line is idle. The KS8721CL synchronizes the receive data and control signals on the falling edge of RXC in order to stabilize the signals at the rising edge of the clock with 10ns setup and hold times.

Transmit Enable: The MAC must assert TXEN at the same time as the first nibble of the preamble, and de-assert TXEN after the last bit of the packet.

Receive Data Valid: The KS8721CL asserts RXDV when it receives a valid packet. Line operating speed and MII mode will determine timing changes in the following way:

- For 100BASE-TX links with the MII in 4B mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the data packet.
- For 10BASE-T links, the entire preamble is truncated. RXDV is asserted with the first nibble of the SFD “5D” and remains asserted until the end of the packet.

Error Signals: Whenever the KS8721CL receives an error symbol from the network, it asserts RXER and drives “1110” (4B) on the RXD pins. When the MAC asserts TXER, the KS8721CL will drive “H” symbols (a Transmit Error defined in the IEEE 802.3 4B/5B code group) out on the line to force signaling errors.

Carrier Sense (CRS): For 100BASE-TX links, a start-of-stream delimiter, or /J/K symbol pair causes assertion of Carrier Sense (CRS). An end-of-stream delimiter, or /T/R symbol pair, causes de-assertion of CRS. The PMA layer will also de-assert CRS if IDLE symbols are received without /T/R, yet in this case RXER will be asserted for one clock cycle when CRS is de-

asserted. For 10BASE-T links, CRS assertion is based on reception of valid preamble, and de-assertion on reception of an end-of-frame (EOF) marker.

Collision: Whenever the line state is half-duplex and the transmitter and receiver are active at the same time, the KS8721CL asserts its collision signal, which is asynchronous to any clock.

RMII (Reduced MII) Data Interface

RMII interface specifies a low-pin count, Reduced Media Independent Interface (RMII) intended for use between Ethernet PHYs and Switch or Repeater ASICs. It is fully compliant with IEEE 802.3u [2].

This interface has the following characteristics:

- It is capable of supporting 10Mbps and 100Mbps data rates.
- A single clock reference is sourced from the MAC to PHY (or from an external source).
- It provides independent 2-bit wide (di-bit) transmit and receive data paths.
- It uses TTL signal levels compatible with common digital CMOS ASIC processes.

RMII Signal Definition

Signal Name	Direction (w/respect to the PHY)	Direction (w/respect to the MAC)	Use
REF_CLK	Input	Input or Output	Synchronous clock reference for receive, transmit and control interface
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data
TX_EN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data
RX_ER	Output	Input (Not Required)	Receive Error

Reference Clock (REF_CLK)

REF_CLK is a continuous 50MHz clock that provides the timing reference for CRS_DV, RXD[1:0], TX_EN, TXD[1:0], and RX_E. REF_CLK is sourced by the MAC or an external source. Switch implementations may choose to provide REF_CLK as an input or an output depending on whether they provide a REF_CLK output or rely on an external clock distribution device. Each PHY device must have an input corresponding to this clock but may use a single clock input for multiple PHYs implemented on a single IC.

Carrier Sense/Receive Data Valid (CRS_DV)

CRS_DV is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. That is, in 10BASE-T mode, when squelch is passed or in 100BASE-X mode when 2 noncontiguous zeroes in 10 bits are detected, the carrier is detected.

Loss-of-carrier results in the de-assertion of CRS_DV synchronous to REF_CLK. As carrier criteria are met, CRS_DV remains continuously asserted from the first recovered di-bit of the frame through the final recovered di-bit and is negated prior to the first REF_CLK that follows the final di-bit.

The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] remains as “00” until proper receive signal decoding takes place (see “Definition of RXD[1:0] Behavior”).

Receive Data [1:0] (RXD[1:0])

RXD[1:0] transitions synchronously to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY. In some cases (e.g., before data recovery or during error conditions), a predetermined value for RXD[1:0] is transferred instead of recovered data. RXD[1:0] remains as “00” to indicate idle when CRS_DV is de-asserted. Values of RXD[1:0] other than “00” when CRS_DV is de-asserted are reserved for out-of-band signalling (to be defined). Values other than “00” on RXD[1:0] while CRS_DV is de-asserted are ignored by the MAC/repeater. Upon assertion of CRS_DV, the PHY ensures that RXD[1:0]=00 until proper receive decoding takes place.

Transmit Enable (TX_EN)

Transmit Enable TX_EN indicates that the MAC is presenting di-bits on TXD[1:0] on the RMII for transmission. TX_EN is asserted synchronously with the first nibble of the preamble and remains asserted while all transmitted di-bits are presented

to the RMII. TX_EN is negated prior to the first REF_CLK following the final di-bit of a frame. TX_EN transitions synchronously with respect to REF_CLK.

Transmit Data [1:0] (TXD[1:0])

Transmit Data TXD[1:0] transitions synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] are accepted for transmission by the PHY. TXD[1:0] remains as “00” to indicate idle when TX_EN is de-asserted. Values of TXD[1:0] other than “00” when TX_EN is de-asserted are reserved for out-of-band signalling (to be defined). Values other than “00” on TXD[1:0] while TX_EN is de-asserted are ignored by the PHY.

Collision Detection

Since the definition of CRS_DV and TX_EN both contain an accurate indication of the start of frame, the MAC reliably regenerates the COL signal of the MII by ending TX_EN and CRS_DV.

During the IPG time following the successful transmission of a frame, the COL signal is asserted by some transceivers as a self-test. The Signal Quality Error (SQE) function is not supported by the reduced MII due to the lack of the COL signal. Historically, SQE was present to indicate that a transceiver located physically remote from the MAC was functioning. Since the reduced MII only supports chip-to-chip connections on a PCB, SQE functionality is not required.

RX_ER

The PHY provides RX_ER as an output according to the rules specified in IEEE 802.3u [2] (see Clause 24, Figure 24-11–Receive State Diagram). RX_ER is asserted for one or more REF_CLK periods to indicate that an error (e.g., a coding error or any error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sublayer) is detected somewhere in the frame presently being transferred from the PHY. RX_ER transitions synchronously with respect to REF_CLK. While CRS_DV is de-asserted, RX_ER has no effect on the MAC.

RMII AC Characteristics

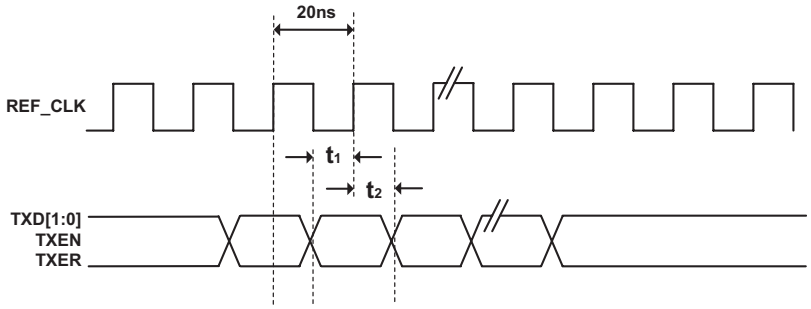
Symbol	Parameter	Min	Typ	Max	Unit
	REF_CLK Frequency		50		MHz
	REF_CLK Duty Cycle	35		65	%
t_{SU}	TXD[1:0], TX_EN, RXD[1:0], CRS_DV, RXER	4			ns
t_H	TXD[1:0], TX_EN, RXD[1:0], CRS_DV, RXER Data Hold from REF_CLK Rising Edge	2			ns

Unused RMII Pins

Input Pins TXD[2:3] and TXER are pull-down to GND.

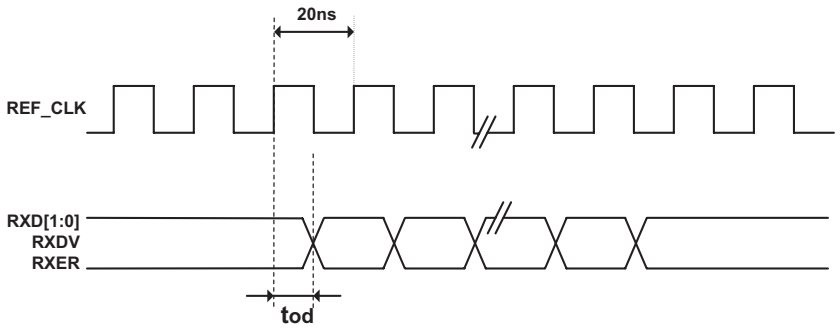
Output Pins RXD[2:3] and RXC are no connect. Note that the RMII pin needs to be pulled up to enable RMII mode.

RMII Transmit Timing



Parameter	Min	Typ	Max	Units
REF_CLK Frequency		50		MHz
TXEN, TXD[1:0], TX_EN, Data Setup to REF_CLK rising edge	4			ns
TXEN, TXD[1:0], TX_EN, Data hold from REF_CLK rising edge	2			ns

RMII Receive Timing



Parameter	Min	Typ	Max	Units
REF_CLK Frequency		50		MHz
RXD[1:0], CRS_DV, RX_ER Output delay from REF_CLK rising edge	2.8		10	ns

Auto-Crossover (Auto-MDI/MDI-X)

Automatic MDI/MDI-X configuration is intended to eliminate the need for crossover cables between similar devices. The assignment of pinouts for a 10BASE-T/100BASE-TX crossover function cable is shown below.

This feature eliminates the confusion in applications by allowing the use of both straight and crossover cables. This feature is controlled by register 1f:13. See the “Register 1fh–100BASE-TX PHY Controller” section for details.

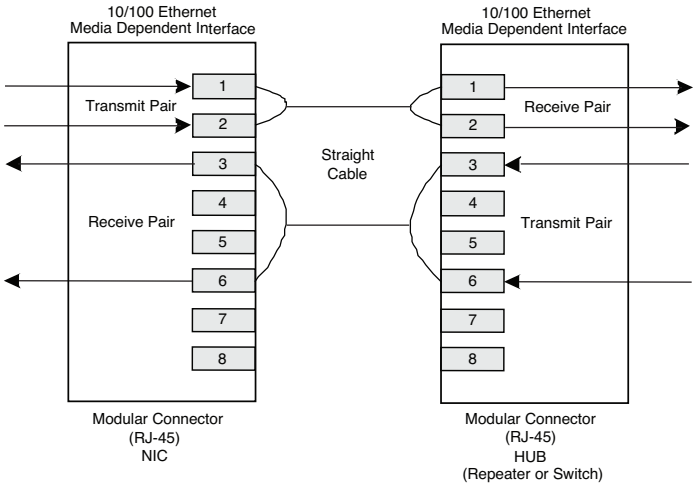


Figure 1. Straight Through Cable

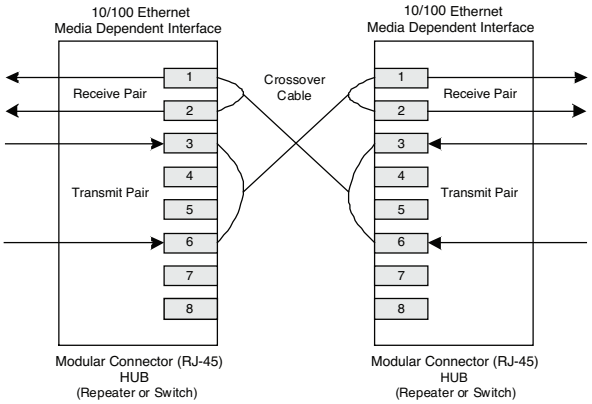


Figure 2. Crossover Cable

Power Management

The KS8721CL offers the following modes for power management:

- Power-Down Mode: This mode can be achieved by writing to Register 0.11 or pulling pin 30 PD# low.
- Power-Saving Mode: This mode can be disabled by writing to Register 1fh.10. The KS8721CL turns off everything except for the Energy Detect and PLL circuits when the cable is not installed. In other words, the KS8721CL shuts down most of the internal circuits to save power if there is no link. Power-saving mode is in the most effective state when auto-negotiation mode is enabled.

100BT FX Mode

Please contact your local field application engineer (FAE) for a reference schematic on fiber connection.

100BT FX mode is activated when FXSD/FXEN is higher than 0.6V (this pin has a default pull down). Under this mode, the auto-negotiation and auto-MDI-X features are disabled.

In fiber operation, the FXSD pin should connect to the signal detect (SD) output of the fiber module. The internal threshold of FXSD is around 1/2 V_{DD} ±50mV (1.25V ±0.05V). Above this level, the fiber signal is considered detected. The operation is summarized in the following table:

FXSD/FXEN	Condition
Less than 0.6V	100TX mode
Less than 1.25V, but greater than 0.6V	FX mode No signal detected FEF generated
Greater than 1.25	FX mode Signal detected

Table 1. 100BT FX Mode

To ensure proper operation, the swing of fiber module SD should cover the threshold variation. A resistive voltage divider is recommended to adjust the SD voltage range.

FEF, repetition of a special pattern which consists of 84-one and 1-zero, is generated under “FX mode with no signal detected.” The purpose of FEF is to notify the sender of a faulty link. When receiving an FEF, the LINK will go down to indicate a fault, even with fiber signal detected. The transmitter is not affected by receiving an FEF and still sends out its normal transmit pattern from MAC. FEF can be disabled by strapping pin 27 low. Refer to the “Strapping Options” section.

Media Converter Operation

The KS8721CL is capable of performing media conversion with two parts in a back-to-back RMII loop-back mode as indicated in the diagram. Both parts are in RMII mode and with RMII BTB asserted (pins 21 and 22 strapped high). One part is operating in TX mode and the other is operating in FX mode. Both parts can share a common 50MHz oscillator.

Under this operation, auto-negotiation on the TX side prohibits 10BASE-T link-up. Additional options can be implemented under this operation. Disable the transmitter and set it at tri-state by controlling the high TXD2 pin. In order to do this, RXD2 and TXD2 pins need to be connected via inverter. When TXD2 pin is high in both the copper and fiber operation, it is disabled transmit. Meanwhile, the RXD2 pin on the copper side serves as the energy detect and can indicate if a line signal is detected. TXD3 should be tied low and RXD3 allowed to float. Please contact your Micrel FAE for a media converter reference design.

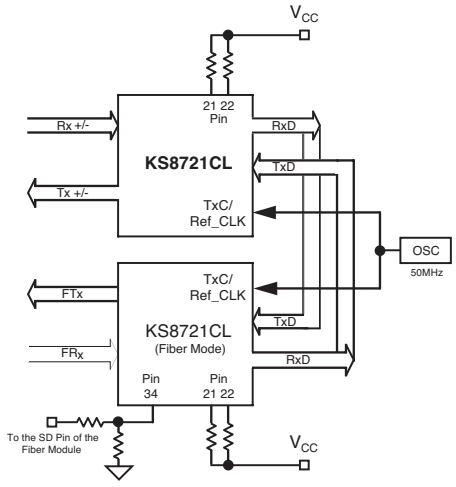


Figure 3. Fiber Module

Circuit Design Reference for Power Supply

Micrel's integrated built-in, voltage regulator technology allows the user to save BOM costs on both existing and future designs with the use of the new KS8721CL single supply, single port, 10/100 Ethernet PHY.

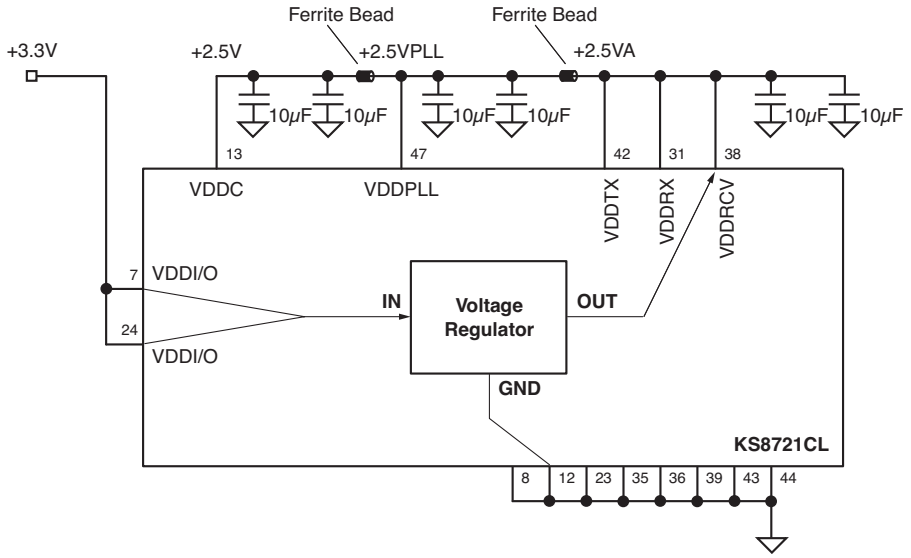


Figure 4. Circuit Design

The circuit design in Figure 4 shows the power connections for the power supply: the 3.3V to VDDI/O is the only input power source and the 2.5V at VDDRCV, pin 38, is the output of the voltage regulator that needs to supply through the rest of the 2.5V VDD pins via the 2.5V power plane.

Register Map

Register No.	Description
0h	Basic Control Register
1h	Basic Status Register
2h	PHY Identifier I
3h	PHY Identifier II
4h	Auto-Negotiation Advertisement Register
5h	Auto-Negotiation Link Partner Ability Register
6h	Auto-Negotiation Expansion Register
7h	Auto-Negotiation Next Page Register
8h	Link Partner Next Page Ability
15h	RXER Counter Register
1bh	Interrupt Control/Status Register
1fh	100BASE-TX PHY Control Register

Address	Name	Description	Mode[1]	Default
Register 0h - Basic Control				
0.15	Reset	1 = software reset. Bit is self-clearing.	RW/SC	0
0.14	Loop-Back	1 = loop-back mode; 0 = normal operation.	RW	0
0.13	Speed Select (LSB)	1 = 100Mbps; 0 = 10Mbps. Ignored if Auto-Negotiation is enabled (0.12 = 1).	RW	Set by SPD100
0.12	Auto-Negotiation Enable	1 = enable auto-negotiation process (override 0.13 and 0.8). 0 = disable auto-negotiation process.	RW	Set by NWAYEN
0.11	Power Down	1 = power-down mode; 0 = normal operation.	RW	0
0.10	Isolate	1 = electrical isolation of PHY from MII and TX+/TX-. 0 = normal operation.	RW	Set by ISO
0.9	Restart Auto-Negotiation	1 = restart auto-negotiation process. 0 = normal operation. Bit is self-clearing.	RW/SC	0
0.8	Duplex Mode	1 = full-duplex; 0 = half-duplex.	RW	Set by DUPLEX
0.7	Collision Test	1 = enable COL test; 0 = disable COL test.	RW	0
0.6:1	Reserved		RO	0
0.0	Disable Transmitter	0 = enable transmitter. 1 = disable transmitter.	R/W	0
Register 1h - Basic Status				
1.15	100BASE-T4	1 = T4 capable; 0 = not T4 capable.	RO	0
1.14	100BASE-TX Full-Duplex	1 = capable of 100BASE-X full-duplex. 0 = not capable of 100BASE-X full-duplex.	RO	1
1.13	100BASE-TX Half-Duplex	1 = capable of 100BASE-X half-duplex. 0 = not capable of 100BASE-X half-duplex.	RO	1
1.12	10BASE-T Full-Duplex	1 = 10Mbps with full-duplex. 0 = no 10Mbps with full-duplex capability.	RO	1
1.11	10BASE-T Half-Duplex	1 = 10Mbps with half-duplex. 0 = no 10Mbps with half-duplex capability.	RO	1

Note:

1. RW: Read/Write, RO: Read Only, SC: Self Clear, LH: Latch High, LL: Latch Low. Some of the default values are set by strap-in. See “Strapping Options.”

Address	Name	Description	Mode[1]	Default
1.10:7	Reserved		RO	0
1.6	No Preamble	1 = preamble suppression; 0 = normal preamble.	RO	1
1.5	Auto-Negotiation Complete	1 = auto-negotiation process completed. 0 = auto-negotiation process not completed.	RO	0
1.4	Remote Fault	1 = remote fault; 0 = no remote fault.	RO/LH	0
1.3	Auto-Negotiation Ability	1 = capable to perform auto-negotiation. 0 = unable to perform auto-negotiation.	RO	1
1.2	Link Status	1 = link is up; 0 = link is down.	RO/LL	0
1.1	Jabber Detect	1 = jabber detected; 0 = jabber not detected. Default is low.	RO/LH	0
1.0	Extended Capability	1 = supports extended capabilities registers.	RO	1
Register 2h - PHY Identifier 1				
2.15:0	PHY ID Number	Assigned to the 3rd through 18th bits of the organizationally. unique identifier (OUI). Micrel's OUI is 0010A1 (hex).	RO	0022h
Register 3h - PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the organizationally unique identifier (OUI). Micrel's OUI is 0010A1 (hex).	RO	000101
3.9:4	Model Number	Six bit manufacturer's model number.	RO	100001
3.3:0	Revision Number	Four bit manufacturer's model number.	RO	1001
Register 4h - Auto-Negotiation Advertisement				
4.15	Next Page	1 = next page capable; 0 = no next page capability.	RW	0
4.14	Reserved		RO	0
4.13	Remote Fault	1 = remote fault supported; 0 = no remote fault.	RW	0
4.12 : 11	Reserved		RO	0
4.10	Pause	1 = pause function supported; 0 = no pause function.	RW	0
4.9	100BASE-T4	1 = T4 capable; 0 = no T4 capability.	RO	0
4.8	100BASE-TX Full-Duplex	1 = TX with full-duplex; 0 = no TX full-duplex capability.	RW	Set by SPD100 & DUPLEX
4.7	100BASE-TX	1 = TX capable; 0 = no TX capability.	RW	Set by SPD100
4.6	10BASE-T Full-Duplex	1 = 10Mbps with full-duplex. 0 = no 10Mbps full-duplex capability.	RW	Set by DUPLEX
4.5	10BASE-T	1 = 10Mbps capable; 0 = no 10Mbps capability.	RW	1
4.4:0	Selector Field	[00001] = IEEE 802.3.	RW	00001
Register 5h - Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = next page capable; 0 = no next page capability.	RO	0
5.14	Acknowledge	1 = link code word received from partner. 0 = link code word not yet received.	RO	0
5.13	Remote Fault	1 = remote fault detected; 0 = no remote fault.	RO	0
5.12	Reserved		RO	0

Note:

1. RW: Read/Write, RO: Read Only, SC: Self Clear, LH: Latch High, LL: Latch Low. Some of the default values are set by strap-in. See "Strapping Options."

Address	Name	Description	Mode[1]	Default
5.11:10	Pause	5.10 5 .11 0 0 No PAUSE 0 1 Asymmetric PAUSE (link partner) 1 0 Symmetric PAUSE 1 1 Symmetric & Asymmetric PAUSE (local device)	RO	0
5.9	100 BASE-T4	1 = T4 capable; 0 = no T4 capability.	RO	0
5.8	100BASE-TX Full-Duplex	1 = TX with full-duplex; 0 = no TX full-duplex capability.	RO	0
5.7	100BASE-TX	1 = TX capable; 0 = no TX capability.	RO	0
5.6	10BASE-T Full-Duplex	1 = 10Mbps with full-duplex. 0 = no 10Mbps full-duplex capability.	RO	0
5.5	10BASE-T	1 = 10Mbps capable; 0 = no 10Mbps capability.	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3.	RO	00001
Register 6h - Auto-Negotiation Expansion				
6.15:5	Reserved		RO	0
6.4	Parallel Detection Fault	1 = fault detected by parallel detection. 0 = no fault detected by parallel detection.	RO/LH	0
6.3	Link Partner Next Page Able	1 = link partner has next page capability. 0 = link partner does not have next page capability.	RO	0
6.2	Next Page Able	1 = local device has next page capability. 0 = local device does not have next page capability.	RO	1
6.1	Page Received	1 = new page received; 0 = new page not yet received.	RO/LH	0
6.0	Link Partner Auto-Negotiation Able	1 = link partner has auto-negotiation capability. 0 = link partner does not have auto-negotiation capability.	RO	0
Register 7h - Auto-Negotiation Next Page				
7.15	Next Page	1 = additional next page(s) will follow; 0 = last page.	RW	0
7.14	Reserved		RO	0
7.13	Message Page	1 = message page; 0 = unformatted page.	RW	1
7.12	Acknowledge 2	1 = will comply with message. 0 = cannot comply with message.	RW	0
7.11	Toggle	1 = previous value of the transmitted link code word. equaled logic One; 0 = logic Zero.	RO	0
7.10:0	Message Field	11-bit wide field to encode 2048 messages.	RW	001
Register 8h - Link Partner Next Page Ability				
8.15	Next Page	1 = additional next page(s) will follow; 0 = last page.	RO	0
8.14	Acknowledge	1 = successful receipt of link word. 0 = no successful receipt of link word.	RO	0
8.13	Message Page	1 = Message Page; 0 = unformatted page.	RO	0
8.12	Acknowledge 2	1 = able to act on the information. 0 = not able to act on the information.	RO	0
8.11	Toggle	1 = previous value of transmitted link code word equal to logic zero; 0 = previous value of transmitted link code word equal to logic one.	RO	0
8.10:0	Message Field		RO	0

Note:

1. RW: Read/Write, RO: Read Only, SC: Self Clear, LH: Latch High, LL: Latch Low. Some of the default values are set by strap-in. See “Strapping Options.”

Address	Name	Description	Mode[1]	Default
Register 15h - RXER Counter				
15.15:0	RXER Counter	RX Error counter for the RX_ER in each package.	RO	0000
Register 1bh - Interrupt Control/Status Register				
1b.15	Jabber Interrupt Enable	1 = Enable jabber interrupt; 0 = Disable jabber interrupt.	RW	0
1b.14	Receive Error Interrupt Enable	1 = Enable receive error interrupt. 0 = Disable receive error interrupt.	RW	0
1b.13	Page Received Interrupt Enable	1 = Enable page received interrupt. 0 = Disable page received interrupt.	RW	0
1b.12	Parallel Detect Fault Interrupt Enable	1 = Enable parallel detect fault interrupt. 0 = Disable parallel detect fault interrupt.	RW	0
1b.11	Link Partner Acknowledge Interrupt Enable	1 = Enable link partner acknowledge interrupt. 0 = Disable link partner acknowledge interrupt.	RW	0
1b.10	Link Down Interrupt Enable	1 = Enable link down interrupt. 0 = Disable link down interrupt.	RW	0
1b.9	Remote Fault Interrupt Enable	1 = Enable remote fault interrupt. 0 = Disable remote fault interrupt.	RW	0
1b.8	Link Up Interrupt Enable	1 = Enable link up interrupt. 0 = Disable link up interrupt.	RW	0
1b.7	Jabber Interrupt	1 = Jabber interrupt occurred. 0 = Jabber interrupt has not occurred.	RO/SC	0
1b.6	Receive Error Interrupt	1 = Receive error occurred. 0 = Receive error has not occurred.	RO/SC	0
1b.5	Page Receive Interrupt	1 = Page receive occurred. 0 = Page receive has not occurred.	RO/SC	0
1b.4	Parallel Detect Fault Interrupt	1 = Parallel detect fault occurred. 0 = Parallel detect fault has not occurred.	RO/SC	0
1b.3	Link Partner Acknowledge Interrupt	1 = Link partner acknowledge occurred. 0 = Link partner acknowledge has not occurred.	RO/SC	0
1b.2	Link Down Interrupt	1 = Link down occurred. 0 = Link down has not occurred.	RO/SC	0
1b.1	Remote Fault Interrupt	1 = Remote fault occurred. 0 = Remote fault has not occurred.	RO/SC	0
1b.0	Link Up Interrupt	1 = Link up interrupt occurred. 0 = Link up interrupt has not occurred.	RO/SC	0
Register 1fh - 100BASE-TX PHY Controller				
1f.15:14	Reserved			
1f:13	Pairswap Disable	1 = Disable MDI/MDI-X; 0 = Enable MDI/MDI-X.	R/W	0
1f.12	Energy Detect	1 = Presence of signal on RX+/RX- analog wire pair. 0 = No signal detected on RX+/RX-.	RO	0
1f.11	Force Link	1 = Force link pass; 0 = Normal link operation. This bit bypasses the control logic and allow transmitter to send pattern even if there is no link.	R/W	0
1f.10	Power-Saving	1 = Enable power-saving; 0 = Disable.	RW	1
1f.9	Interrupt Level	1 = Interrupt pin active high; 0 = Active low.	RW	0
1f.8	Enable Jabber	1 = Enable jabber counter; 0 = Disable.	RW	1
1f.7	Auto-Negotiation Complete	1 = Auto-Negotiation complete; 0 = Not complete.	RW	0

Note:

1. RW: Read/Write, RO: Read Only, SC: Self Clear, LH: Latch High, LL: Latch Low. Some of the default values are set by strap-in. See “Strapping Options.”

Address	Name	Description	Mode[1]	Default
1f.6	Enable Pause (Flow-Control Result)	1 = Flow control capable; 0 = No flow control.	RO	0
1f.5	PHY Isolate	1 = PHY in isolate mode; 0 = Not isolated.	RO	0
1f.4:2	Reserved			
1f.1	Enable SQE Test	1 = Enable SQE test; 0 = Disable.	RW	0
1f.0	Disable Data Scrambling	1 = Disable scrambler; 0 = Enable.	RW	0

Note:

1. RW: Read/Write, RO: Read Only, SC: Self Clear, LH: Latch High, LL: Latch Low. Some of the default values are set by strap-in. See “Strapping Options.”

Absolute Maximum Ratings[1]

Storage Temperature (T_S) ..... –55°C to +150°C
Supply Referenced to GND ..... –0.5V to +4.0V
All Pins ..... –0.5V to +4.0V

Important: Please read the Notes at the bottom of the page.

Operating Ratings[2]

Supply Voltage
(V_{DD_PLL}, V_{DD_TX}, V_{DD_RXC}, V_{DD_RCV}, V_{DDC}) ..... +2.5V
(V_{DDIO}) ..... +3.3V
Ambient Temperature (T_A)
Commercial ..... 0°C to +70°C
Industrial ..... –40°C to +85°C
Package Thermal Resistance[3]
LQFP (θ_{JA})
No Airflow ..... 83.56°C/W

Electrical Characteristics[4]

V_{DD} = 3.3V ±10%

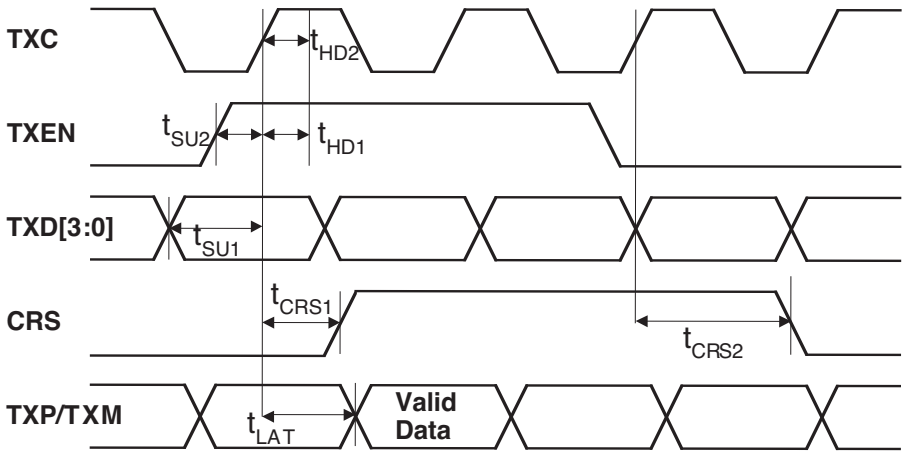
Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Total Supply Current (including TX output driver current)[5]						
I_{DD1}	Normal 100BASE-TX	Including 43mA output current		116		mA
I_{DD2}	Normal 10BASE-T (independent of utilization)	Including 103mA output current		151		mA
I_{DD3}	Power-Saving Mode 1	Auto-Negotiation is Enable		47		mA
I_{DD5}	Power-Down Mode			4		mA
TTL Inputs						
V_{IH}	Input High Voltage		1/2V_{DD}(I/O) +0.2			V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current	V_{IN} = GND ~ V_{DD}	–10		10	µA
TTL Outputs						
V_{OH}	Output High Voltage	I_{OH} = –4mA	1/2V_{DD}(I/O) +0.6			V
V_{OL}	Output Low Voltage	I_{OL} = 4mA			0.4	V
$\|I_{OZ}\|$	Output Tri-State Leakage				10	µA
100BASE-TX Receive						
R_{IN}	RX+/RX– Differential Input Resistance			8		kΩ
	Propagation Delay	From magnetics to RDTX		50	110	ns
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	50Ω from each output to V_{DD}	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	50Ω from each output to V_{DD}			2	%
t_r, t_t	Rise/Fall Time Rise/Fall Time Imbalance		3 0		5 0.5	ns ns

Notes:

1. Exceeding the absolute maximum rating(s) may cause permanent damage to the device. Operating at maximum conditions for extended periods may affect device reliability.
2. The device is not guaranteed to function outside its operating rating. Unused inputs must always be tied to an appropriate logic voltage level (Ground to V_{DD}).
3. No HS (heat spreader) in package.
4. Specification for packaged product only.
5. There is 100% data transmission in full-duplex mode and a minimum IPG with a 130-meter cable.

Symbol	Parameter	Condition	Min	Typ	Max	Units
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
	Duty Cycle Distortion				±0.5	ns
	Overshoot				5	%
V_{SET}	Reference Voltage of ISET			0.75		V
	Propagation Delay	from TDTX to magentics		45	60	ns
	Jitters			0.7	1.4	$ns_{(pp)}$
10BASE-TX Receive						
R_{IN}	RX+/RX– Differential Input Resistance			8		kW
V_{SQ}	Squelch Threshold	5MHz square wave		400		mV
10BASE-TX Transmit (measured differentially after 1:1 transformer)						
V_P	Peak Differential Output Voltage	50W from each output to V_{DD}	2.2		2.8	V
	Jitters Added	50W from each output to V_{DD}			±3.5	ns
t_r, t_t	Rise/Fall Time			25		ns
Clock Outputs						
X1, X2	Crystal Oscillator			25		MHZ
RXC_{100}	Receive Clock, 100TX			25		MHZ
RXC_{10}	Receive Clock, 10T			2.5		MHZ
	Receive Clock Jitters			3.0		$ns_{(pp)}$
TXC_{100}	Transmit Clock, 100TX			25		MHZ
TXC_{10}	Transmit Clock, 10T			2.5		MHZ
	Transmit Clock Jitters			1.8		$ns_{(pp)}$

Timing Diagrams



SQE Timing

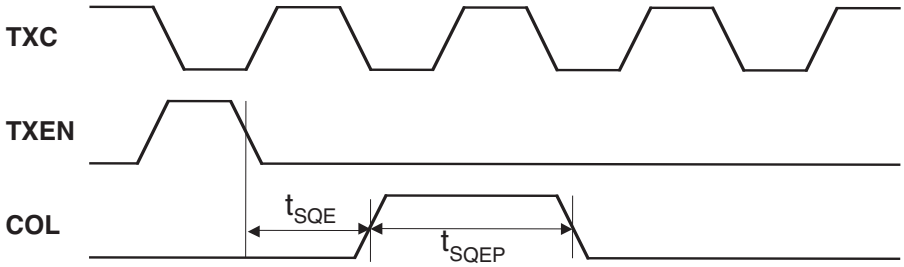


Figure 5. 10BASE-T MII Transmit Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{SU1}	TXD [3:0] Set-Up to TXC High	10			ns
t_{SU2}	TXEN Set-Up to TXC High	10			ns
t_{HD1}	TXD [3:0] Hold After TXC High	0			ns
t_{HD2}	TXEN Hold After TXC High	0			ns
t_{CRS1}	TXEN High to CRS Asserted Latency		4		BT(1)
t_{CRS2}	TXEN Low to CRS De-Asserted Latency		8		BT
t_{LAT}	TXEN High to TXP/TXM Output (TX Latency)		4		BT
t_{SQE}	COL (SQE) Delay After TXEN De-Asserted		2.5		µs
t_{SQEP}	COL (SQE) Pulse Duration		1.0		µs

Table 2. 10BASE-T MII Transmit Timing Parameters

Note:

1. BT = bit time.
   1BT = 10ns @ 100BT.

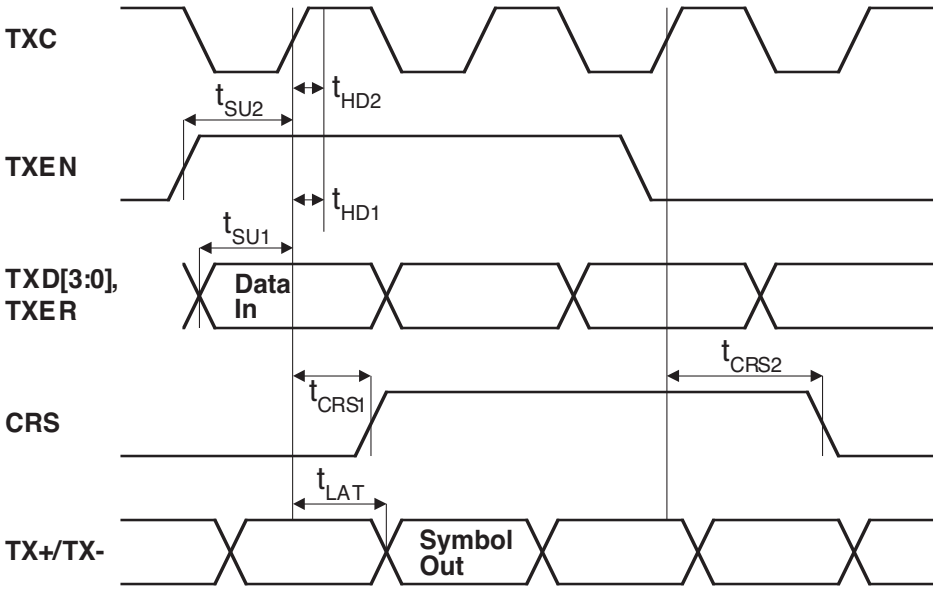


Figure 6. 100BASE-T MII Transmit Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{SU1}	TXD [3:0] Set-Up to TXC High	10			ns
t_{SU2}	TXEN Set-Up to TXC High	10			ns
t_{HD1}	TXD [3:0] Hold After TXC High	0			ns
t_{HD2}	TXER Hold After TXC High	0			ns
t_{HD3}	TXEN Hold After TXC High	0			ns
t_{CRS1}	TXEN High to CRS Asserted Latency		4		BT
t_{CRS2}	TXEN Low to CRS De-Asserted Latency		4		BT
t_{LAT}	TXEN High to TX+/TX– Output (TX Latency)		9		BT

Table 3. 100BASE-T MII Transmit Timing Parameters

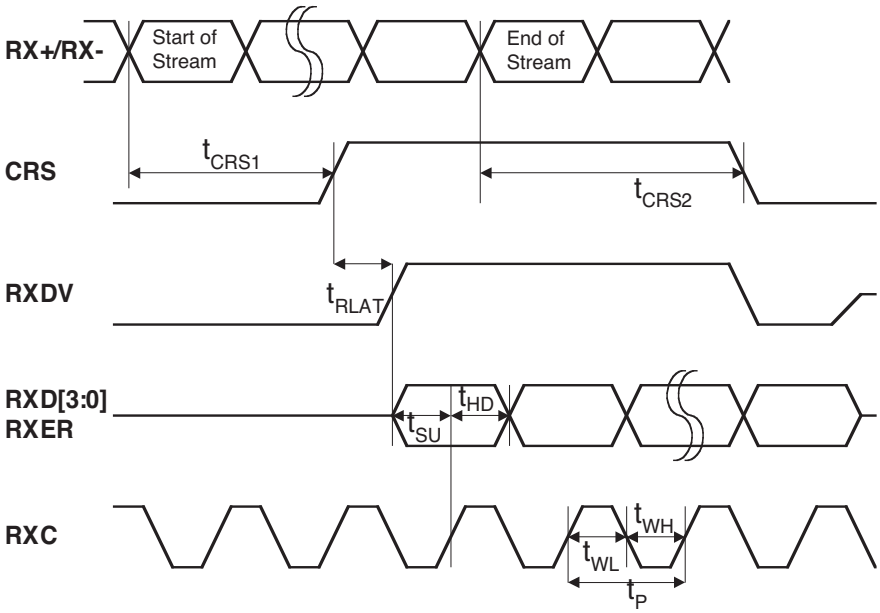


Figure 7. 100BASE-T MII Receive Timing

Symbol	Parameter	Min	Typ	Max	Units
t_P	RXC Period		40		ns
t_{WL}	RXC Pulse Width	20			ns
t_{WH}	RXC Pulse Width	20			ns
t_{SU}	RXD [3:0], RXER, RXDV Set-Up to Rising Edge of RXC		20		ns
t_{HD}	RXD [3:0], RXER, RXDV Hold from Rising Edge of RXC		20		ns
t_{RLAT}	CRS to RXD Latency, 4B or 5B Aligned		6		BT
t_{CRS1}	“Start of Stream” to CSR Asserted	106		138	ns
t_{CRS2}	“End of Stream” to CSR De-Asserted	154		186	ns

Table 4. 100BASE-T MII Receive Timing Parameters

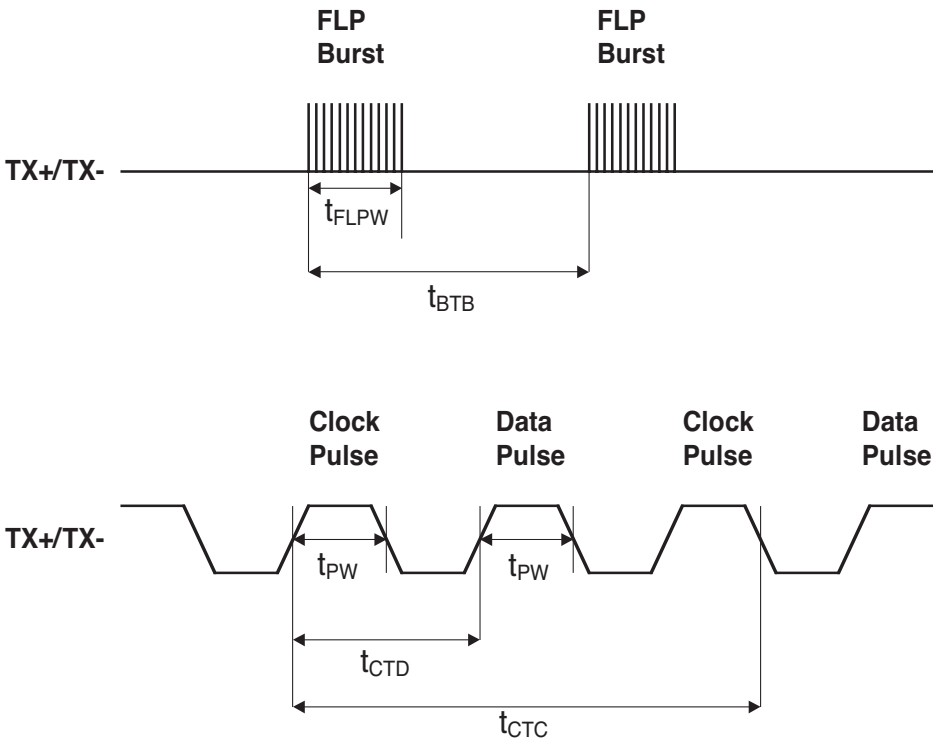


Figure 8. Auto-Negotiation/Fast Link Pulse Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{BTB}	FLP Burst to FLP Burst	8	16	24	ms
t_{FLPW}	FLP Burst Width		2		ms
t_{PW}	Clock/Data Pulse Width		100		ns
t_{CTD}	Clock Pulse to Data Pulse		69		µs
t_{CTC}	Clock Pulse to Clock Pulse Number of Clock/Data Pulses per Burst	 17	136	 33	µs µs

Table 5. Auto-Negotiation/Fast Link Pulse Timing

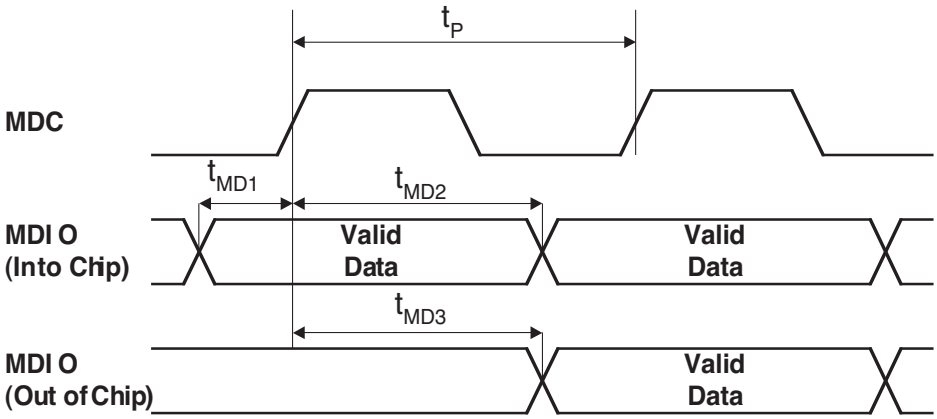


Figure 9. Serial Management Interface Timing

Symbol	Parameter	Min	Typ	Max	Units
t_P	MDC Period		400		ns
t_{MD1}	MDIO Set-Up to MDC (MDIO as Input)	10			ns
t_{MD2}	MDIO Hold After MDC (MDIO as Input)	10			ns
t_{MD3}	MDC to MDIO Valid (MDIO as Output)		222		ns

Table 6. Serial Management Interface Timing

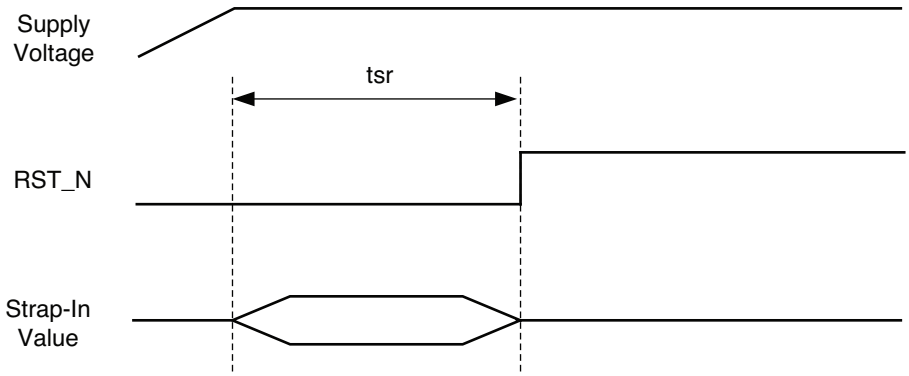


Figure 10. Reset Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{sr}	Stable Supply Voltages to Reset High	50			µs

Table 7. Reset Timing Parameters

Reference Circuit for Strapping Option Configuration

Figure 10 shows the reference circuit for strapping option pins.

Reset Circuit Diagram

Micrel recommendeds the following discrete reset circuit as shown in Figure 11 when powering up the KS8721CL device. For the application where the reset circuit signal comes from another device (e.g., CPU, FPGA, etc), we recommend the reset circuit as shown in Figure 12.

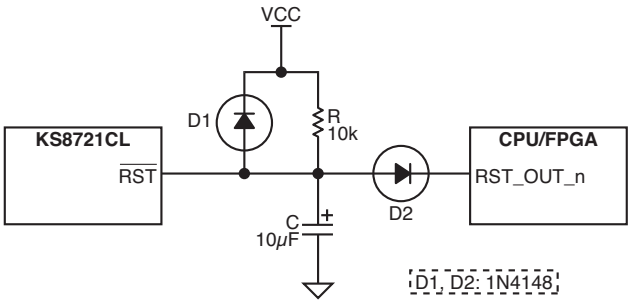


Figure 11. Recommended Reset Circuit.

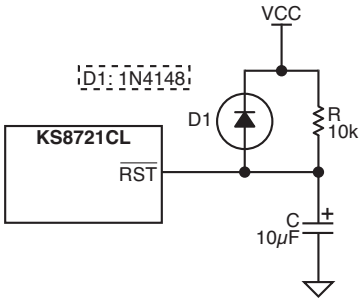
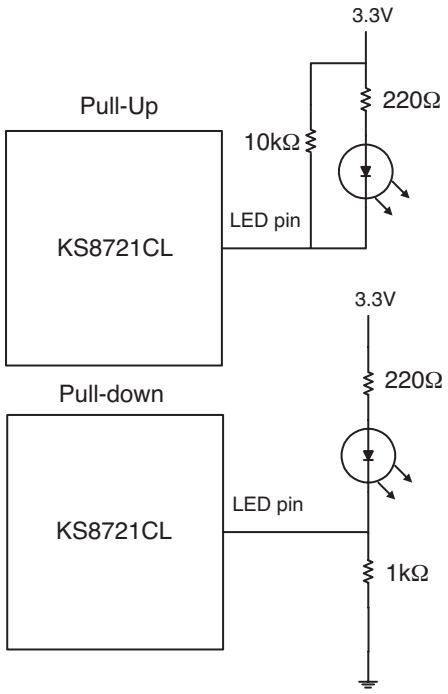


Figure 12. Recommended Circuit for Interfacing with CPU/FPGA Reset

At power-on-reset, R, C, and D1 provide the necessary ramp rise time to reset the Micrel device. The reset out from CPU/FPGA provides warm reset after power up. It is also recommended to power up the VDD core voltage earlier than VDDIO voltage. At worst case, the both VDD core and VDDIO voltages should come up at the same time.



Reference circuits for unmanaged programming through LED ports

Figure 13. Reference Circuit, Strapping Option Pins

Selection of Isolation Transformer(1)

One simple 1:1 isolation transformer is needed at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements. The following table gives recommended transformer characteristics.

Characteristic	Value	Test Condition
Turns Ratio	1 CT : 1 CT	
Open-Circuit Inductance (min.)	350μH	100mV, 100kHz, 8mA
Leakage Inductance (max.)	0.4μH	1MHz (min.)
Inter-Winding Capacitance (max.)	12pF	
D.C. Resistance (max.)	0.9Ω	
Insertion Loss (max.)	1.0dB	0MHz to 65MHz
HIPOT (min.)	1500Vrms	

Note:

1. The IEEE 802.3u standard for 100BASE-TX assumes a transformer loss of 0.5dB. For the transmit line transformer, insertion loss of up to 1.3dB can be compensated or by increasing the line drive current by means of reducing the ISET resistor value. Please select the transformer that supports auto-MDI/MDI-X.

Selection of Reference Crystal

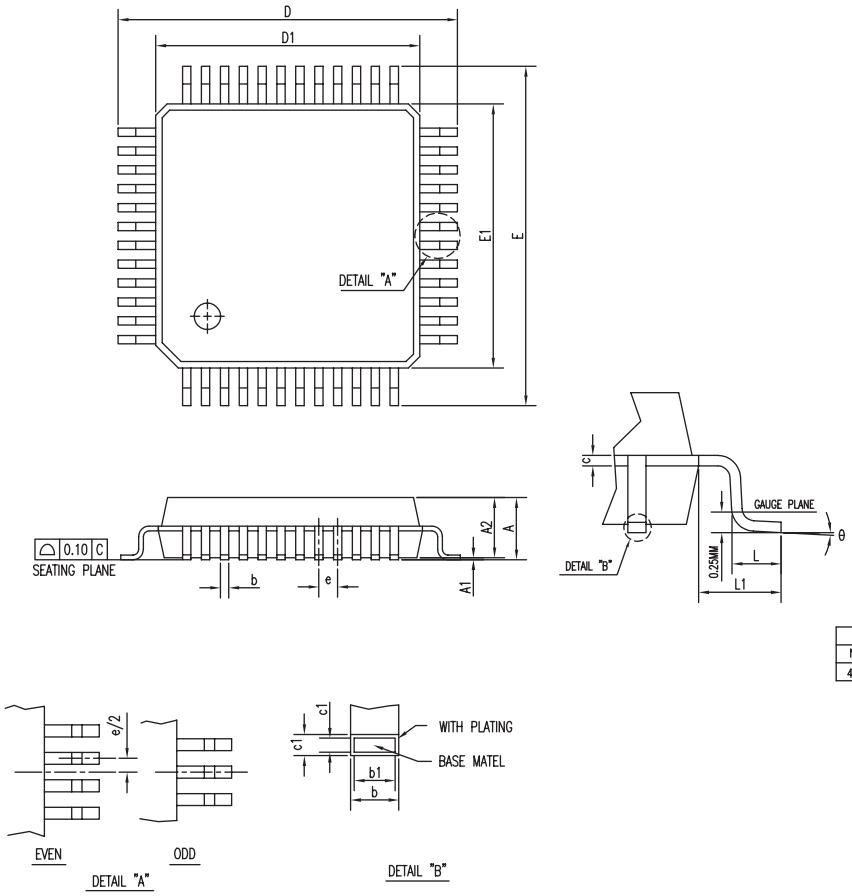
An oscillator or crystal with the following typical characteristics is recommended.

Characteristic	Value	Units
Frequency	25.00000	MHz
Frequency Tolerance (max.)	±100	ppm
Load Capacitance (max.)	20	pF
Series Resistance (max.)	40	Ω

Single Port Magnetic Manufacturer	Part Number	Auto-MDI-X	Number of Ports
Pulse	H1102	Yes	1
Bel Fuse	S558-5999-U7	Yes	1
YCL	PH163112	Yes	1
Transpower	HB726	Yes	1
Delta	LF8505	Yes	1
LanKom	LF-H41S	Yes	1
Intergrated Transformers			
Pulse	J0011D21	Yes	1
Pulse	J00-0061	Yes	1

Table 8. Qualified Transformer List

Package Information



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
c	0.129 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						

	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.19	0.22	0.25	0.17	0.20	0.23	0.50 BSC.			

48-pin LQFP (LQ)

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