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LS1046A

QorIQ LS1046A, LS1026A Data Sheet

Features

- LS1046A has four cores and LS1026A has two cores
- Four 32-bit/64-bit Arm® Cortex®-v8 A72 CPUs
  - Arranged as a single cluster of four cores sharing a single 2 MB L2 cache
  - Up to 1.8 GHz operation
  - Single-threaded cores with 32 KB L1 data cache and 48 KB L1 instruction cache
- Hierarchical interconnect fabric
  - Up to 700 MHz operation
- One 32-bit/64-bit DDR4 SDRAM memory controller with ECC and interleaving support
  - Up to 2.1 GT/s
- Data Path Acceleration Architecture (DPAA) incorporating acceleration for the following functions:
  - Packet parsing, classification, and distribution (FMan)
  - Queue management for scheduling, packet sequencing, and congestion management (QMan)
  - Hardware buffer management for buffer allocation and de-allocation (BMan)
  - Cryptography acceleration (SEC)
  - IEEE 1588™ support
- Two RGMII interfaces
- Eight SerDes lanes for high-speed peripheral interfaces
  - Three PCI Express 3.0 controllers
  - One Serial ATA (SATA 6 Gbit/s) controller
  - Up to two XFI (10 GbE) interfaces
  - Up to five SGMII interfaces supporting 1000 Mbps
  - Up to three SGMII interfaces supporting 2500 Mbps
  - Up to one QSGMII interface
  - Supports 10GBase-KR
  - Supports 1000Base-KX
- Additional peripheral interfaces
  - One Quad Serial Peripheral Interface (QSPI) controller
  - One Serial Peripheral Interface (SPI) controller
  - Integrated flash controller (IFC) supporting NAND and NOR flash
  - Three high-speed USB 3.0 controllers with integrated PHY
  - One Enhanced Secure Digital Host Controller supporting SD 3.0, eMMC 4.4, and eMMC 4.5
  - Four I2C controllers
  - Two 16550-compliant DUARTs and six low-power UARTs (LPUARTs)
  - General purpose IO (GPIO), eight Flextimers
  - One Queue Direct Memory Access Controller (qDMA)
  - One Enhanced Direct Memory Access Controller (eDMA)
  - Global programmable interrupt controller (GIC)
  - Thermal monitoring unit (TMU)
- 780 FC-PBGA package, 23 mm x 23 mm

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

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1 Introduction

The LS1046A is a cost-effective, power-efficient, and highly integrated system-on-chip (SoC) design that extends the reach of the NXP value-performance line of QorIQ communications processors. Featuring power-efficient 64-bit Arm® Cortex®-A72 cores with ECC-protected L1 and L2 cache memories for high reliability, running up to 1.8 GHz.

The LS1046A and LS1026A processors are perfectly suited for a range of embedded applications such as enterprise routers and switches, linecard controllers, network attached storage, security appliances, virtual customer premise equipment (vCPE), service providers gateways, and single board computers.

This figure shows the block diagram of the chip.

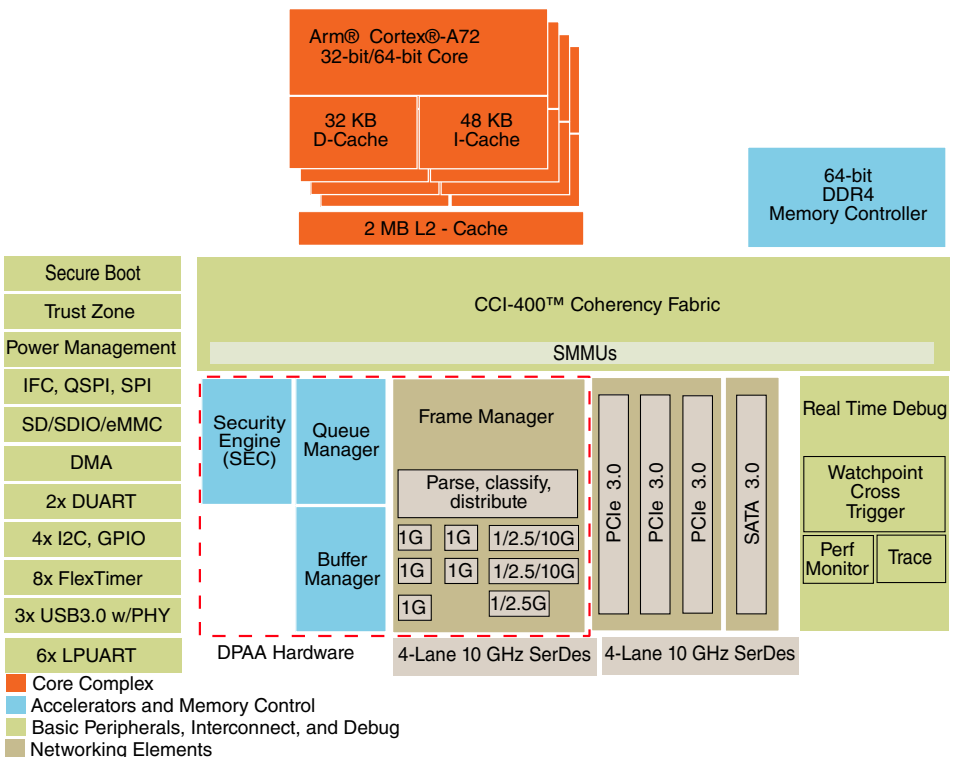


Figure 1. LS1046A block diagram

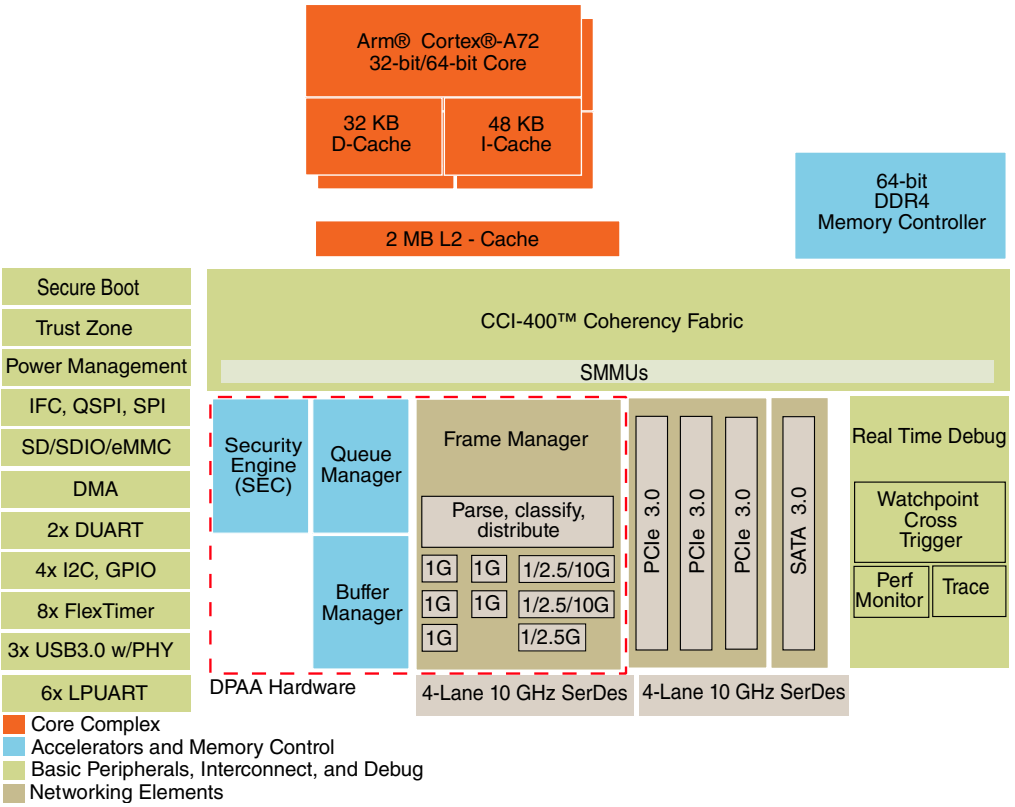


Figure 2. LS1026A block diagram

2 Pin assignments

2.1 780 BGA ball layout diagrams

This figure shows the complete view of the LS1046A BGA ball map diagram. Figure 4, Figure 5, Figure 6, and Figure 7 show quadrant views.

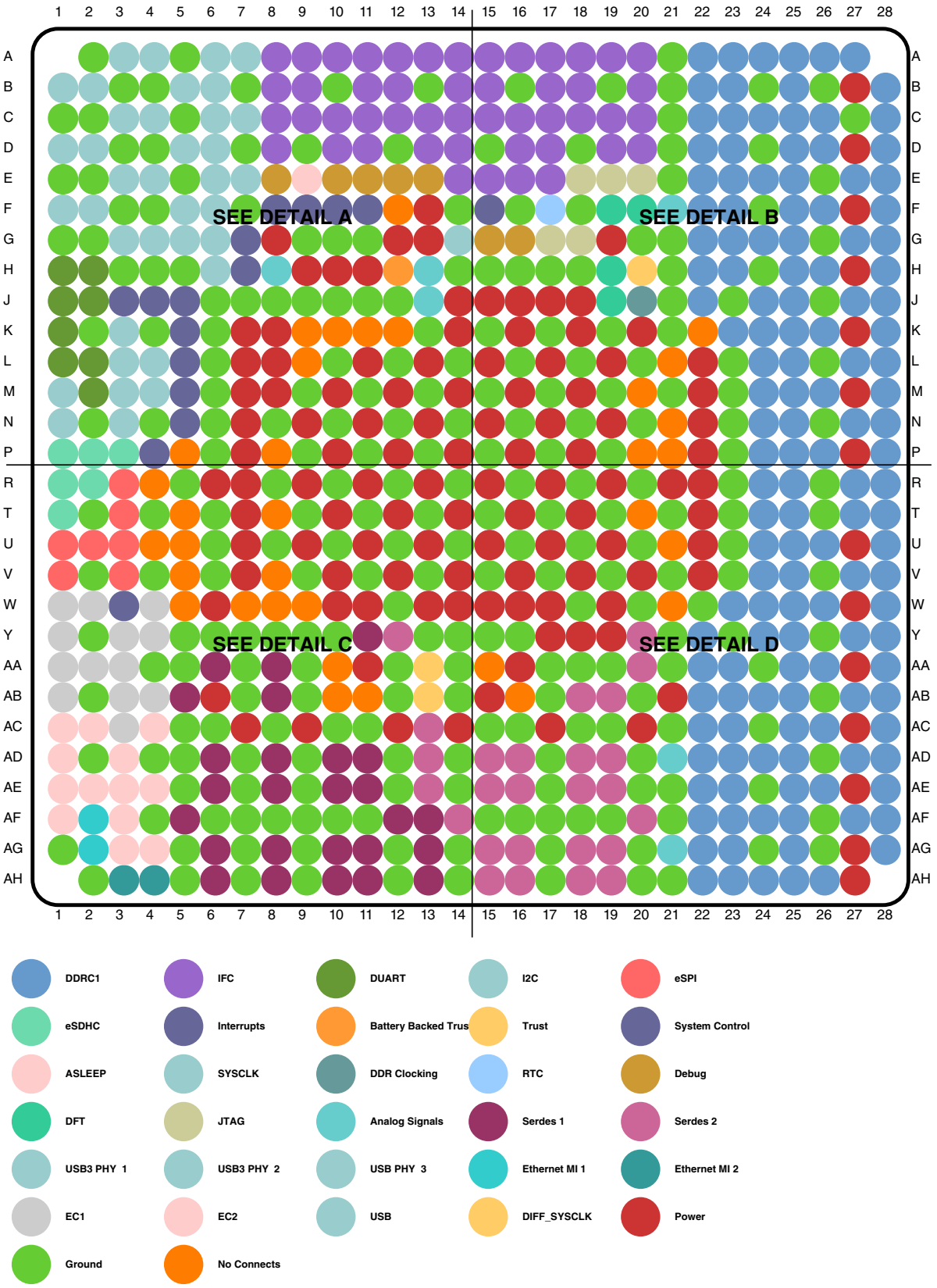


Figure 3. Complete BGA Map for the LS1046A

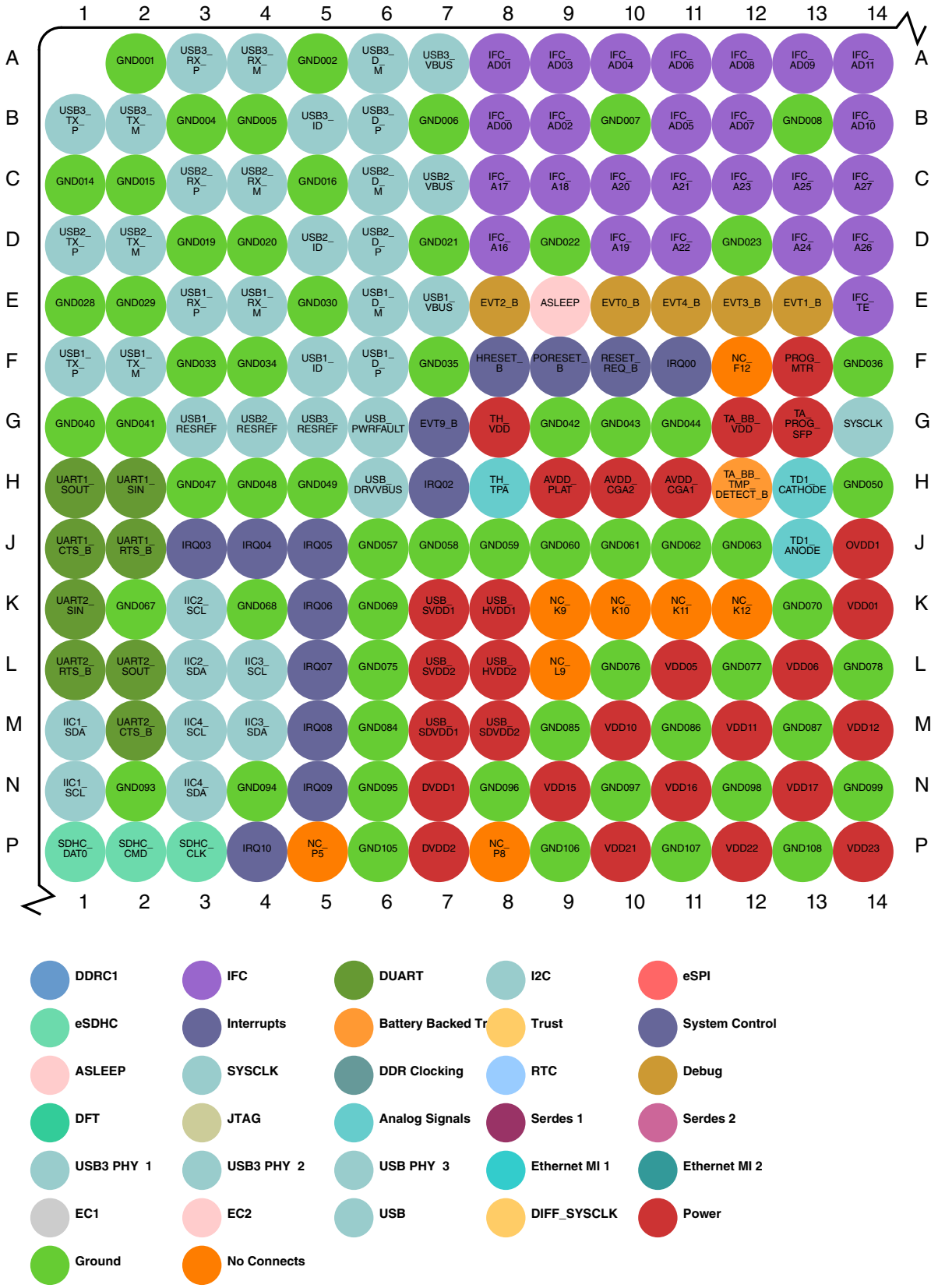


Figure 4. Detail A

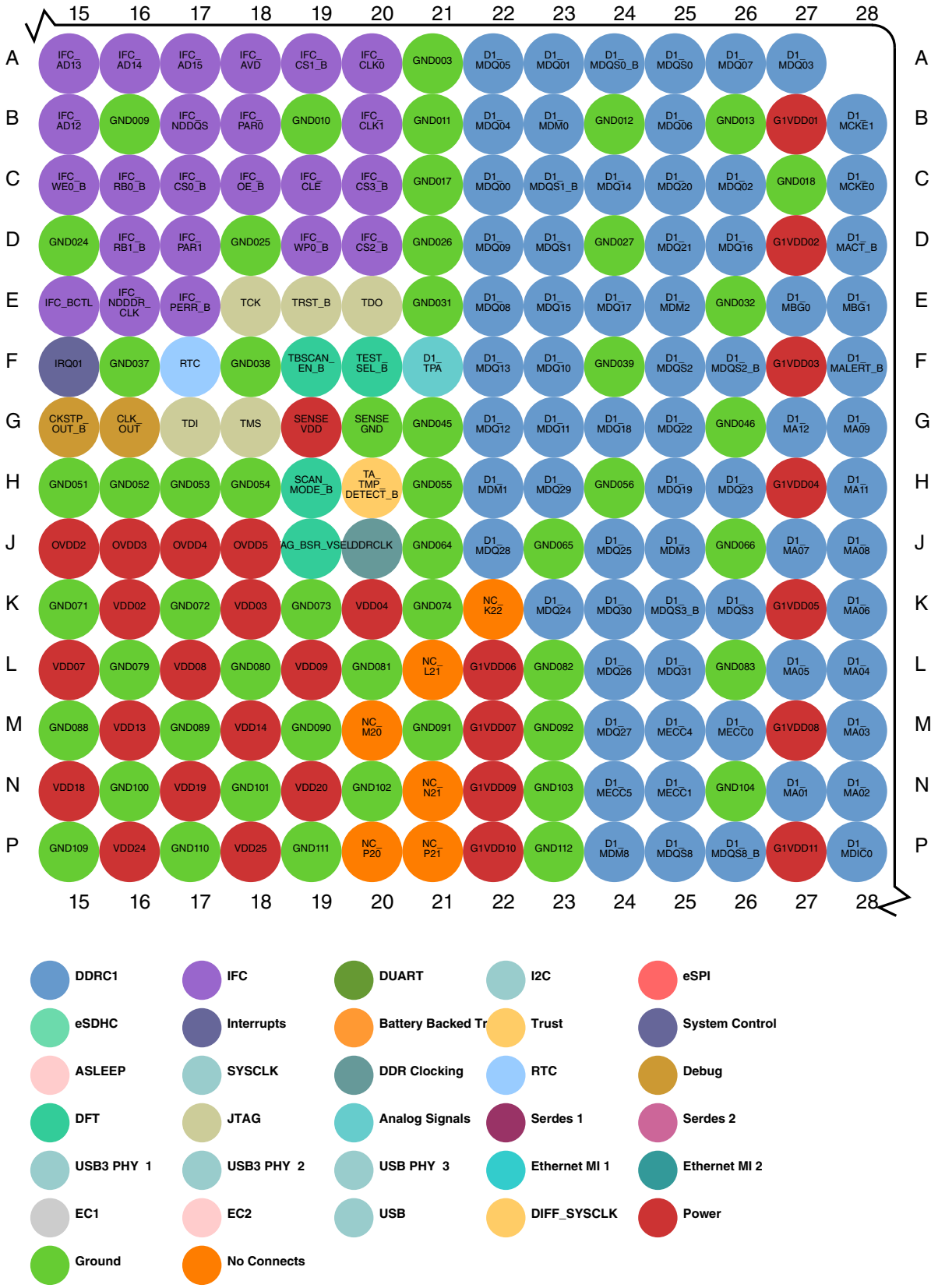


Figure 5. Detail B

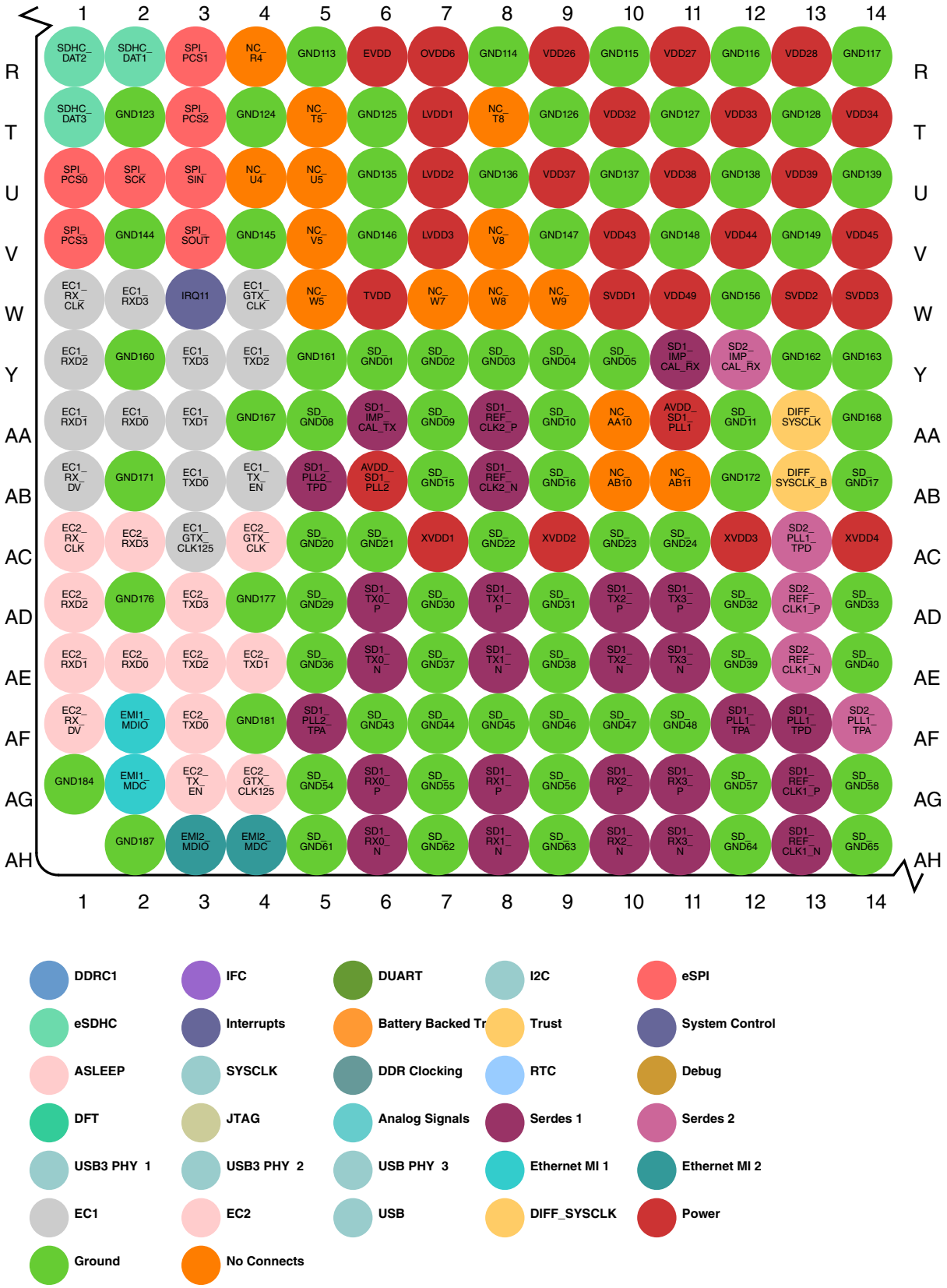


Figure 6. Detail C

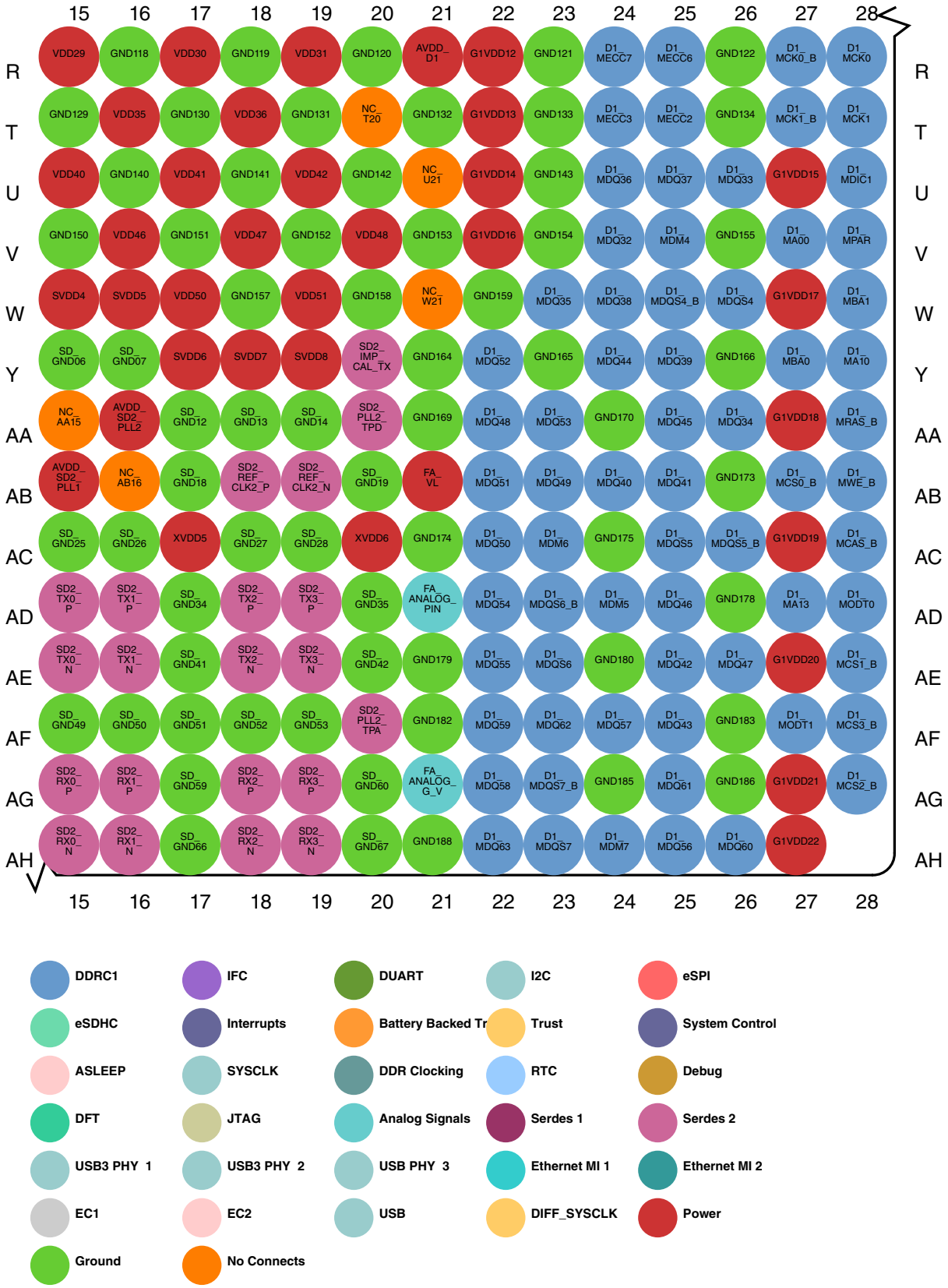


Figure 7. Detail D

2.2 Pinout list

This table provides the pinout listing for the LS1046A by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
D1_MA00	Address	V27	O	$G1V_{DD}$	---
D1_MA01	Address	N27	O	$G1V_{DD}$	---
D1_MA02	Address	N28	O	$G1V_{DD}$	---
D1_MA03	Address	M28	O	$G1V_{DD}$	---
D1_MA04	Address	L28	O	$G1V_{DD}$	---
D1_MA05	Address	L27	O	$G1V_{DD}$	---
D1_MA06	Address	K28	O	$G1V_{DD}$	---
D1_MA07	Address	J27	O	$G1V_{DD}$	---
D1_MA08	Address	J28	O	$G1V_{DD}$	---
D1_MA09	Address	G28	O	$G1V_{DD}$	---
D1_MA10	Address	Y28	O	$G1V_{DD}$	---
D1_MA11	Address	H28	O	$G1V_{DD}$	---
D1_MA12	Address	G27	O	$G1V_{DD}$	---
D1_MA13	Address	AD27	O	$G1V_{DD}$	---
D1_MACT_B	Activate	D28	O	$G1V_{DD}$	---
D1_MALERT_B	Alert	F28	I	$G1V_{DD}$	1, 27
D1_MBA0	Bank Select	Y27	O	$G1V_{DD}$	---
D1_MBA1	Bank Select	W28	O	$G1V_{DD}$	---
D1_MBG0	Bank Group	E27	O	$G1V_{DD}$	---
D1_MBG1	Bank Group	E28	O	$G1V_{DD}$	---
D1_MCAS_B	Column Address Strobe / MA[15]	AC28	O	$G1V_{DD}$	---
D1_MCK0	Clock	R28	O	$G1V_{DD}$	---
D1_MCK0_B	Clock Complement	R27	O	$G1V_{DD}$	---
D1_MCK1	Clock	T28	O	$G1V_{DD}$	---
D1_MCK1_B	Clock Complement	T27	O	$G1V_{DD}$	---
D1_MCKE0	Clock Enable	C28	O	$G1V_{DD}$	2
D1_MCKE1	Clock Enable	B28	O	$G1V_{DD}$	2
D1_MCS0_B	Chip Select	AB27	O	$G1V_{DD}$	---
D1_MCS1_B	Chip Select	AE28	O	$G1V_{DD}$	---
D1_MCS2_B	Chip Select / MCID[0]	AG28	O	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MCS3_B	Chip Select / MCID[1]	AF28	O	$G1V_{DD}$	---
D1_MDIC0	Driver Impedence Calibration	P28	IO	$G1V_{DD}$	3
D1_MDIC1	Driver Impedence Calibration	U28	IO	$G1V_{DD}$	3
D1_MDM0	Data Mask	B23	IO	$G1V_{DD}$	---
D1_MDM1	Data Mask	H22	IO	$G1V_{DD}$	---
D1_MDM2	Data Mask	E25	IO	$G1V_{DD}$	---
D1_MDM3	Data Mask	J25	IO	$G1V_{DD}$	---
D1_MDM4	Data Mask	V25	IO	$G1V_{DD}$	---
D1_MDM5	Data Mask	AD24	IO	$G1V_{DD}$	---
D1_MDM6	Data Mask	AC23	IO	$G1V_{DD}$	---
D1_MDM7	Data Mask	AH24	IO	$G1V_{DD}$	---
D1_MDM8	Data Mask	P24	IO	$G1V_{DD}$	---
D1_MDQ00	Data	C22	IO	$G1V_{DD}$	---
D1_MDQ01	Data	A23	IO	$G1V_{DD}$	---
D1_MDQ02	Data	C26	IO	$G1V_{DD}$	---
D1_MDQ03	Data	A27	IO	$G1V_{DD}$	---
D1_MDQ04	Data	B22	IO	$G1V_{DD}$	---
D1_MDQ05	Data	A22	IO	$G1V_{DD}$	---
D1_MDQ06	Data	B25	IO	$G1V_{DD}$	---
D1_MDQ07	Data	A26	IO	$G1V_{DD}$	---
D1_MDQ08	Data	E22	IO	$G1V_{DD}$	---
D1_MDQ09	Data	D22	IO	$G1V_{DD}$	---
D1_MDQ10	Data	F23	IO	$G1V_{DD}$	---
D1_MDQ11	Data	G23	IO	$G1V_{DD}$	---
D1_MDQ12	Data	G22	IO	$G1V_{DD}$	---
D1_MDQ13	Data	F22	IO	$G1V_{DD}$	---
D1_MDQ14	Data	C24	IO	$G1V_{DD}$	---
D1_MDQ15	Data	E23	IO	$G1V_{DD}$	---
D1_MDQ16	Data	D26	IO	$G1V_{DD}$	---
D1_MDQ17	Data	E24	IO	$G1V_{DD}$	---
D1_MDQ18	Data	G24	IO	$G1V_{DD}$	---
D1_MDQ19	Data	H25	IO	$G1V_{DD}$	---
D1_MDQ20	Data	C25	IO	$G1V_{DD}$	---
D1_MDQ21	Data	D25	IO	$G1V_{DD}$	---
D1_MDQ22	Data	G25	IO	$G1V_{DD}$	---
D1_MDQ23	Data	H26	IO	$G1V_{DD}$	---
D1_MDQ24	Data	K23	IO	$G1V_{DD}$	---
D1_MDQ25	Data	J24	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ26	Data	L24	IO	$G1V_{DD}$	---
D1_MDQ27	Data	M24	IO	$G1V_{DD}$	---
D1_MDQ28	Data	J22	IO	$G1V_{DD}$	---
D1_MDQ29	Data	H23	IO	$G1V_{DD}$	---
D1_MDQ30	Data	K24	IO	$G1V_{DD}$	---
D1_MDQ31	Data	L25	IO	$G1V_{DD}$	---
D1_MDQ32	Data	V24	IO	$G1V_{DD}$	---
D1_MDQ33	Data	U26	IO	$G1V_{DD}$	---
D1_MDQ34	Data	AA26	IO	$G1V_{DD}$	---
D1_MDQ35	Data	W23	IO	$G1V_{DD}$	---
D1_MDQ36	Data	U24	IO	$G1V_{DD}$	---
D1_MDQ37	Data	U25	IO	$G1V_{DD}$	---
D1_MDQ38	Data	W24	IO	$G1V_{DD}$	---
D1_MDQ39	Data	Y25	IO	$G1V_{DD}$	---
D1_MDQ40	Data	AB24	IO	$G1V_{DD}$	---
D1_MDQ41	Data	AB25	IO	$G1V_{DD}$	---
D1_MDQ42	Data	AE25	IO	$G1V_{DD}$	---
D1_MDQ43	Data	AF25	IO	$G1V_{DD}$	---
D1_MDQ44	Data	Y24	IO	$G1V_{DD}$	---
D1_MDQ45	Data	AA25	IO	$G1V_{DD}$	---
D1_MDQ46	Data	AD25	IO	$G1V_{DD}$	---
D1_MDQ47	Data	AE26	IO	$G1V_{DD}$	---
D1_MDQ48	Data	AA22	IO	$G1V_{DD}$	---
D1_MDQ49	Data	AB23	IO	$G1V_{DD}$	---
D1_MDQ50	Data	AC22	IO	$G1V_{DD}$	---
D1_MDQ51	Data	AB22	IO	$G1V_{DD}$	---
D1_MDQ52	Data	Y22	IO	$G1V_{DD}$	---
D1_MDQ53	Data	AA23	IO	$G1V_{DD}$	---
D1_MDQ54	Data	AD22	IO	$G1V_{DD}$	---
D1_MDQ55	Data	AE22	IO	$G1V_{DD}$	---
D1_MDQ56	Data	AH25	IO	$G1V_{DD}$	---
D1_MDQ57	Data	AF24	IO	$G1V_{DD}$	---
D1_MDQ58	Data	AG22	IO	$G1V_{DD}$	---
D1_MDQ59	Data	AF22	IO	$G1V_{DD}$	---
D1_MDQ60	Data	AH26	IO	$G1V_{DD}$	---
D1_MDQ61	Data	AG25	IO	$G1V_{DD}$	---
D1_MDQ62	Data	AF23	IO	$G1V_{DD}$	---
D1_MDQ63	Data	AH22	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQS0	Data Strobe	A25	IO	$G1V_{DD}$	---
D1_MDQS0_B	Data Strobe	A24	IO	$G1V_{DD}$	---
D1_MDQS1	Data Strobe	D23	IO	$G1V_{DD}$	---
D1_MDQS1_B	Data Strobe	C23	IO	$G1V_{DD}$	---
D1_MDQS2	Data Strobe	F25	IO	$G1V_{DD}$	---
D1_MDQS2_B	Data Strobe	F26	IO	$G1V_{DD}$	---
D1_MDQS3	Data Strobe	K26	IO	$G1V_{DD}$	---
D1_MDQS3_B	Data Strobe	K25	IO	$G1V_{DD}$	---
D1_MDQS4	Data Strobe	W26	IO	$G1V_{DD}$	---
D1_MDQS4_B	Data Strobe	W25	IO	$G1V_{DD}$	---
D1_MDQS5	Data Strobe	AC25	IO	$G1V_{DD}$	---
D1_MDQS5_B	Data Strobe	AC26	IO	$G1V_{DD}$	---
D1_MDQS6	Data Strobe	AE23	IO	$G1V_{DD}$	---
D1_MDQS6_B	Data Strobe	AD23	IO	$G1V_{DD}$	---
D1_MDQS7	Data Strobe	AH23	IO	$G1V_{DD}$	---
D1_MDQS7_B	Data Strobe	AG23	IO	$G1V_{DD}$	---
D1_MDQS8	Data Strobe	P25	IO	$G1V_{DD}$	---
D1_MDQS8_B	Data Strobe	P26	IO	$G1V_{DD}$	---
D1_MECC0	Error Correcting Code	M26	IO	$G1V_{DD}$	---
D1_MECC1	Error Correcting Code	N25	IO	$G1V_{DD}$	---
D1_MECC2	Error Correcting Code	T25	IO	$G1V_{DD}$	---
D1_MECC3	Error Correcting Code	T24	IO	$G1V_{DD}$	---
D1_MECC4	Error Correcting Code	M25	IO	$G1V_{DD}$	---
D1_MECC5	Error Correcting Code	N24	IO	$G1V_{DD}$	---
D1_MECC6	Error Correcting Code	R25	IO	$G1V_{DD}$	---
D1_MECC7	Error Correcting Code	R24	IO	$G1V_{DD}$	---
D1_MODT0	On Die Termination	AD28	O	$G1V_{DD}$	2
D1_MODT1	On Die Termination / MCID[2]	AF27	O	$G1V_{DD}$	2
D1_MPAR	Address Parity Out	V28	O	$G1V_{DD}$	---
D1_MRAS_B	Row Address Strobe / MA[16]	AA28	O	$G1V_{DD}$	---
D1_MWE_B	Write Enable / MA[14]	AB28	O	$G1V_{DD}$	---
Integrated Flash Controller					
IFC_A16/QSPI_A_CS0	IFC Address	D8	O	OV_{DD}	1, 5
IFC_A17/QSPI_A_CS1	IFC Address	C8	O	OV_{DD}	1, 5
IFC_A18/QSPI_A_SCK	IFC Address	C9	O	OV_{DD}	1, 5
IFC_A19/QSPI_B_CS0	IFC Address	D10	O	OV_{DD}	1, 5
IFC_A20/QSPI_B_CS1	IFC Address	C10	O	OV_{DD}	1, 5

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_A21/QSPI_B_SCK/ cfg_dram_type	IFC Address	C11	O	OV_{DD}	1, 15
IFC_A22/QSPI_A_DATA0/ IFC_WP1_B	IFC Address	D11	O	OV_{DD}	1
IFC_A23/QSPI_A_DATA1/ IFC_WP2_B	IFC Address	C12	O	OV_{DD}	1
IFC_A24/QSPI_A_DATA2/ IFC_WP3_B	IFC Address	D13	O	OV_{DD}	1
IFC_A25/GPIO2_25/ QSPI_A_DATA3/FTM5_CH0/ IFC_CS4_B/IFC_RB2_B	IFC Address	C13	O	OV_{DD}	1
IFC_A26/GPIO2_26/ FTM5_CH1/IFC_CS5_B/ IFC_RB3_B	IFC Address	D14	O	OV_{DD}	1
IFC_A27/GPIO2_27/ FTM5_EXTCLK/IFC_CS6_B	IFC Address	C14	O	OV_{DD}	1
IFC_AD00/cfg_gpinput0	IFC Address / Data	B8	IO	OV_{DD}	4
IFC_AD01/cfg_gpinput1	IFC Address / Data	A8	IO	OV_{DD}	4
IFC_AD02/cfg_gpinput2	IFC Address / Data	B9	IO	OV_{DD}	4
IFC_AD03/cfg_gpinput3	IFC Address / Data	A9	IO	OV_{DD}	4
IFC_AD04/cfg_gpinput4	IFC Address / Data	A10	IO	OV_{DD}	4
IFC_AD05/cfg_gpinput5	IFC Address / Data	B11	IO	OV_{DD}	4
IFC_AD06/cfg_gpinput6	IFC Address / Data	A11	IO	OV_{DD}	4
IFC_AD07/cfg_gpinput7	IFC Address / Data	B12	IO	OV_{DD}	4
IFC_AD08/cfg_rcw_src0	IFC Address / Data	A12	IO	OV_{DD}	4
IFC_AD09/cfg_rcw_src1	IFC Address / Data	A13	IO	OV_{DD}	4
IFC_AD10/cfg_rcw_src2	IFC Address / Data	B14	IO	OV_{DD}	4
IFC_AD11/cfg_rcw_src3	IFC Address / Data	A14	IO	OV_{DD}	4
IFC_AD12/cfg_rcw_src4	IFC Address / Data	B15	IO	OV_{DD}	4
IFC_AD13/cfg_rcw_src5	IFC Address / Data	A15	IO	OV_{DD}	4
IFC_AD14/cfg_rcw_src6	IFC Address / Data	A16	IO	OV_{DD}	4
IFC_AD15/cfg_rcw_src7	IFC Address / Data	A17	IO	OV_{DD}	4
IFC_AVD	IFC Address Valid	A18	O	OV_{DD}	1, 5
IFC_BCTL	IFC Buffer control	E15	O	OV_{DD}	---
IFC_CLE/cfg_rcw_src8	IFC Command Latch Enable / Write Enable	C19	O	OV_{DD}	1, 4
IFC_CLK0	IFC Clock	A20	O	OV_{DD}	---
IFC_CLK1	IFC Clock	B20	O	OV_{DD}	---
IFC_CS0_B	IFC Chip Select	C17	O	OV_{DD}	1, 6
IFC_CS1_B/GPIO2_10/ FTM7_CH0	IFC Chip Select	A19	O	OV_{DD}	1, 6

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_CS2_B/GPIO2_11/ FTM7_CH1	IFC Chip Select	D20	O	OV_{DD}	1, 6
IFC_CS3_B/GPIO2_12/ QSPI_B_DATA3/ FTM7_EXTCLK	IFC Chip Select	C20	O	OV_{DD}	1, 6
IFC_CS4_B/**IFC_A25**/ GPIO2_25/QSPI_A_DATA3/ FTM5_CH0/IFC_RB2_B	IFC Chip Select	C13	O	OV_{DD}	1
IFC_CS5_B/**IFC_A26**/ GPIO2_26/FTM5_CH1/ IFC_RB3_B	IFC Chip Select	D14	O	OV_{DD}	1
IFC_CS6_B/**IFC_A27**/ GPIO2_27/FTM5_EXTCLK	IFC Chip Select	C14	O	OV_{DD}	1
IFC_NDDDR_CLK	IFC NAND DDR Clock	E16	O	OV_{DD}	---
IFC_NDDQS	IFC DQS Strobe	B17	IO	OV_{DD}	---
IFC_OE_B/cfg_eng_use1	IFC Output Enable	C18	O	OV_{DD}	1, 4
IFC_PAR0/GPIO2_13/ QSPI_B_DATA0/FTM6_CH0	IFC Address & Data Parity	B18	IO	OV_{DD}	---
IFC_PAR1/GPIO2_14/ QSPI_B_DATA1/FTM6_CH1	IFC Address & Data Parity	D17	IO	OV_{DD}	---
IFC_PERR_B/GPIO2_15/ QSPI_B_DATA2/ FTM6_EXTCLK	IFC Parity Error	E17	I	OV_{DD}	1
IFC_RB0_B	IFC Ready / Busy CS0	C16	I	OV_{DD}	6
IFC_RB1_B	IFC Ready / Busy CS1	D16	I	OV_{DD}	6
IFC_RB2_B/**IFC_A25**/ GPIO2_25/QSPI_A_DATA3/ FTM5_CH0/IFC_CS4_B	IFC Ready/Busy CS 2	C13	I	OV_{DD}	1
IFC_RB3_B/**IFC_A26**/ GPIO2_26/FTM5_CH1/ IFC_CS5_B	IFC Ready/Busy CS 3	D14	I	OV_{DD}	1
IFC_TE/cfg_ifc_te	IFC External Transceiver Enable	E14	O	OV_{DD}	1, 4
IFC_WE0_B/cfg_eng_use0	IFC Write Enable	C15	O	OV_{DD}	1, 4, 26
IFC_WP0_B/cfg_eng_use2	IFC Write Protect	D19	O	OV_{DD}	1, 4
IFC_WP1_B/**IFC_A22**/ QSPI_A_DATA0	IFC Write Protect	D11	O	OV_{DD}	1
IFC_WP2_B/**IFC_A23**/ QSPI_A_DATA1	IFC Write Protect	C12	O	OV_{DD}	1
IFC_WP3_B/**IFC_A24**/ QSPI_A_DATA2	IFC Write Protect	D13	O	OV_{DD}	1
DUART					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
UART1_CTS_B/GPIO1_21/ UART3_SIN/FTM4_CH4/ LPUART2_SIN	Clear To Send	J1	I	DV_{DD}	1
UART1_RTS_B/GPIO1_19/ UART3_SOUT/ LPUART2_SOUT/FTM4_CH2	Ready to Send	J2	O	DV_{DD}	1
UART1_SIN/GPIO1_17	Receive Data	H2	I	DV_{DD}	1
UART1_SOUT/GPIO1_15	Transmit Data	H1	O	DV_{DD}	1
UART2_CTS_B/GPIO1_22/ UART4_SIN/FTM4_CH5/ LPUART1_CTS_B/ LPUART4_SIN	Clear To Send	M2	I	DV_{DD}	1
UART2_RTS_B/GPIO1_20/ UART4_SOUT/ LPUART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	Ready to Send	L1	O	DV_{DD}	1
UART2_SIN/GPIO1_18/ FTM4_CH1/LPUART1_SIN	Receive Data	K1	I	DV_{DD}	1
UART2_SOUT/GPIO1_16/ LPUART1_SOUT/FTM4_CH0	Transmit Data	L2	O	DV_{DD}	1
UART3_SIN/**UART1_CTS_B**/ GPIO1_21/FTM4_CH4/ LPUART2_SIN	Receive Data	J1	I	DV_{DD}	1
UART3_SOUT/ **UART1_RTS_B**/GPIO1_19/ LPUART2_SOUT/FTM4_CH2	Transmit Data	J2	O	DV_{DD}	1
UART4_SIN/**UART2_CTS_B**/ GPIO1_22/FTM4_CH5/ LPUART1_CTS_B/ LPUART4_SIN	Receive Data	M2	I	DV_{DD}	1
UART4_SOUT/ **UART2_RTS_B**/GPIO1_20/ LPUART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	Transmit Data	L1	O	DV_{DD}	1
I2C					
IIC1_SCL	Serial Clock (supports PBL)	N1	IO	DV_{DD}	7, 8
IIC1_SDA	Serial Data (supports PBL)	M1	IO	DV_{DD}	7, 8
IIC2_SCL/GPIO4_2/ SDHC_CD_B/FTM3_QD_PHA	Serial Clock	K3	IO	DV_{DD}	7, 8
IIC2_SDA/GPIO4_3/ SDHC_WP/FTM3_QD_PHB	Serial Data	L3	IO	DV_{DD}	7, 8
IIC3_SCL/GPIO4_10/EVT5_B/ USB2_DRVVBUS/FTM8_CH0	Serial Clock	L4	IO	DV_{DD}	7, 8
IIC3_SDA/GPIO4_11/EVT6_B/ USB2_PWRFAULT/ FTM8_CH1	Serial Data	M4	IO	DV_{DD}	7, 8

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IIC4_SCL/GPIO4_12/EVT7_B/ USB3_DRVVBUS/ FTM3_FAULT	Serial Clock	M3	IO	DV_{DD}	7, 8
IIC4_SDA/GPIO4_13/EVT8_B/ USB3_PWRFAULT/ FTM3_EXTCLK	Serial Data	N3	IO	DV_{DD}	7, 8
SPI Interface					
SPI_PCS0/GPIO2_00/ SDHC_DAT4/SDHC_VS	SPI Chip Select	U1	O	OV_{DD}	1
SPI_PCS1/GPIO2_01/ SDHC_DAT5/ SDHC_CMD_DIR	SPI Chip Select	R3	O	OV_{DD}	1
SPI_PCS2/GPIO2_02/ SDHC_DAT6/ SDHC_DAT0_DIR	SPI Chip Select	T3	O	OV_{DD}	1
SPI_PCS3/GPIO2_03/ SDHC_DAT7/ SDHC_DAT123_DIR	SPI Chip Select	V1	O	OV_{DD}	1
SPI_SCK	SPI Clock	U2	O	OV_{DD}	1
SPI_SIN/ SDHC_CLK_SYNC_IN	Master In Slave Out	U3	I	OV_{DD}	1
SPI_SOUT/ SDHC_CLK_SYNC_OUT	Master Out Slave In	V3	IO	OV_{DD}	---
eSDHC					
SDHC_CD_B/**IIC2_SCL**/ GPIO4_2/FTM3_QD_PHA	Command	K3	I	DV_{DD}	1
SDHC_CLK/GPIO2_09/ LPUART3_CTS_B/ LPUART6_SIN/ FTM4_QD_PHB	Host to Card Clock	P3	O	EV_{DD}	1
SDHC_CLK_SYNC_IN/ **SPI_SIN**	IN	U3	I	OV_{DD}	1
SDHC_CLK_SYNC_OUT/ **SPI_SOUT**	OUT	V3	O	OV_{DD}	1
SDHC_CMD/GPIO2_04/ LPUART3_SOUT/FTM4_CH6	Command/Response	P2	IO	EV_{DD}	---
SDHC_CMD_DIR/**SPI_PCS1**/ GPIO2_01/SDHC_DAT5	DIR	R3	O	OV_{DD}	1
SDHC_DAT0/GPIO2_05/ FTM4_CH7/LPUART3_SIN	Data	P1	IO	EV_{DD}	---
SDHC_DAT0_DIR/**SPI_PCS2**/ GPIO2_02/SDHC_DAT6	DIR	T3	O	OV_{DD}	1
SDHC_DAT1/GPIO2_06/ LPUART5_SOUT/	Data	R2	IO	EV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
FTM4_FAULT/ LPUART2_RTS_B					
SDHC_DAT123_DIR/ **SPI_PCS3**/GPIO2_03/ SDHC_DAT7	DIR	V1	O	OV_{DD}	1
SDHC_DAT2/GPIO2_07/ LPUART2_CTS_B/ LPUART5_SIN/ FTM4_EXTCLK	Data	R1	IO	EV_{DD}	---
SDHC_DAT3/GPIO2_08/ LPUART6_SOUT/ FTM4_QD_PHA/ LPUART3_RTS_B	Data	T1	IO	EV_{DD}	---
SDHC_DAT4/**SPI_PCS0**/ GPIO2_00/SDHC_VS	Data	U1	IO	OV_{DD}	---
SDHC_DAT5/**SPI_PCS1**/ GPIO2_01/SDHC_CMD_DIR	Data	R3	IO	OV_{DD}	---
SDHC_DAT6/**SPI_PCS2**/ GPIO2_02/SDHC_DAT0_DIR	Data	T3	IO	OV_{DD}	---
SDHC_DAT7/**SPI_PCS3**/ GPIO2_03/ SDHC_DAT123_DIR	Data	V1	IO	OV_{DD}	---
SDHC_VS/**SPI_PCS0**/ GPIO2_00/SDHC_DAT4	VS	U1	O	OV_{DD}	1
SDHC_WP/**IIC2_SDA**/ GPIO4_3/FTM3_QD_PHB	Write Protect	L3	I	DV_{DD}	1
Programmable Interrupt Controller					
EVT9_B	Event 9	G7	IO	OV_{DD}	1, 6, 7
IRQ00	External Interrupt	F11	I	OV_{DD}	1
IRQ01	External Interrupt	F15	I	OV_{DD}	1
IRQ02	External Interrupt	H7	I	OV_{DD}	1
IRQ03/GPIO1_23/FTM3_CH7	External Interrupt	J3	I	DV_{DD}	1
IRQ04/GPIO1_24/FTM3_CH0	External Interrupt	J4	I	DV_{DD}	1
IRQ05/GPIO1_25/FTM3_CH1	External Interrupt	J5	I	DV_{DD}	1
IRQ06/GPIO1_26/FTM3_CH2	External Interrupt	K5	I	DV_{DD}	1
IRQ07/GPIO1_27/FTM3_CH3	External Interrupt	L5	I	DV_{DD}	1
IRQ08/GPIO1_28/FTM3_CH4	External Interrupt	M5	I	DV_{DD}	1
IRQ09/GPIO1_29/FTM3_CH5	External Interrupt	N5	I	DV_{DD}	1
IRQ10/GPIO1_30/FTM3_CH6	External Interrupt	P4	I	DV_{DD}	1
IRQ11/GPIO1_31	External Interrupt	W3	I	LV_{DD}	1
Battery Backed Trust					
TA_BB_TMP_DETECT_B	Battery Backed Tamper Detect	H12	I	$TA_BB_V_{DD}$	---
Trust					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
TA_TMP_DETECT_B	Tamper Detect	H20	I	OV_{DD}	1
System Control					
HRESET_B	Hard Reset	F8	IO	OV_{DD}	7, 28
PORESET_B	Power On Reset	F9	I	OV_{DD}	---
RESET_REQ_B	Reset Request	F10	O	OV_{DD}	1, 5
Power Management					
ASLEEP/GPIO1_13	Asleep	E9	O	OV_{DD}	1
SYSCLK					
SYSCLK	System Clock	G14	I	OV_{DD}	22
DDR Clocking					
DDRCLK	DDR Controller Clock	J20	I	OV_{DD}	22
RTC					
RTC/GPIO1_14	Real Time Clock	F17	I	OV_{DD}	1
Debug					
CKSTP_OUT_B	RSVD	G15	-	OV_{DD}	6, 7
CLK_OUT	Clock Out	G16	O	OV_{DD}	---
EVT0_B	Event 0	E10	IO	OV_{DD}	9
EVT1_B	Event 1	E13	IO	OV_{DD}	---
EVT2_B	Event 2	E8	IO	OV_{DD}	---
EVT3_B	Event 3	E12	IO	OV_{DD}	---
EVT4_B	Event 4	E11	IO	OV_{DD}	---
EVT5_B/**IIC3_SCL**/GPIO4_10/ USB2_DRVVBUS/FTM8_CH0	Event 5	L4	IO	DV_{DD}	---
EVT6_B/**IIC3_SDA**/GPIO4_11/ USB2_PWRFAULT/ FTM8_CH1	Event 6	M4	IO	DV_{DD}	---
EVT7_B/**IIC4_SCL**/GPIO4_12/ USB3_DRVVBUS/ FTM3_FAULT	Event 7	M3	IO	DV_{DD}	---
EVT8_B/**IIC4_SDA**/GPIO4_13/ USB3_PWRFAULT/ FTM3_EXTCLK	Event 8	N3	IO	DV_{DD}	---
DFT					
JTAG_BSR_VSEL	An IEEE 1149.1 JTAG Compliance Enable pin. 0: normal operation. 1: To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL.	J19	I	OV_{DD}	24, 25
SCAN_MODE_B	Reserved	H19	I	OV_{DD}	10, 25

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
TBSCAN_EN_B	An IEEE 1149.1 JTAG Compliance Enable pin. 0: To be compliant to the 1149.1 specification for boundary scan functions. The JTAG compliant state is documented in the BSDL. 1: JTAG connects to DAP controller for the Arm core debug.	F19	I	OV_{DD}	20, 25
TEST_SEL_B	Reserved	F20	I	OV_{DD}	19, 25
JTAG					
TCK	Test Clock	E18	I	OV_{DD}	---
TDI	Test Data In	G17	I	OV_{DD}	9
TDO	Test Data Out	E20	O	OV_{DD}	2
TMS	Test Mode Select	G18	I	OV_{DD}	9
TRST_B	Test Reset	E19	I	OV_{DD}	9
Analog Signals					
D1_TPA	DDR Controller 1 Test Point Analog	F21	IO		12
FA_ANALOG_G_V	Reserved	AG21	IO		15
FA_ANALOG_PIN	Reserved	AD21	IO		15
TD1_ANODE	Thermal diode anode	J13	IO		17
TD1_CATHODE	Thermal diode cathode	H13	IO		17
TH_TPA	Thermal Test Point Analog	H8	-	-	12
SerDes 1					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	Y11	I	SV_{DD}	11
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	AA6	I	XV_{DD}	16
SD1_PLL1_TPA	SerDes PLL 1 Test Point Analog	AF12	O	AVDD_SD1_PLL1	12
SD1_PLL1_TPD	SerDes Test Point Digital	AF13	O	XV_{DD}	12
SD1_PLL2_TPA	SerDes PLL 2 Test Point Analog	AF5	O	AVDD_SD1_PLL2	12
SD1_PLL2_TPD	SerDes Test Point Digital	AB5	O	XV_{DD}	12
SD1_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AH13	I	SV_{DD}	---
SD1_REF_CLK1_P	SerDes PLL 1 Reference Clock	AG13	I	SV_{DD}	---
SD1_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AB8	I	SV_{DD}	---
SD1_REF_CLK2_P	SerDes PLL 2 Reference Clock	AA8	I	SV_{DD}	---
SD1_RX0_N	SerDes Receive Data (negative)	AH6	I	SV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_RX0_P	SerDes Receive Data (positive)	AG6	I	SV_{DD}	---
SD1_RX1_N	SerDes Receive Data (negative)	AH8	I	SV_{DD}	---
SD1_RX1_P	SerDes Receive Data (positive)	AG8	I	SV_{DD}	---
SD1_RX2_N	SerDes Receive Data (negative)	AH10	I	SV_{DD}	---
SD1_RX2_P	SerDes Receive Data (positive)	AG10	I	SV_{DD}	---
SD1_RX3_N	SerDes Receive Data (negative)	AH11	I	SV_{DD}	---
SD1_RX3_P	SerDes Receive Data (positive)	AG11	I	SV_{DD}	---
SD1_TX0_N	SerDes Transmit Data (negative)	AE6	O	XV_{DD}	---
SD1_TX0_P	SerDes Transmit Data (positive)	AD6	O	XV_{DD}	---
SD1_TX1_N	SerDes Transmit Data (negative)	AE8	O	XV_{DD}	---
SD1_TX1_P	SerDes Transmit Data (positive)	AD8	O	XV_{DD}	---
SD1_TX2_N	SerDes Transmit Data (negative)	AE10	O	XV_{DD}	---
SD1_TX2_P	SerDes Transmit Data (positive)	AD10	O	XV_{DD}	---
SD1_TX3_N	SerDes Transmit Data (negative)	AE11	O	XV_{DD}	---
SD1_TX3_P	SerDes Transmit Data (positive)	AD11	O	XV_{DD}	---
SerDes 2					
SD2_IMP_CAL_RX	SerDes Receive Impedence Calibration	Y12	I	SV_{DD}	11
SD2_IMP_CAL_TX	SerDes Transmit Impedance Calibration	Y20	I	XV_{DD}	16
SD2_PLL1_TPA	SerDes PLL 1 Test Point Analog	AF14	O	AVDD_SD2_PLL1	12
SD2_PLL1_TPD	SerDes Test Point Digital	AC13	O	XV_{DD}	12
SD2_PLL2_TPA	SerDes PLL 2 Test Point Analog	AF20	O	AVDD_SD2_PLL2	12
SD2_PLL2_TPD	SerDes Test Point Digital	AA20	O	XV_{DD}	12
SD2_REF_CLK1_N	SerDes PLL 1 Reference Clock Complement	AE13	I	SV_{DD}	---
SD2_REF_CLK1_P	SerDes PLL 1 Reference Clock	AD13	I	SV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD2_REF_CLK2_N	SerDes PLL 2 Reference Clock Complement	AB19	I	SV_{DD}	---
SD2_REF_CLK2_P	SerDes PLL 2 Reference Clock	AB18	I	SV_{DD}	---
SD2_RX0_N	SerDes Receive Data (negative)	AH15	I	SV_{DD}	---
SD2_RX0_P	SerDes Receive Data (positive)	AG15	I	SV_{DD}	---
SD2_RX1_N	SerDes Receive Data (negative)	AH16	I	SV_{DD}	---
SD2_RX1_P	SerDes Receive Data (positive)	AG16	I	SV_{DD}	---
SD2_RX2_N	SerDes Receive Data (negative)	AH18	I	SV_{DD}	---
SD2_RX2_P	SerDes Receive Data (positive)	AG18	I	SV_{DD}	---
SD2_RX3_N	SerDes Receive Data (negative)	AH19	I	SV_{DD}	---
SD2_RX3_P	SerDes Receive Data (positive)	AG19	I	SV_{DD}	---
SD2_TX0_N	SerDes Transmit Data (negative)	AE15	O	XV_{DD}	---
SD2_TX0_P	SerDes Transmit Data (positive)	AD15	O	XV_{DD}	---
SD2_TX1_N	SerDes Transmit Data (negative)	AE16	O	XV_{DD}	---
SD2_TX1_P	SerDes Transmit Data (positive)	AD16	O	XV_{DD}	---
SD2_TX2_N	SerDes Transmit Data (negative)	AE18	O	XV_{DD}	---
SD2_TX2_P	SerDes Transmit Data (positive)	AD18	O	XV_{DD}	---
SD2_TX3_N	SerDes Transmit Data (negative)	AE19	O	XV_{DD}	---
SD2_TX3_P	SerDes Transmit Data (positive)	AD19	O	XV_{DD}	---
USB3 PHY #1					
USB1_D_M	USB PHY HS Data (-)	E6	IO	-	---
USB1_D_P	USB PHY HS Data (+)	F6	IO	-	---
USB1_ID	USB PHY ID Detect	F5	I	-	---
USB1_RESREF	USB PHY Impedance Calibration	G3	IO	-	18
USB1_RX_M	USB PHY SS Receive Data (-)	E4	I	-	---
USB1_RX_P	USB PHY SS Receive Data (+)	E3	I	-	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB1_TX_M	USB PHY SS Transmit Data (-)	F2	O	-	---
USB1_TX_P	USB PHY SS Transmit Data (+)	F1	O	-	---
USB1_VBUS	USB PHY VBUS	E7	I	-	---
USB3 PHY #2					
USB2_D_M	USB PHY HS Data (-)	C6	IO	-	---
USB2_D_P	USB PHY HS Data (+)	D6	IO	-	---
USB2_ID	USB PHY ID Detect	D5	I	-	---
USB2_RESREF	USB PHY Impedance Calibration	G4	IO	-	18
USB2_RX_M	USB PHY SS Receive Data (-)	C4	I	-	---
USB2_RX_P	USB PHY SS Receive Data (+)	C3	I	-	---
USB2_TX_M	USB PHY SS Transmit Data (-)	D2	O	-	---
USB2_TX_P	USB PHY SS Transmit Data (+)	D1	O	-	---
USB2_VBUS	USB PHY VBUS	C7	I	-	---
USB PHY #3					
USB3_D_M	USB PHY HS Data (-)	A6	IO	-	---
USB3_D_P	USB PHY HS Data (+)	B6	IO	-	---
USB3_ID	USB PHY ID Detect	B5	I	-	---
USB3_RESREF	USB PHY Impedance Calibration	G5	IO	-	18
USB3_RX_M	USB PHY SS Receive Data (-)	A4	I	-	---
USB3_RX_P	USB PHY SS Receive Data (+)	A3	I	-	---
USB3_TX_M	USB PHY SS Transmit Data (-)	B2	O	-	---
USB3_TX_P	USB PHY SS Transmit Data (+)	B1	O	-	---
USB3_VBUS	USB PHY VBUS	A7	I	-	---
Ethernet Management Interface 1					
EMI1_MDC/GPIO3_00	Management Data Clock	AG2	O	LV_{DD}	1
EMI1_MDIO/GPIO3_01	Management Data In/Out	AF2	IO	LV_{DD}	---
Ethernet Management Interface 2					
EMI2_MDC/GPIO4_00	Management Data Clock	AH4	O	TV_{DD}	1
EMI2_MDIO/GPIO4_01	Management Data In/Out	AH3	IO	TV_{DD}	---
Ethernet Controller 1					
EC1_GTX_CLK/GPIO3_07/ FTM1_EXTCLK	Transmit Clock Out	W4	O	LV_{DD}	1
EC1_GTX_CLK125/GPIO3_08	Reference Clock	AC3	I	LV_{DD}	1
EC1_RXD0/GPIO3_12/ FTM1_CH0	Receive Data	AA2	I	LV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC1_RXD1/GPIO3_11/ FTM1_CH1	Receive Data	AA1	I	LV_{DD}	1
EC1_RXD2/GPIO3_10/ FTM1_CH6	Receive Data	Y1	I	LV_{DD}	1
EC1_RXD3/GPIO3_09/ FTM1_CH4	Receive Data	W2	I	LV_{DD}	1
EC1_RX_CLK/GPIO3_13/ FTM1_QD_PHA	Receive Clock	W1	I	LV_{DD}	1
EC1_RX_DV/GPIO3_14/ FTM1_QD_PHB	Receive Data Valid	AB1	I	LV_{DD}	1
EC1_TXD0/GPIO3_05/ FTM1_CH2	Transmit Data	AB3	O	LV_{DD}	1
EC1_TXD1/GPIO3_04/ FTM1_CH3	Transmit Data	AA3	O	LV_{DD}	1
EC1_TXD2/GPIO3_03/ FTM1_CH7	Transmit Data	Y4	O	LV_{DD}	1
EC1_TXD3/GPIO3_02/ FTM1_CH5	Transmit Data	Y3	O	LV_{DD}	1
EC1_TX_EN/GPIO3_06/ FTM1_FAULT	Transmit Enable	AB4	O	LV_{DD}	1, 14
Ethernet Controller 2					
EC2_GTX_CLK/GPIO3_20/ FTM2_EXTCLK	Transmit Clock Out	AC4	O	LV_{DD}	1
EC2_GTX_CLK125/GPIO3_21	Reference Clock	AG4	I	LV_{DD}	1
EC2_RXD0/GPIO3_25/ TSEC_1588_TRIG_IN2/ FTM2_CH0	Receive Data	AE2	I	LV_{DD}	1
EC2_RXD1/GPIO3_24/ TSEC_1588_PULSE_OUT1/ FTM2_CH1	Receive Data	AE1	I	LV_{DD}	1
EC2_RXD2/GPIO3_23/ FTM2_CH6	Receive Data	AD1	I	LV_{DD}	1
EC2_RXD3/GPIO3_22/ FTM2_CH4	Receive Data	AC2	I	LV_{DD}	1
EC2_RX_CLK/GPIO3_26/ TSEC_1588_CLK_IN/ FTM2_QD_PHA	Receive Clock	AC1	I	LV_{DD}	1
EC2_RX_DV/GPIO3_27/ TSEC_1588_TRIG_IN1/ FTM2_QD_PHB	Receive Data Valid	AF1	I	LV_{DD}	1
EC2_TXD0/GPIO3_18/ TSEC_1588_PULSE_OUT2/ FTM2_CH2	Transmit Data	AF3	O	LV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC2_TXD1/GPIO3_17/ TSEC_1588_CLK_OUT/ FTM2_CH3	Transmit Data	AE4	O	LV_{DD}	1
EC2_TXD2/GPIO3_16/ TSEC_1588_ALARM_OUT1/ FTM2_CH7	Transmit Data	AE3	O	LV_{DD}	1
EC2_TXD3/GPIO3_15/ TSEC_1588_ALARM_OUT2/ FTM2_CH5	Transmit Data	AD3	O	LV_{DD}	1
EC2_TX_EN/GPIO3_19/ FTM2_FAULT	Transmit Enable	AG3	O	LV_{DD}	1, 14
USB					
USB2_DRVVBUS/**IIC3_SCL**/ GPIO4_10/EVT5_B/ FTM8_CH0	DRV VBus	L4	O	DV_{DD}	1
USB2_PWRFAULT/**IIC3_SDA**/ GPIO4_11/EVT6_B/ FTM8_CH1	PWR Fault	M4	I	DV_{DD}	1
USB3_DRVVBUS/**IIC4_SCL**/ GPIO4_12/EVT7_B/ FTM3_FAULT	DRV Bus	M3	O	DV_{DD}	1
USB3_PWRFAULT/**IIC4_SDA**/ GPIO4_13/EVT8_B/ FTM3_EXTCLK	PWR Fault	N3	I	DV_{DD}	1
USB_DRVVBUS/GPIO4_29	USB_DRVVBUS	H6	O	DV_{DD}	1
USB_PWRFAULT/GPIO4_30	USB_PWRFAULT	G6	I	DV_{DD}	1
DSYSCLK					
DIFF_SYSCLK	Single Source System Clock Differential (positive)	AA13	I	OV_{DD}	21
DIFF_SYSCLK_B	Single Source System Clock Differential (negative)	AB13	I	OV_{DD}	21
Power-On-Reset Configuration					
cfg_dram_type/**IFC_A21**/ QSPI_B_SCK	Power-on-Reset Configuration	C11	I	OV_{DD}	1, 15
cfg_eng_use0/**IFC_WE0_B**	Power-on-Reset Configuration	C15	I	OV_{DD}	1, 4, 26
cfg_eng_use1/**IFC_OE_B**	Power-on-Reset Configuration	C18	I	OV_{DD}	1, 4
cfg_eng_use2/**IFC_WP0_B**	Power-on-Reset Configuration	D19	I	OV_{DD}	1, 4
cfg_gpinput0/**IFC_AD00**	Power-on-Reset Configuration	B8	I	OV_{DD}	1, 4
cfg_gpinput1/**IFC_AD01**	Power-on-Reset Configuration	A8	I	OV_{DD}	1, 4
cfg_gpinput2/**IFC_AD02**	Power-on-Reset Configuration	B9	I	OV_{DD}	1, 4
cfg_gpinput3/**IFC_AD03**	Power-on-Reset Configuration	A9	I	OV_{DD}	1, 4
cfg_gpinput4/**IFC_AD04**	Power-on-Reset Configuration	A10	I	OV_{DD}	1, 4
cfg_gpinput5/**IFC_AD05**	Power-on-Reset Configuration	B11	I	OV_{DD}	1, 4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
cfg_gpinput6/**IFC_AD06**	Power-on-Reset Configuration	A11	I	OV_{DD}	1, 4
cfg_gpinput7/**IFC_AD07**	Power-on-Reset Configuration	B12	I	OV_{DD}	1, 4
cfg_ifc_te/**IFC_TE**	Power-on-Reset Configuration	E14	I	OV_{DD}	1, 4
cfg_rcw_src0/**IFC_AD08**	Power-on-Reset Configuration	A12	I	OV_{DD}	1, 4
cfg_rcw_src1/**IFC_AD09**	Power-on-Reset Configuration	A13	I	OV_{DD}	1, 4
cfg_rcw_src2/**IFC_AD10**	Power-on-Reset Configuration	B14	I	OV_{DD}	1, 4
cfg_rcw_src3/**IFC_AD11**	Power-on-Reset Configuration	A14	I	OV_{DD}	1, 4
cfg_rcw_src4/**IFC_AD12**	Power-on-Reset Configuration	B15	I	OV_{DD}	1, 4
cfg_rcw_src5/**IFC_AD13**	Power-on-Reset Configuration	A15	I	OV_{DD}	1, 4
cfg_rcw_src6/**IFC_AD14**	Power-on-Reset Configuration	A16	I	OV_{DD}	1, 4
cfg_rcw_src7/**IFC_AD15**	Power-on-Reset Configuration	A17	I	OV_{DD}	1, 4
cfg_rcw_src8/**IFC_CLE**	Power-on-Reset Configuration	C19	I	OV_{DD}	1, 4
QSPI					
QSPI_A_CS0/**IFC_A16**	Chip Select	D8	O	OV_{DD}	1, 5
QSPI_A_CS1/**IFC_A17**	CS1	C8	O	OV_{DD}	1, 5
QSPI_A_DATA0/**IFC_A22**/ IFC_WP1_B	DATA0	D11	IO	OV_{DD}	---
QSPI_A_DATA1/**IFC_A23**/ IFC_WP2_B	DATA1	C12	IO	OV_{DD}	---
QSPI_A_DATA2/**IFC_A24**/ IFC_WP3_B	DATA2	D13	IO	OV_{DD}	---
QSPI_A_DATA3/**IFC_A25**/ GPIO2_25/FTM5_CH0/ IFC_CS4_B/IFC_RB2_B	DATA3	C13	IO	OV_{DD}	---
QSPI_A_SCK/**IFC_A18**	SCK	C9	O	OV_{DD}	1, 5
QSPI_B_CS0/**IFC_A19**	Chip Select	D10	O	OV_{DD}	1, 5
QSPI_B_CS1/**IFC_A20**	CS1	C10	O	OV_{DD}	1, 5
QSPI_B_DATA0/**IFC_PAR0**/ GPIO2_13/FTM6_CH0	DATA0	B18	IO	OV_{DD}	---
QSPI_B_DATA1/**IFC_PAR1**/ GPIO2_14/FTM6_CH1	DATA1	D17	IO	OV_{DD}	---
QSPI_B_DATA2/ **IFC_PERR_B**/GPIO2_15/ FTM6_EXTCLK	DATA2	E17	IO	OV_{DD}	---
QSPI_B_DATA3/**IFC_CS3_B**/ GPIO2_12/FTM7_EXTCLK	DATA3	C20	IO	OV_{DD}	---
QSPI_B_SCK/**IFC_A21**/ cfg_dram_type	SCK	C11	O	OV_{DD}	1, 15
General Purpose Input/Output					
GPIO1_13/**ASLEEP**	General Purpose Input/Output	E9	O	OV_{DD}	1
GPIO1_14/**RTC**	General Purpose Input/Output	F17	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO1_15/**UART1_SOUT**	General Purpose Input/Output	H1	IO	DV_{DD}	---
GPIO1_16/**UART2_SOUT**/ LPUART1_SOUT/FTM4_CH0	General Purpose Input/Output	L2	IO	DV_{DD}	---
GPIO1_17/**UART1_SIN**	General Purpose Input/Output	H2	IO	DV_{DD}	---
GPIO1_18/**UART2_SIN**/ FTM4_CH1/LPUART1_SIN	General Purpose Input/Output	K1	IO	DV_{DD}	---
GPIO1_19/**UART1_RTS_B**/ UART3_SOUT/ LPUART2_SOUT/FTM4_CH2	General Purpose Input/Output	J2	IO	DV_{DD}	---
GPIO1_20/**UART2_RTS_B**/ UART4_SOUT/ LPUART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	General Purpose Input/Output	L1	IO	DV_{DD}	---
GPIO1_21/**UART1_CTS_B**/ UART3_SIN/FTM4_CH4/ LPUART2_SIN	General Purpose Input/Output	J1	IO	DV_{DD}	---
GPIO1_22/**UART2_CTS_B**/ UART4_SIN/FTM4_CH5/ LPUART1_CTS_B/ LPUART4_SIN	General Purpose Input/Output	M2	IO	DV_{DD}	---
GPIO1_23/**IRQ03**/FTM3_CH7	General Purpose Input/Output	J3	IO	DV_{DD}	---
GPIO1_24/**IRQ04**/FTM3_CH0	General Purpose Input/Output	J4	IO	DV_{DD}	---
GPIO1_25/**IRQ05**/FTM3_CH1	General Purpose Input/Output	J5	IO	DV_{DD}	---
GPIO1_26/**IRQ06**/FTM3_CH2	General Purpose Input/Output	K5	IO	DV_{DD}	---
GPIO1_27/**IRQ07**/FTM3_CH3	General Purpose Input/Output	L5	IO	DV_{DD}	---
GPIO1_28/**IRQ08**/FTM3_CH4	General Purpose Input/Output	M5	IO	DV_{DD}	---
GPIO1_29/**IRQ09**/FTM3_CH5	General Purpose Input/Output	N5	IO	DV_{DD}	---
GPIO1_30/**IRQ10**/FTM3_CH6	General Purpose Input/Output	P4	IO	DV_{DD}	---
GPIO1_31/**IRQ11**	General Purpose Input/Output	W3	IO	LV_{DD}	---
GPIO2_00/**SPI_PCS0**/ SDHC_DAT4/SDHC_VS	General Purpose Input/Output	U1	IO	OV_{DD}	---
GPIO2_01/**SPI_PCS1**/ SDHC_DAT5/ SDHC_CMD_DIR	General Purpose Input/Output	R3	IO	OV_{DD}	---
GPIO2_02/**SPI_PCS2**/ SDHC_DAT6/ SDHC_DAT0_DIR	General Purpose Input/Output	T3	IO	OV_{DD}	---
GPIO2_03/**SPI_PCS3**/ SDHC_DAT7/ SDHC_DAT123_DIR	General Purpose Input/Output	V1	IO	OV_{DD}	---
GPIO2_04/**SDHC_CMD**/ LPUART3_SOUT/FTM4_CH6	General Purpose Input/Output	P2	IO	EV_{DD}	---
GPIO2_05/**SDHC_DAT0**/ FTM4_CH7/LPUART3_SIN	General Purpose Input/Output	P1	IO	EV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO2_06/**SDHC_DAT1**/ LPUART5_SOUT/ FTM4_FAULT/ LPUART2_RTS_B	General Purpose Input/Output	R2	IO	EV_{DD}	---
GPIO2_07/**SDHC_DAT2**/ LPUART2_CTS_B/ LPUART5_SIN/ FTM4_EXTCLK	General Purpose Input/Output	R1	IO	EV_{DD}	---
GPIO2_08/**SDHC_DAT3**/ LPUART6_SOUT/ FTM4_QD_PHA/ LPUART3_RTS_B	General Purpose Input/Output	T1	IO	EV_{DD}	---
GPIO2_09/**SDHC_CLK**/ LPUART3_CTS_B/ LPUART6_SIN/ FTM4_QD_PHB	General Purpose Input/Output	P3	IO	EV_{DD}	---
GPIO2_10/**IFC_CS1_B**/ FTM7_CH0	General Purpose Input/Output	A19	IO	OV_{DD}	---
GPIO2_11/**IFC_CS2_B**/ FTM7_CH1	General Purpose Input/Output	D20	IO	OV_{DD}	---
GPIO2_12/**IFC_CS3_B**/ QSPI_B_DATA3/ FTM7_EXTCLK	General Purpose Input/Output	C20	IO	OV_{DD}	---
GPIO2_13/**IFC_PAR0**/ QSPI_B_DATA0/FTM6_CH0	General Purpose Input/Output	B18	IO	OV_{DD}	---
GPIO2_14/**IFC_PAR1**/ QSPI_B_DATA1/FTM6_CH1	General Purpose Input/Output	D17	IO	OV_{DD}	---
GPIO2_15/**IFC_PERR_B**/ QSPI_B_DATA2/ FTM6_EXTCLK	General Purpose Input/Output	E17	IO	OV_{DD}	---
GPIO2_25/**IFC_A25**/ QSPI_A_DATA3/FTM5_CH0/ IFC_CS4_B/IFC_RB2_B	General Purpose Input/Output	C13	IO	OV_{DD}	---
GPIO2_26/**IFC_A26**/ FTM5_CH1/IFC_CS5_B/ IFC_RB3_B	General Purpose Input/Output	D14	IO	OV_{DD}	---
GPIO2_27/**IFC_A27**/ FTM5_EXTCLK/IFC_CS6_B	General Purpose Input/Output	C14	IO	OV_{DD}	---
GPIO3_00/**EMI1_MDC**	General Purpose Input/Output	AG2	IO	LV_{DD}	---
GPIO3_01/**EMI1_MDIO**	General Purpose Input/Output	AF2	IO	LV_{DD}	---
GPIO3_02/**EC1_TXD3**/ FTM1_CH5	General Purpose Input/Output	Y3	IO	LV_{DD}	---
GPIO3_03/**EC1_TXD2**/ FTM1_CH7	General Purpose Input/Output	Y4	IO	LV_{DD}	---
GPIO3_04/**EC1_TXD1**/ FTM1_CH3	General Purpose Input/Output	AA3	IO	LV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO3_05/**EC1_TXD0**/ FTM1_CH2	General Purpose Input/Output	AB3	IO	LV_{DD}	---
GPIO3_06/**EC1_TX_EN**/ FTM1_FAULT	General Purpose Input/Output	AB4	IO	LV_{DD}	---
GPIO3_07/**EC1_GTX_CLK**/ FTM1_EXTCLK	General Purpose Input/Output	W4	IO	LV_{DD}	---
GPIO3_08/**EC1_GTX_CLK125**	General Purpose Input/Output	AC3	IO	LV_{DD}	---
GPIO3_09/**EC1_RXD3**/ FTM1_CH4	General Purpose Input/Output	W2	IO	LV_{DD}	---
GPIO3_10/**EC1_RXD2**/ FTM1_CH6	General Purpose Input/Output	Y1	IO	LV_{DD}	---
GPIO3_11/**EC1_RXD1**/ FTM1_CH1	General Purpose Input/Output	AA1	IO	LV_{DD}	---
GPIO3_12/**EC1_RXD0**/ FTM1_CH0	General Purpose Input/Output	AA2	IO	LV_{DD}	---
GPIO3_13/**EC1_RX_CLK**/ FTM1_QD_PHA	General Purpose Input/Output	W1	IO	LV_{DD}	---
GPIO3_14/**EC1_RX_DV**/ FTM1_QD_PHB	General Purpose Input/Output	AB1	IO	LV_{DD}	---
GPIO3_15/**EC2_TXD3**/ TSEC_1588_ALARM_OUT2/ FTM2_CH5	General Purpose Input/Output	AD3	IO	LV_{DD}	---
GPIO3_16/**EC2_TXD2**/ TSEC_1588_ALARM_OUT1/ FTM2_CH7	General Purpose Input/Output	AE3	IO	LV_{DD}	---
GPIO3_17/**EC2_TXD1**/ TSEC_1588_CLK_OUT/ FTM2_CH3	General Purpose Input/Output	AE4	IO	LV_{DD}	---
GPIO3_18/**EC2_TXD0**/ TSEC_1588_PULSE_OUT2/ FTM2_CH2	General Purpose Input/Output	AF3	IO	LV_{DD}	---
GPIO3_19/**EC2_TX_EN**/ FTM2_FAULT	General Purpose Input/Output	AG3	IO	LV_{DD}	---
GPIO3_20/**EC2_GTX_CLK**/ FTM2_EXTCLK	General Purpose Input/Output	AC4	IO	LV_{DD}	---
GPIO3_21/**EC2_GTX_CLK125**	General Purpose Input/Output	AG4	IO	LV_{DD}	---
GPIO3_22/**EC2_RXD3**/ FTM2_CH4	General Purpose Input/Output	AC2	IO	LV_{DD}	---
GPIO3_23/**EC2_RXD2**/ FTM2_CH6	General Purpose Input/Output	AD1	IO	LV_{DD}	---
GPIO3_24/**EC2_RXD1**/ TSEC_1588_PULSE_OUT1/ FTM2_CH1	General Purpose Input/Output	AE1	IO	LV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO3_25/**EC2_RXD0**/ TSEC_1588_TRIG_IN2/ FTM2_CH0	General Purpose Input/Output	AE2	IO	LV_{DD}	---
GPIO3_26/**EC2_RX_CLK**/ TSEC_1588_CLK_IN/ FTM2_QD_PHA	General Purpose Input/Output	AC1	IO	LV_{DD}	---
GPIO3_27/**EC2_RX_DV**/ TSEC_1588_TRIG_IN1/ FTM2_QD_PHB	General Purpose Input/Output	AF1	IO	LV_{DD}	---
GPIO4_00/**EMI2_MDC**	General Purpose Input/Output	AH4	IO	TV_{DD}	---
GPIO4_01/**EMI2_MDIO**	General Purpose Input/Output	AH3	IO	TV_{DD}	---
GPIO4_10/**IIC3_SCL**/EVT5_B/ USB2_DRVVBUS/FTM8_CH0	General Purpose Input/Output	L4	IO	DV_{DD}	---
GPIO4_11/**IIC3_SDA**/EVT6_B/ USB2_PWRFAULT/ FTM8_CH1	General Purpose Input/Output	M4	IO	DV_{DD}	---
GPIO4_12/**IIC4_SCL**/EVT7_B/ USB3_DRVVBUS/ FTM3_FAULT	General Purpose Input/Output	M3	IO	DV_{DD}	---
GPIO4_13/**IIC4_SDA**/EVT8_B/ USB3_PWRFAULT/ FTM3_EXTCLK	General Purpose Input/Output	N3	IO	DV_{DD}	---
GPIO4_2/**IIC2_SCL**/ SDHC_CD_B/FTM3_QD_PHA	General Purpose Input/Output	K3	IO	DV_{DD}	---
GPIO4_29/**USB_DRVVBUS**	General Purpose Input/Output	H6	IO	DV_{DD}	---
GPIO4_3/**IIC2_SDA**/ SDHC_WP/FTM3_QD_PHB	General Purpose Input/Output	L3	IO	DV_{DD}	---
GPIO4_30/**USB_PWRFAULT**	General Purpose Input/Output	G6	IO	DV_{DD}	---
Frequency Timer Module					
FTM1_CH0/**EC1_RXD0**/ GPIO3_12	Channel 0	AA2	IO	LV_{DD}	---
FTM1_CH1/**EC1_RXD1**/ GPIO3_11	Channel 1	AA1	IO	LV_{DD}	---
FTM1_CH2/**EC1_TXD0**/ GPIO3_05	Channel 2	AB3	IO	LV_{DD}	---
FTM1_CH3/**EC1_TXD1**/ GPIO3_04	Channel 3	AA3	IO	LV_{DD}	---
FTM1_CH4/**EC1_RXD3**/ GPIO3_09	Channel 4	W2	IO	LV_{DD}	---
FTM1_CH5/**EC1_TXD3**/ GPIO3_02	Channel 5	Y3	IO	LV_{DD}	---
FTM1_CH6/**EC1_RXD2**/ GPIO3_10	Channel 6	Y1	IO	LV_{DD}	---
FTM1_CH7/**EC1_TXD2**/ GPIO3_03	Channel 7	Y4	IO	LV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
FTM1_EXTCLK/ **EC1_GTX_CLK**/GPIO3_07	External Clock	W4	I	LV_{DD}	1
FTM1_FAULT/**EC1_TX_EN**/ GPIO3_06	Fault	AB4	I	LV_{DD}	1
FTM1_QD_PHA/ **EC1_RX_CLK**/GPIO3_13	Phase A	W1	I	LV_{DD}	1
FTM1_QD_PHB/**EC1_RX_DV**/ GPIO3_14	Phase B	AB1	I	LV_{DD}	1
FTM2_CH0/**EC2_RXD0**/ GPIO3_25/ TSEC_1588_TRIG_IN2	Channel 0	AE2	IO	LV_{DD}	---
FTM2_CH1/**EC2_RXD1**/ GPIO3_24/ TSEC_1588_PULSE_OUT1	Channel 1	AE1	IO	LV_{DD}	---
FTM2_CH2/**EC2_TXD0**/ GPIO3_18/ TSEC_1588_PULSE_OUT2	Channel 2	AF3	IO	LV_{DD}	---
FTM2_CH3/**EC2_TXD1**/ GPIO3_17/ TSEC_1588_CLK_OUT	Channel 3	AE4	IO	LV_{DD}	---
FTM2_CH4/**EC2_RXD3**/ GPIO3_22	Channel 4	AC2	IO	LV_{DD}	---
FTM2_CH5/**EC2_TXD3**/ GPIO3_15/ TSEC_1588_ALARM_OUT2	Channel 5	AD3	IO	LV_{DD}	---
FTM2_CH6/**EC2_RXD2**/ GPIO3_23	Channel 6	AD1	IO	LV_{DD}	---
FTM2_CH7/**EC2_TXD2**/ GPIO3_16/ TSEC_1588_ALARM_OUT1	Channel 7	AE3	IO	LV_{DD}	---
FTM2_EXTCLK/ **EC2_GTX_CLK**/GPIO3_20	External Clock	AC4	I	LV_{DD}	1
FTM2_FAULT/**EC2_TX_EN**/ GPIO3_19	Fault	AG3	I	LV_{DD}	1
FTM2_QD_PHA/ **EC2_RX_CLK**/GPIO3_26/ TSEC_1588_CLK_IN	Phase A	AC1	I	LV_{DD}	1
FTM2_QD_PHB/**EC2_RX_DV**/ GPIO3_27/ TSEC_1588_TRIG_IN1	Phase B	AF1	I	LV_{DD}	1
FTM3_CH0/**IRQ04**/GPIO1_24	Channel 0	J4	IO	DV_{DD}	---
FTM3_CH1/**IRQ05**/GPIO1_25	Channel 1	J5	IO	DV_{DD}	---
FTM3_CH2/**IRQ06**/GPIO1_26	Channel 2	K5	IO	DV_{DD}	---
FTM3_CH3/**IRQ07**/GPIO1_27	Channel 3	L5	IO	DV_{DD}	---
FTM3_CH4/**IRQ08**/GPIO1_28	Channel 4	M5	IO	DV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
FTM3_CH5/**IRQ09**/GPIO1_29	Channel 5	N5	IO	DV_{DD}	---
FTM3_CH6/**IRQ10**/GPIO1_30	Channel 6	P4	IO	DV_{DD}	---
FTM3_CH7/**IRQ03**/GPIO1_23	Channel 7	J3	IO	DV_{DD}	---
FTM3_EXTCLK/**IIC4_SDA**/ GPIO4_13/EVT8_B/ USB3_PWRFAULT	External Clock	N3	I	DV_{DD}	1
FTM3_FAULT/**IIC4_SCL**/ GPIO4_12/EVT7_B/ USB3_DRVVBUS	Fault	M3	I	DV_{DD}	1
FTM3_QD_PHA/**IIC2_SCL**/ GPIO4_2/SDHC_CD_B	Phase A	K3	I	DV_{DD}	1
FTM3_QD_PHB/**IIC2_SDA**/ GPIO4_3/SDHC_WP	Phase B	L3	I	DV_{DD}	1
FTM4_CH0/**UART2_SOUT**/ GPIO1_16/LPUART1_SOUT	Channel 0	L2	IO	DV_{DD}	---
FTM4_CH1/**UART2_SIN**/ GPIO1_18/LPUART1_SIN	Channel 1	K1	IO	DV_{DD}	---
FTM4_CH2/**UART1_RTS_B**/ GPIO1_19/UART3_SOUT/ LPUART2_SOUT	Channel 2	J2	IO	DV_{DD}	---
FTM4_CH3/**UART2_RTS_B**/ GPIO1_20/UART4_SOUT/ LPUART4_SOUT/ LPUART1_RTS_B	Channel 3	L1	IO	DV_{DD}	---
FTM4_CH4/**UART1_CTS_B**/ GPIO1_21/UART3_SIN/ LPUART2_SIN	Channel 4	J1	IO	DV_{DD}	---
FTM4_CH5/**UART2_CTS_B**/ GPIO1_22/UART4_SIN/ LPUART1_CTS_B/ LPUART4_SIN	Channel 5	M2	IO	DV_{DD}	---
FTM4_CH6/**SDHC_CMD**/ GPIO2_04/LPUART3_SOUT	Channel 6	P2	IO	EV_{DD}	---
FTM4_CH7/**SDHC_DAT0**/ GPIO2_05/LPUART3_SIN	Channel 7	P1	IO	EV_{DD}	---
FTM4_EXTCLK/**SDHC_DAT2**/ GPIO2_07/LPUART2_CTS_B/ LPUART5_SIN	External Clock	R1	I	EV_{DD}	1
FTM4_FAULT/**SDHC_DAT1**/ GPIO2_06/LPUART5_SOUT/ LPUART2_RTS_B	Fault	R2	I	EV_{DD}	1
FTM4_QD_PHA/**SDHC_DAT3**/ GPIO2_08/LPUART6_SOUT/ LPUART3_RTS_B	Phase A	T1	I	EV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
FTM4_QD_PHB/**SDHC_CLK**/ GPIO2_09/LPUART3_CTS_B/ LPUART6_SIN	Phase B	P3	I	EV_{DD}	1
FTM5_CH0/**IFC_A25**/ GPIO2_25/QSPI_A_DATA3/ IFC_CS4_B/IFC_RB2_B	Channel 0	C13	IO	OV_{DD}	---
FTM5_CH1/**IFC_A26**/ GPIO2_26/IFC_CS5_B/ IFC_RB3_B	Channel 1	D14	IO	OV_{DD}	---
FTM5_EXTCLK/**IFC_A27**/ GPIO2_27/IFC_CS6_B	External Clock	C14	I	OV_{DD}	1
FTM6_CH0/**IFC_PAR0**/ GPIO2_13/QSPI_B_DATA0	Channel 0	B18	IO	OV_{DD}	---
FTM6_CH1/**IFC_PAR1**/ GPIO2_14/QSPI_B_DATA1	Channel 1	D17	IO	OV_{DD}	---
FTM6_EXTCLK/**IFC_PERR_B**/ GPIO2_15/QSPI_B_DATA2	External Clock	E17	I	OV_{DD}	1
FTM7_CH0/**IFC_CS1_B**/ GPIO2_10	Channel 0	A19	IO	OV_{DD}	---
FTM7_CH1/**IFC_CS2_B**/ GPIO2_11	Channel 1	D20	IO	OV_{DD}	---
FTM7_EXTCLK/**IFC_CS3_B**/ GPIO2_12/QSPI_B_DATA3	External Clock	C20	I	OV_{DD}	1
FTM8_CH0/**IIC3_SCL**/ GPIO4_10/EVT5_B/ USB2_DRVVBUS	Channel 0	L4	IO	DV_{DD}	---
FTM8_CH1/**IIC3_SDA**/ GPIO4_11/EVT6_B/ USB2_PWRFAULT	Channel 1	M4	IO	DV_{DD}	---
LPUART					
LPUART1_CTS_B/ **UART2_CTS_B**/GPIO1_22/ UART4_SIN/FTM4_CH5/ LPUART4_SIN	Clear to send	M2	I	DV_{DD}	1
LPUART1_RTS_B/ **UART2_RTS_B**/GPIO1_20/ UART4_SOUT/ LPUART4_SOUT/FTM4_CH3	Request to send	L1	O	DV_{DD}	1
LPUART1_SIN/**UART2_SIN**/ GPIO1_18/FTM4_CH1	Receive data	K1	I	DV_{DD}	1
LPUART1_SOUT/ **UART2_SOUT**/GPIO1_16/ FTM4_CH0	Transmit data	L2	IO	DV_{DD}	---
LPUART2_CTS_B/ **SDHC_DAT2**/GPIO2_07/	Clear to send	R1	I	EV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
LPUART5_SIN/ FTM4_EXTCLK					
LPUART2_RTS_B/ **SDHC_DAT1**/GPIO2_06/ LPUART5_SOUT/ FTM4_FAULT	Request to send	R2	O	EV_{DD}	1
LPUART2_SIN/ **UART1_CTS_B**/GPIO1_21/ UART3_SIN/FTM4_CH4	Receive data	J1	I	DV_{DD}	1
LPUART2_SOUT/ **UART1_RTS_B**/GPIO1_19/ UART3_SOUT/FTM4_CH2	Transmit data	J2	IO	DV_{DD}	---
LPUART3_CTS_B/ **SDHC_CLK**/GPIO2_09/ LPUART6_SIN/ FTM4_QD_PHB	Clear to send	P3	I	EV_{DD}	1
LPUART3_RTS_B/ **SDHC_DAT3**/GPIO2_08/ LPUART6_SOUT/ FTM4_QD_PHA	Request to send	T1	O	EV_{DD}	1
LPUART3_SIN/**SDHC_DAT0**/ GPIO2_05/FTM4_CH7	Receive data	P1	I	EV_{DD}	1
LPUART3_SOUT/ **SDHC_CMD**/GPIO2_04/ FTM4_CH6	Transmit data	P2	IO	EV_{DD}	---
LPUART4_SIN/ **UART2_CTS_B**/GPIO1_22/ UART4_SIN/FTM4_CH5/ LPUART1_CTS_B	Receive data	M2	I	DV_{DD}	1
LPUART4_SOUT/ **UART2_RTS_B**/GPIO1_20/ UART4_SOUT/FTM4_CH3/ LPUART1_RTS_B	Transmit data	L1	IO	DV_{DD}	---
LPUART5_SIN/**SDHC_DAT2**/ GPIO2_07/LPUART2_CTS_B/ FTM4_EXTCLK	Receive data	R1	I	EV_{DD}	1
LPUART5_SOUT/ **SDHC_DAT1**/GPIO2_06/ FTM4_FAULT/ LPUART2_RTS_B	Transmit data	R2	IO	EV_{DD}	---
LPUART6_SIN/**SDHC_CLK**/ GPIO2_09/LPUART3_CTS_B/ FTM4_QD_PHB	Receive data	P3	I	EV_{DD}	1
LPUART6_SOUT/ **SDHC_DAT3**/GPIO2_08/ FTM4_QD_PHA/ LPUART3_RTS_B	Transmit data	T1	IO	EV_{DD}	---
TSEC_1588					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
TSEC_1588_ALARM_OUT1/ **EC2_TXD2**/GPIO3_16/ FTM2_CH7	Alarm Out	AE3	O	LV_{DD}	1
TSEC_1588_ALARM_OUT2/ **EC2_TXD3**/GPIO3_15/ FTM2_CH5	Alarm Out	AD3	O	LV_{DD}	1
TSEC_1588_CLK_IN/ **EC2_RX_CLK**/GPIO3_26/ FTM2_QD_PHA	Clock In	AC1	I	LV_{DD}	1
TSEC_1588_CLK_OUT/ **EC2_TXD1**/GPIO3_17/ FTM2_CH3	Clock Out	AE4	O	LV_{DD}	1
TSEC_1588_PULSE_OUT1/ **EC2_RXD1**/GPIO3_24/ FTM2_CH1	Pulse Out	AE1	O	LV_{DD}	1
TSEC_1588_PULSE_OUT2/ **EC2_TXD0**/GPIO3_18/ FTM2_CH2	Pulse Out	AF3	O	LV_{DD}	1
TSEC_1588_TRIG_IN1/ **EC2_RX_DV**/GPIO3_27/ FTM2_QD_PHB	Trigger In	AF1	I	LV_{DD}	1
TSEC_1588_TRIG_IN2/ **EC2_RXD0**/GPIO3_25/ FTM2_CH0	Trigger In	AE2	I	LV_{DD}	1
Power and Ground Signals					
GND001	GND	A2	---	---	---
GND002	GND	A5	---	---	---
GND003	GND	A21	---	---	---
GND004	GND	B3	---	---	---
GND005	GND	B4	---	---	---
GND006	GND	B7	---	---	---
GND007	GND	B10	---	---	---
GND008	GND	B13	---	---	---
GND009	GND	B16	---	---	---
GND010	GND	B19	---	---	---
GND011	GND	B21	---	---	---
GND012	GND	B24	---	---	---
GND013	GND	B26	---	---	---
GND014	GND	C1	---	---	---
GND015	GND	C2	---	---	---
GND016	GND	C5	---	---	---
GND017	GND	C21	---	---	---
GND018	GND	C27	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND019	GND	D3	---	---	---
GND020	GND	D4	---	---	---
GND021	GND	D7	---	---	---
GND022	GND	D9	---	---	---
GND023	GND	D12	---	---	---
GND024	GND	D15	---	---	---
GND025	GND	D18	---	---	---
GND026	GND	D21	---	---	---
GND027	GND	D24	---	---	---
GND028	GND	E1	---	---	---
GND029	GND	E2	---	---	---
GND030	GND	E5	---	---	---
GND031	GND	E21	---	---	---
GND032	GND	E26	---	---	---
GND033	GND	F3	---	---	---
GND034	GND	F4	---	---	---
GND035	GND	F7	---	---	---
GND036	GND	F14	---	---	---
GND037	GND	F16	---	---	---
GND038	GND	F18	---	---	---
GND039	GND	F24	---	---	---
GND040	GND	G1	---	---	---
GND041	GND	G2	---	---	---
GND042	GND	G9	---	---	---
GND043	GND	G10	---	---	---
GND044	GND	G11	---	---	---
GND045	GND	G21	---	---	---
GND046	GND	G26	---	---	---
GND047	GND	H3	---	---	---
GND048	GND	H4	---	---	---
GND049	GND	H5	---	---	---
GND050	GND	H14	---	---	---
GND051	GND	H15	---	---	---
GND052	GND	H16	---	---	---
GND053	GND	H17	---	---	---
GND054	GND	H18	---	---	---
GND055	GND	H21	---	---	---
GND056	GND	H24	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND057	GND	J6	---	---	---
GND058	GND	J7	---	---	---
GND059	GND	J8	---	---	---
GND060	GND	J9	---	---	---
GND061	GND	J10	---	---	---
GND062	GND	J11	---	---	---
GND063	GND	J12	---	---	---
GND064	GND	J21	---	---	---
GND065	GND	J23	---	---	---
GND066	GND	J26	---	---	---
GND067	GND	K2	---	---	---
GND068	GND	K4	---	---	---
GND069	GND	K6	---	---	---
GND070	GND	K13	---	---	---
GND071	GND	K15	---	---	---
GND072	GND	K17	---	---	---
GND073	GND	K19	---	---	---
GND074	GND	K21	---	---	---
GND075	GND	L6	---	---	---
GND076	GND	L10	---	---	---
GND077	GND	L12	---	---	---
GND078	GND	L14	---	---	---
GND079	GND	L16	---	---	---
GND080	GND	L18	---	---	---
GND081	GND	L20	---	---	---
GND082	GND	L23	---	---	---
GND083	GND	L26	---	---	---
GND084	GND	M6	---	---	---
GND085	GND	M9	---	---	---
GND086	GND	M11	---	---	---
GND087	GND	M13	---	---	---
GND088	GND	M15	---	---	---
GND089	GND	M17	---	---	---
GND090	GND	M19	---	---	---
GND091	GND	M21	---	---	---
GND092	GND	M23	---	---	---
GND093	GND	N2	---	---	---
GND094	GND	N4	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND095	GND	N6	---	---	---
GND096	GND	N8	---	---	---
GND097	GND	N10	---	---	---
GND098	GND	N12	---	---	---
GND099	GND	N14	---	---	---
GND100	GND	N16	---	---	---
GND101	GND	N18	---	---	---
GND102	GND	N20	---	---	---
GND103	GND	N23	---	---	---
GND104	GND	N26	---	---	---
GND105	GND	P6	---	---	---
GND106	GND	P9	---	---	---
GND107	GND	P11	---	---	---
GND108	GND	P13	---	---	---
GND109	GND	P15	---	---	---
GND110	GND	P17	---	---	---
GND111	GND	P19	---	---	---
GND112	GND	P23	---	---	---
GND113	GND	R5	---	---	---
GND114	GND	R8	---	---	---
GND115	GND	R10	---	---	---
GND116	GND	R12	---	---	---
GND117	GND	R14	---	---	---
GND118	GND	R16	---	---	---
GND119	GND	R18	---	---	---
GND120	GND	R20	---	---	---
GND121	GND	R23	---	---	---
GND122	GND	R26	---	---	---
GND123	GND	T2	---	---	---
GND124	GND	T4	---	---	---
GND125	GND	T6	---	---	---
GND126	GND	T9	---	---	---
GND127	GND	T11	---	---	---
GND128	GND	T13	---	---	---
GND129	GND	T15	---	---	---
GND130	GND	T17	---	---	---
GND131	GND	T19	---	---	---
GND132	GND	T21	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND133	GND	T23	---	---	---
GND134	GND	T26	---	---	---
GND135	GND	U6	---	---	---
GND136	GND	U8	---	---	---
GND137	GND	U10	---	---	---
GND138	GND	U12	---	---	---
GND139	GND	U14	---	---	---
GND140	GND	U16	---	---	---
GND141	GND	U18	---	---	---
GND142	GND	U20	---	---	---
GND143	GND	U23	---	---	---
GND144	GND	V2	---	---	---
GND145	GND	V4	---	---	---
GND146	GND	V6	---	---	---
GND147	GND	V9	---	---	---
GND148	GND	V11	---	---	---
GND149	GND	V13	---	---	---
GND150	GND	V15	---	---	---
GND151	GND	V17	---	---	---
GND152	GND	V19	---	---	---
GND153	GND	V21	---	---	---
GND154	GND	V23	---	---	---
GND155	GND	V26	---	---	---
GND156	GND	W12	---	---	---
GND157	GND	W18	---	---	---
GND158	GND	W20	---	---	---
GND159	GND	W22	---	---	---
GND160	GND	Y2	---	---	---
GND161	GND	Y5	---	---	---
GND162	GND	Y13	---	---	---
GND163	GND	Y14	---	---	---
GND164	GND	Y21	---	---	---
GND165	GND	Y23	---	---	---
GND166	GND	Y26	---	---	---
GND167	GND	AA4	---	---	---
GND168	GND	AA14	---	---	---
GND169	GND	AA21	---	---	---
GND170	GND	AA24	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND171	GND	AB2	---	---	---
GND172	GND	AB12	---	---	---
GND173	GND	AB26	---	---	---
GND174	GND	AC21	---	---	---
GND175	GND	AC24	---	---	---
GND176	GND	AD2	---	---	---
GND177	GND	AD4	---	---	---
GND178	GND	AD26	---	---	---
GND179	GND	AE21	---	---	---
GND180	GND	AE24	---	---	---
GND181	GND	AF4	---	---	---
GND182	GND	AF21	---	---	---
GND183	GND	AF26	---	---	---
GND184	GND	AG1	---	---	---
GND185	GND	AG24	---	---	---
GND186	GND	AG26	---	---	---
GND187	GND	AH2	---	---	---
GND188	GND	AH21	---	---	---
SD_GND01	Serdes core logic GND	Y6	---	---	23
SD_GND02	Serdes core logic GND	Y7	---	---	23
SD_GND03	Serdes core logic GND	Y8	---	---	23
SD_GND04	Serdes core logic GND	Y9	---	---	23
SD_GND05	Serdes core logic GND	Y10	---	---	23
SD_GND06	Serdes core logic GND	Y15	---	---	23
SD_GND07	Serdes core logic GND	Y16	---	---	23
SD_GND08	Serdes core logic GND	AA5	---	---	23
SD_GND09	Serdes core logic GND	AA7	---	---	23
SD_GND10	Serdes core logic GND	AA9	---	---	23
SD_GND11	Serdes core logic GND	AA12	---	---	23
SD_GND12	Serdes core logic GND	AA17	---	---	23
SD_GND13	Serdes core logic GND	AA18	---	---	23
SD_GND14	Serdes core logic GND	AA19	---	---	23
SD_GND15	Serdes core logic GND	AB7	---	---	23
SD_GND16	Serdes core logic GND	AB9	---	---	23
SD_GND17	Serdes core logic GND	AB14	---	---	23
SD_GND18	Serdes core logic GND	AB17	---	---	23
SD_GND19	Serdes core logic GND	AB20	---	---	23
SD_GND20	Serdes core logic GND	AC5	---	---	23

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND21	Serdes core logic GND	AC6	---	---	23
SD_GND22	Serdes core logic GND	AC8	---	---	23
SD_GND23	Serdes core logic GND	AC10	---	---	23
SD_GND24	Serdes core logic GND	AC11	---	---	23
SD_GND25	Serdes core logic GND	AC15	---	---	23
SD_GND26	Serdes core logic GND	AC16	---	---	23
SD_GND27	Serdes core logic GND	AC18	---	---	23
SD_GND28	Serdes core logic GND	AC19	---	---	23
SD_GND29	Serdes core logic GND	AD5	---	---	23
SD_GND30	Serdes core logic GND	AD7	---	---	23
SD_GND31	Serdes core logic GND	AD9	---	---	23
SD_GND32	Serdes core logic GND	AD12	---	---	23
SD_GND33	Serdes core logic GND	AD14	---	---	23
SD_GND34	Serdes core logic GND	AD17	---	---	23
SD_GND35	Serdes core logic GND	AD20	---	---	23
SD_GND36	Serdes core logic GND	AE5	---	---	23
SD_GND37	Serdes core logic GND	AE7	---	---	23
SD_GND38	Serdes core logic GND	AE9	---	---	23
SD_GND39	Serdes core logic GND	AE12	---	---	23
SD_GND40	Serdes core logic GND	AE14	---	---	23
SD_GND41	Serdes core logic GND	AE17	---	---	23
SD_GND42	Serdes core logic GND	AE20	---	---	23
SD_GND43	Serdes core logic GND	AF6	---	---	23
SD_GND44	Serdes core logic GND	AF7	---	---	23
SD_GND45	Serdes core logic GND	AF8	---	---	23
SD_GND46	Serdes core logic GND	AF9	---	---	23
SD_GND47	Serdes core logic GND	AF10	---	---	23
SD_GND48	Serdes core logic GND	AF11	---	---	23
SD_GND49	Serdes core logic GND	AF15	---	---	23
SD_GND50	Serdes core logic GND	AF16	---	---	23
SD_GND51	Serdes core logic GND	AF17	---	---	23
SD_GND52	Serdes core logic GND	AF18	---	---	23
SD_GND53	Serdes core logic GND	AF19	---	---	23
SD_GND54	Serdes core logic GND	AG5	---	---	23
SD_GND55	Serdes core logic GND	AG7	---	---	23
SD_GND56	Serdes core logic GND	AG9	---	---	23
SD_GND57	Serdes core logic GND	AG12	---	---	23
SD_GND58	Serdes core logic GND	AG14	---	---	23

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD_GND59	Serdes core logic GND	AG17	---	---	23
SD_GND60	Serdes core logic GND	AG20	---	---	23
SD_GND61	Serdes core logic GND	AH5	---	---	23
SD_GND62	Serdes core logic GND	AH7	---	---	23
SD_GND63	Serdes core logic GND	AH9	---	---	23
SD_GND64	Serdes core logic GND	AH12	---	---	23
SD_GND65	Serdes core logic GND	AH14	---	---	23
SD_GND66	Serdes core logic GND	AH17	---	---	23
SD_GND67	Serdes core logic GND	AH20	---	---	23
SENSEGND	GND Sense pin	G20	---	---	---
OVDD1	General I/O supply	J14	---	OV_{DD}	---
OVDD2	General I/O supply	J15	---	OV_{DD}	---
OVDD3	General I/O supply	J16	---	OV_{DD}	---
OVDD4	General I/O supply	J17	---	OV_{DD}	---
OVDD5	General I/O supply	J18	---	OV_{DD}	---
OVDD6	General I/O supply	R7	---	OV_{DD}	---
DVDD1	UART/I2C supply	N7	---	DV_{DD}	---
DVDD2	UART/I2C supply	P7	---	DV_{DD}	---
EVDD	eSDHC supply	R6	---	EV_{DD}	---
LVDD1	Ethernet controller 1 & 2 supply	T7	---	LV_{DD}	---
LVDD2	Ethernet controller 1 & 2 supply	U7	---	LV_{DD}	---
LVDD3	Ethernet controller 1 & 2 supply	V7	---	LV_{DD}	---
TVDD	1.2 V / LVDD supply for MDIO interface for 10G Fman (EC2)	W6	---	TV_{DD}	---
G1VDD01	DDR supply	B27	---	$G1V_{DD}$	---
G1VDD02	DDR supply	D27	---	$G1V_{DD}$	---
G1VDD03	DDR supply	F27	---	$G1V_{DD}$	---
G1VDD04	DDR supply	H27	---	$G1V_{DD}$	---
G1VDD05	DDR supply	K27	---	$G1V_{DD}$	---
G1VDD06	DDR supply	L22	---	$G1V_{DD}$	---
G1VDD07	DDR supply	M22	---	$G1V_{DD}$	---
G1VDD08	DDR supply	M27	---	$G1V_{DD}$	---
G1VDD09	DDR supply	N22	---	$G1V_{DD}$	---
G1VDD10	DDR supply	P22	---	$G1V_{DD}$	---
G1VDD11	DDR supply	P27	---	$G1V_{DD}$	---
G1VDD12	DDR supply	R22	---	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD13	DDR supply	T22	---	$G1V_{DD}$	---
G1VDD14	DDR supply	U22	---	$G1V_{DD}$	---
G1VDD15	DDR supply	U27	---	$G1V_{DD}$	---
G1VDD16	DDR supply	V22	---	$G1V_{DD}$	---
G1VDD17	DDR supply	W27	---	$G1V_{DD}$	---
G1VDD18	DDR supply	AA27	---	$G1V_{DD}$	---
G1VDD19	DDR supply	AC27	---	$G1V_{DD}$	---
G1VDD20	DDR supply	AE27	---	$G1V_{DD}$	---
G1VDD21	DDR supply	AG27	---	$G1V_{DD}$	---
G1VDD22	DDR supply	AH27	---	$G1V_{DD}$	---
SVDD1	SerDes1 core logic supply	W10	---	SV_{DD}	---
SVDD2	SerDes1 core logic supply	W13	---	SV_{DD}	---
SVDD3	SerDes1 core logic supply	W14	---	SV_{DD}	---
SVDD4	SerDes1 core logic supply	W15	---	SV_{DD}	---
SVDD5	SerDes1 core logic supply	W16	---	SV_{DD}	---
SVDD6	SerDes1 core logic supply	Y17	---	SV_{DD}	---
SVDD7	SerDes1 core logic supply	Y18	---	SV_{DD}	---
SVDD8	SerDes1 core logic supply	Y19	---	SV_{DD}	---
XVDD1	SerDes1 transceiver supply	AC7	---	XV_{DD}	---
XVDD2	SerDes1 transceiver supply	AC9	---	XV_{DD}	---
XVDD3	SerDes1 transceiver supply	AC12	---	XV_{DD}	---
XVDD4	SerDes1 transceiver supply	AC14	---	XV_{DD}	---
XVDD5	SerDes1 transceiver supply	AC17	---	XV_{DD}	---
XVDD6	SerDes1 transceiver supply	AC20	---	XV_{DD}	---
FA_VL	Reserved	AB21	---	FA_VL	15
PROG_MTR	Reserved	F13	---	PROG_MTR	15
TA_PROG_SFP	SFP Fuse Programming Override supply	G13	---	TA_PROG_SFP	---
TH_VDD	Thermal Monitor Unit supply	G8	---	TH_V_{DD}	---
VDD01	Supply for cores and platform	K14	---	V_{DD}	---
VDD02	Supply for cores and platform	K16	---	V_{DD}	---
VDD03	Supply for cores and platform	K18	---	V_{DD}	---
VDD04	Supply for cores and platform	K20	---	V_{DD}	---
VDD05	Supply for cores and platform	L11	---	V_{DD}	---
VDD06	Supply for cores and platform	L13	---	V_{DD}	---
VDD07	Supply for cores and platform	L15	---	V_{DD}	---
VDD08	Supply for cores and platform	L17	---	V_{DD}	---
VDD09	Supply for cores and platform	L19	---	V_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD10	Supply for cores and platform	M10	---	V_{DD}	---
VDD11	Supply for cores and platform	M12	---	V_{DD}	---
VDD12	Supply for cores and platform	M14	---	V_{DD}	---
VDD13	Supply for cores and platform	M16	---	V_{DD}	---
VDD14	Supply for cores and platform	M18	---	V_{DD}	---
VDD15	Supply for cores and platform	N9	---	V_{DD}	---
VDD16	Supply for cores and platform	N11	---	V_{DD}	---
VDD17	Supply for cores and platform	N13	---	V_{DD}	---
VDD18	Supply for cores and platform	N15	---	V_{DD}	---
VDD19	Supply for cores and platform	N17	---	V_{DD}	---
VDD20	Supply for cores and platform	N19	---	V_{DD}	---
VDD21	Supply for cores and platform	P10	---	V_{DD}	---
VDD22	Supply for cores and platform	P12	---	V_{DD}	---
VDD23	Supply for cores and platform	P14	---	V_{DD}	---
VDD24	Supply for cores and platform	P16	---	V_{DD}	---
VDD25	Supply for cores and platform	P18	---	V_{DD}	---
VDD26	Supply for cores and platform	R9	---	V_{DD}	---
VDD27	Supply for cores and platform	R11	---	V_{DD}	---
VDD28	Supply for cores and platform	R13	---	V_{DD}	---
VDD29	Supply for cores and platform	R15	---	V_{DD}	---
VDD30	Supply for cores and platform	R17	---	V_{DD}	---
VDD31	Supply for cores and platform	R19	---	V_{DD}	---
VDD32	Supply for cores and platform	T10	---	V_{DD}	---
VDD33	Supply for cores and platform	T12	---	V_{DD}	---
VDD34	Supply for cores and platform	T14	---	V_{DD}	---
VDD35	Supply for cores and platform	T16	---	V_{DD}	---
VDD36	Supply for cores and platform	T18	---	V_{DD}	---
VDD37	Supply for cores and platform	U9	---	V_{DD}	---
VDD38	Supply for cores and platform	U11	---	V_{DD}	---
VDD39	Supply for cores and platform	U13	---	V_{DD}	---
VDD40	Supply for cores and platform	U15	---	V_{DD}	---
VDD41	Supply for cores and platform	U17	---	V_{DD}	---
VDD42	Supply for cores and platform	U19	---	V_{DD}	---
VDD43	Supply for cores and platform	V10	---	V_{DD}	---
VDD44	Supply for cores and platform	V12	---	V_{DD}	---
VDD45	Supply for cores and platform	V14	---	V_{DD}	---
VDD46	Supply for cores and platform	V16	---	V_{DD}	---
VDD47	Supply for cores and platform	V18	---	V_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD48	Supply for cores and platform	V20	---	V_{DD}	---
VDD49	Supply for cores and platform	W11	---	V_{DD}	---
VDD50	Supply for cores and platform	W17	---	V_{DD}	---
VDD51	Supply for cores and platform	W19	---	V_{DD}	---
TA_BB_VDD	Battery Backed Security Monitor supply	G12	---	TA_BB_V_{DD}	---
AVDD_CGA1	CPU Cluster Group A PLL1 supply	H11	---	AVDD_CGA1	---
AVDD_CGA2	CPU Cluster Group A PLL2 supply	H10	---	AVDD_CGA2	---
AVDD_PLAT	Platform PLL supply	H9	---	AVDD_PLAT	---
AVDD_D1	DDR1 PLL supply	R21	---	AVDD_D1	---
AVDD_SD1_PLL1	SerDes1 PLL 1 supply	AA11	---	AVDD_SD1_PLL1	---
AVDD_SD1_PLL2	SerDes1 PLL 2 supply	AB6	---	AVDD_SD1_PLL2	---
AVDD_SD2_PLL1	SerDes2 PLL 1 supply	AB15	---	AVDD_SD2_PLL1	---
AVDD_SD2_PLL2	SerDes2 PLL 2 supply	AA16	---	AVDD_SD2_PLL2	---
SENSEVDD	Vdd Sense pin	G19	---	SENSEVDD	---
USB_HVDD1	3.3 V High Supply	K8	---	USB_HV_{DD}	---
USB_HVDD2	3.3 V High Supply	L8	---	USB_HV_{DD}	---
USB_SDVDD1	1.0 V Analog and digital HS supply	M7	---	USB_SDV_{DD}	---
USB_SDVDD2	1.0 V Analog and digital HS supply	M8	---	USB_SDV_{DD}	---
USB_SVDD1	1.0 V Analog and digital SS supply	K7	---	USB_SV_{DD}	---
USB_SVDD2	1.0 V Analog and digital SS supply	L7	---	USB_SV_{DD}	---
No Connection Pins					
NC_AA10	No Connection	AA10	---	---	12
NC_AA15	No Connection	AA15	---	---	12
NC_AB10	No Connection	AB10	---	---	12
NC_AB11	No Connection	AB11	---	---	12
NC_AB16	No Connection	AB16	---	---	12
NC_F12	No Connection	F12	---	---	12
NC_K10	No Connection	K10	---	---	12
NC_K11	No Connection	K11	---	---	12
NC_K12	No Connection	K12	---	---	12
NC_K22	No Connection	K22	---	---	12
NC_K9	No Connection	K9	---	---	12
NC_L21	No Connection	L21	---	---	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
NC_L9	No Connection	L9	---	---	12
NC_M20	No Connection	M20	---	---	12
NC_N21	No Connection	N21	---	---	12
NC_P20	No Connection	P20	---	---	12
NC_P21	No Connection	P21	---	---	12
NC_P5	No Connection	P5	---	---	12
NC_P8	No Connection	P8	---	---	12
NC_R4	No Connection	R4	---	---	12
NC_T20	No Connection	T20	---	---	12
NC_T5	No Connection	T5	---	---	12
NC_T8	No Connection	T8	---	---	12
NC_U21	No Connection	U21	---	---	12
NC_U4	No Connection	U4	---	---	12
NC_U5	No Connection	U5	---	---	12
NC_V5	No Connection	V5	---	---	12
NC_V8	No Connection	V8	---	---	12
NC_W21	No Connection	W21	---	---	12
NC_W5	No Connection	W5	---	---	12
NC_W7	No Connection	W7	---	---	12
NC_W8	No Connection	W8	---	---	12
NC_W9	No Connection	W9	---	---	12

1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either sample configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.

2. This output is actively driven during reset rather than being tri-stated during reset.

3. MDIC[0] is grounded through a 162 Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through a 162 Ω precision 1% resistor. For either full or half driver strength calibration of DDR IOs, use the same MDIC resistor value of 162 Ω. The memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. These pins are used for automatic calibration of the DDR4 IOs.

4. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.

5. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.

6. Recommend that a weak pull-up resistor (2-10 kΩ) be placed on this pin to the respective power supply.

7. This pin is an open-drain signal.

8. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.

9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.

10. These are test signals for factory use only and must be pulled up (100Ω to 1-kΩ) to the respective power supply for normal operation.

11. This pin requires a 200Ω ± 1% pull-up to respective power-supply.

12. Do not connect. These pins should be left floating.

14. This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

15. These pins must be pulled to ground (GND).

16. This pin requires a 698Ω ± 1% pull-up to respective power-supply.

17. These pins should be tied to ground if the diode is not utilized for temperature monitoring.

18. This pin should be grounded through a 200Ω +/-1% 100ppm/°C precision resistor.

19. This pin must be pulled to OVDD through a 100-Ω to 1kΩ resistor for a four core LS1046A device and tied to ground for a two core LS1026A device.

20. In normal operation, this pin must be pulled high to OVDD with 4.7 kΩ.

21. DIFF_SYSCLK and DIFF_SYSCLK_B is tied to cfg_eng_use0, the configuration is described in section "Reset configuration word (RCW)" of *QorIQ LS1046A Reference Manual*.

22. This pin should be connected to ground through 2-10 kΩ resistor when not used.

23. SD_GND must be directly connected to GND.

24. This pin must be pulled down to GND with a pull down resistor of value 1 KΩ

25. This pin will not be tested using JTAG Boundary scan operation.

26. For proper clock selection, terminate cfg_eng_use0 with a pull up or pull down of 4.7 kΩ to ensure that the signal will have a valid state as soon as the IO voltage reach its operating condition.

27. When using discrete DRAM, or RDIMM, the MALERT_B pin needs a 50 ohm to 100 ohm pull-up resistor to G1VDD.

28. This pin requires a pull-up to the respective power supply so as to meet the timing requirements in Table 23

Warning

See **"Connection Recommendations in QorIQ LS1046A Design Checklist (AN5252)"** for additional details on properly connecting these pins for specific applications.

3 Electrical characteristics

This section describes the DC and AC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

Table 2. Absolute maximum ratings[1,5]

Characteristic	Symbol	Max Value	Unit	Notes
Core and platform supply voltage	V_{DD}	-0.3 to 1.08	V	4

Table continues on the next page...

Table 2. Absolute maximum ratings[1,5] (continued)

Characteristic	Symbol	Max Value	Unit	Notes
PLL supply voltage (core PLL, platform, DDR)	AV_{DD}_CGA1 AV_{DD}_CGA2 AV_{DD}_D1 AV_{DD}_PLAT	-0.3 to 1.98	V	—
PLL supply voltage (SerDes, filtered from X*n*V_{DD})	AVDD_SD*n*_PLL1 AVDD_SD*n*_PLL2	-0.3 to 1.48	V	—
SFP Fuse Programming	TA_PROG_SFP	-0.3 to 1.98	V	—
Thermal Unit Monitor supply	TH_V_{DD}	-0.3 to 1.98	V	—
Battery Backed Security Monitor supply	TA_BB_V_{DD}	-0.3 to 1.08	V	—
IFC, SPI, IRQ[0:2], Tamper Detect, System Control, SYSCLK, DDRCLK, RTC, EVT[0:4], DFT, JTAG, DIFF_SYSCLK, CLK_OUT, QSPI, FTM[5:7], eSDHC_DAT[4:7], eSDHC_CMD/DAT0_DIR, eSDHC_DAT123_DIR, eSDHC_SYNC_IN/OUT, SDHC_VS	OV_{DD}	-0.3 to 1.98	V	—
DUART, I2C, IRQ[3:10], USB2/3_PWRFAULT, USB2/3_DRVVBUS, EVT_B[5:8], LPUART[1:2], LPUART4, FTM3_CH[1:7], FTM4_CH[1:5], FTM8, eSDHC_CD/WP	DV_{DD}	-0.3 to 3.63 -0.3 to 1.98	V	—
eSDHC_DAT[0:3], eSDHC_CMD, eSDHC_CLK, FTM4_CH[6:7], LPUART[3:6]	EV_{DD}	-0.3 to 3.63 -0.3 to 1.98	V	—
DDR4 DRAM I/O voltage	$G1V_{DD}$	-0.3 to 1.32	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers	SV_{DD}	-0.3 to 1.08	V	—
Pad power supply for SerDes transmitter	XV_{DD}	-0.3 to 1.48	V	—
Ethernet interface, Ethernet management interface 1 (EMI1), 1588, IRQ11, FTM1, FTM2,	LV_{DD}	-0.3 to 2.75 -0.3 to 1.98	V	—
Ethernet management interface 2 (EMI2), GPIO2	TV_{DD}	-0.3 to 2.75 -0.3 to 1.98 -0.3 to 1.32	V	—
USB PHY Transceiver supply voltage	USB_HV_{DD}	-0.3 to 3.63	V	-
	USB_SDV_{DD}	-0.3 to 1.08	V	3
	USB_SV_{DD}	-0.3 to 1.08	V	2
Storage temperature range	T_{STG}	-55 to 150	°C	--

Notes:

1. Functional operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. Analog and Digital SS supply for USBPHY.

3. Analog and Digital HS supply for USBPHY.

4. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.

Table 2. Absolute maximum ratings[1,5]

Characteristic	Symbol	Max Value	Unit	Notes
5. Exposing device to Absolute Maximum Ratings conditions for long periods of time may affect reliability or cause permanent damage.				

This table provides the absolute maximum ratings for input signal voltage levels.

Table 3. Absolute maximum ratings for input signal voltage levels[1]

Interface Input signals	Symbol	Max DC V_input range	Max undershoot and overshoot voltage range	Unit	Notes
DDR4 DRAM signals	$G1V_{IN}$	GND to ($G1V_{DD}$ x 1.05)	-0.3 to ($G1V_{DD}$ x 1.1)	V	2, 3, 5
Ethernet interface, Ethernet management interface 1 (EMI1), 1588, IRQ11, FTM1, FTM2	LV_{IN}	GND to (LV_{DD} x 1.1)	-0.3 to (LV_{DD} x 1.15)	V	2, 3
IFC, SPI, IRQ[0:2], Tamper Detect, System Control, SYSCLK, DDRCLK, RTC, EVT[0:4], DFT, JTAG, DIFF_SYSCLK, CLK_OUT, QSPI, FTM[5:7], eSDHC_DAT[4:7], eSDHC_CMD/DAT0_DIR, eSDHC_DAT123_DIR, eSDHC_SYNC_IN/OUT, SDHC_VS	OV_{IN}	GND to (OV_{DD} x 1.1)	-0.3 to (OV_{DD} x 1.15)	V	2, 3
DUART, I2C, IRQ[3:10], USB2/3_PWRFAULT, USB2/3_DRVVBUS, EVT_B[5:8], LPUART[1:2], LPUART4, FTM3_CH[1:7], FTM4_CH[1:5], FTM8, eSDHC_CD/WP	DV_{IN}	GND to (DV_{DD} x 1.1)	-0.3 to (DV_{DD} x 1.15)		
eSDHC_DAT[0:3], eSDHC_CMD, eSDHC_CLK, FTM4_CH[6:7], LPUART[3:6]	EV_{IN}	GND to (EV_{DD} x 1.1)	-0.3 to (EV_{DD} x 1.15)	V	2, 3
Main power supply for internal circuitry of SerDes	SnV_{IN}	GND to (SV_{DD} x 1.05)	-0.3 to (SnV_{DD} x 1.1)	V	2, 3
Ethernet management interface 2 (EMI2), GPIO2	TV_{IN}	GND to (TV_{DD} x 1.05)	-0.3 to (TV_{DD} x 1.15)	V	2, 3
USB PHY Transceiver signals	USB_HV_{IN}	GND to (USB_HV_{DD} x 1.05)	-0.3 to (USB_HV_{DD} x 1.15)	V	2, 3
	USB_SV_{IN}	GND to (USB_SV_{DD} x 1.1)	-0.3 to (USB_SV_{DD} x 1.15)	V	2, 3

Notes:

1. Functional operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. **Caution:** The input voltage level of the signals must not exceed corresponding Max DC V_input range. For example DDR4 must not exceed 5% of $G1V_{DD}$.

3. **Caution:** (S, G, L, O, D, E, T) VIN, USB_HVIN, USB_SVIN may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 8.

Table 3. Absolute maximum ratings for input signal voltage levels[1]

Interface Input signals	Symbol	Max DC V_input range	Max undershoot and overshoot voltage range	Unit	Notes
5. Typical DDR interface uses ODT enabled mode. For tests purposes with ODT off mode, simulation should be done first so as to make sure that the overshoot signal level at the input pin does not exceed GVDD by more than 10%. The Overshoot/ Undershoot period should comply with JEDEC standards.					

3.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this chip.

NOTE

The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 4. Recommended operating conditions

Characteristic	Symbol	Recommended value	Unit	Notes
Core and platform supply voltage	V_{DD}	1.0 V ± 30 mV	V	3, 4, 5, 8
0.9 V core and platform supply voltage		0.9 V ± 30 mV		
PLL supply voltage (core PLL, platform, DDR)	AV_{DD}_CGA1	1.8 V ± 90 mV	V	9
	AV_{DD}_CGA2			
	AV_{DD}_D1			
	AV_{DD}_PLAT			
PLL supply voltage (SerDes, filtered from X*n*V_{DD})	AV_{DD}_SD1_PLL1 AV_{DD}_SD1_PLL2	1.35 V ± 67 mV	V	—
	AV_{DD}_SD2_PLL1 AV_{DD}_SD2_PLL2			
SFP fuse programming	TA_PROG_SFP	1.8 V ± 90 mV	V	2
Thermal monitor unit supply	TH_V_{DD}	1.8 V ± 90 mV	V	—
Battery Backed Security Monitor supply	TA_BB_V_{DD}	1.0 V ± 30 mV	V	8
		0.9 V ± 30 mV		
IFC, IRQ[0:2], Tamper Detect, System Control, SYSCLK, DDRCLK, RTC, EVT[0:4], DFT, JTAG, DIFF_SYSCLK, CLK_OUT, QSPI, FTM[5:7], SPI, SDHC_DAT[4:7], SDHC_CMD_DIR, SDHC_DAT0_DIR, SDHC_DAT123_DIR, SDHC_SYNC_IN/OUT, SDHC_VS	OV_{DD}	1.8 V ± 90 mV	V	—
DUART, I2C, IRQ[3:10], USB2/3_PWRFAULT, USB2/3_DRVVBUS, EVT_B[5:8], LPUART[1:2], LPUART4, FTM3_CH[1:7], FTM4_CH[1:5], FTM8, SDHC_CD/WP	DV_{DD}	3.3 V ± 165 mV 1.8 V ± 90 mV	V	—
SDHC_DAT[0:3], SDHC_CMD, SDHC_CLK, FTM4_CH[6:7], LPUART3, LPUART5, LPUART6	EV_{DD}	3.3 V ±165 mV 1.8 V ± 90 mV	V	—

Table continues on the next page...

Table 4. Recommended operating conditions (continued)

Characteristic		Symbol	Recommended value	Unit	Notes
DDR4 DRAM I/O voltage		$G1V_{DD}$	1.2 V ± 60 mV	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers		SV_{DD}	1.0 V ± 50 mV 0.9 V + 50 mV 0.9 V - 30 mV	V	—
Pad power supply for SerDes transmitters		XV_{DD}	1.35 V ± 67 mV	V	—
Ethernet interface 1/2, Ethernet management interface 1 (EMI1), 1588, IRQ11, FTM1, FTM2		LV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
Ethernet management interface 2 (EMI2), GPIO2		TV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV 1.2V ± 60 mV	V	
USB PHY 3.3 V high supply voltage		USB_HV_{DD}	3.3 V ± 165 mV	V	
USB PHY analog and digital HS supply		USB_SDV_{DD}	1.0 V ± 50 mV 0.9 V + 50 mV 0.9 V - 30 mV	V	7, 8
USB PHY analog and digital SS supply		USB_SV_{DD}	1.0 V ± 50 mV 0.9 V + 50 mV 0.9 V - 30 mV	V	6, 8
Input voltage	DDR4 DRAM signals	$G1V_{IN}$	GND to $G1V_{DD}$	V	—
	Ethernet interface, Ethernet management interface 1 (EMI1), 1588, IRQ11, FTM1, FTM2	LV_{IN}	GND to LV_{DD}	V	—
	IFC, SPI, IRQ[0:2], Tamper Detect, System Control, SYSCLK, DDRCLK, RTC, EVT[0:4], DFT, JTAG, DIFF_SYSCLK, CLK_OUT, QSPI, FTM[5:7], SDHC_DAT[4:7], SDHC_CMD_DIR/ DAT0_DIR, SDHC_DAT123_DIR, SDHC_SYNC_IN/OUT, SDHC_VS	OV_{IN}	GND to OV_{DD}	V	—
	DUART, I2C, IRQ[3:10], USB2/3_PWRFAULT, USB2/3_DRVVBUS, EVT_B[5:8], LPUART[1:2], LPUART4, FTM3_CH[1:7], FTM4_CH[1:5], FTM8, SDHC_CD/WP	DV_{IN}	GND to DV_{DD}	V	—
	SDHC_DAT[0:3], SDHC_CMD, SDHC_CLK, FTM4_CH[6:7], LPUART[3:6]	EV_{IN}	GND to EV_{DD}	V	—

Table continues on the next page...

Table 4. Recommended operating conditions (continued)

Characteristic		Symbol	Recommended value	Unit	Notes
	Main power supply for internal circuitry of SerDes	SV_{IN}	GND to SV_{DD}	V	—
	Ethernet management interface 2 (EMI2), GPIO2	TV_{IN}	GND to TV_{DD}	V	—
PHY transceiver signals	USB transceiver supply for USB PHY	USB_HV_{IN}	GND to $USBn_HV_{DD}$	V	—
	Analog and digital HS supply for USB PHY	USB_SV_{IN}	GND to USB_SV_{DD}	V	—
Operating temperature range	Normal operation	T_A, T_J	T_A = 0°C (min) to T_J = 105°C (max)	°C	10
	Extended temperature	T_A, T_J	T_A = -40°C (min) to T_J = 105°C (max)	°C	10
	Secure boot fuse programming	T_A, T_J	T_A = 0°C (min) to T_J = 105°C (max)	°C	2

Notes:

1. RGMII is supported at 2.5 V or 1.8 V.

2. TA_PROG_SFP must be supplied 1.8 V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming, subject to the power sequencing constraints shown in Power sequencing. For all other operating conditions, TA_PROG_SFP must be tied to GND.

3. For additional information, see the core and platform supply voltage filtering section in the chip design checklist.

4. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.

5. Operation at 1.08 V is allowable for up to 25 ms at initial power on.

6. Analog and Digital SS supply for USB PHY.

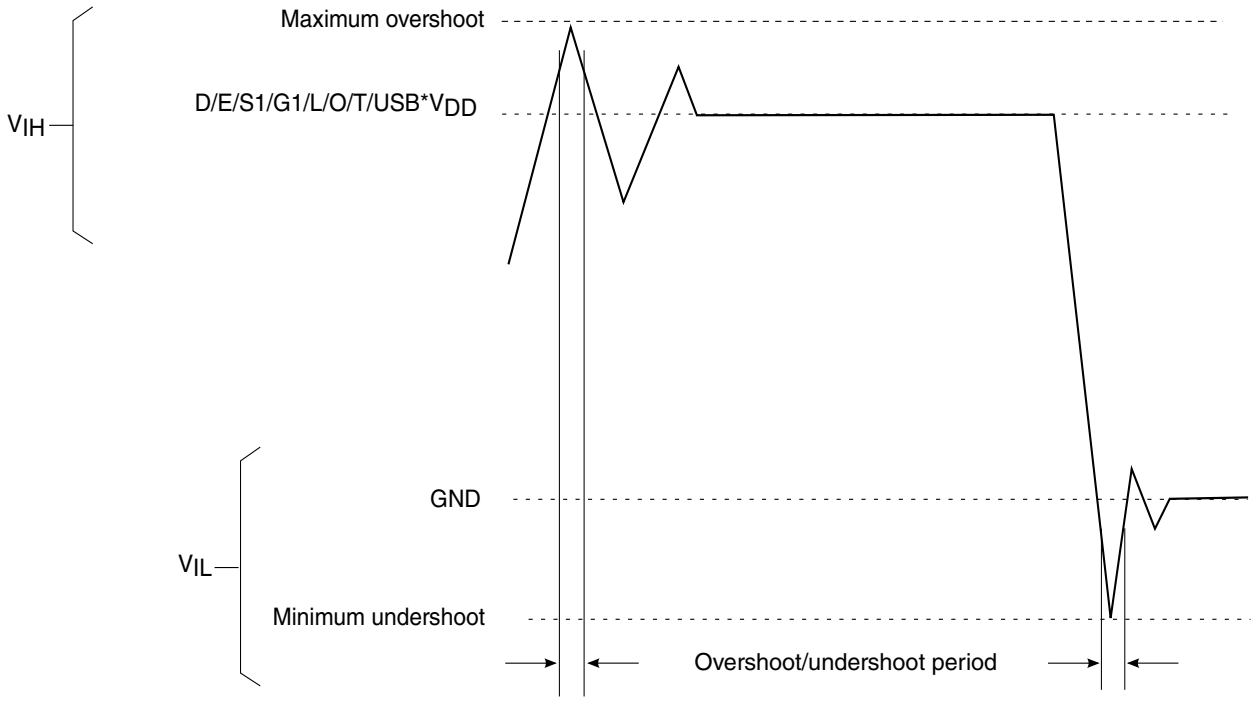
7. Analog and Digital HS supply for USB PHY.

8. For supported voltage requirement for a given part number, see Table 144.

9. AVDD_PLAT, AVDD_CGA1, AVDD_CGA2, and AVDD_D1 are measured at the input to the filter and not at the pin of the device.

10. For supported temperature range for a given part number, see Table 144.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Notes:

The overshoot/undershoot period should be less than 10% of shortest possible toggling period of the input signal or per input signal specific protocol requirement. For GPIO input signal overshoot/undershoot period, it should be less than 10% of the SYSCLK period.

Figure 8. Overshoot/undershoot voltage for $G1V_{DD}/OV_{DD}/SV_{DD}/TV_{DD}/$ $LV_{DD}/EV_{DD}/DV_{DD}/$ USB_HV_{DD}/USB_SV_{DD}

See Table 4 for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 4. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD}, EV_{DD}, DV_{DD}, TV_{DD}, and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the internally supplied reference signal as is appropriate for the JEDEC DDR4 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

3.1.3 Output driver characteristics

This chip provides information on the characteristics of the output driver strengths.

NOTE

These values are preliminary estimates.

Table 5. Output drive capability

Driver type	Output impedance (Ω)			Supply Voltage	Notes
	Minimum[2]	Typical	Maximum[3]		
DDR4 signal	-	18(full-strength mode) 27(half-strength mode)	-	$G1V_{DD}$ = 1.2 V	1
Ethernet interface, Ethernet management interface 1 (EMI1), 1588, FTM1, FTM2	30	50	70	LV_{DD} = 2.5V	-
	30	45	60	LV_{DD} = 1.8V	-
MDC of Ethernet management interface 2 (EMI 2)	45	65	100	TV_{DD} = 1.2 V	-
	40	55	75	TV_{DD} = 1.8V	-
	40	60	90	TV_{DD} = 2.5V	-
MDIO of Ethernet management interface 2 (EMI 2)	30	40	60	TV_{DD} = 1.2 V	-
	25	33	44	TV_{DD} = 1.8V	-
	25	40	57	TV_{DD} = 2.5V	-
IFC, SPI, EVT[0:4], JTAG, CLK_OUT, QSPI, FTM[5:7], eSDHC_DAT[4:7], eSDHC_CMD/DAT0_DIR, eSDHC_DAT123_DIR, eSDHC_SYNC_OUT, SDHC_VS	30	45	60	OV_{DD} = 1.8 V	-
eSDHC_DAT[0:3], eSDHC_CMD, eSDHC_CLK, FTM4_CH[6:7], LPUART[3:6]	45	65	90	EV_{DD} = 3.3V	-
	40	55	75	EV_{DD} = 1.8V	
DUART, I2C, USB2/3_DRVVBUS, EVT_B[5:8], LPUART[1:2], LPUART4, FTM3_CH[1:7], FTM4_CH[1:5], FTM8	40	55	75	DV_{DD} = 1.8V	-
	45	65	90	DV_{DD} = 3.3V	

1. The drive strength of the DDR4 in half-strength mode is at T_j = 105°C and at $G1V_{DD}$ (min).
2. Estimated number based on best case processed device.
3. Estimated number based on worst case processed device.

3.2 Power sequencing

The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation. For power up, these requirements are as follows:

1. OV_{DD}, DV_{DD}, LV_{DD}, EV_{DD}, TV_{DD}, XV_{DD}, AV_{DD}_CGA*n*, AV_{DD}_PLAT, AV_{DD}_D1, AV_{DD}_SD*n*_PLL1, AV_{DD}_SD*n*_PLL2, USB_HV_{DD}. Drive TA_PROG_SFP = GND.
   - PORESET_B input must be driven asserted and held during this step.
2. V_{DD}, SV_{DD}, $TA_BB_V_{DD}$, USB_SDV_{DD}, USB_SV_{DD}

- The 3.3 V (USB_HV_{DD}) in Step 1 and 1.0 V (USB_SDV_{DD}, USB_SV_{DD}) in Step 2 supplies can power up in any sequence provided all these USB supplies ramp up within 95 ms with respect to each other.

3. $G1V_{DD}$

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of their value.

All supplies must be at their stable values within 400 ms.

Negate PORESET_B input when the required assertion/hold time has been met per Table 23.

NOTE

- While V_{DD} is ramping up, current may be supplied from V_{DD} through LS1046A to $G1V_{DD}$.
- If using Trust Architecture Security Monitor battery backed features, prior to VDD ramping up to the 0.5 V level, ensure that OVDD is ramped to recommended operational voltage and SYSCLK or DIFF_SYSCLK/ DIFF_SYSCLK_B is running. These clocks should have a minimum frequency of 800 Hz and a maximum frequency not greater than the supported system clock frequency for the device.
- Ramp rate requirements should be met per Table 12.
- While XVDD is ramping, current may be supplied from XVDD through chip to SVDD.

Warning

Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates and is preliminary.

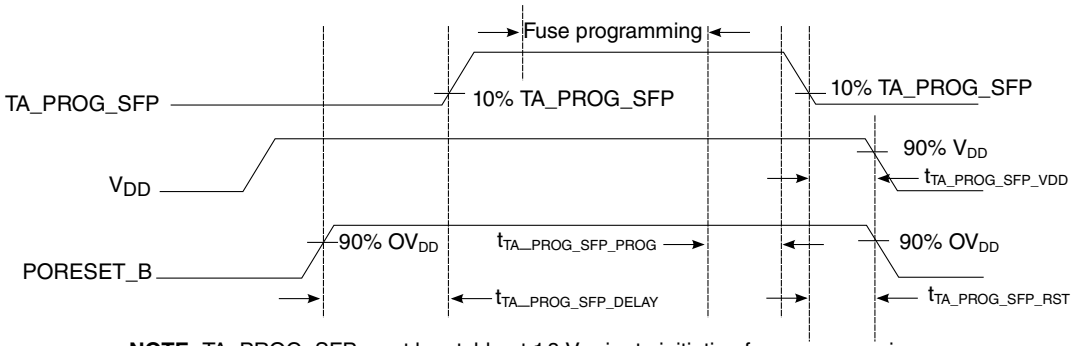
For secure boot fuse programming, use the following steps:

1. After negation of PORESET_B, drive TA_PROG_SFP = 1.8 V after a required minimum delay per Table 6.
2. After fuse programming is complete, it is required to return TA_PROG_SFP = GND before the system is power cycled or powered down (V_{DD} ramp down) per the required timing specified in Table 6. See Security fuse processor for additional details.

Warning

No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND.

This figure shows the TA_PROG_SFP timing diagram.



NOTE: TA_PROG_SFP must be stable at 1.8 V prior to initiating fuse programming.

Figure 9. TA_PROG_SFP timing diagram

This table provides information on the power-down and power-up sequence parameters for TA_PROG_SFP.

Table 6. TA_PROG_SFP timing [5]

Driver type	Min	Max	Unit	Notes
$t_{TA_PROG_SFP_DELAY}$	100	—	SYSCLKs	1
$t_{TA_PROG_SFP_PROG}$	0	—	us	2
$t_{TA_PROG_SFP_VDD}$	0	—	us	3
$t_{TA_PROG_SFP_RST}$	0	—	us	4

Notes:

1. Delay required from the deassertion of PORESET_B to driving TA_PROG_SFP ramp up. Delay measured from PORESET_B deassertion at 90% OV_{DD} to 10% TA_PROG_SFP ramp up.

2. Delay required from fuse programming completion to TA_PROG_SFP ramp down start. Fuse programming must complete while TA_PROG_SFP is stable at 1.8 V. No activity other than that required for secure boot fuse programming is permitted while TA_PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while TA_PROG_SFP = GND. After fuse programming is complete, it is required to return TA_PROG_SFP = GND.

3. Delay required from TA_PROG_SFP ramp-down complete to V_{DD} ramp-down start. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before V_{DD} reaches 90% V_{DD}.

4. Delay required from TA_PROG_SFP ramp-down complete to PORESET_B assertion. TA_PROG_SFP must be grounded to minimum 10% TA_PROG_SFP before PORESET_B assertion reaches 90% OV_{DD}.

5. Only six secure boot fuse programming events are permitted per lifetime of a device.

3.3 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per the requirements in Power sequencing, it is required that TA_PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Power sequencing.

3.4 Power characteristics

This table provides the power dissipations of the V_{DD} supply and SerDes supply (SV_{DD}) for various operating platform clock frequencies versus the core and DDR clock frequencies.

Table 7. LS1046A core power dissipation[9]

Core frequency (MHz)	Platform/ FMan frequency (MHz)	DDR frequency (MHz)	V_{DD} (V)	SV_{DD} (V)	Junction temperature (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]	Notes
							V_{DD}	SV_{DD}[8]		
1800	700/800	2100	1.0	1.0	65	Typical	8.5	0.9	9.4	2, 3
					85	Thermal	11.4	0.9	12.3	4, 7
						Maximum	14.3	0.9	15.2	5, 6, 7
					105	Thermal	14.4	0.9	15.3	4, 7
						Maximum	17.3	0.9	18.2	5, 6, 7
1600	700/800	2100	1.0	1.0	65	Typical	7.7	0.9	8.7	2, 3
					85	Thermal	10.7	0.9	11.6	4, 7
						Maximum	13.2	0.9	14.2	5, 6, 7
					105	Thermal	13.7	0.9	14.6	4, 7
						Maximum	16.3	0.9	17.2	5, 6, 7
1400	600/600	2100	1.0	1.0	65	Typical	7.3	0.9	8.2	2, 3
					85	Thermal	8.7	0.9	9.6	4, 7
						Maximum	11.1	0.9	12.0	5, 6, 7
					105	Thermal	10.5	0.9	11.5	4, 7
						Maximum	12.9	0.9	13.8	5, 6, 7
1200	400/600	1600	1.0	1.0	65	Typical	6.4	0.9	7.3	2, 3, 10
					85	Thermal	7.7	0.9	8.6	4, 7, 10
						Maximum	9.8	0.9	10.7	5, 6, 7, 10

Table continues on the next page...

Table 7. LS1046A core power dissipation[9] (continued)

Core frequency (MHz)	Platform/ FMan frequency (MHz)	DDR frequency (MHz)	V_{DD} (V)	SV_{DD} (V)	Junction temperature (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]	Notes
							V_{DD}	SV_{DD}[8]		
					105	Thermal	9.6	0.9	10.5	4, 7, 10
						Maximum	11.6	0.9	12.5	5, 6, 7, 10
1200	400/600	1600	0.9	0.9	65	Typical	4.9	0.7	5.6	2, 3
					85	Thermal	5.9	0.7	6.6	4, 7
						Maximum	7.4	0.7	8.2	5, 6, 7
					105	Thermal	7.2	0.7	8.0	4, 7
						Maximum	8.8	0.7	9.5	5, 6, 7

1. Combined power of V_{DD} and SV_{DD} with DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 70% (on all cores) and executing DMA on the platform with 100% activity factor.
3. Typical power based on nominal, processed device.
4. Thermal power assumes Dhrystone running with activity factor of 70% (on all cores) and executing DMA on the platform at 100% activity factor.
5. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and executing DMA on the platform at 115% activity factor.
6. Maximum power is provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.
8. Total SV_{DD} Power conditions:
   a. SerDes 1 : XFI x2, 10 Gbaud
   b. SerDes 1 : SGMII x2, 1.25 Gbaud
   c. SerDes 2 : PEX x2, 5 Gbaud
9. Power numbers are only applicable to part numbering offering from Table 144. For example: A 1.8GHz offering part when runs at 1.4GHz will have power numbers higher than listed for 1.4GHz.
10. These power numbers are valid when purchasing the 1400MHz device and running the clocks at these conditions.

Table 8. LS1026A core power dissipation[9]

Core frequency (MHz)	Platform/ FMan frequency (MHz)	DDR frequency (MHz)	V_{DD} (V)	SV_{DD} (V)	Junction temperature (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]	Notes
							V_{DD}	SV_{DD}[8]		
1800	700/800	2100	1.0	1.0	65	Typical	6.7	0.9	7.6	2, 3
					85	Thermal	9.3	0.9	10.2	4, 7
						Maximum	11.5	0.9	12.4	5, 6, 7
					105	Thermal	12.3	0.9	13.2	4, 7
						Maximum	14.5	0.9	15.4	5, 6, 7
1600	700/800	2100	1.0	1.0	65	Typical	6.2	0.9	7.1	2, 3
					85	Thermal	8.7	0.9	9.6	4, 7
						Maximum	10.7	0.9	11.6	5, 6, 7
					105	Thermal	11.7	0.9	12.6	4, 7
						Maximum	13.7	0.9	14.6	5, 6, 7

Table continues on the next page...

Table 8. LS1026A core power dissipation[9] (continued)

Core frequency (MHz)	Platform/ FMan frequency (MHz)	DDR frequency (MHz)	V_{DD} (V)	SV_{DD} (V)	Junction temperature (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]	Notes
							V_{DD}	SV_{DD}[8]		
1400	600/600	2100	1.0	1.0	65	Typical	6.0	0.9	6.9	2, 3
					85	Thermal	7.2	0.9	8.1	4, 7
						Maximum	9.1	0.9	10.0	5, 6, 7
					105	Thermal	9.0	0.9	10.0	4, 7
						Maximum	10.9	0.9	11.8	5, 6, 7
1200	400/600	1600	1.0	1.0	65	Typical	5.2	0.9	6.2	2, 3, 10
					85	Thermal	6.4	0.9	7.3	4, 7, 10
						Maximum	8.0	0.9	9.0	5, 6, 7, 10
					105	Thermal	8.3	0.9	9.2	4, 7, 10
						Maximum	9.9	0.9	10.8	5, 6, 7, 10
1200	400/600	1600	0.9	0.9	65	Typical	3.9	0.7	4.7	2, 3
					85	Thermal	4.7	0.7	5.5	4, 7
						Maximum	6.0	0.7	6.7	5, 6, 7
					105	Thermal	6.1	0.7	6.9	4, 7
						Maximum	7.3	0.7	8.1	5, 6, 7

1. Combined power of V_{DD} and SV_{DD} with DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform with 100% activity factor.
3. Typical power based on nominal, processed device.
4. Thermal power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform at 100% activity factor.
5. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and executing DMA on the platform at 115% activity factor.
6. Maximum power is provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.
8. Total SV_{DD} power conditions:
   a. SerDes 1 : XFI x2, 10 Gbaud
   b. SerDes 1 : SGMII x2, 1.25 Gbaud
   c. SerDes 2 : PEX x2, 5 Gbaud
9. Power numbers are only applicable to part numbering offering from Table 144. For example: A 1.8GHz offering part when runs at 1.4GHz will have power numbers higher than listed for 1.4GHz.
10. These power numbers are valid when purchasing the 1400MHz device and running the clocks at these conditions.

3.4.1 Low-power mode saving estimation

See this table for low-power mode savings.

Table 9. Low-power mode savings, 65C[1, 2, 3]

Mode	Core Frequency = 1.2 GHz (VDD =0.9V)	Core Frequency = 1.2 GHz (VDD =1.0V)	Core Frequency = 1.4 GHz (VDD =1.0V)	Core Frequency = 1.6 GHz (VDD =1.0V)	Core Frequency = 1.8 GHz (VDD =1.0V)	Units	Comments	Notes
PW15	0.71	0.74	0.77	0.88	0.99	Watts	Saving realized moving from run to PW15 state, single core. Arm in STANDBYWFI/WFE	4
PH20	0.05	0.17	0.21	0.24	0.26	Watts	Saving realized moving from PW15 to PH20 state, single core. Arm in STANDBYWFI/ WFE-retain	
LPM20	1.02	1.46	1.70	1.94	2.18	Watts	Saving realized moving from PW15 to LPM20 per device	5

Notes:

1. Power for VDD only
2. Typical power assumes Dhrystone running with activity factor of 70%
3. Typical power based on nominal process distribution for this device.
4. PW15 power savings with 1 core. Maximum savings would be N times, where N is the number of used cores.
5. LPM20 has all platform clocks disabled.

3.5 I/O power dissipation

This table provides the estimated I/O power numbers for each block: DDR, PCI Express, IFC, Ethernet controller, SGMII, eSDHC, USB, SPI, DUART, IIC, SATA, and GPIO. Note that these numbers are based on design estimates only.

Table 10. IO power supply estimated values

Interface	Parameter	Symbol	Typical	Unit	Notes
DDR4	x64 2100 MT/s data rate	G1VDD (1.2 V)	990	mW	1, 2
	x64 1600 MT/s data rate		860		
	x64 2100 MT/s data rate		761	mW	1, 7
	x64 1600 MT/s data rate		660		
	x32 2100 MT/s data rate		740	mW	1, 2

Table continues on the next page...

Table 10. IO power supply estimated values (continued)

	x32 1600 MT/s data rate		637		
	x32 2100 MT/s data rate		518	mW	1, 7
	x32 1600 MT/s data rate		490		
PCI Express	x1, 2.5 Gbaud	XVDD (1.35 V)	79	mW	1, 3
	x2, 2.5 Gbaud		132	mW	
	x4, 2.5 Gbaud		237	mW	
	x1, 5 Gbaud		80	mW	
	x2, 5 Gbaud		133	mW	
	x4, 5 Gbaud		239	mW	
	x1, 8 Gbaud		81	mW	
	x2, 8 Gbaud		136	mW	
	x4, 8 Gbaud		245	mW	
SGMII	x1, 1.25 Gbaud	XVDD (1.35 V)	77	mW	1, 3
	x2, 1.25 Gbaud		127	mW	
	x3, 1.25 Gbaud		177	mW	
	x4, 1.25 Gbaud		227	mW	
	x1, 3.125 Gbaud		79	mW	
	x2, 3.125 Gbaud		132	mW	
	x3, 3.125 Gbaud		184	mW	
QSGMII	x1, 5 Gbaud	XVDD (1.35 V)	80	mW	1, 3
XFI	x1, 10 Gbaud	XVDD (1.35 V)	81	mW	1, 3
	x2, 10 Gbaud		136	mW	
SATA (per port)	3.0 Gbaud	XVDD (1.35 V)	73	mW	1, 3
	6.0 Gbaud		74	mW	
USB1/USB2/USB3 (per PHY)	x1 Super speed mode	USB_HVDD (3.3 V)	46	mW	1, 5
		USB_SVDD (1 V)	37	mW	
		USB_SDVDD (1 V)	4	mW	
USB1/USB2/USB3 (per PHY)	x1 High speed mode	USB_HVDD (3.3 V)	79	mW	1, 5
		USB_SVDD (1 V)	0.31	mW	
		USB_SDVDD (1 V)	4.9	mW	
IFC	16-bit, 100 MHz	OVDD (1.8 V)	60	mW	1
DUART	.	DVDD (3.3 V)	18	mW	1
		DVDD (1.8 V)	9	mW	
I2C	.	DVDD (3.3 V)	17	mW	1
		DVDD (1.8 V)	9	mW	
SPI	.	OVDD (1.8 V)	8	mW	1, 9
eSDHC	.	EVDD (3.3 V)	19	mW	1, 9
	.	EVDD (1.8V)	21	mW	

Table continues on the next page...

Table 10. IO power supply estimated values (continued)

System control	.	OVDD (1.8 V)	16	mW	1, 9
EC1	RGMII	LVDD (2.5 V)	24	mW	1, 9
		LVDD (1.8 V)	17	mW	
EC2	RGMII	LVDD (2.5 V)	24	mW	
		LVDD (1.8 V)	17	mW	
QSPI	.	OVDD (1.8V)	17	mW	1, 9
IEEE1588	.	LVDD (2.5 V)	14	mW	1, 9
		LVDD (1.8 V)	10	mW	
JTAG + DFT	.	OVDD (1.8V)	10	mW	1, 9
GPIO	x8	3.3 V	5	mW	1, 4, 9
		2.5 V	4	mW	
		1.8 V	3	mW	
PLL core and system (per PLL)	.	AVDD_CGA1, AVDD_CGA2, AVDD_PLAT (1.8 V)	30	mW	1, 9
PLL DDR	.	AVDD_D1 (1.8 V)	30	mW	1, 9
PLL SerDes	.	AVDD_SD1_PLL1, AVDD_SD1_PLL2, AVDD_SD2_PLL1, AVDD_SD2_PLL2 (1.35 V)	100	mW	1, 9
Interrupts (IRQ)	.	OVDD (1.8 V)	4	mW	1
		DVDD (1.8 V)	9	mW	
		DVDD (3.3 V)	18	mW	
		LVDD (2.5 V)	2	mW	
		LVDD (1.8 V)	1	mW	
Ethernet management interface 1	.	LVDD (2.5 V)	3	mW	1
		LVDD (1.8 V)	2	mW	
Ethernet management interface 2	.	TVDD (2.5 V)	3	mW	1
		TVDD (1.8 V)	2	mW	
		TVDD (1.2 V)	2	mW	
TA_PROG_SFP	.	TA_PROG_SFP (1.8 V)	173	mW	6
TH_VDD	.	TH_VDD (1.8 V)	18	mW	

1. The typical values are estimates and based on simulations at nominal recommended voltage for the I/O power supply and assuming 105°C junction temperature.

2. Typical DDR4 power numbers are based on two Rank DIMM with 40% utilization.

3. The total power numbers of XVDD is dependent on customer application use case. This table lists all the SerDes configurations possible for the device. To get the X1VDD power numbers, the user should add the combined lanes to match to the total SerDes Lanes used, not simply multiply the power numbers by the number of lanes.

4. GPIOs are supported on OVDD, LVDD, DVDD, TVDD and EVDD power rails.

5. USB power supply pins are shared between three USB controllers.

Table 10. IO power supply estimated values

6. The maximum power requirement is during programming. No active power beyond leakage levels should be drawn and the supply must be grounded when not programming.
7. Typical DDR4 power numbers are based on single Rank DIMM with 40% utilization.
9. Assuming 15 pF total capacitance load per pin.

Table 11. TA_BB_VDD power dissipation

Supply	Maximum	Unit	Notes
TA_BB_VDD (SoC off, 40°C)	40	µW	1
TA_BB_VDD (SoC off, 70°C)	55	µW	1
Note: 1. When SoC is off, TA_BB_VDD may be supplied by battery power to retain the Zeroizable Master Key and other trust architecture state. Board should implement a PMIC, which switches TA_BB_VDD to battery when SoC is powered down. See the Device reference manual trust architecture chapter for more information.			

3.6 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 12. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/DV_{DD}/$G1V_{DD}$/ SV_{DD}/XV_{DD}/LV_{DD}/EV_{DD}/TV_{DD} all core and platform V_{DD} supplies, TA_PROG_SFP, and all AV_{DD} supplies.)	—	25	V/ms	1, 2
Required ramp rate for TA_PROG_SFP	---	25	V/ms	1,2
Required ramp rate for USB_HVDD	---	26.7	V/ms	1,2
Notes: 1. Ramp rate is specified as a linear ramp from 10% to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 mV to 500 mV is the most critical as this range might falsely trigger the ESD circuitry. 2. Over full recommended operating temperature range. See Table 4.				

3.7 Input clocks

3.7.1 System clock (SYSCLK)

This section describes the system clock DC electrical characteristics and AC timing specifications.

3.7.1.1 SYSCLK DC electrical characteristics

This table provides the SYSCLK DC characteristics.

Table 13. SYSCLK DC electrical characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	—	V	1
Input low voltage	V_{IL}	—	—	0.3 x OV_{DD}	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (V_{IN}= 0 V or V_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 4.
2. At recommended operating conditions with OV_{DD}= 1.8 V. See Table 4.

3.7.1.2 SYSCLK AC timing specifications

This table provides the SYSCLK AC timing specifications.

Table 14. SYSCLK AC timing specifications[1, 5]

Parameter/condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}		100.0		MHz	1
SYSCLK cycle time	t_{SYSCLK}		10.0		ns	1
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	1
SYSCLK slew rate	—	1	—	4	V/ns	2
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase noise at -56 dBc	—	—	—	500	kHz	3
AC Input Swing Limits at 1.8 V OV_{DD}	ΔV_{AC}	1.08	—	1.8	V	—

Notes:

1. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
2. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.
3. Phase noise is calculated as FFT of TIE jitter.
4. At recommended operating conditions with OV_{DD} = 1.8 V. See Table 4.

3.7.1.3 USB 3.0 reference clock requirements

This table summarizes the requirements of the reference clock provided to the USB 3.0 SSPHY. There are two options for the reference clock of USB PHY: SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B. The following table provides the additional requirements when SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B is used as USB REFCLK. This table can also be used for 100 MHz reference clock requirements.

Table 15. Reference clock requirements

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Reference clock frequency offset	FREF_OFFSET	-300	—	300	ppm	—
Reference clock random jitter (RMS)	RMSJREF_CLK	—	—	3	ps	1, 2
Reference clock deterministic jitter	DJREF_CLK	—	—	150	ps	3
Duty cycle	DCREF_CLK	40	—	60	%	—

Notes:

1. 1.5 MHz to Nyquist frequency. For example, for 100 MHz reference clock, the Nyquist frequency is 50 MHz.
2. The peak-to-peak Rj specification is calculated as 14.069 times the RMS Rj for 10-12 BER.
3. DJ across all frequencies.

3.7.2 Spread-spectrum sources

Spread-spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content.

The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement.

Frequency modulation and spread are separate concerns; the chip is compatible with spread-spectrum sources if the recommendations listed in this table are observed.

Table 16. Spread-spectrum clock source recommendations[1]

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	—

Notes:

1. At recommended operating conditions with OVDD = 1.8 V. See Table 4.

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded, regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should use only down-spreading to avoid violating the stated limits.

3.7.3 Real-time clock timing (RTC)

The real-time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the Watchdog, Flextimer, 1588 Timer and snvs unit; there is no need for jitter specification. The minimum period of the RTC signal should be greater than or equal to 16x the period of the platform clock with a 50% duty cycle. There is no minimum RTC frequency; RTC may be pulled to ground, if not needed.

3.7.4 Gigabit Ethernet reference clock timing

This table provides the Ethernet gigabit reference clock DC electrical characteristics with LV_{DD} = 2.5 V / 1.8 V.

Table 17. EC*n*_GTX_CLK125 DC electrical characteristics (LV_{DD} = 2.5 V / 1.8 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	—	—	V	2
Input low voltage	V_{IL}	—	—	0.2 x LV_{DD}	V	2
Input capacitance	C_{IN}	—	—	6	pF	—
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	—	—	± 50	μA	3

Notes:

1. For recommended operating conditions, see Table 4.
2. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values found in Table 4.
3. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 4.

This table provides the Ethernet gigabit reference clock AC timing specifications.

Table 18. EC*n*_GTX_CLK125 AC timing specifications [1]

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 frequency	f_{G125}	125 - 100 ppm	125	125 + 100 ppm	MHz	—
EC*n*_GTX_CLK125 cycle time	t_{G125}	--	8	--	ns	—
EC*n*_GTX_CLK125 rise and fall time	t_{G125R}/t_{G125F}	—	—	0.75	ns	2
EC*n*_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	40	—	60	%	3

Notes:

1. At recommended operating conditions with LV_{DD} = 1.8 V ± 90mV / 2.5 V ± 125 mV. See Table 4.
2. Rise times are measured from 20% of LV_{DD} to 80% of LV_{DD}. Fall times are measured from 80% of LV_{DD} to 20% of LV_{DD}.
3. EC*n*_GTX_CLK125 is used to generate the GTX clock for the Ethernet transmitter. See RGMII AC timing specifications for duty cycle for the 10Base-T and 100Base-T reference clocks.

3.7.5 DDR clock (DDRCLK)

This section provides the DDRCLK DC electrical characteristics and AC timing specifications.

3.7.5.1 DDRCLK DC electrical characteristics

This table provides the DDRCLK DC electrical characteristics.

Table 19. DDRCLK DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	—	V	1
Input low voltage	V_{IL}	—	—	0.3 x OV_{DD}	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (V_{IN}= 0V or V_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 4.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 4.
3. At recommended operating conditions with OV_{DD} = 1.8 V. See Table 4.

3.7.5.2 DDRCLK AC timing specifications

This table provides the DDRCLK AC timing specifications.

Table 20. DDRCLK AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}		100.0		MHz	1, 2
DDRCLK cycle time	t_{DDRCLK}		10.0		ns	1, 2
DDRCLK duty cycle	t_{KHK}/t_{DDRCLK}	40	—	60	%	2
DDRCLK slew rate	—	1	—	4	V/ns	3
DDRCLK peak period jitter	—	—	—	± 150	ps	—
DDRCLK jitter phase noise at -56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits at 1.8 V OV_{DD}	ΔV_{AC}	1.08	—	1.8	V	—

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting DDRCLK frequencies do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.
4. Phase noise is calculated as FFT of TIE jitter.
5. At recommended operating conditions with OV_{DD} = 1.8V. See Table 4.

3.7.6 Differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) timing specifications

Single Source clocking mode requires single onboard oscillator to provide reference clock input to Differential System clock pair (DIFF_SYSCLK/DIFF_SYSCLK_B).

This Differential clock pair input provides clock to Core, Platform, DDR and USB PLL's

This figure shows a receiver reference diagram of the Differential System clock.

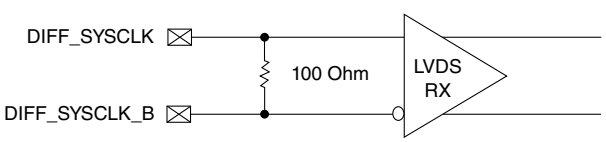


Figure 10. LVDS receiver

This section provides the differential system clock DC and AC timing specifications.

3.7.6.1 Differential system clock DC electrical characteristics

The differential system clock receiver voltage requirements are as specified in the Recommended operating conditions table.

The differential system clock can also be single-ended. For this, DIFF_SYSCLK_B should be connected to $OV_{DD}/2$.

This table provides the differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) DC specifications.

Table 21. Differential system clock DC electrical characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage swing	V_{id}	100	-	600	mV	2
Input common mode voltage	V_{icm}	50	-	1570	mV	-
Power supply current	I_{cc}	-	-	5	mA	-
Input capacitance	C_{in}	1.45	1.5	1.55	pF	-

Note:

1. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 4 for details.
2. Input differential voltage swing (Vid) specified is equal to |VDIFF_SYSCLK_P - VDIFF_SYSCLK_N|

This figure shows the differential system clock (DIFF_SYSCLK) input DC specifications.

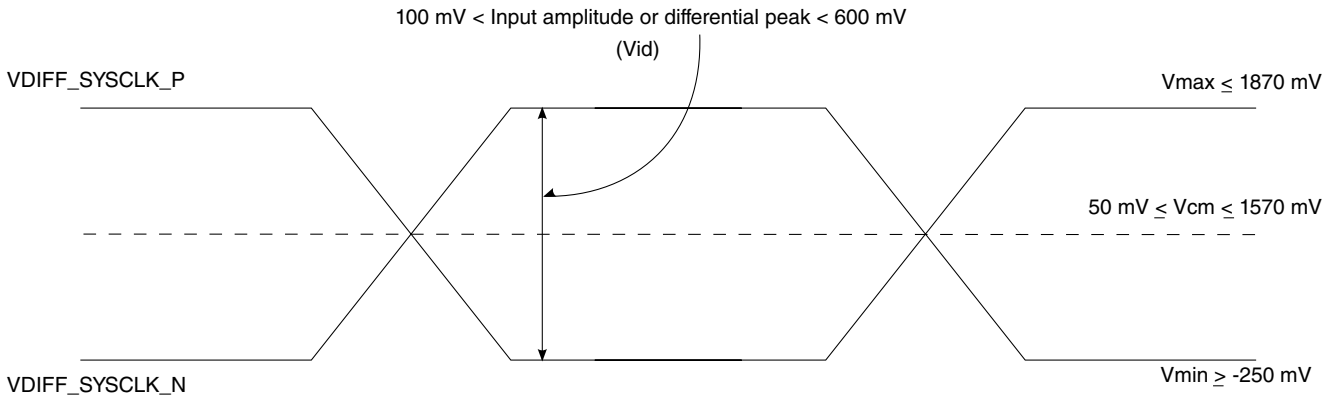


Figure 11. DIFF_SYSCLK input DC requirements (external DC-coupled)

3.7.6.2 Differential system clock AC timing specifications

Spread spectrum clocking is not supported on differential system clock pair input.

This table provides the differential system clock (DIFF_SYSCLK/DIFF_SYSCLK_B) AC specifications.

Table 22. Differential system clock AC electrical characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
DIFF_SYSCLK/DIFF_SYSCLK_B frequency range	t_{DIFF_SYSCLK}	-	100	-	MHz	-
DIFF_SYSCLK/DIFF_SYSCLK_B frequency tolerance	t_{DIFF_TOL}	-300	-	+300	ppm	-

Table continues on the next page...

Table 22. Differential system clock AC electrical characteristics[1] (continued)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Duty cycle	t_{DIFF_DUTY}	40	50	60	%	-

Note:

1. This is evaluated with supply noise profile at +/- 5% sine wave
2. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 4

3.7.7 Other input clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information about the input clock requirements of functional sourced external of the chip, such as SerDes, Ethernet management, eSDHC, and IFC, see the specific interface section.

3.8 RESET initialization

This table provides the AC timing specifications for the RESET initialization timing.

Table 23. RESET Initialization timing specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of PORESET_B after all power rails are stable	1	—	ms	1
Required input assertion time of HRESET_B	32	—	SYSCLKs	2, 3
Maximum rise/fall time of HRESET_B	—	10	SYSCLK	4, 6
Maximum rise/fall time of PORESET_B	—	1	SYSCLK	4, 7
Input setup time for POR configs (other than cfg_eng_use0) with respect to negation of PORESET_B	4	—	SYSCLKs	2, 5
Input hold time for all POR configs with respect to negation of PORESET_B	2	—	SYSCLKs	2
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	—	5	SYSCLKs	2

Notes:

1. PORESET_B must be driven asserted before the core and platform power supplies are powered up.
2. SYSCLK is the primary clock input for the chip.
3. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The device releases HRESET_B sometime after PORESET_B is deasserted. The exact sequencing of HRESET_B deassertion is documented in the reference manual's "Power-on Reset Sequence" section.
4. The system/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.
5. For proper clock selection, terminate cfg_eng_use0 with a pull up or pull down of 4.7 kΩ to ensure that the signal will have a valid state as soon as the IO voltage reach its operating condition.

Table 23. RESET Initialization timing specifications

Parameter/Condition	Min	Max	Unit	Notes
6. For HRESET_B the rise/fall time should not exceed 10 SYSCLKs. Rise time refers to signal transitions from 20% to 70% of O1VDD. Fall time refers to transitions from 70% to 20% of O1VDD.				
7. For PORESET_B the rise/fall time should not exceed 1 SYSCLK. Rise time refers to signal transitions from 20% to 70% of OVDD. Fall time refers to transitions from 70% to 20% of OVDD.				

3.9 DDR4 SDRAM controller

This section describes the DC and AC electrical specifications for the DDR4 SDRAM controller interface. Note that the required $G1V_{DD}$(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

3.9.1 DDR4 SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR4 SDRAM.

Table 24. DDR4 SDRAM interface DC electrical characteristics ($G1V_{DD}$ = 1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input low	V_{IL}	—	0.7 x $G1V_{DD}$ - 0.175	V	3
Input high	V_{IH}	0.7 x $G1V_{DD}$ + 0.175	—	V	3
I/O leakage current	I_{OZ}	-200	200	μA	

Notes:

1. $G1V_{DD}$ is expected to be within 60 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. V_{TT} and VREFCA are applied directly to the DRAM device. Both V_{TT} and VREFCA voltages must track $G1V_{DD}/2$.
3. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
4. See the IBIS model for the complete output IV curve characteristics.
5. Output leakage is measured with all outputs disabled, 0V ≤ VOUT ≤ $G1V_{DD}$
6. For recommended operating conditions, see Table 4.

3.9.2 DDR4 SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR4 memories. Note that the required GV_{DD}(typ) voltage is 1.2 V when interfacing to DDR4 SDRAM.

3.9.2.1 DDR4 SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 25. DDR4 SDRAM interface input AC timing specifications [1]

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage ≤ 2100 MT/s data rate	V_{ILAC}	—	0.7 x $G1V_{DD}$ - 0.175	V	—
AC input high voltage ≤ 2100 MT/s data rate	V_{IHAC}	0.7 x $G1V_{DD}$ + 0.175	—	V	—

Note:

1. For recommended operating conditions, see Table 4.

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR4 SDRAM.

Table 26. DDR4 SDRAM interface input AC timing specifications [3]

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS-MDQ/MECC	t_{CISKEW}	—	—	ps	1
2100 MT/s data rate		-80	80		
1800 MT/s data rate		-93	93		
1600 MT/s data rate		-112	112		
1300 MT/s data rate		-125	125		
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}	—	—	ps	2
2100 MT/s data rate		-154	154		
1800 MT/s data rate		-175	175		
1600 MT/s data rate		-200	200		
1300 MT/s data rate		-250	250		

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.

2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

3. For recommended operating conditions, see Table 4.

This figure shows the DDR4 SDRAM interface input timing diagram.

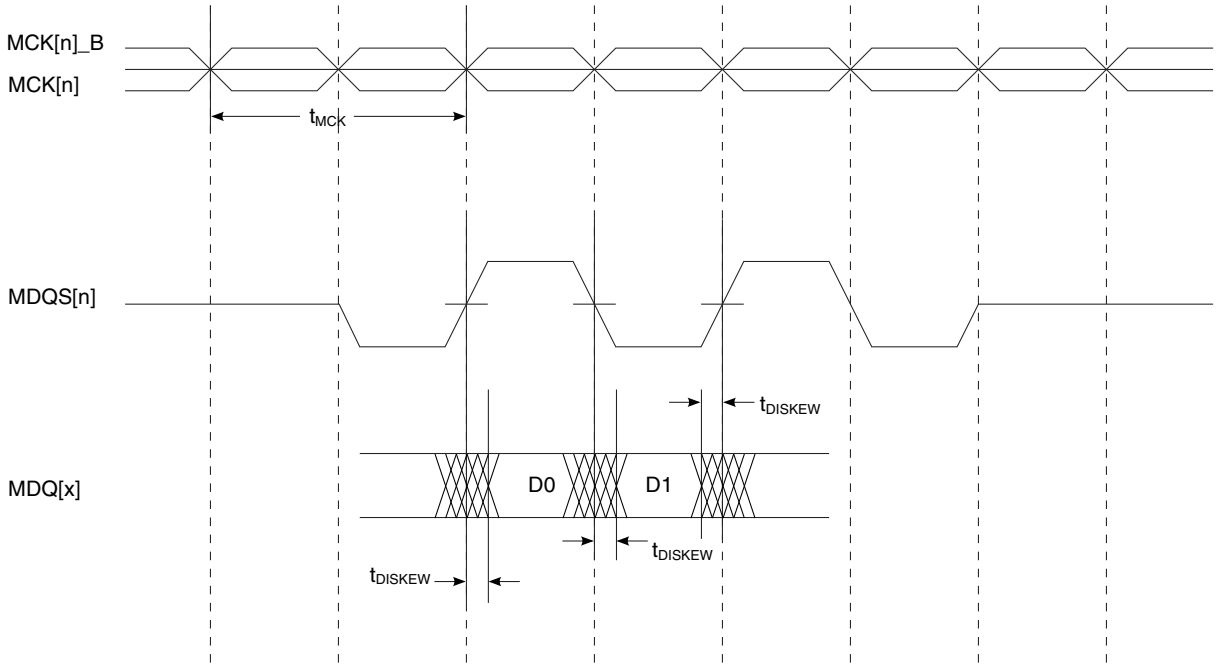


Figure 12. DDR4 SDRAM interface input timing diagram

3.9.2.2 DDR4 SDRAM interface output AC timing specifications

This table contains the output AC timing targets for the DDR4 SDRAM interface.

Table 27. DDR4 SDRAM interface output AC timing specifications ($G1V_{DD}$ = 1.2 V)[7]

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	952	1538	ps	2
ADDR/CMD/CNTL output setup with respect to MCK	t_{DDKHAS}	—	—	ps	3
2100 MT/s data rate		350	—		
1800 MT/s data rate		410	—		
1600 MT/s data rate		495	—		
1300 MT/s data rate		606	—		
ADDR/CMD/CNTL output hold with respect to MCK	t_{DDKHAX}	—	—	ps	3
2100 MT/s data rate		350	—		
1800 MT/s data rate		390	—		
1600 MT/s data rate		495	—		
1300 MT/s data rate		606	—		
MCK to MDQS Skew	t_{DDKHMH}	-150	150	ps	4,7
MDQ/MECC/MDM output data eye	$t_{DDKXDEYE}$	—	—	ps	5
2100 MT/s data rate		320	—		
1800 MT/s data rate		350	—		

Table continues on the next page...

Table 27. DDR4 SDRAM interface output AC timing specifications ($G1V_{DD}$ = 1.2 V)[7] (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
1600 MT/s data rate		400	—		
1300 MT/s data rate		500	—		
MDQS preamble	t_{DDKHMP}	0.9 x t_{MCK}	—	ps	—
MDQS postamble	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ps	—

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.

2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.

3. ADDR/CMD/CNTL includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.

4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the chip reference manual for a description and explanation of the timing modifications enabled by the use of these bits.

5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.

6. Note that this is required to program the start value of the DQS adjust for write leveling.

7. For recommended operating conditions, see Table 4.

NOTE

For the ADDR/CMD/CNTL setup and hold specifications in Table 27, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure shows the DDR4 SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

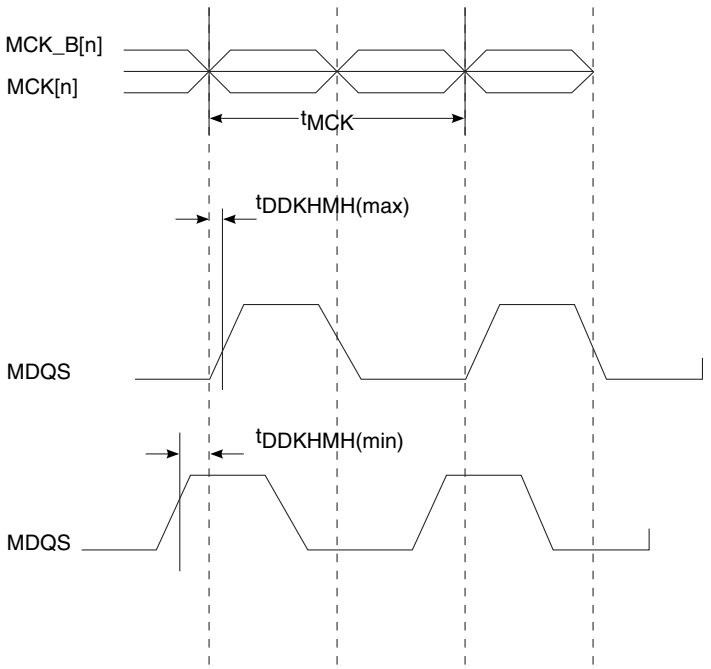


Figure 13. t_{DDKHMH} timing diagram

This figure shows the DDR4 SDRAM output timing diagram.

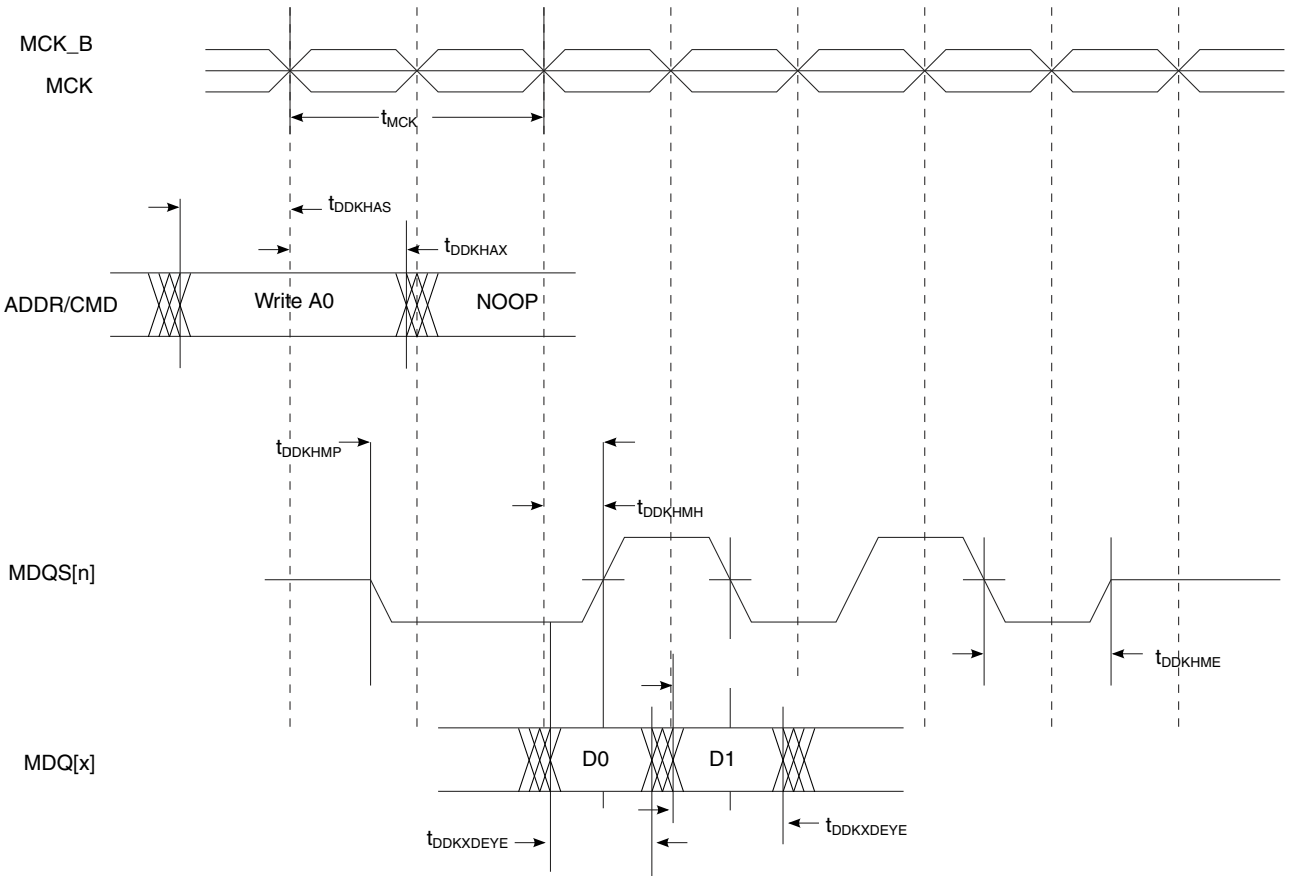


Figure 14. DDR4 output timing diagram

3.10 Ethernet interface, Ethernet management interface, IEEE Std 1588™

This section describes the DC and AC electrical characteristics for the Ethernet controller, Ethernet management, and IEEE Std 1588 interfaces.

3.10.1 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 15, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to GND*n*. The reference circuit of the SerDes transmitter and receiver is shown in Figure 85.

3.10.1.1 SGMII clocking requirements for SDn_REF_CLK1_P and SDn_REF_CLK1_N

When operating in SGMII mode, the EC*n*_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SDn_REF_CLK[1:2]_P and SDn_REF_CLK[1:2]_N pins. SerDes lanes may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.10.1.2 SGMII DC electrical characteristics

This section describes the electrical characteristics for the SGMII interface.

3.10.1.2.1 SGMII and SGMII 2.5G transmit DC specifications

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N) as shown in Figure 16.

Table 28. SGMII DC transmitter electrical characteristics (X*n*V_{DD} = 1.35 V)[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	-	-	1.5 x $\lvert V_{OD} \rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD} \rvert_{-min}/2$	-	-	mV	1
Output differential voltage[2, 3, 5]	$\lvert V_{OD} \rvert$	320	500.0	725.0	mV	TECR0[AMP_RED]=0b000000
(XV_{DD-Typ} at 1.35 V)		293.8	459.0	665.6		TECR0[AMP_RED]=0b000001
		266.9	417.0	604.7		TECR0[AMP_RED]=0b000011
		240.6	376.0	545.2		TECR0[AMP_RED]=0b000010
		213.1	333.0	482.9		TECR0[AMP_RED]=0b000110
		186.9	292.0	423.4		TECR0[AMP_RED]=0b000111
		160.0	250.0	362.5		TECR0[AMP_RED]=0b010000
Output impedance (differential)	R_O	80	100	120	Ω	-

Notes:

1. This does not align to DC-coupled SGMII.
2. $\lvert V_{OD} \rvert = \lvert V_{SD_TXn_P} - V_{SD_TXn_N} \rvert$. $\lvert V_{OD} \rvert$ is also referred to as output differential peak voltage. $V_{TX-DIFFp-p} = 2 \times \lvert V_{OD} \rvert$.
3. The $\lvert V_{OD} \rvert$ value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.35 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SDn _TXn_P and SDn_TXn_N.

Table 28. SGMII DC transmitter electrical characteristics (XnV_{DD} = 1.35 V)[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
4. For recommended operating conditions, see Table 4.						
5. Example amplitude reduction setting for SGMII on SerDes1 lane A: LNATECR0[AMP_RED] = 0b000001 for an output differential voltage of 459 mV typical.						

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

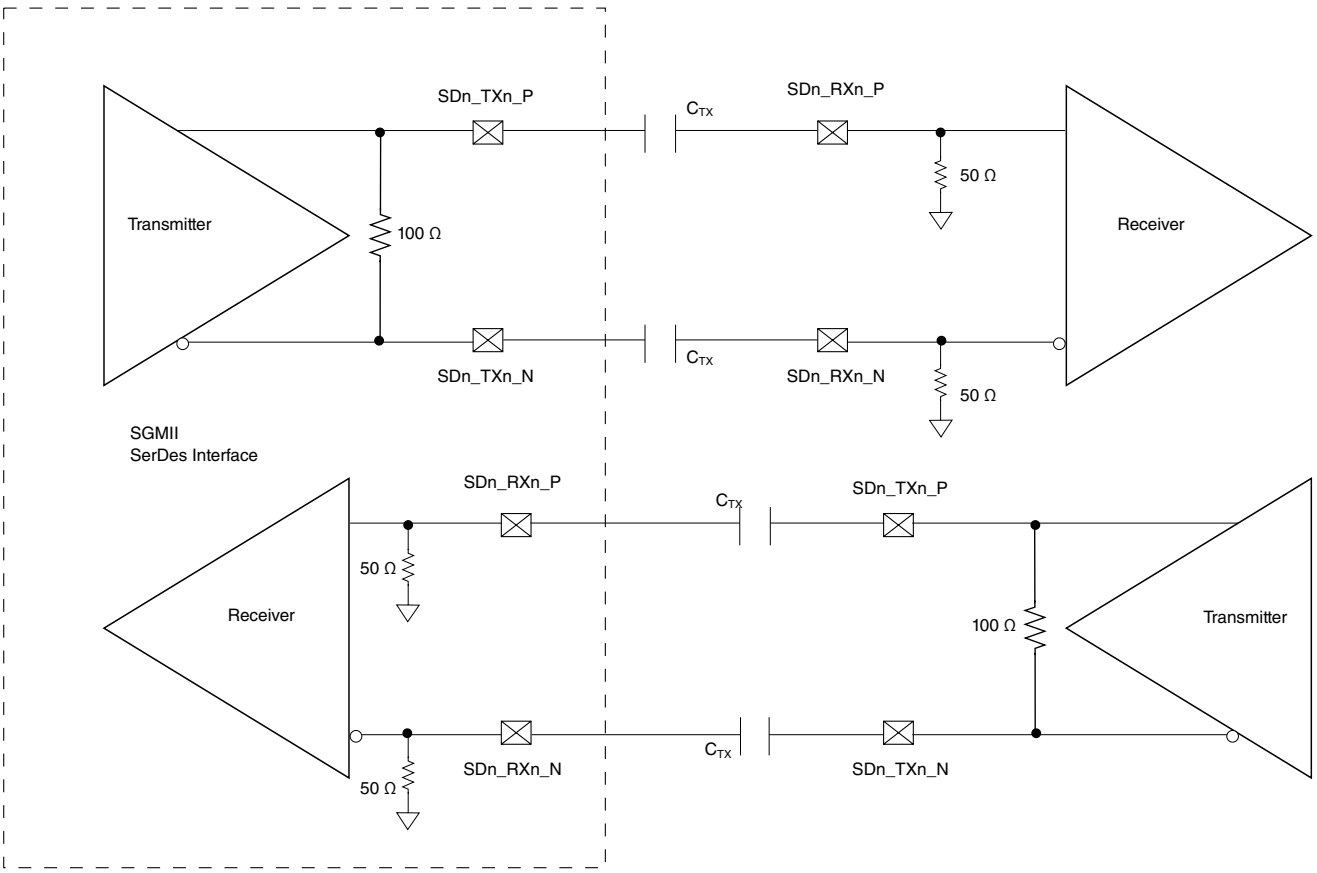


Figure 15. 4-wire AC-coupled SGMII serial link connection example

This figure shows the SGMII transmitter DC measurement circuit.

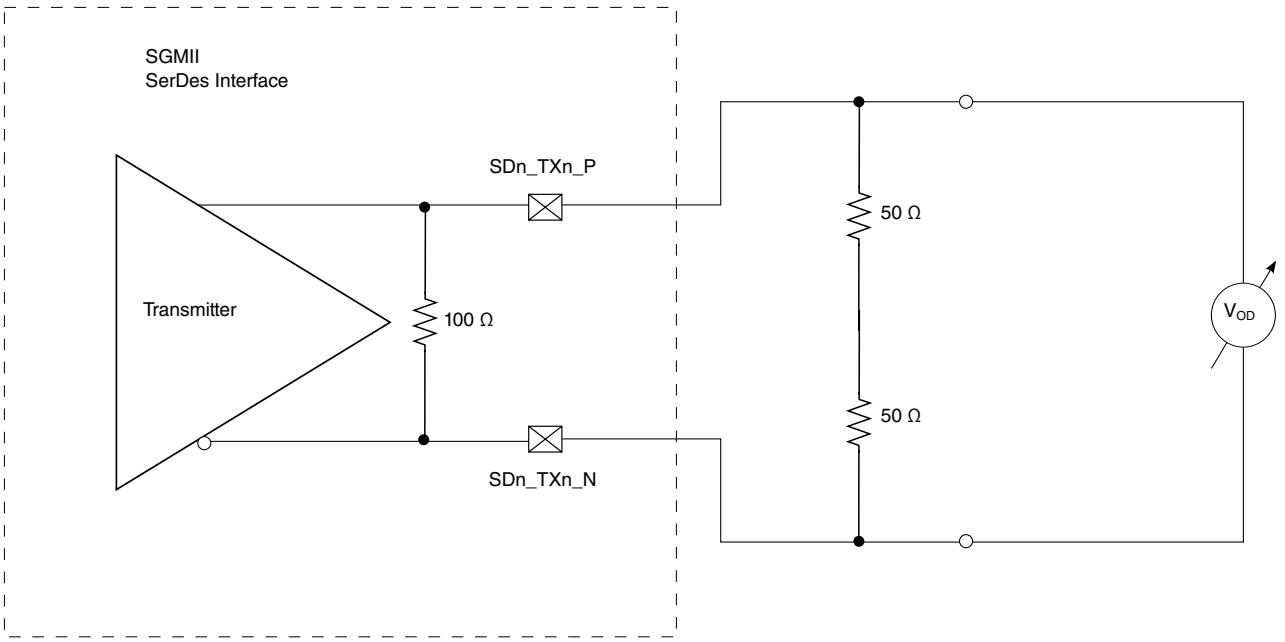


Figure 16. SGMII transmitter DC measurement circuit

This table defines the SGMII 2.5G transmitter DC electrical characteristics for 3.125 GBaud.

Table 29. SGMII 2.5G transmitter DC electrical characteristics (X*n*V_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$\lvert V_{OD} \rvert$	400	-	600	mV	
Output impedance (differential)	R_O	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 4.						

3.10.1.2.2 SGMII and SGMII 2.5G DC receiver electrical characteristics

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 30. SGMII DC receiver electrical characteristics [4]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC input voltage range		-	N/A			-	1
Input differential voltage	REIDL_TH = 001	$V_{RX_DIFFp\text{-}p}$	100	-	1200	mV	2, 5
	REIDL_TH = 100		175	-			
Loss of signal threshold	REIDL_TH = 001	V_{LOS}	30	-	100	mV	3, 5
	REIDL_TH = 100		65	-	175		

Table continues on the next page...

Table 30. SGMII DC receiver electrical characteristics [4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver differential input impedance	Z_{RX_DIFF}	80	-	120	Ω	-

Notes:

1. Input must be externally AC coupled.
2. $V_{RX_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See PCI Express DC physical layer receiver specifications, and PCI Express AC physical layer receiver specifications, for further explanation.
4. For recommended operating conditions, see Table 4.
5. The REIDL_TH shown in the table refers to the chip's SRDSxLNmGCR1[REIDL_TH] bit field.

This table defines the SGMII 2.5G receiver DC electrical characteristics for 3.125 GBaud.

Table 31. SGMII 2.5G receiver DC timing specifications [1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX_DIFFp\text{-}p}$	200	-	1200	mV	-
Loss of signal threshold	V_{LOS}	75	-	200	mV	-
Receiver differential input impedance	Z_{RX_DIFF}	80	-	120	Ω	-

Notes:

1. For recommended operating conditions, see Table 4.

3.10.1.3 SGMII AC timing specifications

This section describes the AC timing specifications for the SGMII interface.

3.10.1.3.1 SGMII and SGMII 2.5G transmit AC timing specifications

This table provides the SGMII and SGMII 2.5G transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 32. SGMII transmit AC timing specifications[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	-	-	0.17	UI p-p	-
Total jitter	JT	-	-	0.35	UI p-p	2
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5G SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1

Table continues on the next page...

Table 32. SGMII transmit AC timing specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
AC coupling capacitor	C_{TX}	10	-	200	nF	3

Notes:

1. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.
2. See Figure 18 for single frequency sinusoidal jitter measurements.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter output.
4. For recommended operating conditions, see Table 4.

3.10.1.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD*n*_TX*n*_P and SD*n*_TX*n*_N) or at the receiver inputs (SD*n*_RX*n*_P and SD*n*_RX*n*_N) respectively, as shown in this figure.

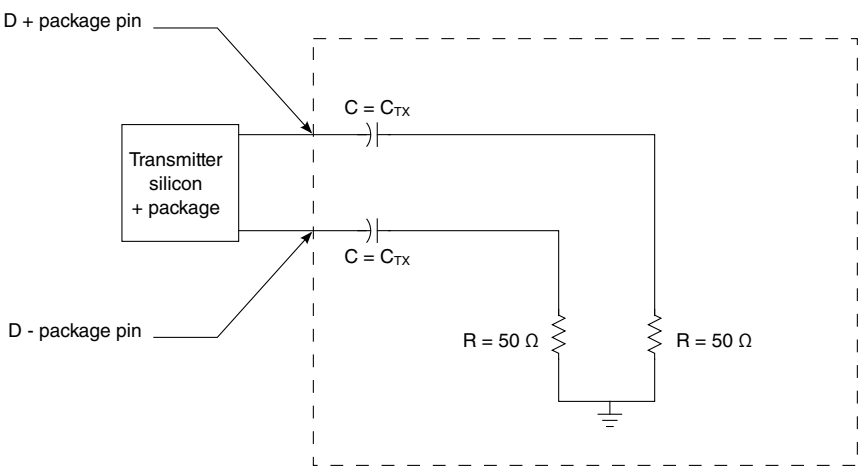


Figure 17. SGMII AC test/measurement load

3.10.1.3.3 SGMII and SGMII 2.5G receiver AC timing specifications

This table provides the SGMII and SGMII 2.5G receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 33. SGMII receiver AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1

Table continues on the next page...

Table 33. SGMII receiver AC timing specifications[3] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2
Bit error ratio	BER	-	-	10^{-12}	-	-
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5G SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1

Notes:

1. Measured at receiver

2.Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 18. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

3. For recommended operating conditions, see Table 4.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of this figure.

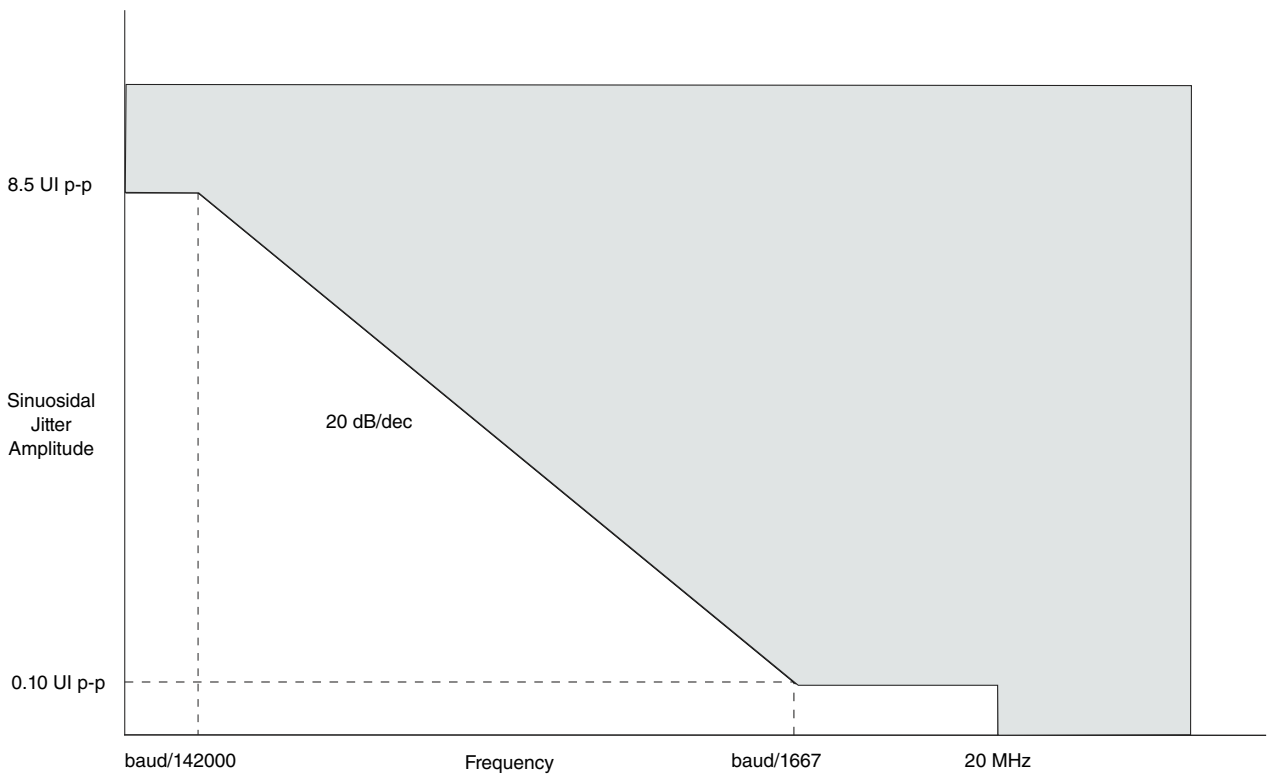


Figure 18. Single-frequency sinusoidal jitter limits

3.10.2 QSGMII interface

This section describes the QSGMII clocking and its DC and AC electrical characteristics.

3.10.2.1 QSGMII clocking requirements for SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

For more information on these specifications, see SerDes reference clocks.

3.10.2.2 QSGMII DC electrical characteristics

This section discusses the electrical characteristics for the QSGMII interface.

3.10.2.2.1 QSGMII transmitter DC specifications

This table describes the QSGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n* and SD*n*_TX*n*_B).

Table 34. QSGMII DC transmitter electrical characteristics (X*n*V_{DD} = 1.35V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	V_{DIFF}	400	-	900	mV	-
Differential resistance	T_{RD}	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 4.						

3.10.2.2.2 QSGMII DC receiver electrical characteristics

This table defines the QSGMII receiver DC electrical characteristics.

Table 35. QSGMII receiver DC timing specifications [1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	V_{DIFF}	100	-	900	mV	-
Differential resistance	R_{RDIN}	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 4.						

3.10.2.3 QSGMII AC timing specifications

This section discusses the AC timing specifications for the QSGMII interface.

3.10.2.3.1 QSGMII transmit AC timing specifications

This table provides the QSGMII transmitter AC timing specifications.

Table 36. QSGMII transmit AC timing specifications[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter baud rate	T_{BAUD}	5.000 - 100 ppm	5.000	5.000 + 100 ppm	Gb/s	-
Uncorrelated high probability jitter	T_{UHPJ}	-	-	0.15	UI p-p	-
Total jitter tolerance	J_T	-	-	0.30	UI p-p	-

Notes:

1. For recommended operating conditions, see Table 4.

3.10.2.3.2 QSGMII receiver AC timing Specification

This table provides the QSGMII receiver AC timing specifications.

Table 37. QSGMII receive AC timing specifications[2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	5.000 - 100 ppm	5.000	5.000 + 100 ppm	Gb/s	-
Uncorrelated bounded high probability jitter	R_{DJ}	-	-	0.15	UI p-p	-
Correlated bounded high probability jitter	R_{CBHPJ}	-	-	0.30	UI p-p	1
Bounded high probability jitter	R_{BHPJ}	-	-	0.45	UI p-p	-
Sinusoidal jitter, maximum	$R_{SJ\text{-}max}$	-	-	5.00	UI p-p	-
Sinusoidal jitter, high frequency	$R_{SJ\text{-}hf}$	-	-	0.05	UI p-p	-
Total jitter (does not include sinusoidal jitter)	R_{Tj}	-	-	0.60	UI p-p	-

Notes:

1. The jitter (R_{CBHPJ}) and amplitude have to be correlated, for example, by a PCB trace.
2. For recommended operating conditions, see Table 4.

The sinusoidal jitter may have any amplitude and frequency in the unshaded region of this figure.

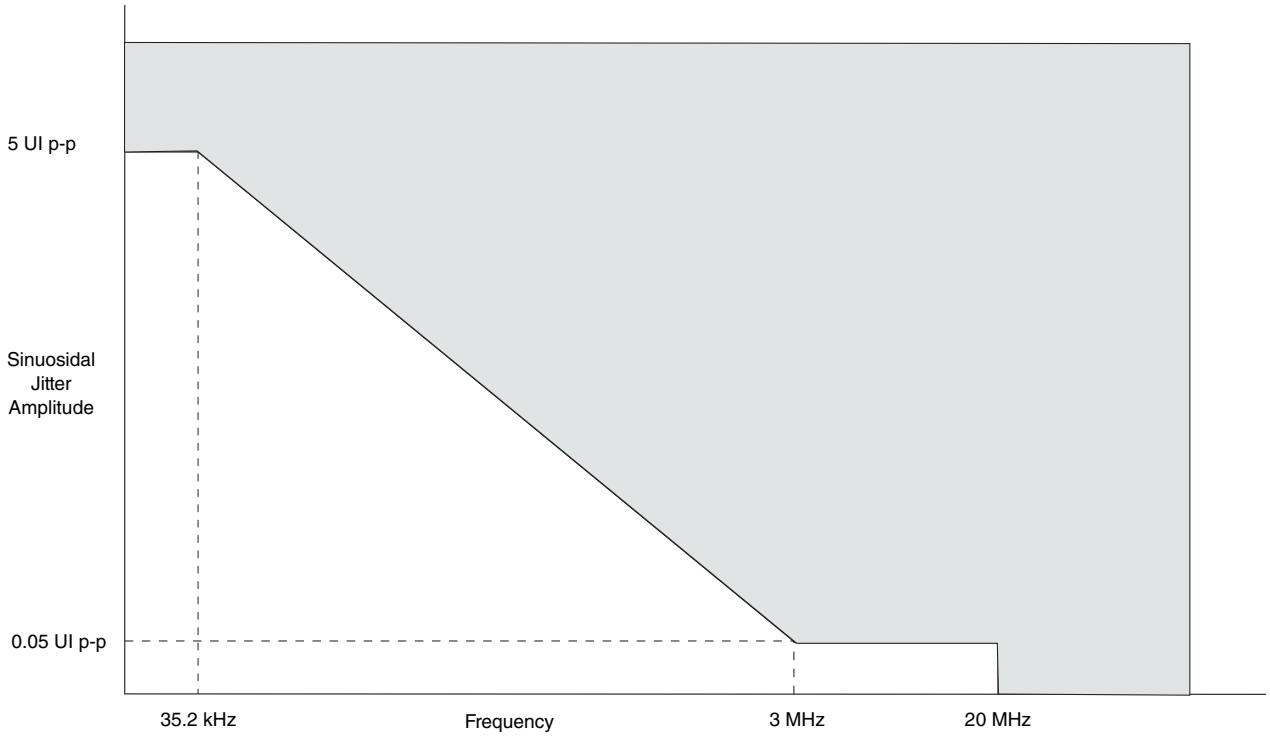


Figure 19. QSGMII single-frequency sinusoidal jitter limits

3.10.3 XFI interface

This section describes the XFI clocking requirements and its DC and AC electrical characteristics.

3.10.3.1 XFI clocking requirements for SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N

Only SerDes 1 (SD1_REF_CLK[1:2]_P and SD1_REF_CLK[1:2]_N) may be used for SerDes XFI configurations based on the RCW configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.10.3.2 XFI DC electrical characteristics

This section describes the DC electrical characteristics for XFI.

3.10.3.2.1 XFI transmitter DC electrical characteristics

This table defines the XFI transmitter DC electrical characteristics.

Table 38. XFI transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX\text{-}DIFF}$	360	-	770	mV	- LNmTECR0[AMP_RED]= 0b000111
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}1.14dB}$	0.6	1.1	1.6	dB	- LNmTECR0[RATIO_PST1Q]=0b00011
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	3	3.5	4	dB	- LNmTECR0[RATIO_PST1Q]=0b01000
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}4.66dB}$	4.1	4.6	5.1	dB	- LNmTECR0[RATIO_PST1Q]=0b01010
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$	5.5	6.0	6.5	dB	- LNmTECR0[RATIO_PST1Q]=0b01100
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}9.5dB}$	9	9.5	10	dB	- LNmTECR0[RATIO_PST1Q]=0b10000
Differential resistance	T_{RD}	80	100	120	Ω	-

Notes:

1. For recommended operating conditions, see Table 4.

3.10.3.2.2 XFI receiver DC electrical characteristics

This table defines the XFI receiver DC electrical characteristics.

Table 39. XFI receiver DC electrical characteristics [2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX\text{-}DIFF}$	110	-	1050	mV	1
Differential resistance	R_{RD}	80	100	120	Ω	-

1. Measured at receiver
2. For recommended operating conditions, see Table 4.

3.10.3.3 XFI AC timing specifications

This section describes the AC timing specifications for XFI.

3.10.3.3.1 XFI transmitter AC timing specifications

This table defines the XFI transmitter AC timing specifications. RefClk jitter is not included.

Table 40. XFI transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100ppm	10.3125	10.3125 + 100ppm	Gb/s
Unit Interval	UI	-	96.96	-	ps
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter	T_J	-	-	0.30	UI p-p

Notes:

1. For recommended operating conditions, see Table 4.

3.10.3.3.2 XFI receiver AC timing specifications

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

Table 41. XFI receiver AC timing specifications[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100ppm	10.3125	10.3125 + 100ppm	Gb/s	-
Unit Interval	UI	-	96.96	-	ps	-
Total non-EQJ jitter	$T_{NON-EQJ}$	-	-	0.45	UI p-p	1
Total jitter tolerance	T_J	-	-	0.65	UI p-p	1, 2

1. The total jitter (T_J) consists of Random Jitter (R_J), Duty Cycle Distortion (DCD), Periodic Jitter (P_J), and Inter symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (R_J), and periodic jitter (P_J). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ = T_J - ISI = R_J + DCD + P_J

2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.

3. For recommended operating conditions, see Table 4.

This figure shows the sinusoidal jitter tolerance of XFI receiver.

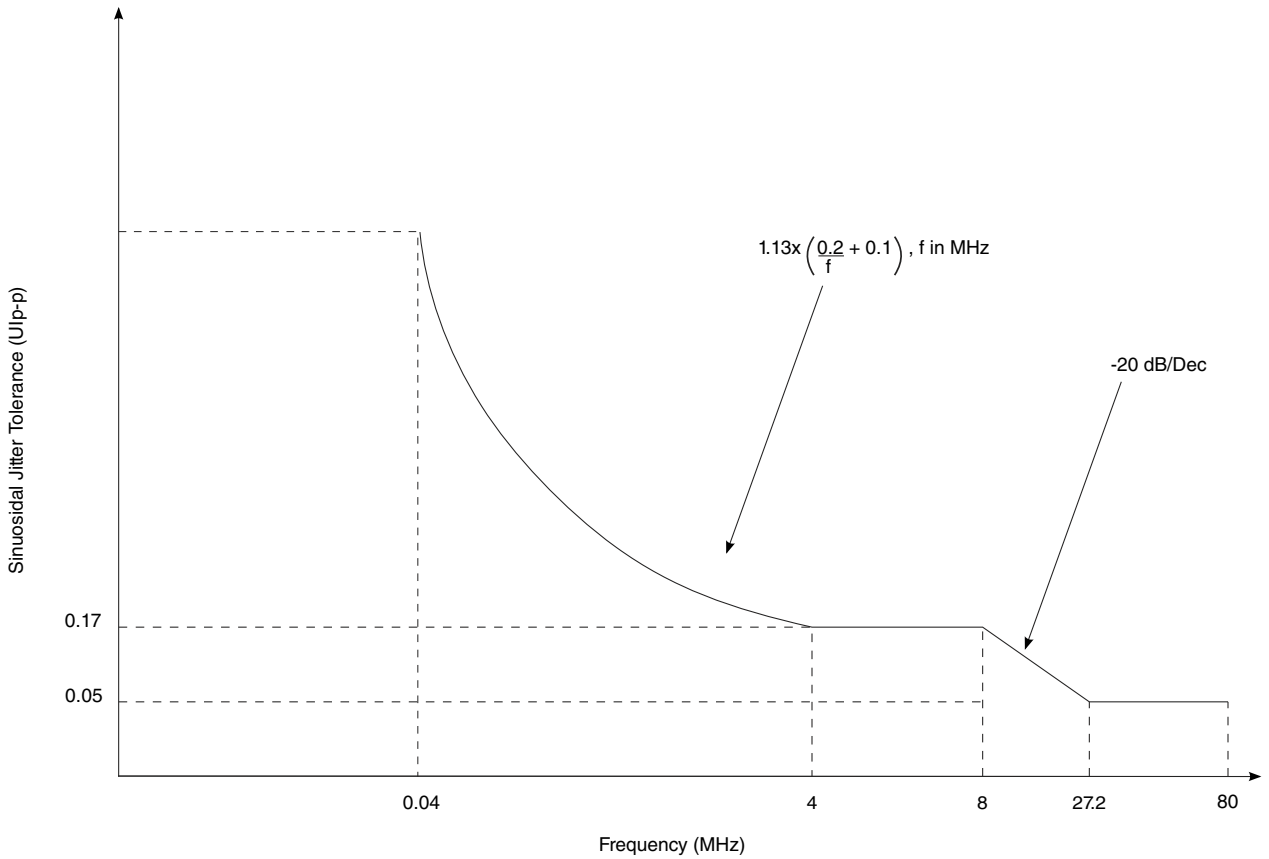


Figure 20. XFI host receiver input sinusoidal jitter tolerance

3.10.4 10GBase-KR interface

This section describes the 10GBase-KR clocking requirements and its DC and AC electrical characteristics.

3.10.4.1 10GBase-KR clocking requirements for SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N

Only SerDes 1 (SD1_REF_CLK1_P and SD1_REF_CLK1_N) may be used for SerDes 10GBase-KR configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.10.4.2 10GBase-KR DC electrical characteristics

This section describes the DC electrical characteristics for 10GBase-KR.

3.10.4.2.1 10GBase-KR transmitter DC electrical characteristics

This table defines the 10GBase-KR transmitter DC electrical characteristics.

Table 42. 10GBaseKR transmitter DC electrical characteristics (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	800	-	1200	mV	- LNmTECR0[AMP_RED]= 0b000000
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	- LNmTECR0[RATIO_PST1Q]=0b00011
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3	3.5	4	dB	- LNmTECR0[RATIO_PST1Q]=0b01000
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	- LNmTECR0[RATIO_PST1Q]=0b01010
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	- LNmTECR0[RATIO_PST1Q]=0b01100
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-9.5dB}$	9	9.5	10	dB	- LNmTECR0[RATIO_PST1Q]=0b10000
Differential resistance	T_{RD}	80	100	120	Ω	-

1. For recommended operating conditions, see Table 4.

3.10.4.2.2 10GBase-KR receiver DC electrical characteristics

This table defines the 10GBase-KR receiver DC electrical characteristics.

Table 43. 10GBase-KR receiver DC electrical characteristics[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX-DIFF}$	-	-	1200	mV	-

Table continues on the next page...

Table 43. 10GBase-KR receiver DC electrical characteristics[1] (continued)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential resistance	R_{RD}	80	-	120	Ω	-
1. For recommended operating conditions, see Table 4.						

3.10.4.3 10GBase-KR AC timing specifications

This section describes the AC timing specifications for 10GBase-KR.

3.10.4.3.1 10GBase-KR transmitter AC timing specifications

This table defines the 10GBase-KR transmitter AC timing specifications. RefClk jitter is not included.

Table 44. 10GBase-KR transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	Gb/s
Uncorrelated high probability jitter/Random jitter	U_{HPJ}/R_J	-	-	0.15	UI p-p
Deterministic jitter	D_J	-	-	0.15	UI p-p
Total jitter	T_J	-	-	0.30	UI p-p
1. For recommended operating conditions, see Table 4.					

3.10.4.3.2 10GBase-KR receiver AC timing specifications

This table defines the 10GBase-KR receiver AC timing specifications. RefClk jitter is not included.

Table 45. 10GBase-KR receiver AC timing specifications[2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	Gb/s	-
Random jitter	R_J	-	-	0.130	UI p-p	-
Sinusodial jitter, maximum	$S_{J\text{-}max}$	-	-	0.115	UI p-p	-
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p	-
Total jitter	T_J	-	-	See Note 1	UI p-p	1
1. The total jitter (TJ) is per Interference tolerance test IEEE Standard 802.3ap-2007 specified in Annex 69A. 2. For recommended operating conditions, see Table 4.						

3.10.5 1000Base-KX interface

This section discusses the electrical characteristics for the 1000Base-KX. Only AC-coupled operation is supported.

3.10.5.1 1000Base-KX DC electrical characteristics

3.10.5.1.1 1000Base-KX Transmitter DC Specifications

This table describes the 1000Base-KX SerDes transmitter DC specification at TP1 per IEEE Std 802.3ap-2007. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TXn_P and SD*n*_TXn_N).

Table 46. 1000Base-KX Transmitter DC Specifications

Parameter	Symbols	Min	Typ	Max	Units	Notes
Output differential voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	-	1600	mV	1
Differential resistance	T_{RD}	80	100	120	ohm	-
Notes: 1. SRDSxLNmTECR0[AMP_RED]=00_0000. 2. For recommended operating conditions, see Table 4.						

3.10.5.1.2 1000Base-KX Receiver DC Specifications

This table provides the 1000Base-KX receiver DC timing specifications.

Table 47. 1000Base-KX Receiver DC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Input differential voltage	$V_{RX\text{-}DIFFp\text{-}p}$	-	-	1600	mV	1
Differential resistance	T_{RDIN}	80	-	120	ohm	-
Notes: 1. For recommended operating conditions, see Table 4.						

3.10.5.2 1000Base-KX AC electrical characteristics

3.10.5.2.1 1000Base-KX Transmitter AC Specifications

This table provides the 1000Base-KX transmitter AC specification.

Table 48. 1000Base-KX Transmitter AC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Baud Rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Uncorrelated High Probability Jitter/ Random Jitter	$T_{UHPJ}T_{RJ}$	-	-	0.15	UI p-p	-
Deterministic Jitter	T_{DJ}	-	-	0.10	UI p-p	-
Total Jitter	T_{TJ}	-	-	0.25	UI p-p	1

Notes:

1. Total jitter is specified at a BER of 10^{-12}.
2. For recommended operating conditions, see Table 4.

3.10.5.2.2 1000Base-KX Receiver AC Specifications

This table provides the 1000Base-KX receiver AC specification with parameters guided by IEEE Std 802.3ap-2007.

Table 49. 1000Base-KX Receiver AC Specifications

Parameter	Symbols	Min	Typical	Max	Units	Notes
Receiver Baud Rate	T_{BAUD}	1.25-100ppm	1.25	1.25+100ppm	Gb/s	-
Random Jitter	R_{RJ}	-	-	0.15	UI p-p	1
Sinusoidal Jitter, maximum	R_{SJ-max}	-	-	0.10	UI p-p	2
Total Jitter	R_{TJ}	-	-	See Note 3	UI p-p	2

Notes:

1. Random jitter is specified at a BER of 10^{-12}.
2. The receiver interference tolerance level of this parameter shall be measured as described in Annex 69A of the IEEE Std 802.3ap-2007.
3. Per IEEE 802.3ap-clause 70.
4. The AC specifications do not include Refclk jitter.
5. For recommended operating conditions, see Table 4.

3.10.6 RGMII electrical specifications

This section describes the electrical characteristics for the RGMII interface.

3.10.6.1 RGMII DC electrical characteristics

This table provides the DC electrical characteristics for the RGMII interface at LV_{DD} = 2.5 V.

Table 50. RGMII DC electrical characteristics (LV_{DD} = 2.5 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x LV_{DD}	V	1
Input current (LV_{IN}=0 V or LV_{IN}= LV_{DD})	I_{IH}	—	±50	μA	2
Output high voltage (LV_{DD} = min,I_{OH} = -1.0 mA)	V_{OH}	2.00	—	V	
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for the RGMII interface at LV_{DD} = 1.8 V.

Table 51. RGMII DC electrical characteristics (LV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x LV_{DD}	V	1
Input current (LV_{IN} = 0 V or LV_{IN}= LV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	

Notes:

1. The min V_{IL} and max V_{IH} values are based on the min and max LV_{IN} values found in Table 4.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.10.6.2 RGMII AC timing specifications

This table provides the RGMII AC timing specifications.

Table 52. RGMII AC timing specifications (LV_{DD} = 2.5 /1.8 V)[8]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	-500	0	500	ps	7

Table continues on the next page...

Table 52. RGMII AC timing specifications (LV_{DD} = 2.5 /1.8 V)[8] (continued)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.6	ns	2, 9
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—
Rise time (20%-80%)	t_{RGTR}	—	—	0.75	ns	5, 6
Fall time (20%-80%)	t_{RGTF}	—	—	0.75	ns	5, 6

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).

2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.

3. For 10 Mbps and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.

4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

5. Applies to inputs and outputs.

6. The system/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

7. The frequency of EC*n*_RX_CLK (input) should not exceed the frequency of EC*n*_GTX_CLK (output) by more than 300 ppm.

8. For recommended operating conditions, see Table 4.

9. For 10 Mbps and 100 Mbps, the max value is unspecified.

This figure shows the RGMII AC timing and multiplexing diagrams.

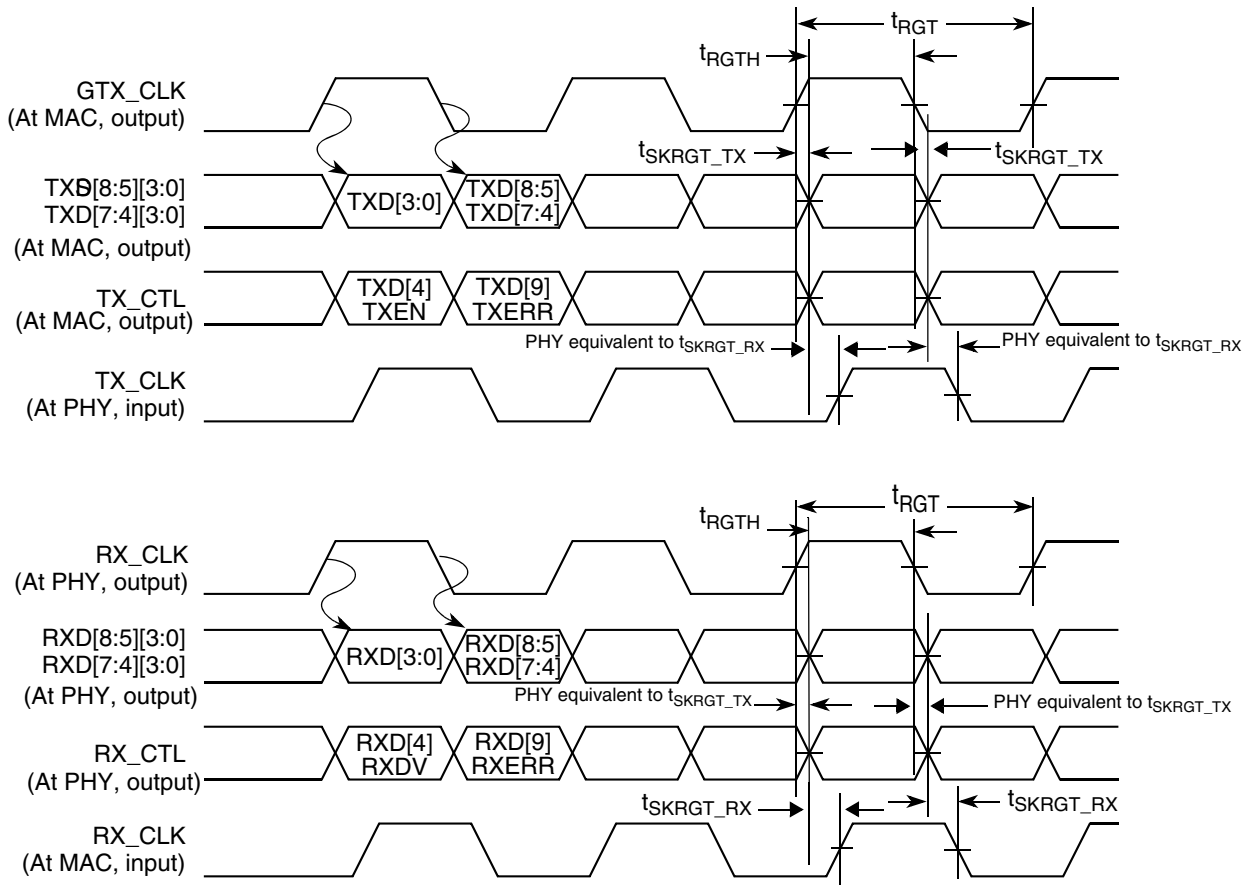


Figure 21. RGMII AC timing and multiplexing diagrams

Warning

NXP guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

3.10.7 Ethernet management interface (EMI)

This section describes the electrical characteristics for the Ethernet Management Interface (EMI) interface.

Both the interfaces (EMI1 and EMI2) interface timing is compatible with IEEE Std 802.3™ clause 22.

3.10.7.1 Ethernet management interface 1 (EMI1)

This section describes the electrical characteristics for the EMI1 interface.

The EMI1 interface timing is compatible with IEEE Std 802.3™ clause 22.

3.10.7.1.1 EMI1 DC electrical characteristics

This section describes the DC electrical characteristics for EMI1_MDIO and EMI1_MDC. The pins are available on LV_{DD}. See Table 4 for operating voltages.

This table provides the EMI1 DC electrical characteristics when LV_{DD} = 2.5 V.

Table 53. EMI1 DC electrical characteristics (LV_{DD} = 2.5 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x LV_{DD}	V	1
Input current (LV_{IN} = 0 or LV_{IN} = LV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the EMI1 DC electrical characteristics when LV_{DD} = 1.8 V.

Table 54. EMI1 DC electrical characteristics (LV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x LV_{DD}	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	

Notes:

1. The min V_{IL} and max V_{IH} values are based on the min and max LV_{IN} respective values found in Table 4.
2. The symbol LV_{IN} represents the LV_{IN} symbols referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.10.7.1.2 EMI1 AC timing specifications

This table provides the EMI1 AC timing specifications.

Table 55. EMI1 AC timing specifications[5]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	—	2.5	MHz	2

Table continues on the next page...

Table 55. EMI1 AC timing specifications[5] (continued)

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	(Y+5) x t_{enet_clk} - 4	—	(Y+5) x t_{enet_clk} + 4	ns	3
MDIO to MDC setup time	t_{MDDVKH}	8	—	—	ns	
MDIO to MDC hold time	t_{MDDXKH}	2.6	—	—	ns	6

Notes:

1. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.

2. This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG[MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC.

3. Ethernet clock period (t_{enet_clk}) is equal to Frame Manager Clock period (t_{FMAN_clk})

4. Y is the value programmed to adjust hold time by MDIO_CFG[MDIO_HOLD].

5. For recommended operating conditions, see Table 4.

6. See Ethernet A-010717 erratum.

This figure shows the Ethernet management interface 1 timing diagram

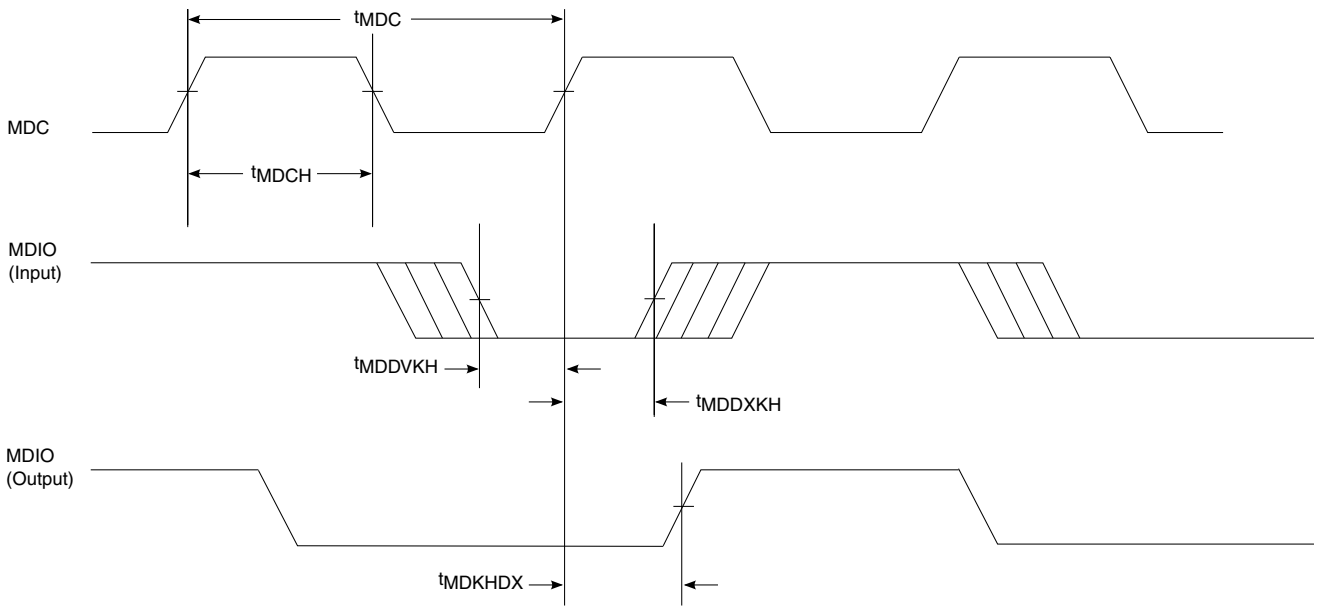


Figure 22. Ethernet management interface 1 timing diagram

3.10.7.2 Ethernet management interface 2 (EMI2)

This section describes the electrical characteristics for the EMI2 interface.

The EMI2 interface timing is compatible with IEEE Std 802.3™ clause 45.

3.10.7.2.1 EMI2 DC electrical characteristics

This section describes the DC electrical characteristics for EMI2_MDIO and EMI2_MDC. The pins are available on TV_{DD}. See Table 4 for operating voltages.

This table provides the EMI2 DC electrical characteristics when TV_{DD} = 2.5 V.

Table 56. EMI2 DC electrical characteristics (TV_{DD} = 2.5 V)[4]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x TV_{DD}	V	1
Input current (TV_{IN} = 0 or TV_{IN} = TV_{DD})	I_{IN}	—	±50	μA	2, 3
Output high voltage (TV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (TV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the TV_{IN} symbols referenced in Recommended operating conditions.
3. The symbol TV_{DD}, in this case, represents the TV_{DD} symbols referenced in Recommended operating conditions.
4. For recommended operating conditions, see Table 4.

This table provides the EMI2 DC electrical characteristics when TV_{DD} = 1.8 V.

Table 57. EMI2 DC electrical characteristics (TV_{DD} = 1.8 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x TV_{DD}	V	1
Input current (TV_{IN} = 0 V or TV_{IN} = TV_{DD})	I_{IN}	—	±50	μA	2, 3
Output high voltage (TV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	3
Output low voltage (TV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	3

Notes:

1. The min V_{IL} and max V_{IH} values are based on the min and max TV_{IN} respective values found in Table 4.
2. The symbol TV_{IN} represents the TV_{IN} symbols referenced in Recommended operating conditions.
3. The symbol TV_{DD}, in this case, represents the TV_{DD} symbols referenced in Recommended operating conditions.
4. For recommended operating conditions, see Table 4.

This table provides the EMI2 DC electrical characteristics when TV_{DD} = 1.2 V.

Table 58. EMI2 DC electrical characteristics (TV_{DD} = 1.2 V) [1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	—	V	—
Input low voltage	V_{IL}	—	0.2 x TV_{DD}	V	—
Output low current (V_{OL} = 0.2 V)	I_{OL}	4		mA	—
Output high voltage (TV_{DD} = min, I_{OH} = -100uA)	V_{OH}	1.0	—	V	—
Output low voltage (TV_{DD} = min, I_{OL} = 100 uA)	V_{OL}	—	0.2	V	—
Input Capacitance	C_{IN}	—	10	pF	—

Notes:

1. For recommended operating conditions, see Table 4.

3.10.7.2.2 EMI2 AC timing specifications

This table provides the EMI2 AC timing specifications.

Table 59. EMI2 AC timing specifications[6]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	(Y+5) x t_{enet_clk} - 25	—	(Y+5) x t_{enet_clk}) + 25	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	36	—	—	ns	5
MDIO to MDC hold time (TV_{DD}=1.2V)	t_{MDDXKH}	2.6	—	—	ns	7
MDIO to MDC hold time (TV_{DD}=1.8V / 2.5V)	t_{MDDXKH}	1.1	—	—	ns	7

Notes:

1. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.

2. This parameter is dependent on the Ethernet clock frequency. The MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock EC_MDC.

3. Ethernet clock period (t_{enet_clk}) is equal to Frame Manager Clock period (t_{FMAN_clk})

4. Y is the value programmed to adjust hold time by MDIO_CFG[MDIO_HOLD].

5. The setup time t_{MDDVKH} is measured at following load conditions
   - For MDC = 65 pf and for MDIO =75 pf @1.2 V open drain configuration

6. For recommended operating conditions, see Table 4.

7. See Ethernet A-010717 erratum.

This figure shows the Ethernet management interface 2 timing diagram

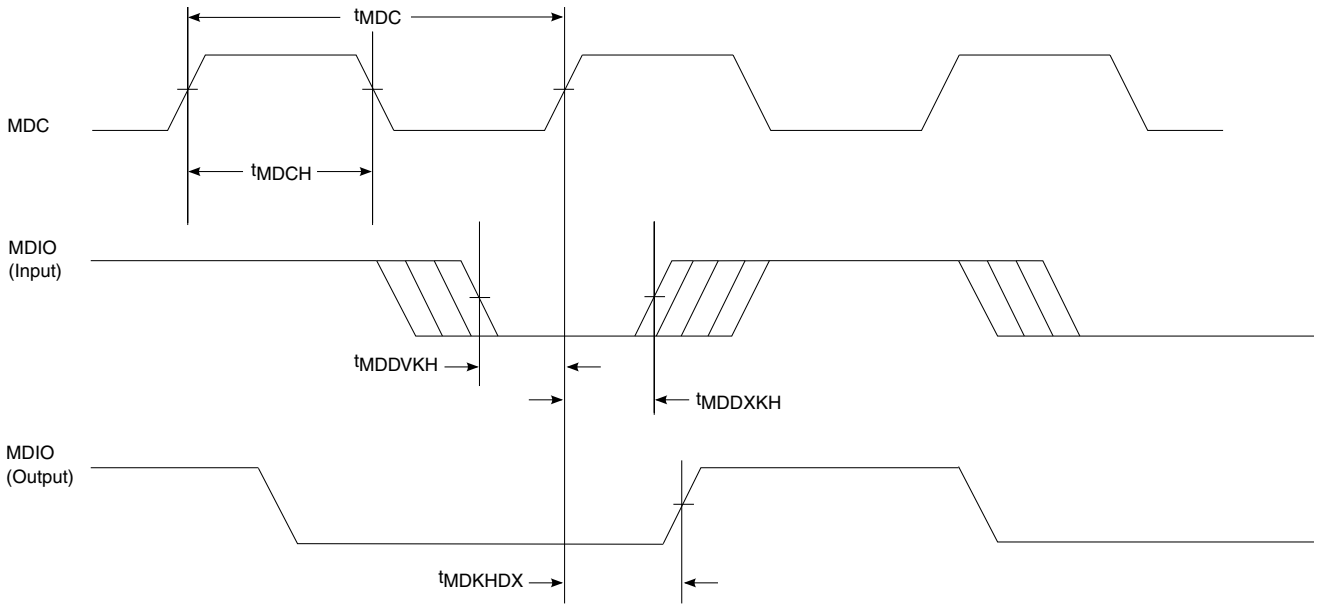


Figure 23. Ethernet management interface 2 timing diagram

3.10.8 IEEE 1588 electrical specifications

3.10.8.1 IEEE 1588 DC electrical characteristics

This table provides the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 60. IEEE 1588 DC electrical characteristics(LV_{DD} = 2.5 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x LV_{DD}	V	1
Input current (LV_{IN}= 0 V or LV_{IN}= LV_{DD})	I_{IH}	—	±50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 1.8 V supply.

Table 61. IEEE 1588 DC electrical characteristics(LV_{DD} = 1.8 V)[3]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x LV_{DD}	V	1
Input current (LV_{IN}= 0 V or LV_{IN}= LV_{DD})	I_{IH}	—	±50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.40	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.10.8.2 IEEE 1588 AC timing specifications

This table provides the IEEE 1588 AC timing specifications.

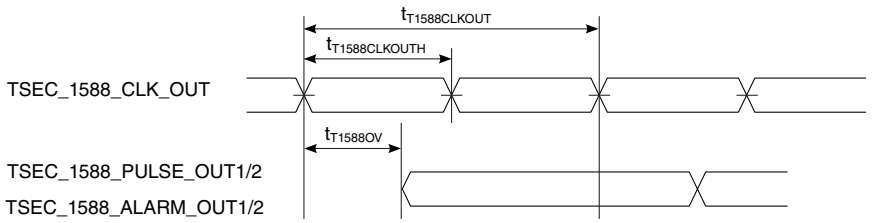
Table 62. IEEE 1588 AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK_IN clock period	$t_{T1588CLK}$	5.0	—	T_{RX_CLK} x 7	ns	1, 3
TSEC_1588_CLK_IN duty cycle	$t_{T1588CLKH}$/ $t_{T1588CLK}$	40	50	60	%	2
TSEC_1588_CLK_IN peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time TSEC_1588_CLK_IN (20%-80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time TSEC_1588_CLK_IN (80%-20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	5.0	—	—	ns	4
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$/ $t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT1/2, TSEC_1588_ALARM_OUT1/2	$t_{T1588OV}$	0	—	4.0	ns	—
TSEC_1588_TRIG_IN1/2 pulse width	$t_{T1588TRIGH}$	2 x $t_{T1588CLK_MAX}$	—	—	ns	3

Notes:

1. T_{RX_CLK} is the maximum clock period of the ethernet receiving clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
2. This needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns, respectively.
4. There are three input clock sources for 1588: TSEC_1588_CLK_IN, RTC, and MAC clock / 2. When using TSEC_1588_CLK_IN, the minimum clock period is 2 x $t_{T1588CLK}$.
5. For recommended operating conditions, see Table 4.

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 24. IEEE 1588 output AC timing

This figure shows the data and command input AC timing diagram.

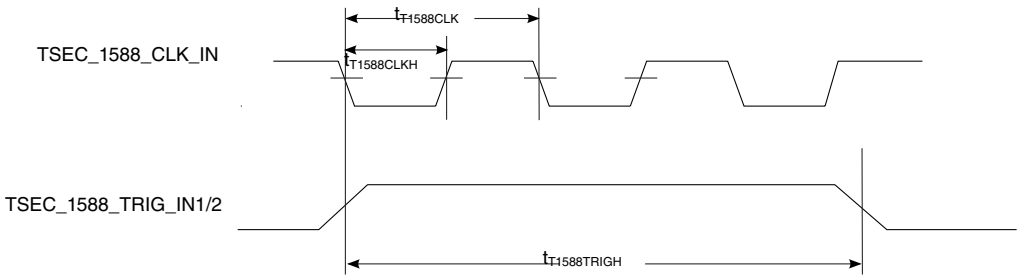


Figure 25. IEEE 1588 input AC timing

3.11 USB 3.0 interface

This section describes the DC and AC electrical specifications for the USB 3.0 interface.

3.11.1 USB 3.0 PHY transceiver supply DC voltage

This table provides the DC electrical characteristics for the USB 3.0 interface when operating at USB_HV_{DD} = 3.3 V.

Table 63. USB 3.0 PHY transceiver supply DC voltage (USB_HV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (USB_HV_{IN} = 0 V or USB_HV_{IN}= USB_HV_{DD})	I_{IN}	—	±50	μA	2

Table continues on the next page...

Table 63. USB 3.0 PHY transceiver supply DC voltage (USB_HV_{DD} = 3.3 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (USB_HV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.8	—	V	—
Output low voltage (USB_HV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max USB_HV_{IN} values found in Table 4.
2. The symbol USB_HV_{IN}, in this case, represents the USB_HV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.11.2 USB 3.0 DC electrical characteristics

This table provides the USB 3.0 transmitter DC electrical characteristics at package pins.

Table 64. USB 3.0 transmitter DC electrical characteristics[1]

Characteristic	Symbol	Min	Nom	Max	Unit
Differential output voltage	$V_{tx\text{-}diff\text{-}pp}$	800	1000	1200	$mV_{p\text{-}p}$
Low-power differential output voltage	$V_{tx\text{-}diff\text{-}pp\text{-}low}$	400	—	1200	$mV_{p\text{-}p}$
Tx de-emphasis	$V_{tx\text{-}de\text{-}ratio}$	3	—	4	dB
Differential impedance	Z_{diffTX}	72	100	120	Ohm
Tx common mode impedance	$R_{TX\text{-}DC}$	18	—	30	Ohm
Absolute DC common mode voltage between U1 and U0	$T_{TX\text{-}CM\text{-}DC\text{-}ACTIVEIDLE\text{-}DELTA}$	—	—	200	mV
DC electrical idle differential output voltage	$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC}$	0	—	10	mV

Note:

1. For recommended operating conditions, see Table 4.

This table provides the USB 3.0 receiver DC electrical characteristics at the Rx package pins.

Table 65. USB 3.0 receiver DC electrical characteristics

Characteristic	Symbol	Min	Nom	Max	Unit	Notes
Differential Rx input impedance	$R_{RX\text{-}DIFF\text{-}DC}$	72	100	120	Ohm	—
Receiver DC common mode impedance	$R_{RX\text{-}DC}$	18	—	30	Ohm	—
DC input CM input impedance for V > 0 during reset or power down	ZRX-HIGH-IMP-DC	25 K	—	—	Ohm	—

Table continues on the next page...

Table 65. USB 3.0 receiver DC electrical characteristics (continued)

Characteristic	Symbol	Min	Nom	Max	Unit	Notes
LFPS detect threshold	VRX-IDLE-DET-DC-DIFF$_{pp}$	100	—	300	mV	1
Note: 1. Below the minimum is noise. Must wake up above the maximum.						

3.11.3 USB 3.0 AC timing specifications

This table provides the USB 3.0 transmitter AC timing specifications at package pins.

Table 66. USB 3.0 transmitter AC timing specifications[1]

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Speed	—	—	5.0	—	Gb/s	—
Transmitter eye	t_{TX-Eye}	0.625	—	—	UI	—
Unit interval	UI	199.94	—	200.06	ps	2
AC coupling capacitor	AC coupling capacitor	75	—	200	nF	—
Note: 1. For recommended operating conditions, see Table 4. 2. UI does not account for SSC-caused variations.						

This table provides the USB 3.0 receiver AC timing specifications at Rx package pins.

Table 67. USB 3.0 receiver AC timing specifications[1]

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Unit interval	UI	199.94	—	200.06	ps	2
Notes: 1. For recommended operating conditions, see Table 4. 2. UI does not account for SSC-caused variations.						

3.11.4 USB 3.0 reference clock requirements

There are two options for the reference clock of USB PHY: SYSCLK or DIFF_SYSCLK/DIFF_SYSCLK_B. For more information, see USB 3.0 reference clock requirements.

3.11.5 USB 3.0 LFPS specifications

This table provides the key LFPS electrical specifications at the transmitter.

Table 68. LFPS electrical specifications at the transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Period	tPeriod	20	—	100	ns	—
Peak-to-peak differential amplitude	$V_{TX\text{-}DIFF\text{-}PP\text{-}LFPS}$	800	—	1200	mV	—
Rise/fall time	$t_{RiseFall20\text{-}80}$	—	—	4	ns	1
Duty cycle	Duty cycle	40	—	60	%	1
Note: 1. Measured at compliance TP1. See Figure 26 for details.						

This figure shows the transmit normative setup with reference channel as per USB 3.0 specifications.

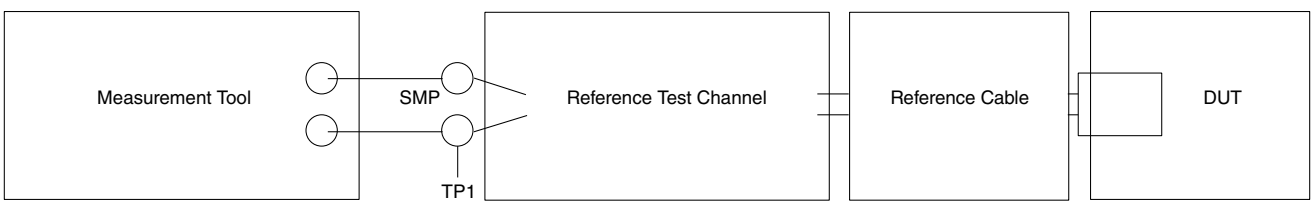


Figure 26. Transmit normative setup

3.12 Integrated Flash Controller

This section describes the DC and AC electrical specifications for the integrated flash controller.

3.12.1 Integrated Flash Controller DC electrical characteristics

This table provides the DC electrical characteristics for the integrated flash controller.

Table 69. Integrated Flash Controller DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	1
Input current	I_{IN}	-	±50	μA	2

Table continues on the next page...

Table 69. Integrated Flash Controller DC electrical characteristics (1.8 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Note
(V_{IN} = 0 V or V_{IN} = OV_{DD})					
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.6	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.32	V	-

NOTE:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.12.2 Integrated Flash Controller AC timing specifications

This section describes the AC timing specifications for the integrated flash controller.

3.12.2.1 Test condition

The figure below provides the AC test load for the integrated flash controller.

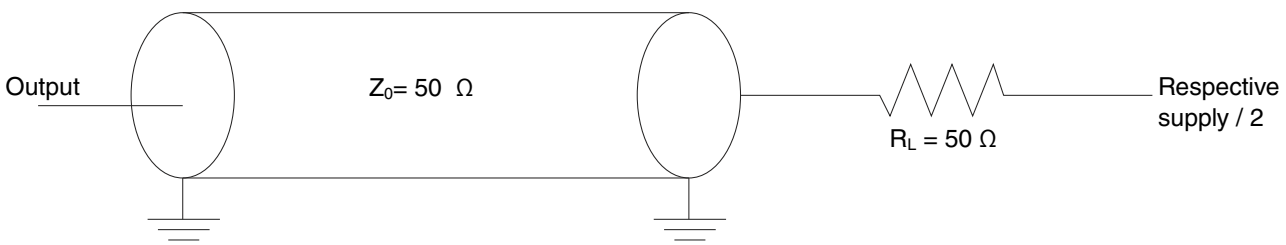


Figure 27. Integrated Flash Controller AC test load

3.12.2.2 IFC AC timing specifications (GPCM/GASIC)

This table describes the input AC timing specifications for the IFC-GPCM and IFC-GASIC interface.

Table 70. Integrated flash controller input timing specifications for GPCM and GASIC mode (OV_{DD} = 1.8 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH1}$	4	-	ns	-

Table continues on the next page...

Table 70. Integrated flash controller input timing specifications for GPCM and GASIC mode (OV_{DD} = 1.8 V)[1] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input hold	$t_{IBIXKH1}$	1	-	ns	-

NOTE:

1. For recommended operating conditions, see Table 4.

This figure shows the input AC timing diagram for the IFC-GPCM, IFC-GASIC interface.

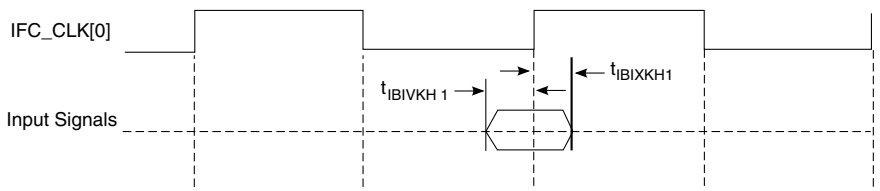


Figure 28. IFC-GPCM, IFC-GASIC input AC timing specifictions

This table describes the output AC timing specifications for the IFC-GPCM and IFC-GASIC interfaces.

Table 71. Integrated flash controller IFC-GPCM and IFC-GASIC interface output timing specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
IFC_CLK cycle time	t_{IBK}	10	-	ns	-
IFC_CLK duty cycle	t_{IBKH}/ t_{IBK}	45	55	%	-
Output delay	$t_{IBKLOV1}$	-	1.5	ns	-
Output hold	t_{IBKLOX}	-	-2	ns	1
IFC_CLK[0] to IFC_CLK[m] skew	$t_{IBKSKEW}$	0	±75	ps	-

NOTE:

1. The output hold is negative. This means that output transition happens earlier than the falling edge of IFC_CLK.
2. For recommended operating conditions, see Table 4.

This figure shows the output AC timing diagram for the IFC-GPCM and IFC-GASIC interface.

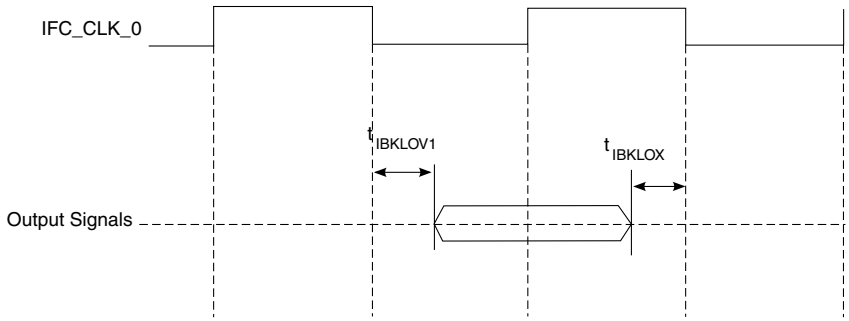


Figure 29. IFC-GPCM, IFC-GASIC signals

3.12.2.3 IFC AC timing specifications (NOR)

This table describes the input timing specifications for the IFC-NOR interface.

Table 72. Integrated flash controller input timing specifications for NOR mode (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH2}$	(2 x t_{IP_CLK}) + 2	-	ns	1
Input hold	$t_{IBIXKH2}$	(1 x t_{IP_CLK}) + 1	-	ns	1

Notes:

1. t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.
2. For recommended operating conditions, see Table 4.
3. The NOR flash state machine will de-assert OE_B once the flash controller samples data. Hold time tIBIXKH2 given in the datasheet is not a requirement for customer but rather an information used internally for test purpose.

The figure below shows the AC input timing diagram for input signals for the IFC-NOR interface. Here TRAD is a programmable delay parameter. See the IFC section of the chip reference manual for more information.

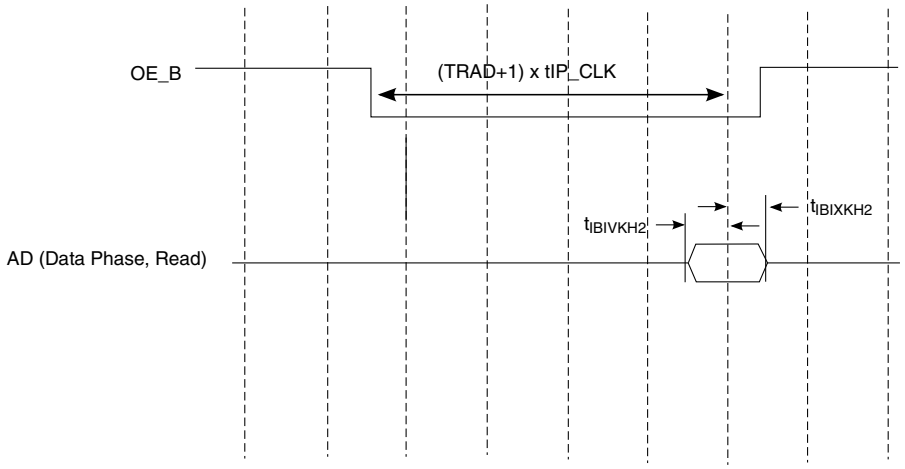


Figure 30. IFC-NOR interface input AC timings

This table describes the output AC timing specifications of IFC-NOR interface.

Table 73. Integrated flash controller IFC-NOR interface output timing specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV2}$	-	±1.5	ns	1

NOTE:

1. This effectively means that a signal change may appear anywhere within $\pm t_{IBKLOV2}$ (max) duration, from the point where it's expected to change.

2. For recommended operating conditions, see Table 4.

The figure below shows the AC timing diagram for IFC-NOR interface output signals. The timing specs have been illustrated here by taking timings between two signals, CS_B and OE_B as an example. In a read operation, OE_B is supposed to change the TACO (a programmable delay; see the IFC section of the chip reference manual for more information) time after CS_B. Because of the skew between the signals, OE_B may change anywhere within the window of time defined by tIBKLOV2. This concept applies to other IFC-NOR interface output signals as well. The diagram is an example that shows the skew between any two chronological toggling signals as per the protocol. The list of IFC-NOR output signals is as follows: NRALE, NRAVD_B, NRWE_B, NROE_B, CS_B, AD (Address phase).

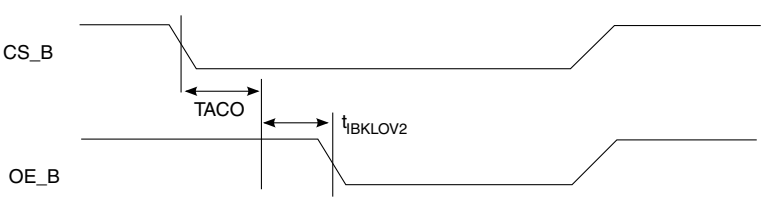


Figure 31. IFC-NOR interface output AC timings

3.12.2.4 IFC AC timing specifications (NAND)

This table describes the input timing specifications of the IFC-NAND interface.

Table 74. Integrated flash controller input timing specifications for NAND mode (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input setup	$t_{IBIVKH3}$	(2 x t_{IP_CLK}) + 2	-	ns	1
Input hold	$t_{IBIXKH3}$	1	-	ns	1
IFC_RB_B pulse width	t_{IBCH}	2	-	t_{IP_CLK}	1

NOTE:

1. t_{IP_CLK} is the period of ip clock on which IFC is running.
2. For recommended operating conditions, see Table 4.

The figure below shows the AC input timing diagram for input signals of IFC-NAND interface. Here TRAD is a programmable delay parameter. See the IFC section of the chip reference manual for more information.

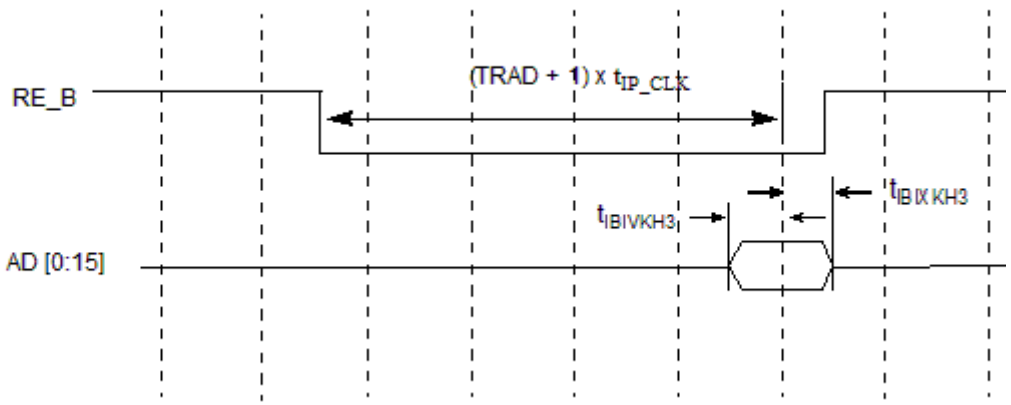


Figure 32. IFC-NAND interface input AC timings

NOTE

t_{IP_CLK} is the period of ip clock (not the IFC_CLK) on which IFC is running.

This table describes the output AC timing specifications for the IFC-NAND interface.

Table 75. Integrated flash controller IFC-NAND interface output timing specifications (OV_{DD} = 1.8 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Output delay	$t_{IBKLOV3}$	-	±1.5	ns	1

Table continues on the next page...

Table 75. Integrated flash controller IFC-NAND interface output timing specifications (OV_{DD} = 1.8 V)[2] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
NOTE: 1. This effectively means that a signal change may appear anywhere within $t_{IBKLOV3}$ (min) to $t_{IBKLOV3}$ (max) duration, from the point where it's expected to change. 2. For recommended operating conditions, see Table 4.					

The figure below shows the AC timing diagram for output signals of IFC-NAND interface.The timing specs are shown here by taking the timings between two signals, CS_B and CLE as an example. CLE is supposed to change TCCST (a programmable delay; see the IFC section of the chip reference manual for more information) time after CS_B. Because of the skew between the signals, CLE may change anywhere within window of time defined by $t_{IBKLOV3}$. This concept applies to other output signals of the IFC-NAND interface as well. The diagram is an example to show the skew between any two chronological toggling signals as per the protocol. The list of output signals is as follows: NDWE_B, NDRE_B, NDALE, WP_B, NDCLE, CS_B, and AD.

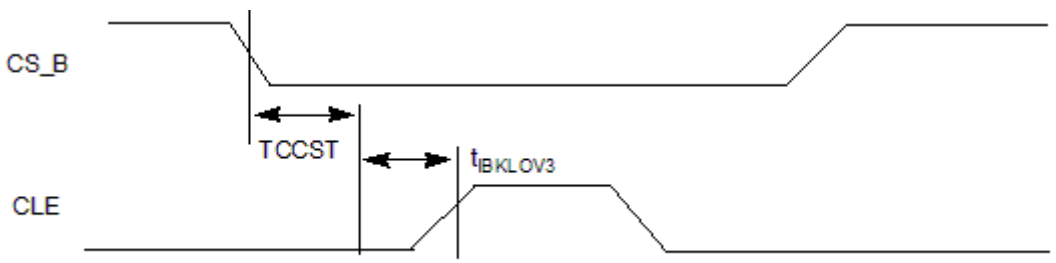


Figure 33. IFC-NAND interface output AC timings

3.12.2.5 IFC-NAND SDR AC timing specifications

This table describes the AC timing specifications for the IFC-NAND SDR interface. These specifications are compliant to the SDR mode of the ONFI specification revision 3.0.

Table 76. Integrated flash controller IFC-NAND SDR interface AC timing specifications (OVDD = 1.8 V)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Address cycle to data loading time	t_{ADL}	O	TADLE - 1500(ps)	TADLE + 1500(ps)	t_{IP_CLK}	Figure 34
ALE hold time	t_{ALH}	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}	Figure 35
ALE setup time	t_{ALS}	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}	Figure 35

Table continues on the next page...

Table 76. Integrated flash controller IFC-NAND SDR interface AC timing specifications (OVDD = 1.8 V) (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
ALE to RE_n delay	t_{AR}	O	TWHRE - 1500(ps)	TWHRE + 1500(ps)	t_{IP_CLK}	Figure 36
CE_n hold time	t_{CH}	O	5 + 1500(ps)	-	ns	Figure 35
CE_n high to input hi-Z	t_{CHZ}	I	TRHZ - 1500(ps)	TRHZ + 1500(ps)	t_{IP_CLK}	Figure 37
CLE hold time	t_{CLH}	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}	Figure 35
CLE to RE_n delay	t_{CLR}	O	TWHRE - 1500(ps)	TWHRE - 1500(ps)	t_{IP_CLK}	Figure 38
CLE setup time	t_{CLS}	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}	Figure 35
CE_n high to input hold	t_{COH}	I	150 - 1500(ps)	-	ns	Figure 37
CE_n setup time	t_{CS}	O	TCS - 1500(ps)	TCS + 1500(ps)	t_{IP_CLK}	Figure 35
Data hold time	t_{DH}	O	TWCHT - 1500(ps)	TWCHT + 1500(ps)	t_{IP_CLK}	Figure 35
Data setup time	t_{DS}	O	TWP - 1500(ps)	TWP + 1500(ps)	t_{IP_CLK}	Figure 35
Busy time for Set Features and Get Features	t_{FEAT}	O	-	FTOCNT	t_{IP_CLK}	Figure 39
Output hi-Z to RE_n low	t_{IR}	O	TWHRE - 1500(ps)	TWHRE + 1500(ps)	t_{IP_CLK}	Figure 40
Interface and Timing Mode Change time	t_{ITC}	O	-	FTOCNT	t_{IP_CLK}	Figure 39
RE_n cycle time	t_{RC}	O	TRP + TREH - 1500(ps)	TRP + TREH + 1500(ps)	t_{IP_CLK}	Figure 37
RE_n access time	t_{REA}	I	-	(TRAD - 1) + 2(ns)	t_{IP_CLK}	Figure 37
RE_n high hold time	t_{REH}	I	TREH	TREH	t_{IP_CLK}	Figure 37
RE_n high to input hold	t_{RHOH}	I	0	-	ns	Figure 37
RE_n high to WE_n low	t_{RHW}	O	100 + 1500(ps)	-	ns	Figure 41
RE_n high to input hi-Z	t_{RHZ}	I	TRHZ - 1500(ps)	TRHZ + 1500(ps)	t_{IP_CLK}	Figure 37
RE_n low to input data hold	t_{RLOH}	I	0	-	ns	Figure 42
RE_n pulse width	t_{RP}	O	TRP	TRP	t_{IP_CLK}	Figure 37
Ready to data input cycle (data only)	t_{RR}	O	TRR - 1500(ps)	TRR + 1500(ps)	t_{IP_CLK}	Figure 37
Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n.	t_{RST} (raw NAND)	O	-	FTOCNT	t_{IP_CLK}	Figure 43
Device reset time, measured from the falling edge of R/B_n to the rising edge of R/B_n.	t_{RST2} (EZ NAND)	O	-	FTOCNT	t_{IP_CLK}	Figure 43

Table continues on the next page...

Table 76. Integrated flash controller IFC-NAND SDR interface AC timing specifications (OVDD = 1.8 V) (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
(WE_n high or CLK rising edge) to SR[6] low	t_{WB}	O	TWBE + TWH - 1500(ps)	TWBE + TWH + 1500(ps)	t_{IP_CLK}	Figure 35
WE_n cycle time	t_{WC}	O	TWP + TWH	TWP + TWH	t_{IP_CLK}	Figure 44
WE_n high hold time	t_{WH}	O	TWH	TWH	t_{IP_CLK}	Figure 44
Command, address, or data input cycle to data output cycle	t_{WHR}	O	TWHRE + TWH - 1500(ps)	TWHRE + TWH + 1500(ps)	t_{IP_CLK}	Figure 45
WE_n pulse width	t_{WP}	O	TWP	TWP	t_{IP_CLK}	Figure 35
WP_n transition to command cycle	t_{WW}	O	TWW - 1500(ps)	TWW + 1500(ps)	t_{IP_CLK}	Figure 46
Data Input hold	$t_{IBIXKH4}$	I	1	-	t_{IP_CLK}	Figure 47

NOTE:

1. t_{IP_CLK} is the clock period of the IP clock (on which the IFC IP is running). Note that the IFC IP clock does not come out of the device.

This figure shows the t_{ADL} timing.

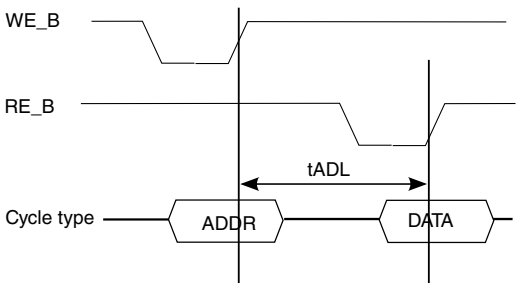


Figure 34. t_{ADL} timing

This figure shows the command cycle.

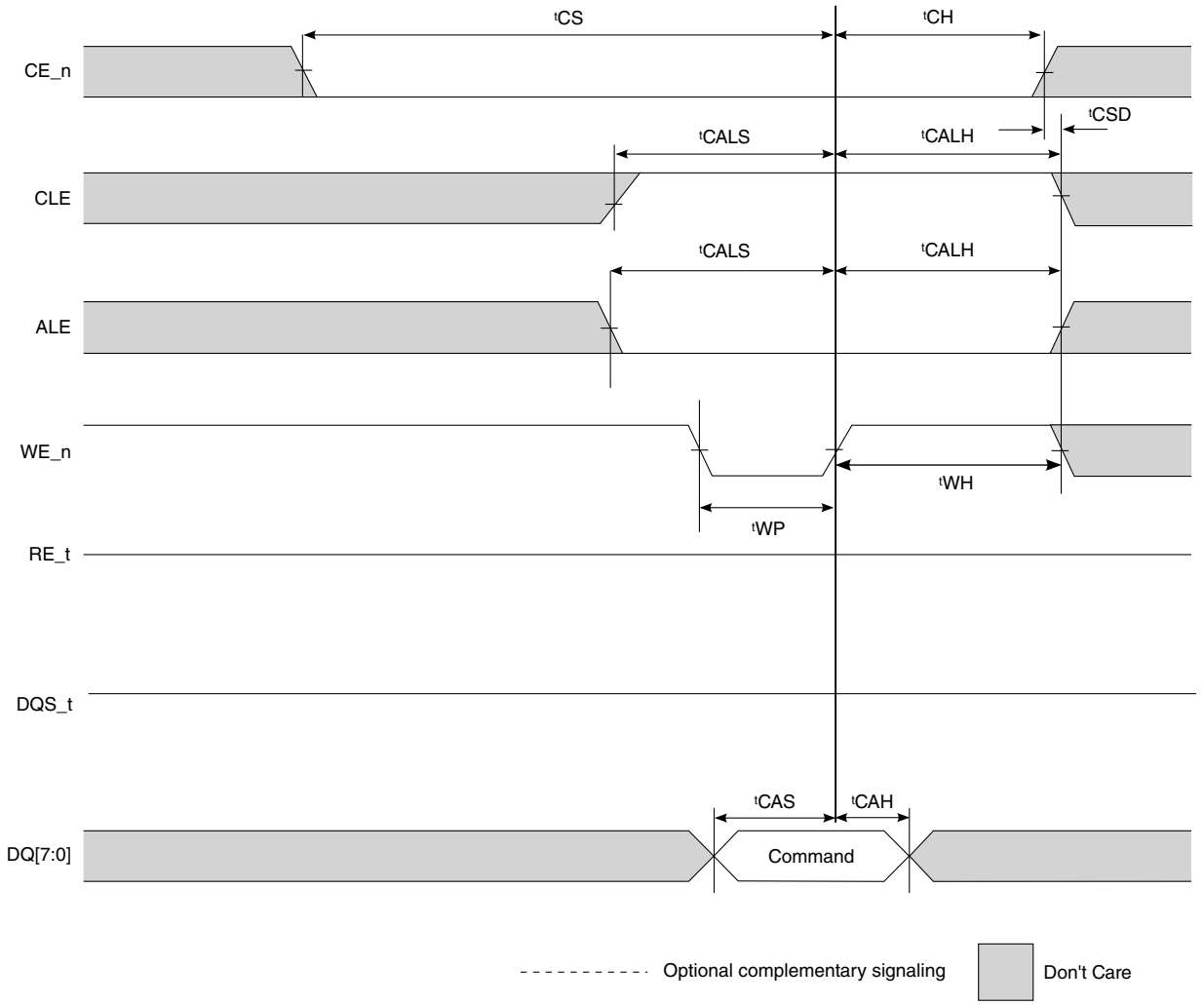


Figure 35. Command cycle

This figure shows the t_{AR} timings.

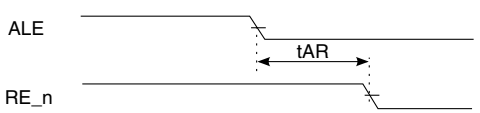


Figure 36. t_{AR} timings

This figure shows the data input cycle timings.

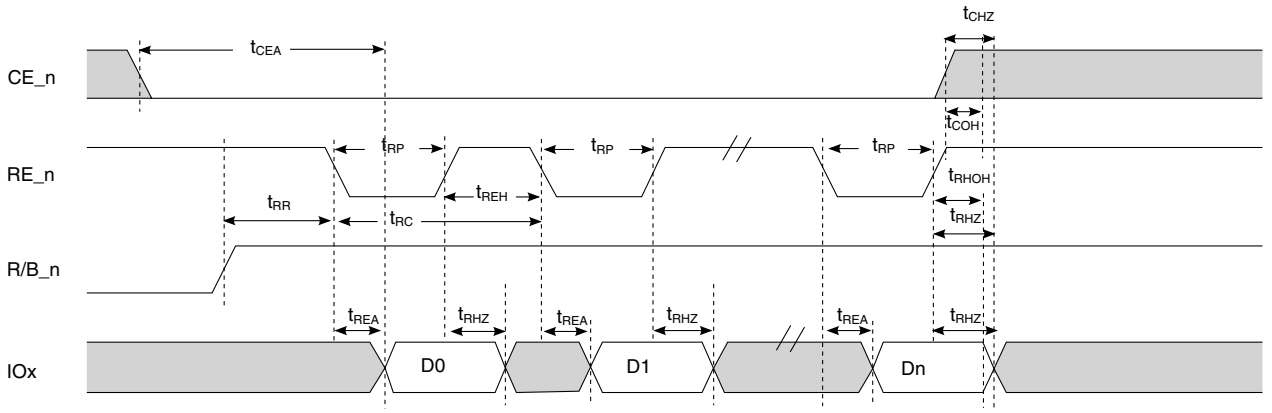


Figure 37. Data input cycle timings

This figure shows the t_{CLR} timings.

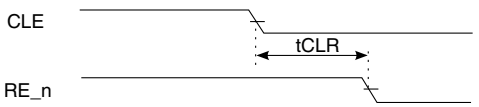


Figure 38. t_{CLR} timings

This figure shows the t_{WB}, t_{FEAT}, t_{ITC}, and t_{RR} timings.

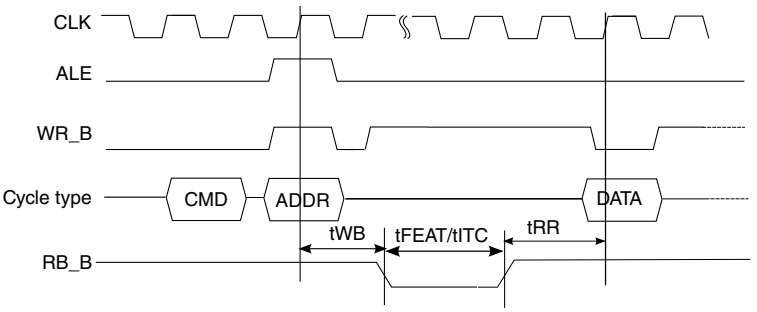


Figure 39. t_{WB}, t_{FEAT}, t_{ITC}, and t_{RR} timings

This figure shows the read status timings.

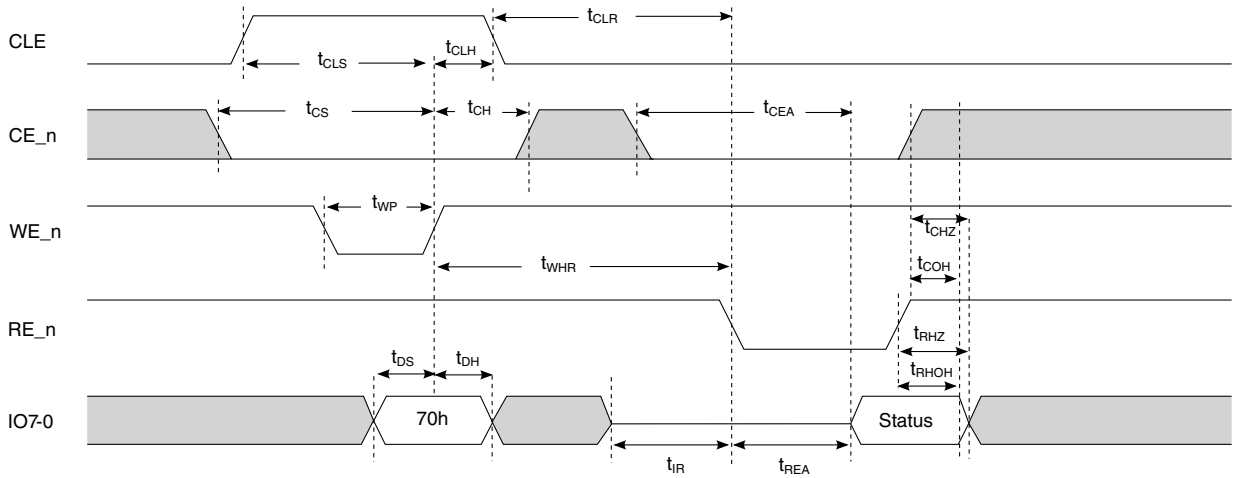


Figure 40. Read status timings

This figure shows the t_{RHW} timings.

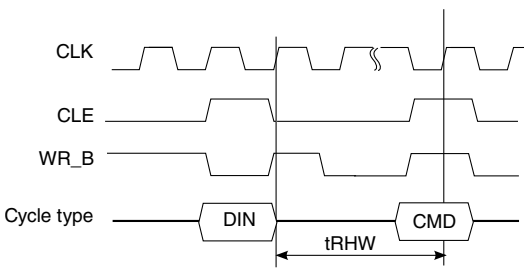


Figure 41. t_{RHW} timings

This figure shows the EDO mode data input cycle timings.

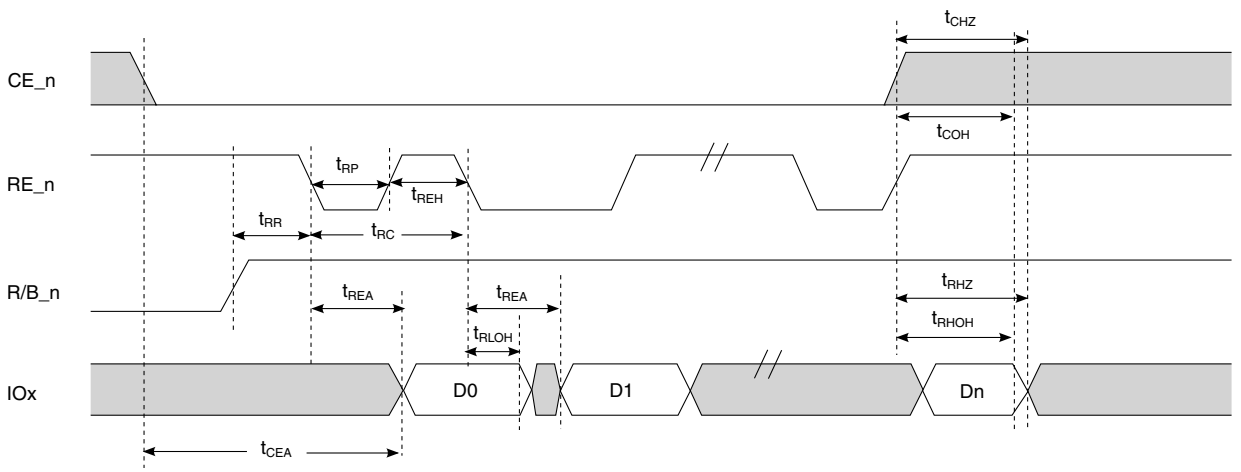


Figure 42. EDO mode data input cycle timings

This figure shows the t_{WB} and t_{RST} timings.

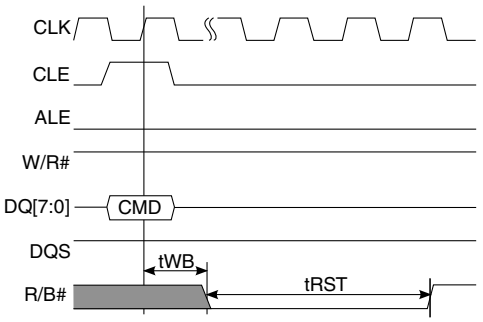


Figure 43. t_{WB} and t_{RST} timings

This figure shows the address latch timings.

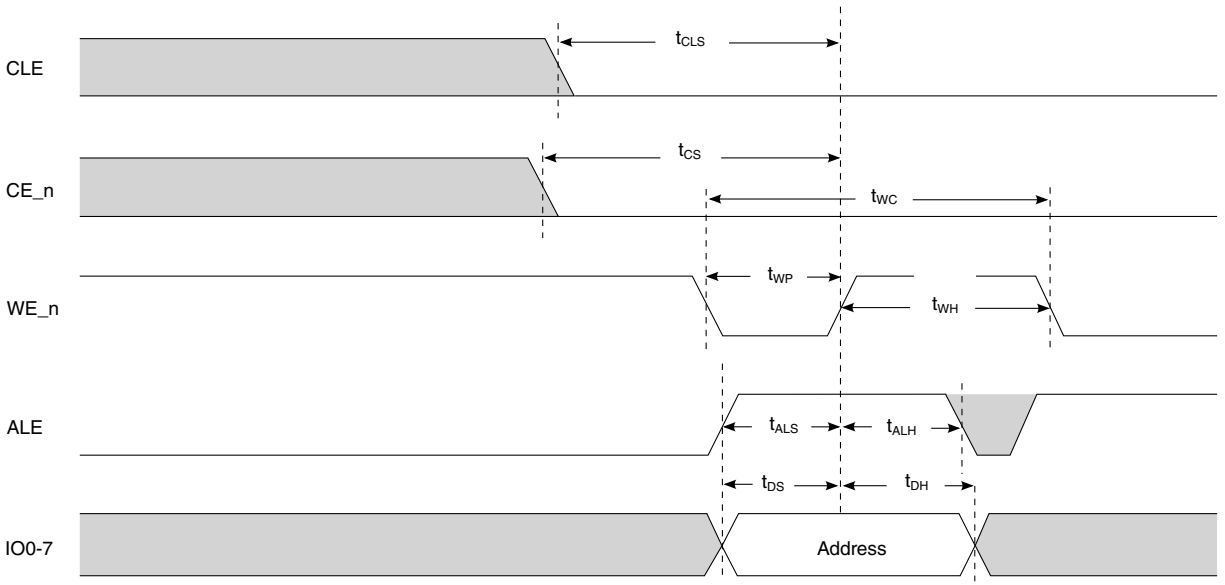


Figure 44. Address latch timings

This figure shows the t_{WHR} timings.

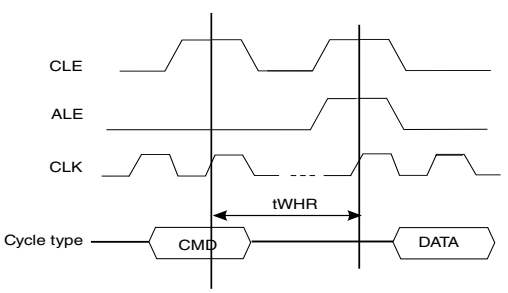


Figure 45. t_{WHR} timings

This figure shows the t_{WW} timings.

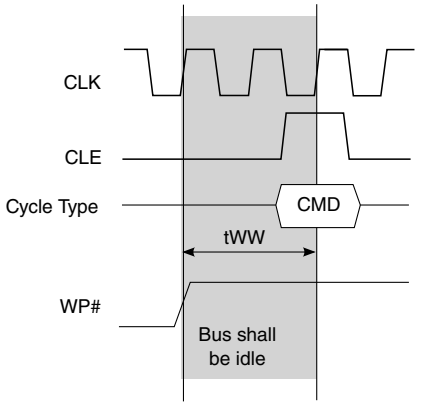


Figure 46. t_{WW} timings

This figure shows the $t_{IBIXKH4}$ timings.

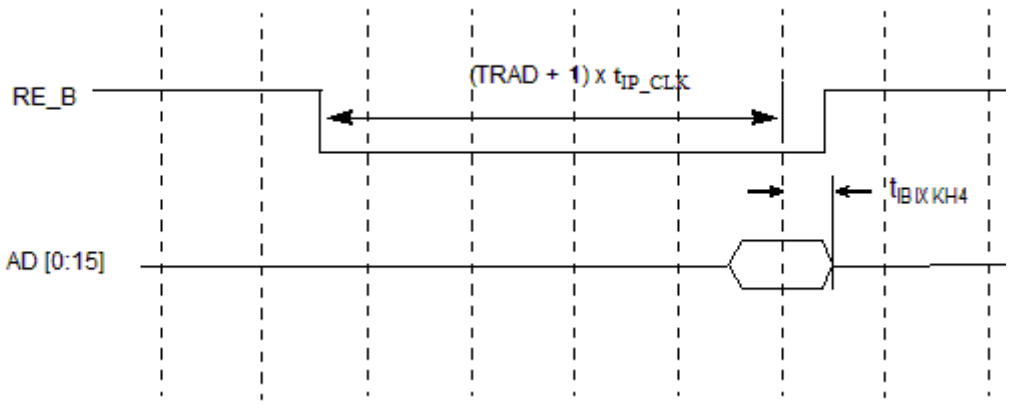


Figure 47. $t_{IBIXKH4}$ timings

3.12.2.6 IFC-NAND NVDDR AC timing specification

The table below describes the AC timing specifications for the IFC-NAND NVDDR interface. These specifications are compliant to NVDDR mode of ONFI specification revision 3.0.

Table 77. Integrated flash controller IFC-NAND NVDDR interface AC timing specifications (OVDD = 1.8 V)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Access window of DQ[7:0] from CLK	t_{AC}	I	3 - 150 (ps)	20 + 150 (ps)	ns	Figure 51
Address cycle to data loading time	t_{ADL}	I	TADL	-	t_{IP_CLK}	Figure 52

Table continues on the next page...

Table 77. Integrated flash controller IFC-NAND NVDDR interface AC timing specifications (OVDD = 1.8 V) (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
Command, Address, Data delay (command to command, address to address, command to address, address to command, command/ address to start of data) Fast	tCADf	O	TCAD - 150 (ps)	TCAD + 150 (ps)	t_{IP_CLK}	Figure 48
Command, Address, Data delay (command to command, address to address, command to address, address to command, command/ address to start of data) slow	tCADs	O	TCAD - 150 (ps)	TCAD + 150 (ps)	t_{IP_CLK}	Figure 48
Command/address DQ hold time	t_{CAH}	O	2 + 150 (ps)	-	ns	Figure 48
CLE and ALE hold time	t_{CALH}	O	2 + 150 (ps)	-	ns	Figure 48
CLE and ALE setup time	t_{CALS}	O	2 + 150 (ps)	-	ns	Figure 48
Command/address DQ setup time	t_{CAS}	O	2 + 150 (ps)	-	ns	Figure 48
CE# hold time	t_{CH}	O	2 + 150 (ps)	-	ns	Figure 48
Average clock cycle time, also known as tCK	t_{CK}(avg) or t_{CK}	O	10	-	ns	Figure 48
Absolute clock period, measured from rising edge to the next consecutive rising edge	t_{CK}(abs)	O	tCK(avg) + tJIT(per) min	tCK(avg) + tJIT(per) max	ns	Figure 48
Clock cycle high	t_{CKH}(abs)	O	0.45	0.55	tCK	Figure 48
Clock cycle low	t_{CKL}(abs)	O	0.45	0.55	tCK	Figure 48
Data input end to W/R# high B16	t_{CKWR}	O	TCKWR - 150 (ps)	TCKWR + 150 (ps)	t_{IP_CLK}	Figure 51
CE# setup time	t_{CS}	O	TCS - 150 (ps)	TCS + 150 (ps)	t_{IP_CLK}	Figure 50
Data DQ hold time	t_{DH}	O	1050	-	ps	Figure 50
Access window of DQS from CLK	t_{DQSCK}	I	-	20 + 150 (ps)	ns	Figure 51
W/R# low to DQS/DQ driven by device	t_{DQSD}	I	-150 (ps)	18 + 150 (ps)	ns	Figure 51
DQS output high pulse width	t_{DQSH}	O	0.45	0.55	tCK	Figure 50
W/R# high to DQS/DQ tri-state by device	t_{DQSHZ}	O	RHZ - 150 (ps)	RHZ + 150 (ps)	t_{IP_CLK}	Figure 48
DQS output low pulse width	t_{DQSL}	O	0.45	0.55	tCK	Figure 50

Table continues on the next page...

Table 77. Integrated flash controller IFC-NAND NVDDR interface AC timing specifications (OVDD = 1.8 V) (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
DQS-DQ skew, DQS to last DQ valid, per access	t_{DQSQ}	I	-	1000	ps	Figure 51
Data output to first DQS latching transition	t_{DQSS}	O	0.75 + 150 (ps)	1.25 - 150 (ps)	tCK	Figure 50
Data DQ setup time	t_{DS}	O	1050	-	ps	Figure 50
DQS falling edge to CLK rising - hold time	t_{DSH}	O	0.2 + 150 (ps)	-	tCK	Figure 50
DQS falling edge to CLK rising - setup time	t_{DSS}	O	0.2 + 150 (ps)	-	tCK	Figure 50
Input data valid window	t_{DVW}	I	tDVW = tQH - tDQSQ	-	ns	Figure 51
Busy time for Set Features and Get Features	t_{FEAT}	I	-	FTOCNT	t_{IP_CLK}	Figure 53
Half-clock period	t_{HP}	O	tHP = min(tCKL, tCKH)	-	ns	Figure 51
Interface and Timing Mode Change time	t_{ITC}	I	-	FTOCNT	t_{IP_CLK}	Figure 53
The deviation of a given tCK(abs) from tCK(avg)	t_{JIT}(per)	O	-0.5	0.5	ns	NA
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t_{QH}	I	tQH = tHP - tQHS	-	t_{IP_CLK}	Figure 51
Data input cycle to command, address, or data output cycle	t_{RHW}	O	TRHW	-	t_{IP_CLK}	Figure 54
Ready to data input cycle (data only)	t_{RR}	I	TRR	-	t_{IP_CLK}	Figure 53
Device reset time, measured from the falling edge of R/B# to the rising edge of R/B#.	t_{RST} (raw NAND)	O	FTOCNT	FTOCNT	t_{IP_CLK}	Figure 55
Device reset time, measured from the falling edge of R/B# to the rising edge of R/B#.	t_{RST2} (EZ NAND)	O	FTOCNT	FTOCNT	t_{IP_CLK}	Figure 55
CLK rising edge to SR[6] low	t_{WB}	O	TWB - 150 (ps)	TWB + 150 (ps)	t_{IP_CLK}	Figure 55
Command, address or data output cycle to data input cycle	t_{WHR}	O	TWHR	-	t_{IP_CLK}	Figure 56
DQS write preamble	t_{WPRE}	O	1.5	-	tCK	Figure 50
DQS write postamble	t_{WPST}	O	1.5	-	tCK	Figure 50
W/R# low to data input cycle	t_{WRCK}	I	TWRCK - 150 (ps)	TWRCK + 150 (ps)	t_{IP_CLK}	Figure 51

Table continues on the next page...

Table 77. Integrated flash controller IFC-NAND NVDDR interface AC timing specifications (OVDD = 1.8 V) (continued)

Parameter	Symbol	I/O	Min	Max	Unit	Notes
WP# transition to command cycle	t_{WW}	O	TWW - 150 (ps)	TWW + 150 (ps)	t_{IP_CLK}	Figure 57

NOTE:

1. t_{IP_CLK} is the clock period of IP clock (on which IFC IP is running). Note that the IFC IP clock does not come out of device.

The following diagrams show the AC timing for the IFC-NAND NVDDR interface.

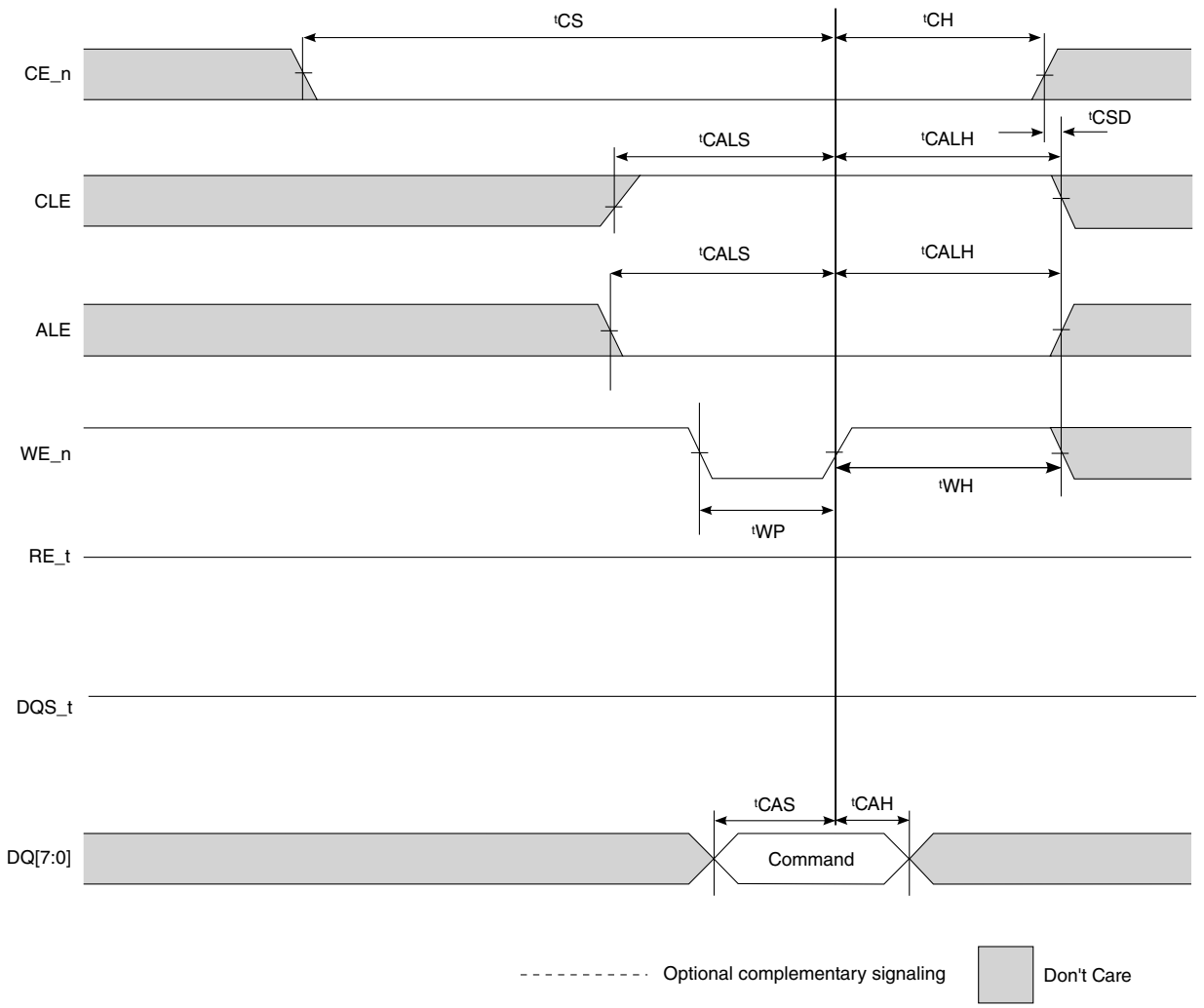


Figure 48. Command cycle

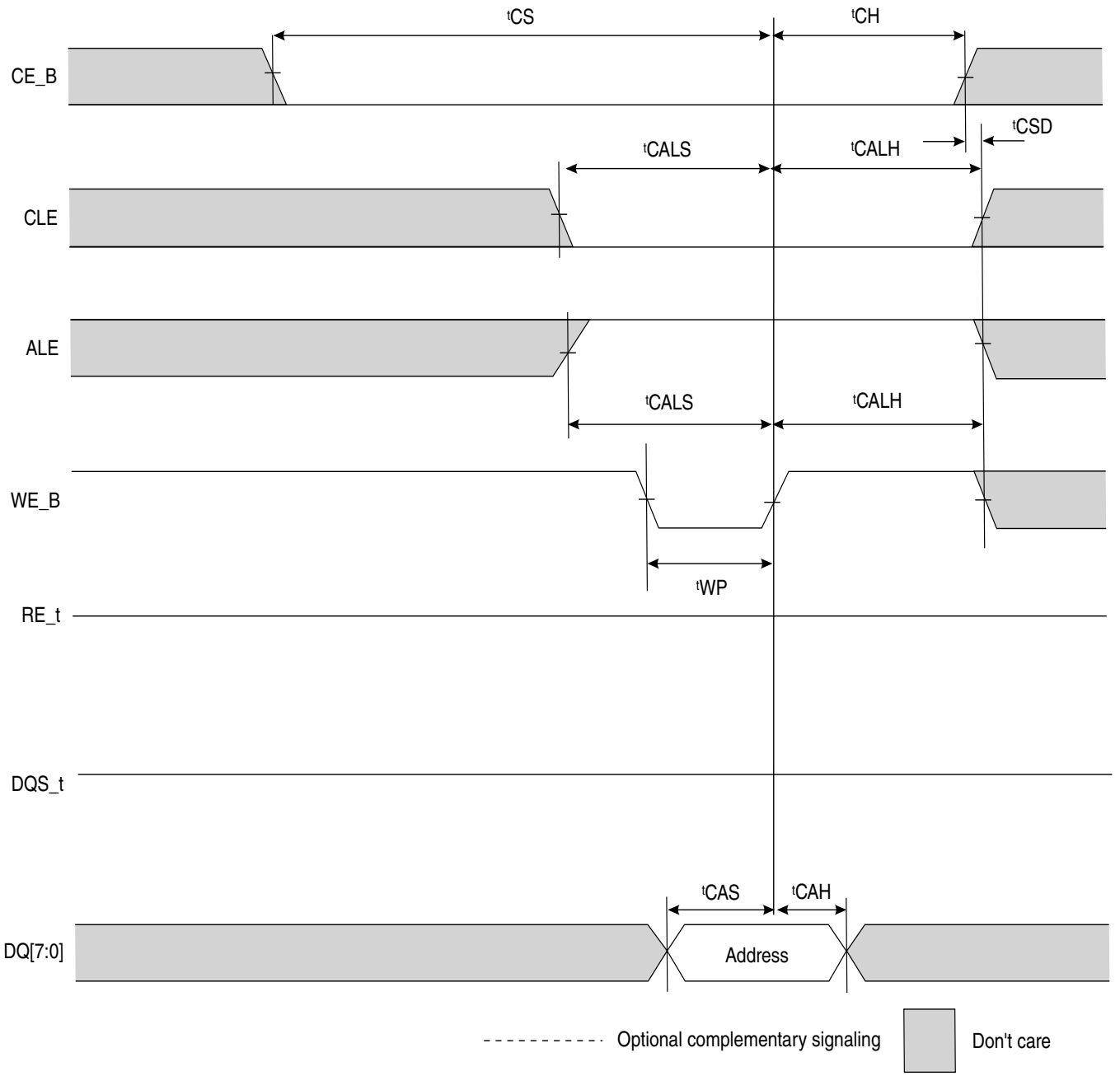


Figure 49. Address cycle

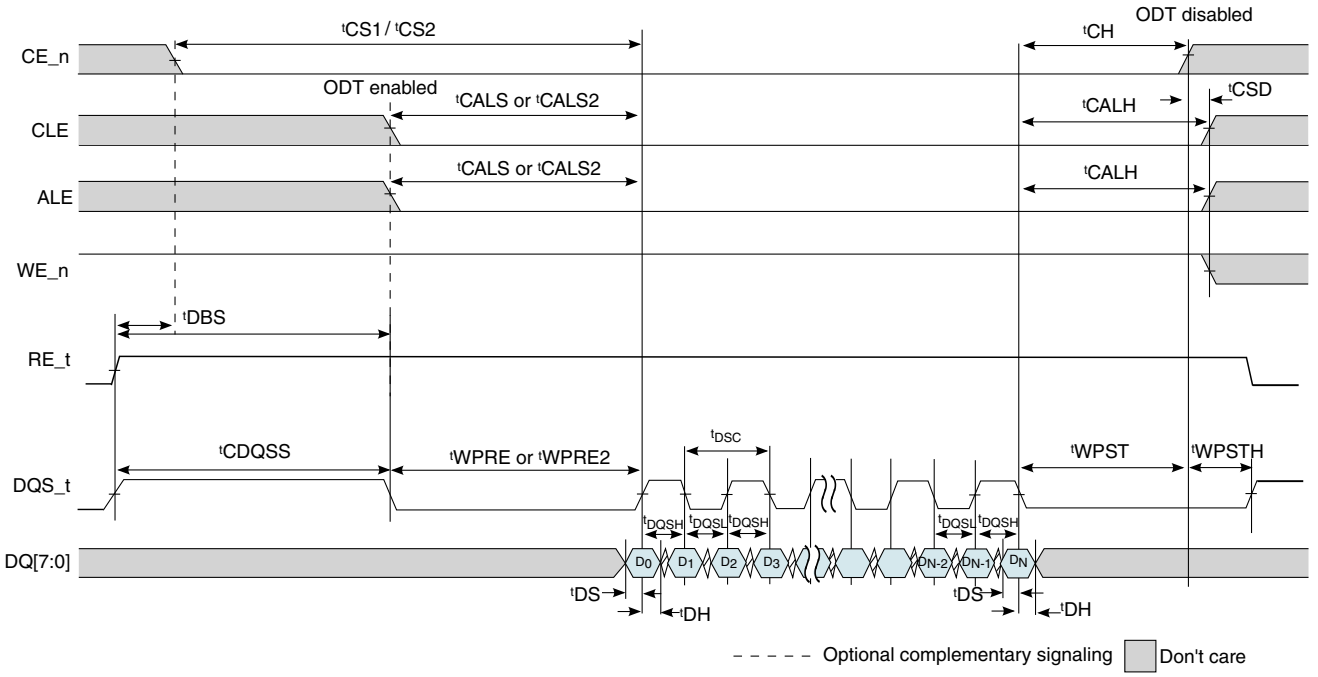


Figure 50. Write cycle

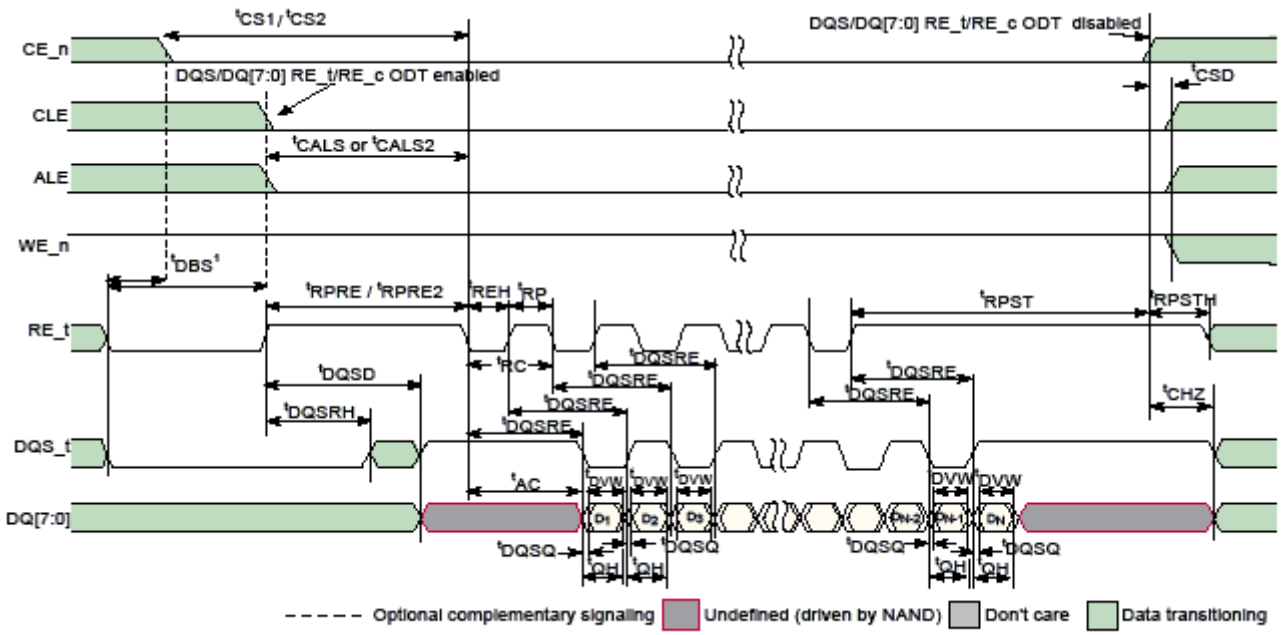


Figure 51. Read cycle

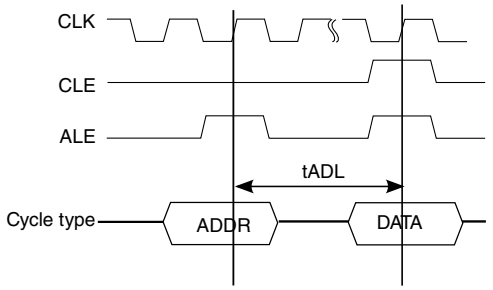


Figure 52. t_{ADL} timings

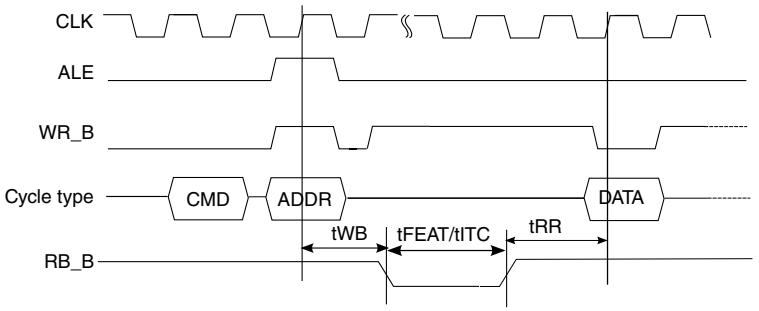


Figure 53. t_{WB}, t_{FEAT}, t_{ITC}, t_{RR} timings

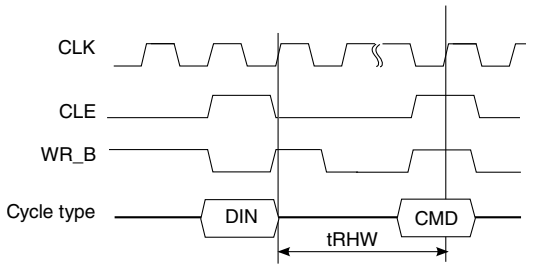


Figure 54. t_{RHW} timings

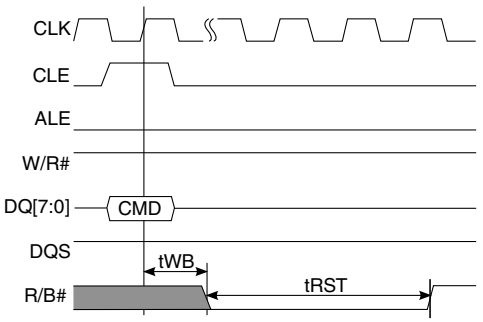


Figure 55. t_{WB} and t_{RST} timings

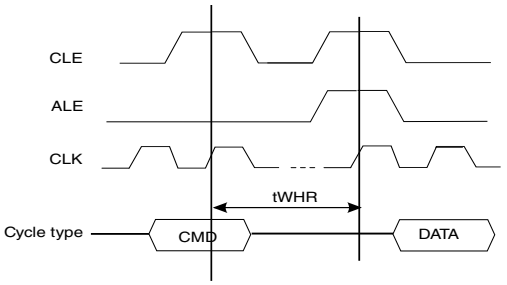


Figure 56. tWHR timings

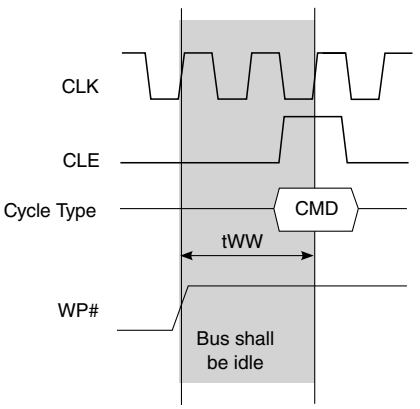


Figure 57. tWW timings

3.13 LPUART interface

This section describes the DC and AC electrical specifications for the LPUART interface.

3.13.1 LPUART DC electrical characteristics

This table provides the DC electrical characteristics for the LPUART interface when operating at DV_{DD}/EV_{DD} = 3.3 V.

Table 78. LPUART DC electrical characteristics (DV_{DD}/EV_{DD} = 3.3 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/EV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x D/EV_{DD}	V	1
Input current (D/EV_{IN} = 0 V or D/EV_{IN} = D/EV_{DD})	I_{IN}	—	±50	μA	—
Output high voltage (I_{OH} = -2.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (I_{OL} = 2.0 mA)	V_{OL}	—	0.4	V	—
Notes:					

Table 78. LPUART DC electrical characteristics (DV_{DD}/EV_{DD} = 3.3 V)[2]

Parameter	Symbol	Min	Max	Unit	Notes
1. The min V_{IL} and max V_{IH} values are based on the min and max D/EV_{DD} respective values found in Table 4.					
2. For recommended operating conditions, see Table 4.					

This table provides the DC electrical characteristics for the LPUART interface when operating at EV_{DD}/ DV_{DD} = 1.8 V.

Table 79. LPUART DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x E/ DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x E/DV_{DD}	V	1
Input current (E/DV_{IN} = 0 V or E/DV_{IN} = E/DV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (E/DV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (DV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—
Notes:					
1. The min V_{IL} and max V_{IH} values are based on the min and max E/DV_{DD} respective values found in Table 4.					
2. The symbol E/DV_{IN} represents the input voltage of the supply referenced in Table 4.					
3. For recommended operating conditions, see Table 4.					

3.13.2 LPUART AC timing specifications

This table provides the AC timing specifications for the LPUART interface.

Table 80. LPUART AC timing specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{PLAT}/(2 x 32 x 8192)	baud	1, 3, 4
Maximum baud rate	f_{PLAT}/(2 x 4)	baud	1, 2, 4
Notes:			
1. f_{PLAT} refers to the internal platform clock.			
2. The actual attainable baud rate is limited by the latency of interrupt processing.			
3. Every bit can be over sampled with a sample clock rate of 8 and 64 times (software configurable) and each bit is the majority of the values sampled at the sample rate divided by two, (sample rate/2)+1 and (sample rate/2)+2.			
4. The 1-to-0 transition during a data word can cause a resynchronization of the sample point.			

3.14 DUART interface

This section describes the DC and AC electrical specifications for the DUART interface.

3.14.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 3.3 V.

Table 81. DUART DC electrical characteristics (3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -2.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (DV_{DD} = min, I_{OL} = 2.0 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 4.
2. The symbol DV_{IN} represents the input voltage of the supply referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 1.8 V.

Table 82. DUART DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (DV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the min and max DV_{IN} respective values found in Table 4.
2. The symbol DV_{IN} represents the input voltage of the supply referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.14.2 DUART AC timing specifications

This table provides the AC timing specifications for the DUART interface.

Table 83. DUART AC timing specifications

Parameter	Value	Unit	Notes
Minimum baud rate	f_{PLAT}/(2 x 1,048,576)	baud	1, 3
Maximum baud rate	f_{PLAT}/(2 x 16)	baud	1, 2

Notes:

1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

3.15 Flextimer interface

This section describes the DC and AC electrical characteristics for the Flextimer interface. There are Flextimer pins on various power supplies in this device.

3.15.1 Flextimer DC electrical characteristics

This table provides the DC electrical characteristics for Flextimer pins operating at DV_{DD}/EV_{DD} = 3.3 V.

Table 84. Flextimer DC electrical characteristics (DV_{DD}/EV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/EV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x D/EV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN}= D/EV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (D/EV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (D/EV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN}/EV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the DV_{IN}/EV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for Flextimer pins operating at $DV_{DD}/EV_{DD}/LV_{DD}/OV_{DD}$ = 1.8 V.

Table 85. Flextimer DC electrical characteristics ($DV_{DD}/EV_{DD}/LV_{DD}/OV_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/E/L/ OV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x D/E/L/V_{DD}	V	1
Input low voltage	V_{IL}	—	0.3 x OV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = D/E/L/ OV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (D/E/L/OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (D/E/L/OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max $DV_{IN}/EV_{IN}/L/OV_{IN}$ values found in Table 4.
2. The symbol V_{IN}, in this case, represents the $DV_{IN}/EV_{IN}/L/OV_{IN}$ symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for Flextimer pins operating at LV_{DD} = 2.5 V.

Table 86. Flextimer DC electrical characteristics (LV_{DD}= 2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LVDD	—	V	1
Input low voltage	V_{IL}	—	0.2 x LVDD	V	1
Input current (V_{IN} = 0 V or V_{IN}= LV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.15.2 Flextimer AC timing specifications

This table provides the Flextimer AC timing specifications.

Table 87. Flextimer AC timing specifications[2]

Parameter	Symbol	Min	Unit	Notes
Flextimer inputs—minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. Flextimer inputs and outputs are asynchronous to any visible clock. Flextimer outputs should be synchronized before use by any external synchronous logic. Flextimer inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

2. For recommended operating conditions, see Table 4.

This figure provides the AC test load for the Flextimer.

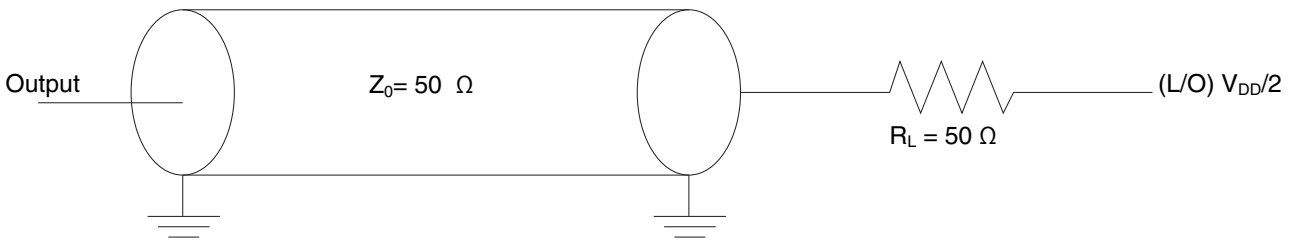


Figure 58. Flextimer AC test load

3.16 SPI interface

This section describes the DC and AC electrical characteristics for the SPI interface.

3.16.1 SPI DC electrical characteristics

This table provides the DC electrical characteristics for the SPI interface operating at OV_{DD} = 1.8 V.

Table 88. SPI DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.3 x OV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

Table 88. SPI DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 4.					
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 4.					
3. For recommended operating conditions, see Table 4.					

3.16.2 SPI AC timing specifications

This table provides the SPI timing specifications.

Table 89. SPI AC timing specifications

Parameter	Symbol	Condition	Min	Max	Unit	Notes
SCK clock pulse width	t_{SDC}	—	40%	60%	t_{SCK}	—
CS to SCK delay	t_{CSC}	Master	tp*2 - 5.0	—	ns	1, 2
After SCK delay	t_{ASC}	Master	tp*2 - 1.0	—	ns	1, 3
Data setup time for inputs	t_{NIIVKH}	Master	9	—	ns	—
Data hold time for inputs	t_{NIIXKH}	Master	0	—	ns	—
Data valid (after SCK edge) for Outputs	t_{NIKHOV}	Master	—	5	ns	—
Data hold time for outputs	t_{NIKHOX}	Master	0	—	ns	—
Notes: 1. tp represents the input clock period for the SPI controller. 2. Refer the CTARx register in QorIQ LS1046ARM for more details. The t_{CSC} = tp*(Delay Scaler Value)*CTARx[PCSSCK] -5.0, where the Delay Scaler Value comes from Table Delay Scaler Encoding. For example, the t_{CSC} = tp*4*3-5.0 when CTARx[PCSSCK] = 0b01, CTARx[CSSCK]=0b0001. 3. Refer the CTARx register in QorIQ LS1046ARM for more details. The t_{ASC} = tp*(Delay Scaler Value)*CTARx[PASC] -1.0, where the Delay Scaler Value comes from Table Delay Scaler Encoding. For example, the t_{ASC} = tp*8*3-1.0 when CTARx[PASC] = 0b01, CTARx[ASC]=0b0010.						

This figure shows the SPI timing master when CPHA = 0.

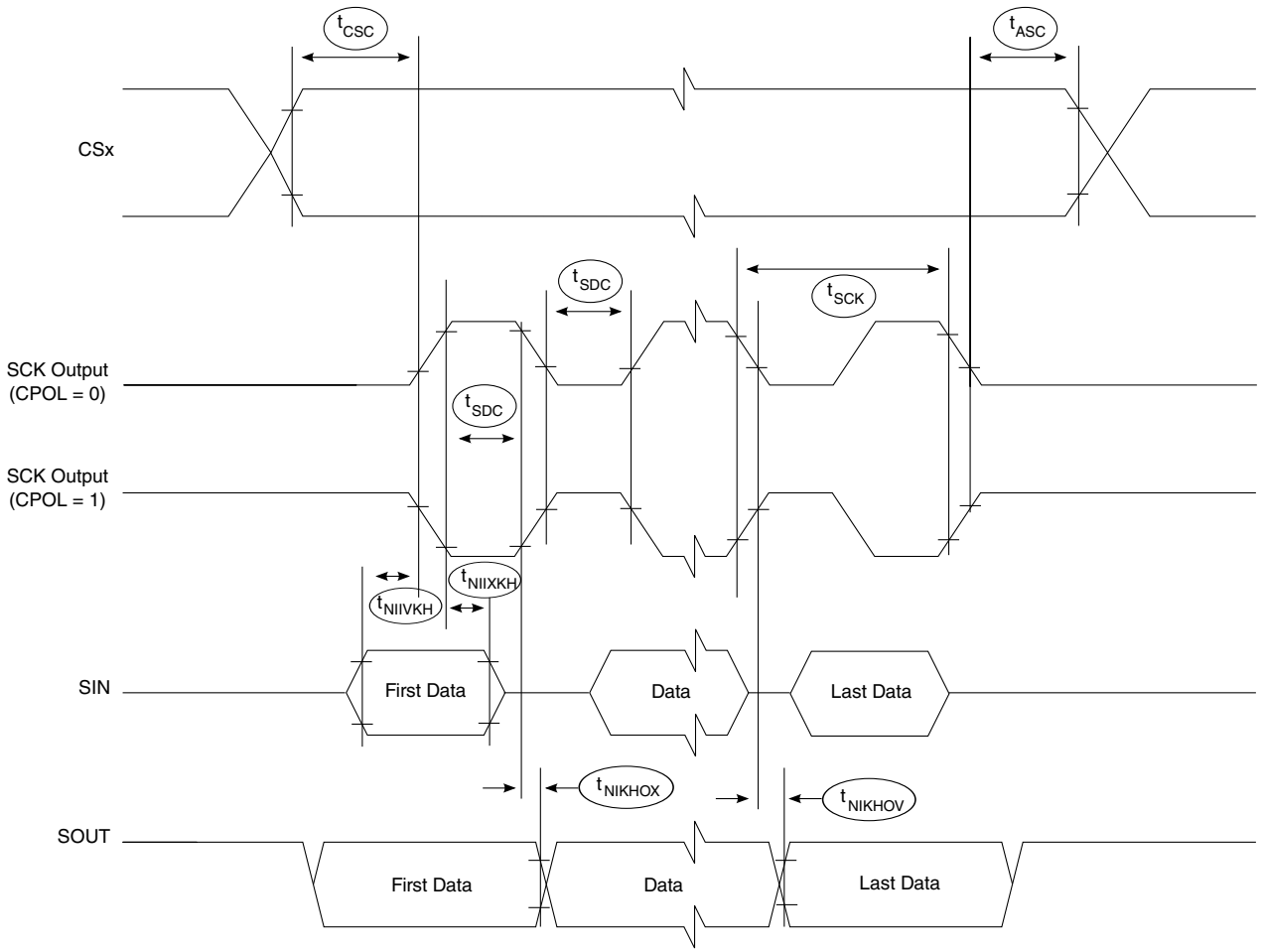


Figure 59. SPI timing master, CPHA = 0

This figure shows the SPI timing master when CPHA = 1.

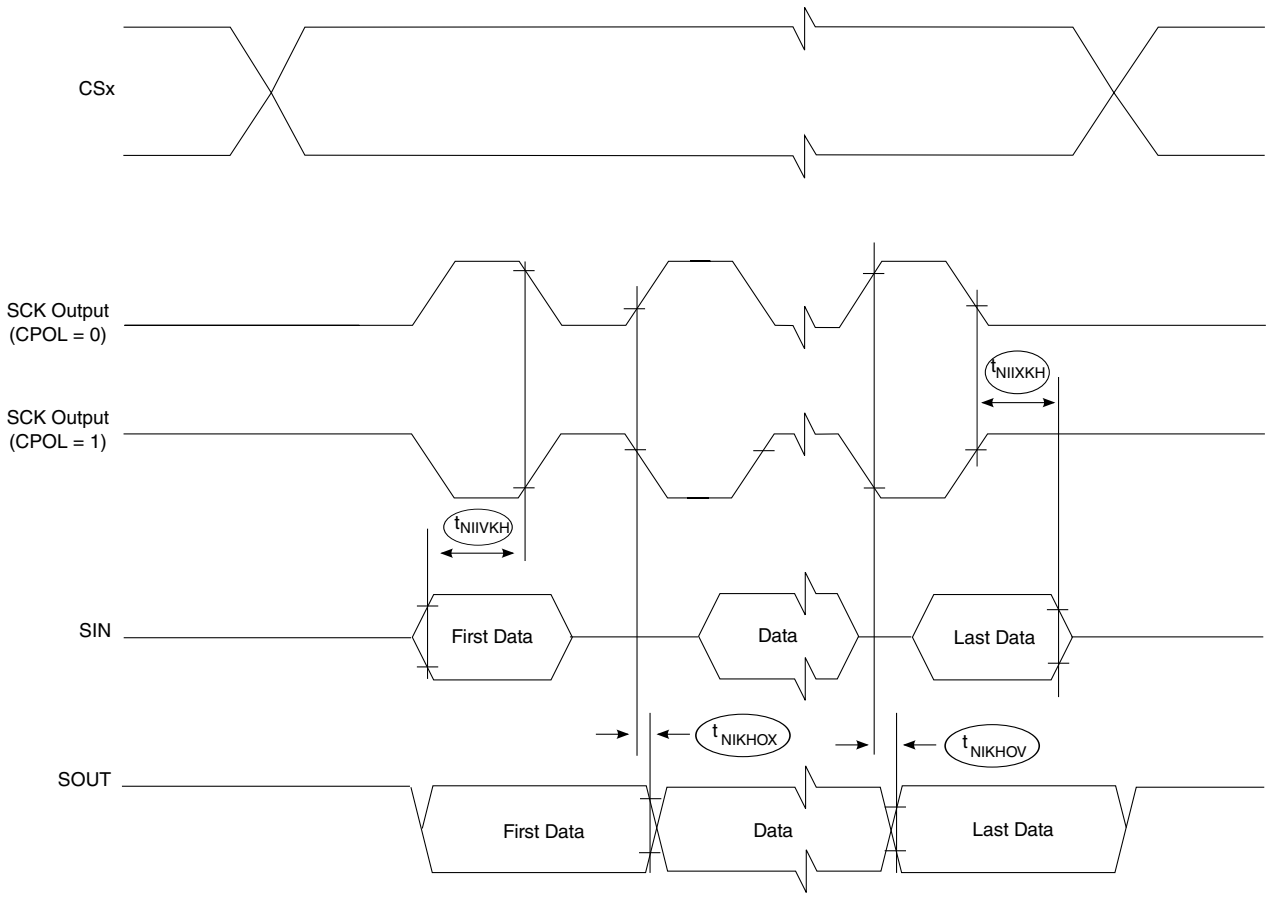


Figure 60. SPI timing master, CPHA = 1

3.17 QSPI interface

This section describes the DC and AC electrical characteristics for the QSPI interface.

3.17.1 QSPI DC electrical characteristics

This table provides the DC electrical characteristics for the QSPI interface operating at OV_{DD} = 1.8 V.

Table 90. QSPI DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.3 x OV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage	V_{OH}	OV_{DD} - 0.2	—	V	—

Table continues on the next page...

Table 90. QSPI DC electrical characteristics (1.8 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
(OV_{DD} = min, I_{OH} = -0.5 mA)					
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.17.2 QSPI AC timing specifications

This section describes the QuadSPI timing specifications in Single data rate (SDR) mode. All data is based on a negative edge data launch and a positive edge data capture for the flash device. Double data rate (DDR)/Double trasfer rate (DTR) mode is not supported.

3.17.2.1 QSPI timing SDR mode

This table provides the QSPI input and output timing in SDR mode.

Table 91. SDR mode QSPI input and output timing

Parameter	Symbol	Min	Max	Unit
Clock frequency	F_{SCK}	—	62.5	MHz
Clock rise/fall time	T_{RISE}/T_{FALL}	1	—	ns
CS output hold time	$t_{NIKHOX2}$	-3.4 + j * T	—	ns
CS output delay	$t_{NIKHOV2}$	-3.5 + k * T	—	ns
Setup time for incoming data	t_{NIIVKH}	8.6	—	ns
Hold time requirement for incoming data	t_{NIIXKH}	0.4	—	ns
Output data valid	t_{NIKHOV}	—	4.5	ns
Output data hold	t_{NIKHOX}	-4.4	—	ns

NOTE

T represents the clock period, j represents qSPI_FLSHCR[TCSH], and k depends on qSPI_FLSHCR[TCSS].

This figure shows the QSPI AC timing in SDR mode.

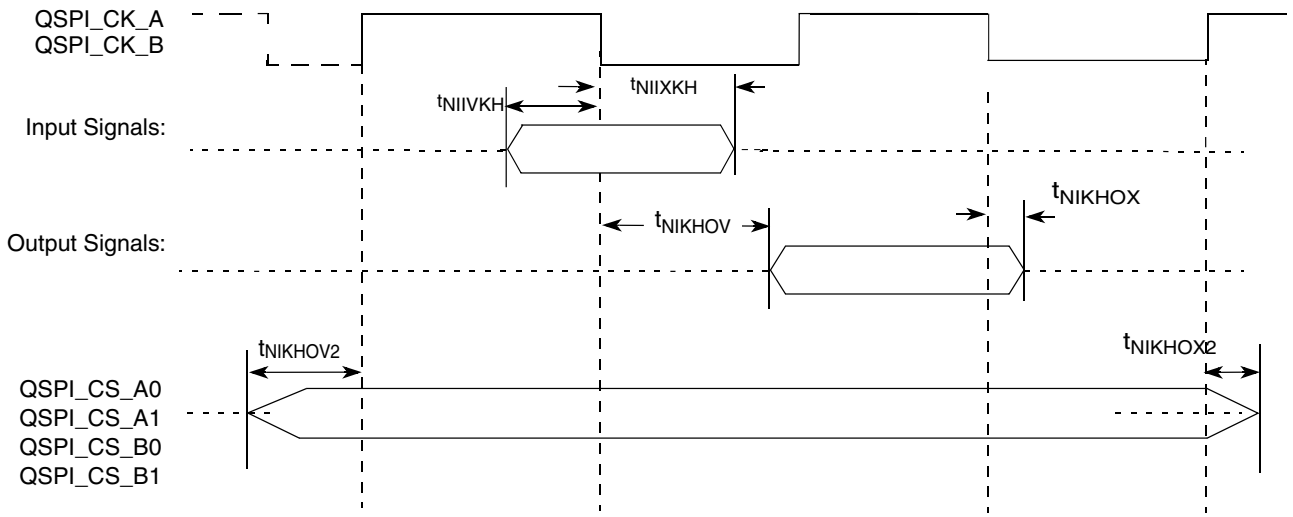


Figure 61. QSPI AC timing — SDR mode

3.18 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

3.18.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface at D/EV_{DD} = 3.3 V.

Table 92. eSDHC interface DC electrical characteristics[2]

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x D/EV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.25 x D/EV_{DD}	V	1
Output high voltage (D/EV_{DD} = min, I_{OH} = -100 μA)	V_{OH}	0.75 x D/EV_{DD}	-	V	-
Output low voltage (D/EV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	-	0.125 x D/EV_{DD}	V	-

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max D/EV_{IN} values found in Table 4 .
2. At recommended operating conditions with D/EV_{DD}= 3.3 V.

This table provides the DC electrical characteristics for the eSDHC interface at $D/O/EV_{DD}$ = 1.8 V.

Table 93. eSDHC interface DC electrical characteristics [3]

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $D/O/EV_{DD}$	-	V	1
Input low voltage	V_{IL}	-	0.3 x $D/O/EV_{DD}$	V	1
Output high voltage ($D/O/EV_{DD}$= min, I_{OH} = -2mA)	V_{OH}	$D/O/EV_{DD}$ - 0.45	-	V	-
Output low voltage ($D/O/EV_{DD}$= min, I_{OL} = 2mA)	V_{OL}	-	0.45	V	-

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max $DV_{IN}/OV_{IN}/EV_{IN}$ values found in Table 4 .

3. At recommended operating conditions $DV_{DD}/OV_{DD}/EV_{DD}$= 1.8V.

3.18.2 eSDHC AC timing specifications

This section provides the AC timing specifications.

This table provides the eSDHC AC timing specifications as defined in Figure 62, Figure 63, and Figure 64.

Table 94. eSDHC AC timing specifications (full-speed/high-speed mode)[6]

Parameter	Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency: • SD/SDIO (full-speed/high-speed mode) • eMMC (full-speed/high-speed mode)	f_{SHSCK}	0	25/50 26/52	MHz	2, 4
SDHC_CLK clock low time (full-speed/high-speed mode)	t_{SHSCKL}	10/7	-	ns	4
SDHC_CLK clock high time (full-speed/high-speed mode)	t_{SHSCKH}	10/7	-	ns	4
SDHC_CLK clock rise and fall times	$t_{SHSCKR/}$ t_{SHSCKF}	-	3	ns	4
Input setup times: SDHC_CMD, SDHC_DATx to SDHC_CLK	$t_{SHSIVKH}$	2.5	-	ns	3, 4, 5
Input hold times: SDHC_CMD, SDHC_DATx to SDHC_CLK	$t_{SHSIXKH}$	2.5	-	ns	4, 5
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOX}$	-3	-	ns	4, 5
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOV}$	-	3	ns	4, 5

Notes:

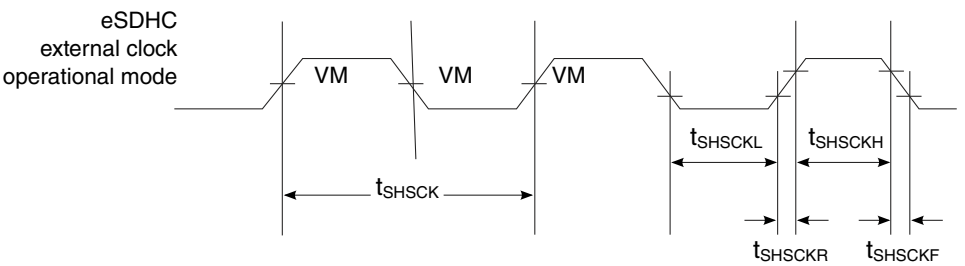
1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SHKHOX} symbolizes eSDHC high-speed mode device timing (SH) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. In full-speed mode, the clock frequency value can be 0-25MHz for an SD/SDIO card and 0-26MHz for an eMMC device. In high-speed mode, the clock frequency value can be 0-50MHz for an SD/SDIO card and 0-52MHz for an eMMC device.

Table 94. eSDHC AC timing specifications (full-speed/high-speed mode)[6]

Parameter	Symbol[1]	Min	Max	Unit	Notes
3. SDHC_SYNC_OUT/IN loop back is recommended to compensate the clock delay. In case the SDHC_SYNC_OUT/IN loopback is not used, to satisfy setup timing, one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1ns for any high-speed MMC card. For any high-speed or default speed mode SD card, the one-way board-routing delay between host and card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1.5ns. 4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF. 5. The parameter values apply to both full-speed and high-speed modes. 6. At recommended operating conditions with EV_{DD}=1.8 V or 3.3V, see Table 4.					

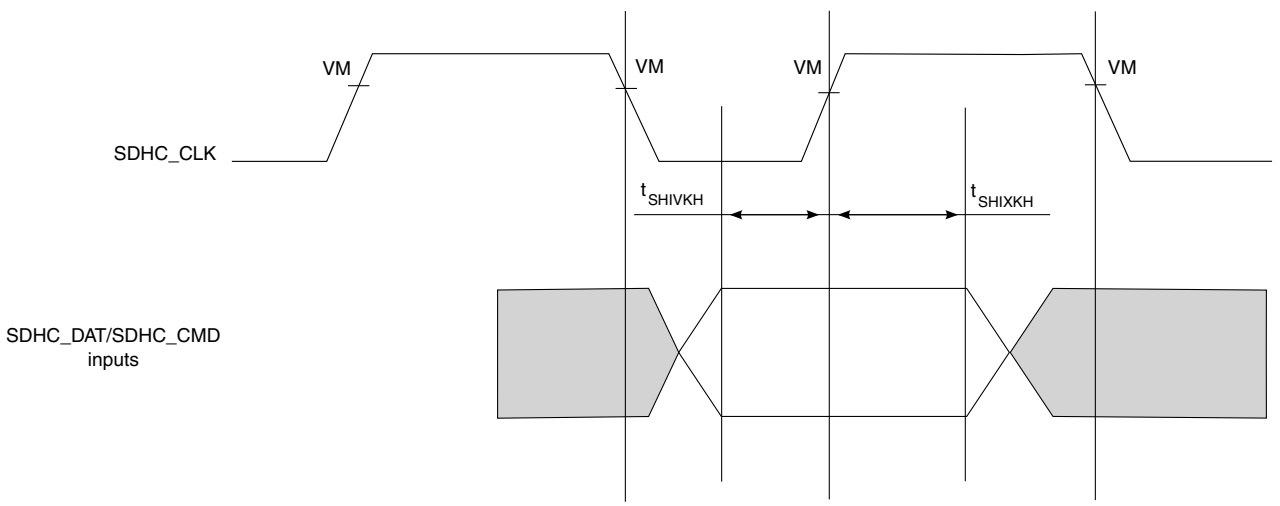
This figure provides the eSDHC clock input timing diagram.



VM = Midpoint voltage (Respective supply/2)

Figure 62. eSDHC clock input timing diagram

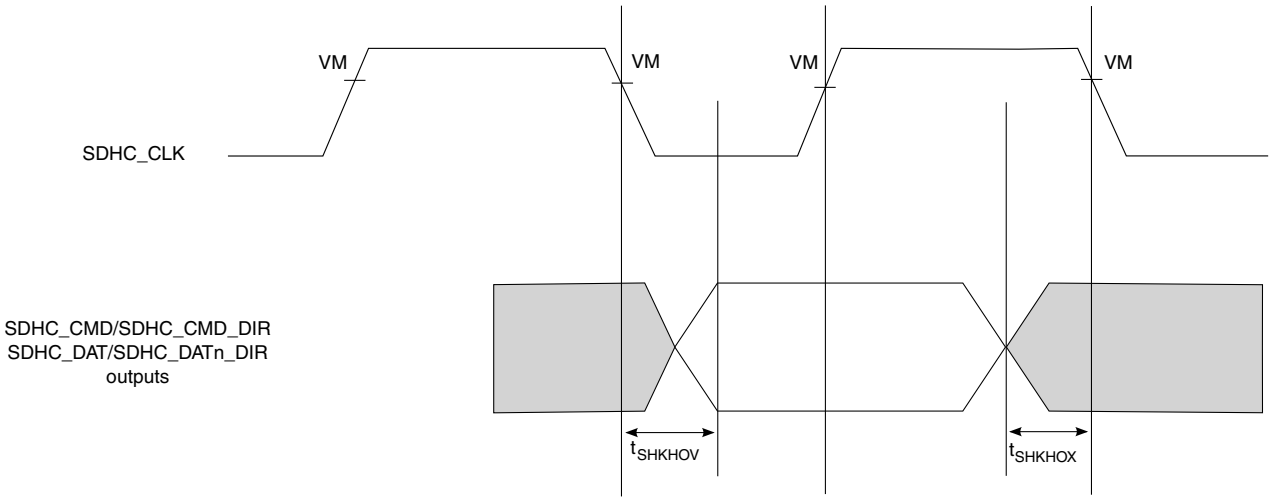
This figure provides the input AC timing diagram for high-speed mode.



VM = Midpoint voltage (EV_{DD}/2)

Figure 63. eSDHC high-speed mode input AC timing diagram

This figure provides the output AC timing diagram for high-speed mode.



VM = Midpoint voltage ($EV_{DD}/2$)

Figure 64. eSDHC high-speed mode output AC timing diagram

This table provides the eSDHC AC timing specifications for SDR50 mode.

Table 95. eSDHC AC timing specifications (SDR 50 mode)

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK clock frequency:	f_{SHSCK}	0	90	MHz	
SDHC_CLK duty cycle	t_{SHSCKH}/ t_{SHSCK}	45	55	%	
SDHC_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	-	2	ns	1
Skew between SD_CLK_SYNC_OUT and SD_CLK	-	-0.1	0.1	ns	1
Input setup times: SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN	$t_{SHSIVKH}$	3.21	-	ns	2,1
Input hold times: SDHC_CMD, SDHC_DATx to SDHC_CLK_SYNC_IN	$t_{SHSIXKH}$	1.1	-	ns	2,1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_DATx_DIR, SDHC_CMD_DIR	$t_{SHSKHOX}$	1.7	-	ns	2,1
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_DATx_DIR, SDHC_CMD_DIR	$t_{SHSKHOV}$	-	7.21	ns	2,1

Notes:

1. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 30$ pF
2. Without a voltage translator
3. At recommended operating conditions with EV_{DD}=1.8 V, see Table 4.

This figure provides the eSDHC clock input timing diagram for SDR50 mode.

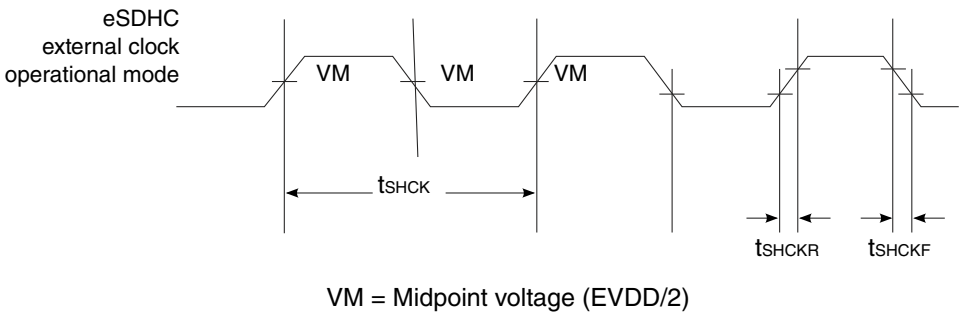


Figure 65. eSDHC SDR50 mode clock input timing diagram

This figure provides the eSDHC input AC timing diagram for SDR50 mode.

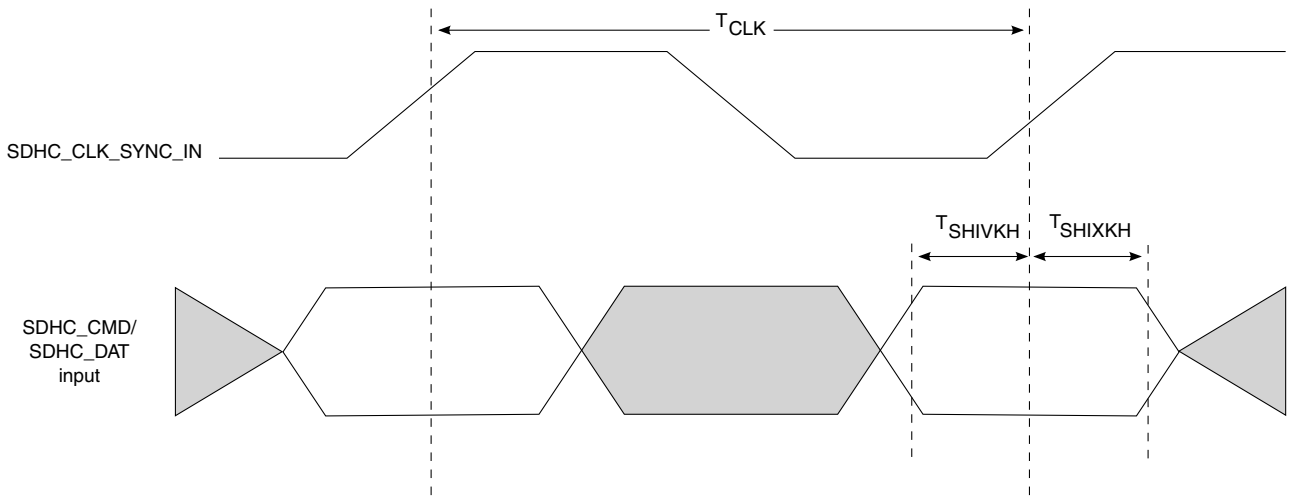


Figure 66. eSDHC SDR50 mode input AC timing diagram

This figure provides the eSDHC output timing diagram for SDR50 mode.

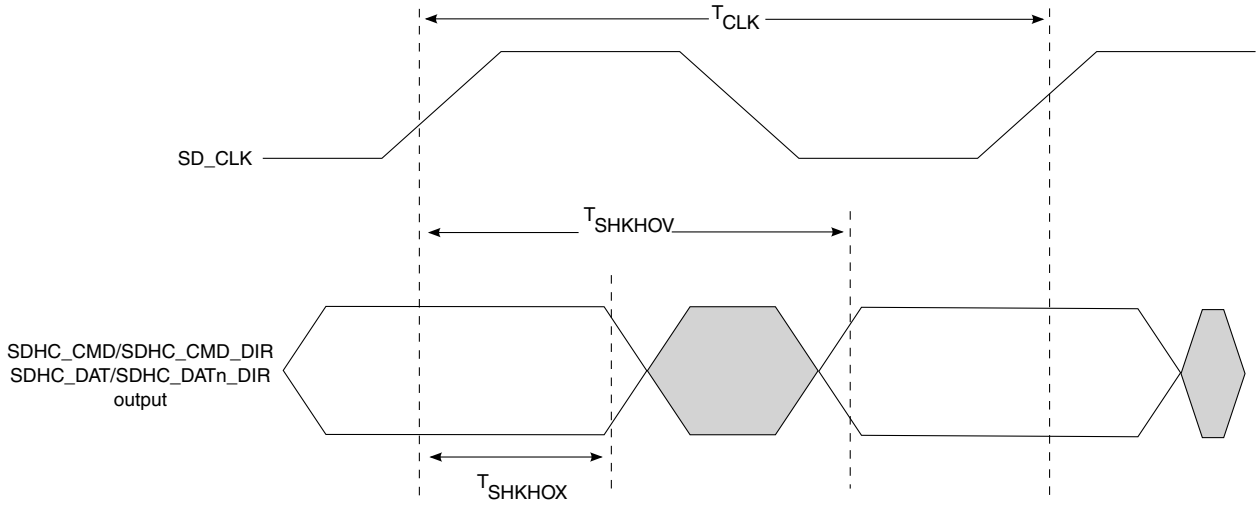


Figure 67. eSDHC SDR50 mode output timing diagram

This table provides the eSDHC AC timing specifications for DDR50/DDR mode.

Table 96. eSDHC AC timing specifications (DDR50/DDR)[3]

Parameter	Symbol	Min	Max	Unit	Notes
SDHC_CLK clock frequency	f_{SHCK}	-	-	MHz	-
SD/SDIO DDR50 mode			50		
eMMC DDR mode			52		
SDHC_CLK duty cycle	t_{SHSCKH}/ t_{SHSCK}	47	53	%	
Skew between SDHC_CLK_SYNC_OUT and SDHC_CLK	-	-0.1	0.1	ns	-
SDHC_CLK clock rise and fall times	t_{SHCKR}/ t_{SHCKF}	-	-	ns	1
SD/SDIO DDR50 mode			4		2
eMMC DDR mode			2		
Input setup times: SDHC_DATx to SDHC_CLK_SYNC_IN	$t_{SHDIVKH}$	-	-	ns	1, 4
SD/SDIO DDR50 mode		2.0			2
eMMC DDR mode		1.6			
Input hold times: SDHC_DATx to SDHC_CLK_SYNC_IN	$t_{SHDIXKH}$	-	-	ns	1
SD/SDIO DDR50 mode		1.1			2
eMMC DDR mode		1.1			
Output hold time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	$t_{SHDKHOX}$	-	-	ns	1
SD/SDIO DDR50 mode		1.7			2
eMMC DDR mode		3.4			
Output delay time: SDHC_CLK to SDHC_DATx valid, SDHC_DATx_DIR	$t_{SHDKHOV}$	-	-	ns	1
			6.1		2

Table continues on the next page...

Table 96. eSDHC AC timing specifications (DDR50/DDR)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
SD/SDIO DDR50 mode eMMC DDR mode			6.2		
Input setup times: SDHC_CMD to SDHC_CLK_SYNC_IN	$t_{SHCIVKH}$	- 5.3 4.5	-	ns	1 2
SD/SDIO DDR50 mode eMMC DDR mode					
Input hold times: SDHC_CMD to SDHC_CLK_SYNC_IN	$t_{SHCIXKH}$	- 1.1 1.1	-	ns	1 2
SD/SDIO DDR50 mode eMMC DDR mode					
Output hold time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	$t_{SHCKHOX}$	- 1.7 3.9	-	ns	1 2
SD/SDIO DDR50 mode eMMC DDR mode					
Output delay time: SDHC_CLK to SDHC_CMD valid, SDHC_CMD_DIR	$t_{SHCKHOV}$	-	- 13.1 15.3	ns	1 2
SD/SDIO DDR50 mode eMMC DDR mode					

Notes:

1. $C_{CARD} \leq 10$ pF, (1 card).
2. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 20$ pF for MMC, ≤ 25 pF for Input Data of DDR50, ≤ 30 pF for Input CMD of DDR50.
3. At recommended operating conditions with EV_{DD} = 1.8 or 3.3 V for eMMC DDR mode, EV_{DD} = 1.8 V for DDR50, see Table 4.

This figure provides the eSDHC DDR50/DDR mode input AC timing diagram.

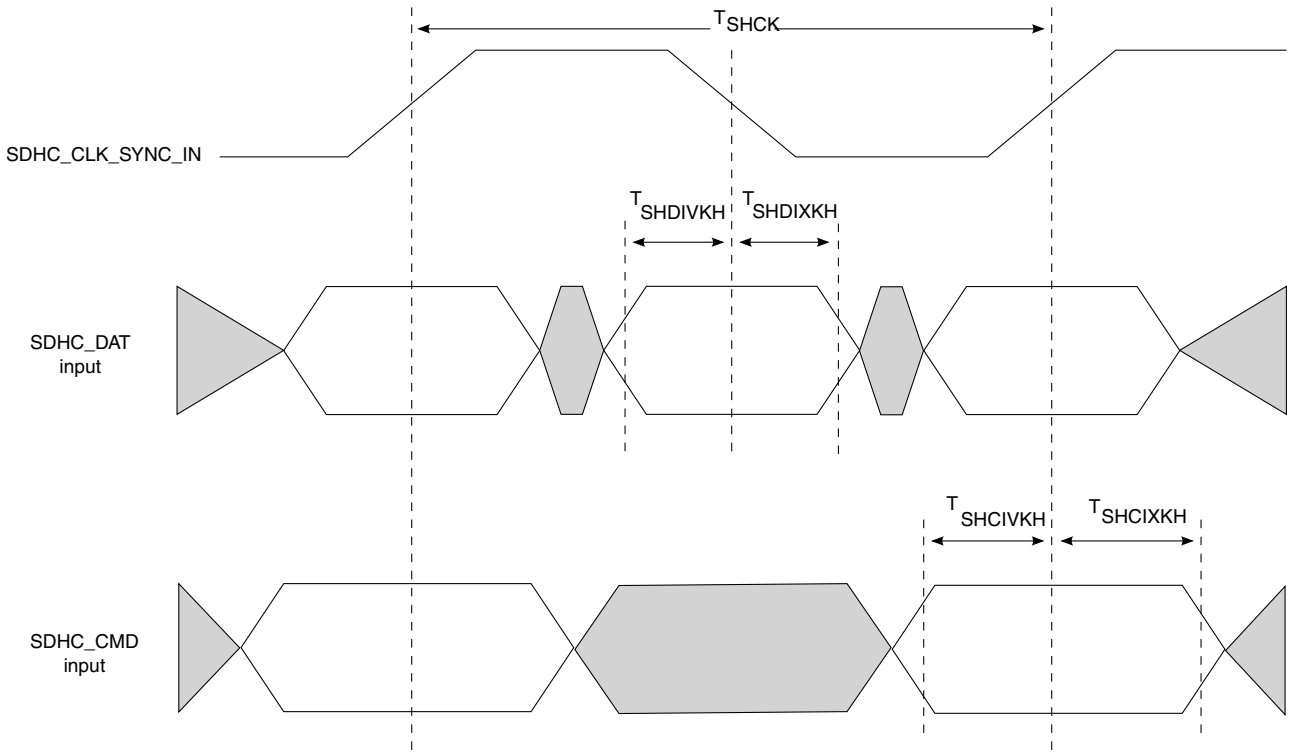


Figure 68. eSDHC DDR50/DDR mode input AC timing diagram

This figure provides the eSDHC DDR50/DDR mode output AC timing diagram.

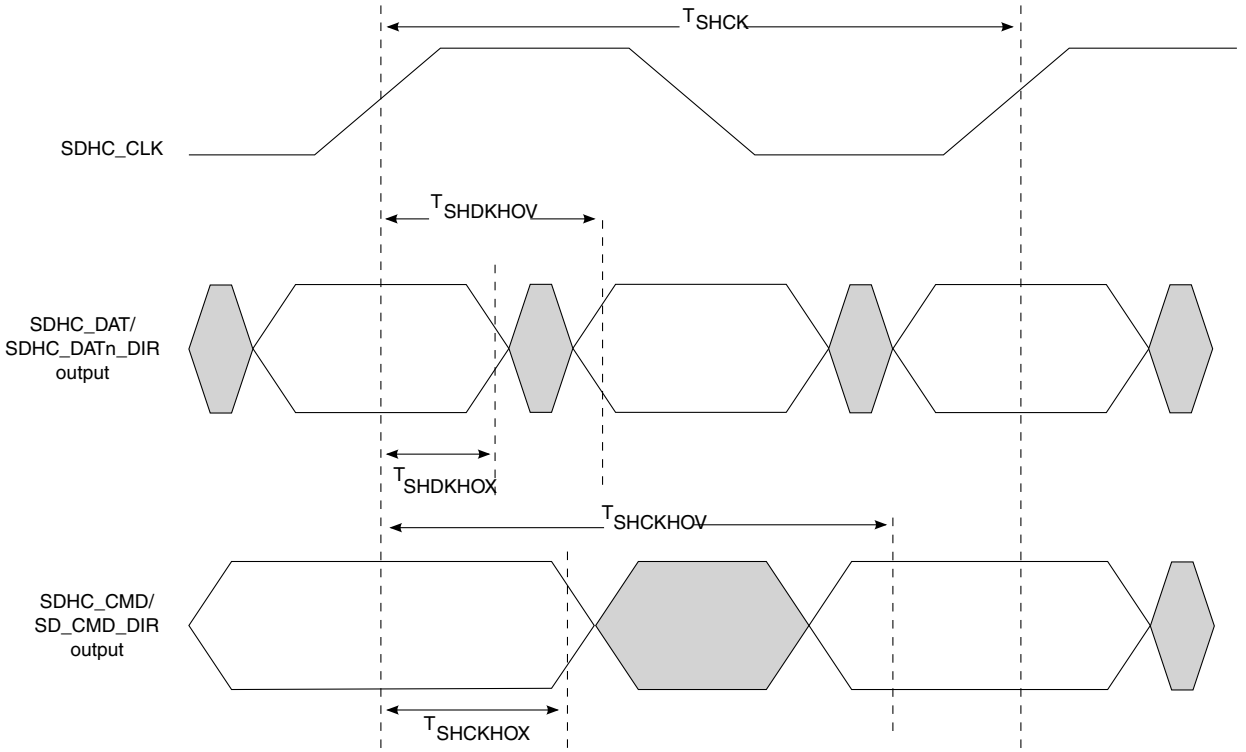


Figure 69. eSDHC DDR50/DDR mode output AC timing diagram

This table provides the eSDHC AC timing specifications for SDR104/eMMC HS200 mode.

Table 97. eSDHC AC timing specifications (SDR104/eMMC HS200)

Parameter		Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency	SD/SDIO SDR104 mode	f_{SHCK}	-	167	MHz	1
	eMMC HS200 mode			167		-
SDHC_CLK duty cycle		t_{SHSCKH}/t_{SHSCK}	40	60	%	
SDHC_CLK clock rise and fall times		t_{SHCKR}/t_{SHCKF}	-	1	ns	1
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{SHKHOX}	1.58	-	ns	1
	eMMC HS200 mode		1.6			
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid, SDHC_CMD_DIR, SDHC_DATx_DIR	SD/SDIO SDR104 mode	T_{SHKHOV}	-	3.94	ns	1
	eMMC HS200 mode			3.92		
Input data window (UI)	SD/SDIO SDR104 mode	t_{SHIDV}	0.5	-	Unit Interval	1
	eMMC HS200 mode		0.475			

Notes:

1. $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 15pF$.
2. At recommended operating conditions with EV_{DD} =1.8 V, see Table 4.

This figure provides the eSDHC SDR104/HS200 mode timing diagram.

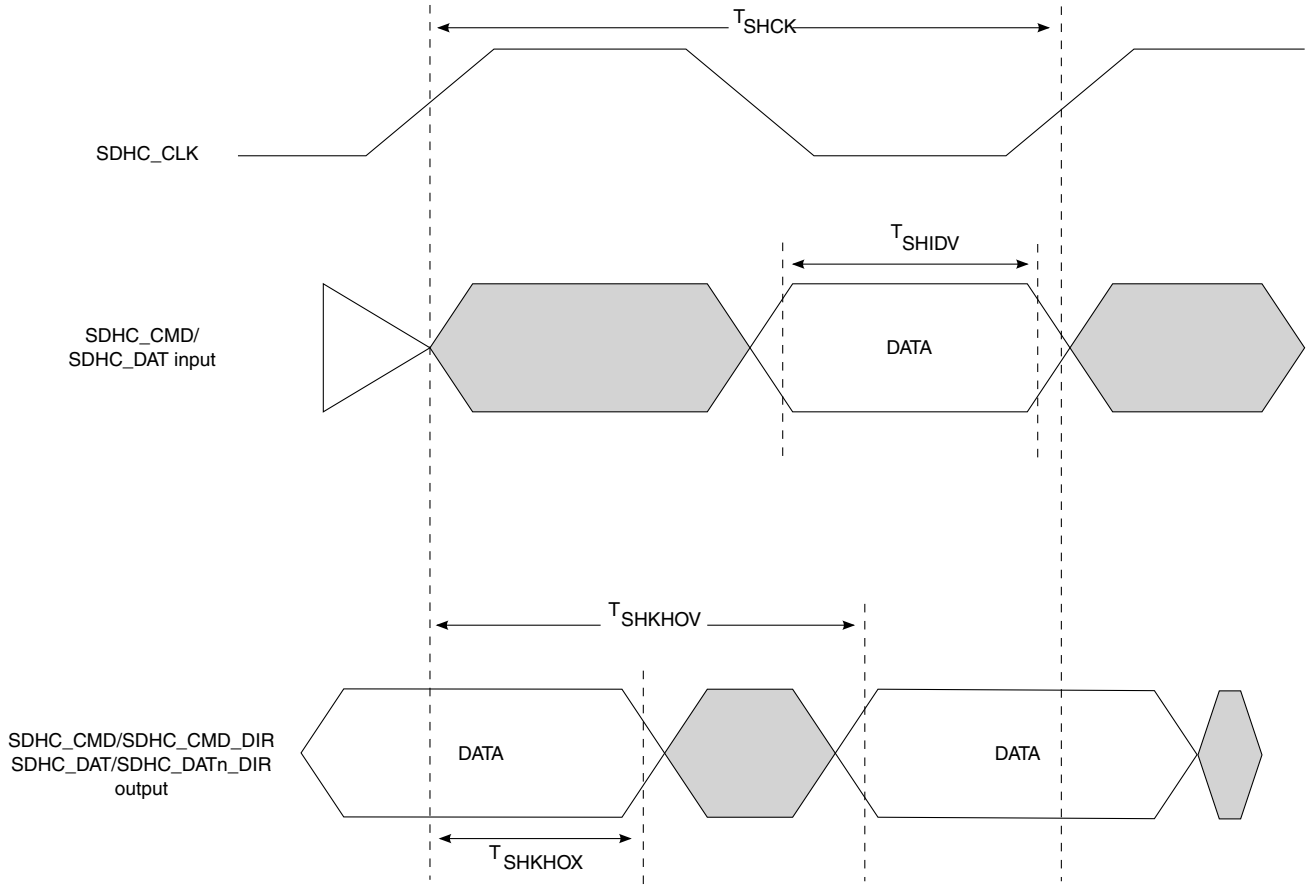


Figure 70. eSDHC SDR104/HS200 mode timing diagram

3.19 JTAG controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

3.19.1 JTAG DC electrical characteristics

This table provides the JTAG DC electrical characteristics.

Table 98. JTAG DC electrical characteristics (OV_{DD} = 1.8V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.3 x OV_{DD}	V	1

Table continues on the next page...

Table 98. JTAG DC electrical characteristics (OV_{DD} = 1.8V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	-100/+50	μA	2, 4
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (OV_{DD} = min, I_{OL}= 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol found in Table 4.
3. For recommended operating conditions, see Table 4.
4. Per IEEE Std. 1149.1 specification, TDI, TMS, and TRST_B have internal pull-up.

3.19.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 71, Figure 72, Figure 73, and Figure 74.

Table 99. JTAG AC timing specifications[4]

Parameter		Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation		f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time		t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V		t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times		t_{JTGR}/t_{JTGF}	0	2	ns	—
TRST_B assert time		t_{TRST}	25	—	ns	2
Input setup times		t_{JTDVKH}	4	—	ns	—
Input hold times		t_{JTDXKH}	10	—	ns	—
Output valid times	Boundary-scan data	t_{JTKLDV}	—	15	ns	3
	TDO		—	10		
Output hold times		t_{JTKLDX}	0	—	ns	3

Notes:

1. The symbols used for timing specifications follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2.TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.

3. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

4. For recommended operating conditions, see Table 4.

This figure shows the AC test load for TDO and the boundary-scan outputs of the device.

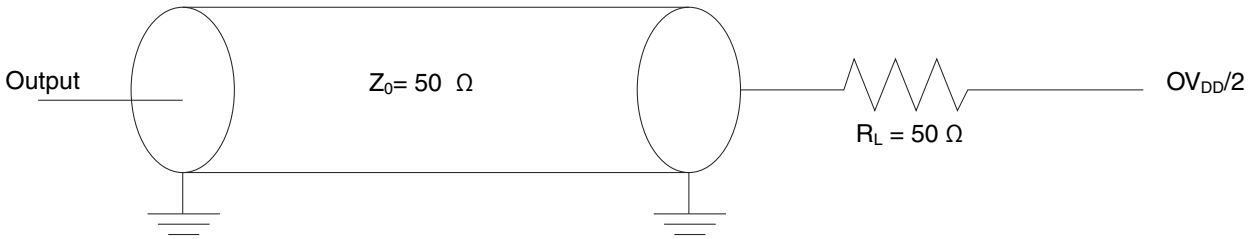


Figure 71. AC test load for the JTAG interface

This figure shows the JTAG clock input timing diagram.

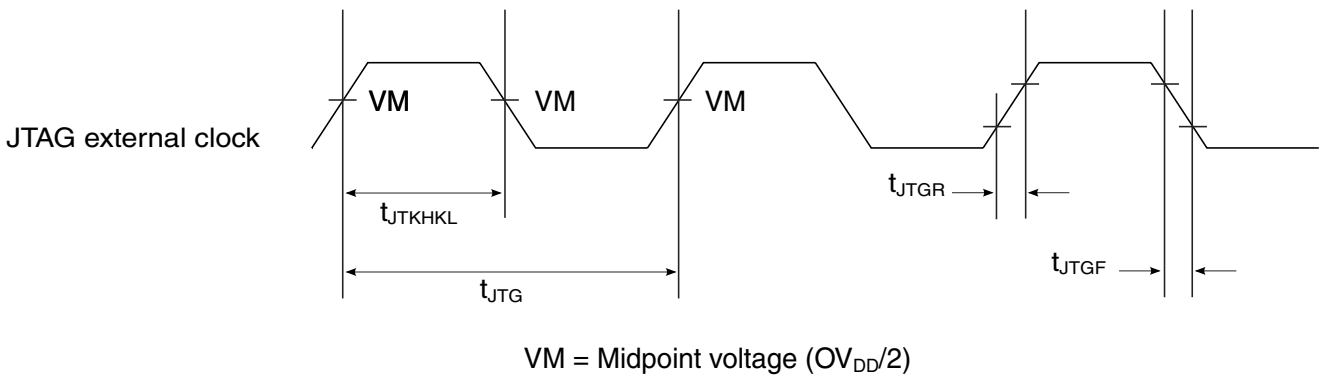


Figure 72. JTAG clock input timing diagram

This figure shows the TRST_B timing diagram.

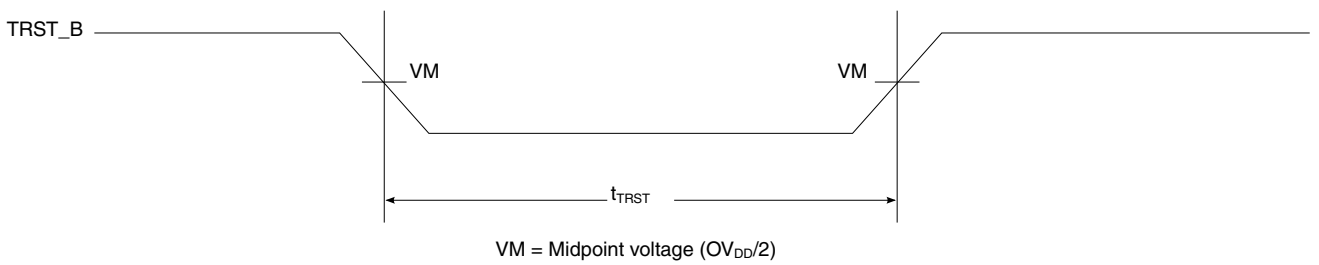


Figure 73. TRST_B timing diagram

This figure shows the boundary-scan timing diagram.

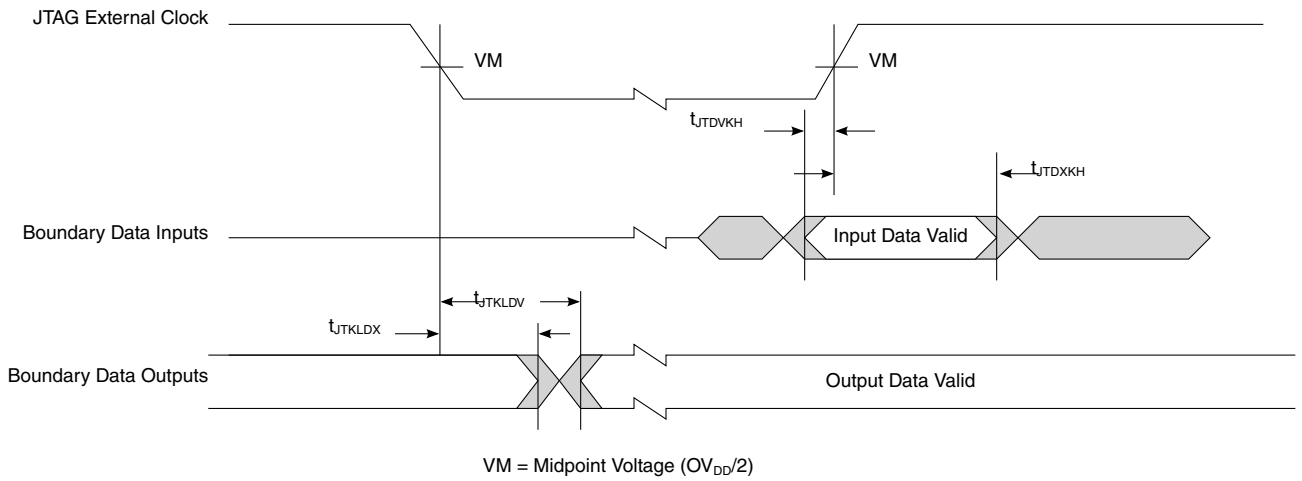


Figure 74. Boundary-scan timing diagram

3.20 I²C interface

This section describes the DC and AC electrical characteristics for the I²C interfaces.

3.20.1 I²C DC electrical characteristics

This table provides the DC electrical characteristics for the I²C interfaces operating at DV_{DD} = 3.3 V.

Table 100. I²C DC electrical characteristics (DV_{DD} = 3.3 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Output low voltage (DV_{DD} = min, I_{OL} = 3 mA)	V_{OL}	—	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} and 0.9 x DV_{DD}(max)	I_I	-50	50	μA	-
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 4.
2. The output voltage (open drain or open collector) condition = 3 mA sink current.

Table 100. I²C DC electrical characteristics (DV_{DD} = 3.3 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
3. See the chip reference manual for information about the digital filter used.					
4. For recommended operating conditions, see Table 4.					

This table provides the DC electrical characteristics for the I²C interfaces operating at DV_{DD} = 1.8 V.

Table 101. I²C DC electrical characteristics (DV_{DD} = 1.8 V)[5]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Output low voltage (DV_{DD} = min, I_{OL} = 3 mA)	V_{OL}	0	0.36	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 x DV_{DD} and 0.9 x DV_{DD}(max)	I_I	-50	50	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—
Notes:					
1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 4.					
2. The output voltage (open drain or open collector) condition = 3 mA sink current.					
3. See the chip reference manual for information about the digital filter used.					
4. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.					
5. For recommended operating conditions, see Table 4.					

3.20.2 I²C AC timing specifications

This table provides the AC timing specifications for the I²C interfaces.

Table 102. I²C AC timing specifications[5]

Parameter	Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—

Table continues on the next page...

Table 102. I²C AC timing specifications[5] (continued)

Parameter		Symbol[1]	Min	Max	Unit	Notes
Data input hold time	CBUS compatible masters	t_{I2DXKL}	—	—	μs	3
	I²C bus devices		0	—		
Data output delay time		t_{I2OVKL}	—	0.9	μs	4
Setup time for STOP condition		t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition		t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)		V_{NL}	0.1 x DV_{DD}	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)		V_{NH}	0.2 x DV_{DD}	—	V	—
Capacitive load for each bus line		Cb	—	400	pF	—

Notes:

1. The symbols used for timing specifications herein follow these patterns: $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.

2. The requirements for I²C frequency calculation must be followed. See *Determining the I²C Frequency Divider Ratio for SCL* (AN2919).

3. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, see *Determining the I²C Frequency Divider Ratio for SCL* (AN2919).

4. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

5. For recommended operating conditions, see Table 4.

This figure shows the AC test load for the I²C.

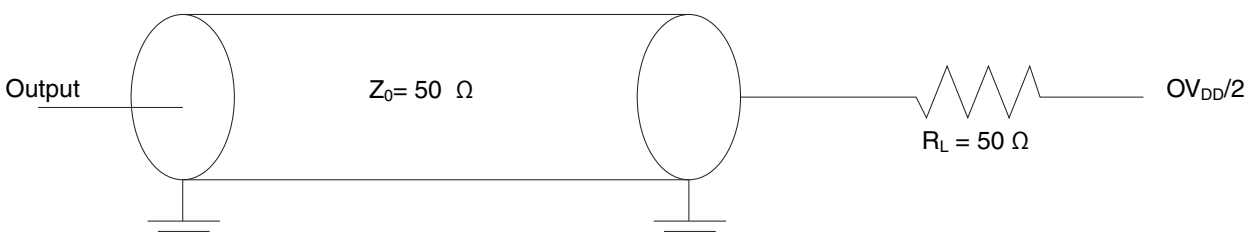


Figure 75. I²C AC test load

This figure shows the AC timing diagram for the I²C bus.

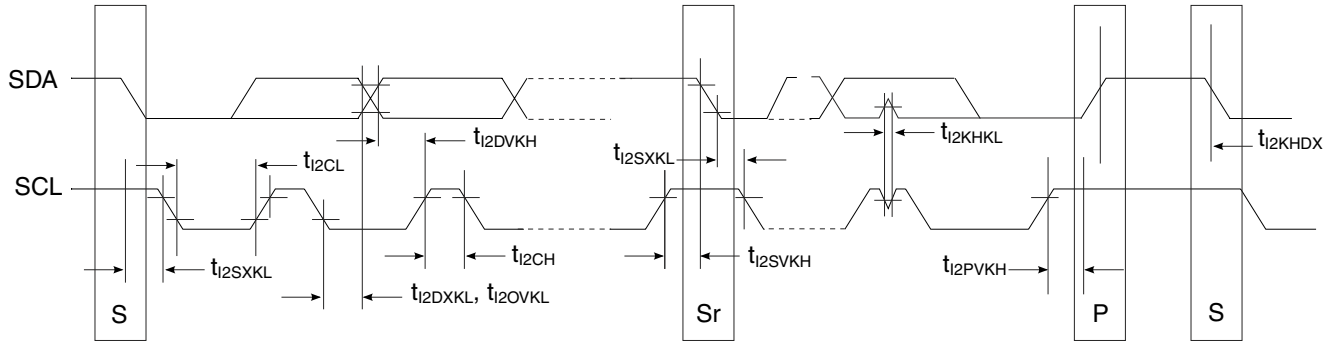


Figure 76. I²C bus AC timing diagram

3.21 GPIO interface

This section describes the DC and AC electrical characteristics for the GPIO interface. There are GPIO pins on various power supplies in this device.

3.21.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for GPIO pins operating at EV_{DD} = 3.3 V.

Table 103. GPIO DC electrical characteristics (EV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x EV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x EV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN}= LV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (EV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (EV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max EV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the EV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for GPIO pins operating at TV_{DD}/ LV_{DD} = 2.5 V.

Table 104. GPIO DC electrical characteristics (TV_{DD}/LV_{DD} = 2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x T/LV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x T/LV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN}= T/LV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (T/LV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.0	—	V	—
Output low voltage (T/LV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max L/TV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the L/TV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for GPIO pins operating at $LV_{DD}/EV_{DD}/DV_{DD}/TV_{DD}/OV_{DD}$ = 1.8 V.

Table 105. GPIO DC electrical characteristics ($LV_{DD}/EV_{DD}/DV_{DD}/TV_{DD}/OV_{DD}$ = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $L/E/D/T/OV_{DD}$	—	V	1
Input low voltage	V_{IL}	—	0.2 x $L/E/D/TV_{DD}$	V	1
Input low voltage	V_{IL}	—	0.3 x OV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN} = $L/E/D/T/OV_{DD}$)	I_{IN}	—	±50	μA	2
Output high voltage ($L/E/D/T/OV_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage ($L/E/D/T/OV_{DD}$ = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max $LV_{IN}/EV_{IN}/DV_{IN}/TV_{IN}/OV_{IN}$ values found in Table 4.
2. The symbol V_{IN}, in this case, represents the $LV_{IN}/EV_{IN}/DV_{IN}/TV_{IN}/OV_{IN}$ symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the DC electrical characteristics for GPIO pins operating at TV_{DD} = 1.2 V.

Table 106. GPIO DC electrical characteristics (TV_{DD} = 1.2 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x TV_{DD}	—	V	
Input low voltage	V_{IL}	—	0.2 x TV_{DD}	V	
Output low current current (V_{OL}= 0.2 V)	I_{OL}	4		mA	
Output high voltage (TV_{DD} = min, I_{OH} = -100uA)	V_{OH}	1.0	—	V	—
Output low voltage (TV_{DD} = min, I_{OL} = 100uA)	V_{OL}	—	0.2	V	—
Input Capacitance	C_{IN}	—	10	pF	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max TV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the TV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

3.21.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

Table 107. GPIO Input AC timing specifications

Parameter	Symbol	Min	Unit	Notes
GPIO inputs-minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least tPIWID to ensure proper operation.
2. For recommended operating conditions, see Table 4.

This figure provides the AC test load for the GPIO.

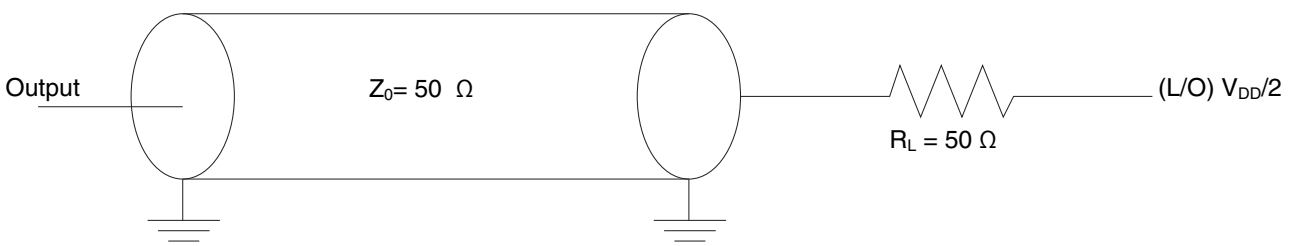


Figure 77. GPIO AC test load

3.22 GIC interface

This section describes the DC and AC electrical characteristics for the GIC interface.

3.22.1 GIC DC electrical characteristics

This table provides the DC electrical characteristics for GIC pins operating at DV_{DD} = 3.3 V.

Table 108. GIC DC electrical characteristics (DV_{DD} = 3.3 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x DV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x DV_{DD}	V	1
Input current (V_{IN} = 0 V or V_{IN}= DV_{DD})	I_{IN}	—	±50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (DV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the DV_{IN} symbol referenced in Table 4.
3. For recommended operating conditions, see Table 4.

This table provides the GIC DC electrical characteristics when LV_{DD} = 2.5 V.

Table 109. GIC DC electrical characteristics (LV_{DD} = 2.5 V)[4]

Parameters	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x LV_{DD}	—	V	1
Input low voltage	V_{IL}	—	0.2 x LV_{DD}	V	1
Input current (LV_{IN} = 0 or LV_{IN} = LV_{DD})	I_{IN}	—	±50	μA	2, 3
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	—	V	—
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	—	0.40	V	—

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in Table 4.
3. The symbol LV_{DD}, in this case, represents the LV_{DD} symbols referenced in Table 4.
4. For recommended operating conditions, see Table 4.

This table provides the GIC DC electrical characteristics when $LV_{DD}/DV_{DD}/OV_{DD}$ = 1.8 V.

Table 110. GIC DC electrical characteristics (LV_{DD}/ DV_{DD}/ OV_{DD} = 1.8 V)[4]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x $L/D/OV_{DD}$	—	V	1
Input low voltage	V_{IL}	—	0.2 x L/DV_{DD}	V	1
Input low voltage	V_{IL}	—	0.3 x OV_{DD}	V	1
Input current ($L/D/OV_{IN}$ = 0 V or $L/D/OV_{IN}$ = $L/D/OV_{DD}$)	I_{IN}	—	±50	μA	2, 3
Output high voltage ($L/D/OV_{DD}$ = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	—	V	3
Output low voltage ($L/D/OV_{DD}$ = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	3

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max $L/D/OV_{IN}$ respective values found in Table 4.
2. The symbol $L/D/OV_{IN}$ represents the $L/D/OV_{IN}$ symbols referenced in Table 4.
3. The symbol $L/D/OV_{DD}$, in this case, represents the $L/D/OV_{DD}$ symbols referenced in Table 4.
4. For recommended operating conditions, see Table 4.

3.22.2 GIC AC timing specifications

This table provides the GIC input and output AC timing specifications.

Table 111. GIC input AC timing specifications[2]

Characteristic	Symbol	Min	Max	Unit	Notes
GIC inputs-minimum pulse width	t_{PIWID}	3	-	SYSCLKs	1

1. GIC inputs and outputs are asynchronous to any visible clock. GIC outputs must be synchronized before use by any external synchronous logic. GIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.
2. For recommended operating conditions, see Table 4.

3.23 High-speed serial interfaces (HSSI)

The chip features a Serializer/Deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, SGMII, and serial ATA (SATA) data transfers.

This section describes the most common portion of the SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also described.

3.23.1 Signal terms definitions

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n*_P and SD_TX*n*_N) or a receiver input (SD_RX*n*_P and SD_RX*n*_N). Each signal swings between A volts and B volts where A > B.

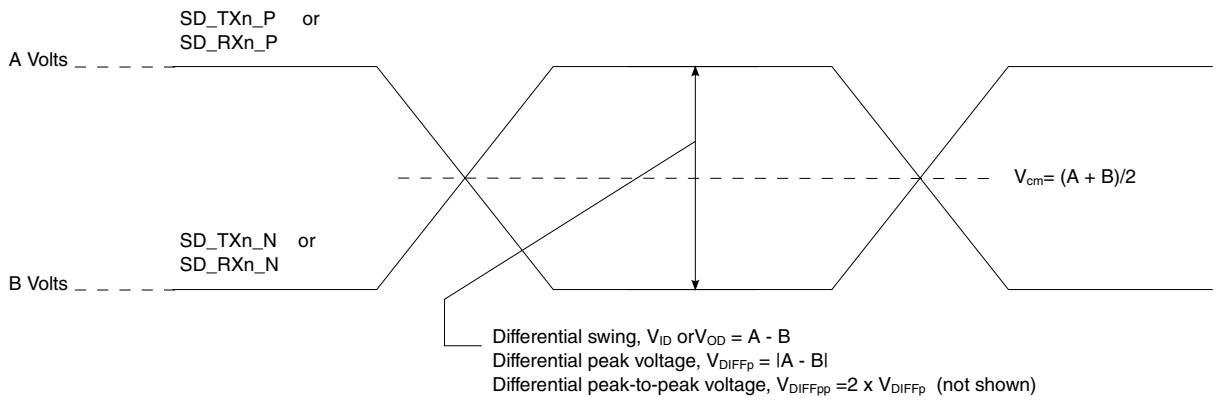


Figure 78. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as described in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing

The transmitter output signals and the receiver input signals SD_TX*n*_P, SD_TX*n*_N, SD_RX*n*_P and SD_RX*n*_N each have a peak-to-peak swing of A - B volts. This is also referred to as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing)

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complementary output voltages: $V_{SD_TXn_}$P - $V_{SD_TXn_N.}$ The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing)

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complementary input voltages: $V_{SD_RXn_P}$- $V_{SD_RXn_N}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_N, for example) from the non-inverting signal (SD_TX*n*_P, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 83 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SD_TXn_P} + V_{SD_TXn_N}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complementary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

3.23.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal phase-locked loop (PLL) whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD*n*_REF_CLK[1:2]_P and SD*n*_REF_CLK[1:2]_N.

SerDes may be used for various combinations of the following IP block based on the RCW Configuration field SRDS_PRTCLn:

- SGMII (1.25 Gbit/s or 3.125 Gbit/s), QSGMII (5 Gbit/s)
- XFI (10 Gbit/s)
- PCIe (2.5 Gbit/s, 5 Gbit/s, and 8 Gbit/s)
- SATA (1.5 Gbit/s, 3.0 Gbit/s, and 6.0 Gbit/s)

The following sections describe the SerDes reference clock requirements and provide application information.

3.23.2.1 SerDes spread-spectrum clock source recommendations

SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N are designed to work with spread-spectrum clocking for the PCI Express protocol only with the spreading specification defined in Table 112. When using spread-spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

The SerDes transmitter does not support spread-spectrum clocking for the SATA protocol. The SerDes receiver does support spread-spectrum clocking on receive, which means the SerDes receiver can receive data correctly from a SATA serial link partner using spread-spectrum clocking.

Spread-spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread-spectrum-supported protocols. For example, if spread-spectrum clocking is desired on a SerDes reference clock for the PCI Express protocol and the same reference clock is used for any other protocol, such as SATA or SGMII because of the SerDes lane usage mapping option, spread-spectrum clocking cannot be used at all.

This table provides the source recommendations for SerDes spread-spectrum clocking.

Table 112. SerDes spread-spectrum clock source recommendations [1]

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	—
Frequency spread	+0	-0.5	%	2

Notes:

1. At recommended operating conditions. See Table 4.

Table 112. SerDes spread-spectrum clock source recommendations [1]

Parameter	Min	Max	Unit	Notes
2. Only down-spreading is allowed.				

3.23.2.2 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

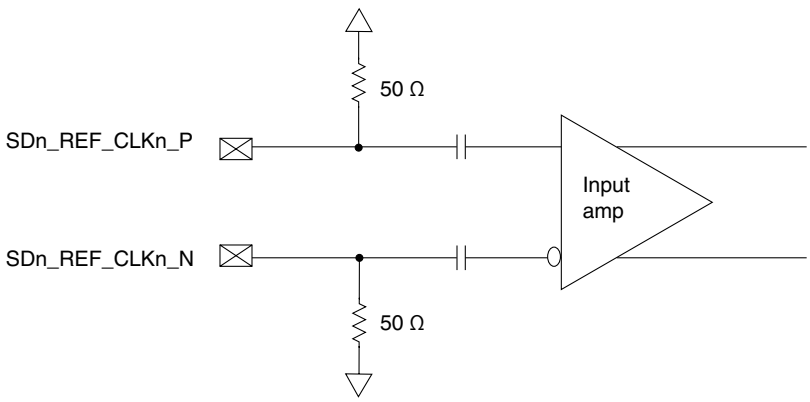


Figure 79. Receiver of SerDes reference clocks

The characteristics of the clock signals are as follows:

- The SerDes receiver's core power supply voltage requirements ($SV_{DD}n$) are as specified in Table 4.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N are internally AC-coupled differential inputs as shown in Figure 79. Each differential clock input (SD*n*_REF_CLK*n*_P or SD*n*_REF_CLK*n*_N) has on-chip 50-Ω termination to SGND*n* followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions in Signal terms definitions for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.

- This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND*n*. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
- If the device driving the SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N inputs cannot drive 50 Ω to SGND*n* DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.

- The input amplitude requirement is described in detail in the following sections.

3.23.2.3 DC-level requirements for SerDes reference clocks

The DC-level requirements for the SerDes reference clock inputs are different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, as described in Figure 79, the maximum average current requirements set the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV.
  - This figure shows the SerDes reference clock input requirement for a DC-coupled connection scheme.

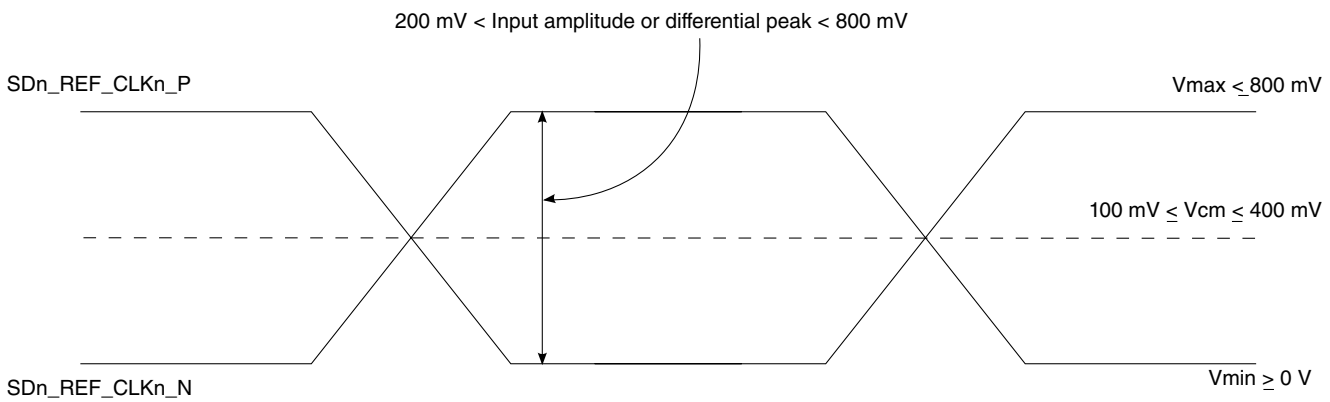


Figure 80. Differential reference clock input DC requirements (external DC-coupled)

  - For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver

operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND*n*. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND*n*).

- This figure shows the SerDes reference clock input requirement for an AC-coupled connection scheme.

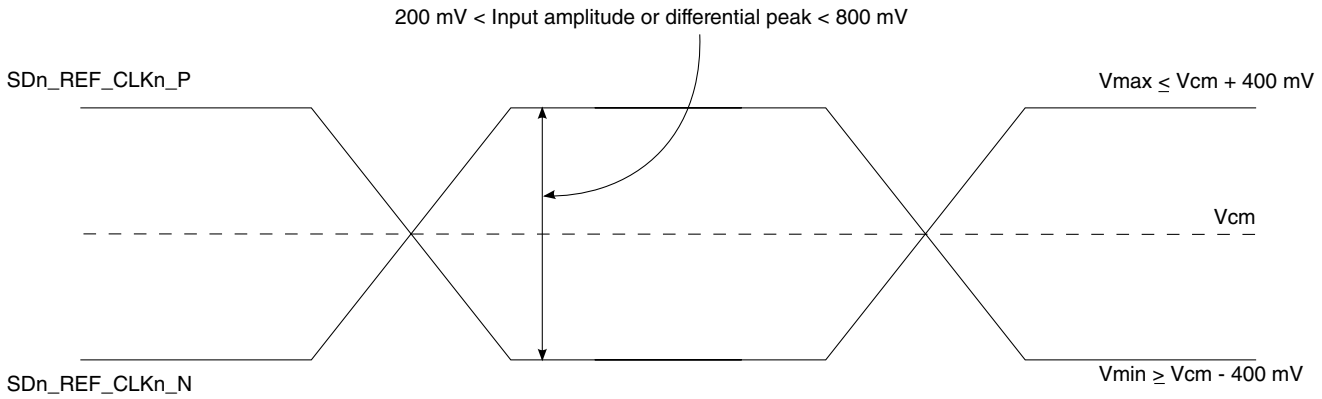


Figure 81. Differential reference clock input DC requirements (external AC-coupled)

- Single-ended mode
  - The reference clock can also be single-ended. The SD*n*_REF_CLK*n*_P input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to-peak (from V_{MIN} to V_{MAX}) with SD*n*_REF_CLK*n*_N either left unconnected or tied to ground.
  - To meet the input amplitude requirement, the reference clock inputs may need to be externally DC- or AC-coupled. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD*n*_REF_CLK*n*_N) through the same source impedance as the clock input (SD*n*_REF_CLK*n*_P) in use.
  - The SD*n*_REF_CLK*n*_P input average voltage must be between 200 and 400 mV.
  - This figure shows the SerDes reference clock input requirement for single-ended signaling mode.

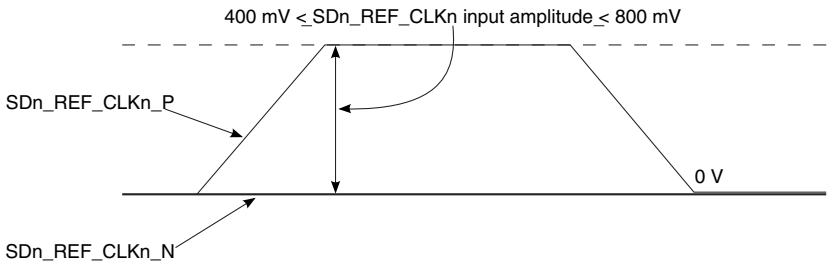


Figure 82. Single-ended reference clock input DC requirements

3.23.2.4 AC requirements for SerDes reference clocks

This table provides the AC requirements for SerDes reference clocks for PCI Express protocols running at data rates up to 5 Gbit/s.

This includes PCI Express (2.5 GT/s and 5 GT/s), SGMII (1.25 Gbit/s), and SATA (1.5 Gbit/s, 3.0 Gbit/s, and 6.0 Gbit/s). SerDes reference clocks need to be verified by the customer's application design.

Table 113. SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N input clock requirements [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N frequency range	t_{CLK_REF}	—	100/125/156.25	—	MHz	2
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N clock frequency tolerance	t_{CLK_TOL}	-300	—	300	ppm	3
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N clock frequency tolerance	t_{CLK_TOL}	-100	—	100	ppm	4
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	6
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N 10 kHz to 1.5 MHz RMS jitter	$t_{REFCLK\text{-}LF\text{-}RMS}$	—	—	3	ps RMS	7
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N > 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK\text{-}HF\text{-}RMS}$	—	—	3.1	ps RMS	7
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N RMS reference clock jitter	$t_{REFCLK\text{-}RMS\text{-}DC}$	—	—	1	ps RMS	8
SD*n*_REF_CLK*n*_P/ SD*n*_REF_CLK*n*_N rising/ falling edge rate	t_{CLKRR}/t_{CLKFR}	0.6	—	4	V/ns	9
Differential input high voltage	V_{IH}	150	—	—	mV	5
Differential input low voltage	V_{IL}	—	—	-150	mV	5
Rising edge rate (SD*n*_REF_CLK*n*_P) to falling edge rate (SD*n*_REF_CLK*n*_N) matching	Rise-Fall Matching	—	—	20	%	10, 11

Notes:

1. For recommended operating conditions, see Table 4.
2. **Caution:** Only 100 and 125 have been tested. In-between values do not work correctly with the rest of the system.
3. For PCI Express (2.5, 5 and 8 GT/s).
4. For SGMII, 2.5GSGMII and QSGMII.
5. Measurement taken from differential waveform.
6. Limits from PCI Express CEM Rev 2.0.
7. For PCI Express 5 GT/s, per PCI Express base specification Rev 3.0.

Table 113. SD*n*_REF_CLK*n*_P and SD*n*_REF_CLK*n*_N input clock requirements [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
8. For PCI-Express-8 GT/s, per PCI-Express base specification rev 3.0 9. Measured from -150 mV to +150 mV on the differential waveform (derived from SD*n*_REF_CLK*n*_P minus SD*n*_REF_CLK*n*_N). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 83. 10. Measurement taken from single-ended waveform. 11. Matching applies to rising edge for SD*n*_REF_CLK*n*_P and falling edge rate for SD*n*_REF_CLK*n*_N. It is measured using ±75 mV window centered on the median cross point where SD*n*_REF_CLK*n*_P rising meets SD*n*_REF_CLK*n*_N falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK*n*_P must be compared to the fall edge rate of SD*n*_REF_CLK*n*_N, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 84.						

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates greater than 8 GBaud.

This includes XFI (10.3125 GBaud), SerDes reference clocks to be guaranteed by the customer's application design.

Table 114. SD1_REF_CLKn_P/ SD1_REF_CLKn_N input clock requirements [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD1_REF_CLKn_P/ SD1_REF_CLKn_N frequency range	t_{CLK_REF}	-	156.25	-	MHz	2
SD1_REF_CLKn_P/ SD1_REF_CLKn_N clock frequency tolerance	t_{CLK_TOL}	-100	-	100	ppm	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	3
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@1 kHz	-	-	-85	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@10 kHz	-	-	-108	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@100 kHz	-	-	-128	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@1 MHz	-	-	-138	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N single side band noise	@10MHz	-	-	-138	dBC/Hz	4
SD1_REF_CLKn_P/ SD1_REF_CLKn_N random jitter (1.2 MHz to 15 MHz)	t_{CLK_RJ}	-	-	0.8	ps	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N total reference clock jitter at 10^{-12} BER (1.2 MHz to 15 MHz)	t_{CLK_TJ}	-	-	11	ps	-
SD1_REF_CLKn_P/ SD1_REF_CLKn_N spurious noise (1.2 MHz to 15 MHz)	-	-	-	-75	dBC	-
Notes: 1. For recommended operating conditions, see Table 4. 2. **Caution:** Only 156.25 have been tested. In-between values do not work correctly with the rest of the system.						

Table 114. SD1_REF_CLKn_P/ SD1_REF_CLKn_N input clock requirements [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
3. Measurement taken from differential waveform.						
4. Per XFP Spec. Rev 4.5, the Module Jitter Generation spec at XFI Optical Output is 10mUI (RMS) and 100 mUI (p-p). In the CDR mode the host is contributing 7 mUI (RMS) and 50 mUI (p-p) jitter.						

This figure shows the differential measurement points for rise and fall time.

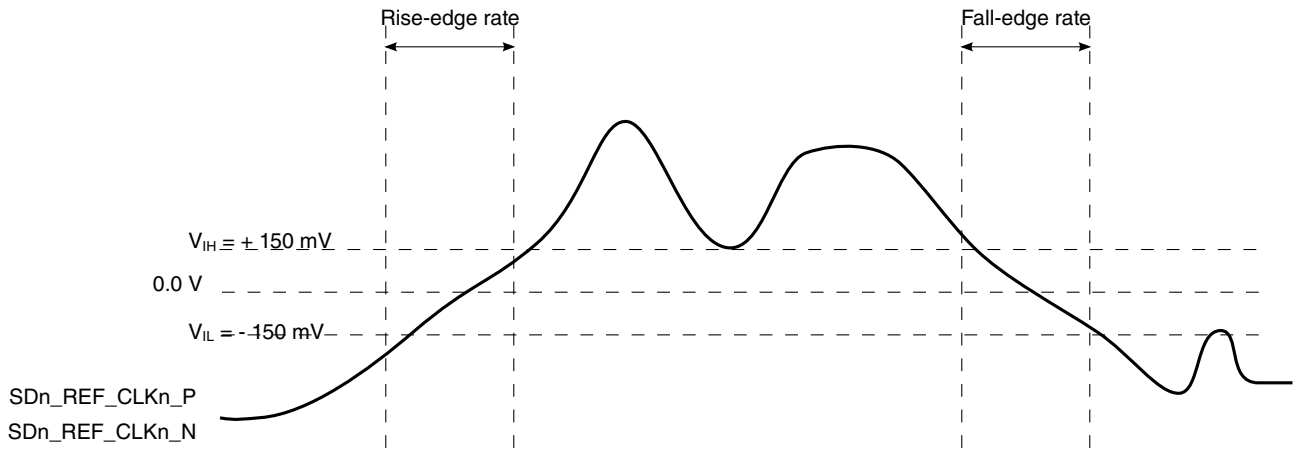


Figure 83. Differential measurement points for rise and fall time

This figure shows the single-ended measurement points for rise and fall time matching.

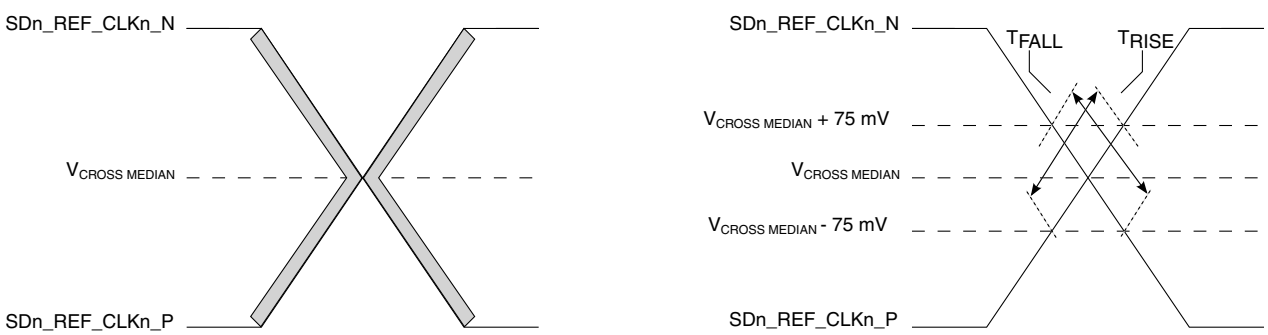


Figure 84. Single-ended measurement points for rise and fall time matching

3.23.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

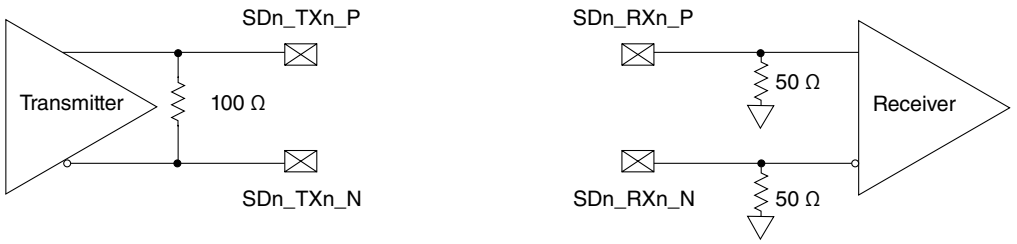


Figure 85. SerDes transmitter and receiver reference circuits

The DC and AC specifications of the SerDes data lanes are defined in each interface protocol section below based on the application usage:

- PCI Express
- Serial ATA (SATA) interface
- SGMII interface
- XFI interface

Note that an external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.23.4 PCI Express

This section describes the clocking dependencies, as well as the DC and AC electrical specifications for the PCI Express bus.

3.23.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 ppm of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

The platform clock frequency must be greater than or equal to 400 MHz for PCI Express Gen2. For more details, see Minimum platform frequency requirements for high-speed interfaces.

3.23.4.2 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

3.23.4.2.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 115. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Transmitter DC differential mode low Impedance
Transmitter DC impedance	$Z_{TX\text{-}DC}$	40	50	60	Ω	Required transmitter D+ as well as D- DC Impedance during all states

Notes:

1. For recommended operating conditions, see Table 4.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 116. PCI Express 2.0 (5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$
Low-power differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p_low}$	400	500	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	$Z_{TX\text{-}DC}$	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:

1. For recommended operating conditions, see Table 4.

This table defines the PCI Express 3.0 (8 GT/s) DC characteristics for the differential output at all transmitters. The parameters are specified at the component pins.

Table 117. PCI Express 3.0 (8 GT/s) differential transmitter output DC characteristics (XV_{DD} = 1.35 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Full swing transmitter voltage with no TX Eq	$V_{TX-FS-NO-EQ}$	800	—	1300	mVp-p	See Note 1.
Reduced swing transmitter voltage with no TX Eq	$V_{TX-RS-NO-EQ}$	400	—	1300	mV	See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	—
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	—
Minimum swing during EIEOS for full swing	$V_{TX-EIEOS-FS}$	250	—	—	mVp-p	See Note 2
Minimum swing during EIEOS for reduced swing	$V_{TX-EIEOS-RS}$	232	—	—	mVp-p	See Note 2
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:

1. Voltage measurements for $V_{TX-FS-NO-EQ}$ and $V_{TX-RS-NO-EQ}$ are made using the 64-zeroes/64-ones pattern in the compliance pattern.

2. Voltage limits comprehend both full swing and reduced swing modes. The transmitter must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX-FS-NO-EQ}$ measurement which represents the maximum peak voltage the transmitter can drive. The $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 mV_{P-P} at the receiver pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel.

3. For recommended operating conditions, see Table 4.

3.23.4.2.2 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 118. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications [4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX\text{-}DIFFp\text{-}p}$	120	1000	1200	mV	$V_{RX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	$Z_{RX\text{-}DC}$	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	65	-	175	mV	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.

2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.

4. For recommended operating conditions, see Table 4.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 119. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications [4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX\text{-}DIFFp\text{-}p}$	120	1000	1200	mV	$V_{RX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	$Z_{RX\text{-}DC}$	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$	65	-	175	mV	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$ Measured at the package pins of the receiver

Table continues on the next page...

Table 119. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications [4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes

Notes:

1. Measured at the package pins with a test load of 50 Ω to GND on each pin.

2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.

4. For recommended operating conditions, see Table 4.

This table defines the DC characteristics for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 120. PCI Express 3.0 (8 GT/s) differential receiver input DC characteristics [6]

Characteristic	Symbol	Min	Typ	Max	Units	Notes
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Generator launch voltage	$V_{RX-LAUNCH-8G}$	—	800	—	mV	Measured at TP1 per PCI Express base spec. rev 3.0
Eye height (-20dB Channel)	$V_{RX-SV-8G}$	25	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-12dB Channel)	$V_{RX-SV-8G}$	50	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-3dB Channel)	$V_{RX-SV-8G}$	200	—	—	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50 Ω to GND on each pin.

2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.

3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.

Table 120. PCI Express 3.0 (8 GT/s) differential receiver input DC characteristics [6]

Characteristic	Symbol	Min	Typ	Max	Units	Notes
4. $V_{RX-SV-8G}$ is tested at three different voltages to ensure the receiver device under test is capable of equalizing over a range of channel loss profiles. The "SV" in the parameter names refers to stressed voltage. 5. $V_{RX-SV-8G}$ is referenced to TP2P and is obtained after post processing data captured at TP2. 6. For recommended operating conditions, see Table 4.						

3.23.4.3 PCI Express AC physical layer specifications

This section describes the AC specifications for the physical layer of PCI Express on this device.

3.23.4.3.1 PCI Express AC physical layer transmitter specifications

This section describes the PCI Express AC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 121. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. Does not include spread-spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1 and 2.
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.
Notes:						

Table 121. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes

1. Specified at the measurement point into a timing and voltage test load as shown in Figure 87 and measured over any 250 consecutive transmitter UIs.

2. A $T_{TX\text{-}EYE}$ = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX\text{-}JITTER\text{-}MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

4. For recommended operating conditions, see Table 4.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 122. PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	$T_{TX\text{-}EYE}$	0.75	-	-	UI	The maximum transmitter jitter can be derived as: $T_{TX\text{-}MAX\text{-}JITTER}$ = 1 - $T_{TX\text{-}EYE}$ = 0.25 UI. See Note 1.
Transmitter deterministic jitter > 1.5 MHz	$T_{TX\text{-}HF\text{-}DJ\text{-}DD}$	-	-	0.15	UI	-
Transmitter RMS jitter < 1.5 MHz	$T_{TX\text{-}LF\text{-}RMS}$	-	3.0	-	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 2.

Notes:

1. Specified at the measurement point into a timing and voltage test load as shown in Figure 87 and measured over any 250 consecutive transmitter UIs.

2. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

3. For recommended operating conditions, see Table 4.

This table defines the PCI Express 3.0 (8 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 123. PCI Express 3.0 (8 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Transmitter uncorrelated total jitter	T_{TX-UTJ}	—	—	31.25	ps p-p	—
Transmitter uncorrelated deterministic jitter	$T_{TX-UDJ-DD}$	—	—	12	ps p-p	—
Total uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-TJ}$	—	—	24	ps p-p	See Note 1, 2
Deterministic data dependent jitter (DjDD) uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-DJDD}$	—	—	10	ps p-p	See Note 1, 2
Data dependent jitter	T_{TX-DDJ}	—	—	18	ps p-p	See Note 2
AC coupling capacitor	C_{TX}	176	—	265	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:

1. PWJ parameters shall be measured after data dependent jitter (DDJ) separation.
2. Measured with optimized preset value after de-embedding to transmitter pin.
3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
4. For recommended operating conditions, see Table 4.

3.23.4.3.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 GT/s, 5 GT/s, and 8 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 124. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum receiver eye width	T_{RX-EYE}	0.4	-	-	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 1 and 2.

Table continues on the next page...

Table 124. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	-	-	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX\text{-}DIFFp\text{-}p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1, 2 and 3.

Notes:

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 87 must be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

2. A $T_{RX\text{-}EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

3. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

4. For recommended operating conditions, see Table 4.

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 125. PCI Express 2.0 (5 GT/s) differential receiver input AC specifications[1]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Max receiver inherent timing error	$T_{RX\text{-}TJ\text{-}CC}$	-	-	0.4	UI	The maximum inherent total timing error for common RefClk receiver architecture
Max receiver inherent deterministic timing error	$T_{RX\text{-}DJ\text{-}DD\text{-}CC}$	-	-	0.30	UI	The maximum inherent deterministic timing error for common RefClk receiver architecture

Note:

1. For recommended operating conditions, see Table 4.

This table defines the AC specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 126. PCI Express 3.0 (8 GT/s) differential receiver input AC specifications[5]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations. See Note 1.
Eye Width at TP2P	$T_{RX-SV-8G}$	0.3	—	0.35	UI	See Note 1
Differential mode interference	$V_{RX-SV-DIFF-8G}$	14	—	—	mV	Frequency = 2.1GHz. See Note 2.
Sinusoidal Jitter at 100 MHz	$T_{RX-SV-SJ-8G}$	—	—	0.1	UI p-p	Fixed at 100 MHz. See Note 3.
Random Jitter	$T_{RX-SV-RJ-8G}$	—	—	2.0	ps RMS	Random jitter spectrally flat before filtering. See Note 4.

Note:

1. $T_{RX-SV-8G}$ is referenced to TP2P and obtained after post processing data captured at TP2. $T_{RX-SV-8G}$ includes the effects of applying the behavioral receiver model and receiver behavioral equalization.

2. $V_{RX-SV-DIFF-8G}$ voltage may need to be adjusted over a wide range for the different loss calibration channels.

3. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency as shown in Figure 86.

4. Random jitter (Rj) is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. See Figure 86 for details. Rj may be adjusted to meet the 0.3 UI value for $T_{RX-SV-8G}$.

5. For recommended operating conditions, see Table 4.

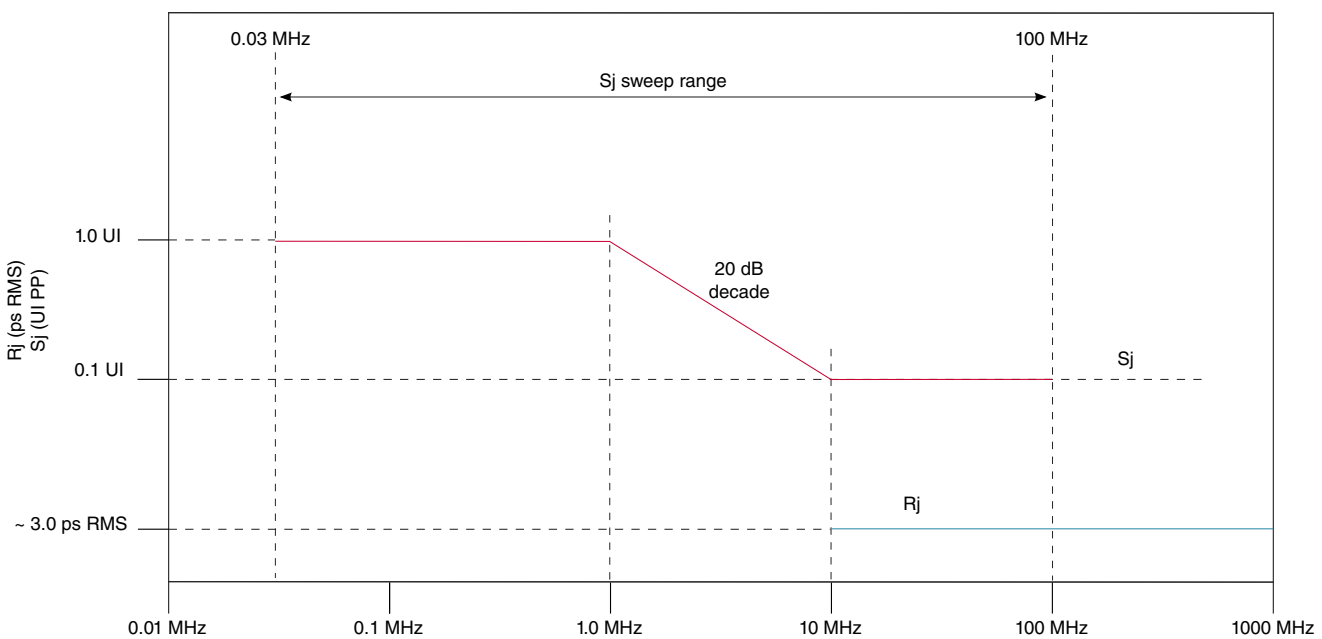


Figure 86. Swept sinusoidal jitter mask

3.23.4.4 Test and measurement load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D- package pins.

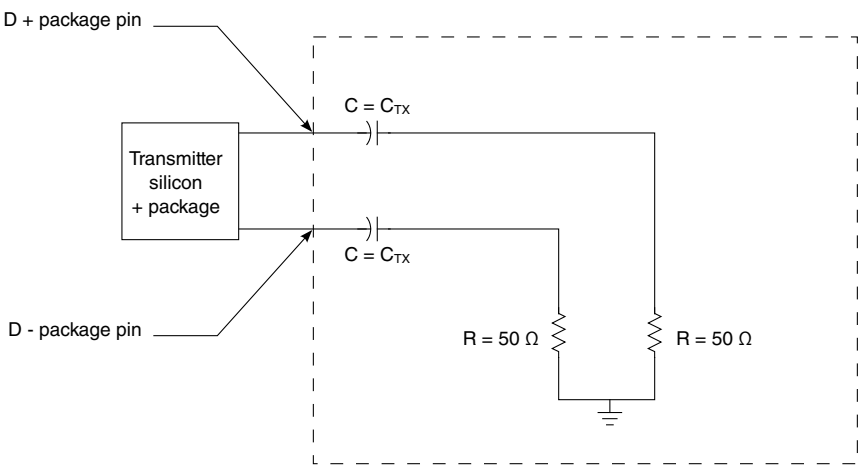


Figure 87. Test and measurement load

3.23.5 Serial ATA (SATA) interface

This section describes the DC and AC electrical specifications for the SATA interface.

3.23.5.1 SATA DC electrical characteristics

This section describes the DC electrical characteristics for SATA.

3.23.5.1.1 SATA DC transmitter output characteristics

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen1i/1m or 1.5 Gbit/s transmission.

Table 127. Gen1i/1m 1.5 G transmitter DC specifications (XV_{DD} = 1.35 V)[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Tx differential output voltage	V_{SATA_TXDIFF}	400	500	600	mV p-p	1
Tx differential pair impedance	$Z_{SATA_TXDIFFIM}$	85	100	115	Ω	2

Notes:

1. Terminated by 50 Ω load.
2. DC impedance.
3. For recommended operating conditions, see Table 4.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbit/s transmission.

Table 128. Gen 2i/2m 3 G transmitter DC specifications (XV_{DD} = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	400	—	700	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA_TXDIFFIM}$	85	100	115	Ω	—

Notes:

1. Terminated by 50 Ω load.
2. For recommended operating conditions, see Table 4.

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen 3i transmission.

Table 129. Gen 3i transmitter DC specifications (XV_{DD} = 1.35 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	240	—	900	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA_TXDIFFIM}$	85	100	115	Ω	—

Notes:

1. Terminated by 50 Ω load.
2. For recommended operating conditions, see Table 4.

3.23.5.1.2 SATA DC receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbit/s differential receiver input DC characteristics for the SATA interface.

Table 130. Gen1i/1m 1.5 G receiver input DC specifications [3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	500	600	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	50	120	240	mV p-p	—

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 4.

This table provides the Gen2i/2m or 3 Gbit/s differential receiver input DC characteristics for the SATA interface.

Table 131. Gen2i/2m 3 G receiver input DC specifications [3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	—	750	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	240	mV p-p	2

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 4.

This table provides the Gen 3i differential receiver input DC characteristics for the SATA interface.

Table 132. Gen 3i receiver input DC specifications [3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	—	1000	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	—	75	120	200	mV p-p	—

Notes:

1. Voltage relative to common of either signal comprising a differential pair.
2. DC impedance.
3. For recommended operating conditions, see Table 4.

3.23.5.2 SATA AC timing specifications

This section describes the SATA AC timing specifications.

3.23.5.2.1 AC requirements for SATA REF_CLK

This table provides the AC requirements for the SATA reference clock. These requirements must be guaranteed by the customer's application design.

Table 133. SATA reference clock input requirements[6]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N clock frequency tolerance	t_{CLK_TOL}	-350	—	+350	ppm	—
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N cycle-to-cycle clock jitter (period jitter)	t_{CLK_CJ}	—	—	100	ps	2
SD*n*_REF_CLK1_P/SD*n*_REF_CLK1_N total reference clock jitter, phase jitter (peak-to-peak)	t_{CLK_PJ}	-50	—	+50	ps	2, 3, 4

Notes:

1. **Caution:** Only 100 and 125 MHz have been tested. In-between values do not work correctly with the rest of the system.
2. At RefClk input.
3. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}.
4. Total peak-to-peak deterministic jitter must be less than or equal to 50 ps.
5. Measurement taken from differential waveform.
6. For recommended operating conditions, see Table 4.

3.23.5.2.2 AC transmitter output characteristics

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 1i/1m or 1.5 Gbit/s transmission. The AC timing specifications do not include RefClk jitter.

Table 134. Gen 1i/1m 1.5 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	—	1.5	—	Gbit/s	—
Unit interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA_TXTJ5UI}$	—	—	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA_TXTJ250UI}$	—	—	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA_TXDJ5UI}$	—	—	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA_TXDJ250UI}$	—	—	0.22	UI p-p	1

Notes:

1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.
2. For recommended operating conditions, see Table 4.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 2i/2m or 3.0 Gbit/s transmission. The AC timing specifications do not include RefClk jitter.

Table 135. Gen 2i/2m 3 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	—	3.0	—	Gbit/s	—
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_TXTJfB/500}$	—	—	0.37	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_TXTJfB/1667}$	—	—	0.55	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_TXDJfB/500}$	—	—	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Notes:

1. Measured at transmitter output pins peak-to-peak phase variation; random data pattern.
2. For recommended operating conditions, see Table 4.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen 3i transmission. The AC timing specifications do not include RefClk jitter.

Table 136. Gen 3i transmitter AC specifications [1]

Parameter	Symbol	Min	Typ	Max	Units
Speed	—	—	6.0	—	Gbit/s
Total jitter before and after compliance interconnect channel	J_T	—	—	0.52	UI p-p
Random jitter before compliance interconnect channel	J_R	—	—	0.18	UI p-p
Unit interval	UI	166.6083	166.6667	167.5583	ps

Notes:

1. For recommended operating conditions, see Table 4.

3.23.5.2.3 AC differential receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbit/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 137. Gen 1i/1m 1.5 G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—

Table continues on the next page...

Table 137. Gen 1i/1m 1.5 G receiver AC specifications[2] (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Total jitter data-data 5 UI	$U_{SATA_RXTJ5UI}$	—	—	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA_RXTJ250UI}$	—	—	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA_RXDJ5UI}$	—	—	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA_RXDJ250UI}$	—	—	0.35	UI p-p	1

Notes:

1. Measured at the receiver.
2. For recommended operating conditions, see Table 4.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbit/s transmission. The AC timing specifications do not include RefClk jitter.

Table 138. Gen 2i/2m 3 G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_RXTJfB/500}$	—	—	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_RXTJfB/1667}$	—	—	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA_RXDJfB/500}$	—	—	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA_RXDJfB/1667}$	—	—	0.35	UI p-p	1

Notes:

1. Measured at the receiver.
2. For recommended operating conditions, see Table 4.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen 3i transmission. The AC timing specifications do not include RefClk jitter.

Table 139. Gen 3i receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Total jitter after compliance interconnect channel	J_T	—	—	0.60	UI p-p	1
Random jitter before compliance interconnect channel	J_R	—	—	0.18	UI p-p	1
Unit interval: 6.0 Gb/s	UI	166.6083	166.6667	167.5583	ps	—

Notes:

1. Measured at the receiver.
2. The AC specifications do not include RefClk jitter.

4 Security fuse processor

This chip implements the QorIQ platform's trust architecture, supporting capabilities such as secure boot. Use of the trust architecture feature is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the trust architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.8 V to the TA_PROG_SFP pin per Power sequencing. TA_PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of six fuse programming cycles. All other times, TA_PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering TA_PROG_SFP are shown in Figure 9. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 4.

NOTE

Users not implementing the QorIQ platform's trust architecture features should connect TA_PROG_SFP to GND.

5 Hardware design considerations

5.1 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and integrated flash controller.

Table 140. Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency								Unit	Notes
	1200 MHz		1400 MHz		1600 MHz		1800 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
Core cluster group PLL frequency	1000	1200	1000	1400	1000	1600	1000	1800	MHz	1, 2
Platform clock frequency	400	400	400	600	400	700	400	700	MHz	1, 3
Memory Bus Clock Frequency (DDR4)	650	800	650	1050	650	1050	650	1050	MHz	1, 4, 5
IFC clock frequency	-	100	-	100	-	100	-	100	MHz	
FMan	400	600	400	600	400	800	400	800	MHz	

Table continues on the next page...

Table 140. Processor, platform, and memory clocking specifications (continued)

Characteristic	Maximum processor core frequency								Unit	Notes
	1200 MHz		1400 MHz		1600 MHz		1800 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		

1. **Caution:**The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR4 data rate. The DDR4 memory bus clock frequency is limited to min = 650 MHz.
3. The memory bus clock speed is dictated by its own PLL.
4. The integrated flash controller (IFC) clock speed on IFC_CLK[0:1] is determined by the IFC module input clock (platform clock / 2) divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information.
5. The minimum platform frequency should meet the requirements in Minimum platform frequency requirements for high-speed interfaces.
6. For supported voltage/frequency options, see the orderable part list of QorIQ LS1046A and LS1026A Multicore Communications Processors at www.nxp.com.

5.1.1 DDR clock ranges

The DDR memory controller can run only in asynchronous mode, where the memory bus is clocked with the clock provided on the DDRCLK input pin, which has its own dedicated PLL.

This table provides the clocking specifications for the memory bus.

Table 141. Memory bus clocking specifications

Characteristic	Min Freq.(MHz)	Max Freq.(MHz)	Min Data Rate (MT/s)	Max Data Rate (MT/s)	Notes
Memory bus clock frequency and data rate for DDR4	650	1050	1300	2100	1, 2, 3

Notes:

1. **Caution:** The platform clock to SYSCLK ratio, core to SYSCLK ratio and DDR to SYSCLK (or DDRCLK) ratio settings must be chosen such that the resulting platform frequency, core frequency and DDRCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock refers to the chip's memory controllers' Dn_MCK[0:1] and Dn_MCK[0:1] output clocks, running at half of the DDR data rate.
3. The memory bus clock speed is dictated by its own PLL.
4. For supported voltage/frequency options, see the orderable part list of QorIQ LS1046A and LS1026A Multicore Communications Processors at www.nxp.com.

5.2 Minimum platform frequency requirements for high-speed interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below. For proper PCI Express operation, the platform clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{16}$$

Figure 88. Gen 1 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 89. Gen 2 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{4}$$

Figure 90. Gen 3 PEX minimum platform frequency

See section "Link Width," in the chip reference manual for PCI Express interface width details. Note that "PCI Express link width" in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection. It refers to the widest port in use, not the combined width of the number ports in use.

5.3 Minimum DPAA frequency requirements

The minimum DPAA frequency of 533 MHz is required for 10 G operations.

6 Thermal

This table shows the thermal characteristics for the chip. Note that these numbers are based on design estimates and are preliminary.

Table 142. Package thermal characteristics

Rating	Board	Symbol	Value	Unit	Notes
Junction-to-ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	25.18	°C/W	1
Junction-to-ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	14.35	°C/W	1

Table continues on the next page...

Table 142. Package thermal characteristics (continued)

Rating	Board	Symbol	Value	Unit	Notes
Junction-to-ambient, moving air (1 m/s)	Single-layer board (1s)	$R_{\Theta JMA}$	15.47	°C/W	1
Junction-to-ambient, moving air (1 m/s)	Four-layer board (2s2p)	$R_{\Theta JMA}$	9.35	°C/W	1
Junction-to-board	-	$R_{\Theta JB}$	4.66	°C/W	2
Junction-to-case (top)	-	$R_{\Theta JC}$	0.71	°C/W	3
Junction-to-lid top	-	$R_{\Theta JLT}$	0.36	°C/W	4

1. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-2A and JESD51-6 (moving air). Thermal test board meets JEDEC specification for this package (JESD51-9).

2. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4. Junction-to-lid-top thermal resistance is determined using the MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance layer between the package and cold plate.

5. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a specific standardized environment. It is not meant to predict the performance of a package in an application-specific environment

Table 143. Thermal resistance with heat sink in open flow

Heat sink with thermal grease	Air flow	Thermal resistance (°C/W)
Wakefield 53 x 53 x 25 mm Pin Fin	Natural Convection	6.5
Wk698	0.5 m/s	4.0
	1 m/s	2.9
	2 m/s	2.4
	4 m/s	2.1
Aavid 35x31x23 mm Pin Fin	Natural Convection	8.8
av10563	0.5 m/s	5.3
	1 m/s	4.2
	2 m/s	3.9
	4 m/s	3.3
Aavid 30x30x9.4 mm Pin Fin	Natural Convection	12.5
Av 3358	0.5 m/s	8.9
	1 m/s	6.7
	2 m/s	5.1
	4 m/s	4.1
Aavid 43x41x16.5 mm Pin Fin	Natural Convection	9.0
Av 2332	0.5 m/s	5.8
	1 m/s	4.3
	2 m/s	3.2
	4 m/s	2.7

Table continues on the next page...

Table 143. Thermal resistance with heat sink in open flow (continued)

1. Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board.
2. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease.
3. See Thermal management information, for additional details.

6.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

6.2 Temperature diode

The chip has temperature diodes that can be used to monitor its temperature by using some external temperature monitoring devices (such as ADT7481A™).

The following are the specifications of the chip temperature diodes:

- Operating range: 10 - 230 µA
- Ideality factor over temperature range 85°C - 105°C, n = 1.006 ± 0.003, with approximate error ± 1°C and error under ± 3°C for temperature range 0°C - 85°C.

6.3 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 91. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 15 pounds force (65 N).

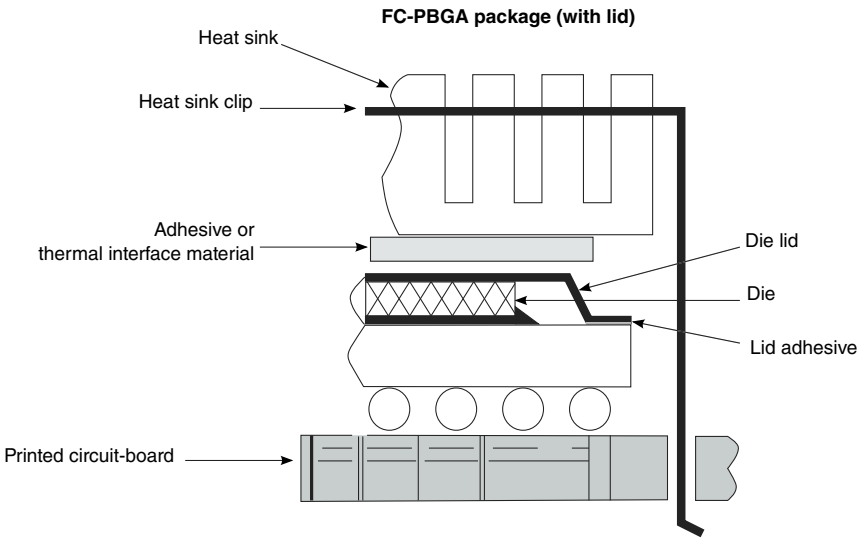


Figure 91. Package exploded, cross-sectional view-FC-PBGA

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

6.3.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lid-top thermal resistance
- The die junction-to-board thermal resistance

This figure shows the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

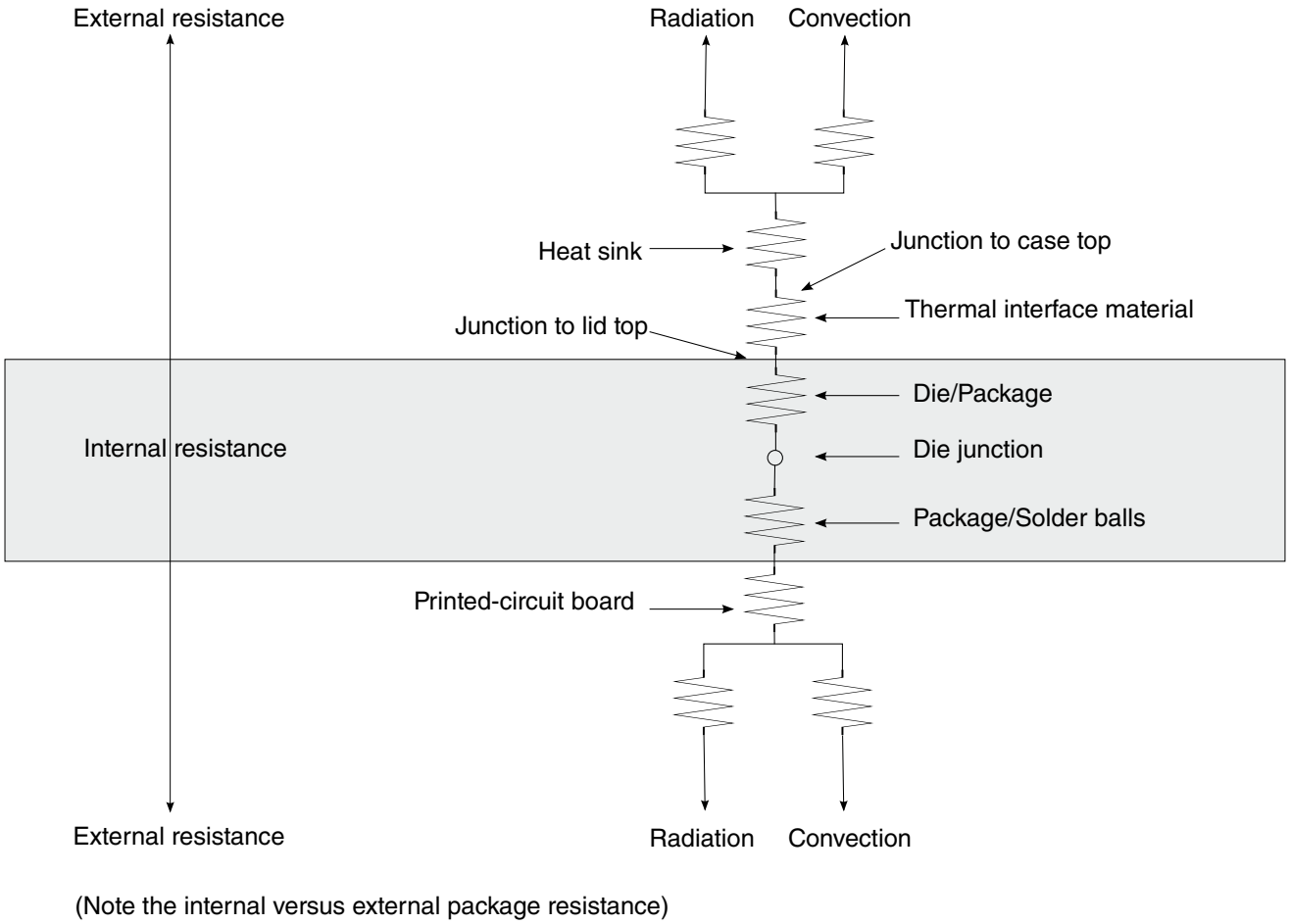


Figure 92. Package with heat sink mounted to a printed-circuit board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

6.3.2 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 91).

The system board designer can choose among several types of commercially available thermal interface materials.

7 Package information

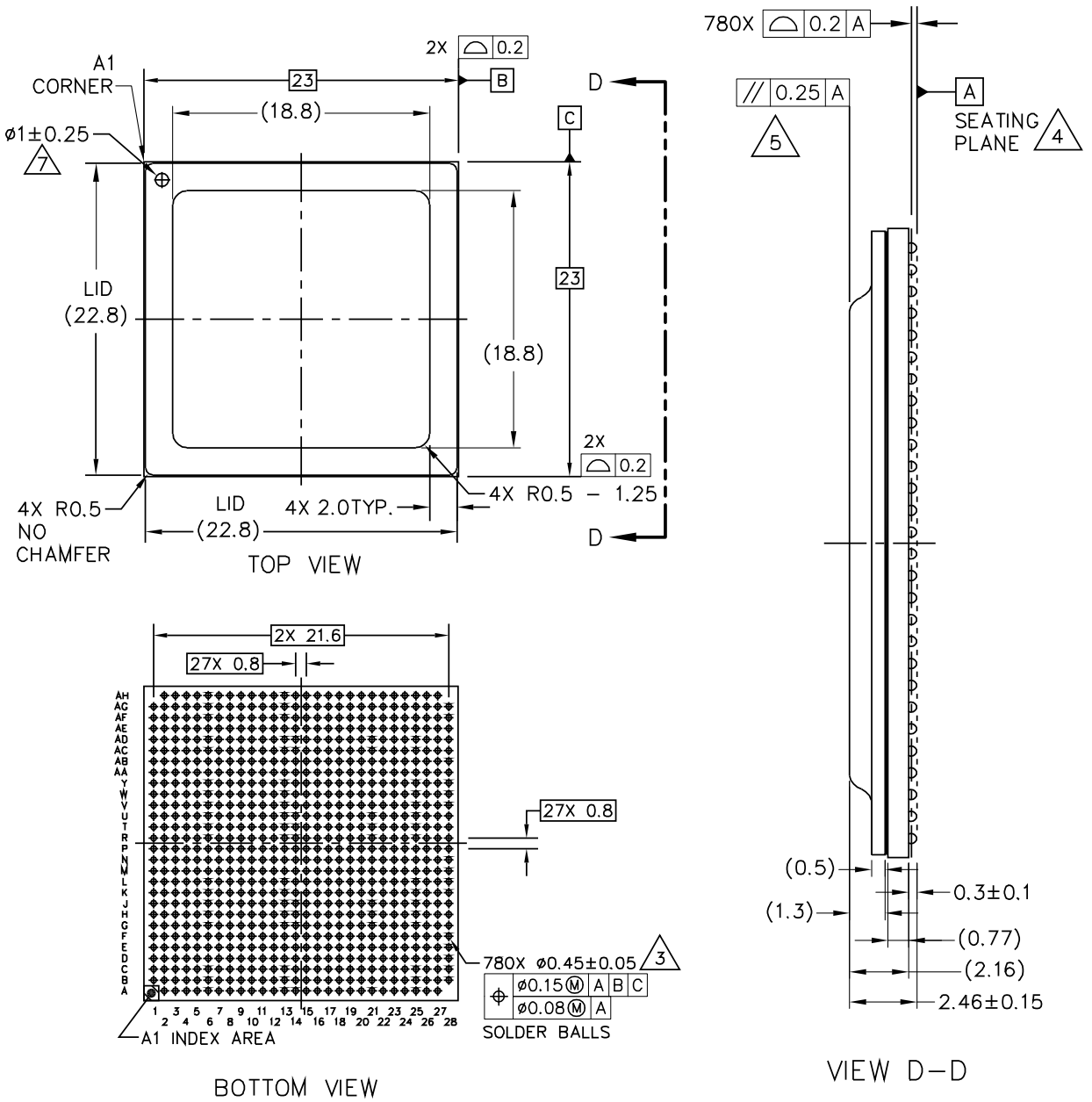
7.1 Package parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 23 mm x 23 mm, 780 flip-chip, plastic-ball, grid array.

- Package outline - 23 mm x 23 mm
- Interconnects - 780
- Ball Pitch - 0.8 mm
- Ball Diameter (nominal) - 0.45 mm
- Ball Height (nominal) - 0.3 mm
- Solder Balls Composition - 96.5% Sn, 3% Ag, and 0.5% Cu
- Module height (typical) - 2.31 (minimum), 2.46 mm (typical), and 2.61 mm (maximum)

7.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.



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TITLE: FCPBGA, WITH LID, 23 X 23 X 2.46 PKG, 0.8 MM PITCH, 780 I/O	DOCUMENT NO: 98ASA00854D	REV: A
	STANDARD: NON–JEDEC	
	SOT1653–1	14 JAN 2016

Figure 93. Mechanical dimensions of the FC-PBGA

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.
7. Pin 1 thru hole shall be centered within foot area.
8. 23.2 mm maximum package assembly (lid + laminate) X and Y.

8 Ordering information

This table provides the NXP QorIQ platform part numbering nomenclature.

8.1 Part numbering nomenclature

This table provides the NXP QorIQ platform part numbering nomenclature.

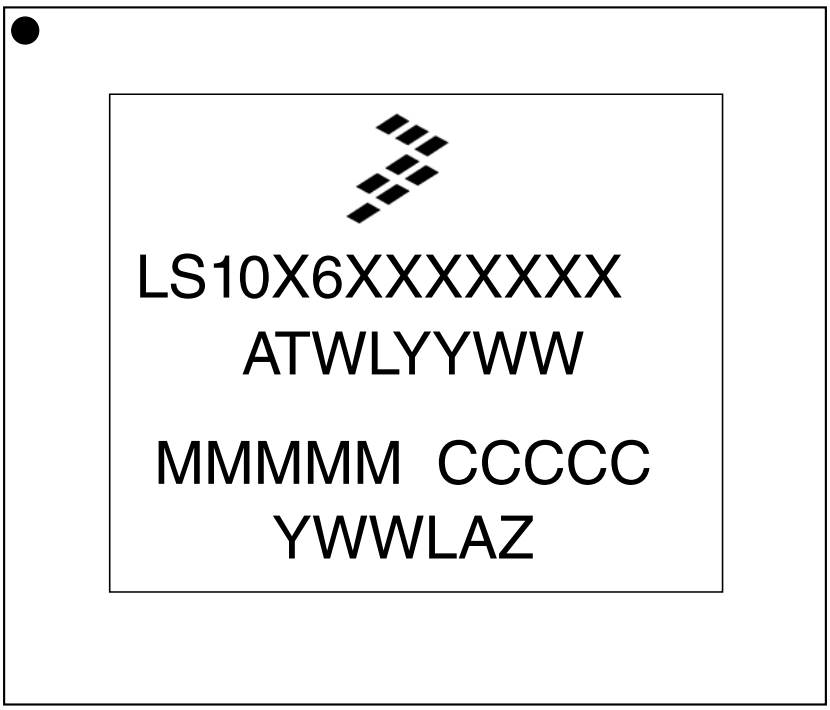
Table 144. Part numbering nomenclature

p	ls	n	nn	n	x	t	e	n	c	d	r
Qual status	**Generation**	**Performance Level**	**Number of Virtual cores**	**Unique ID**	**Core Type**	**Temperature Range**	**Encryption**	**Package Type**	**CPU Speed[1,2]**	**DDR Data Rate**	**Die Revision**
P="Pre-qual" Blank="Qualified"	LS = Layerscape	1	04 = Four Cores 02 = Two Cores	6	A = Arm	S = Standard (0 - 105^{0}C) X = Extended (-40 - 105^{0}C)	E = Encryption N = Non-Encryption	8 = LCFC 780 balls	M = 1200 MHz P = 1400 MHz Q = 1600 MHz T = 1800 MHz	Q = 1600 MHz 1 = 2100 MHz	A = Rev 1.0

1. For the LS1046A family of devices, parts marked with "M" require 0.9 V operating voltage.
2. For the LS1046A family of devices, only parts marked with "P", "Q", and "T" support extended temperature range.

8.2 Part marking

Parts are marked as in the example shown in this figure.



Legend:
LS10X6XXXXXXX is the orderable part number
ATWLYYWW is the test traceability code
MMMMM is the mask number
CCCCC is the country code
YWWLAZ is the assembly traceability code

Figure 94. Part marking for FC-PBGA chip LS1046A

9 Revision history

This table summarizes revisions to this document.

Table 145. Revision history

Revision	Date	Description

4	06/2020	• In Table 4
		  • Updated recommended value of USB_SV_{IN} from "0.3 to USB_SV_{DD}" to "GND to USB_SV_{DD}"
		  • Added note 10 for available temperature range for part numbers
		• Removed input signals from Table 5 as they are irrelevant for output drive capability
		• Removed typo "PORESET_B assertion" from step2 of secure boot fuse programming in Power sequencing
		• In Table 7 and Table 8
		  • Added note 9 regarding power numbers applicability
		  • Added power numbers for 1200MHz at 1.0V
		  • Added note 10 regarding power numbers applicability for 1200MHz at 1.0V
		• In Table 9
		  • Added column for Core Frequency = 1.2 GHz (VDD =1.0V)
		  • For PH20 mode, corrected "run to PH20 state" as "PW15 to PH20 state"
		  • For LPM20, corrected "PH20 to LPM20" as "PW15 to LPM20"
		• Added note 2 regarding extended temperature range in Table 144

3	07/2019	• Updated Figure 80

2	05/2019	• In Pinout list,
		  • added note 27, 28
		  • changed the note reference of "D1_MALERT_B" signal from 6 to 27
		  • changed the note reference of "HRESET_B" signal from 6 to 28
		  • Removed switchable from I2C/DUART and EVDD
		  • updated Warning
		• Removed section "General AC timing specifications"
		• Removed note 1 "Caution: The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequencies do not exceed their respective maximum or minimum operating frequencies." from Table 14
		• Removed note 1 and 2 from Table 16
		• Added Figure 11
		• Added notes 6 and 7 in Table 23
		• Added note 3 in Table 72
		• In Table 89,
		  • added a new column Notes
		  • updated "CS to SCK delay" and "After SCK delay" parameters
		  • removed "SCK cycle time" parameter
		• Updated section QSPI AC timing specifications
		• In section QSPI timing SDR mode,
		  • updated "CS output hold time" and "CS output delay" parameters in Table 91
		  • added a note below the table
		• Updated Figure 61
		• Updated section Temperature diode
		• Removed jitter specs of GTX_CLK125 from Table 18
		• Added note in Power sequencing

1	03/2018	• In Features, updated two to three for SGMII interfaces supporting 2500 Mbps • Updated Figure 92 • In Power sequencing, updated 10 ms to 95 ms in second bullet point • In Table 9, updated PW20 to PH20 and PCL10 to PH20 • In Table 10, updated X1VDD to XVDD and PROG_SFP to TA_PROG_SFP • Updated Figure 1 and Figure 2 to show 8 MACs • In Table 12, updated PROG_SFP to TA_PROG_SFP • Updated Real-time clock timing (RTC) • Updated rise/fall time spec to 0.75ns and removed 0.54ns from Table 18 and Table 52 • Removed Clock period jitter (peak to peak) row from Table 22 • Updated first row of Table 23

Table continues on the next page...

Table 145. Revision history (continued)

Revision	Date	Description
		• Removed table "PLL lock times" • Removed note reference 7 from Table 24 • In SGMII interface, updated XGNDn to GNDn • Updated note for USB_SDVDD for HS and USB_SVDD for SS in Table 2 • Updated eSDHC to SDHC and corrected signal name eSDHC_CMD/DAT0_DIR to SDHC_CMD_DIR/DAT0_DIR in Table 4 • Updated TA_BB_VDD power dissipation numbers in Table 11 • Added note 9 in Table 52 • Added rms clock jitter for PCIe- 8GT/s in Table 113 • Added notes to Table 38 and Table 42
0	02/2017	initial public release

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