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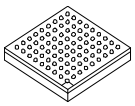
i.MX 8QuadMax 1.3GHz Automotive and Infotainment Applications Processors



Package Information
29 x 29 mm package case outline

Ordering Information
See Table 2 on page 5

1 Introduction

The i.MX 8 Family consists of two processors: i.MX 8QuadMax and 8QuadPlus. This data sheet covers the i.MX 8QuadMax processor, which is composed of eight cores (two Arm® Cortex®-A72, four Arm Cortex®-A53, and two Arm Cortex®-M4F), dual 32-bit GPU subsystems, 4K H.265 capable VPU, and dual failover-ready display controllers. This processor supports a single 4K display (with multiple display output options, including MIPI-DSI, HDMI, eDP/DP, and LVDS), or multiple smaller displays. Memory interfaces supporting LPDDR4, Quad SPI/Octal SPI (FlexSPI), eMMC 5.1, RAW NAND, SD 3.0, and a wide range of peripheral I/Os such as PCIe, provide wide flexibility. Advanced multicore audio processing is supported by the Arm cores and a high performance Tensilica® HiFi 4 DSP for pre- and post-audio processing as well as voice recognition.

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The i.MX 8QuadMax processor offers numerous advanced features as shown in this table.

Table 1. i.MX 8QuadMax advanced features

Function	Feature
Multicore architecture provides 4× Cortex-A53, 2× Cortex-A72 cores, and 2× Cortex-M4F cores	AArch64 for 64-bit support and new architectural features
	AArch32 for full backward compatibility with ARMv7
	Cortex-A72 and Cortex-A53 cores support ARM virtualization extensions. sMMU provides address virtualization to all subsystems.
	Cortex-M4F cores for real-time applications
Graphics Processing Unit (GPU)	16× Vec4 shaders with 64 execution units. Split GPU architecture allows for dual independent 8-Vec4 shader GPUs or a combined 16-Vec4 shader GPU.
	Supports OpenGL 3.0, 2.1,; OpenGL ES 3.2, 3.1 (with AEP), 3.0, 2.0, and 1.1; OpenCL 1.2 Full Profile and 1.1; OpenVG 1.1; and Vulkan
	High-performance 2D Blit Engine
Video Processing Unit (VPU)	H.265 decode (4Kp60)
	H.264 decode (4Kp30)
	WMV9/VC-1 imple decode
	MPEG 1 and 2 decode
	AVS decode
	MPEG4.2 ASP, H.263, Sorenson Spark decode
	Divx 3.11 including GMC decode
	ON2/Google VP6/VP8 decode
	RealVideo 8/9/10 decode
	JPEG and MJPEG decode
	2× H.264 encode (1080p30)
Tensilica HiFi 4 DSP for pre- and post-processing	666 MHz Fixed-point and vector-floating-point support 32 KB instruction cache, 48 KB data cache, 512 KB SRAM (448 KB of OCRAM and 64 KB of TCM)
Memory	64-bit LPDDR4 @1600 MHz
	1× Quad SPI which can be used to connect to an FPGA
	2× Quad SPI or 1× Octal SPI (FlexSPI) for fast boot from SPI NOR flash
	2× SD 3.0 card interfaces
	1× eMMC5.1/SD3.0
	RAW NAND (62-bit ECC support via BCH-62 module)

Table 1. i.MX 8QuadMax advanced features (continued)

Function	Feature
Display Controller	Supports single UltraHD 4Kp60 display or up to 4 independent FullHD 1080p60 displays
	Up to 18-layer composition
	Complementary 2D blitting engines and online warping functionality
	Integrated Failover Path (SafeAssure) to ensure display content stays valid even in event of a software failure
Display I/O	2× MIPI-DSI with 4 lanes each
	1× HDMI-TX/DisplayPort compliant with: • HDMI 1.4b and 2.0a • eDP 1.4 • DP 1.3
	This high performance serializer supports a pair of LVDS displays with 8 lanes each. Each port can be configured for 2x Tx with 4 lanes each.
Camera I/O and video	• 2× MIPI-CSI with 4-lanes each, MIPI DPHYSM v1.1 • 1× HDMI-RX (See restrictions in Section 4.10.8)
Security	Advanced High Assurance Boot (AHAB) secure & encrypted boot
	Random Number Generator with a high-quality entropy source generator and Hash_DRBG (based on hash functions)
	RSA up to 4096, Elliptic Curve up to 1023
	AES-128/192/256, DES, 3DES, MD5, SHA-1, SHA-224/256/384/512
	Dedicated Security Controller for Flashless SHE and HSM support, Trustzone
	Built-in ECDSA/DSA protocol support
	See the security reference manual for this chip for a full list of security features.

System Control	• 2× I^2C tightly coupled with Cortex-M4 cores (1× per Cortex M4F core)
	  • The tightly coupled M4 I^2C ports cannot be used for general-purpose use
	• System Control Unit (SCU):
	  • Power control, clocks, reset
	  • Boot ROMs
	  • PMIC interface
	  • Resource Domain Controller

Table 1. i.MX 8QuadMax advanced features (continued)

Function	Feature
I/O	1× PCIe (2-lanes). Can be used as two PCIe 3.0 controllers with one-lane, independent operation. PCIe 1.0 and 2.0 compliant. PCIe 3.0 capable, contact your NXP representative.
	1× USB 3.0 with PHY
	2× USB 2.0 (1 with PHY, 1 with HSIC)
	1× SATA 3.0 can be used as PCIe one-lane. This is in addition to the standard PCIe controller. PCIe 1.0 and 2.0 compliant. PCIe 3.0 capable, contact your NXP representative.
	2× 1Gb Ethernet with AVB (can be used as 10/100 Mbps ENET with AVB)
	3× CAN/CAN-FD
	8× UARTs: • 5× UARTs (2× with hardware flow control) • 2× UARTs tightly coupled with Cortex-M4F cores (1× per Cortex-M4F core) • 1× UART tightly coupled with SCU

	18× I^2C:
	• 5× General-Purpose I^2C (full-speed with DMA support)
	• Low-speed I^2C without DMA support:
	  • 2× master I^2C in MIPI-DSI (1× per instance)
	  • 4× master I^2C in LVDS (2× per instance)
	  • 2× master I^2C in HDMI-TX
	  • 2× master I^2C in MIPI-CSI (1× per instance)
	  Note: Although low-speed I^2Cs can be made available for general purpose use which requires the associated PHY (for example, MIPI) to be powered on, it is not recommended.
	  Note: I/O muxing constraints prevent using all I^2Cs simultaneously.
	• 2x I2C tightly coupled with Cortex-M4 cores (1x per Cortex M4F core)
	  Note: The tightly coupled M4 I2C ports cannot be used for general purpose use.
	• 1× I^2C tightly coupled with SCU for communication with the PMIC. Not general purpose and not available for non-PMIC uses.

	4× SAI (SAI0 and SAI1 are transmit/receive; SAI2 and SAI3 are receive only)
	2× Enhanced Serial Audio Interface (ESAI)
	× ASRC (Asynchronous Sample Rate Converter) (note: no I/O signals are directly connected to this module)
	1× SPDIF (Tx and Rx)
	2× 4-channel ADC converters
	3.3 V/1.8 V GPIO
	4× PWM channels
	1× 6×8 KPP (Key Pad Port)
	1× MQS (Medium Quality Sound)
	4× SPI
Packaging	Case FCPBGA 29 x 29 mm, 0.75 mm pitch

1.1 Ordering Information

The following table provides the ordering information.

Table 2. i.MX 8QuadMax Orderable part numbers

Part Number	Options	Cortex-A72	Cortex-A53	Cortex-M4F	GPU	Qualification Tier	Package
MIMX8QM5AVUFEAB	1 x VPU	Two @ 1.296 GHz	Four @ 1.2 GHz	Two @ 264 MHz	Two @ 650 MHz	Automotive AEC-Q100	29 mm × 29 mm 0.75 mm pitch FCPBGA (lidded)
MIMX8QM6AVUFEAB	1 x VPU 1 x DSP						

1.2 System Controller Firmware (SCFW) Requirements

The i.MX 8 and 8X families require a minimum SCFW release version for correct operation and to prevent potential reliability issues.

The SCFW is released as part of a Board Support Package (e.g. Linux, Android) which may vary in version number for a specific BSP.

For example, LF6.6.y_2.0.0 GA contains SCFW version 1.16, Whereas 5.10.0_1.0.0 GA contains SCFW version 1.8.0.

For i.MX 8 part numbers in this datasheet, LF6.6.y_2.0.0 GA and SCFW 1.16 or later MUST be used.

The released SCFW version associated within each BSP is the minimum version required to correctly support the wider BSP functionality.

Customers should always check that they are using the specific SCFW binary delivered within their chosen BSP release. Customers should not mix newer BSP versions with older revisions of the SCFW.

1.3 Related resources

Table 3. Related resources

Type	Description
Reference manual	The *i.MX 8QuadMax Applications Processor Reference Manual* (IMX8QMRM) contains a comprehensive description of the structure and function (operation) of the SoC.
Data sheet	This data sheet includes electrical characteristics and signal connections.
Chip Errata	The chip mask set errata provides additional and/or corrective information for a particular device mask set.
Package drawing	Package dimensions are provided in Section 6, “Package information and contact assignments"."
Hardware guide	The *i.MX 8QuadMax/8QuadPlus Hardware Developer’s Guide* (IMX8HWDG) provides system design guidelines.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 8QuadMax processor system.

2.1 Block Diagram

The following figure shows the functional modules in the processor system.

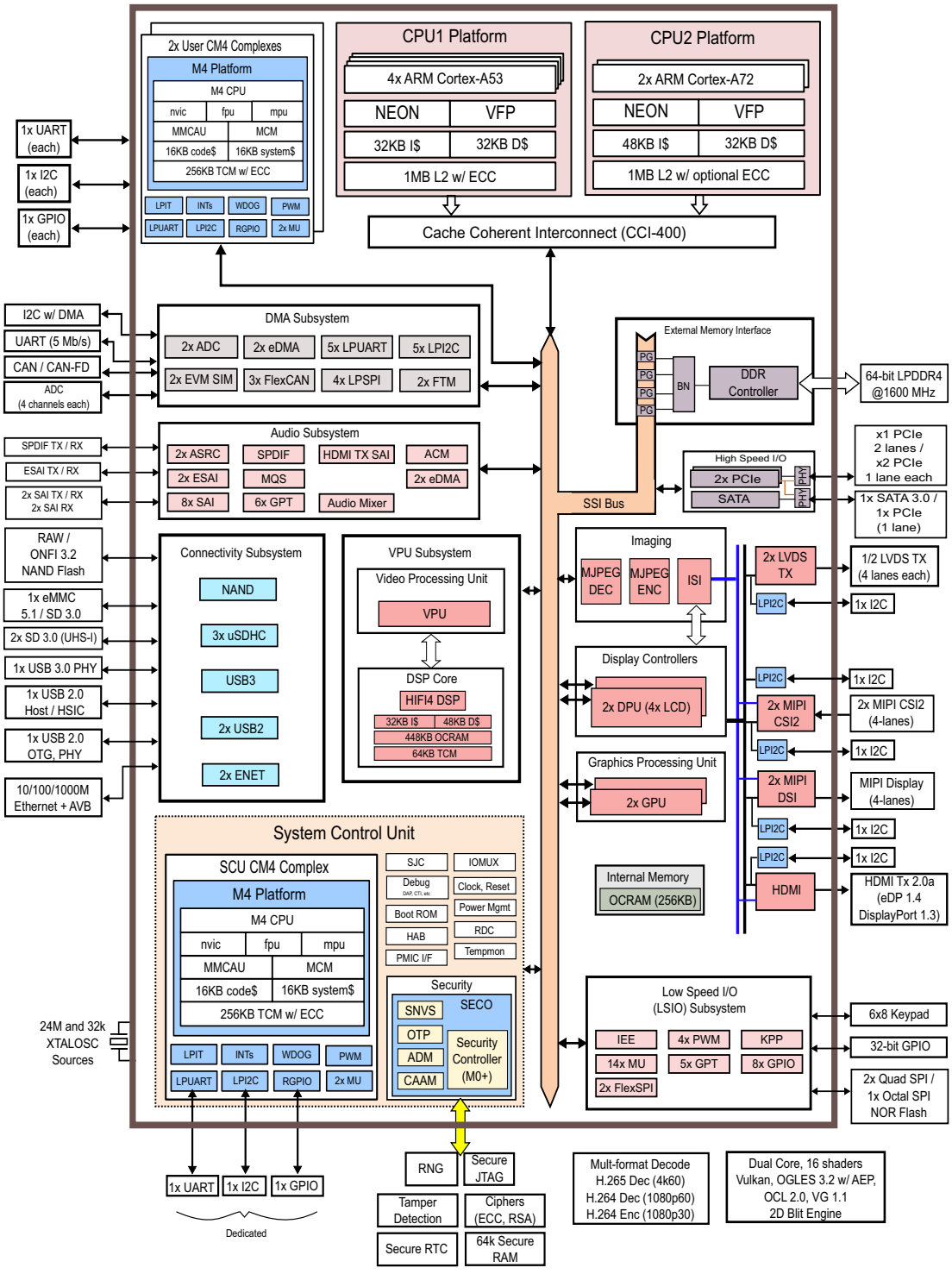

Figure 1. i.MX 8QuadMax System Block Diagram

3 Modules List

The i.MX 8QuadMax processors contain a variety of digital and analog modules. This table describes the processor modules in alphabetical order.

Table 4. i.MX 8QuadMax modules list

Block Mnemonic	Block Name	Brief Description
ADC	Analog-to-Digital Converter	The analog-to-digital converter (ADC) is a successive approximation ADC designed for operation within a SoC.
APBH-DMA	NAND Flash and BCH ECC DMA Controller	The AHB-to-APBH bridge provides the chip with a peripheral attachment bus running on the AHB's HCLK, which includes the AHB-to-APB PIO bridge for a memory-mapped I/O to the APB devices, as well as a central DMA facility for devices on this bus and a vectored interrupt controller for the Arm core.
A53	Arm (CPU1)	CPU cluster embedding 4x Cortex-A53 CPUs with a 32KB L1 instruction cache and a 32KB data cache. The CPUs share a 1 MB L2 cache.
A72	Arm (CPU2)	CPU cluster embedding 2x Cortex-A72 CPUs with a 48 KB L1 instruction cache and 32 KB data cache. The CPUs have a 1MB L2 cache.
ASRC	Asynchronous Sample Rate Converter	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
BCH-62	Binary-BCH ECC Processor	The BCH62 module provides up to 62-bit ECC for NAND Flash controller (GPMI2)
CAAM	Cryptographic Accelerator and Assurance Module	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). CAAM also implements a Secure Memory mechanism. In this device the security memory provided is 64 KB.
CTI	Cross Trigger Interface	CTI sends signals across the chip indicating that debug events have occurred. It is used by features of the Coresight infrastructure.
CTM	Cross Trigger Matrix	Cross Trigger Matrix IP is used to route triggering events between CTIs.
DAP	Debug Access Port	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains.
DC	Display Controller	Dual display controller
DDR Controller	DRAM Controller	• Memory types: LPDDR4 • Two channels of 32-bit memory: • LPDDR4 up to 1.6 GHz

Table 4. i.MX 8QuadMax modules list (continued)

Block Mnemonic	Block Name	Brief Description
DPR	Display/Prefetch/ Resolve	The DPR prefetches data from memory and converts the data to raster format for display output. Raster source buffers can also be prefetched unconverted. The resolve process supports graphics and video formatted tile frame buffers and converts them to raster format. Embedded display memory is used as temporary storage for data which is sourced by the display controller to drive the display.

eDMA	Enhanced Direct Memory Access	• 4× eDMA with a total of 128 channels (note: all channels are not assigned; see the product reference manual for more information):
		  • 4× instances with 32 channels each
		• Programmable source, destination addresses, transfer size, plus support for enhanced addressing modes
		• Internal data buffer, used as temporary storage to support 64-byte burst transfers, one outstanding transaction per DMA controller.
		• Transfer control descriptor organized to support two-deep, nested transfer operations
		• Channel service request via one of three methods:
		  • Explicit software initiation
		  • Initiation via a channel-to-channel linking mechanism for continuous transfers
		  • Peripheral-paced hardware requests (one per channel)
		• Support for fixed-priority and round-robin channel arbitration
		• Channel completion reported via interrupt requests
		• Support for scatter/gather DMA processing
		• Support for complex data structures via transfer descriptors
		• Support to cancel transfers via software or hardware
		• Each eDMA instance can be uniquely assigned to a different resource domain, security (TZ) state, and virtual machine
		• In scatter-gather mode, each transfer descriptor's buffers can be assigned to different SMMU translation

ENET	Ethernet Controller	2× 1 Gbps Ethernet controllers supporting RGMII + AVB (Audio Video Bridging, IEEE 802.1Qav)
ESAI	Enhanced Serial Audio Interface	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.
FTM	FlexTimer	Provides input signal capture and PWM support
FlexCAN	Flexible Controller Area Network	Communication controller implementing the CAN with Flexible Data rate (CAN FD) protocol and the CAN protocol according to the CAN 2.0B protocol specification.

Table 4. i.MX 8QuadMax modules list (continued)

Block Mnemonic	Block Name	Brief Description
FlexSpi (Quad SPI/Octal SPI)	Flexible Serial Peripheral Interface	• Flexible sequence engine to support various flash vendor devices, including HyperBus™ devices: • Support for FPGA interface • Single, dual, quad, and octal mode of operation. • DDR/DTR mode wherein the data is generated on every edge of the serial flash clock. • Support for flash data strobe signal for data sampling in DDR and SDR mode. • Two identical serial flash devices can be connected and accessed in parallel for data read operations, forming one (virtual) flash memory with doubled readout bandwidth.
GIC	Generic Interrupt Controller	The GIC-500 handles all interrupts from the various subsystems and is ready for virtualization.
GPIO	General Purpose I/O Modules	Used for general purpose input/output to external devices. Each GPIO module supports 32 bits of I/O.
GPMI	General Purpose Media Interface	The GPMI module supports up to 8× NAND devices. 62-bit ECC (BCH) encryption/decryption for NAND Flash controller (GPMI). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU	Graphics Processing	2× GC7000XSVX GPUs with 8 shaders each that can run either independently or in “dual-mode” with 16 shaders.
HDMI Tx/ DP/eDP	HDMI Tx interface	HDMI transmitter, Display Port 1.3 and embedded Display Port 1.4
HDMI Rx	HDMI Rx interface	HDMI 1.4b receiver (See restrictions in Section 4.10.8)
HiFi 4 DSP	Audio Processor	A highly optimized audio processor geared for efficient execution of audio and voice codecs and pre- and post-processing modules to offload the Arm core.
I^2C	I^2C Interface	I^2C provides serial interface for external devices.

IEE		• Supports direct encryption and decryption of FlexSPI memory type
		• Provides decryption services (lower performance) for DRAM traffic
		• Supports I/O direct encrypted storage and retrieval
		• Support for a number of cryptographic standards:
		  • 128/256-bit AES Encryption (AES-CTR, AES-XTS mode options)
		• Multiple keys supported:
		  • Loaded via secure key channel from security block
		  • Key selection is per access and based on source of transaction

IOMUXC	IOMUX Control	This module enables flexible I/O multiplexing. Each I/O pad has default and several alternate functions. The alternate functions are software configurable.

Table 4. i.MX 8QuadMax modules list (continued)

Block Mnemonic	Block Name	Brief Description
JPEG/dec	MJPEG engine for decode	Provides up to 4-stream decoding in parallel.
JPEG/enc	MJPEG engine for encode	Provides up to 4-stream encoding in parallel.
KPP	Key Pad Port	The Keypad Port (KPP) is a 16-bit peripheral that can be used as a 6 x 8 keypad matrix interface or as general purpose input/output (I/O).
LPIT-1 LPIT-2	Low-Power Periodic Interrupt Timer	Each LPIT is a 32-bit “set and forget” timer that starts counting after the LPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
LPSPI 0–3	Configurable SPI	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
LVDS	LVDS Display Bridge	This high performance serializer supports a pair of LVDS displays with 8 lanes each. Each port can be configured for 2x Tx with 4 lanes each.
M4F	Arm (CPU3)	• Cortex-M4F core • AHB LMEM (Local Memory Controller) including controllers for TCM and cache memories • 256 KB embedded tightly coupled memory(TCM) (128 KB TCMU, 128 KB TCML) • 16 KB Code Bus Cache • 16 KB System Bus Cache • ECC for TCM memories and parity for code and system caches • Integrated Nested Vector Interrupt Controller (NVIC) • Wakeup Interrupt Controller (WIC) • FPU (Floating Point Unit) • Core MPU (Memory Protection Unit) • Support for exclusive access on the system bus • MMCAU (Crypto Acceleration Unit) • MCM (Miscellaneous Control Module)
MIPI CSI-2	MIPI CSI-2 Interface	The MIPI CSI-2 IP provides MIPI CSI-2 standard camera interface ports. The MIPI CSI-2 interface supports up to 1.5 Gbps for up to 4 data lanes
MIPI-DSI	MIPI DSI interface	The MIPI DSI IP provides DSI standard display serial interface. The DSI interface supports 80 Mbps to 1.5 Gbps speed per data lane.
MQS	Medium Quality Sound	Medium Quality Sound (MQS) is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.
OCOTP_CTRL	OTP Controller	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent nonvolatility.

Table 4. i.MX 8QuadMax modules list (continued)

Block Mnemonic	Block Name	Brief Description
OCRAM	On-Chip Memory Controller	The On-Chip Memory controller (OCRAM) module is designed as an interface between the system's AXI bus and the internal (on-chip) SRAM memory module. The OCRAM is used for controlling the 256 KB multimedia RAM through a 64-bit AXI bus.
PCIe	PCI Express	PCIe 1.0 and 2.0 compliant. PCIe 3.0 capable; contact your NXP representative. .
PRG	Prefetch/Resolve Gasket	The PRG is a gasket which translates system memory accesses to local display RTRAM accesses for display refresh. It works with the DPR to complete the prefetch and resolving operations needed to drive the display.
PWM	Pulse Width Modulation	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4×16 data FIFO to generate square waveforms.
RAM 64 KB Secure RAM	Secure/non-secure RAM	Secure/non-secure Internal RAM, interfaced through the CAAM.
RAM 256 KB	Internal RAM	Internal RAM, which is accessed through OCRAM memory controllers.
RNG	Random Number Generator	The purpose of the RNG is to generate cryptographically strong random data. It uses a true random number generator (TRNG) and a pseudo-random number generator (PRNG) to achieve true randomness and cryptographic strength. The RNG generates random numbers for secret keys, per message secrets, random challenges, and other similar quantities used in cryptographic algorithms.
SAI	I2S/SSI/AC97 Interface	The SAI module provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.
SECO	Security Controller	Core and associated memory and hardware responsible for key management.
SJC	Secure JTAG Controller	The SJC provides the JTAG interface, which is compatible with JTAG TAP standards, to internal logic. This device uses JTAG port for production, testing, and system debugging. Additionally, the SJC provides BSR (Boundary Scan Register) standard support, which is compatible with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
sMMU	System MMU	The System MMU is an MMU-500 from Arm. It supports two-stage address translation and multiple translation contexts.
SNVS	Secure Non-Volatile Storage	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control.
SPDIF	Sony Philips Digital Interconnect Format	The Sony/Philips Digital Interface (SPDIF) audio block is a stereo transceiver that allows the processor to receive and transmit digital audio. The SPDIF transceiver allows the handling of both SPDIF channel status (CS) and User (U) data and includes a frequency measurement block that allows the precise measurement of an incoming sampling frequency.

Table 4. i.MX 8QuadMax modules list (continued)

Block Mnemonic	Block Name	Brief Description
TEMPMON	Temperature Monitor	The temperature monitor/sensor IP module for detecting high temperature conditions. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed; therefore, the read-out value may not be the reflection of the temperature value for the entire die.
UART	UART Interface	• High-speed TIA/EIA-232-F compatible, up to 5.0 Mbps • Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s) • 9-bit or Multidrop mode (RS-485) support (automatic slave address detection) • 7, 8, 9, or 10-bit data characters (7-bits only with parity) • 1 or 2 stop bits • Programmable parity (even, odd, and no parity) • Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals
USB3/USB2		The USB3/USB2 OTG module has been specified to perform USB 3.0 dual role and USB 2.0 On-The-Go (OTG) compatible with the USB 3.0, and USB 2.0 specification with OTG supplementary specifications. This controller supports twoindependent USB cores (1× USB3.0 dual-role, 1× USB2.0 OTG) and includes the PHY and I/O interfaces to support this operation. The full pinout of the USB 3.0 controller includes the signaling for both USB 3.0 and USB 2.0. This does not mean there is a separate USB 2.0 controller that can be used independently and simultaneously with USB 3.0. This device has an additional separate, independent USB 2.0 OTG controller which can be used simultaneously with this USB 3.0. Specific features requested for this updated module: • Super Speed (5 Gbps), High Speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps) • Fully compatible with the USB 3.0 specification (backward compatible with USB 2.0) • Fully compatible with the USB On-The-Go supplement to the USB 2.0 specification • Hardware support for OTG signaling • Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) implemented in hardware, which can also be controlled by software
USBOH		The USBOH module has been specified which performs USB 2.0 On-The-Go (OTG) and USB 2.0 Host functionality compatible with the USB 2.0 with OTG supplement and HS IC-USB specification. This controller supports two independent USB cores (1× USB2.0 OTG, 1× USB2.0 Host) and includes the PHY and I/O interfaces to support this operation. Key features: • One USB2.0 OTG controller • High Speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps) • Fully compatible with the USB 2.0 specification • Fully compatible with the USB On-The-Go supplement to the USB 2.0 specification • Hardware support for OTG signaling • Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) implemented in hardware, which can also be controlled by software • USB2.0 Host with HS IC-USB specification • HS IC-USB transceiver-less downstream support (Host only).

Table 4. i.MX 8QuadMax modules list (continued)

Block Mnemonic	Block Name	Brief Description
uSDHC	SD/eMMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	i.MX 8 Family SoC-specific characteristics: All three MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. The uSDHC is a host controller used to communicate with external low cost data storage and communication media. It supports the previous versions of the MultiMediaCard (MMC) and Secure Digital Card (SD) standards. Specifically, the uSDHC supports: • SD Host Controller Standard Specification v3.0 with the exception that all the registers do not match the standards address mapping. • SD Physical Layer Specification v3.0 UHS-I (SDR104/DDR50) • SDIO specification v3.0 • eMMC System Specification v5.1
VPU	Video Processing Unit	See the device reference manual for the complete list of the VPU's decoding/encoding capabilities.
WDOG	Watchdog	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
XTAL OSC24M		The 24 MHz clock source is an external crystal that acts as the main system clock. The OSC24M is used as the source clock for subsystem PLLs. OSC24M can be turned off by the System Control Unit (SCU) during sleep mode.
XTAL OSC32K		The 32.768 kHz clock source is an external crystal. The OSC32K is intended to be always on and is distributed by the SCU to modules in the chip.

3.1 Special Signal Considerations

Special signal considerations can be found in the Hardware Developer's Guide for this device in the Design Checklist section.

3.2 Recommended Connections for Unused Interfaces

The recommended connections for unused analog interfaces can be found in the section, "Unused Input/Output Terminations," in the Hardware Developer's Guide for this device.

4 Electrical characteristics

This section provides the device and module-level electrical characteristics for these processors.

4.1 Chip-level conditions

This section provides the device-level electrical characteristics for the SoC. See the following table for a quick reference to the individual tables and sections.

Table 5. Chip-level conditions

For these characteristics, …	Topic appears …
Absolute maximum ratings	on page 16
FCPBGA package thermal resistance data	on page 18
Operating ranges	on page 18
External Input Clock Frequency	on page 22
Maximum supply currents	on page 23
Standby use cases	on page 48
USB 2.0 PHY typical current consumption in Power-Down Mode	on page 27
USB 3.0 PHY typical current consumption in Power-Down Mode	on page 27
Typical current consumption in Power-Down mode for USB 2.0 PHY embedded in USB 3.0 PHY	on page 27

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 6 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the "Operating ranges" or other parameter tables is not implied. Exposure to absolute-maximum-rated conditions for extended periods will affect device reliability.

Table 6. Absolute maximum ratings

Parameter Description	Symbol	Min	Max	Units
Core Supplies Input Voltage	VDD_A72	-0.3	1.2	V
	VDD_A53			
	VDD_GPU0			
	VDD_GPU1			
	VDD_MAIN			
	VDD_MEMC			
DDR PHY supplies	VDD_DDR_VDDQ	-0.3	1.75	V
1.0V IO supplies	VDD_MIPI_1P0	-0.3	1.2	V
	VDD_USB_OTG_1P0			
IO Supply for GPIO Type 1.8V IO Single supply	VDD_ADC_1P8	-0.5	2.1	V
	VDD_ADC_DIG_1P8			
	VDD_ANA0_1P8 (IO, analog,OSC SCU)			
	VDD_ANA1_1P8 (IO, analog,OSC SCU)			
	VDD_DDR_PLL_1P8 (memory PLLs)			
	VDD_MIPI_1P8 (PHY, GPIO)			
	VDD_MIPI_CSI_DIG_1P8 (PHY, GPIO)			
	VDD_PCIE_1P8 (PHY)			
	VDD_USB_1P8 (PHY, GPIO)			
IO Supply for GPIO Type 1.8 / 2.5 / 3.3V IO Tri-voltage Supply	VDD_ENET1_1P8_2P5_3P3	-0.3	3.8	V
	VDD_ENET0_1P8_3P3			

Table 6. Absolute maximum ratings (continued)

Parameter Description	Symbol	Min	Max	Units
IO Supply for GPIO Type 1.8 / 3.3V IO Dual Voltage Supply	VDD_CAN_UART_1P8_3P3	-0.3	3.9	V
	VDD_CSI_1P8_3P3			
	VDD_EMMC0_1P8_3P3			
	VDD_EMMC0_VSELECT_1P8_3P3			
	VDD_ENET_MDIO_1P8_3P3			
	VDD_MIPI_DSI_DIG_1P8_3P3			
	VDD_PCIE_DIG_1P8_3P3			
	VDD_QSPI0A_1P8_3P3			
	VDD_QSPI0B_1P8_3P3			
	VDD_SPI_MCLK_UART_1P8_3P3			
	VDD_SPI_SAI_1P8_3P3			
	VDD_TMPR_CSI_1P8_3P3			
	VDD_USB_3P3 (PHY & GPIO)			
	VDD_USDHC1_1P8_3P3			
	VDD_USDHC1_VSELECT_1P8_3P3			
SNVS Coin Cell	VDD_SNVS_4P2	-0.3	4.3	V
USB VBUS (OTG2)	USB_OTG2_VBUS	-0.3	3.63	V
USB VBUS (OTG1)	USB_OTG1_VBUS	-0.3	5.5	V
I/O Voltage for USB Drivers	USB_OTG1_DP/USB_OTG1_DN	-0.3	3.63	V
	USB_OTG2_DP/USB_OTG2_DN			
I/O Voltage for ADC	ADC_IN*x*	-0.1	2.1	V
Vin/Vout input/output voltage range (GPIO Type Pins)	Vin/Vout	See Section 4.6.1		V
Vin/Vout input/output voltage range (DDR pins)	Vin/Vout	See Section 4.6.1		V
ESD immunity (HBM).	Vesd_HBMX	—	1000	V
ESD immunity (CDM).	Vesd_CDM	—	250	V
Storage temperature range	Tstorage	-40	150	°C

NOTE

HDMI CEC is 3.3V tolerant. HDMI DDC signals and HPD are 5V tolerant. Refer to the Hardware Developer's Guide for proper terminations.

4.1.2 Thermal resistance

4.1.2.1 FCPBGA package thermal resistance

This table provides the FCPBGA package thermal resistance data.

Table 7. FCPBGA package thermal resistance data

Rating	Board Type[1]	Symbol	29x29 mm package	Unit
Junction to Ambient Thermal Resistance[2]	JESD51-9, 2s2p	$R_{\theta JA}$	12.9	°C/W
Junction to Package Top Thermal Resistance[2]	JESD51-9, 2s2p	Ψ_{JT}	0.1	°C/W
Junction to Case Thermal Resistance[3]	JESD51-9, 1s	$R_{\theta JC}$	0.3	°C/W

1 Thermal test board meets JEDEC specification for this package (JESD51-9).

2 Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

3 Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers to the mold surface temperature at the package top side dead center.

4.1.3 Operating Ranges

The following table provides the operating ranges of these processors.

Table 8. Operating ranges[1]

Symbol	Description	Mode	Min	Typ	Max	Unit	Comments
VDD_A72	Power supply of Cortex-A72 cluster	Overdrive	1.05	1.10	1.15	V	Min frequency = 208.5 MHz Max frequency = 1.296 GHz
		Nominal	0.95	1.00	1.10	V	Max frequency = 1.06 GHz
VDD_A53	Power supply of Cortex-A53 cluster	Overdrive	1.05	1.10	1.15	V	Min frequency = 208.5 MHz Max frequency = 1.2 GHz
		Nominal	0.95	1.00	1.10	V	Max frequency - 900 MHz
VDD_GPU0	Power supply of first GPU instance	Nominal	0.980	1.03125	1.14	V	Max frequencies: Shaders = 700 MHz; Core = 650 MHz
VDD_GPU1	Power supply of second GPU instance	Nominal	0.980	1.03125	1.14	V	Max frequencies.: Shaders = 700 GHz; Core = 650 MHz
VDD_MEMC	Power supply of memory controller	N/A	1.05	1.10	1.15	V	—

Table 8. Operating ranges[1] (continued)

Symbol	Description	Mode	Min	Typ	Max	Unit	Comments
VDD_MAIN[2]	Power supply of remaining core logic	N/A	0.95	1.00	1.10	V	Min frequency: M4 = 24 MHz Max frequencies.: HiFi4 DSP = 666 MHz M4 = 264 MHz VPU = 600 MHz
VDD_DDR_CH0_VDDQ, VDD_DDR_CH0_VDDQ_CKE, VDD_DDR_CH1_VDDQ, VDD_DDR_CH1_VDDQ_CKE,	Power supplies of memory I/Os	LPDDR4	1.06	1.10	1.17	V	Max frequency = 1.6 GHz Supports LPDDR4-3200
VDD_DDR_CH0_VDDA_PLL_1P8, VDD_DDR_CH1_VDDA_PLL_1P8	Power supplies of memory PLLs	N/A	1.65	1.80	1.95	V	PLL supply can be merged with other 1.8V supplies with proper on board decoupling.
VDD_MIPI_CSI0_1P0, VDD_MIPI_CSI1_1P0, VDD_MIPI_DSI0_1P0, VDD_MIPI_DSI0_PLL_1P0, VDD_MIPI_DSI1_1P0, VDD_MIPI_DSI1_PLL_1P0, VDD_LVDS0_1P0, VDD_LVDS1_1P0	Power supplies of PHYs (1.0 V part)	N/A	0.95	1.00	1.10	V	These balls shall be connected to the same power supply as VDD_MAIN. It shall be a star connection from the power supply. Each VDD power supply ball shall have its own dedicated decoupling caps.
VDD_ANA1_1P8, VDD_ANA2_1P8, VDD_ANA3_1P8, VDD_CP_1P8, VDD_SCU_1P8, VDD_SCU_ANA_1P8, VDD_SCU_XTAL_1P8	Power supplies of I/Os, analog and oscillator of the SCU	N/A	1.65	1.70	1.75	V	These balls shall be powered by a dedicated supply. **Note:** The disconnect between the ball naming, implying a 1.8 V supply, and the actual required operating voltage of 1.7 V is known and correct as shown.

Table 8. Operating ranges[1] (continued)

Symbol	Description	Mode	Min	Typ	Max	Unit	Comments
VDD_PCIE_IOB_1P8, VDD_ADC_1P8, VDD_ADC_DIG_1P8, VDD_HDMI_RX0_1P8[3], VDD_HDMI_TX0_1P8, VDD_LVDS0_1P8, VDD_LVDS1_1P8, VDD_MIPI_CSI0_1P8, VDD_MIPI_CSI1_1P8, VDD_MIPI_DSI0_1P8, VDD_MIPI_DSI1_1P8, VDD_MLB_1P8[4], VDD_PCIE_LDO_1P8, VDD_PCIE_SATA0_PLL_1P8[3], VDD_PCIE0_PLL_1P8, VDD_PCIE1_PLL_1P8, VDD_USB_HSIC0_1P8, VDD_ANA0_1P8, VDD_MIPI_CSI_DIG_1P8	Power supplies of PHYs (1.8 V part) and GPIO operating at 1.8 V only.	N/A	1.65	1.80	1.95	V	—
VDD_HDMI_RX0_VH_RX_3P3[3], VDD_HDMI_TX0_DIG_3P3, VDD_USB_OTG1_3P3, VDD_USB_OTG2_3P3, VDD_USB_SS3_TC_3P3	Power supplies of PHYs (3.3 V part) and GPIO operating at 3.3 V only	N/A	3.00	3.30	3.60	V	—
VDD_PCIE_DIG_1P8_3P3, VDD_ENET0_1P8_3P3, VDD_ENET_MDIO_1P8_3P3, VDD_EMMC0_1P8_3P3, VDD_USDHC1_1P8_3P3, VDD_USDHC2_1P8_3P3, VDD_USDHC_VSELECT_1P8_3P3, VDD_SIM0_1P8_3P3, VDD_ESAI0_MCLK_1P8_3P3, VDD_ESAI1_SPDIF_SPI_1P8_3P3, VDD_FLEXCAN_1P8_3P3, VDD_LVDS_DIG_1P8_3P3, VDD_M4_GPT_UART_1P8_3P3, VDD_MIPI_DSI_DIG_1P8_3P3, VDD_MLB_DIG_1P8_3P3[5], VDD_QSPI0_1P8_3P3, VDD_QSPI1A_1P8_3P3, VDD_SPI_SAI_1P8_3P3	Power supplies of GPIO supporting both 1.8 V or 3.3 V	1.8 V	1.65	1.80	1.95	V	When VDD_USDHC1_1P8_3P3 or VDD_USDHC2_1P8_3P3 is used to support an SD card then it shall be on a dedicated 1.8V/3.3V regulator. When VDD_SIM0_1P8_3P3 is used to support a SIM card, it shall be on a dedicated 1.8V/3.3V regulator. VDDs of this list targeting 1.8V can share 1.8V regulator of 1.8V only VDDs VDDs of this list targeting 3.3V can share 3.3V regulator of 3.3V only VDDs
		3.3 V	3.00	3.30	3.60	V	
VDD_ENET1_1P8_2P5_3P3	Power supplies of ethernet I/Os	1.8 V	1.65	1.80	1.95	V	—
		2.5 V	2.38	2.50	2.63	V	—
		3.3 V	3.00	3.30	3.60	V	—

Table 8. Operating ranges[1] (continued)

Symbol	Description	Mode	Min	Typ	Max	Unit	Comments
VDD_USB_HSIC0_1P2	Power supply of USB-HSIC I/Os	N/A	1.1	1.2	1.3	V	—
VDD_SNVS_4P2	Power supply of SNVS	N/A	2.80	3.30	4.20	V	It can be supplied by a backup battery: a coin cell or a super cap.
Output of embedded LDOs and negative charge pump							
VDD_USB_SS3_LDO_1P0_CAP, VDD_HDMI_RX0_LDO0_1P0_CAP[3], VDD_HDMI_RX0_LDO1_1P0_CAP[3], VDD_HDMI_TX0_LDO_1P0_CAP, VDD_PCIE_LDO_1P0_CAP	1.0 V output of embedded LDOs	N/A	—	1.00	—	V	—
VDD_SNVS_LDO_1P8_CAP	1.8 V output of SNVS embedded LDO	N/A	—	1.80	—	V	—
VDD_M1P8 _CAP	-1.8 V output of embedded charge pump	N/A	—	-1.80	—	V	—
Power supplies that shall be connected to output of an embedded LDO							
VDD_HDMI_TX0_1P0	—	N/A	—	1.00	—	V	Shall be externally connected to VDD_HDMI_TX0_LDO_1P0_CAP
VDD_PCIE_SATA0_1P0, VDD_PCIE0_1P0, VDD_PCIE1_1P0	—	N/A	—	1.00	—	V	Shall be externally connected to VDD_PCIE_LDO_1P0_CAP
VDD_USB_OTG1_1P0, VDD_USB_OTG2_1P0	—	N/A	—	1.00	—	V	Shall be externally connected to VDD_USB_SS3_LDO_1P0_CAP
Junction temperature							
Junction temperature	—	—	-40		125	°C	—

1 Voltage ranges are defined to group as many supplies as possible. Individual supplies may have a wider range than listed here.

2 During low power state, this voltage can be dropped to 0.8 V +/- 3% for retention.

3 HDMI-RX is not fully supported. See restrictions in Section 4.10.8.

4 MLB is not supported on this product. This MLB power rail may be tied to the power supply voltage indicated or may be terminated, per the Hardware Developer's Guide power supplies of unused functions.

5 MLB is not supported on this product. The MLB power rail must be tied to the power supply voltage indicated if other I/O functions are used, as determined by IOMUX selection. Alternately, terminate the MLB supply per the Hardware Developer's Guide power supplies of unused functions.

4.1.4 External clock sources

Each processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for real time functions. It supplies the clock for real time clock operation and for slow-system and watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input requires a crystal using the internal oscillator amplifier.

The PCIe oscillator can be sourced internally or input to the chip. In both cases, it is a 100 MHz nominal clock using HCSL signaling to provide the PCIe reference clock.

The following table shows the interface frequency requirements.

Table 9. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[4,2]	f_{xtal}	—	24	—	MHz
PCIe oscillator[5]	f_{100M}	—	100	—	MHz
Frequency accuracy	—	—	—	±300	ppm

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. For recommendations, see the hardware development guide for this device.

3 Recommended nominal frequency 32.768 kHz.

4 Fundamental frequency crystal with internal oscillator amplifier.

5 If using an external clock instead of the internal clock source, an HCSL-compatible clock is required. Concerning EMI/EMC, note that internal source is not spread-spectrum capable.

The typical values shown in Table 9 are required for use with NXP board support packages (BSPs) to ensure precise time keeping and USB and HDMI operations.

4.1.5 Maximum Supply Currents

NOTE

Some of the numbers shown in this table are based on the companion regulator limits and not actual use cases. Current-drain application note AN13249 is also available for reference.

Table 10. Maximum supply currents

Symbol	Value	Unit	Comments
VDD_A72	5000	mA	Value based on max current delivered by PMIC
VDD_A53	2500	mA	Value based on max current delivered by PMIC
VDD_GPU0	5000	mA	Value based on max current delivered by PMIC
VDD_GPU1	5000	mA	Value based on max current delivered by PMIC
VDD_MAIN	5000	mA	Value based on max current delivered by PMIC
VDD_MEMC	3200	mA	Value based on max current delivered by PMIC
VDD_DDR_CH0_VDDQ	800	mA	Does not include current used by external memory.
VDD_DDR_CH0_VDDQ_CKE	200	mA	Does not include current used by external memory.
VDD_DDR_CH0_VDDA_PLL_1P8	20	mA	
VDD_DDR_CH1_VDDQ	800	mA	Does not include current used by external memory.
VDD_DDR_CH1_VDDQ_CKE	200	mA	Does not include current used by external memory.
VDD_DDR_CH1_VDDA_PLL_1P8	20	mA	
VDD_SCU_ANA_1P8	5	mA	
VDD_SCU_1P8	20	mA	Digital I/Os of SCU
VDD_CP_1P8	60	ma	There is a peak current of 60mA over 140 μs.
VDD_SCU_XTAL_1P8	10	mA	Supply of crystal oscillator and integrated 200 MHz oscillator
VDD_ANA0_1P8	175	mA	
VDD_ANA1_1P8	45	mA	
VDD_ANA2_1P8	140	mA	
VDD_ANA3_1P8	110	mA	
VDD_SIM0_1P8_3P3	15	mA	
VDD_M4_GPT_UART_1P8_3P3	45	mA	
VDD_ESAI1_SPDIF_SPI_1P8_3P3	40	mA	
VDD_ESAI0_MCLK_1P8_3P3	25	mA	
VDD_SPI_SAI_1P8_3P3	35	mA	
VDD_FLEXCAN_1P8_3P3	15	mA	
VDD_QSPI1A_1P8_3P3	20	mA	
VDD_QSPI0_1P8_3P3	35	mA	
VDD_EMMC0_1P8_3P3	55	mA	
VDD_USDHC_VSELECT_1P8_3P3	5	mA	
VDD_USDHC1_1P8_3P3	55	mA	
VDD_USDHC2_1P8_3P3	35	mA	

Table 10. Maximum supply currents (continued)

Symbol	Value	Unit	Comments
VDD_ENET_MDIO_1P8_3P3	15	mA	
VDD_ENET0_1P8_3P3	25	mA	
VDD_ENET1_1P8_2P5_3P3	25	mA	
VDD_LVDS_DIG_1P8_3P3	25	mA	
VDD_LVDSx_1P8	100	mA	x is 0 or 1
VDD_LVDSx_1P0	5	mA	x is 0 or 1
VDD_MIPI_DSI_DIG_1P8_3P3	20	mA	
VDD_MIPI_DSIx_1P8	5	mA	x is 0 or 1
VDD_MIPI_DSIx_1P0	35	mA	x is 0 or 1
VDD_MIPI_DSIx_PLL_1P0	5	mA	x is 0 or 1
VDD_MIPI_CSI_DIG_1P8	20	mA	
VDD_MIPI_CSIx_1P8	5	mA	x is 0 or 1
VDD_MIPI_CSIx_1P0	20	mA	x is 0 or 1
VDD_HDMI_TX0_DIG_3P3	5	mA	
VDD_HDMI_TX0_1P8	80	mA	
VDD_HDMI_TX0_1P0	80	mA	Shall be externally connected to VDD_HDMI_TX0_LDO_1P0_CAP
VDD_ADC_1P8	5	mA	
VDD_ADC_DIG_1P8	1	mA	
VDD_MLB_DIG_1P8_3P3[1]	10	mA	
VDD_MLB_1P8[2]	50	mA	
VDD_USB_OTG1_1P0	1	mA	Shall be externally connected to VDD_USB_SS3_LDO_1P0_CAP
VDD_USB_OTG1_3P3	30	mA	
VDD_USB_OTG2_1P0	35	mA	Shall be externally connected to VDD_USB_SS3_LDO_1P0_CAP
VDD_USB_OTG2_3P3	10	mA	
VDD_USB_SS3_TC_3P3	10	mA	
VDD_USB_HSIC0_1P2	10	mA	
VDD_USB_HSIC0_1P8	5	mA	
VDD_PCIE_DIG_1P8_3P3	5	mA	
VDD_PCIE_IOB_1P8	45	mA	
VDD_PCIE_LDO_1P8	190	mA	
VDD_PCIE_SATA0_PLL_1P8	20	mA	
VDD_PCIE0_PLL_1P8	20	mA	
VDD_PCIE1_PLL_1P8	20	mA	

Table 10. Maximum supply currents (continued)

Symbol	Value	Unit	Comments
VDD_PCIE_SATA0_1P0	65	mA	Shall be externally connected to VDD_PCIE_LDO_1P0_CAP
VDD_PCIE0_1P0	65	mA	Shall be externally connected to VDD_PCIE_LDO_1P0_CAP
VDD_PCIE1_1P0	60	mA	Shall be externally connected to VDD_PCIE_LDO_1P0_CAP
VDD_SNVS_4P2[3]	5	mA	Start-up current

1 MLB is not supported on this product. This MLB power rail must be tied to the voltage specified in Table 8 if other I/O functions are used, as determined by IOMUX selection. Alternately, terminate the MLB supply per the Hardware Developer's Guide power supplies of unused functions.

2 MLB is not supported on this product. The MLB power rail must be tied to the voltage specified in Table 8 or may be terminated, per the Hardware Developer's Guide power supplies of unused tables.

3 Under normal operating conditions, the maximum current on VDD_SNVS_4P2 is shown Table 11. During initial power on, VDD_SNVS_4P2 can draw up to 5 mA if the supply is capable of sourcing that current. If less than 5 mA is available, the VDD_SNVS_LDO_1P8_CAP charge time will increase.

4.1.6 Low power mode supply currents

The following table shows the current core consumption (not including I/O) in selected low power modes.

Table 11. i.MX 8QuadMax Key State (KSx) power consumption

Mode	Test conditions	Supply	Max	Unit
KS0	SNVS only, all other supplies OFF. RTC running, tamper not active, external 32K crystal.	VDD_SNVS_4P2 (4.2 V)	50	μA
KS1[1]	RAM and IO state retained. DRAM in self-refresh, associated I/O's OFF. 32K running, 24M, PLLs and ring oscillators OFF PHYs are in idle state. MEMC, A53, A72, and GPU supplies OFF. MAIN[2] dropped to 0.8 V.	VDD_ANAx_1P8, VDD_SCUx_1P8, VDD_CP_1P8 (1.7V)	6	mA
		VDD_A53 (OFF)	—	mA
		VDD_A72 (OFF)	—	mA
		VDD_GPU0 (OFF)	—	mA
		VDD_GPU1 (OFF)	—	mA
		VDD_MEMC (OFF)	—	mA
		VDD_DDR_CHx_VDDQ (1.1V)	1.4	mA
		VDD_MAIN (0.8V)	12	mA
		Total	21.94	mW

Table 11. i.MX 8QuadMax Key State (KSx) power consumption

Mode	Test conditions	Supply	Max	Unit
KS4[3]	Leakage test, not intended as a customer use case. Overdrive conditions set, memories active, all sub-systems powered ON. Active power minimized.	VDD_A53 (1.1V)	1066	mA
		VDD_A72 (1.1V)	2000	mA
		VDD_GPU0 (1.03125V)	2000	mA
		VDD_GPU1 (1.03125V)	2000	mA
		VDD_MEMC (1.1V)	1800	mA
		VDD_MAIN (1.0V)	1500	mA
		Total	11252.6	mW

1 Maximum values are for 25 °C $T_{ambient}$.

2 0.8 V nominal—voltage specification under this case is ± 3%.

3 Maximum values are for 125 °C $T_{junction}$. Stated supply voltages do not exceed +2% during test.

4.1.7 USB 2.0 PHY typical current consumption in Power-Down mode

In power down mode, everything is powered down, including the VBUS valid detectors, typical condition. The following table shows the USB interface typical current consumption in Power-Down mode.

Table 12. USB 2.0 PHY typical current consumption in Power-Down Mode

	VDD_USB_OTG1_3P3 (3.3 V)	VDD_ANA0_1P8 (1.8 V)	VDD_USB_OTG1_1P0 (1.0 V)
Current	1 μA	0.06 μA	0.5 μA

4.1.8 USB 3.0 PHY typical current consumption in Power-Down mode

In power down mode, everything is powered down, including the VBUS valid detectors, typical condition. The following table shows the USB interface typical current consumption in Power-Down mode.

Table 13. USB 3.0 PHY typical current consumption in Power-Down Mode

	—	VDD_ANA0_1P8 (1.8 V)	VDD_USB_OTG2_1P0 (1.0 V)
Current	—	10 μA	70 μA

The following table shows the current consumption for the USB 2.0 PHY embedded in the USB 3.0 PHY.

Table 14. Typical current consumption in Power-Down mode for USB 2.0 PHY embedded in USB 3.0 PHY

	VDD_USB_OTG2_3P3 (3.3 V)	VDD_ANA0_1P8 (1.8 V)	VDD_USB_OTG2_1P0 (1.0 V)
Current—Host mode	22.6 μA	12.7 μA	81.5 μA
Current—Device mode	12.6 μA	85.7 μA	78.5 μA

4.2 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to ensure the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor

4.2.1 Power-up sequence

The device has the following power-up sequence requirements:

- Supply group 0 (SNVS) must be powered first. It is expected that group 0 will typically remain always on after the first power-on.
- Supply group 1 (MAIN and SCU) and group 0 must both be powered to their nominal values prior to boot. They must power up after or simultaneously with group 0.
- Supply group 2 (I/O's and DDR interface) consists of those modules required to start the boot process by accessing external storage devices. These must be fully powered prior to POR release if booting from one of these supplies interfaces. They must power up after or simultaneously with group 1.
- Supply group 3 consists of the remaining portions of the SoC. This includes nonboot I/O voltages and supplies for the major computational units. These can be sequenced in any order and as required to perform the desired functions for the intended application. They must power up after or simultaneously with group 2.

NOTE

The definition of "power-up" refers to a stable voltage operating within the range defined in Table 8. This should be taken into consideration, along with the different capacitive loading on each rail, if considering simultaneous switch-on of the different supply groups.

4.2.2 Power-down sequence

The device processor has the following power-down sequence requirements:

- Supply group 0 must be turned off last, after all other supplies.
- Supply group 1 can be turned off just prior to group 0.

All remaining supplies can be turned off prior to group 1.

NOTE

When switching off supply group 0 (SNVS), VDD_SNVS_LDO_1P8_CAP must be fully discharged to 0 V before starting the next power-up sequence to ensure correct operation.

4.2.3 Power Supplies Usage

The following table shows the power supplies usage by group.

Table 15. Power supplies usage

Supply Groups	Voltage				
Group 0	**2.4 - 4.2v**				
	VDD_SNVS_4P2				
Group 1	**1.0v**	**1.8v**			
	VDD_MAIN	VDD_ANA1_1P8			
	VDD_LVDS**x**_1P0	VDD_ANA2_1P8			
	VDD_MIPI_CSI**x**_1P0	VDD_ANA3_1P8			
	VDD_MIPI_DSI**x**_1P0	VDD_CP_1P8			
	VDD_MIPI_DSI**x**_PLL_1P0	VDD_SCU_1P8			
		VDD_SCU_**x**_1P8			
Group 2	**1.1V**		**1.8v**	**1.8v or 3.3v**	**1.8v or 3.3v switchab**
	VDD_MEMC		VDD_ADC_DIG_1P8	VDD_EMMC0_1P8_3P3	VDD_USDHC**x**_1P8_3
	VDD_DDR_CH**x**_VDDQ		VDD_ADC_1P8	VDD_ESAI0_MCLK_1P8_3P3	VDD_SIM0_1P8_3P3
	VDD_DDR_CH**x**_VDDQ_CKE		VDD_ANA0_1P8	VDD_ESAI1_SPDIF_SPI_1P8_3P3	
			VDD_DDR_CH**x**_VDDA_PLL_1P8	VDD_FLEXCAN_1P8_3P3	
			VDD_HDMI_**x**_1P8	VDD_LVDS_DIG_1P8_3P3	
			VDD_LVDS**x**_1P8	VDD_M4_GPT_UART_1P8_3P3	
			VDD_MIPI_CSI_DIG_1P8	VDD_MIPI_DSI_DIG_1P8_3P3	
			VDD_MIPI_**x**_1P8	VDD_MLB_DIG_1P8_3P3[1]	
			VDD_MLB_1P8[2]	VDD_PCIE_DIG_1P8_3P3	
			VDD_PCIE_SATA0_PLL_1P8	VDD_QSPI**x**_1P8_3P3	
			VDD_PCIE_**x**_1P8	VDD_SPI_SAI_1P8_3P3	
			VDD_PCIE**x**_PLL_1P8	VDD_USDHC_VSELECT_1P8_3P3	
			VDD_USB_HSIC0_1P8		
Group 3	**1.1 - 1.1v**	**1.0v internal LDO's**	**1.2v**	**1.8v or 2.5v or 3.3v**	
	VDD_A53	VDD_HDMI_TX0_1P0	VDD_USB_HSIC0_1P2	VDD_ENET_MDIO_1P8_3P3	
	VDD_A72	VDD_PCIE_SATA0_1P0		VDD_ENET0_1P8_3P3	
				VDD_ENET1_1P8_2P5_3P3	
	VDD_GPU**x**	VDD_PCIE**x**_1P0			
		VDD_USB_OTG**x**_1P0			

[1] MLB is not supported on this product. This MLB power rail must be tied to the voltage specified in Table 8 if other I/O functions ar IOMUX selection. Alternately, terminate the MLB supply, per the Hardware Developer's Guide power supplies usage of unused fe

[2] MLB is not supported on this product. The MLB power rail must be tied to the voltage specified in Table 8 or may be terminated, pe Guide power supplies of unused funtions.

4.3 PLL electrical characteristics

4.3.1 PLLs of subsystems

i.MX 8QuadMax embeds a large number of PLLs to address clocking requirements of the various subsystems. These PLLs are controlled through the SCU and not directly by Cortex-A or Cortex-M4F processors. A software API shall be used by those processors to access the PLL settings. Additional PLLs are specific to high-performance interfaces. These are described in the following sections.

This table summarizes the PLLs controlled by the SCU.

Table 16. PLLs controlled by SCU

Subsystem	PLL usage	Source clock	Locking range[1]		Unit
			Min freq.	Max freq.	
Cortex-A53	Subsystem	24	1250	2500	MHz
Cortex-A72	Subsystem	24	1250	2500	MHz
CCI	Subsystem	24	650	1300	MHz
GPU	PLL #0: subsystem	24	1250	2500	MHz
	PLL #1: shaders	24	1250	2500	MHz
DRC (DRAM Controller)	Subsystem	24	1250	2500	MHz
DB (DRAM Block)	Subsystem	24	650	1300	MHz
DBLog	Subsystem	24	650	1300	MHz
Display Controller 0	PLL #0: subsystem	24	650	1300	MHz
	PLL #1: display clock #0	24	650	1300	MHz
	PLL #2: display clock #1	24	650	1300	MHz
Display Controller 1	PLL #0: subsystem	24	650	1300	MHz
	PLL #1: display clock #0	24	650	1300	MHz
	PLL #2: display clock #1	24	650	1300	MHz
Imaging	Subsystem	24	650	1300	MHz
Audio	PLL #0: subsystem	24	650	1300	MHz
	PLL #1: audio PLL #0	24	650	1300	MHz
	PLL #2: audio PLL #1	24	650	1300	MHz
Connectivity	Subsystem	24	650	1300	MHz
HSIO (High-speed I/O)	Subsystem	24	650	1300	MHz
LSIO (Low-speed I/O)	Subsystem	24	650	1300	MHz

Table 16. PLLs controlled by SCU (continued)

Subsystem	PLL usage	Source clock	Locking range[1]		Unit
			Min freq.	Max freq.	
Cortex-M4	Subsystem	24	650	1300	MHz
VPU	PLL #0: subsystem	24	650	1300	MHz
	PLL #1: Audio DSP (HiFi 4)	24	650	1300	MHz
HDMI-TX / eDP	Subsystem	24	650	1300	MHz
MIPI-DSI	Subsystem	24	650	1300	MHz
MIPI-CSI	Subsystem	24	650	1300	MHz
DMA	Subsystem	24	650	1300	MHz
SCU (System Controller Unit)	Subsystem	24	650	1300	MHz

1 Operating frequencies are limited to only those supported by the SCFW.

4.3.2 PLLs dedicated to specific interfaces

The following sections cover PLLs used for specific interfaces. Clock output frequency and clock output range refer to the output of the PLL. Additional clock dividers may be on the output path to divide the output frequency down to the targeted frequency. See the related sections in the reference manual for settings of these clock dividers.

4.3.2.1 Ethernet PLL

This PLL is controlled by the SCU.

Table 17. Ethernet PLL

Parameter	Value	Unit
Reference clock	24	MHz
Clock output frequency	1	GHz

4.3.2.2 USB 3.0 PLLs

USB 3.0 has two PLLs. One is embedded in Super-Speed PHY. The other one is embedded in the USB 2.0 OTG PHY that is part of the USB 3.0 interface.

The table below describes the PLL embedded in the Super-Speed PHY.

Table 18. USB 3.0 PLL embedded in Super Speed PHY

Parameter	Value	Unit
Reference clock	24	MHz
Clock output frequency	5	GHz

The table below describes the PLL embedded in the USBOTG PHY.

Table 19. USB 3.0 PLL embedded in USBOTG PHY

Parameter	Value	Unit
Reference clock	24	MHz
Clock output frequency	480	MHz

4.3.2.3 USB 2.0 OTG and USB-HSIC PLLs

This PLL is embedded in the USB 2.0 OTG PHY (the one which is not part of the USB 3.0 feature). It is also used to supply the 480 MHz clock to the HSIC interface.

Table 20. USB 2.0 OTG and USB-HSIC PLLs

Parameter	Value	Unit
Reference clock	24	MHz
Clock output frequency	480	MHz

4.3.2.4 PCIe PLLs

The PCIe interface has seven PLLs:

- One is used to generate the single, common 100 MHz reference clock to each lane
- One Transmit and one Receive PLL per lane (three lanes)

The table below shows the characteristics for the reference clock PLL.

Table 21. PCIe reference clock PLLs

Parameter	Value	Unit	Comments
Reference clock	24	MHz	—
Clock output frequency	100	MHz	Used to generate internal 100 MHz reference clock to PCIe lanes

The table below shows characteristics of the TX and RX PLLs used in each lane.

Table 22. PCIe Transmit and Receive PLLs[1]

Parameter	Value	Unit	Comments
Reference clock	100	MHz	From differential input clock pads or from internal PLL
Clock output range	6 ~ 10	GHz	PCIe gen3: 8GHz to get 8GHz baud clock PCIe gen2: 10GHz to get 5GHz baud clock PCIe gen1: 10GHz to get 2.5GHz baud clock

[1] PCIe 1.0 and 2.0 compliant. PCIe 3.0 capable; contact your NXP representative.

4.3.2.5 HDMI-TX / DP PLLs

The HDMI-TX interface uses two PLLs. One is used to generate the reference clock when using the HDMI PHY itself in HDMI mode. In DP mode, this PLL is bypassed and only the PLL embedded in the PHY is used.

The table below shows characteristics of the reference clock PLL for HDMI.

Table 23. HDMI reference clock PLL

Parameter	Value	Unit	Comments
Reference clock	24	MHz	—
Clock output range	1.25 ~ 2.5	GHz	Refer to HDMI / DP section of reference manual

The table below shows characteristics of the PLL embedded in HDMI/DP PHY.

Table 24. PLL embedded in HDMI/DP PHY

Parameter	Value	Unit	Comments
Reference clock	24MHz / derived from HDMI-TX PLL	MHz	24MHz: when in DP mode derived from HDMI-TX PLL: when in HDMI mode
Clock output range	≤5.4	GHz	Dependent on targeted display configuration

4.3.2.6 MIPI-DSI PLL

The table below shows characteristics of the PLL embedded in the MIPI-DSI PHY.

Table 25. MIPI-DSIPHY PLL

Parameter	Value	Unit	Comments
Reference clock	24	MHz	—
Clock output range	0.75 ~ 1.5	GHz	Dependent on targeted display configuration

4.3.2.7 LVDS PLL

The table below shows characteristics of the PLL embedded in LVDS PHY.

Table 26. LVDS PHY PLL

Parameter	Value	Unit	Comments
Reference clock	25 ~ 160	MHz	—
Data rate range	175 ~ 1120	Mbps	Dependent on targeted display configuration

4.4 On-chip oscillators

4.4.1 OSC24M

This block integrates trimmable internal loading capacitors and driving circuitry. When combined with a suitable 24 MHz external quartz element, it can generate a low-jitter clock. The oscillator is powered from VDD_SCU_XTAL_1P8. The internal loading capacitors are trimmable to provide fine adjustment of the 24 MHz oscillation frequency. It is expected that customers burn appropriate trim values for the selected crystal and board parasitics.

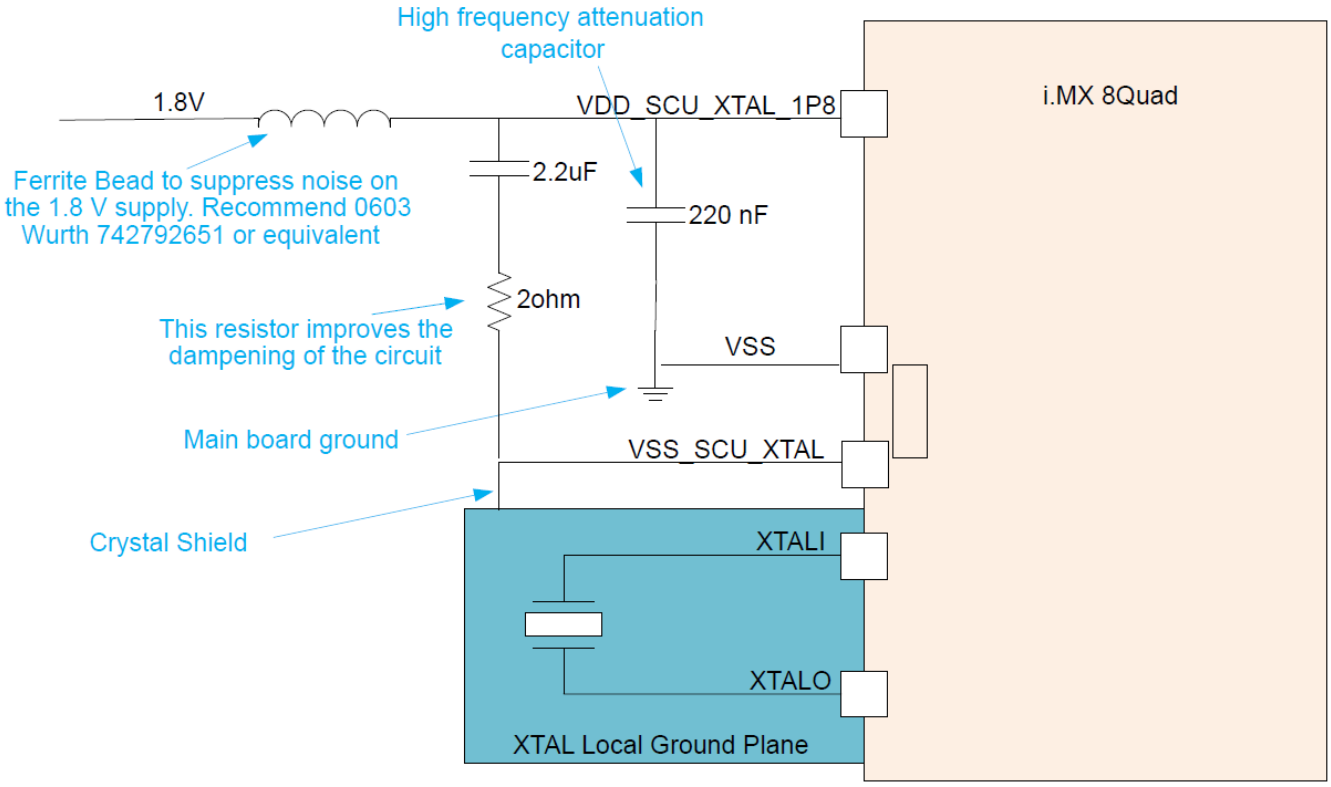

Figure 2. Normal Crystal Oscillation mode

Table 27. Crystal specifications

Parameter description	Min	Typ	Max	Unit
Frequency[1]	—	24	—	MHz
Cload[2]	—	18	—	pF
Maximum drive level	200	—	—	μW
ESR	—	—	60	Ω

1 The required frequency accuracy is set by the serial interfaces utilized for a specific application and is detailed in the respective standard documents.

2 Cload is the specification of the quartz element, not for the capacitors coupled to the quartz element.

4.4.2 OSC32K

This block implements an internal amplifier, trimmable load capacitors and a bias network that when combined with a suitable quartz crystal implements a low power oscillator.

Additionally, if the clock monitor determines that the 32KHz oscillation is not present, then the source of the 32 KHz clock will automatically switch to the internal relaxation oscillator of lesser frequency accuracy.

CAUTION

The internal ring oscillator is not meant to be used in customer applications, due to gross frequency variation over wafer processing, temperature, and supply voltage. These variations will cause timing issues to many different circuits that use the internal ring oscillator for reference; and, if this timing is critical, application issues will occur. To prevent application issues, it is recommended to only use an external crystal or an accurate external clock. If this recommendation is not followed, NXP cannot guarantee full compliance of any circuit using this clock. The OSC32K runs from VDD_SNVS_LDO_1P8_CAP, which is regulated from VDD_SNVS. The target battery/voltage range is 2.8 to 4.2 V for VDD_SNVS, with a regulated output of approximately 1.75 V.

Table 28. OSC32K main characteristics

Parameter	Min	Typ	Max	Comments
Fosc	—	32.768 kHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 KHz is also supported.
Current consumption	—	• xtal oscillator mode: 5 μA • 32K internal oscillator mode: 10 μA	—	These values are for typical process and room temperature. Values will be updated after silicon characterization.

Table 28. OSC32K main characteristics (continued)

Parameter	Min	Typ	Max	Comments
Bias resistor	—	200 MΩ	—	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amplifier. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

Table 29. External input clock for OSC32K

	Min	Typ	Max	Unit	Notes
Frequency	—	32.768 or 32	—	kHz	—
V_{PP} RTC_XTALI	700	—	VDD_SNVS_LDO_1P8_CAP	mV	1,2,3
Rise/fall time	—	—	—	ns	4

1 The external clock is fed into the chip from the RTC_XTALI pin; the RTC_XTALO pin should be left floating.

2 The parameter specified here is a peak-to-peak value and VI_H/V_{IL} specifications do not apply.

3 The voltage applied on RTC_XTALI must be within the range of VSS to VDD_SNVS_LDO_1P8_CAP.

4 The rise/fall time of the applied clock are not strictly confined.

4.5 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- XTALI and RTC_XTALI (clock inputs) DC parameters
- General Purpose I/O (GPIO) DC parameters

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

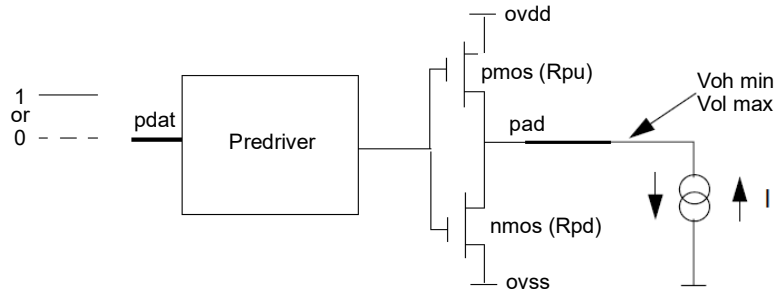

Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.5.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

For RTC_XTALI, V_{IH}/V_{IL} specifications do not apply. The high and low levels of the applied clock on this pin are not strictly defined, as long as the input's peak-to-peak amplitude meet the requirements and the input's voltage value does not exceed the limits.

4.5.2 General-purpose I/O (GPIO) DC parameters

NOTE

The term "OVDD" in this section refers to the associated supply rail of an input or output. The association is shown in Table 127.

4.5.2.1 Tri-voltage GPIO DC parameters

The following tables show tri-voltage 1.8V, 2.5 V, and 3.3 V DC parameters, respectively, for GPIO pads. These parameters are guaranteed per the operating ranges in Table 8, unless otherwise noted.

Table 30. Tri-voltage 1.8 V GPIO DC parameters[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[2,3]	V_{OH}	I_{OH}= 0.1mA PDRV=1	0.8 × OVDD	—	V
		I_{OH}= 2mA PDRV=0			
Low-level output voltage[2,3]	V_{OL}	I_{OL}= -0.1mA PDRV=1	—	0.125 × OVDD	V
		I_{OL}= -2mA PDRV=0			
High-Level input voltage[2,4]	V_{IH}	—	0.625 × OVDD	OVDD	V
Low-Level input voltage[2,4]	V_{IL}	—	0	0.25 × OVDD	V
Pull-up resistance	R_{PU}	V_{IN}=0V (Pullup Resistor) PUN = "L", PDN = "H"	15	50	kΩ

Table 30. Tri-voltage 1.8 V GPIO DC parameters[1] (continued)

Parameter	Symbol	Test Conditions	Min	Max	Units
Pull-down resistance	R_{DOWN}	V_{IN}=OVDD(Pulldown Resistor) PUN = "H", PDN = "L"	15	50	kΩ
Input current (no PU/PD)	I_{IN}	VI = 0, VI = OVDD PUN = "H", PDN = "H"	-1	1	μA

1 For tri-voltage I/O, the associated IOMUXD compensation control register PSW_OVR and COMP bits must be set correctly. For 1.8 or 3.3 V operation, the SCFW API must be used to set PSW_OVR = 0b0 and COMP=0b000. For 2.5 V operation, PSW_OVR = 0b1 and COMP = 0b010.

2 Refer to Section 4.6.1 for undershoot and overshoot specifications.

3 As programmed in the associated IOMUX (PDRV field) register. High Drive mode is recommended for 3v3 and 2v5 modes. Low Drive mode is recommended for 1v8 mode.

4 Refer to Section 4.6.2 for monotonic requirements.

Table 31. Tri-voltage 2.5 V GPIO DC parameters[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[2,3]	V_{OH}	I_{OH}= 2mA PDRV=0	0.8 × OVDD	—	V
Low-level output voltage[2,3]	V_{OL}	I_{OL}= -2mA PDRV=0	—	0.125 × OVDD	V
High-Level input voltage[2,4]	V_{IH}	—	0.625 × OVDD	OVDD	V
Low-Level input voltage[2,4]	V_{IL}	—	0	0.25 × OVDD	V
Pull-up resistance	RPU	V_{IN}=0V (Pullup Resistor) PUN = "L", PDN = "H"	10	100	kΩ
Pull-down resistance	R_{DOWN}	V_{IN}=OVDD(Pulldown Resistor) PUN = "H", PDN = "L"	10	100	kΩ
Input current (no PU/PD)	I_{IN}	VI = 0, VI = OVDD PUN = "H", PDN = "H"	-1	1	μA

1 For tri-voltage I/O, the associated IOMUXD compensation control register PSW_OVR and COMP bits must be set correctly. For 1.8 or 3.3 V operation, the SCFW API must be used to set PSW_OVR = 0b0 and COMP=0b000. For 2.5 V operation, PSW_OVR = 0b1 and COMP = 0b010.

2 Refer to Section 4.6.1 for undershoot and overshoot specifications.

3 As programmed in the associated IOMUX (PDRV field) register. High Drive mode is recommended for 3v3 and 2v5 modes. Low Drive mode is recommended for 1v8 mode.

4 Refer to Section 4.6.2 for monotonic requirements.

Table 32. Tri-voltage 3.3 V GPIO DC parameters[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[2,3]	V_{OH}	I_{OH}= 0.1mA PDRV=1	0.8 × OVDD		V
		I_{OH}= 2mA PDRV=0			
Low-level output voltage[2,3]	V_{OL}	I_{OL}= -0.1mA PDRV=1	—	0.125 × OVDD	V
		I_{OL}= -2mA PDRV=0			
High-Level input voltage[2,4]	V_{IH}	—	0.725 × OVDD	OVDD	V
Low-Level input voltage[2,4]	V_{IL}	—	0	0.25 × OVDD	V
Pull-up resistance	RPU	V_{IN}=0V (Pullup Resistor) PUN = "L", PDN = "H"	10	100	kΩ
Pull-down resistance	R_{DOWN}	V_{IN}=OVDD(Pulldown Resistor) PUN = "H", PDN = "L"	10	100	kΩ
Input current (no PU/PD)	IIN	VI = 0, VI = OVDD PUN = "H", PDN = "H"	-2	2	μA

1 For tri-voltage I/O, the associated IOMUXD compensation control register PSW_OVR and COMP bits must be set correctly. For 1.8 or 3.3 V operation, the SCFW API must be used to set PSW_OVR = 0b0 and COMP=0b000. For 2.5 V operation, PSW_OVR = 0b1 and COMP = 0b010.

2 Refer to Section 4.6.1 for undershoot and overshoot specifications.

3 As programmed in the associated IOMUX (PDRV field) register. High Drive mode recommended for 3v3 and 2v5 modes. Low Drive mode is recommended for 1v8 mode.

4 Refer to Section 4.6.2 for monotonic requirements.

4.5.2.2 Dual-voltage GPIO DC parameters

The following two tables show dual-voltage 1.8 V and 3.3 V DC parameters, respectively, for GPIO pads. These parameters are guaranteed per the operating ranges in Table 8, unless otherwise noted.

Table 33. Dual-voltage 1.8 V GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1,2]	V_{OH}	Ioh= 0.1mA PDRV=1	0.8 × OVDD	—	V
		Ioh= 2mA PDRV=0			
Low-level output voltage[1,2]	V_{OL}	Iol= -0.1mA PDRV=1	—	0.125 × OVDD	V
		Iol= -2mA PDRV=0			

Table 33. Dual-voltage 1.8 V GPIO DC parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Units
High-Level input voltage[1,3]	V_{IH}	—	0.625 × OVDD	OVDD	V
Low-Level input voltage[1,3]	V_{IL}	—	0	0.25 × OVDD	V
Pull-up resistance	R_{PU}	Vin=0 V (Pullup Resistor) PUN = "L", PDN = "H"	15	50	kΩ
Pull-down resistance	R_{down}	Vin=OVDD(Pulldown Resistor) PUN = "H", PDN = "L"	15	50	kΩ
Input current (no PU/PD)	I_{IN}	V_I = 0, V_I = OVDD PUN = "H", PDN = "H"	-1	1	μA

1 Refer to Section 4.6.1 for undershoot and overshoot specifications.

2 As programmed in the associated IOMUX (PDRV field) register. High Drive mode is recommended for SD standard (3v3 mode) and MMC standard (1v8/3v3 modes). Low Drive mode is recommended for SD standard (1v8 mode).

3 Refer to Section 4.6.2 for monotonic requirements.

Table 34. Dual-voltage 3.3 V GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1,2]	V_{OH}	Ioh= 0.1mA PDRV=1	0.8 × OVDD	—	V
		Ioh= 2mA PDRV=0			
Low-level output voltage[1,2]	V_{OL}	Iol= -0.1mA PDRV=1	—	0.125 × OVDD	V
		Iol= -2mA PDRV=0			
High-Level input voltage[1,3]	V_{IH}	—	0.725 × OVDD	OVDD	V
Low-Level input voltage[1,3]	V_{IL}	—	0	0.25 × OVDD	V
Pull-upresistance	R_{PU}	Vin=0V (Pullup Resistor) PUN = "L", PDN = "H"	10	100	kΩ
Pull-down resistance	R_{down}	Vin=OVDD(Pulldown Resistor) PUN = "H", PDN = "L"	10	100	kΩ
Input current (no PU/PD)	I_{IN}	V_I = 0, V_I = OVDD PUN = "H", PDN = "H"	-2	2	μA

1 Refer to Section 4.6.1 for undershoot and overshoot specifications.

2 As programmed in the associated IOMUX (PDRV field) register. High Drive mode is recommended for SD standard (3v3 mode) and MMC standard (1v8/3v3 modes). Low Drive mode is recommended for SD standard (1v8 mode).

3 Refer to Section 4.6.2 for monotonic requirements.

4.5.2.3 Single-voltage GPIO DC parameters

Table 35 and Table 36 show single-voltage 1.8 V and 3.3 V DC parameters, respectively, for GPIO pads. These parameters are guaranteed per the operating ranges in Table 8 unless otherwise noted.

Table 35. Single-voltage 1.8 V GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1,2]	V_{OH}	I_{OH}= 0.1mA DSE = 000 or 001	OVDD × 0.8	—	V
		I_{OH}= 2mA DSE = 010 or 011			
		I_{OH}= 4mA DSE = 100 to 110			
Low-level output voltage[1,2]	V_{OL}	I_{OL}= -0.1mA DSE = 000 or 001	—	OVDD × 0.2	V
		I_{OL}= -2mA DSE = 010 or 011			
		I_{OL}= -4mA DSE = 100 to 110			
High-Level input voltage[2,3]	V_{IH}	—	0.65 × OVDD	OVDD	V
Low-Level input voltage[2,3]	V_{IL}	—	0	0.35 × OVDD	V
Pull-up resistance	R_{PU}	Vin=0V (Pullup Resistor) PUN = "L", PDN = "H"	20	90	kΩ
Pull-down resistance	R_{down}	Vin=OVDD(Pulldown Resistor) PUN = "H", PDN = "L"	20	90	kΩ
Input current (no PU/PD)	I_{IN}	V_I = 0, V_I = OVDD PUN = "H", PDN = "H"	-5	5	μA
Keeper Circuit Resistance	R_Keeper	V_I =.3xOVDD, VI = .7x OVDD PUN = "L", PDN = "L"	12	92	kΩ

1 As programmed in the associated IOMUX (DSE field) register.

2 Refer to Section 4.6.1 for undershoot and overshoot specifications.

3 Refer to Section 4.6.2 for monotonic requirements.

Table 36. Single-voltage 3.3 V GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1,2]	V_{OH}	I_{OH} = 0.1mA DSE = 00 or 01	0.8 × OVDD	—	V
		I_{OH}= 2mA DSE = 10 or 11			

Table 36. Single-voltage 3.3 V GPIO DC parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Units
Low-level output voltage[1,2]	V_{OL}	I_{OL}= -0.1mA DSE = 00 or 01	—	0.2 × OVDD	V
		I_{OL} = -2mA DSE = 10 or 11			
High-Level input voltage[2,3]	V_{IH}	—	0.75 × OVDD	OVDD	V
Low-Level input voltage[2,3]	V_{IL}	—	0	0.25 × OVDD	V
Pull-upresistance	R_{PU}	Vin=0 V (Pullup Resistor) PUN = "L", PDN = "H"	20	90	kΩ
Pull-down resistance	R_{down}	Vin=OVDD(Pulldown Resistor) PUN = "H", PDN = "L"	20	90	kΩ
Input current (no PU/PD)	I_{IN}	V_I = 0, V_I = OVDD PUN = "H", PDN = "H"	-5	5	μA
Keeper Circuit Resistance	R_Keeper	V_I =.3xOVDD, VI = .7x OVDD PUN = "L", PDN = "L"	6	60	kΩ

1 As programmed in the associated IOMUX (DSE field) register.

2 Refer to Section 4.6.1 for undershoot and overshoot specifications.

3 Refer to Section 4.6.2 for monotonic requirements.

4.5.3 HDMI control signals parameters

The following table shows HDMI control signals DC parameters. These parameters are guaranteed per the operating ranges in Table 8, unless otherwise noted.

Table 37. HDMI DDC and HPD DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level input voltage	V_{IH}	—	2	5.3	V
Low-level input voltage	V_{IL}	—	0	0.8	V

4.5.4 DDR I/O DC parameters

4.5.4.1 LPDDR4 mode I/O DC parameters

These parameters are guaranteed per the operating ranges in Table 8 unless otherwise noted.

Table 38. LPDDR4 DC parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
High-level output voltage[1]	V_{OH}	Output Drive = All settings (40,48,60,80,120,240) unterminated outputs	$0.9 \times V_{DDQ}$	—	V
Low-level output voltage[1]	V_{OL}	Output Drive = All settings (40,48,60,80,120,240) unterminated outputs	—	$0.1 \times V_{DDQ}$	V
Input current (no ODT)	I_{IN}	V_I = VSSQ, V_I = VDDQ	-2	2	µA
DC High-Level input voltage[1]	V_{IH_DC}	—	VREF + 0.1	VDDQ	V
DC Low-Level input voltage[1]	V_{IL_DC}	—	VSSQ	VREF – 0.1	V

[1] Refer to Section 4.6.1 for undershoot and overshoot specifications.

4.6 I/O AC Parameters

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

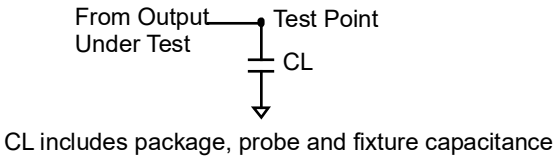

Figure 4. Load Circuit for Output

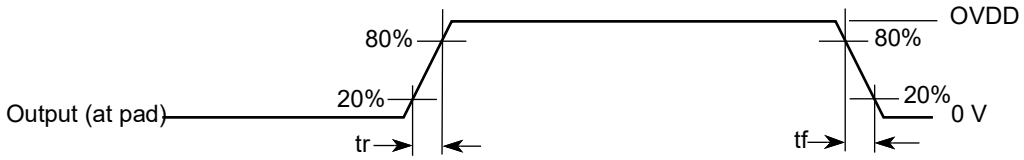

Figure 5. Output Transition Time Waveform

4.6.1 I/O Overshoot and Undershoot Parameters

For all inputs/outputs, maximum peak amplitude allowed for overshoot and undershoot is specified in Table 39. OVDD is the I/O Supply.

NOTE

If a signal edge produces more than one overshoot/undershoot event, the sum of all areas following the transition must be less than the area specified.

Table 39. Overshoot and Undershoot Parameters

Parameter	Symbol	Min	Max	Units
Amplitude above OVDD or below GND	V_{Peak}	—	0.35	V
Area above OVDD or below GND (A + B)	V_{Area}	—	0.8	V-ns

Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, and other methods. Noncompliance to this specification may affect device reliability or cause permanent damage to the device.

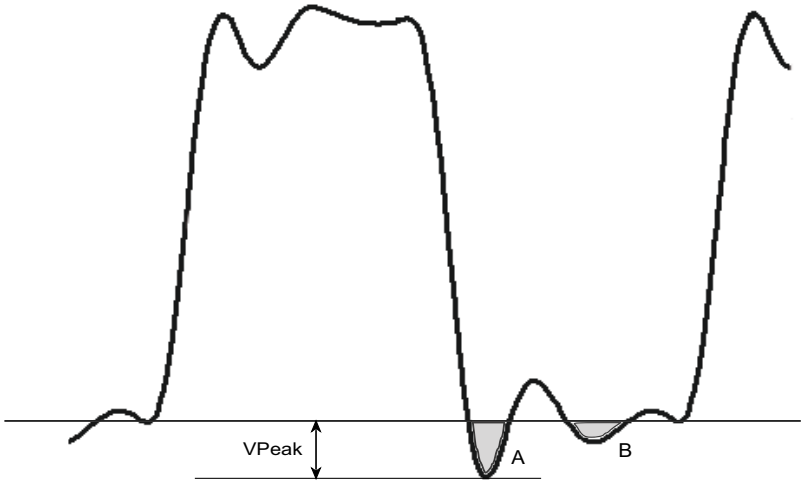

Figure 6. Undershoot Waveform Example

4.6.2 Input Signal Monotonic Requirements

Processor input signal monotonic requirements are illustrated in the following figure.

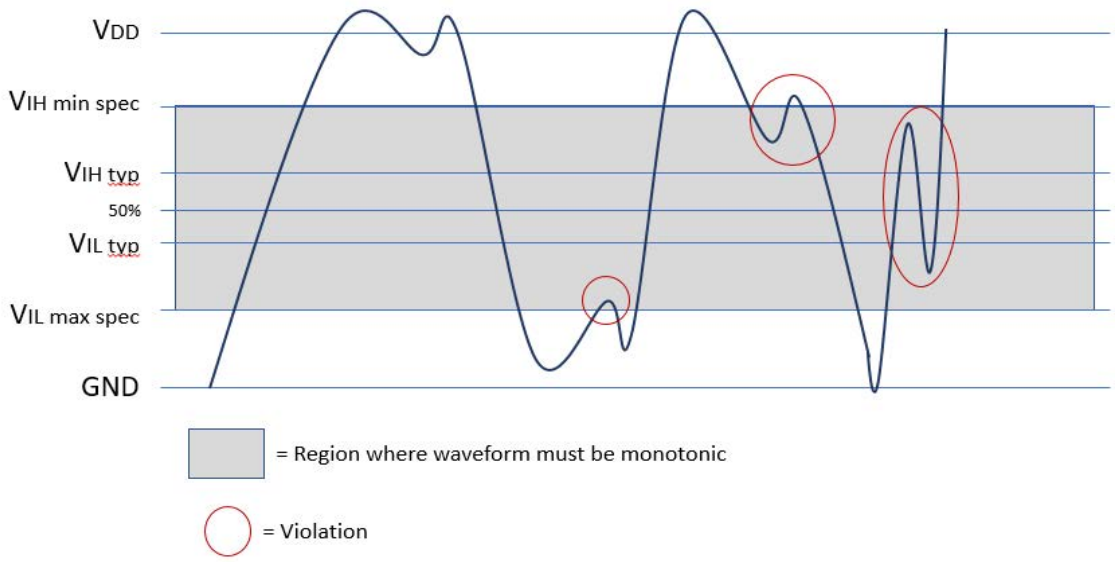

Figure 7. Input Waveform Monotonic Requirement

VIH_min and VIL_max are the guaranteed minimum logic-high and maximum logic-low voltage specifications, respectively. NXP devices are typically better than guaranteed specifications; these values are shown in the diagram as “typ”. Nominally, lower voltages than the guaranteed specification are accepted by the device as logic high and higher voltages than the guaranteed specification are accepted as logic low.

4.6.3 General Purpose I/O (GPIO) AC Parameters

Table 40. General Purpose I/O AC Parameters[1]

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
1.8 V application[2]						
f_{max}	Maximum frequency	Load = 21 pF (PDRV = L, high drive, 33 Ω	—	—	208	MHz
		Load = 15 pF (PDRV = H, low drive, 50 Ω				
tr	Rise time	Measured between V_{OL} and V_{OH}	0.4	—	1.32	ns
tf	Fall time	Measured between V_{OH} and V_{OL}	0.4	—	1.32	ns
Driver 3.3 V application[3]						
f_{max}	Maximum frequency	Load = 30 pF	—	—	52	MHz

Table 40. General Purpose I/O AC Parameters[1] (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
tr	Rise time	Measured between V_{OL} and V_{OH}	—	—	3	ns
tf	Fall time	Measured between V_{OH} and V_{OL}	—	—	3	ns

1 All output I/O specifications are guaranteed for Accurate mode of the compensation cell operation. This is applicable for both DC and AC specifications.

2 All timing specifications in 1.8 V application are valid for High Drive mode (PDRV = L). In Low Drive mode (PDRV = H), the driver is functional.

3 All timing specifications in 3.3 V application are valid for Low Drive only. For High Drive setting, the driver is functional.

Table 41. Dynamic input characteristics

Symbol	Parameter	Condition[1,2]	Min	Max	Unit
Dynamic Input Characteristics for 3.3 V Application					
f_{op}	Input frequency of operation	—	—	52	MHz
INPSL	Slope of input signal at I/O	Measured between 10% to 90% of the I/O swing	—	3.5	ns
Dynamic Input Characteristics for 1.8 V Application					
f_{op}	Input frequency of operation	—	—	208	MHz
INPSL	Slope of input signal at I/O	Measured between 10% to 90% of the I/O swing	—	1.5	ns

1 For all supply ranges of operation.

2 The dynamic input characteristic specifications are applicable for the digital bidirectional cells.

4.7 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters for the following I/O types:

- General Purpose I/O (GPIO) output buffer impedance
- Double Data Rate I/O (DDR) output buffer impedance for LPDDR4

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 8).

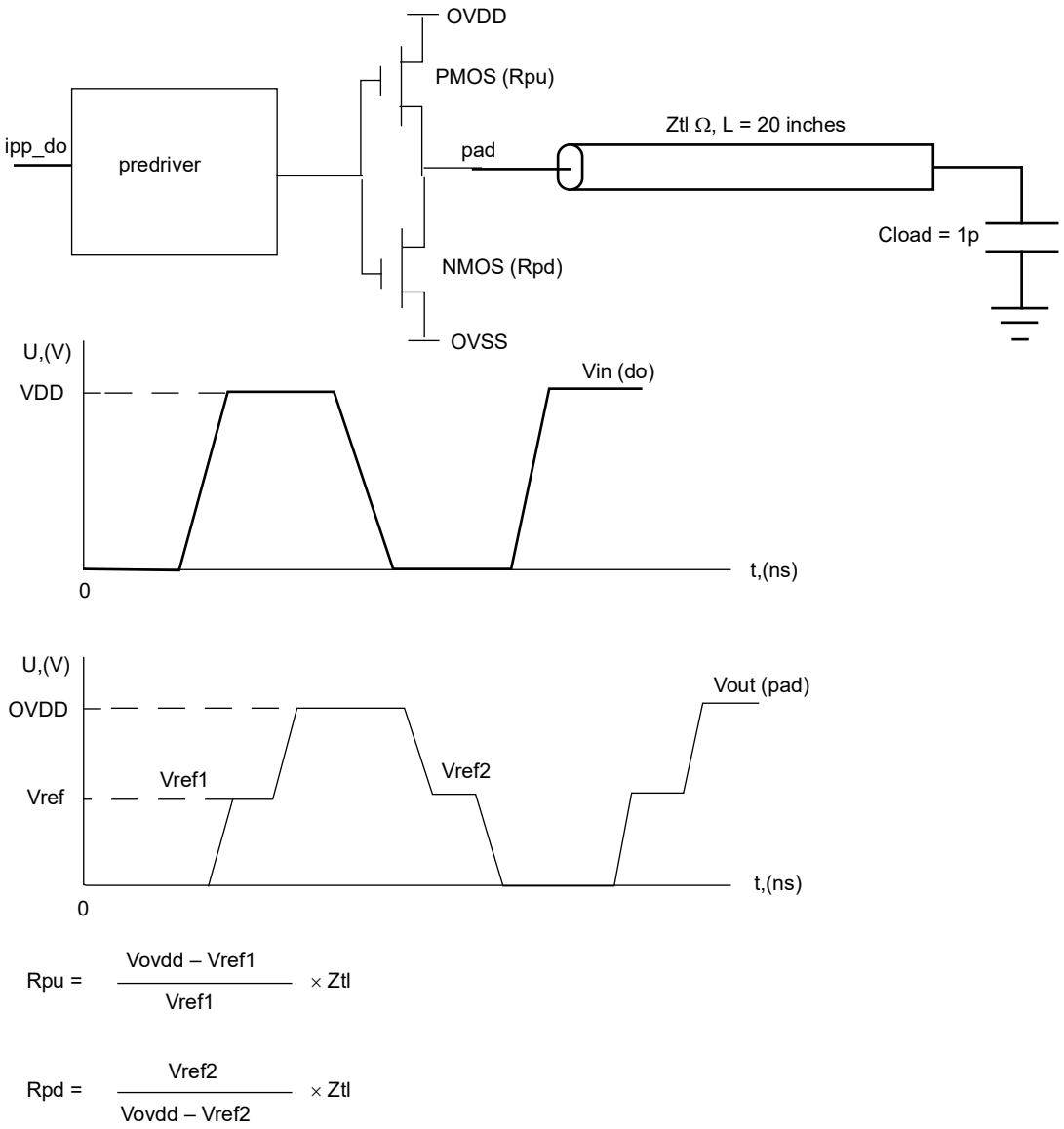

Figure 8. Impedance Matching Load for Measurement

4.7.1 GPIO output buffer impedance

4.7.1.1 Tri-voltage GPIO output buffer impedance

Table 42. Tri-voltage 1.8 V GPIO output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1]DSE=0	33	Ω
Output impedance	Z_O	[1]DSE=1	50	Ω

[1] As programmed in the associated IOMUX (PDRV field) register.

Table 43. Tri-voltage 2.5 V GPIO output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1]DSE=0	25	Ω
Output impedance	Z_O	[1]DSE=1	33	Ω

[1] As programmed in the associated IOMUX (PDRV field) register.

Table 44. Tri-voltage 3.3 V GPIO output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1]DSE=0	25	Ω
Output impedance	Z_O	[1]DSE=1	37	Ω

[1] As programmed in the associated IOMUX (PDRV field) register.

4.7.1.2 Dual-voltage GPIO output buffer impedance

Table 45. Dual-voltage 1.8 V GPIO output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1]DSE=0	33	Ω
Output impedance	Z_O	[1]DSE=1	50	Ω

[1] ‘As programmed in the associated IOMUX (PDRV field) register.

Table 46. Dual-voltage 3.3 V GPIO output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1]DSE=0	25	Ω
Output impedance	Z_O	[1]DSE=1	37	Ω

[1] As programmed in the associated IOMUX (PDRV field) register.

4.7.1.3 Single-voltage 1.8 V GPIO output buffer drive strength

The following table shows the GPIO output buffer drive strength (OVDD 1.8 V).

Table 47. Single-voltage GPIO 1.8 V output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1]DSE=000	200	Ω
		[1]DSE=001	100	
		[1]DSE=010	55	
		[1]DSE=011	40	
		[1]DSE=100	30	
		[1]DSE=101	24	
		[1]DSE=110	20	
		[1]DSE=111	18	

1 As programmed in the associated IOMUX (DSE field) register.

4.7.1.4 Single-voltage 3.3 V GPIO output buffer drive strength

The following table shows the GPIO output buffer drive strength (OVDD 3.3 V).

Table 48. Single-voltage GPIO 3.3 V output impedance DC parameters

Parameter	Symbol	Test conditions	Typical	Units
Output impedance	Z_O	[1]DSE=00	400	Ω
		[1]DSE=01	200	
		[1]DSE=10	100	
		[1]DSE=11	50	

1 As programmed in the associated IOMUX (DSE field) register.

4.7.2 DDR I/O output buffer impedance

The following tables show LPDDR4 I/O output buffer impedance of the device.

The ZQ Calibration cell uses a single register (ZQnPR0) to determine the target output buffer impedances of the pull-up driver and the pull-down driver, as well as the target on-die termination impedance. The resulting calibration setting is then applied to all DDR pads within the PHY complex.

Table 49 shows the recommended ZQnPR0 field settings for the LPDDR4 I/Os to achieve the desired output buffer impedances.

Table 49. LPDDR4 I/O output buffer impedance

Parameter	Typical			
	ZQnPR0 ZPROG_ASYM_PU_DRV	Impedance	ZQnPR0 ZPROG_ASYM_PD_DRV	Impedance
Recommended combinations for DQ /CA pins	5	80 Ω	3	120 Ω
	7	60 Ω	5	80 Ω
	9	48 Ω	7	60 Ω
	11	40 Ω	9	48 Ω

Table 50. LPDDR4 I/O on-die termination impedance

Parameter	Typical Impedance	ZQnPR0. ZPROG_HOST_ODT
Recommended combinations for DQ/CA pins	120.0 Ω	3
	80.0 Ω	5
	60.0 Ω	7
	48.0 Ω	9
	40.0 Ω	11

4.8 System Modules Timing

This section contains the timing and electrical parameters for the modules in each processor.

4.8.1 Reset Timing Parameters

The following figure shows the reset timing and Table 51 lists the timing parameters.

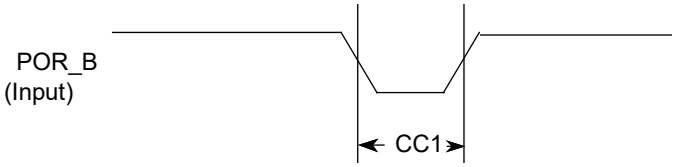

Figure 9. Reset timing diagram

Table 51. Reset timing parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of SRC_POR_B to be qualified as valid	1	—	XTALOSC_RTC_ XTALI cycle

4.8.2 WDOG reset timing parameters

The following figure shows the WDOG reset timing and Table 52 lists the timing parameters.

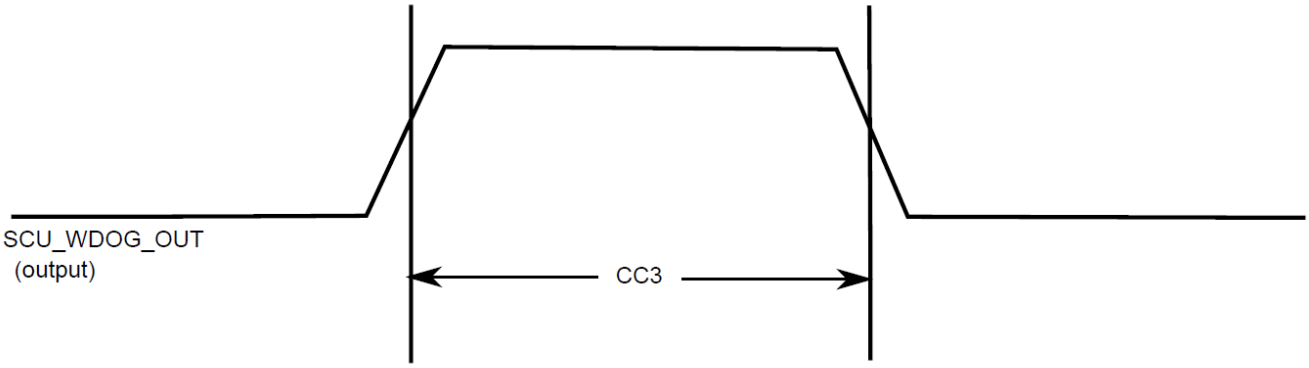

Figure 10. SCU_WDOG_OUT timing diagram

Table 52. WDOG1_B timing parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of SCU_WDOG_OUT assertion	1	—	XTALOSC_RTC_ XTALI cycle

NOTE

XTALOSC_RTC_XTALI is approximately 32 kHz.
XTALOSC_RTC_XTALI cycle is one period or approximately 30 µs.

4.8.3 DDR SDRAM–specific parameters (LPDDR4)

The i.MX 8 Family of processors have been designed and tested to work with JEDEC JESD209-4A–compliant LPDDR4 memory . Timing diagrams and tolerances required to work with these memories are specified in the respective documents and are not reprinted here.

Meeting the necessary timing requirements for a DDR memory system is highly dependent on the components chosen and the design layout of the system as a whole. NXP cannot cover in this document all the requirements needed to achieve a design that meets full system performance over temperature, voltage, and part variation; PCB trace routing, PCB dielectric material, number of routing layers used, placement of bulk/decoupling capacitors on critical power rails, VIA placement, GND and Supply planes layout, and DDR controller/PHY register settings all are factors affecting the performance of the memory system. Consult the hardware user guide for this device and NXP validated design layouts for information on how to properly design a PCB for best DDR performance. NXP strongly recommends duplicating an NXP validated design as much as possible in the design of critical power rails, placement of bulk/decoupling capacitors and DDR trace routing between the processor and the selected DDR memory. All supporting material is readily available on the device web page on https://www.nxp.com/products/processors-and-microcontrollers/applications-processors/i.mx-applications-processors/i.mx-8-processors:IMX8-SERIES .

Processors that demonstrate full DDR performance on NXP validated designs, but do not function on customer designs, are not considered marginal parts. A report detailing how the returned part behaved on an NXP validated system will be provided to the customer as closure to a customer's reported DDR issue. Customers bear the responsibility of properly designing the Printed Circuit Board, correctly simulating and modeling the designed DDR system, and validating the system under all expected operating conditions (temperatures, voltages) prior to releasing their product to market.

Table 53. i.MX 8 Family DRAM controller supported SDRAM configurations

Parameter	LPDDR4
Number of Controllers	2
Number of Channels	2 per controller
Number of Chip Selects	2 per channel
Bus Width	16 bit per channel[1]
Number of Address Rows	16 (R0-R15)
Maximum Clock Frequency	1600 MHz

[1] Only 16-bit external memory configurations are supported.

4.8.3.1 Clock/data/command/address pin allocations

These processors uses generic names for clock, data and command address bus (DCF—DRAM controller functions); the following table provides mapping of clock, data and command address signals for LPDDR4 modes.

Table 54. Clock, data, and command address signals for LPDDR4 modes

Signal name	LPDDR4
DDR_CH[1:0].CK0_P	CK_t_A
DDR_CH[1:0].CK0_N	CK_c_A
DDR_CH[1:0].CK1_P	CK_t_B
DDR_CH[1:0].CK1_N	CK_c_B
DDR_CH[1:0].DQ_[15:0]	DQ[15:0]_A
DDR_CH[1:0].DQ_[31:16]	DQ[15:0]_B
DDR_CH[1:0].DQS_N_[3:0]	DQS_N_[3:0]
DDR_CH[1:0].DQS_P_[3:0]	DQS_P_[3:0]
DDR_CH[1:0].DM_[3:0]	DM_[3:0]
DDR_CH[1:0].DCF00	CA2_A
DDR_CH[1:0].DCF01	CA4_A
DDR_CH[1:0].DCF02	
DDR_CH[1:0].DCF03	CA5_A
DDR_CH[1:0].DCF04	
DDR_CH[1:0].DCF05	
DDR_CH[1:0].DCF06	
DDR_CH[1:0].DCF07	
DDR_CH[1:0].DCF08	CA3_A
DDR_CH[1:0].DCF09	ODT_CA_A
DDR_CH[1:0].DCF10	CS0_A
DDR_CH[1:0].DCF11	CA0_A
DDR_CH[1:0].DCF12	CS1_A
DDR_CH[1:0].DCF13	
DDR_CH[1:0].DCF14	CKE0_A
DDR_CH[1:0].DCF15	CKE1_A
DDR_CH[1:0].DCF16	CA1_A
DDR_CH[1:0].DCF17	CA4_B
DDR_CH[1:0].DCF18	RESET_N
DDR_CH[1:0].DCF19	CA5_B
DDR_CH[1:0].DCF20	
DDR_CH[1:0].DCF21	
DDR_CH[1:0].DCF22	

Table 54. Clock, data, and command address signals for LPDDR4 modes (continued)

Signal name	LPDDR4
DDR_CH[1:0].DCF23	
DDR_CH[1:0].DCF24	
DDR_CH[1:0].DCF25	ODT_CA_B
DDR_CH[1:0].DCF26	CA3_B
DDR_CH[1:0].DCF27	CA0_B
DDR_CH[1:0].DCF28	CS0_B
DDR_CH[1:0].DCF29	CS1_B
DDR_CH[1:0].DCF30	CKE0_B
DDR_CH[1:0].DCF31	CKE1_B
DDR_CH[1:0].DCF32	CA1_B
DDR_CH[1:0].DCF33	CA2_B

4.9 General-Purpose Media Interface (GPMI) Timing

The GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 400 MB/s I/O speed, and individual chip select. It supports Asynchronous Timing mode, Source Synchronous Timing mode, and Toggle Timing mode, as described in the following subsections.

4.9.1 GPMI Asynchronous mode AC timing (ONFI 1.0 compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 11 through Figure 14 depict the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 55 describes the timing parameters (NF1–NF17) that are shown in the figures.

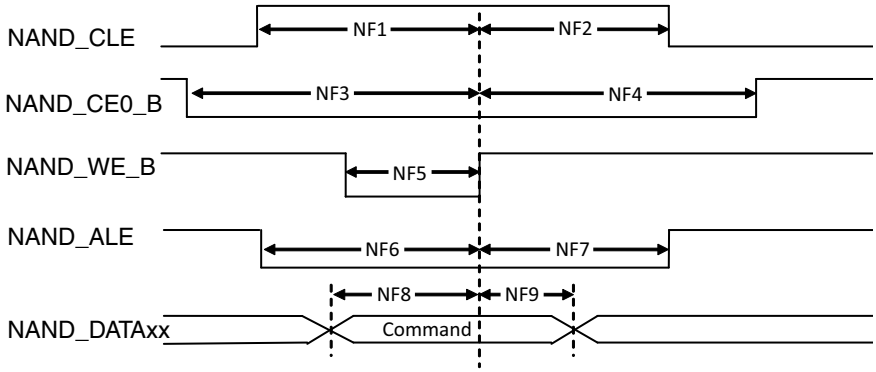

Figure 11. Command Latch Cycle Timing Diagram

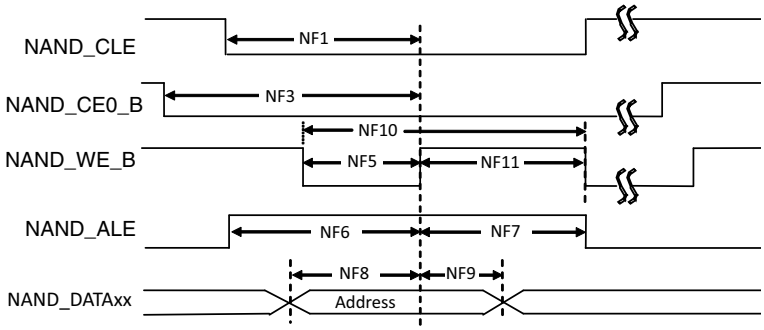

Figure 12. Address Latch Cycle Timing Diagram

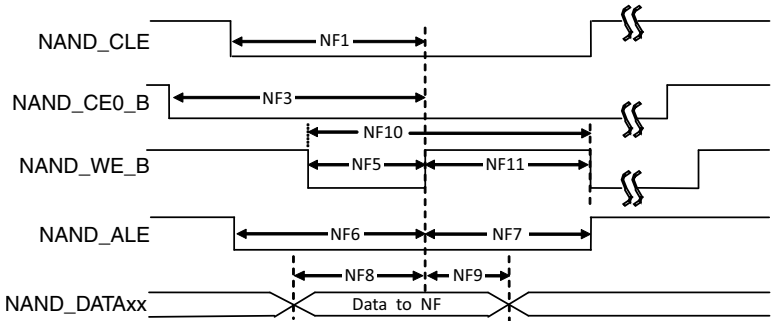

Figure 13. Write Data Latch Cycle Timing Diagram

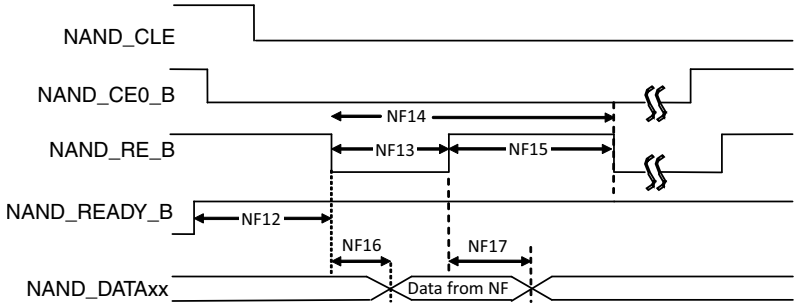

Figure 14. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

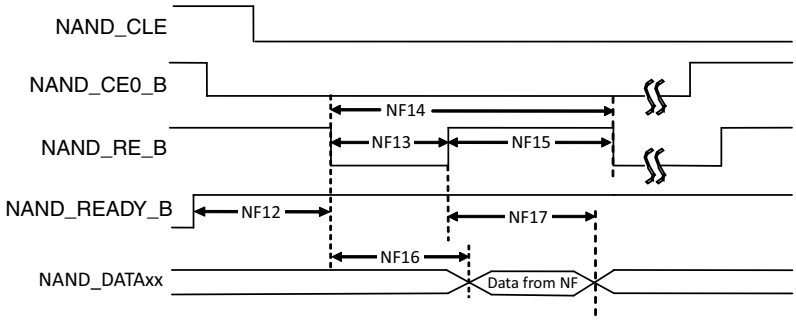

Figure 15. Read Data Latch Cycle Timing Diagram (EDO Mode)

Table 55. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see 2,3]		ns
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see 2]		ns
NF3	NAND_CEx_B setup time	tCS	(AS + DS + 1) × T [see 3,2]		ns
NF4	NAND_CEx_B hold time	tCH	(DH+1) × T - 1 [see 2]		ns
NF5	NAND_WE_B pulse width	tWP	DS × T [see 2]		ns
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see 3,2]		ns
NF7	NAND_ALE hold time	tALH	(DH × T - 0.42 [see 2]		ns
NF8	Data setup time	tDS	DS × T - 0.26 [see 2]		ns
NF9	Data hold time	tDH	DH × T - 1.37 [see 2]		ns
NF10	Write cycle time	tWC	(DS + DH) × T [see 2]		ns
NF11	NAND_WE_B hold time	tWH	DH × T [see 2]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	(AS + 2) × T [see 3,2]	—	ns
NF13	NAND_RE_B pulse width	tRP	DS × T [see 2]		ns
NF14	READ cycle time	tRC	(DS + DH) × T [see 2]		ns
NF15	NAND_RE_B high hold time	tREH	DH × T [see 2]		ns

Table 55. Asynchronous Mode Timing Parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF16	Data setup on read	tDSR	—	(DS × T -0.67)/18.38 [see [5,6]]	ns
NF17	Data hold on read	tDHR	0.82/11.83 [see [5,6]]	—	ns

1 The GPMI asynchronous mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = GPMI clock period -0.075ns (half of maximum p-p jitter).

4 NF12 is met automatically by the design.

5 Non-EDO mode.

6 EDO mode, GPMI clock ≈ 100 MHz
(AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 15), NF16/NF17 are different from the definition in non-EDO mode (Figure 14). They are called tREA/tRHOH (NAND_RE_B access time/NAND_RE_B HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the device reference manual. The typical value of this control register is 0x8 at 50 MT/s EDO mode. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.9.2 GPMI Source Synchronous mode AC timing (ONFI 2.x compatible)

The following figure shows the write and read timing of Source Synchronous mode.

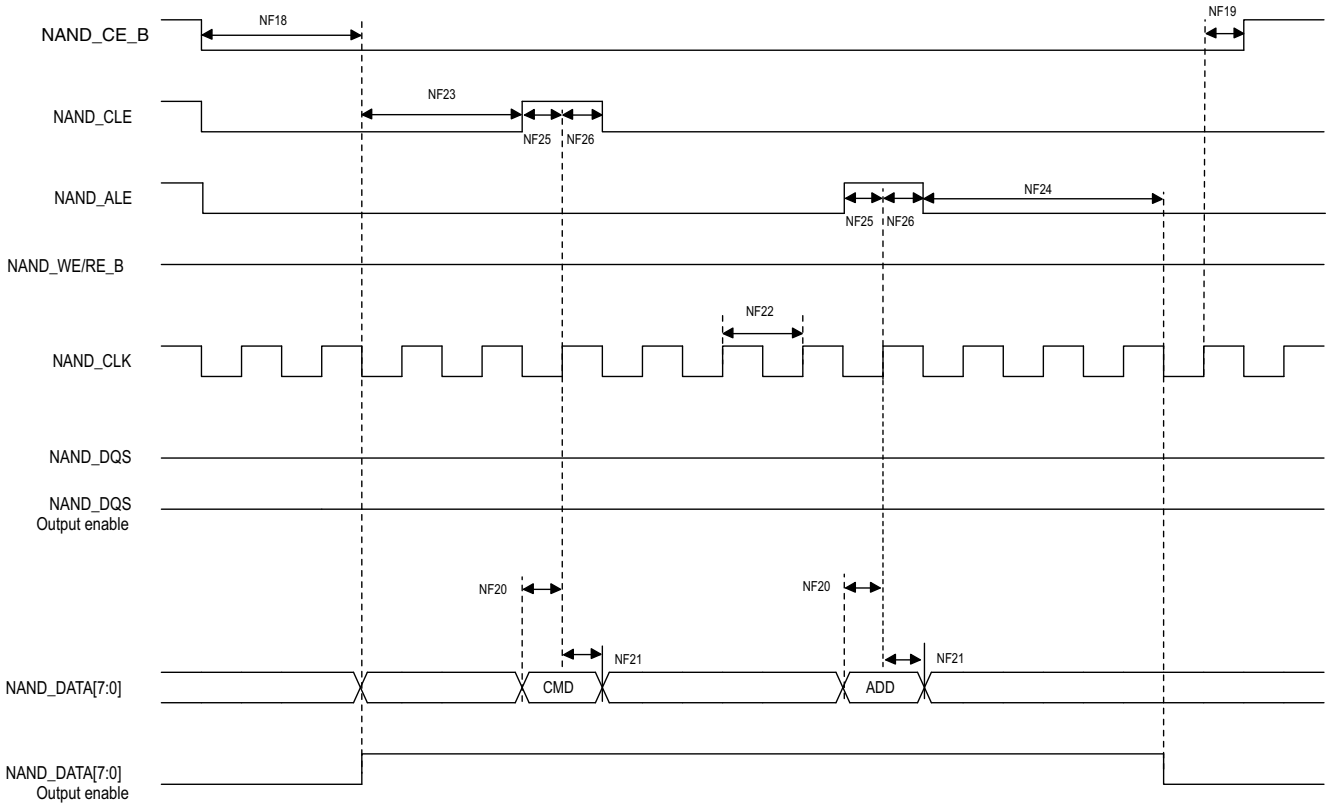

Figure 16. Source Synchronous Mode Command and Address Timing Diagram

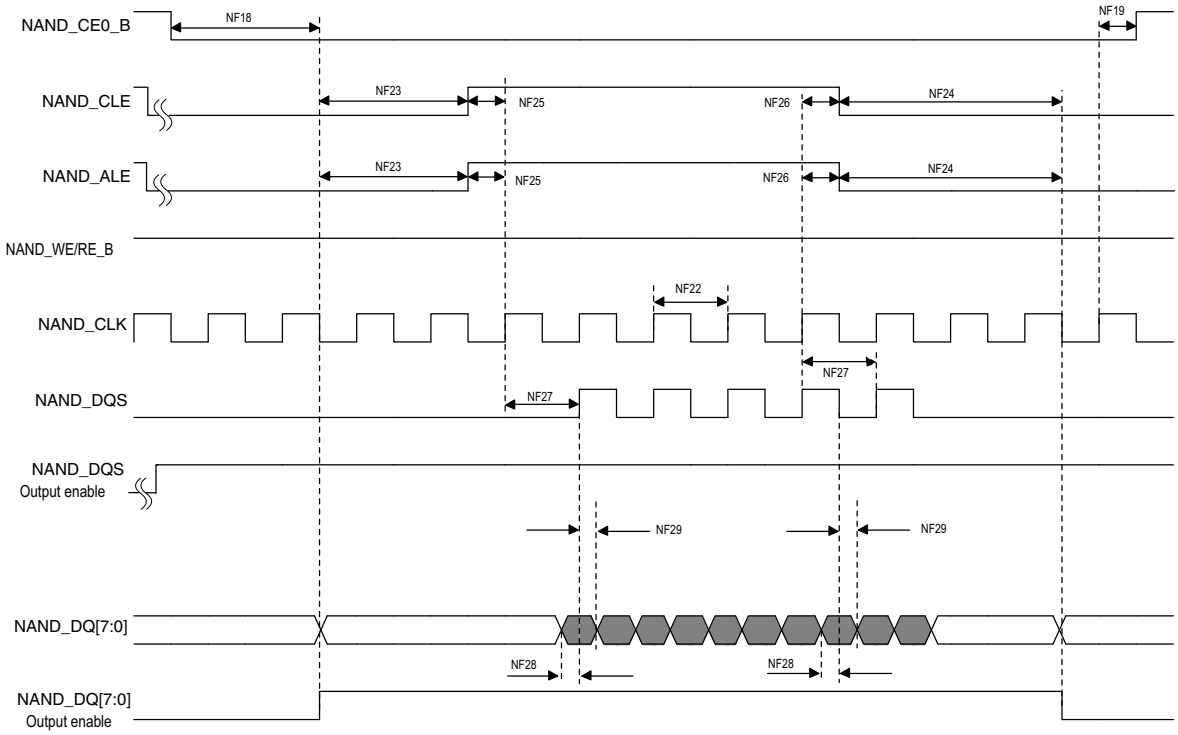

Figure 17. Source Synchronous Mode Data Write Timing Diagram

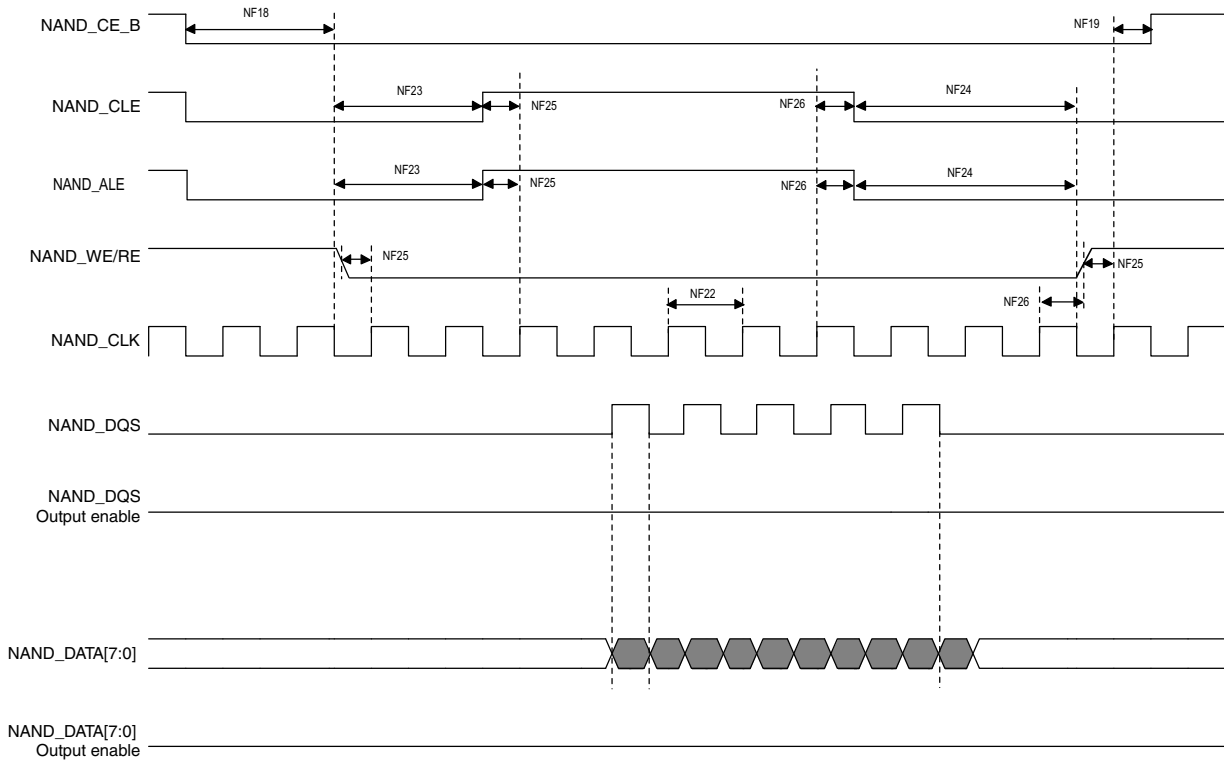

Figure 18. Source Synchronous Mode Data Read Timing Diagram

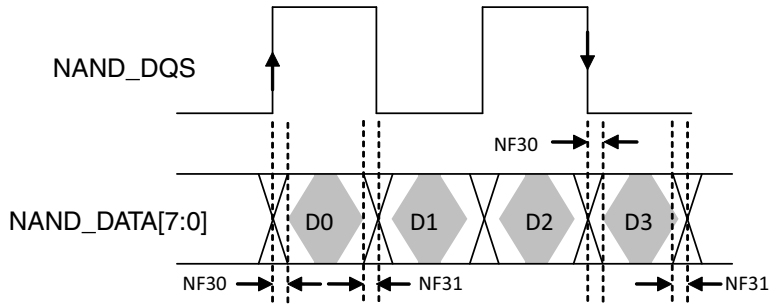

Figure 19. NAND_DQS/NAND_DQ Read Valid Window

Table 56. Source Synchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min	Max	
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T - 0.79 [see 2]		ns
NF19	NAND_CEx_B hold time	tCH	0.5 × tCK - 0.63 [see 2]		ns
NF20	Command/address NAND_DATAxx setup time	tCAS	0.5 × tCK - 0.05		ns
NF21	Command/address NAND_DATAxx hold time	tCAH	0.5 × tCK - 1.23		ns
NF22	clock period	tCK	—		ns
NF23	preamble delay	tPRE	PRE_DELAY × T - 0.29 [see 2]		ns
NF24	postamble delay	tPOST	POST_DELAY × T - 0.78 [see 2]		ns
NF25	NAND_CLE and NAND_ALE setup time	tCALS	0.5 × tCK - 0.86		ns
NF26	NAND_CLE and NAND_ALE hold time	tCALH	0.5 × tCK - 0.37		ns
NF27	NAND_CLK to first NAND_DQS latching transition	tDQSS	T - 0.41 [see 2]		ns
NF28	Data write setup	tDS	0.25 × tCK - 0.35		ns
NF29	Data write hold	tDH	0.25 × tCK - 0.85		ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ	—	2.06	—
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS	—	1.95	—

1 The GPMI source synchronous mode output timing can be controlled by the module's internal registers GPMI_TIMING2_CE_DELAY, GPMI_TIMING_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers settings. In the table, CE_DELAY/PRE_DELAY/POST_DELAY represents each of these settings.

2 T = tCK (GPMI clock period) -0.075ns (half of maximum p-p jitter).

Figure 19 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. For Source Synchronous mode, the typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of a delayed NAND_DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the device reference manual. Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. However, if the board delay is large enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.9.3 ONFI NV-DDR2 mode (ONFI 3.2 compatible)

4.9.3.1 Command and address timing

ONFI 3.2 mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.9.1, “GPMI Asynchronous mode AC timing (ONFI 1.0 compatible)",” for details.

4.9.3.2 Read and write timing

ONFI 3.2 mode read and write timing is the same as Toggle mode AC timing. See Section 4.9.4, “Toggle mode AC Timing",” for details.

4.9.4 Toggle mode AC Timing

4.9.4.1 Command and address timing

NOTE

Toggle mode command and address timing is the same as ONFI 1.0 compatible Asynchronous mode AC timing. See Section 4.9.1, “GPMI Asynchronous mode AC timing (ONFI 1.0 compatible)",” for details.

4.9.4.2 Read and write timing

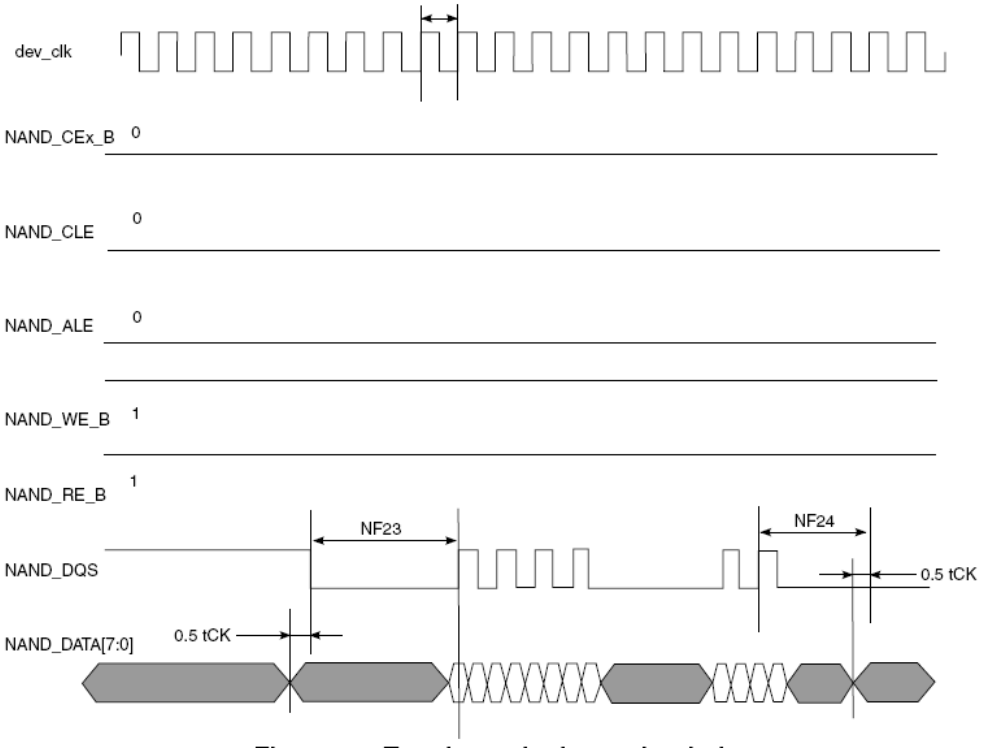

Figure 20. Toggle mode data write timing

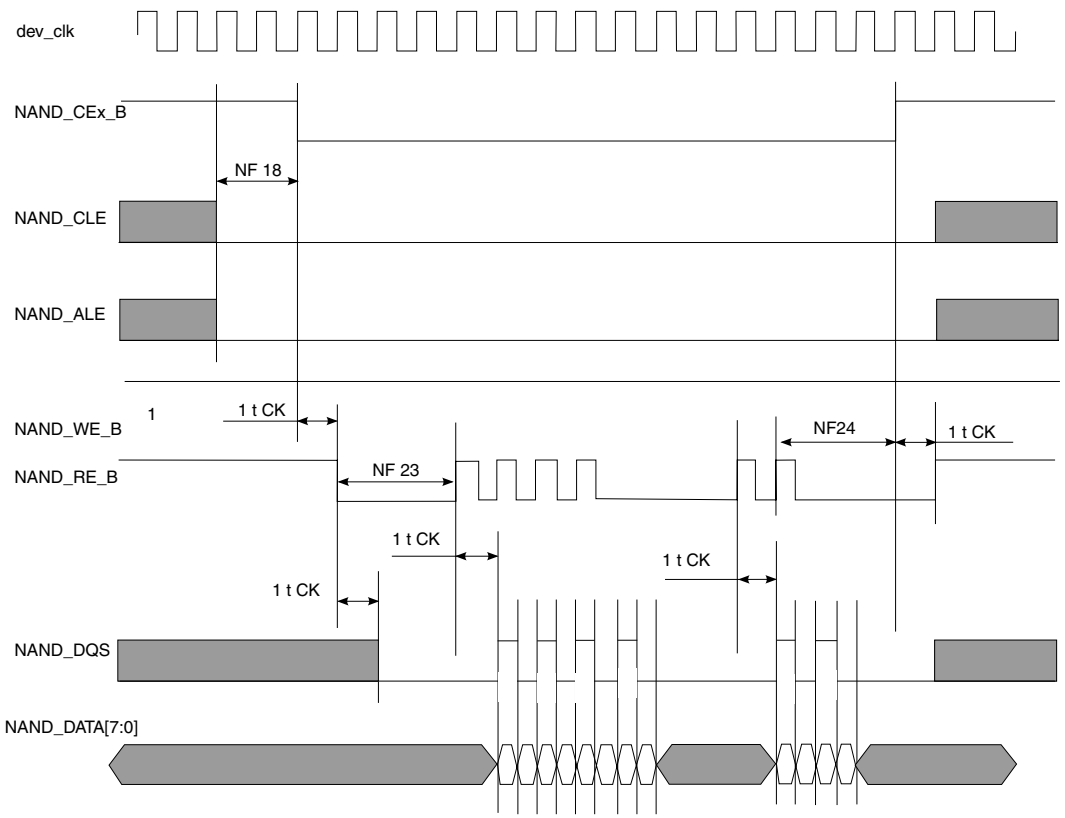

Figure 21. Toggle mode data read timing

Table 57. Toggle mode timing parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF1	NAND_CLE setup time	tCLS	(AS + DS) × T - 0.12 [see note[2]s[,3]]		
NF2	NAND_CLE hold time	tCLH	DH × T - 0.72 [see note[2]]		
NF3	NAND_CE0_B setup time	tCS	(AS + DS) × T - 0.58 [see notes[,2]]		
NF4	NAND_CE0_B hold time	tCH	DH × T - 1 [see note[2]]		
NF5	NAND_WE_B pulse width	tWP	DS × T [see note[2]]		
NF6	NAND_ALE setup time	tALS	(AS + DS) × T - 0.49 [see notes[,2]]		
NF7	NAND_ALE hold time	tALH	DH × T - 0.42 [see note[2]]		
NF8	Command/address NAND_DATAxx setup time	tCAS	DS × T - 0.26 [see note[2]]		
NF9	Command/address NAND_DATAxx hold time	tCAH	DH × T - 1.37 [see note[2]]		
NF18	NAND_CEx_B access time	tCE	CE_DELAY × T [see notes[4,2]]	—	ns
NF22	clock period	tCK	—	—	ns
NF23	preamble delay	tPRE	PRE_DELAY × T [see notes[5,2]]	—	ns
NF24	postamble delay	tPOST	POST_DELAY × T +0.43 [see note[2]]	—	ns

Table 57. Toggle mode timing parameters[1] (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF28	Data write setup	tDS[6]	0.25 × tCK - 0.32	—	ns
NF29	Data write hold	tDH[6]	0.25 × tCK - 0.79	—	ns
NF30	NAND_DQS/NAND_DQ read setup skew	tDQSQ[7]	—	3.18	
NF31	NAND_DQS/NAND_DQ read hold skew	tQHS[7]	—	3.27	

1 The GPMI toggle mode output timing can be controlled by the module's internal registers HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

2 AS minimum value can be 0, while DS/DH minimum value is 1.

3 T = tCK (GPMI clock period) -0.075 ns (half of maximum p-p jitter).

4 CE_DELAY represents HW_GPMI_TIMING2[CE_DELAY]. NF18 is guaranteed by the design. Read/Write operation is started with enough time of ALE/CLE assertion to low level.

5 PRE_DELAY+1) ≥ (AS+DS)

6 Shown in Figure 20.

7 Shown in Figure 21.

For DDR Toggle mode, Figure 21 shows the timing diagram of NAND_DQS/NAND_DATAxx read valid window. The typical value of tDQSQ is 1.4 ns (max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample NAND_DATA[7:0] at both rising and falling edge of an delayed NAND_DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the device reference manual. Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.10 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.10.1 LPSPI timing parameters

All LPSPI interfaces do not have the same maximum serial clock frequency. There are two groups. LPSPI interfaces which can operate at 60 MHz in Master mode and 40 MHz in Slave mode and the other group where interfaces operate at 40 MHz in Master mode and 20 MHz in Slave mode. The same performance is achieved at 1.8 V and 3.3 V unless otherwise stated.

Below are the LPSPI interfaces and their respective chip selects:

Table 58. LPSPI interfaces and chip selects

LPSPI interface	Chip select	Comment
60 MHz in Master mode and 40 MHz in Slave mode	SPI0, SPI1, SPI2, SPI3 (primary mode)	SPI1 is muxed behind ADC pins so it operates at 1.8 V only.
40 MHz in Master mode and 20 MHz in Slave mode	SPI3b (behind UART1)	—

4.10.1.1 LPSPI Master mode

Waveform is assuming LPSPI is configured in mode 0, i.e. TCR.CPOL=0b0 and TCR.CPHA=0b0. Timing parameters are valid for all modes using appropriate edge of the clock.

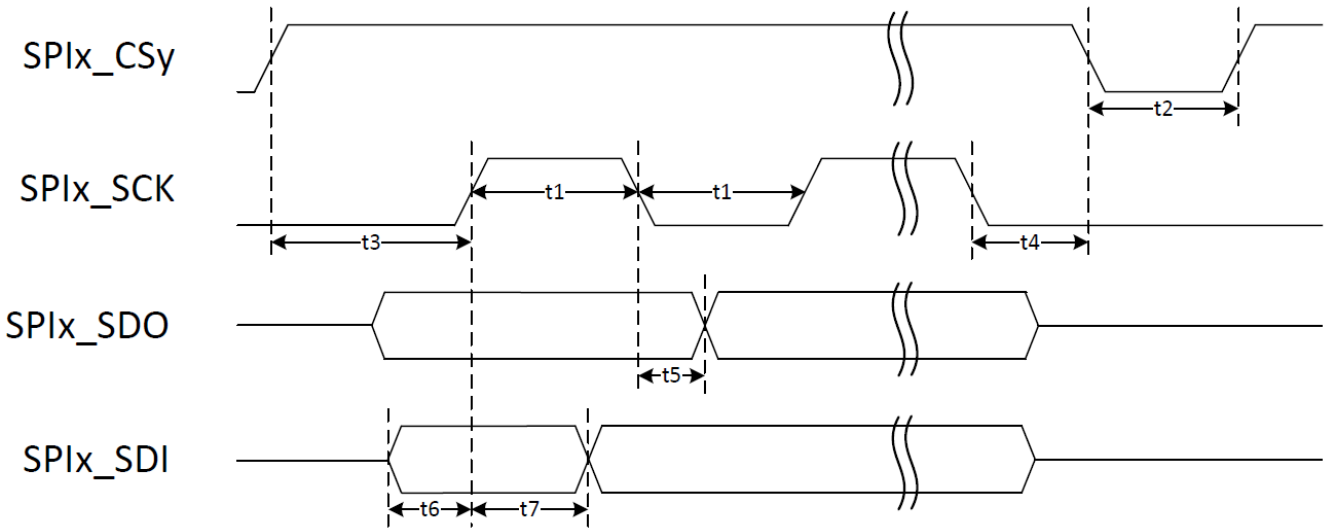

Figure 22. LPSPI Master mode

Table 59. LPSPI timings—Master mode at 60 MHz

ID	Parameter	Min	Max	Unit
—	SPIx_SCLK Cycle frequency	—	60	MHz
t1	SPIx_SCLK High or Low Time–Read SPIx_SCLK High or Low Time–Write	7.5	—	ns
t2	SPIx_CSy pulse width	7.5	—	ns
t3	SPIx_CSy Lead Time(1)	FCLK_PERIOD(2) x (PCSSCK + 1) / $2^{PRESCALE}$ - 3	—	ns
t4	SPIx_CSy Lag Time(3)	FCLK_PERIOD(2) x (SCKPCS + 1) / $2^{PRESCALE}$ + 3	—	ns

Table 59. LPSPI timings—Master mode at 60 MHz (continued)

ID	Parameter	Min	Max	Unit
t5	SPIx_SDO output Delay (CLOAD = 20 pF)	—	3	ns
t6	SPIx_SDI Setup Time	2	—	ns
t7	SPIx_SDI Hold Time	2	—	ns

1 This timing is controllable through CCR.PCSSCK and TCR.PRESCALE registers.

2 FCLK_PERIOD is the period of the functional clock provided to LPSPI module. Maximum allowed frequency is 240 MHz.

3 This timing is controllable through CCR.SCKPCS and TCR.PRESCALE registers.

Table 60. LPSPI timings—Master mode at 40 MHz

ID	Parameter	Min	Max	Unit
—	SPIx_SCLK Cycle frequency	—	40	MHz
t1	SPIx_SCLK High or Low Time–Read SPIx_SCLK High or Low Time–Write	11	—	ns
t2	SPIx_CSy pulse width	11	—	ns
t3	SPIx_CSy Lead Time(1)	FCLK_PERIOD(2) x (PCSSCK + 1) / $2^{PRESCALE}$ + 3	—	ns
t4	SPIx_CSy Lag Time(3)	FCLK_PERIOD(2) x (SCKPCS + 1) / $2^{PRESCALE}$ + 3	—	ns
t5	SPIx_SDO output Delay (CLOAD = 20 pF)	—	5	ns
t6	SPIx_SDI Setup Time	5	—	ns
t7	SPIx_SDI Hold Time	4	—	ns

1 This timing is controllable through CCR.PCSSCK and TCR.PRESCALE registers.

2 FCLK_PERIOD is the period of the functional clock provided to LPSPI module. Maximum allowed frequency is 240 MHz.

3 This timing is controllable through CCR.SCKPCS and TCR.PRESCALE registers.

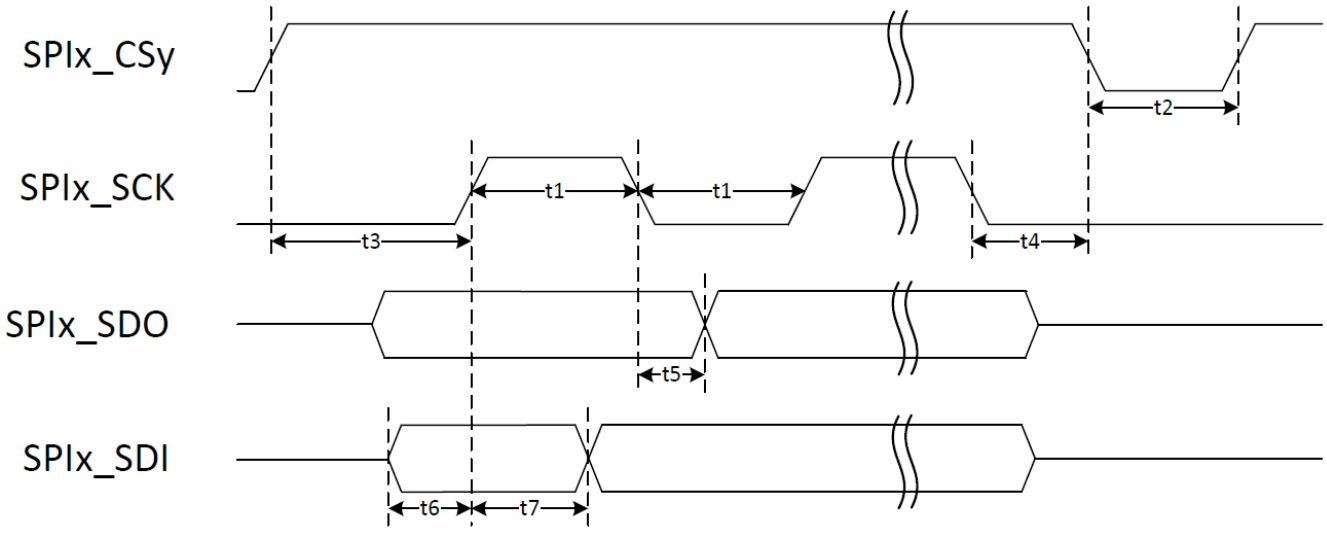

Figure 23. LPSPI Slave mode

Table 61. LPSPI timings—Slave mode at 40 MHz

ID	Parameter	Min	Max	Unit
—	SPI*x*_SCLK Cycle frequency	—	40	MHz
t1	SPI*x*_SCLK High or Low Time–Read SPI*x*_SCLK High or Low Time–Write	11	—	ns
t2	SPI*x*_CSy pulse width	11	—	ns
t3	SPI*x*_CSy Lead Time (CS setup time)	4	—	ns
t4	SPI*x*_CSy Lag Time (CS hold time)	2	—	ns
t5	SPI*x*_SDO output Delay (CLOAD = 20 pF)	—	5	ns
t6	SPI*x*_SDI Setup Time	2	—	ns
t7	SPI*x*_SDI Hold Time	2	—	ns

Table 62. LPSPI timings—Slave mode at 20 MHz

ID	Parameter	Min	Max	Unit
—	SPI*x*_SCLK Cycle frequency	—	20	MHz
t1	SPI*x*_SCLK High or Low Time–Read SPI*x*_SCLK High or Low Time–Write	22	—	ns
t2	SPI*x*_CSy pulse width	22	—	ns
t3	SPI*x*_CSy Lead Time (CS setup time)	4	—	ns

Table 62. LPSPI timings—Slave mode at 20 MHz (continued)

ID	Parameter	Min	Max	Unit
t4	SPI*x*_CSy Lag Time (CS hold time)	2	—	ns
t5	SPI*x*_SDO output Delay (CLOAD = 20 pF)	—	18	ns
t6	SPI*x*_SDI Setup Time	2	—	ns
t7	SPI*x*_SDI Hold Time	2	—	ns

4.10.2 Serial audio interface (SAI) timing parameters

The timings and figures in this section are valid for noninverted clock polarity (I2S_TCR2.BCP = 0b0, I2S_RCR2.BCP = 0b0) and non-inverted frame sync polarity (I2S_TCR4.FSP = 0b0, I2S_RCR4.FSP = 0b0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_TXC / SAI_RXC) and/or the frame sync (SAI_TXFS / SAI_RXFS) shown in the figures below.

The same performance is achieved at both 1.8 V and 3.3 V unless otherwise stated.

NOTE

SAI0 and SAI1 are transmit/receive capable. SAI2 and SAI3 are receive only.

4.10.2.1 SAI Master Synchronous mode

In this mode, transmitter clock and frame sync are used by both transmitter and receiver (I2S_TCR2.SYNC=0b00, I2S_RCR2.SYNC=0b01). In that case, SAI interface requires only 4 signals to be routed: SAI_TXC, SAI_TXFS, SAI_TXD and SAI_RXD. SAI_RXC and SAI_RXFS can be left unconnected. I2S_RCR2.BCI shall be set to 0b1 to get setup and hold times provided in Table 63.

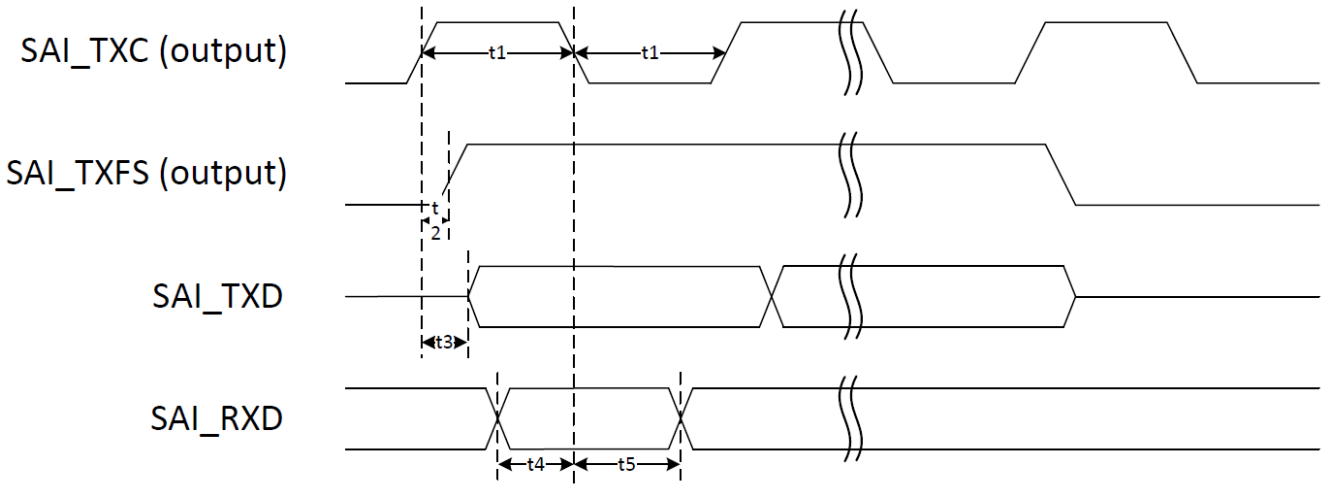

Figure 24. SAI Master Synchronous mode

Table 63. SAI timings—Master Synchronous mode

ID	Parameters	Min	Max	Unit
—	SAI TXC clock frequency	—	49.152	MHz
t1	SAI TXC pulse width low / high	45%	55%	SAI_TXC period
t2	SAI TXFS output valid	—	2	ns
t3	SAI TXD output valid	—	2	ns
t4	SAI RXD input setup	1	—	ns
t5	SAI RXD input hold	4	—	ns

4.10.2.2 SAI Master mode

In this mode, transmitter and/or receiver part are set to bring out transmit and/or receive clock. Frame sync can be either input or output.

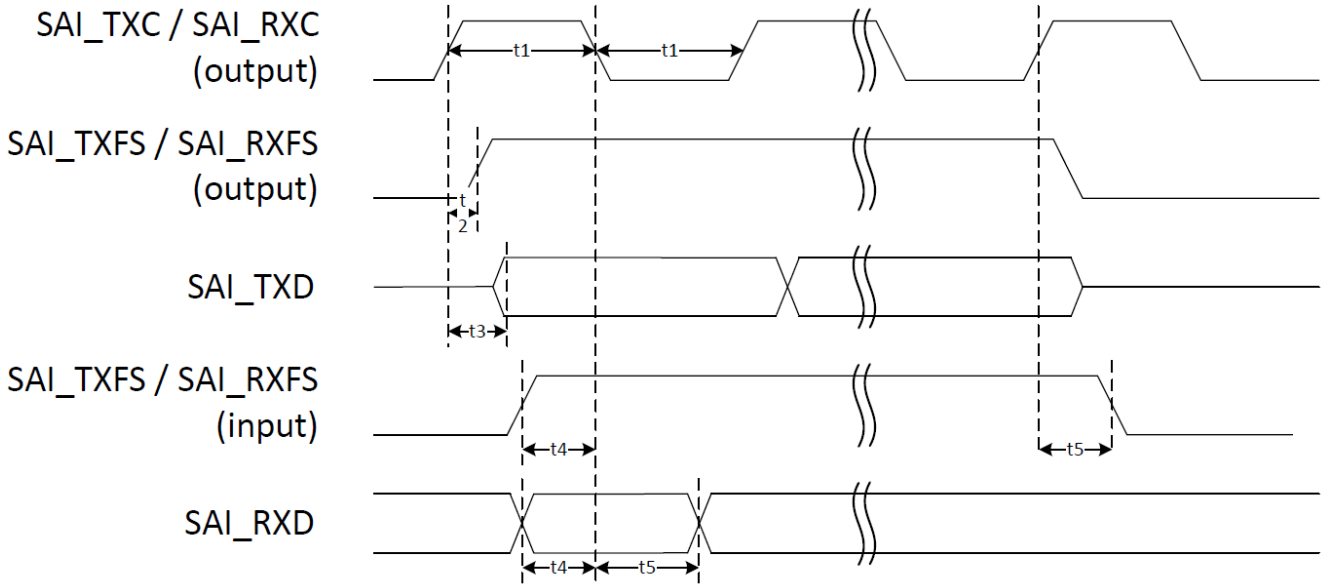

Figure 25. SAI Master mode

Table 64. SAI timings—Master mode

ID	Parameters	Min	Max	Unit
—	SAI TXC / RXC clock frequency[1]	—	49.152	MHz
t1	SAI TXC / RXC pulse width low / high	45%	55%	TXC/RXC period
t2	SAI TXFS / RXFS output valid	—	2	ns

Table 64. SAI timings—Master mode (continued)

ID	Parameters	Min	Max	Unit
t3	SAI TXD output valid	—	2	ns
t4	SAI RXD/RXFS/TXFS input setup	6	—	ns
t5	SAI RXD/RXFS/TXFS input hold	0	—	ns

1 Given the high setup time requirement on inputs, receiver and transmitter, when using frame sync in input, are likely to run at a lower frequency. This frequency will be driven by characteristics of the external component connected to the interface.

4.10.2.3 SAI Slave mode

In this mode, transmitter and/or receiver parts are set to receive transmit and/or receive clock from external world. Frame sync can be either input or output.

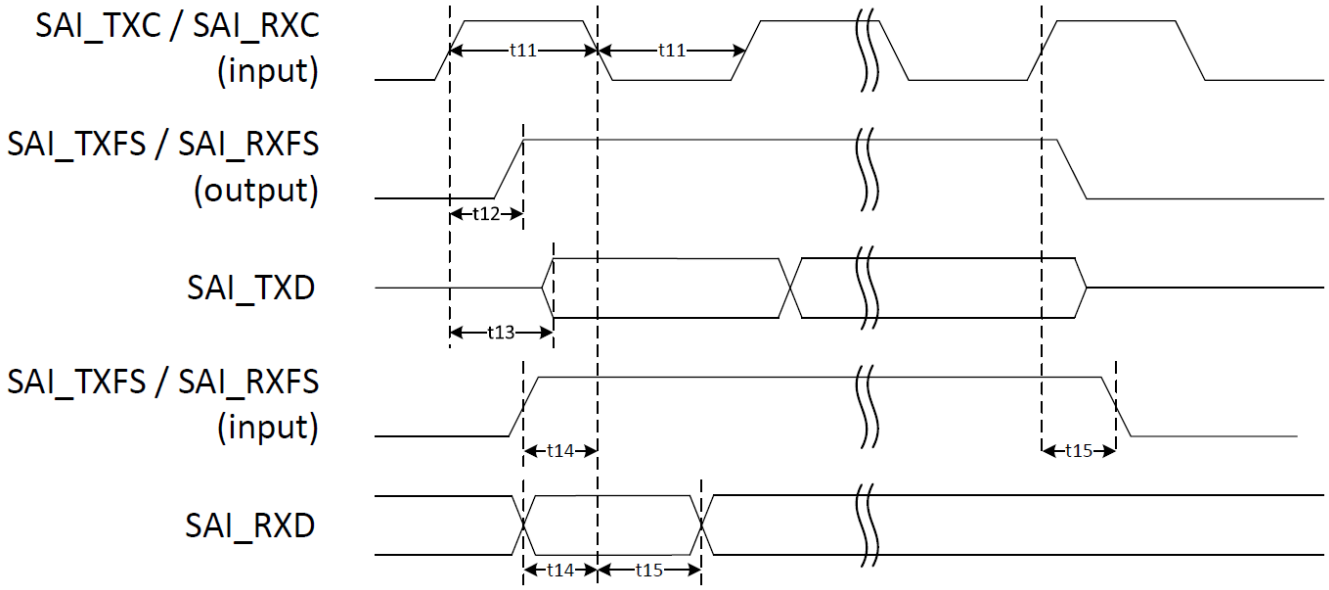

Figure 26. SAI Slave mode

Table 65. SAI timings—Slave mode

ID	Parameters	Min	Max	Unit
—	SAI TXC/RXC clock frequency	—	24.576	MHz
t11	SAI TXC/RXC pulse width low/high	45%	55%	TXC/RXC period
t12	SAI TXFS/RXFS output valid	—	13	ns
t13	SAI TXD output valid	—	13	ns
t14	SAI RXD/RXFS/TXFS input setup	1	—	ns
t15	SAI RXD/RXFS/TXFS input hold	4	—	ns

4.10.3 Enhanced serial audio interface (ESAI)

The same performance is achieved at both 1.8 V and 3.3 V unless otherwise stated.

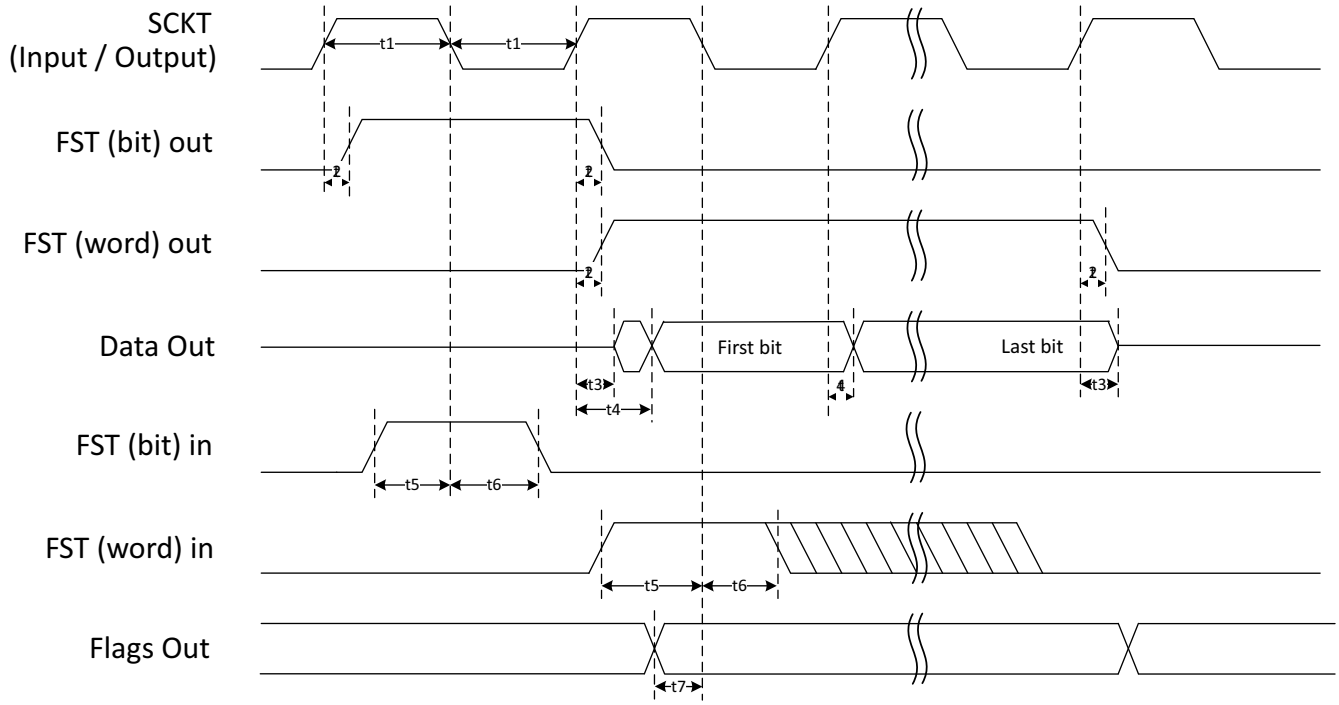

Figure 27. ESAI Transmit timing

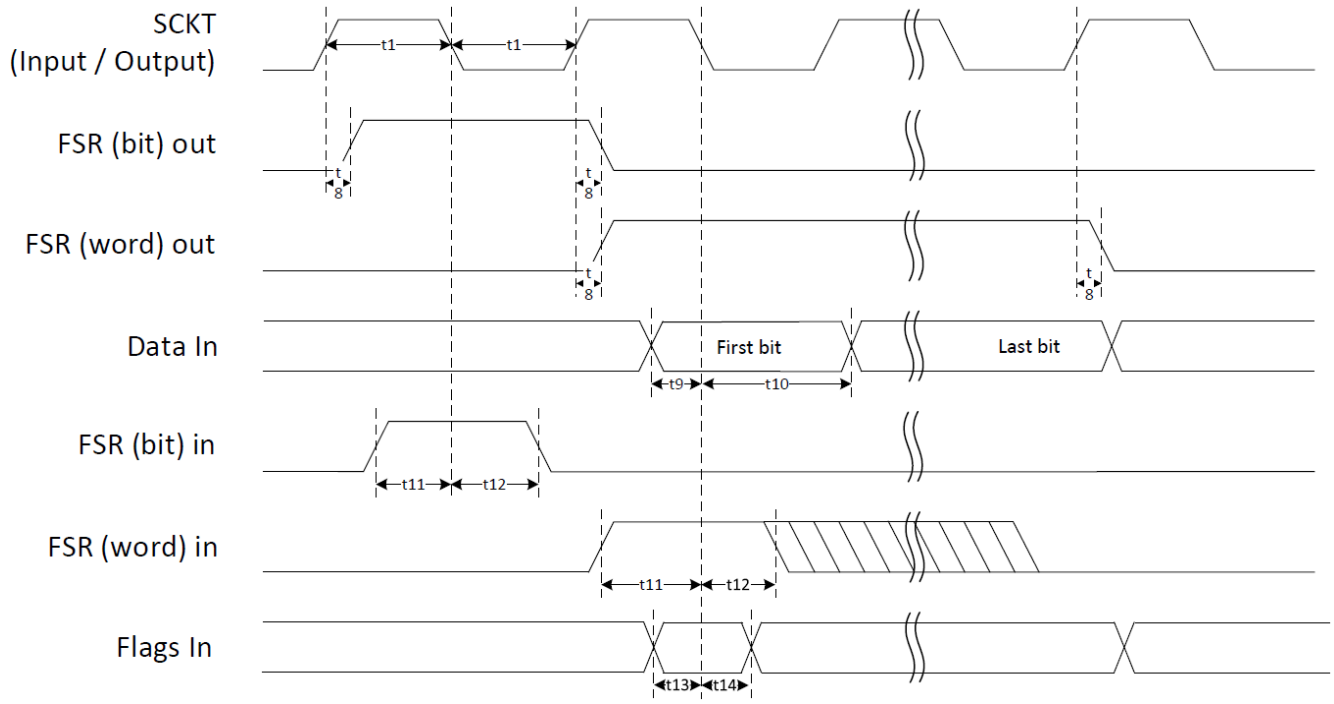

Figure 28. ESAI Receive timing

The following table shows the interface timing values. The ID field in the table refers to timing signals found in Figure 27 and Figure 28.

Table 66. Enhanced Serial Audio Interface (ESAI) Timing

ID	Parameters	Min	Max	Condition[1]	Unit
—	Clock frequency	—	24.576	—	MHz
t1	SCKT / SCKT pulse width high / low	45%	55%	—	SCKT / SCKR period
t2	FST output delay	—	10 2	x ck i ck	ns
t3	TX data - high impedance / valid data	—	9 1	x ck i ck	ns
t4	TX data output delay	—	10 2	x ck i ck	ns
t5	FST - setup requirement	—	2 10	x ck i ck	ns
t6	FST - hold requirement	—	2 0	x ck i ck	ns
t7	Flag output delay		10 2	x ck i ck	ns

Table 66. Enhanced Serial Audio Interface (ESAI) Timing (continued)

ID	Parameters	Min	Max	Condition[1]	Unit
t8	FSR output delay		7 4	x ck i ck a	ns
t9	RX data pins - setup requirement	2 10	—	x ck i ck	ns
t10	RX data pins - hold requirement	2 0	—	x ck i ck	ns
t11	FSR - setup requirement	2 10	—	x ck i ck a	ns
t12	FSR - hold requirement	2 0	—	x ck i ck a	ns
t13	Flags - setup requirement	2 10	—	x ck i ck s	ns
t14	Flags - hold requirement	2 0	—	x ck i ck s	ns
—	RX_HF_CLK / TX_HX_CLK clock cycle	20	—	—	ns
—	TX_HF_CLK input to SCKT		10	—	ns
—	RX_HF_CLK input to SCKR		10	—	ns

1 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode (SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode (SCKT and SCKR are the same clock)

4.10.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, including:

- SD3.1/eMMC5.1 High-Speed mode AC Timing
- eMMC5.1 DDR 52 mode/SD3.1 DDR 50 mode timing
- HS400 AC timing—eMMC 5.1 only
- HS200 Mode Timing
- SDR50/SDR104 AC Timing

4.10.4.1 SD3.1/eMMC5.1 High-Speed mode AC Timing

The following figure depicts the timing of SD3.1/eMMC5.1 High-Speed mode, and Table 67 lists the timing characteristics.

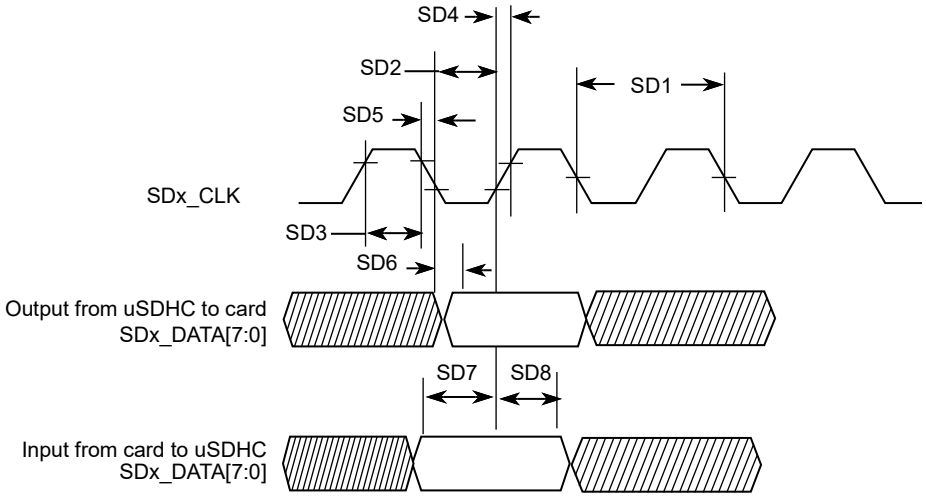

Figure 29. SD3.1/eMMC5.1 High-Speed mode Timing

Table 67. SD3.1/eMMC5.1 High-Speed mode interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs SD_CMD, SD_DATA (Reference to SD_CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns
eSDHC Input/Card Outputs SD_CMD, SD_DATA (Reference to SD_CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0—25 MHz. In high-speed mode, clock frequency can be any value between 0—50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0—20 MHz. In high-speed mode, clock frequency can be any value between 0—52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.10.4.2 eMMC5.1 DDR 52 mode/SD3.1 DDR 50 mode timing

The following figure depicts the timing of eMMC5.1 DDR 52 mode/SD3.1 DDR 50 mode, and Table 68 lists the timing characteristics. Be aware that only SD*x*_DATA is sampled on both edges of the clock (not applicable to SD_CMD).

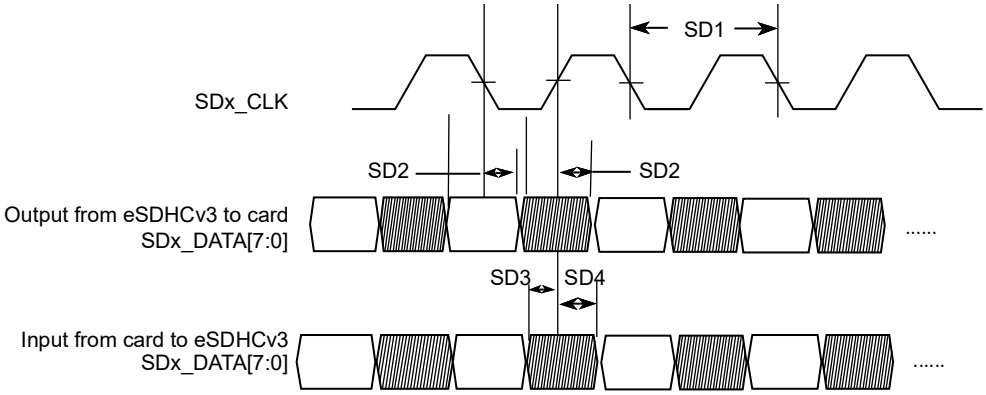

Figure 30. eMMC 5.1 timing

Figure 31. eMMC5.1 DDR 52 mode/SD3.1 DDR 50 mode interface timing

Table 68. eMMC5.1 DDR 52 mode/SD3.150 mode interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock[1]					
SD1	Clock Frequency (eMMC5.1 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.1 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SD*x*_DATA*x* (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.8	6.8	ns
uSDHC Input / Card Outputs SD_CMD, SD*x*_DATA*x* (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

1 Clock duty cycle will be in the range of 47% to 53%.

4.10.4.3 HS400 AC timing—eMMC 5.1 only

Figure 32 depicts the timing of HS400. Table 69 lists the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for

HS400 mode is the same as CMD input/output timing for SDR104 mode. Check SD5, SD6 and SD7 parameters in Table 71 SDR50/SDR104 Interface Timing Specification for CMD input/output timing for HS400 mode.

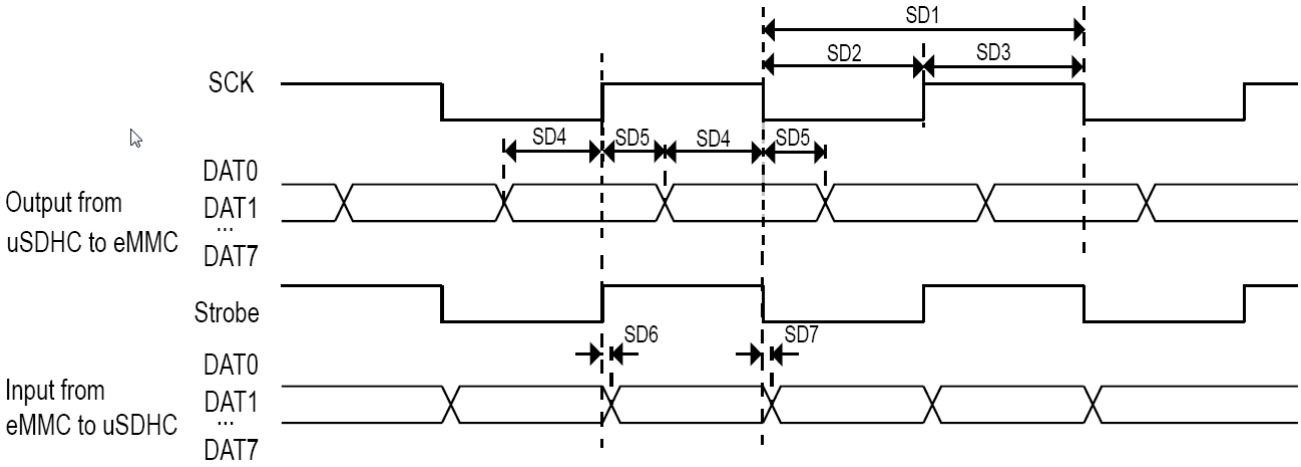

Figure 32. HS400 timing

Table 69. HS400 interface timing specifications

ID	Parameter	Symbols	Min	Max	Unit
Card Input clock					
SD1	Clock Frequency	fPP	0	200	Mhz
SD2	Clock Low Time	t_{CL}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
uSDHC Output/Card inputs DAT (Reference to SCK)					
SD4	Output Skew from Data of Edge of SCK	t_{OSkew1}	0.45	—	ns
SD5	Output Skew from Edge of SCK to Data	t_{OSkew2}	0.45	—	ns
uSDHC input/Card Outputs DAT (Reference to Strobe)					
SD6	uSDHC input skew	t_{RQ}	—	0.45	ns
SD7	uSDHC hold skew	t_{RQH}	—	0.45	ns

4.10.4.4 HS200 Mode Timing

The following figure depicts the timing of HS200 mode, and Table 70 lists the HS200 timing characteristics.

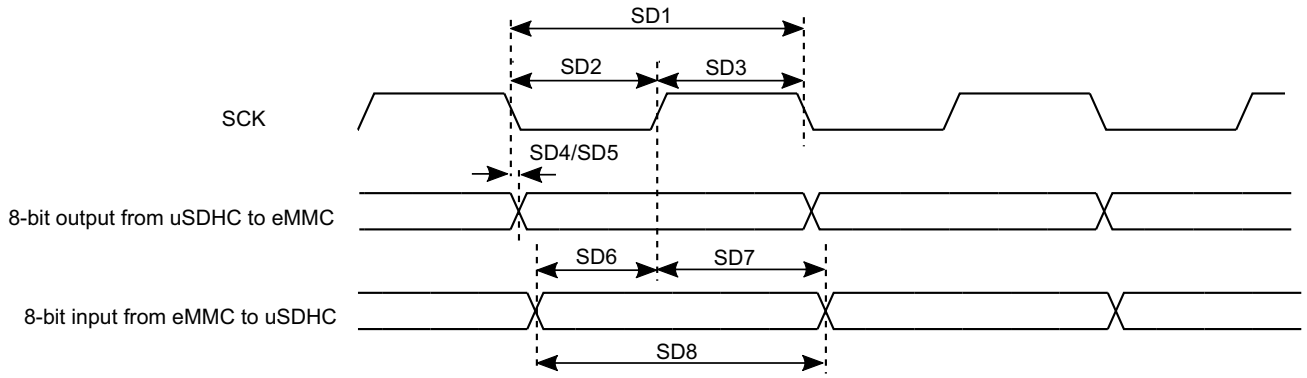

Figure 33. HS200 Mode Timing

Table 70. HS200 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
SD2	Clock High Time	t_{CH}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5*t_{CLK}	—	ns

[1]HS200 is for 8 bits while SDR104 is for 4 bits.

4.10.4.5 SDR50/SDR104 AC Timing

The following figure depicts the timing of SDR50/SDR104, and Table 71 lists the SDR50/SDR104 timing characteristics.

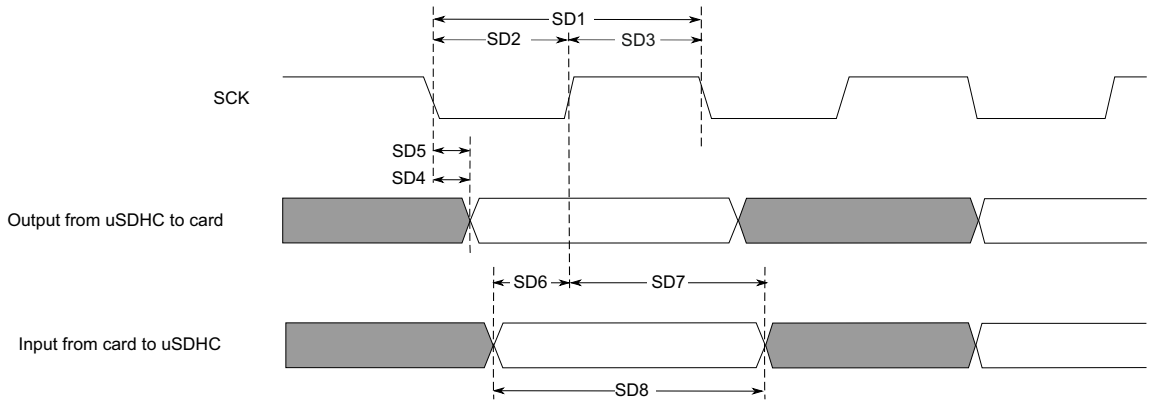

Figure 34. SDR50/SDR104 timing

Table 71. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
SD3	Clock High Time	t_{CH}	0.46 × t_{CLK}	0.54 × t_{CLK}	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	0.5 × t_{CLK}	—	ns

[1]Data window in SDR100 mode is variable.

4.10.4.6 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signaling level of SD/eMMC 5.1 and eMMC 5.1 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. DC parameters for I/O associated with VDD_USDHC1_1P8_3P3, VDD_USDHC2_1P8_3P3, VDD_USDHC_VSELECT_1P8_3P3, and VDD_EMMC0_1P8_3P3 in Table 33, "Dual-voltage 1.8 V GPIO DC parameters" and Table 34, "Dual-voltage 3.3 V GPIO DC parameters".

4.10.5 Ethernet Controller (ENET) AC Electrical Specifications

ENET interface supporting RGMII protocol in delay and non-delay mode. RGMII is used to support up to 1000 Mbps Ethernet as well as RMII protocol. RMII is used to support up to 100 Mbps Ethernet.

NOTE

ENET1 supports RGMII at 1.8 V and 2.5 V, and RMII at 3.3 V. ENET0 supports RGMII at 1.8 V only and RMII at 3.3 V.

Table 72. RGMII/RMII pin mapping

Pin name[1]	RGMII	RMII	Comment[2]
ENETx_RGMII_TXC	RGMII_TXC	RCLK50M	RCLK50M can be an input or an output. It's using different Alternate pin muxing modes. Refer to pin muxing for details.
ENETx_RGMII_TX_CTL	RGMII_TX_CTL	RMII_TXEN	—
ENETx_RGMII_TXD0	RGMII_TXD0	RMII_TXD0	—
ENETx_RGMII_TXD1	RGMII_TXD1	RMII_TXD1	—
ENETx_RGMII_TXD2	RGMII_TXD2	N/A	—
ENETx_RGMII_TXD3	RGMII_TXD3	N/A	—
ENETx_RGMII_RXC	RGMII_RXC	N/A	—
ENETx_RGMII_RX_CTL	RGMII_RX_CTL	RMII_CRS_DV	—
ENETx_RGMII_RXD0	RGMII_RXD0	RMII_RXD0	—
ENETx_RGMII_RXD1	RGMII_RXD1	RMII_RXD1	—
ENETx_RGMII_RXD2	RGMII_RXD2	RMII_RXER	RMII_RXER is mapped on ALT1 mode of pin muxing.
ENETx_RGMII_RXD3	RGMII_RXD3	N/A	—
ENETx_REFCLK_125M_25M	RGMII_REF_CLK	N/A	RGMII_REF_CLK is optional for RGMII operation and dependent on the intended clock configuration.
ENETx_MDIO	RGMII_MDIO	RMII_MDIO	—
ENETx_MDC	RGMII_MDC	RMII_MDC	—

1 *x* can be 0 or 1.

2 Except for RCLK50M and RMII_RXER, all other RMII functions are using the same pin muxing mode as RGMII.

4.10.5.1 RGMII

4.10.5.1.1 No-Internal-Delay mode

This mode corresponds to the RGMIIv1.3 specification.

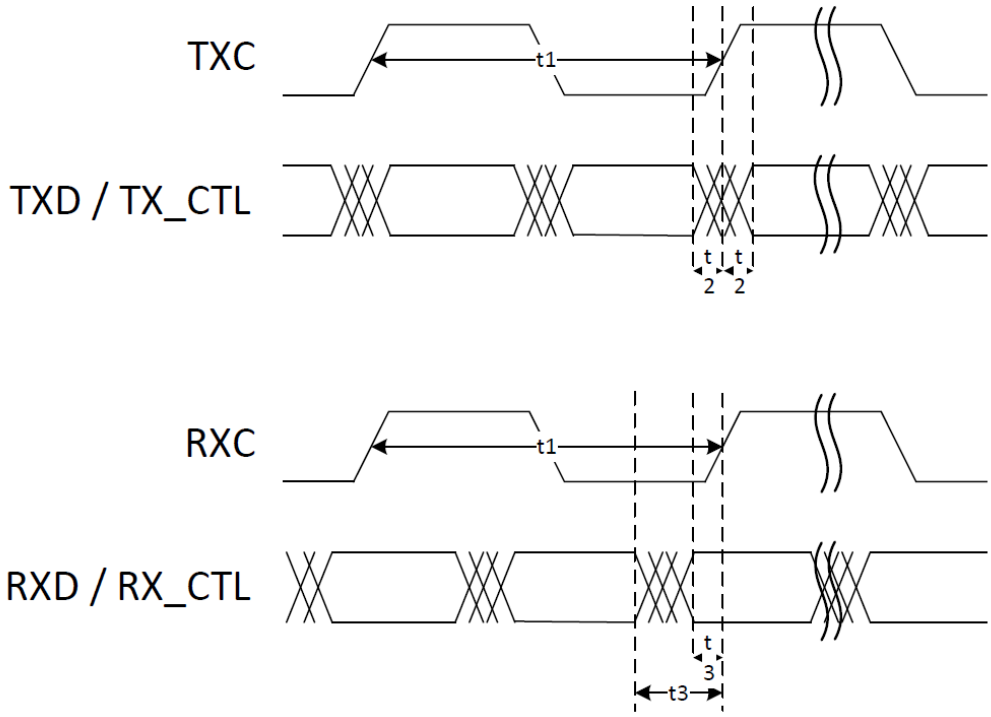

Figure 35. RGMII timing diagram—No-Internal-Delay mode

Table 73. RGMII timings—No-Internal-Delay mode

ID	Parameter	Min	Typ	Max	Unit
	TXC / RXC frequency	—	125	—	MHz
t1	Clock cycle	7.2	8	8.8	ns
t2	Data to clock output skew	-500	—	500	ps
t3	Data to clock input skew[1(1)]	1	—	2.6	ns

1 This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.

4.10.5.1.2 Internal-delay mode

This mode corresponds to RGMIIv2.0 specification. The interface is still operating at 2.5 V. 1.5 V is not supported.

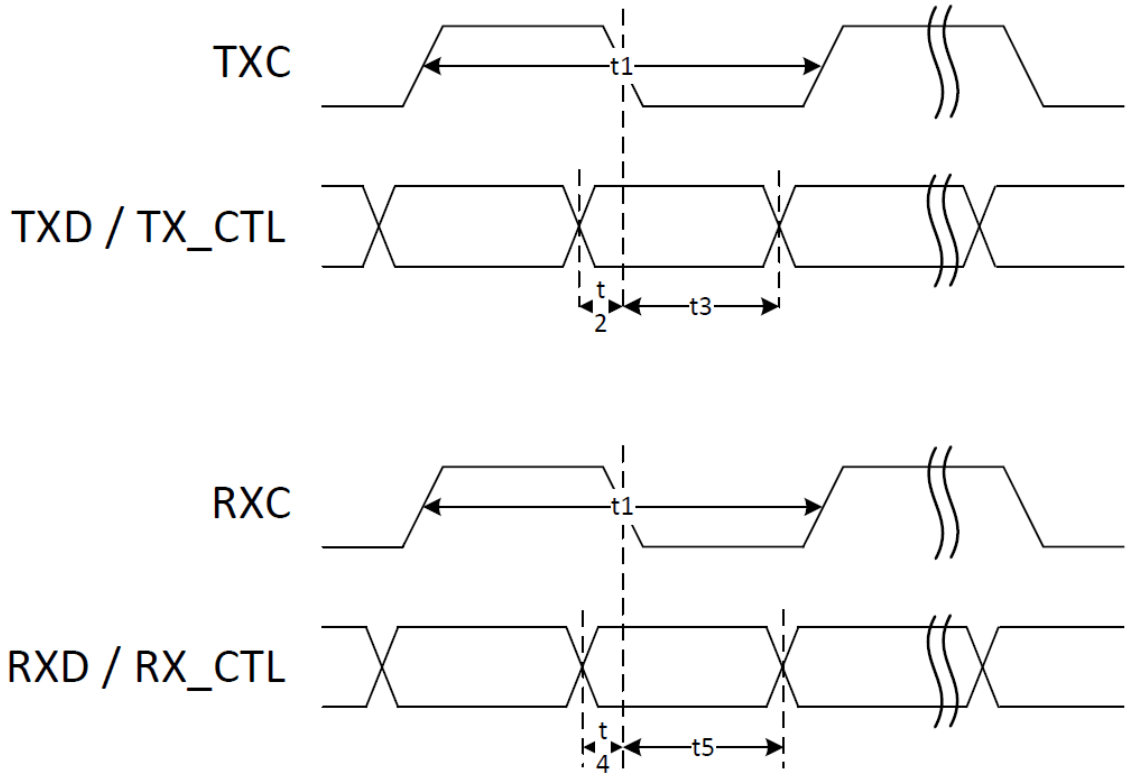

Figure 36. RGMII timing diagram—Internal-Delay mode

Table 74. RGMII timing—Internal-Delay mode

ID	Parameter	Min	Typ	Max	Unit
	TXC / RXC frequency	—	125	—	MHz
t1	Clock cycle	7.2	8	8.8	ns
t2	TXD setup time	1.2	—	—	ns
t3	TXD hold time	1.2	—	—	ns
t4	RXD setup time	0	—	—	ns
t5	RXD hold time	2.5	—	—	ns

4.10.5.2 RMII

RMII interface is matching RMII v1.2 specification. In RMII mode, the reference clock can be generated internally and provided to the PHY through RCLK50M_OUT. Or, it come from and external 50MHz clock generator which is connected to the PHY and to i.MX8 through RCLK50M_IN pin.

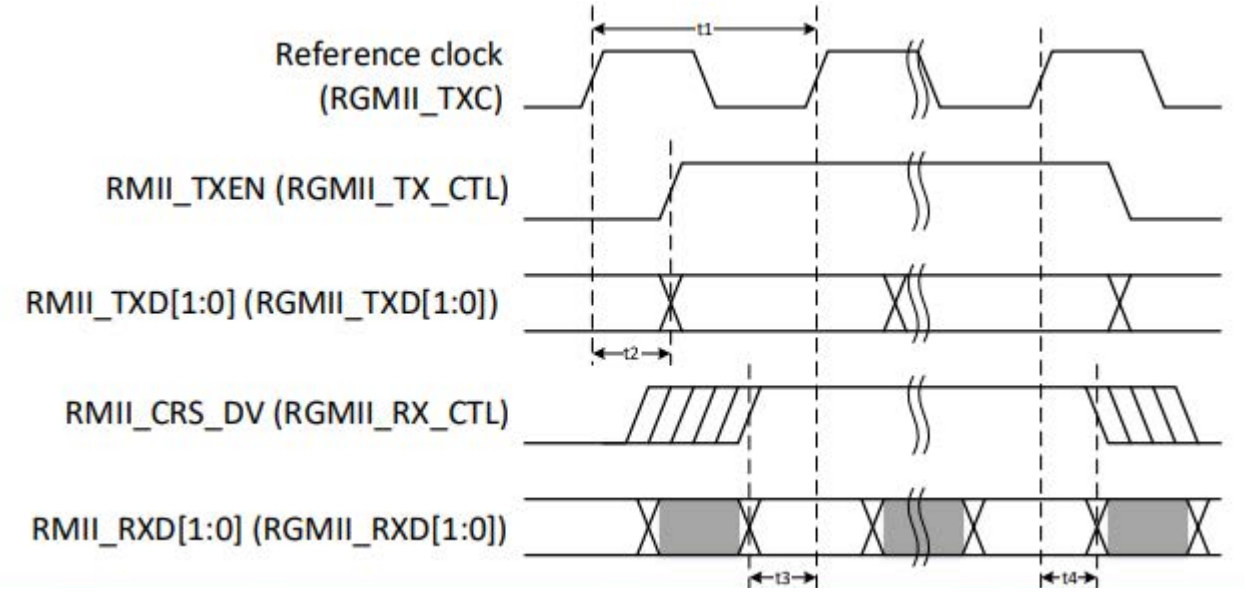

Figure 37. RMII timing diagram

Timings in table below are covering both cases: reference clock generated internally or externally.

Table 75. RMII timing

ID	Parameter	Min	Typ	Max	Unit
t1	Reference clock	—	50	—	MHz
	Reference clock accuracy	—	—	50	ppm
	Reference clock duty-cycle	35	—	65	%
t2	RMII_TXEN, RMII_TXD output delay	2	—	12	ns
t3	RMII_CRS_DV, RMII_RXD setup time	4	—	—	ns
t4	RMII_CRS_DV, RMII_RXD hold time	2	—	—	ns

4.10.5.3 MDIO

MDIO is the control link used to configure Ethernet PHY connected to i.MX8 device.

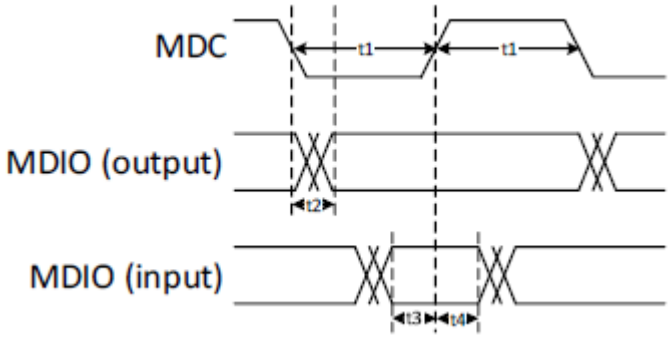

Figure 38. MDIO timing diagram

Table 76. MDIO timing

ID	Parameter	Min	Typ	Max	Unit
	MDC frequency	—	2.5	—	MHz
t1	MDC high / low pulse width	180	—	—	%
t2	MDIO output delay	0	—	20	ns
t3	MDIO setup time	10	—	—	ns
t4	MDIO hold time	10	—	—	ns

4.10.6 CAN network AC Electrical Specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0B protocol specification. The processor has three CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the device reference manual to see which pins expose Tx and Rx pins; these ports are named FLEXCAN_TX and FLEXCAN_RX, respectively.

4.10.7 HDMI Tx module timing parameters

See the following specifications:

- DisplayPort 1.3 standard (VESA.org)
- Embedded DisplayPort 1.4 standard (VESA.org)

4.10.8 HDMI Rx module

The module passes CTS 1.4 (up to 3.4 Gbps) tests such as TMDS min/max differential swing tolerance, intra-pair skew, and jitter tolerance. However, HDMI-RX is not certified because the IP does not support

DVI mode and cannot detect the video timing. In DVI mode, without the AVI info frame, detection of the video mode utilized is not possible. In addition, only HDCP 2.2 is supported.

For full HDMI-RX compliance, NXP recommends utilizing an external HDMI to MIPI CSI-2 bridge device.

4.10.9 HDMI Tx and Rx resistor connections

The DDC link requires external pull-up resistors to be connected to a 5 V supply. The following table provides the range for those pull-ups.

Table 77. HDMI—Pull-up resistors for DDC link

Ball name	Min	Typ	Max	Unit
HDMI_TX0_DDC_SCL, HDMI_RX0_DDC_SCL	1.5	—	2	kΩ
HDMI_TX0_DDC_SDA, HDMI_RX0_DDC_SDA	1.5	—	2	kΩ

Table 78. HDMI_REXT reference resistor connection

Name	Min	Typ	Max	Unit	Descriptions
REXT	497.50	500	502.50	Ω	REXT resistor is 500 Ω ± 0.5%. It shall be connected to ground.

4.10.10 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. The following figure depicts the timing of the I²C module, and Table 79 lists the I²C module timing characteristics.

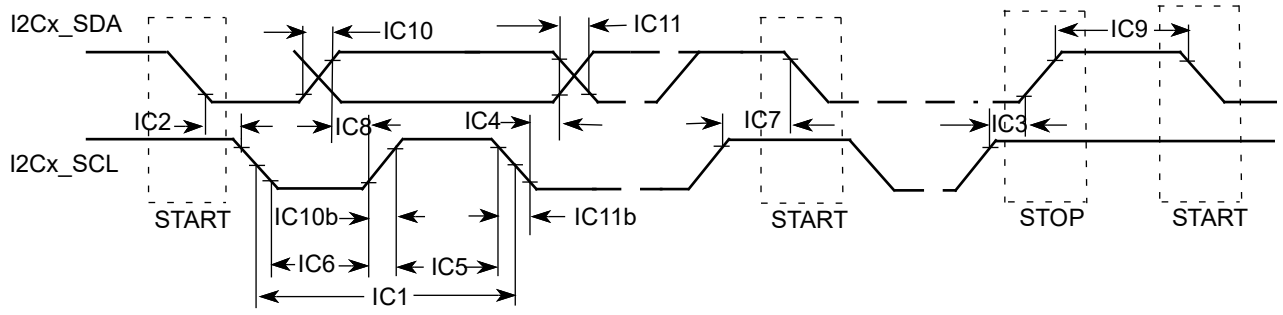

Figure 39. I²C bus timing

Table 79. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10/IC10b	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11/IC11b	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal in order to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

Table 80. I2C timing

		Fast Mode Plus		High Speed[1]		Unit
ID	Parameter	Min	Max	Min	Max	
IC1	SCL clock frequency	—	1	—	3.4	MHz
IC2	Hold time (repeated) START condition	260	—	160	—	ns
IC3	Set-up time for STOP condition	260	—	160	—	ns
IC4	Data hold time	0	—	0	70	ns
IC5	HIGH Period of I2Cx_SCL Clock	260	—	60	—	ns
IC6	LOW Period of the I2Cx_SCL Clock	500	—	160	—	ns
IC7	Set-up time for a repeated START condition	260	—	160	—	ns
IC8	Data set-up time	50	—	10	—	ns
IC9	Bus free time between a STOP and START condition	500	—	150	—	ns
IC10	Rise time of I2Cx_SDA signals	—	120	10	80	ns
IC11	Fall time of I2Cx_SDA signals	12 (@3.3 V) 6.5 (@1.8 V)	120	10	80	ns
IC10b	Rise time of I2Cx_SCL signals	—	120	10	40	ns
IC11b	Fall time of I2Cx_SCL signals	12 (@3.3 V) 6.5 (@1.8 V)	120	10	40	ns
IC12	Capacitive load for each bus line (Cb)	—	550	—	100	pF

1 High-speed mode is only available for I2C modules in DMA, SCU and Cortex-M4 subsystems.

4.10.11 LVDS and MIPI-DSI display output specifications

4.10.11.1 LVDS display bridge module parameters

Maximum frequency support for dedicated LVDS channels on this device:

Table 81. LVDS pins

Function[1]	Channel A	Channel B
Single channel	4 pairs LVDS up to 1.12 Gbps per pair	4 pairs LVDS up to 1.12 Gbps per pair
Dual channel	8 pairs LVDS up to 595 Mbps per pair	

1 In single channel operation the maximum clock speed is 160 MHz; in dual channel operation with a single synchronized clock the maximum clock speed is 85 MHz.

4.10.11.2 MIPI-DSI display bridge module parameters

Maximum frequency support for dedicated MIPI-DSI channels on this device:

Table 82. MIPI-DSI pins

Function[1]	Channel A
DSI	DSI up to 1.5 Gb/per lane

1 Maximum clock speed is 1.5 GHz.

4.10.11.3 LVDS display bridge (LDB) module electrical specifications

The LVDS interface is compatible with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits.”

Table 83. LVDS Display Bridge (LDB) Electrical Specifications

Parameter	Symbol	Test Condition	Min	Max	Units
Differential Voltage Output Voltage	V_{OD}	100 Ω Differential load	0.25	0.4	V
Output Voltage High	Voh	100 Ω differential load (0 V Diff—Output High Voltage static)	—	1.475	V
Output Voltage Low	Vol	100 Ω differential load (0 V Diff—Output Low Voltage static)	0.925	—	V
Offset Static Voltage	V_{OS}	Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors.	1.125	1.275	V
VOS Differential	V_{OSDIFF}	Difference in V_{OS} between a One and a Zero state	—	—	mV
Output short-circuited to GND	ISA ISB	With the output common shorted to GND	—	40	mA
Output short current	ISAB		—	12	mA

4.10.11.4 MIPI-DSI HS-TX specifications

Table 84. MIPI high-speed transmitter DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{CMTX}[1]	High Speed Transmit Static Common Mode Voltage	150	200	250	mV
$\lvert\Delta V_{CMTX}\rvert_{(1,0)}$	V_{CMTX} mismatch when Output is Differential-1 or Differential-0	—	—	5	mV
$\lvert V_{OD}\rvert$[1]	High Speed Transmit Differential Voltage	140	200	270	mV
$\lvert\Delta V_{OD}\rvert$	V_{OD} mismatch when Output is Differential-1 or Differential-0	—	—	10	mV

Table 84. MIPI high-speed transmitter DC specifications (continued)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OHHS}[1]	High Speed Output High Voltage	—	—	360	mV
Z_{OS}	Single Ended Output Impedance	40	50	62.5	Ω
ΔZ_{OS}	Single Ended Output Impedance Mismatch	—	—	10	%

1 Value when driving into load impedance anywhere in the Z_{ID} range.

Table 85. MIPI high-speed transmitter AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
$\Delta V_{CMTX(HF)}$	Common-level variations above 450 MHz	—	—	15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450 MHz	—	—	25	mV_{PEAK}
t_R and t_F[1]	Rise Time and Fall Time (20% to 80%)	100	—	0.35 UI	ps

1 UI is the long-term average unit interval.

4.10.11.5 MIPI-DSI LP-TX specifications

Table 86. MIPI low-power transmitter DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}[1]	Thevenin Output High Level	1.1	1.2	1.3	V
V_{OL}	Thevenin Output Low Level	–50	—	50	mV
Z_{OLP}[2]	Output Impedance of Low Power Transmitter	110	—	—	Ω

1 This specification can only be met when limiting the core supply variation from 1.1 V till 1.3 V.

2 Although there is no specified maximum for ZOLP, the LP transmitter output impedance ensures the TRLP/TFLP specification is met.

Table 87. MIPI low-power transmitter AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
T_{RLP}/T_{FLP}[1]	15% to 85% Rise Time and Fall Time	—	—	25	ns
T_{REOT}[1,2,3]	30% to 85% Rise Time and Fall Time	—	—	35	ns
$T_{LP\text{-}PULSE\text{-}TX}$[4]	Pulse width of the LP exclusive-OR clock: First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	—	—	ns
	Pulse width of the LP exclusive-OR clock: All other pulses	20	—	—	ns
$T_{LP\text{-}PER\text{-}TX}$	Period of the LP exclusive-OR clock	90	—	—	ns

Table 87. MIPI low-power transmitter AC specifications (continued)

Symbol	Parameter	Min	Typ	Max	Unit
$\delta V/\delta t_{SR}$ [1,5,6,7]	Slew Rate @ C_{LOAD}= 0 pF	30	—	500	mV/ns
	Slew Rate @ C_{LOAD}= 5 pF	30	—	200	mV/ns
	Slew Rate @ C_{LOAD}= 20 pF	30	—	150	mV/ns
	Slew Rate @ C_{LOAD}= 70 pF	30	—	100	mV/ns
C_{LOAD}	Load Capacitance	0	—	70	pF

1 C_{LOAD} includes the low equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be < 10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2 ns delay.

2 The rise-time of TREOT starts from the HS common-level at the moment of the differential amplitude drops below 70 mV, due to stopping the differential drive.

3 With an additional load capacitance CCM between 0 to 60 pF on the termination center tap at RX side of the lane.

4 This parameter value can be lower then TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in Low-Power Receiver section.

5 When the output voltage is between 15% and below 85% of the fully settled LP signal levels.

6 Measured as average across any 50 mV segment of the output signal transition.

7 This value represents a corner point in a piecewise linear curve.

4.10.11.6 MIPI-DSI LP-RX specifications

Table 88. MIPI low power receiver DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Logic 1 input voltage	880	—	1.3	mV
V_{IL}	Logic 0 input voltage, not in ULP state	—	—	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULP state	—	—	300	mV
V_{HYST}	Input hysteresis	25	—	—	mV

Table 89. MIPI low power receiver AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
e_{SPIKE} [1,2]	Input pulse rejection	—	—	300	V.ps
T_{MIN-RX} [3]	Minimum pulse width response	20	—	—	ns
V_{INT}	Peak Interference amplitude	—	—	200	mV
f_{INT}	Interference frequency	450	—	—	MHz

1 Time-voltage integration of a spike above V_{IL} when in LP-0 state or below VIH when in LP-1 state.

2 An impulse below this value will not change the receiver state.

3 An input pulse greater than this value shall toggle the output.

4.10.11.7 MIPI-DSI LP-CD specifications

Table 90. MIPI contention detector DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IHCD}	Logic 1 contention threshold	450	—	—	mV
V_{ILCD}	Logic 0 contention threshold	—	—	200	mV

4.10.11.8 MIPI-DSI DC specifications

Table 91. MIPI input characteristics DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{PIN}	Pad signal voltage range	–50	—	1350	mV
I_{LEAK}[1]	Pin leakage current	–10	—	10	μA
V_{GNDSH}	Ground shift	–50	—	50	mV
$V_{PIN(absmax)}$[2]	Maximum pin voltage level	–0.15	—	1.45	V
$T_{VPIN(absmax)}$[3]	Maximum transient time above $V_{PIN(max)}$ or below $V_{PIN(min)}$	—	—	20	ns

1 When the pad voltage is within the signal voltage range between $V_{GNDSH(min)}$ to VOH + $V_{GNDSH(max)}$ and the Lane Module is in LP receive mode.

2 This value includes ground shift.

3 The voltage overshoot and undershoot beyond the V_{PIN} is only allowed during a single 20 ns window after any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range.

4.10.12 PCIe PHY Parameters

The TX and RX eye diagrams specifications are per the template shown in the following figure. The summary of specifications is shown in Table 92 and Table 93. Note that the time closure (1–A OPENING) in the eye templates needs not match jitter specifications in the Standards Specifications, as there are such discrepancies in some Standards Specifications. The design meets the tightest of specifications in case of discrepancy.

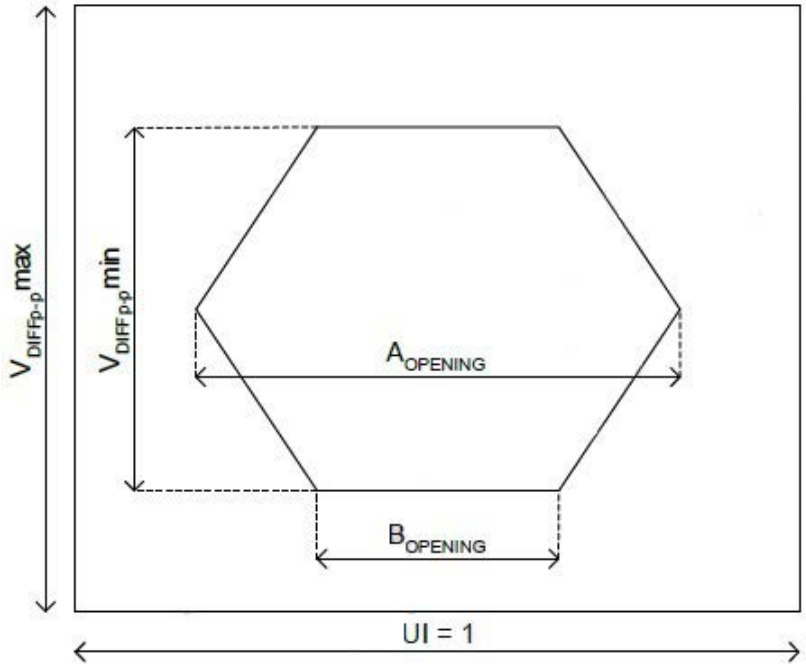

Figure 40. TX and RX eye diagram template

Table 92. PCIe transmitter eye specifications for example standards

	UI	$A_{OPENING}$	$B_{OPENING}$	$A_{OPENING}$	$B_{OPENING}$	$V_{DIFFp-p}$min	$V_{DIFFp-p}$max
	ps	UI		ps		mV	
PCI Express Gen 1 Transition Bit	400	0.75	0	300	0	800	1200[1]
PCI Express Gen 1 De-emphasized Bit	400	0.75	0	300	0	505	757
PCI Express Gen 2 Transition Bit	200	0.75	0	150	0	800	1200[1]
PCI Express Gen 2 De-emphasized Bit	200	0.75	0	150	0	379	850

[1] $V_{DIFFp-p}$ eye opening is limited to VDDIO under matched termination conditions.

Table 93. PCIe receiver eye specifications for example standards

	UI	$A_{OPENING}$	$B_{OPENING}$	$A_{OPENING}$	$B_{OPENING}$	$V_{DIFFp-p}$min	$V_{DIFFp-p}$max
	ps	UI		ps		mV	
PCI Express Gen 1 Transition Bit	400	0.4	0	160	0	175	1200
PCI Express Gen 2 Transition Bit[1]	200	0.32	0	64	0	100	1200
PCI Express Gen 3 Virtual EYE[2]	125	0.3	0	38	0	25	1300

1 For a lossy channel, the default DFE setting may not work for PCIe Gen2 -3.5dB TX de-emphasis. It is recommended to use a higher DFE setting (reg241[7]=A1_force=1 and reg241[5:0]=A1_init) in this case.

2 PCIE 3.0 8 GT/s measured using PCIE reference equalizer + CDR per PCIE specification. PCIe 1.0 and 2.0 compliant. PCIe 3.0 capable; contact your NXP representative.

Table 94. PCIe differential output driver characteristics (including board and load)

Parameter	Min	Typ	Max	Units	Notes
Output Rise and fall time T_R, T_F	175	—	350	ps	1
Output Rise/Fall matching	—	—	20	%	1, 2
Output skewT_{OSKEW}	—	—	50	ps	—
Initialization time from assertion of TXOE	100	—	—	ns	—
Initialization time from assertion of TXENA	—	10	—	μs	—
Transmission line characteristic impedance (Z_O)	—	50	—	Ω	—
Driver output impedance, single ended (small signal @ Vout=Vcm)	—	1000	—	Ω	—
Output single ended voltage (RS= 33, RT= 50 Ω) V_{OH} I_{OH}@ 6 * I_R V_{OL}	 0.65 -13 -0.20	 0.71 -14.2 0.00	 0.85 -17 0.05	 V mA V	3, 4 3
Output common mode voltage (RS = 33, RT= 50 Ω) $\|V_{OCM}\|$ $\Delta V_{OCM\ (DC)}$ $\Delta V_{OCM\ (AC)}$	 0.25 -0.015 -0.050	 0.375	 0.55 0.015 0.050	 V	 5 6
Buffer induced deterministic jitter (absolute, pk-pk)	—	—	4	ps	7,8
Reference Buffer Dynamic Power (Digital)	—	0.015	0.66	μA	9
Reference Buffer Dynamic Power (Analog)	—	2.8	3.14	mA	9
Output Buffer Dynamic Power (Digital)	—	0.035	1.8	μA	9
Output Buffer Dynamic Power (Analog)	—	18.9	22.11	mA	9

1 When the output is transitioning between logic 0 and logic 1, or logic 1 and logic 0, and driving a terminated transmission line, the outputs monotonically transition between VOL and VOH, VOH, and VOL respectively. Target rise and fall times observed at the receiver and are primarily set by board trace impedance and Load capacitance. Rise and fall times are defined by 25% and 75% crossing points.

2 Calculated as: 2 × (TR–TF) / (TR+ TF)

3 I_R is proportional to the reference current. Measured across RT. The primary contributor to output voltage spread is VDD spread, and so a VDD tighter than ±10% may be required to achieve this spread.

4 Higher output voltages may occur depending on load, power supply, and selected output drive. Higher output voltages may transiently occur during initialization period following TXENA assertion.

5 Peak change in output differential voltage when driving a logic 0 and when driving a logic 1 under DC conditions.

6 Peak change in output differential voltage when driving a logic 0 and when driving a logic 1 under AC conditions.

7 Measured under “clean power supply and ground” conditions, and after de-embedding the jitter of the input, measured over a time span of 1000 cycles

8 Power supply induced jitter is included under this category, and the power supply variation is to be less than 8mVpp. Note that customer has to be uncommonly careful with power supply fidelity due to the small jitter numbers.

9 Power consumption is simulated under the following conditions:
Typ: TT, VDD=1.0 V, VD18=1.8 V, 25 °C
Max: FF, VDD=1.1 V, VD18=1.98 V, 125 °C
Dynamic: TXENA=1, TXOE=1
Static: TXENA=0, TXOE=1

4.10.12.1 PCIE_REXT reference resistor connection

The following figure shows the PCIE_REXT reference resistor connection.

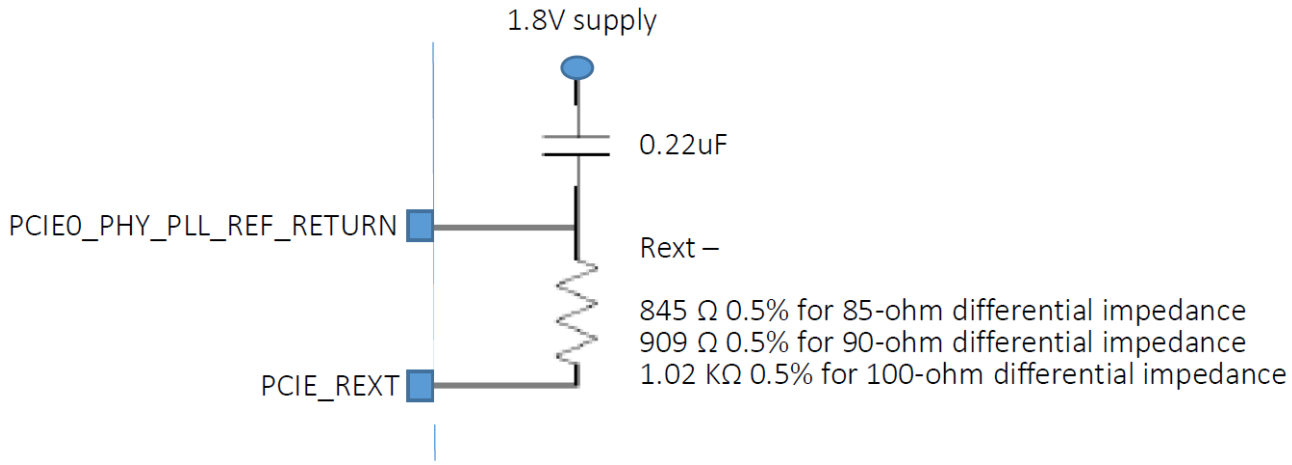

Figure 41. PCIE_REXT reference resistor connection

4.10.12.2 PCIE_REF_CLK

Refer to the Hardware Developer's Guide for this device, which contains details on the PCIe reference clock requirements.

4.10.13 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

The following figure depicts the timing of the PWM, and Table 95 lists the PWM timing parameters.

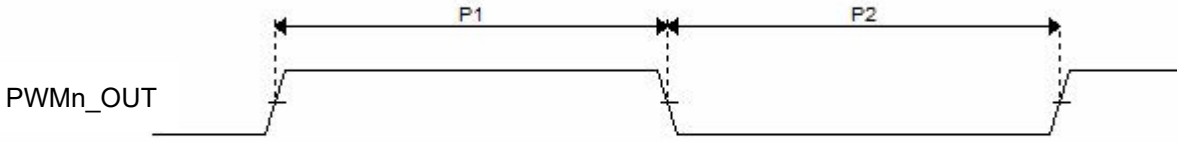

Figure 42. PWM Timing

Table 95. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
—	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15	—	ns
P2	PWM output pulse width low	15	—	ns

4.10.14 FlexSPI (Quad SPI/Octal SPI) timing parameters

The FlexSPI interface can work in SDR or DDR modes. It can operate up to 60 MHz at 3.3 V, 166 MHz at 1.8 V SDR mode or 200 MHz at 1.8 V DDR mode. It supports single-ended and differential DQS signaling.

FlexSPI supports the following clocking scheme for a read data path:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPIn_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPIn_MCR0[RXCLKSRC] = 0x1). It means the I/O cannot be used for another feature.
- Read strobe provided by memory device and input from DQS pad (FlexSPIn_MCR0[RXCLKSRC] = 0x3)

4.10.14.1 SDR mode

4.10.14.1.1 SDR mode timing diagrams

The following write timing diagram is valid for any FlexSPI*n*_MCR0[RXCLKSRC] value.

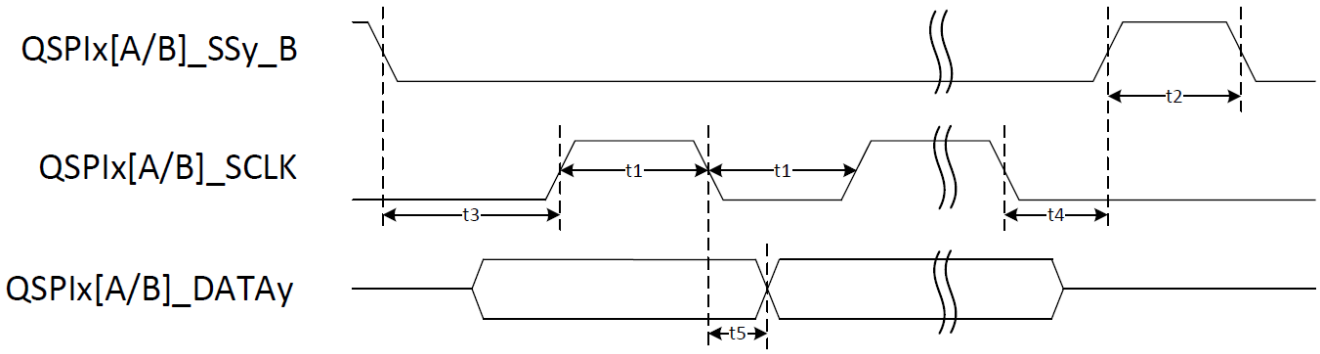

Figure 43. FlexSPI write timing diagram (SDR mode)

The following read timing diagram is valid for FlexSPI*n*_MCR0[RXCLKSRC] = 0x0 or 0x1.

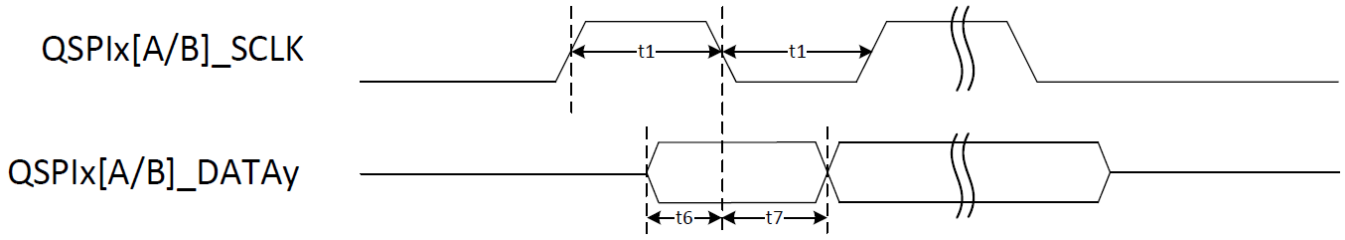

Figure 44. FlexSPI read timing diagram (SDR mode)

The following read timing diagram is valid for FlexSPI*n*_MCR0[RXCLKSRC] = 0x3.

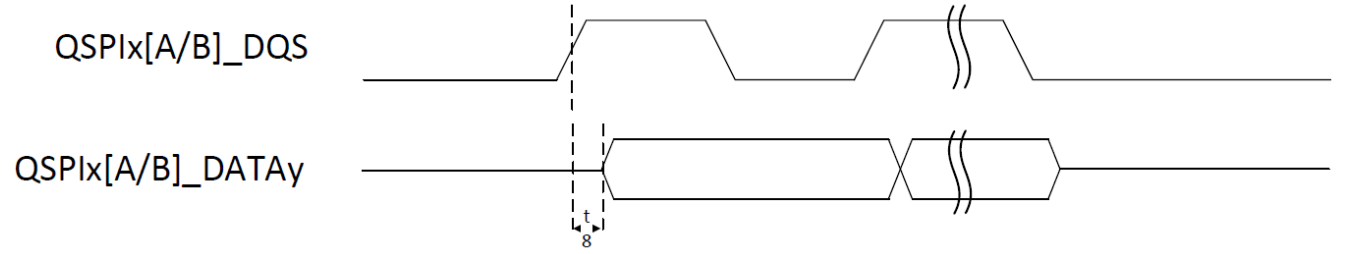

Figure 45. FlexSPI read with DQS timing diagram (SDR mode)

4.10.14.1.2 SDR mode timing parameter tables

Table 96. FlexSPI timings with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0 (SDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	60	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	7.5	—	ns
t2	QSPI*x*[A/B]_SS*y*_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SS*y*_B Lead Time[1]	TCSS+0.5	—	SCLK
t4	QSPI*x*[A/B]_SS*y*_B Lag Time[1]	TCSH	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output Delay	—	1	ns
t6	QSPI*x*[A/B]_DATA*y* Setup Time	6	—	ns
t7	QSPI*x*[A/B]_DATA*y* Hold Time	0	—	ns

[1] Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

Table 97. FlexSPI timings with FlexSPI*n*_MCR0[RXCLKSRC] = 0x1 (SDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	166	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	2.7	—	ns
t2	QSPI*x*[A/B]_SSy_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SSy_B Lead Time[1]	TCSS+0.5	—	SCLK
t4	QSPI*x*[A/B]_SSy_B Lag Time[1]	TCSH	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output Delay	—	1	ns
t6	QSPI*x*[A/B]_DATA*y* Setup Time	1	—	ns
t7	QSPI*x*[A/B]_DATA*y* Hold Time	2	—	ns

1 Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

Table 98. FlexSPI timings with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (SDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_DQS Cycle frequency	—	200	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	2.25	—	ns
t2	QSPI*x*[A/B]_SS*y*_B pulse width[1]	CSINTERVAL	—	SCLK
t3	QSPI*x*[A/B]_SS*y*_B Lead Time[2]	TCSS+0.5	—	SCLK
t4	QSPI*x*[A/B]_SS*y*_B Lag Time[2]	TCSH	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output Delay	—	1	ns
t8	QSPI*x*[A/B]_DQS / QSPI*x*[A/B]_DATA*y* delta	-0.65	0.65	ns

1 Minimum is 2 SCLK cycles even if CSINTERVAL value is less than 2.

2 Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

4.10.14.2 DDR mode

4.10.14.2.1 DDR mode timing diagrams

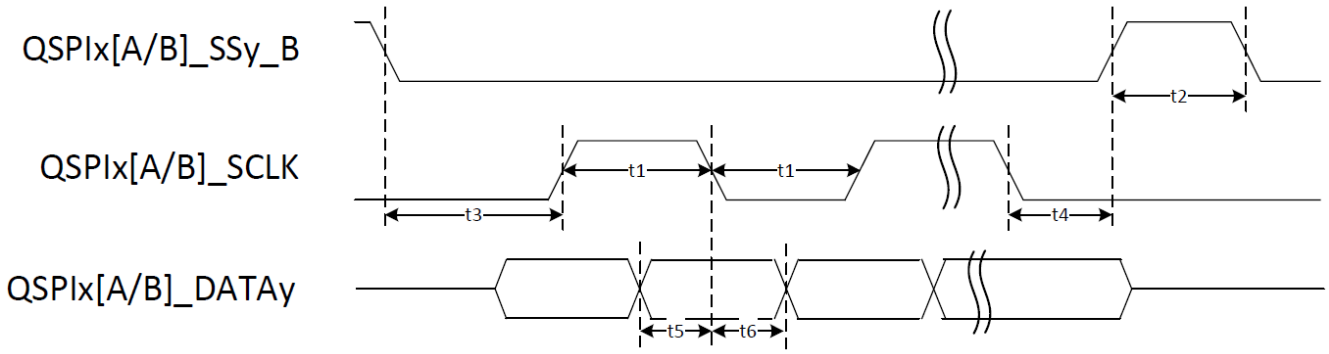

Figure 46. FlexSPI write timing diagram (DDR mode)

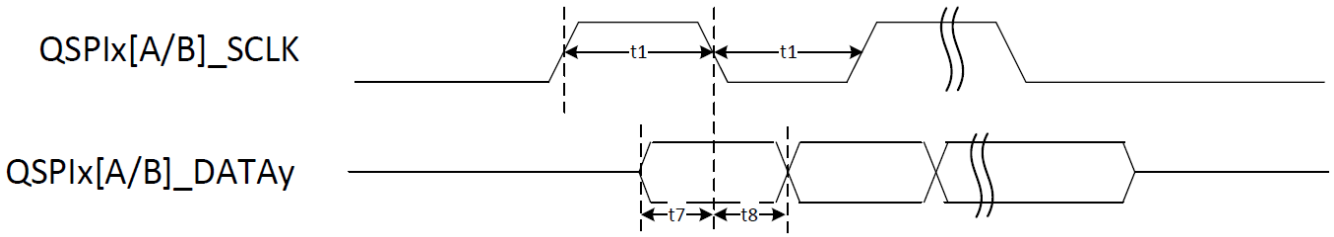

Figure 47. FlexSPI read timing diagram (DDR mode)

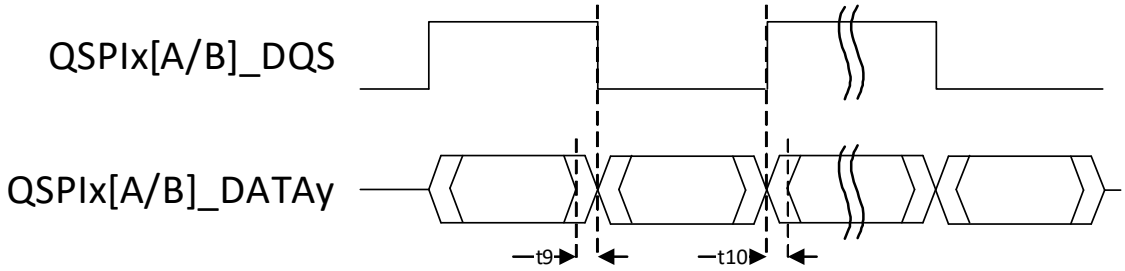

Figure 48. FlexSPI read with DQS timing diagram (DDR mode)

Table 99. FlexSPI timings with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0 (DDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	30	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	15	—	ns

Table 99. FlexSPI timings with FlexSPI*n*_MCR0[RXCLKSRC] = 0x0 (DDR mode) *(continued)*

ID	Parameter	Min	Max	Unit
t2	QSPI*x*[A/B]_SS*y*_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SS*y*_B Lead Time[1]	(TCSS+0.5)/2	—	SCLK
t4	QSPI*x*[A/B]_SS*y*_B Lag Time[1]	TCSH/2	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output valid time	6.5	—	ns
t6	QSPI*x*[A/B]_DATA*y* output hold time	6.5	—	ns
t7	QSPI*x*[A/B]_DATA*y* Setup Time	6	—	ns
t8	QSPI*x*[A/B]_DATA*y* Hold Time	0	—	ns

1 Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

Table 100. FlexSPI timings with FlexSPI*n*_MCR0[RXCLKSRC] = 0x1 (DDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	83	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	5.4	—	ns
t2	QSPI*x*[A/B]_SSy_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SSy_B Lead Time[1]	(TCSS+0.5)/2	—	SCLK
t4	QSPI*x*[A/B]_SSy_B Lag Time[1]	TCSH/2	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output valid time	2	—	ns
t6	QSPI*x*[A/B]_DATA*y* output hold time	2	—	ns
t7	QSPI*x*[A/B]_DATA*y* Setup Time	1	—	ns
t8	QSPI*x*[A/B]_DATA*y* Hold Time	1	—	ns

1 Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

Table 101. FlexSPI timings with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (DDR mode)

ID	Parameter	Min	Max	Unit
—	QSPI*x*[A/B]_SCLK Cycle frequency	—	200	MHz
t1	QSPI*x*[A/B]_SCLK High or Low Time	2.25	—	ns
t2	QSPI*x*[A/B]_SS*y*_B pulse width	1	—	SCLK
t3	QSPI*x*[A/B]_SS*y*_B Lead Time[1]	(TCSS+0.5)/2	—	SCLK
t4	QSPI*x*[A/B]_SS*y*_B Lag Time[1]	TCSH/2	—	SCLK
t5	QSPI*x*[A/B]_DATA*y* output valid time	0.65	—	ns
t6	QSPI*x*[A/B]_DATA*y* output hold time	0.65	—	ns

Table 101. FlexSPI timings with FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (DDR mode) *(continued)*

ID	Parameter	Min	Max	Unit
t9	QSPI*x*[A/B]_DATA*y* Setup Skew	—	0.65	ns
t10	QSPI*x*[A/B]_DATA*y* Hold Skew	—	0.65	ns

1 Timing is controlled from FLSH*x*CR1 register (*x*=A1, A2, B1, or B2).

4.10.15 Secure JTAG controller (SJC)

4.10.15.1 Internal pull-up/pull-down configuration

The following table describes the default configuration of internal pull-ups and pull-downs of the JTAG interface. External pull-ups and pull-downs are needed when this interface is routed to a connector.

Table 102. JTAG default configuration for internal pull-up/pull-down

Ball name	Internal pull setting[1]	Typical pull value	Unit
JTAG_TMS	PU	50	KΩ
JTAG_TCK	PD		
JTAG_TDI	PU		
JTAG_TRST_B	PU		
TEST_MODE_SELECT	PD		

1 PU = pull-up; PD = pull-down

4.10.15.2 JTAG timing parameters

Figure 49 depicts the SJC test clock input timing. Figure 50 depicts the SJC boundary scan timing. Figure 51 depicts the SJC test access port. Figure 52 depicts the JTAG_TRST_B timing. Signal parameters are listed in Table 103.

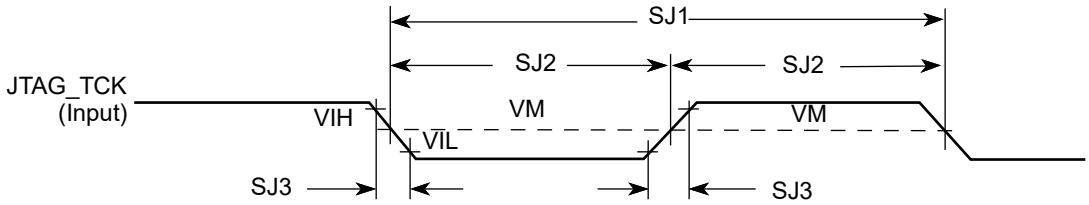

Figure 49. Test Clock Input Timing Diagram

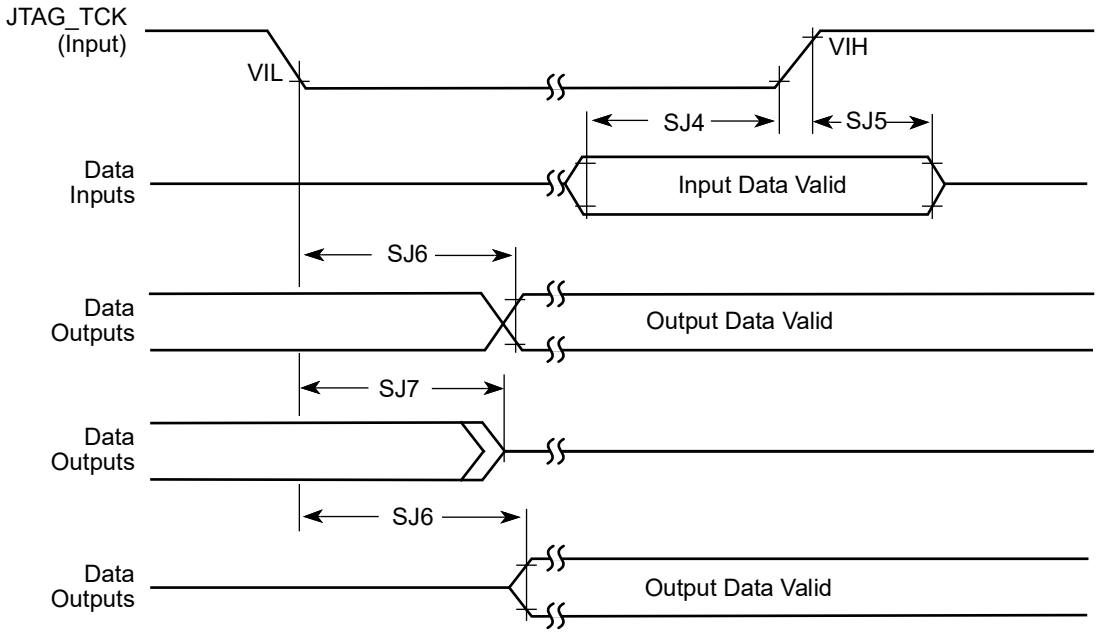

Figure 50. Boundary system (JTAG) timing diagram

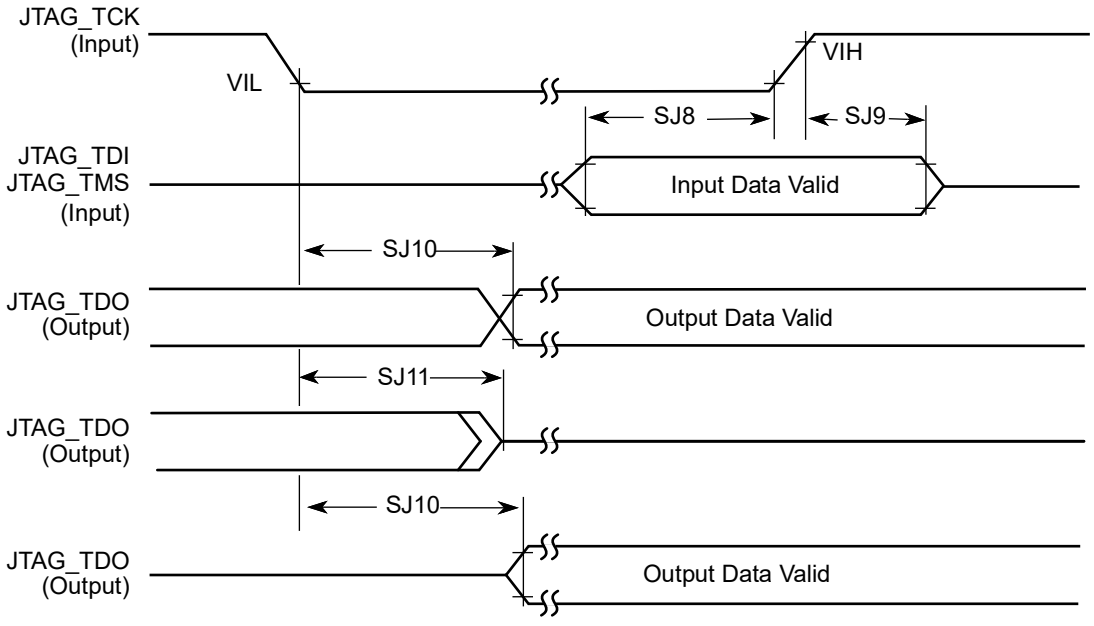

Figure 51. Test Access Port Timing Diagram

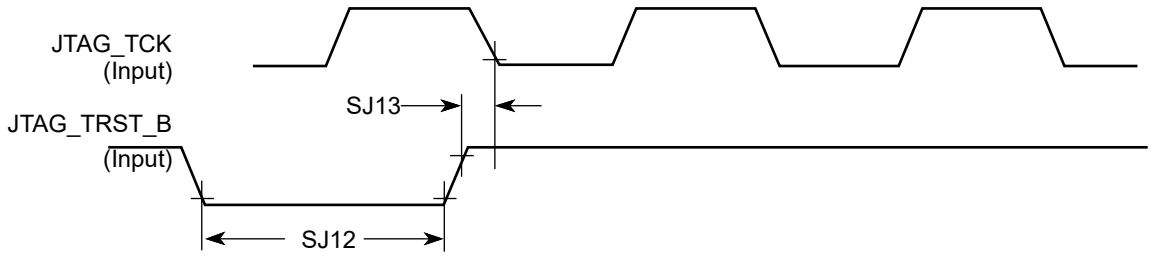

Figure 52. JTAG_TRST_B Timing Diagram

Table 103. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3xT_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC

2 V_M = mid-point voltage

4.10.16 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 104, Figure 53, and Figure 54 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 104. SPDIF Timing Parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 24.2 31.3	ns
SPDIF_OUT output (Load = 30pf) • Skew • Transition rising • Transition falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

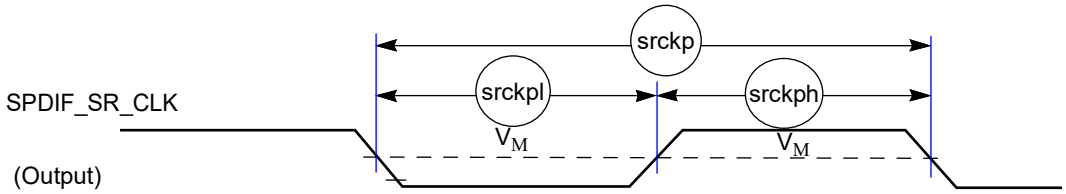

Figure 53. SPDIF_SR_CLK Timing Diagram

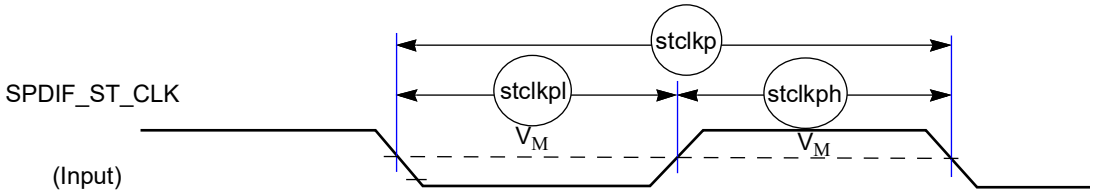

Figure 54. SPDIF_ST_CLK Timing Diagram

4.10.17 UART I/O configuration and timing parameters

4.10.17.0.1 UART Transmitter

The following figure depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 105 lists the UART RS-232 serial mode transmit timing characteristics.

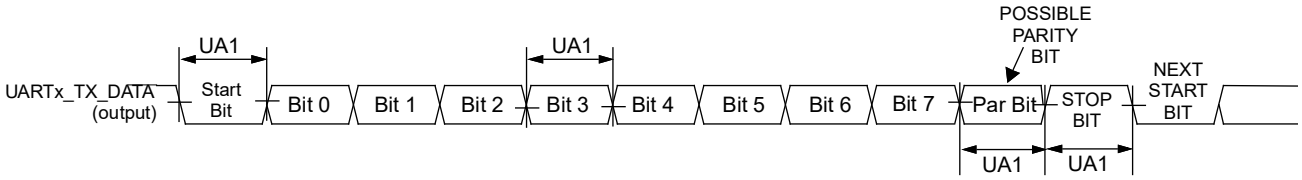

Figure 55. UART RS-232 Serial Mode Transmit Timing Diagram

Table 105. UART RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (LPUART_clk frequency)/(SBR[12:0] × (OSR+1)).

2 T_{ref_clk}: The period of UART reference clock ref_clk (LPUART_clk after SBR divider).

4.10.17.0.2 UART Receiver

The following figure depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 106 lists serial mode receive timing characteristics.

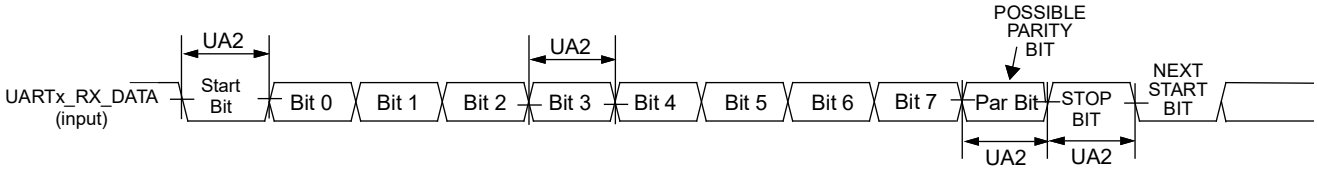

Figure 56. UART RS-232 Serial Mode Receive Timing Diagram

Table 106. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate}$ + $1/(16 \times F_{baud\_rate})$	—

1 The UART receiver can tolerate 1/((OSR+1) × Fbaud_rate) tolerance in each bit, but accumulation tolerance in one frame must not exceed 3/((OSR+1) × Fbaud_rate).

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (LPUART_clk frequency)/(SBR[12:0] × (OSR+1)).

4.10.17.0.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

The following figure depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 107 lists the transmit timing characteristics.

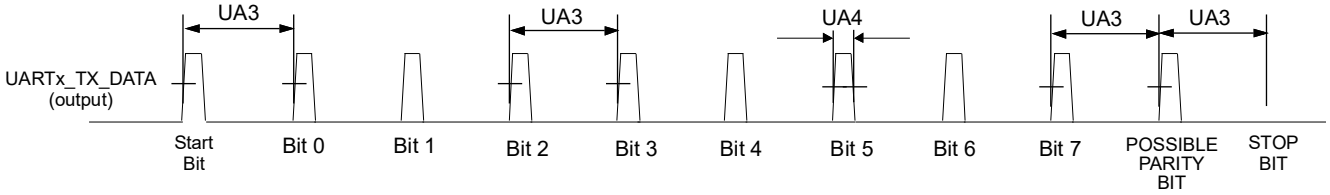

Figure 57. UART IrDA Mode Transmit Timing Diagram

Table 107. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(TNP+1)/(OSR+1) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(TNP+1)/(OSR+1) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (LPUART_clk frequency)/(SBR[12:0] × (OSR+1)).

2 T_{ref_clk}: The period of UART reference clock ref_clk (LPUART_clk after SBR divider).

UART IrDA Mode Receiver

The following figure depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 108 lists the receive timing characteristics.

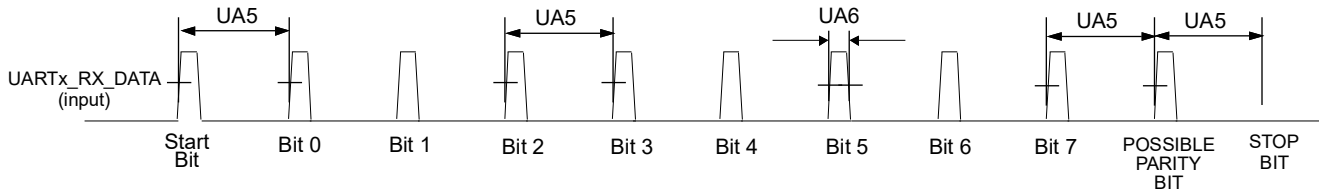

Figure 58. UART IrDA Mode Receive Timing Diagram

Table 108. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate 1/((OSR+1) × Fbaud_rate) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/((OSR+1) × Fbaud_rate).

[2] Fbaud_rate: Baud rate frequency. The maximum baud rate the UART can support is (LPUART_clk frequency)/(SBR[12:0] × (OSR+1)).

4.10.18 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is a DDR signal. The following timing specification is for both rising and falling edges.

4.10.18.1 USB HSIC Transmit Timing

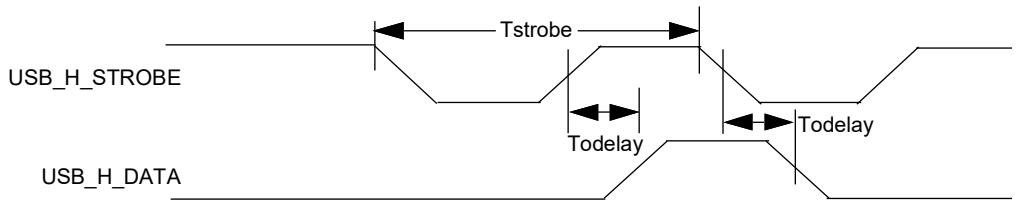

Figure 59. USB HSIC Transmit Waveform

Table 109. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.165	4.168	ns	—
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.10.18.2 USB HSIC Receive Timing

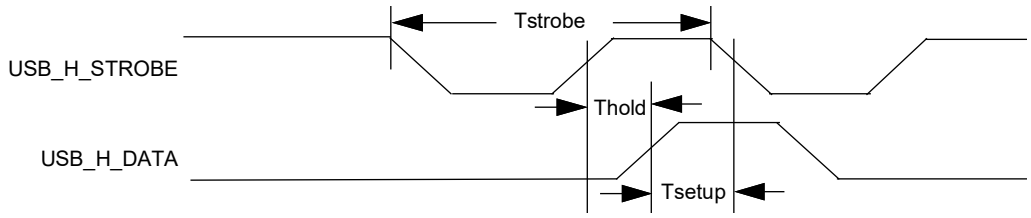

Figure 60. USB HSIC Receive Waveform

Table 110. USB HSIC Receive Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.165	4.168	ns	—
Thold	data hold time	300	—	ps	Measured at 50% point

Table 110. USB HSIC Receive Parameters[1] (continued)

Name	Parameter	Min	Max	Unit	Comment
Tsetup	data setup time	300	—	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

1 The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9× to 1× the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.10.19 USB 2.0 PHY Parameters

4.10.19.1 USB 2.0 PHY Transmitter specifications

This section describes the transmitter specifications for USB2.0 PHY.

4.10.19.1.1 USB 2.0 PHY full-speed/low-speed transmitter specifications

The following table lists the full-speed/low-speed (FS/LS) transmitter specifications for USB2.0 PHY.

Table 111. USB 2.0 PHY FS/LS transmitter specifications

Symbol	Description	Min	Typ	Max	Units
VOL	Output Voltage Low	0	—	0.3	V
VOH	Output Voltage High (Driven)	2.8	—	3.6	V
VOSE1	Single Ended One (SE1)	0.8	—	—	V
VCRS	Output Signal Cross Over Voltage	1.3	—	2.0	V
TFR	Driver Rise Time - FS	4	—	20	ns
TLR	Driver Rise Time - LS	75	—	300	ns
TFF	Driver Fall Time - FS	4	—	20	ns
TLF	Driver Fall Time - LS	75	—	300	ns
TFRFM	Differential Rise and Fall Time Matching - FS	90	—	111.11	%
TLRFM	Differential Rise and Fall Time Matching - LS	80	—	125	%
ZHSDRV	Driver Output Resistance (Also serves as HS Termination)	40.5	—	49.5	Ω
TDJ1	Source Jitter (Next Transition) - FS	-3.5	—	3.5	ns
TDJ2	Source Jitter (Paired Transition) - FS	-4	—	4	ns
TFDEOP	Source Jitter (Differential to SE0 transition) - FS	-2	—	5	ns
TFEOPT	Source SE0 interval of EOP - FS	160	—	175	ns
TDDJ1	Source Jitter in downstream direction (Next Transition) - LS	-25	—	25	ns
TDDJ2	Source Jitter in downstream direction (Paired Transition) - LS	-14	—	14	ns
TUDJ1	Source Jitter in upstream direction (Next Transition) - LS	-95	—	95	ns

Table 111. USB 2.0 PHY FS/LS transmitter specifications (continued)

Symbol	Description	Min	Typ	Max	Units
TUDJ2	Source Jitter in upstream direction (Paired Transition) - LS	-150	—	150	ns
TLDEOP	Source Jitter in upstream direction (Differential to SE0 transition) - LS	-40	—	100	ns
TLEOPT	Source SE0 interval of EOP - LS	1.25	—	1.5	µs

4.10.19.2 USB 2.0 PHY high-speed transmitter specifications

The following table lists the high-speed (HS) transmitter specifications for USB 2.0 PHY.

Table 112. USB 2.0 PHY HS transmitter specifications

Symbol/Parameter	Description	Min	Typ	Max	Units
HSOI	High Speed Idle Level	-10	—	10	mV
VHSTERM	Termination Voltage in High Speed	-10	—	10	mV
VHSOL	High Speed Data Signaling Low	-10	—	10	mV
VCHIRPJ	Chirp J (Differential Voltage)	700	—	1100	mV
VCHIRPK	Chirp K (Differential Voltage)	-900	—	-500	mV
ZHSDRV	Driver Output Resistance	40.5	—	49.5	Ω
THSR	Rise Time (10% to 90%)	100	—	—	ps
THSF	Fall Time (10% to 90%)	100	—	—	ps
HS Eye Opening: Template 1	Differential eye opening at 37.5% US and 62.5% UI for a hub measured at TP2 and for a device without a captive cable measured at TP3.	-300	—	300	mV
HS Eye Opening: Template 2	Differential eye opening at 37.5% US and 62.5% UI for a device with a captive cable measured at TP2.	-175	—	175	mV
HS Jitter: Template 1	Peak-Peak Jitter at Zero crossing for a hub measured at TP2 and for a device without captive cable measured at TP3.	—	—	15	%UI
		—	—	312.5	ps
HS Jitter: Template 2	Peak-Peak Jitter at Zero crossing for a device with captive cable measured at TP2.	—	—	25	%UI
		—	—	520.83	ps

4.10.19.3 USB 2.0 PHY receiver specifications

This section describes the receiver specifications implemented in USB 2.0 PHY.

4.10.19.3.1 USB 2.0 PHY full-speed/low-speed (FS/LS) receiver specifications

Table 113. USB 2.0 PHY FS/LS receiver specifications

Symbol	Description	Min	Typ	Max	Units
VIH	Input Voltage Level - High (Driven)	2	—	—	V
VIHZ	Input Voltage Level - High (Floating)	2.7	—	3.6	V
VIL	Input Voltage Level - Low	—	—	0.8	V
VTH	Switching Threshold	0.8	—	2.0	V
VCM	Common Mode Range	0.8	—	2.5	V
TJR1	Receiver Jitter Budget (Next Transition) - FS	-18.5	—	18.5	ns
TJR2	Receiver Jitter Budget (Paired Transition) - FS	-9	—	9	ns
TFEOPR	Receiver EOP Interval of EOP - FS	82	—	—	ns
TUJR1	US Port Differential Receiver Jitter (Next Transition) - LS	-152	—	152	ns
TUJR2	US Port Differential Receiver Jitter (Paired Transition) - LS	-200	—	200	ns
TDJR1	DS Port Differential Receiver Jitter (Next Transition) - LS	-75	—	75	ns
TDJR2	DS Port Differential Receiver Jitter (Paired Transition) - LS	-45	—	45	ns
TLEOPR	Receiver EOP Interval of EOP - LS	670	—	—	ns

4.10.19.3.2 USB 2.0 PHY high-speed receiver specifications

The following table lists the high-speed (HS) receiver specifications for USB 2.0 PHY.

Table 114. USB 2.0 PHY HS receiver specifications

Symbol/Parameter	Description	Min	Typ	Max	Units
VHSCM	HS RX input common mode voltage range.	-50	—	500	mV
ZHSDRV	HS RX input termination (Same as Driver output resistance).	40.5	—	49.5	Ω
HSRX Jitter: Template 3	HS RX Peak-Peak Jitter specification at differential zero crossing for a device with captive cable when signal applied at TP2.	—	—	20	%UI
		—	—	416.66	ps
HSRX Jitter: Template 4	HS RX Peak-Peak Jitter specification at differential zero crossing for a device without captive cable at TP3 and for a hub at TP2.	—	—	30	%UI
		—	—	625	ps
HSRX Input Eye Opening: Template 3	HS RX differential sensitivity specification at 40% and 60% UI for a device with captive cable when signal is applied at TP2.	-275	—	275	mV
HSRX Input Eye Opening: Template 4	HS RX differential sensitivity specification at 35% and 65% UI for a device without captive cable when signal is applied at TP3 and for a hub when a signal is applied at TP2.	-150	—	150	mV

4.10.19.3.3 USB 2.0 PHY high-speed envelope detector specifications

The following table lists the high-speed (HS) Envelope Detector Specifications of USB 2.0 PHY.

Table 115. USB 2.0 PHY HS envelope detector specifications

Symbol	Description	Min	Typ	Max	Units
VHSSQ	HS Squelch Detection threshold (differential signal amplitude)	100	—	150	mV
VHSDSC	HS Disconnect Detection threshold (differential signal amplitude)	525	—	625	mV

4.10.19.4 USB 2.0 PHY full-speed/high-speed terminations specification

The following table lists the full-speed/low-speed (FS/LS) Terminations Specification of USB 2.0 PHY.

Table 116. USB 2.0 PHY FS/LS terminations specification

Symbol	Description	Min	Typ	Max	Units
RPU	Bus Pull-Up resistor on US Port in IDLE State	900	—	1575	Ω
	Bus Pull-Up resistor on US Port in ACTIVE State	1425	—	3090	Ω
RPD	Bus Pull-Down resistor on DS Port	14.25	—	24.8	KΩ
VTERM	Termination Voltage for US Port Pull-Up (RPU)	3.0	—	3.6	V

4.10.19.5 Voltage threshold specification

The following table lists the OTG Comparator Specifications of USB2.0 PHY.

Table 117. USB 2.0 PHY OTG comparator specifications

Symbol	Description	Min	Typ	Max	Units
sessvld	B-Device Session Valid threshold	0.8	—	4.0	V
vbusvalid	VBUS Valid threshold	4.4	—	4.75	V

4.10.20 USB 3.0 PHY parameters

The following content is from the USB 3.0 PHY specifications.

4.10.20.1 USB 3.0 PHY external component

Table 118. USB 3.0 PHY external component specifications

Name	Min	Typ	Max	Units	Descriptions
rext	497.5	500	502.5	Ω	There needs to be an external resistor component connected at rext ball while the internal resistor or current is getting calibrated. Package routing from rext ball to its respective bump should not contribute more than 0.05 Ω.

4.10.20.2 USB 3.0 PHY transmitter module

Table 119. USB 3.0 PHY transmitter module electrical specifications

Symbol	Description	Min	Typ	Max	Unit
Voltage/current parameters					
$V_{TX-DIFFp}$	Programmable output voltage swing (single-ended)	50	—	500	mV
$V_{TX-DIFFp-p}$	Programmable differential peak-to-peak output voltage	100	—	1000	mV
$V_{TX-DIFFp-p-LOW}$[1]	Low power differential p-p TX voltage swing	400	—	1200	mV
$I_{TX-SHORT}$	Transmit lane short-circuit current	—	—	100	mA
$RL_{TX-DIFF}$	Transmitter differential return loss	—	—	0 < -20dB < 100Mhz 100Mhz < -18dB < 300Mhz 300Mhz < -16dB < 600Mhz 600Mhz < -10dB < 2500Mhz 2500Mhz < -9dB < 4875Mhz 4875Mhz < -8dB < 11200Mhz 11200Mhz < -5dB < 16800Mhz and -3dB beyond that	Db
RL_{TX-CM}	Transmitter common mode return loss	—	—	50Hz < -8dB < 15000Mhz	dB
$Z_{TX-DIFF-DC}$	DC differential TX impedance	80	100	120	Ω
UI	Unit Interval	199.94	—	200.06	ps
$T_{TX-MAX-JITTER}$	Transmitter total jitter (peak-to-peak) (T_j)	—	—	0.4	UI
$T_{TX-RJ-PLL-sigma}$	After application of TX jitter transfer function	—	—	2.42	ps
LTLAT-10	Transmitter data latency	—	—	210	UI

Table 119. USB 3.0 PHY transmitter module electrical specifications (continued)

Symbol	Description	Min	Typ	Max	Unit
Voltage parameters					
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle.	0	—	100	mV
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Peak Output Voltage	0	—	20	mV
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	—	25	mV
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	0	—	600	mV
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical Idle after sending an EIOS	—	—	8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid diff signaling after leaving Electrical Idle	—	—	8	ns
$V_{TX-CM-AC-PP}$	Tx AC peak-peak common mode voltage (5.0 GT/s)	20	—	150	mVpp
T_{EIExit}	Time to exit Electrical Idle (L0s) state and to enter L0	—	—	5	Txsysclk
Tx signal characteristics					
f_{tol}	TX Frequency Long Term Accuracy	-300	—	300	ppm of Fbaud
f_{SSC}	Spread-Spectrum Modulation Frequency	30	—	33	kHz
$t_{20-80TX}$	TX Rise/Fall Time	0.2	—	0.41	UI
t_{skewTX}	TX Differential Skew	—	—	20	ps

[1] For USB 3.0, no EQ is required

4.10.20.3 USB 3.0 PHY receiver module

Table 120. USB 3.0 PHY receiver module electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Comments
Voltage Parameters						
$V_{RX-DIFF(p-p)}$	Differential input voltage (peak-to-peak) (that is, receiver eye voltage opening)	100	—	1200	mV	—

Table 120. USB 3.0 PHY receiver module electrical specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Comments
$V_{RX-IDLE-DET-DIFF(p-p)}$	Differential input threshold voltage (peak-to-peak) to detect idle (LFPS)	100	—	300	mV	USB3 LFPS
$V_{cm, acRX}$	RX AC Common Mode Voltage	—	—	100	mVp-p	Simulated at 250 MHz
$V_{RX-CM-AC}$	Receiver common-mode voltage for AC coupling	—	0	150	mV	—
$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	W	100 Ω ± 10%
$RL_{RX-DIFF}$	Receiver differential return loss	Same as TX RL	—	—	dB	—
Jitter Parameters						
$T_{RX-MAX-JITTER}$	Receiver total jitter tolerance	0	—	0.66	UI	Incoming Jitter: USB3 = 0.43UI DJ + 0.23UI RJ USB3 numbers are with REFC-TLE

Table 121. PLL module electrical specifications

Parameter	Symbol	Description	Min	Typ	Max	Units
Input Reference Clock						
REF CLK Frequency	REF CLK	—	19.2	19.2/24/25/26/38.4	38.4	MHz
REF CLK Duty Cycle	—	—	47	—	53	MHz
REF CLK Frequency	REF CLK	—	40	40/48/50/52/100	100	MHz
REF CLK RJ Tolerance	—	Integrated jitter from 10 kHz to 16 MHz after applying appropriate PLL ref clock transfer function and the protocol JTF	—	—	0.5	ps
REF CLK Duty Cycle	—	—	37	—	63	%
Divided Reference Frequency	—	—	19.2	—	38.4	MHz
Dividers						
Input division	IPDIV<7:0>	—	1	—	255	Counts
Feedback division	pll_fbdiv_high<9:0>	—	2	—	1025	Counts
	pll_fbdiv_low<9:0>	—	2	—	1025	Counts
Feedback fractional division range	—	—	>-2	—	<2	Counts

Table 121. PLL module electrical specifications (continued)

Parameter	Symbol	Description	Min	Typ	Max	Units
Number of fractional bits	—	This includes one bit for sign	—	27	—	Bits
VCO						
Clock frequency	—	Output full rate clocks	—	5000	—	MHz
VCO frequency	—	VCO oscillation frequency	—	5000	—	MHz
Output clock frequency tolerance	—	This includes SSC deviation	-5300	—	300	ppm
SSC modulation rate	—	As applicable for USB3.0	30	—	33	kHz
Output clock RJ sigma for TX	—	After application of TX jitter transfer function	—	—	2.42	ps
Output clock RJ sigma for RX	—	After application of RX jitter transfer function	—	—	1.40	ps

4.11 Analog-to-digital converter (ADC)

The following table shows the ADC electrical specifications for VREFH=VDD_ADC_1P8.

Table 122. ADC electrical specifications (VREFH=VDD_ADC_1P8)

Symbol	Description	Min	Typ[1]	Max	Unit	Notes
V_{ADIN}	Input Voltage	VREFL	—	VREFH	V	—
C_{ADIN}	Input capacitance	—	4.5	—	pF	—
R_{ADIN}	Input Resistance	—	500	—	Ω	—
R_{AS}	Analog Source Resistance	—	—	5	kΩ	2
f_{ADCK}	ADC Conversion Clock Frequency	—	24	—	MHz	—
C_{sample}	Sample cycles	3.5	—	131.5	—	3
$C_{compare}$	Fixed compare cycles	—	17.5	—	cycles	—
$C_{conversion}$	Conversion cycles	$C_{conversion} = C_{sample} + C_{compare}$			cycles	—
DNL	Differential Non-Linearity	—	± 0.6	-0.5 to +1.1	LSB	4
INL	Integral Non-Linearity	—	± 0.9	±1.1	LSB	4
ENOB	Effective Number of Bits	—	—	—	—	5,6,7
	Avg = 1	10.1	10.4	—	Bits	
	Avg = 2	10.5	10.7	—	Bits	
	Avg = 16	11.1	11.3	—	Bits	
SINAD	Signal to Noise plus Distortion	SINAD=6.02 x ENOB + 1.76			dB	—

Table 122. ADC electrical specifications (VREFH=VDD_ADC_1P8) (continued)

Symbol	Description	Min	Typ[1]	Max	Unit	Notes
E_G	Gain error	—	-0.29	—	%FSV	8
E_O	Offset error	—	0.01	—	%FSV	9
I_{VDDA18}	Supply Current	—	480	—	μA	10
$I_{in,ext,leak}$	External Channel Leakage Current	—	30	500	nA	—
E_{IL}	Input leakage error	RAS * I_{in}			mV	—

1 Typical values assume VDD_ADC_1P8 = 1.8 V, Temp = 25 °C, fACLK = Max, unless otherwise stated. Typical values are for reference only. All values, including Min and Max, are derived from lab characterization and are not tested in production.

2 This resistance is external to the input pad. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 15 Ω analog source resistance. The RAS/CAS (analog source capacitance) time constant should be kept to < 1 ns.

3 See Figure 61.

4 ADC conversion clock at max frequency and using linear histogram.

5 Input data used for test was 1 kHz sine wave.

6 Measured at VREFH = 1.8 V and pwrsel = 2.

7 ENOB can be lower than shown, if an ADC channel corrupts other ADC channels through capacitive coupling. This coupling may be dominated by board parasitics. Care must be taken not to corrupt the desired channel being measured. This coupling becomes worse at higher analog frequencies and with switching waveforms due to the harmonic content.

8 Error measured at fullscale at 1.8 V.

9 Error measured at zero scale at 0 V.

10 Power Configuration Select, PWRSEL, is set to 10 binary.

The following table shows the ADC electrical specifications for 1V≤VREFH<VDD_ADC_1P8.

Table 123. ADC electrical specifications (1V≤VREFH<VDD_ADC_1P8)

Symbol	Description	Min	Typ[1]	Max	Unit	Notes
V_{ADIN}	Input Voltage	VREFL	—	VREFH	V	—
C_{ADIN}	Input capacitance	—	4.5	—	pF	—
R_{ADIN}	Input Resistance	—	500	—	Ω	—
R_{AS}	Analog Source Resistance	—	—	5	kΩ	2
f_{ADCK}	ADC Conversion Clock Frequency	—	24	—	MHz	—
C_{sample}	Sample cycles	3.5	—	131.5	—	3
$C_{compare}$	Fixed compare cycles	—	17.5	—	cycles	—
$C_{conversion}$	Conversion cycles	$C_{conversion} = C_{sample} + C_{compare}$			cycles	—
DNL	Differential Non-Linearity	—	± 0.6	-0.5 to +1.1	LSB	4
INL	Integral Non-Linearity	—	± 0.9	±1.1	LSB	4

Table 123. ADC electrical specifications (1V≤VREFH<VDD_ADC_1P8) (continued)

Symbol	Description	Min	Typ[1]	Max	Unit	Notes
ENOB	Effective Number of Bits	—	—	—	—	5,6,7
	Avg = 1	9.5	9.7	—	Bits	
	Avg = 2	9.9	10.1	—	Bits	
	Avg = 16	10.8	11	—	Bits	
SINAD	Signal to Noise plus Distortion	SINAD=6.02 x ENOB + 1.76			dB	—
E_G	Gain error	—	0.29	—	%FSV	8
E_O	Offset error	—	0.01	—	%FSV	9
I_{VDDA18}	Supply Current	—	480	—	μA	10
$I_{in,ext,leak}$	External Channel Leakage Current	—	30	500	nA	—
E_{IL}	Input leakage error	RAS * I_{in}			mV	—

1 Typical values assume VDD_ANA_1P8 = 1.8 V, Temp = 25 °C, fACLK = Max, unless otherwise stated. Typical values are for reference only. All values, including Min and Max, are derived from lab characterization and are not tested in production.

2 This resistance is external to the input pad. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 15 Ω analog source resistance. The RAS/CAS (analog source capacitance) time constant should be kept to < 1 ns.

3 See Figure 61.

4 ADC conversion clock at max frequency and using linear histogram.

5 Input data used for test was 1 kHz sine wave.

6 Measured at VREFH = 1 V and pwrsel = 2.

7 ENOB can be lower than shown, if an ADC channel corrupts other ADC channels through capacitive coupling. This coupling may be dominated by board parasitics. Care must be taken not to corrupt the desired channel being measured. This coupling becomes worse at higher analog frequencies and with switching waveforms due to the harmonic content.

8 Error measured at fullscale at 1.0 V.

9 Error measured at zero scale at 0 V.

10 Power Configuration Select, PWRSEL, is set to 10 binary.

The following figure shows a plot of the ADC sample time versus R_{AS}.

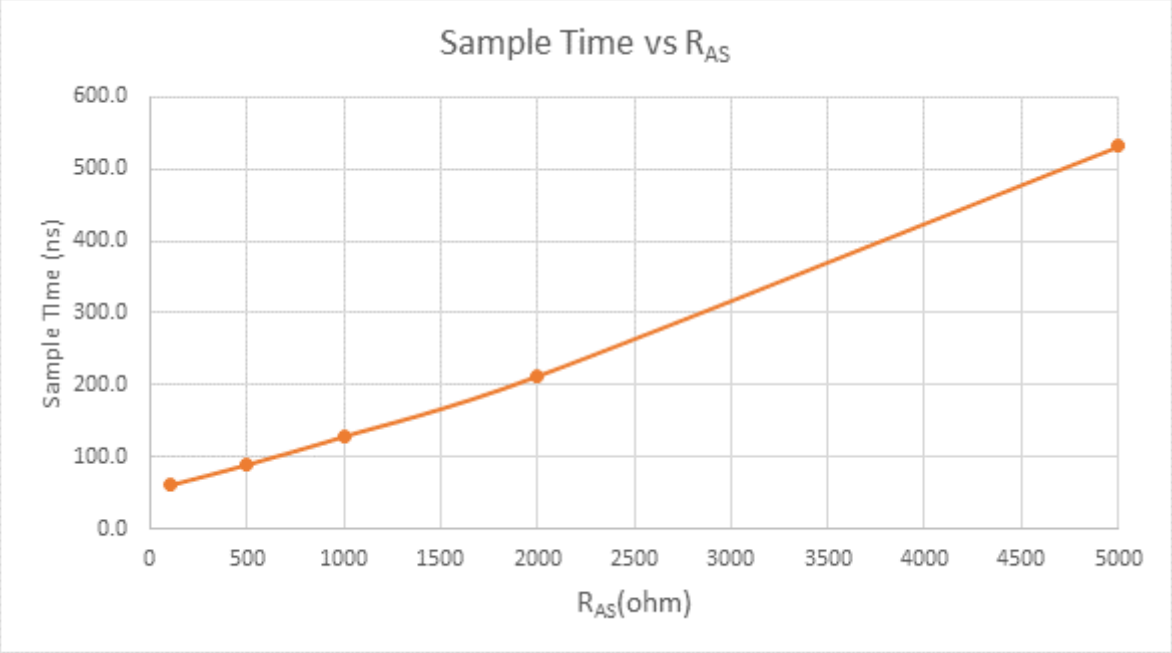

Figure 61. Sample time vs. R_{AS}

5 Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot mode configuration inputs

The following table lists boot option dedicated inputs. These inputs are sampled at reset and can be used to override fuse values, depending on the value of FORCE_BOOT_FROM_FUSE. After this fuse is blown, the Boot mode inputs are ignored by ROM; ROM receives 'boot mode' from the BT_MODE_FUSES fuse. The boot option inputs are in effect when BT_FUSE_SEL fuse is ‘0’ (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the Boot mode pins, see the “System Boot, Fusemap, and eFuse” chapter of the device reference manual.

Table 124. Boot options and associated inputs used for Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
BOOT_MODE[0]	Input	SCU_BOOT_MODE0	Boot mode selection
BOOT_MODE[1]	Input	SCU_BOOT_MODE1	
BOOT_MODE[2]	Input	SCU_BOOT_MODE2	
BOOT_MODE[3]	Input	SCU_BOOT_MODE3	
BOOT_MODE[4]	Input	SCU_BOOT_MODE4	
BOOT_MODE[5]	Input	SCU_BOOT_MODE5	

5.2 Boot devices interfaces allocation

The following table lists the interfaces that can be used by the boot process in accordance with the specific Boot mode configuration. The table also describes the interface’s specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 125. Interface allocation during boot

Interface	IP Instance	Allocated Pads During Boot	Comment
MMC	USDHC-0	EMMC0_CLK, EMMC0_CMD, EMMC0_DATA0, EMMC0_DATA1, EMMC0_DATA2, EMMC0_DATA3, EMMC0_DATA4, EMMC0_DATA5, EMMC0_DATA6, EMMC0_DATA7, EMMC0_RESET_B	4 or 8 bit
SD/MMC	USDHC-1	USDHC1_CLK, USDHC1_CMD, USDHC1_DATA0, USDHC1_DATA1, USDHC1_DATA2, USDHC1_DATA3, USDHC1_DATA4, USDHC1_DATA5, USDHC1_DATA6, USDHC1_DATA7, USDHC1_VSELECT, USDHC1_RESET_B	4 or 8 bit

Table 125. Interface allocation during boot (continued)

Interface	IP Instance	Allocated Pads During Boot	Comment
SD	USDHC-2	USDHC2_CLK, USDHC2_CMD, USDHC2_DATA0, USDHC2_DATA1, USDHC2_DATA2, USDHC2_DATA3, USDHC2_RESET_B, USDHC2_VSELECT, USDHC2_CD_B	4 bit
QSPI	QSPI0	QSPI0A_DATA0, QSPI0A_DATA1, QSPI0A_DATA2, QSPI0A_DATA3, QSPI0A_DQS, QSPI0A_SS0_B, QSPI0A_SS1_B, QSPI0A_SCLK, QSPI0B_SCLK, QSPI0B_DATA0, QSPI0B_DATA1, QSPI0B_DATA2, QSPI0B_DATA3, QSPI0B_DQS, QSPI0B_SS0_B, QSPI0B_SS1_B	4, dual-4, or 8 bit During boot, QSPI0B can only be used in combination with QSPI0A, i.e. booting with 4-bit QSPI0B is not supported.

NAND	GPMI	EMMC0_CLK, EMMC0_CMD, EMMC0_DATA0, EMMC0_DATA1, EMMC0_DATA2, EMMC0_DATA3, EMMC0_DATA4, EMMC0_DATA5, EMMC0_DATA6, EMMC0_DATA7, EMMC0_STROBE, EMMC0_RESET_B,, USDHC1_DATA0, USDHC1_DATA1 USDHC1_DATA2, USDHC1_DATA3, USDHC1_DATA4, USDHC1_DATA5 USDHC1_DATA6, USDHC1_DATA7 USDHC1_STROBE	8 bit
			Boot from CS0 only, but will drive CS1to high when booting if specified in fuse, this is for Multi-CS NAND chip.
			• Single-ended DQS—use EMMC0_CMD
			• Single-ended RE—use USDHC1_DATA5
			• Differential DQS—
			  • _N use USDHC1_DATA2
			  • _P use USDHC1_DATA3
			• Differential RE—
			  • _N use USDHC1_DATA0
			  • _P use USDHC1_DATA1

USB	USB-OTG PHY	USB_OTG1_VBUS, USB_OTG1_DP, USB_OTG1_DN, USB_OTG2_VBUS, USB_OTG2_DP, USB_OTG2_DN	—

6 Package information and contact assignments

This section contains package information and contact assignments for the following package(s):

- FCPBGA, 29 x 29 mm, 0.75 mm pitch

6.1 FCPBGA, 29 x 29 mm, 0.75 mm pitch

This section includes the following information for the 29 x 29 mm, 0.75 mm pitch package:

- Mechanical package drawing
- Ball map
- Contact assignments

6.1.1 29 x 29 mm package case outline

The following figure shows the top, bottom, and side views of the 29 × 29 mm package.

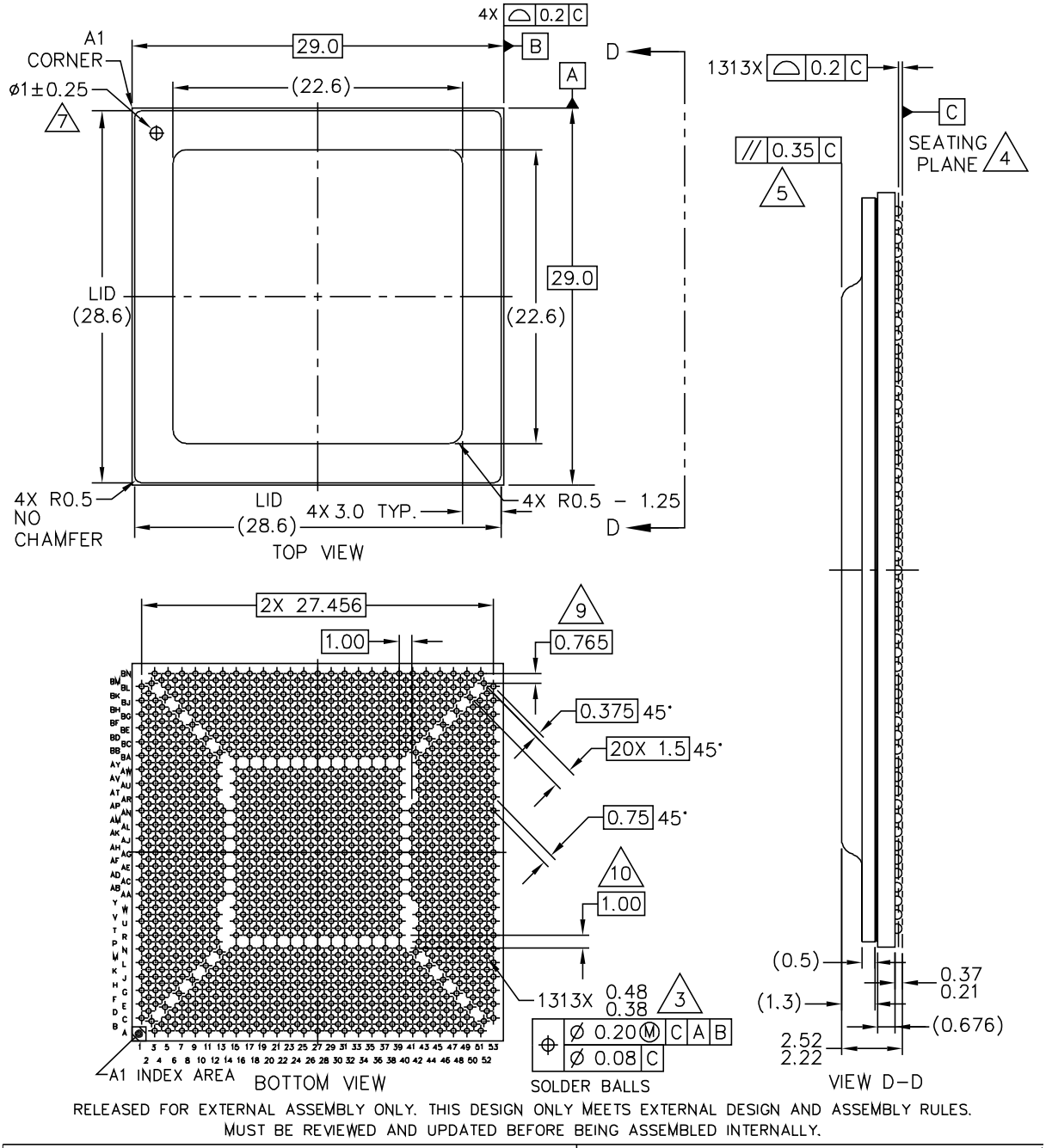

Figure 62. 29 x 29 mm Package Top, Bottom, and Side Views

The notes in the following figure pertain to the preceding figure., “29 x 29 mm Package Top, Bottom, and Side Views.”

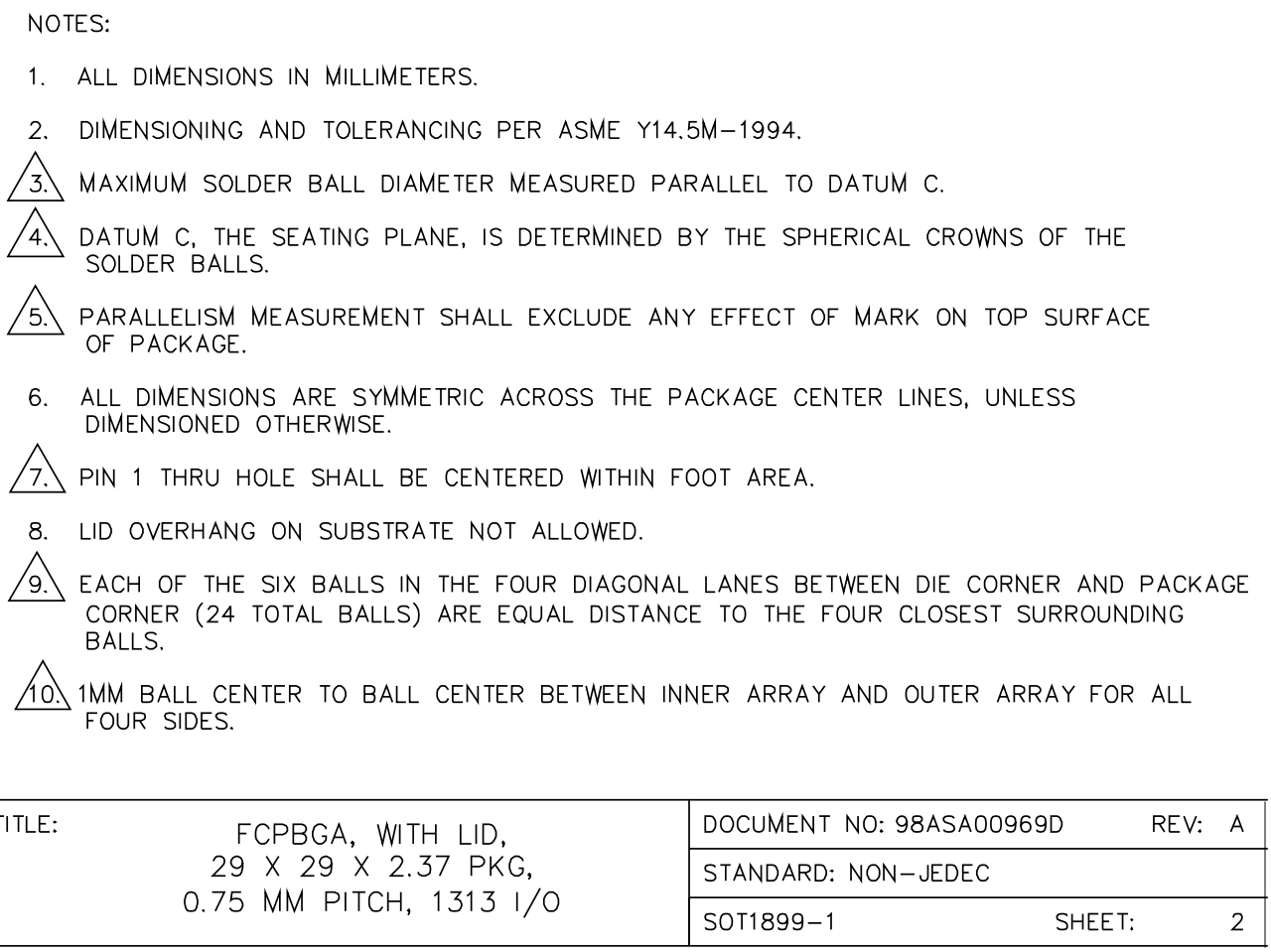

Figure 63. Notes on 29 x 29 mm Package Top, Bottom, and Side Views

6.1.2 29 x 29 mm, 0.75 mm pitch ball map

The following page shows the 29 x 29 mm, 0.75 mm pitch ball map.

29 x 29 mm, 0.75 pitch ballmap

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A			VSS_MAIN		USDHC1_RESET_B		USDHC2_VSELECT		ENET0_MDC		ENET1_REFCLK_125M_25M		ENET1_MDC		PCIE_CTRL0_WAKE_B		PCIE_CTRL0_CLKREQ_B
B				USDHC1_VSELECT		VSS_MAIN		USDHC2_CD_B		ENET0_REFCLK_125M_25M		VSS_MAIN		VSS_MAIN		PCIE_SATA0_TX0_P	
C	VSS_MAIN		FLEXCAN2_RX		FLEXCAN0_RX		USDHC2_RESET_B		VSS_MAIN		VSS_MAIN		ENET1_MDIO		VSS_MAIN		PCIE_SATA0_TX0_N
D		MLB_CLK				VSS_MAIN		USDHC2_WP		ENET0_MDIO		QSPI1A_DATA0		QSPI1A_DATA1		VSS_MAIN	
E	MLB_SIG		MLB_DATA		FLEXCAN1_RX		FLEXCAN2_TX		VSS_MAIN		QSPI1A_DATA3		QSPI1A_DATA2		QSPI0A_SS0_B		QSPI0A_SCLK
F		VSS_MAIN		VSS_MAIN				USB_SS3_TC2		QSPI1A_SCLK		VSS_MAIN		QSPI0A_DATA1		QSPI0A_SS1_B	
G	DDR_CH1_DQ05		DDR_CH1_DQ06		VSS_MAIN		FLEXCAN1_TX		VSS_MAIN		QSPI1A_SS1_B		QSPI0A_DATA0		VSS_MAIN		QSPI0A_DQS
H		DDR_CH1_DM0		DDR_CH1_DQ04		FLEXCAN0_TX				USB_SS3_TC3		QSPI1A_DQS		QSPI0A_DATA2		QSPI0A_DATA3	
J	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		USB_SS3_TC0		QSPI1A_SS0_B		VSS_MAIN		VSS_MAIN		VSS_MAIN
K		DDR_CH1_DQS0_P		DDR_CH1_DQ09		DDR_CH1_DQ03		VSS_MAIN				VSS_MAIN		VSS_MAIN		VSS_MAIN	
L	DDR_CH1_DQS0_N		DDR_CH1_DQ11		DDR_CH1_DQ08		DDR_CH1_DQ02		USB_SS3_TC1		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN
M		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN				VDD_MLB_DIG_1P8_3P3		VDD_USB_SS3_TC_3P3	
N	DDR_CH1_DQS1_P		DDR_CH1_DQ10		DDR_CH1_DQ13		DDR_CH1_DM1		DDR_CH1_DQ01		DDR_CH1_DQ07		VSS_MAIN		VDD_FLEXCAN_1P8_3P3		VDD_ENET_MDIO_1P8_2P5_3P3
P		DDR_CH1_DQS1_N		DDR_CH1_DQ14		DDR_CH1_DQ15		DDR_CH1_DQ12		DDR_CH1_DQ00		VSS_MAIN					
R	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN				VSS_MAIN		VSS_MAIN
T		DDR_CH1_DCF09		DDR_CH1_DCF10		DDR_CH1_DCF08		DDR_CH1_DCF13		DDR_CH1_DTO1		VSS_MAIN				VSS_MAIN	
U	DDR_CH1_DCF16		DDR_CH1_DCF11		DDR_CH1_DCF12		DDR_CH1_DCF00		DDR_CH1_DTO0		DDR_CH1_VREF				VDD_DDR_CH1_VDDQ		VSS_MAIN
V		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN				VDD_DDR_CH1_VDDQ	
W	DDR_CH1_DCF14		DDR_CH1_DCF07		DDR_CH1_CK0_P		DDR_CH1_DCF01		DDR_CH1_DCF06		DDR_CH1_DCF04				VDD_DDR_CH1_VDDQ		VDD_MEMC
Y		DDR_CH1_DCF15		DDR_CH1_CK0_N		DDR_CH1_DCF02		DDR_CH1_DCF03		DDR_CH1_DCF05		VSS_MAIN				VDD_DDR_CH1_VDDQ	
AA	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_DDR_CH1_VDDQ		VSS_MAIN
AB		DDR_CH1_DCF31		DDR_CH1_CK1_N		DDR_CH1_DCF18		DDR_CH1_DCF19		DDR_CH1_DCF24		VSS_MAIN				VDD_DDR_CH1_VDDQ_CKE	
AC	DDR_CH1_DCF30		DDR_CH1_DCF22		DDR_CH1_CK1_P		DDR_CH1_DCF17		DDR_CH1_DCF23		DDR_CH1_DCF20		VSS_MAIN		VDD_DDR_CH1_VDDQ_CKE		VDD_MEMC
AD		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN				VDD_DDR_CH1_VDDQ_CKE	
AE	DDR_CH1_DCF32		DDR_CH1_DCF27		DDR_CH1_DCF29		DDR_CH1_DCF26		DDR_CH1_DCF21		VDD_DDR_CH1_VDDA_PLL_1P8		VSS_MAIN		VDD_DDR_CH1_VDDQ		VSS_MAIN
AF		DDR_CH1_DCF25		DDR_CH1_DCF28		DDR_CH1_DCF33		DDR_CH1_ATO		DDR_CH1_ZQ		VSS_MAIN				VDD_DDR_CH1_VDDQ	
AG	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VDD_DDR_CH1_VDDQ		VDD_MEMC
AH		DDR_CH1_DQS2_N		DDR_CH1_DQ23		DDR_CH1_DQ22		DDR_CH1_DQ21		DDR_CH1_DQ25		VSS_MAIN				VDD_DDR_CH1_VDDQ	
AJ	DDR_CH1_DQS2_P		DDR_CH1_DQ19		DDR_CH1_DQ20		DDR_CH1_DM2		DDR_CH1_DQ24		DDR_CH1_DQ30		VSS_MAIN		VDD_DDR_CH1_VDDQ		VSS_MAIN
AK		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN				VDD_ADC_DIG_1P8	
AL	DDR_CH1_DQS3_N		DDR_CH1_DQ18		DDR_CH1_DQ17		DDR_CH1_DQ27		ADC_IN6		VREFH_ADC		VSS_MAIN		VDD_ADC_1P8		VDD_MAIN
AM		DDR_CH1_DQS3_P		DDR_CH1_DQ16		DDR_CH1_DQ26		VSS_MAIN		VREFL_ADC		VSS_MAIN				VDD_SPI_SAI_1P8_3P3	
AN	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		ADC_IN4		ADC_IN1		VSS_MAIN		VDD_SPI_SAI_1P8_3P3		VSS_MAIN
AP		DDR_CH1_DM3		DDR_CH1_DQ29		ADC_IN7		ADC_IN2		ADC_IN0		VSS_MAIN				VDD_ESAI0_MCLK_1P8_3P3	
AR	DDR_CH1_DQ28		DDR_CH1_DQ31		VSS_MAIN		ADC_IN5		ADC_IN3		VSS_MAIN				VDD_ESAI0_MCLK_1P8_3P3		VDD_MAIN
AT		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		ESAI1_TX5_RX0		VSS_MAIN				VSS_MAIN	
AU	SAI1_TXD		SAI1_RXFS		SAI1_TXC		ESAI0_TX5_RX0		ESAI0_TX2_RX3		ESAI1_TX2_RX3				VDD_ESAI1_SPDIF_SPI_1P8_3P3		VSS_MAIN
AV		SAI1_TXFS		SAI1_RXD		SAI1_RXC		ESAI0_TX4_RX1		ESAI1_TX3_RX2		VSS_MAIN				VDD_HDMI_TX0_1P0	
AW	SPI2_CS0		VSS_MAIN		SPI2_SCK		VSS_MAIN		ESAI0_FSR		VSS_MAIN				VDD_HDMI_TX0_LDO_1P0_CAP		VDD_HDMI_TX0_1P8
AY		SPI2_CS1		SPI2_SDI		SPI0_SDO		ESAI0_SCKT		ESAI1_SCKT		ESAI1_TX4_RX1					
BA	SPI2_SDO		SPI0_CS1		SPI0_SDI		ESAI0_TX1		ESAI0_TX0		ESAI1_TX1		VSS_MAIN		VSS_MAIN		VSS_MAIN
BB		VSS_MAIN		SPI0_SCK		VSS_MAIN		ESAI0_SCKR		VSS_MAIN				VSS_MAIN		VSS_MAIN	
BC	SPI0_CS0		MCLK_IN0		ESAI0_TX3_RX2		SPDIF0_RX		SPDIF0_TX		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN
BD		ANA_TEST_OUT1_N		MCLK_OUT0		SPDIF0_EXT_CLK		SPI3_CS1				ESAI1_SCKR		VSS_MAIN		VSS_MAIN	
BE	ANA_TEST_OUT1_P		VSS_MAIN		SPI3_SDI		VSS_MAIN		VSS_MAIN		ESAI1_FSR		HDMI_RX0_DDC_SDA		MIPI_CSI1_I2C0_SDA		MIPI_CSI0_DATA3_N
BF		SPI3_SDO		VSS_MAIN		SPI3_SCK				ESAI1_TX0		ESAI1_FST		HDMI_RX0_HPD		MIPI_CSI0_DATA3_P	
BG	HDMI_TX0_DDC_SCL		HDMI_TX0_AUX_N		SPI3_CS0		VSS_MAIN		ESAI0_FST		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN
BH		HDMI_TX0_AUX_P		VSS_MAIN				HDMI_TX0_HPD		HDMI_RX0_DDC_SCL		MIPI_CSI1_DATA3_N		MIPI_CSI1_DATA1_N		MIPI_CSI1_CLK_N	
BJ	HDMI_TX0_CEC		VSS_MAIN		VSS_MAIN		HDMI_TX0_REXT		HDMI_RX0_CEC		HDMI_RX0_REXT		MIPI_CSI1_DATA3_P		MIPI_CSI1_DATA1_P		MIPI_CSI1_CLK_P
BK		HDMI_TX0_CLK_EDP3_N				VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN	
BL	VSS_MAIN		HDMI_TX0_CLK_EDP3_P		HDMI_TX0_DATA0_EDP2_P		HDMI_TX0_DATA1_EDP1_P		HDMI_TX0_DATA2_EDP0_P		HDMI_RX0_CLK_N		HDMI_RX0_ARC_N		HDMI_RX0_DATA0_N		HDMI_RX0_DATA1_N
BM				HDMI_TX0_DATA0_EDP2_N		HDMI_TX0_DATA1_EDP1_N		HDMI_TX0_DATA2_EDP0_N		VSS_MAIN		HDMI_RX0_CLK_P		HDMI_RX0_ARC_P		HDMI_RX0_DATA0_P	
BN			VSS_MAIN		HDMI_TX0_DDC_SDA		HDMI_TX0_TS_SDA		HDMI_TX0_TS_SCL		HDMI_RX0_MON_5V		MIPI_CSI1_GPIO0_01		MIPI_CSI1_GPIO0_00		MIPI_CSI1_I2C0_SCL

	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
A		PCIE_SATA0_RX0_P		PCIE1_RX0_P		VSS_MAIN		PCIE_CTRL1_CLKREQ_B		PCIE_CTRL1_WAKE_B		PCIE0_RX0_P		VSS_MAIN		USB_SS3_TX_P		USB_OTG2_VBUS
B	VSS_MAIN		PCIE_SATA0_RX0_N		PCIE1_RX0_N		PCIE1_TX0_P		PCIE0_TX0_P		VSS_MAIN		PCIE0_RX0_N		USB_SS3_TX_N		USB_SS3_RX_N	
C		VSS_MAIN		VSS_MAIN		VSS_MAIN		PCIE1_TX0_N		PCIE0_TX0_N		VSS_MAIN		VSS_MAIN		VSS_MAIN		USB_SS3_RX_P
D	VSS_MAIN		PCIE_CTRL0_PERST_B		PCIE_REXT		VSS_MAIN		VSS_MAIN		VSS_MAIN		MLB_SIG_P		MLB_CLK_P		VSS_MAIN	
E		VSS_MAIN		VSS_MAIN		PCIE_REF_QR		PCIE_SATA_REFCLK100M_N		USB_SS3_REXT		USB_OTG2_REXT		MLB_SIG_N		MLB_CLK_N		MLB_DATA_N
F	QSPI0B_SCLK		QSPI0B_DATA3		QSPI0B_SS0_B		VSS_MAIN		PCIE_SATA_REFCLK100M_P		USB_HSIC0_STROBE		USB_OTG2_ID		VSS_MAIN		MLB_DATA_P	
G		QSPI0B_DATA2		VSS_MAIN		VSS_MAIN		PCIE_CTRL1_PERST_B		VSS_MAIN		EMMC0_DATA0		EMMC0_DATA2		VSS_MAIN		EMMC0_DATA7
H	QSPI0B_DATA0		QSPI0B_DATA1		QSPI0B_DQS		QSPI0B_SS1_B		USB_HSIC0_DATA		EMMC0_CLK		EMMC0_DATA1		EMMC0_DATA3		EMMC0_DATA5	
J		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		EMMC0_CMD		VSS_MAIN		VSS_MAIN		EMMC0_DATA4		VSS_MAIN
K	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN	
L		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN
M	VDD_QSPI1A_1P8_3P3		PCIE_SATA0_PHY_PLL_REF_RETURN		VDD_PCIE1_PLL_1P8		VDD_PCIE_SATA0_1P0		VDD_PCIE0_1P0		PCIE0_PHY_PLL_REF_RETURN		VDD_USB_SS3_LDO_1P0_CAP		VDD_USB_OTG1_1P0		VDD_USB_OTG2_3P3	
N		VDD_QSPI0_1P8_3P3		VDD_PCIE_SATA0_PLL_1P8		PCIE1_PHY_PLL_REF_RETURN		VDD_PCIE1_1P0		VDD_PCIE0_PLL_1P8		VDD_PCIE_LDO_1P0_CAP		VDD_USB_OTG2_1P0		VDD_USB_OTG1_3P3		VDD_EMMC0_1P8_3P3
P																		
R		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN
T	VDD_USDHC_VSELECT_1P8_3P3		VSS_MAIN		VDD_PCIE_DIG_1P8		VSS_MAIN		VDD_PCIE_IOB_1P8		VSS_MAIN		VDD_MLB_1P8		VSS_MAIN		VDD_MAIN	
U		VDD_MAIN		VSS_MAIN		VDD_MAIN		VDD_ANA1_1P8		VDD_PCIE_LDO_1P8		VDD_ANA0_1P8		VDD_ANA0_1P8		VSS_MAIN		VDD_GPU1
V	VSS_MAIN		VDD_GPU0		VSS_MAIN		VDD_MAIN		VDD_USB_HSIC0_1P2		VDD_USB_HSIC0_1P8		VSS_MAIN		VDD_MAIN		VSS_MAIN	
W		VSS_MAIN		VDD_GPU0		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU1		VSS_MAIN
Y	VDD_GPU0		VSS_MAIN		VDD_GPU0		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU1	
AA		VDD_GPU0		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU1
AB	VSS_MAIN		VDD_GPU0		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU1		VSS_MAIN	
AC		VSS_MAIN		VDD_GPU0		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU1		VSS_MAIN
AD	VDD_GPU0		VSS_MAIN		VDD_GPU0		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU1	
AE		VDD_GPU0		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_GPU1
AF	VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN	
AG		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MEMC		VSS_MAIN		VDD_MEMC		VSS_MAIN		VDD_MAIN		VSS_MAIN
AH	VDD_MAIN		VSS_MAIN		VDD_MEMC		VSS_MAIN		VDD_MEMC		VSS_MAIN		VDD_MEMC		VSS_MAIN		VDD_MAIN	
AJ		VDD_MAIN		VSS_MAIN		VDD_MEMC		VSS_MAIN		VDD_MEMC		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_ANA2_1P8
AK	VSS_MAIN		VDD_ANA3_1P8		VSS_MAIN		VDD_MEMC		VSS_MAIN		VDD_MEMC		VSS_MAIN		VDD_MAIN		VSS_MAIN	
AL		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_A72		VSS_MAIN		VDD_A72		VSS_MAIN
AM	VDD_MAIN		VSS_MAIN		VDD_A53		VSS_MAIN		VDD_A53		VSS_MAIN		VDD_A72		VSS_MAIN		VDD_A72	
AN		VDD_MAIN		VSS_MAIN		VDD_A53		VSS_MAIN		VDD_A72		VSS_MAIN		VDD_A72		VSS_MAIN		VDD_A72
AP	VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_A53		VSS_MAIN		VDD_A72		VSS_MAIN		VDD_A72		VSS_MAIN	
AR		VSS_MAIN		VDD_A53		VSS_MAIN		VDD_A53		VSS_MAIN		VDD_A72		VSS_MAIN		VDD_A72		VSS_MAIN
AT	VDD_MAIN		VSS_MAIN		VDD_A53		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_MAIN		VSS_MAIN		VDD_A72	
AU		VDD_HDMI_RX0_LDO0_1P0_CAP		VDD_HDMI_RX0_LDO1_1P0_CAP		VDD_MIPI_CSI1_1P8		VSS_MAIN		VDD_MIPI_DSI_DIG_1P8_3P3		VDD_MIPI_DSI0_1P0		VSS_MAIN		VSS_MAIN		VDD_MAIN
AV	VDD_HDMI_RX0_1P8		VDD_HDMI_RX0_VH_RX_3P3		VDD_MIPI_CSI_DIG_1P8		VDD_MIPI_CSI0_1P8		VDD_MIPI_CSI0_1P0		VDD_MIPI_DSI1_1P0		VDD_MIPI_DSI1_1P8		VDD_LVDS_DIG_1P8_3P3		VDD_LVDS0_1P8	
AW		VSS_MAIN		VDD_HDMI_TX0_DIG_3P3		VSS_MAIN		VDD_MIPI_CSI1_1P0		VDD_MIPI_DSI1_PLL_1P0		VDD_MIPI_DSI0_PLL_1P0		VDD_MIPI_DSI0_1P8		VDD_LVDS1_1P8		VDD_LVDS1_1P0
AY																		
BA		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN
BB	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN	
BC		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN
BD	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		MIPI_DSI0_GPIO0_01		MIPI_DSI0_GPIO0_00		LVDS1_I2C1_SCL		LVDS1_GPIO00	
BE		MIPI_CSI0_DATA1_N		MIPI_CSI0_CLK_N		MIPI_CSI0_DATA0_N		MIPI_CSI0_DATA2_N		MIPI_DSI1_I2C0_SCL		MIPI_DSI0_I2C0_SCL		MIPI_DSI0_I2C0_SDA		LVDS1_I2C0_SDA		LVDS0_I2C1_SDA
BF	MIPI_CSI0_DATA1_P		MIPI_CSI0_CLK_P		MIPI_CSI0_DATA0_P		MIPI_CSI0_DATA2_P		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN	
BG		VSS_MAIN		VSS_MAIN		VSS_MAIN		MIPI_DSI1_I2C0_SDA		MIPI_DSI1_DATA3_P		MIPI_DSI1_DATA1_P		MIPI_DSI1_CLK_P		MIPI_DSI1_DATA0_P		MIPI_DSI1_DATA2_P
BH	MIPI_CSI1_DATA0_N		MIPI_CSI1_DATA2_N		VSS_MAIN		MIPI_CSI0_I2C0_SCL		MIPI_DSI1_DATA3_N		MIPI_DSI1_DATA1_N		MIPI_DSI1_CLK_N		MIPI_DSI1_DATA0_N		MIPI_DSI1_DATA2_N	
BJ		MIPI_CSI1_DATA0_P		MIPI_CSI1_DATA2_P		MIPI_CSI0_MCLK_OUT		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN
BK	VSS_MAIN		VSS_MAIN		VSS_MAIN		MIPI_DSI1_GPIO0_01		MIPI_DSI0_DATA1_P		MIPI_DSI0_DATA0_P		LVDS1_CH1_TX3_N		LVDS1_CH1_TX1_N		LVDS1_CH1_CLK_N	
BL		HDMI_RX0_DATA2_N		VSS_MAIN		MIPI_CSI0_GPIO0_00		MIPI_DSI0_DATA3_P		MIPI_DSI0_CLK_P		MIPI_DSI0_DATA2_P		LVDS1_CH1_TX2_N		LVDS1_CH1_TX0_N		LVDS1_I2C0_SCL
BM	HDMI_RX0_DATA1_P		HDMI_RX0_DATA2_P		MIPI_CSI0_GPIO0_01		MIPI_DSI1_GPIO0_00		MIPI_DSI0_DATA1_N		MIPI_DSI0_DATA0_N		LVDS1_CH1_TX3_P		LVDS1_CH1_TX1_P		LVDS1_CH1_CLK_P	
BN		MIPI_CSI0_I2C0_SDA		VSS_MAIN		MIPI_CSI1_MCLK_OUT		MIPI_DSI0_DATA3_N		MIPI_DSI0_CLK_N		MIPI_DSI0_DATA2_N		LVDS1_CH1_TX2_P		LVDS1_CH1_TX0_P		LVDS1_I2C1_SDA

	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53
A		USB_OTG1_ID		USB_OTG1_VBUS		ENET0_RGMII_TXC		ENET0_RGMII_TXD0		ENET0_RGMII_TXD2		ENET0_RGMII_RXD0		ENET1_RGMII_TXD0		VSS_MAIN		
B	VSS_MAIN		USB_OTG2_DP		USB_OTG1_DP		ENET0_RGMII_TXD1		ENET0_RGMII_RXC		VSS_MAIN		ENET1_RGMII_TX_CTL		ENET1_RGMII_RXC			
C		USB_OTG2_DN		USB_OTG1_DN		VSS_MAIN		VSS_MAIN		ENET0_RGMII_RXD2		ENET1_RGMII_TXD1		VSS_MAIN		ENET1_RGMII_RXD1		VSS_MAIN
D	VSS_MAIN		VSS_MAIN		VSS_MAIN		ENET0_RGMII_TXD3		ENET0_RGMII_RXD1		ENET1_RGMII_TXC		ENET1_RGMII_TXD3				ENET1_RGMII_RXD2	
E		USDHC1_DATA0		USDHC1_DATA2		ENET0_RGMII_TX_CTL		ENET0_RGMII_RX_CTL		ENET0_RGMII_RXD3		VSS_MAIN		ENET1_RGMII_RX_CTL		ENET1_RGMII_RXD0		ENET1_RGMII_RXD3
F	VSS_MAIN		USDHC1_DATA1		USDHC1_DATA3		USDHC1_DATA6		VSS_MAIN		USDHC2_CLK				VSS_MAIN		VSS_MAIN	
G		EMMC0_STROBE		VSS_MAIN		USDHC1_CMD		USDHC1_DATA5		USDHC2_DATA1		ENET1_RGMII_TXD2		VSS_MAIN		DDR_CH0_DQ06		DDR_CH0_DQ05
H	EMMC0_DATA6		EMMC0_RESET_B		USDHC1_DATA4		USDHC1_DATA7		USDHC2_CMD				USDHC2_DATA0		DDR_CH0_DQ04		DDR_CH0_DM0	
J		VSS_MAIN		USDHC1_CLK		VSS_MAIN		USDHC1_STROBE		USDHC2_DATA3		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN
K	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN				VSS_MAIN		DDR_CH0_DQ03		DDR_CH0_DQ09		DDR_CH0_DQS0_P	
L		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		USDHC2_DATA2		DDR_CH0_DQ02		DDR_CH0_DQ08		DDR_CH0_DQ11		DDR_CH0_DQS0_N
M	VDD_USDHC1_1P8_3P3		VDD_USDHC2_1P8_3P3		VDD_ENET0_1P8_3P3				VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN	
N		VDD_USDHC1_1P8_3P3		VDD_ENET0_1P8_3P3		VSS_MAIN		DDR_CH0_DQ07		DDR_CH0_DQ01		DDR_CH0_DM1		DDR_CH0_DQ13		DDR_CH0_DQ10		DDR_CH0_DQS1_P
P							VSS_MAIN		DDR_CH0_DQ00		DDR_CH0_DQ12		DDR_CH0_DQ15		DDR_CH0_DQ14		DDR_CH0_DQS1_N	
R		VSS_MAIN		VSS_MAIN				VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN
T	VSS_MAIN		VDD_ENET1_1P8_2P5_3P3				VSS_MAIN		DDR_CH0_DTO1		DDR_CH0_DCF13		DDR_CH0_DCF08		DDR_CH0_DCF10		DDR_CH0_DCF09	
U		VSS_MAIN		VDD_DDR_CH0_VDDQ				DDR_CH0_VREF		DDR_CH0_DTO0		DDR_CH0_DCF00		DDR_CH0_DCF12		DDR_CH0_DCF11		DDR_CH0_DCF16
V	VDD_GPU1		VDD_DDR_CH0_VDDQ				VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN	
W		VDD_MEMC		VDD_DDR_CH0_VDDQ				DDR_CH0_DCF04		DDR_CH0_DCF06		DDR_CH0_DCF01		DDR_CH0_CK0_P		DDR_CH0_DCF07		DDR_CH0_DCF14
Y	VSS_MAIN		VDD_DDR_CH0_VDDQ				VSS_MAIN		DDR_CH0_DCF05		DDR_CH0_DCF03		DDR_CH0_DCF02		DDR_CH0_CK0_N		DDR_CH0_DCF15	
AA		VSS_MAIN		VDD_DDR_CH0_VDDQ		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN
AB	VDD_GPU1		VDD_DDR_CH0_VDDQ_CKE				VSS_MAIN		DDR_CH0_DCF24		DDR_CH0_DCF19		DDR_CH0_DCF18		DDR_CH0_CK1_N		DDR_CH0_DCF31	
AC		VDD_MEMC		VDD_DDR_CH0_VDDQ_CKE		VSS_MAIN		DDR_CH0_DCF20		DDR_CH0_DCF23		DDR_CH0_DCF17		DDR_CH0_CK1_P		DDR_CH0_DCF22		DDR_CH0_DCF30
AD	VSS_MAIN		VDD_DDR_CH0_VDDQ_CKE				VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN	
AE		VSS_MAIN		VDD_DDR_CH0_VDDQ		VSS_MAIN		VDD_DDR_CH0_VDDA_PLL_1P8		DDR_CH0_DCF21		DDR_CH0_DCF26		DDR_CH0_DCF29		DDR_CH0_DCF27		DDR_CH0_DCF32
AF	VDD_MAIN		VDD_DDR_CH0_VDDQ				VSS_MAIN		DDR_CH0_ZQ		DDR_CH0_ATO		DDR_CH0_DCF33		DDR_CH0_DCF28		DDR_CH0_DCF25	
AG		VDD_MEMC		VDD_DDR_CH0_VDDQ		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN
AH	VSS_MAIN		VDD_DDR_CH0_VDDQ				VSS_MAIN		DDR_CH0_DQ25		DDR_CH0_DQ21		DDR_CH0_DQ22		DDR_CH0_DQ23		DDR_CH0_DQS2_N	
AJ		VSS_MAIN		VDD_DDR_CH0_VDDQ		VSS_MAIN		DDR_CH0_DQ30		DDR_CH0_DQ24		DDR_CH0_DM2		DDR_CH0_DQ20		DDR_CH0_DQ19		DDR_CH0_DQS2_P
AK	VDD_MAIN		VSS_MAIN				VDD_SIM0_1P8_3P3		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN	
AL		VDD_MAIN		VDD_M4_GPT_UART_1P8_3P3		VSS_MAIN		SIM0_PD		SIM0_CLK		DDR_CH0_DQ27		DDR_CH0_DQ17		DDR_CH0_DQ18		DDR_CH0_DQS3_N
AM	VSS_MAIN		VDD_M4_GPT_UART_1P8_3P3				VSS_MAIN		M40_I2C0_SCL		VSS_MAIN		DDR_CH0_DQ26		DDR_CH0_DQ16		DDR_CH0_DQS3_P	
AN		VDD_CP_1P8		VDD_SCU_1P8		VSS_MAIN		VSS_MAIN		SIM0_IO		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN
AP	VDD_MAIN		VDD_SCU_1P8				VDD_M1P8_CAP		M41_GPIO0_00		SIM0_GPIO0_00		SIM0_RST		DDR_CH0_DQ29		DDR_CH0_DM3	
AR		VDD_MAIN		VDD_SCU_ANA_1P8				UART1_RTS_B		M41_I2C0_SCL		M40_GPIO0_00		VSS_MAIN		DDR_CH0_DQ31		DDR_CH0_DQ28
AT	VSS_MAIN		VDD_SNVS_4P2				VSS_MAIN		UART1_RX		VSS_MAIN		SIM0_POWER_EN		VSS_MAIN		VSS_MAIN	
AU		VSS_MAIN		VDD_SCU_XTAL_1P8				SCU_GPIO0_00		UART0_RTS_B		M41_GPIO0_01		M41_I2C0_SDA		M40_I2C0_SDA		M40_GPIO0_01
AV	VDD_LVDS0_1P0		VSS_MAIN				VSS_MAIN		SCU_GPIO0_01		UART1_CTS_B		UART0_TX		UART0_RX		GPT0_CAPTURE	
AW		VSS_MAIN		VDD_SNVS_LDO_1P8_CAP				VSS_MAIN		SCU_GPIO0_02		VSS_MAIN		UART0_CTS_B		VSS_MAIN		GPT0_COMPARE
AY							SCU_BOOT_MODE4		SCU_GPIO0_05		PMIC_I2C_SCL		UART1_TX		GPT1_CAPTURE		GPT0_CLK	
BA		VSS_MAIN		VSS_MAIN		VSS_MAIN		SCU_BOOT_MODE3		VSS_MAIN		SCU_PMIC_STANDBY		JTAG_TMS		GPT1_COMPARE		GPT1_CLK
BB	VSS_MAIN		VSS_MAIN		VSS_MAIN				SCU_BOOT_MODE0		SCU_GPIO0_03		VSS_MAIN		SCU_WDOG_OUT		VSS_MAIN	
BC		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		SCU_BOOT_MODE1		SCU_GPIO0_04		TEST_MODE_SELECT		JTAG_TCK		SCU_PMIC_MEMC_ON
BD	LVDS0_I2C0_SDA		LVDS0_I2C0_SCL		LVDS0_GPIO01		SNVS_TAMPER_OUT1				SNVS_TAMPER_OUT0		VSS_MAIN		VSS_MAIN		JTAG_TDO	
BE		LVDS0_I2C1_SCL		LVDS0_GPIO00		SNVS_TAMPER_IN0		SNVS_TAMPER_IN1		VSS_MAIN		ON_OFF_BUTTON		POR_B		JTAG_TDI		JTAG_TRST_B
BF	VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN				SCU_GPIO0_07		PMIC_EARLY_WARNING		VSS_MAIN	
BG		LVDS0_CH1_TX3_N		LVDS0_CH1_TX2_N		LVDS0_CH1_TX1_N		LVDS0_CH1_TX0_N		LVDS0_CH1_CLK_N		VSS_MAIN		SCU_GPIO0_06		PMIC_I2C_SDA		ANA_TEST_OUT0_P
BH	LVDS1_GPIO01		LVDS0_CH1_TX3_P		LVDS0_CH1_TX2_P		LVDS0_CH1_TX1_P		LVDS0_CH1_TX0_P		LVDS0_CH1_CLK_P				PMIC_INT_B		ANA_TEST_OUT0_N	
BJ		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		VSS_MAIN		SCU_BOOT_MODE2
BK	LVDS1_CH0_CLK_N		LVDS1_CH0_TX1_N		LVDS1_CH0_TX3_N		LVDS0_CH0_TX0_N		LVDS0_CH0_TX2_N		VSS_MAIN		VSS_SCU_XTAL				SCU_BOOT_MODE5	
BL		LVDS1_CH0_TX0_N		LVDS1_CH0_TX2_N		LVDS0_CH0_CLK_N		LVDS0_CH0_TX1_N		LVDS0_CH0_TX3_N		RTC_XTALO		XTALO		PMIC_ON_REQ		VSS_MAIN
BM	LVDS1_CH0_CLK_P		LVDS1_CH0_TX1_P		LVDS1_CH0_TX3_P		LVDS0_CH0_TX0_P		LVDS0_CH0_TX2_P		VSS_MAIN		VSS_SCU_XTAL		VSS_SCU_XTAL			
BN		LVDS1_CH0_TX0_P		LVDS1_CH0_TX2_P		LVDS0_CH0_CLK_P		LVDS0_CH0_TX1_P		LVDS0_CH0_TX3_P		RTC_XTALI		XTALI		VSS_SCU_XTAL		

6.1.3 29 x 29 mm power supplies and functional contact assignments

The following table shows power supplies contact assignments for the 29 × 29 mm package.

Table 126. 29 x 29 mm power supplies contact assignments

Power rail	Ball reference
VDD_A53	AM22, AM26, AN23, AP24, AR21, AR25, AT22
VDD_A72	AL29, AL33, AM30, AM34, AN27, AN31, AN35, AP28, AP32, AR29, AR33, AT34
VDD_ADC_1P8	AL15
VDD_ADC_DIG_1P8	AK16
VDD_ANA0_1P8	U29, U31
VDD_ANA1_1P8	U25
VDD_ANA2_1P8	AJ35
VDD_ANA3_1P8	AK20
VDD_CP_1P8	AN37
VDD_DDR_CH0_VDDA_PLL_1P8	AE43
VDD_DDR_CH0_VDDQ	AA39, AE39, AF38, AG39, AH38, AJ39, U39, V38, W39, Y38
VDD_DDR_CH0_VDDQ_CKE	AB38, AC39, AD38
VDD_DDR_CH1_VDDA_PLL_1P8	AE11
VDD_DDR_CH1_VDDQ	AA15, AE15, AF16, AG15, AH16, AJ15, U15, V16, W15, Y16
VDD_DDR_CH1_VDDQ_CKE	AB16, AC15, AD16
VDD_EMMC0_1P8_3P3	N35
VDD_ENET_MDIO_1P8_3P3	N17
VDD_ENET0_1P8_3P3	M40, N39
VDD_ENET1_1P8_2P5_3P3	T38
VDD_ESAI0_MCLK_1P8_3P3	AP16, AR15
VDD_ESAI1_SPDIF_SPI_1P8_3P3	AU15
VDD_FLEXCAN_1P8_3P3	N15
VDD_GPU0	AA19, AB20, AC21, AD18, AD22, AE19, V20, W21, Y18, Y22
VDD_GPU1	AA35, AB32, AB36, AC33, AD34, AE35, U35, V36, W33, Y34
VDD_HDMI_RX0_1P8[1]	AV18
VDD_HDMI_RX0_LDO0_1P0_CAP[1]	AU19
VDD_HDMI_RX0_LDO1_1P0_CAP[1]	AU21
VDD_HDMI_RX0_VH_RX_3P3[1]	AV20
VDD_HDMI_TX0_1P0	AV16

Table 126. 29 x 29 mm power supplies contact assignments (continued)

Power rail	Ball reference
VDD_HDMI_TX0_1P8	AW17
VDD_HDMI_TX0_DIG_3P3	AW21
VDD_HDMI_TX0_LDO_1P0_CAP	AW15
VDD_LVDS_DIG_1P8_3P3	AV32
VDD_LVDS0_1P0	AV36
VDD_LVDS0_1P8	AV34
VDD_LVDS1_1P0	AW35
VDD_LVDS1_1P8	AW33
VDD_M1P8_CAP	AP42
VDD_M4_GPT_UART_1P8_3P3	AL39, AM38
VDD_MAIN	AA23, AA27, AA31, AB24, AB28, AC25, AC29, AD26, AD30, AE23, AE27, AE31, AF20, AF24, AF28, AF32, AF36, AG21, AG33, AH18, AH34, AJ19, AJ31, AK32, AK36, AL17, AL21, AL25, AL37, AM18, AN19, AP20, AP36, AR17, AR37, AT18, AT26, AT30, AU35, T34, U19, U23, V24, V32, W25, W29, Y26, Y30
VDD_MEMC	AC17, AC37, AG17, AG25, AG29, AG37, AH22, AH26, AH30, AJ23, AJ27, AK24, AK28, W17, W37
VDD_MIPI_CSI_DIG_1P8	AV22
VDD_MIPI_CSI0_1P0	AV26
VDD_MIPI_CSI0_1P8	AV24
VDD_MIPI_CSI1_1P0	AW25
VDD_MIPI_CSI1_1P8	AU23
VDD_MIPI_DSI_DIG_1P8_3P3	AU27
VDD_MIPI_DSI0_1P0	AU29
VDD_MIPI_DSI0_1P8	AW31
VDD_MIPI_DSI0_PLL_1P0	AW29
VDD_MIPI_DSI1_1P0	AV28
VDD_MIPI_DSI1_1P8	AV30
VDD_MIPI_DSI1_PLL_1P0	AW27
VDD_MLB_1P8[2]	T30
VDD_MLB_DIG_1P8_3P3[3]	M14
VDD_PCIE_DIG_1P8_3P3	T22
VDD_PCIE_IOB_1P8	T26
VDD_PCIE_LDO_1P0_CAP	N29
VDD_PCIE_LDO_1P8	U27

Table 126. 29 x 29 mm power supplies contact assignments (continued)

Power rail	Ball reference
VDD_PCIE_SATA0_1P0	M24
VDD_PCIE_SATA0_PLL_1P8	N21
VDD_PCIE0_1P0	M26
VDD_PCIE0_PLL_1P8	N27
VDD_PCIE1_1P0	N25
VDD_PCIE1_PLL_1P8	M22
VDD_QSPI0_1P8_3P3	N19
VDD_QSPI1A_1P8_3P3	M18
VDD_SCU_1P8	AN39, AP38
VDD_SCU_ANA_1P8	AR39
VDD_SCU_XTAL_1P8	AU39
VDD_SIM0_1P8_3P3	AK42
VDD_SNVS_4P2	AT38
VDD_SNVS_LDO_1P8_CAP	AW39
VDD_SPI_SAI_1P8_3P3	AM16, AN15
VDD_USB_HSIC0_1P2	V26
VDD_USB_HSIC0_1P8	V28
VDD_USB_OTG1_1P0	M32
VDD_USB_OTG1_3P3	N33
VDD_USB_OTG2_1P0	N31
VDD_USB_OTG2_3P3	M34
VDD_USB_SS3_LDO_1P0_CAP	M30
VDD_USB_SS3_TC_3P3	M16
VDD_USDHC_VSELECT_1P8_3P3	T18
VDD_USDHC1_1P8_3P3	M36, N37
VDD_USDHC2_1P8_3P3	M38
VREFH_ADC	AL11
VREFL_ADC	AM10

Table 126. 29 x 29 mm power supplies contact assignments (continued)

Power rail	Ball reference
VSS_MAIN	A23, A3, A31, A51, AA1, AA11, AA13, AA17, AA21, AA25, AA29, AA3, AA33, AA37, AA41, AA43, AA45, AA47, AA49, AA5, AA51, AA53, AA7, AA9, AB12, AB18, AB22, AB26, AB30, AB34, AB42, AC13, AC19, AC23, AC27, AC31, AC35, AC41, AD10, AD12, AD2, AD20, AD24, AD28, AD32, AD36, AD4, AD42, AD44, AD46, AD48, AD50, AD52, AD6, AD8, AE13, AE17, AE21, AE25, AE29, AE33, AE37, AE41, AF12, AF18, AF22, AF26, AF30, AF34, AF42, AG1, AG11, AG13, AG19, AG23, AG27, AG3, AG31, AG35, AG41, AG43, AG45, AG47, AG49, AG5, AG51, AG53, AG7, AG9, AH12, AH20, AH24, AH28, AH32, AH36, AH42, AJ13, AJ17, AJ21, AJ25, AJ29, AJ33, AJ37, AJ41, AK10, AK12, AK18, AK2, AK22, AK26, AK30, AK34, AK38, AK4, AK44, AK46, AK48, AK50, AK52, AK6, AK8, AL13, AL19, AL23, AL27, AL31, AL35, AL41, AM12, AM20, AM24, AM28, AM32, AM36, AM42, AM46, AM8, AN1, AN13, AN17, AN21, AN25, AN29, AN3, AN33, AN41, AN43, AN47, AN49, AN5, AN51, AN53, AN7, AP12, AP18, AP22, AP26, AP30, AP34, AR11, AR19, AR23, AR27, AR31, AR35, AR49, AR5, AT12, AT16, AT2, AT20, AT24, AT28, AT32, AT36, AT4, AT42, AT46, AT50, AT52, AT6, AT8, AU17, AU25, AU31, AU33, AU37, AV12, AV38, AV42, AW11, AW19, AW23, AW3, AW37, AW43, AW47, AW51, AW7, B12, B14, B18, B28, B36, B46, B6, BA13, BA15, BA17, BA19, BA21, BA23, BA25, BA27, BA29, BA31, BA33, BA35, BA37, BA39, BA41, BA45, BB10, BB14, BB16, BB18, BB2, BB20, BB22, BB24, BB26, BB28, BB30, BB32, BB34, BB36, BB38, BB40, BB48, BB52, BB6, BC11, BC13, BC15, BC17, BC19, BC21, BC23, BC25, BC27, BC29, BC31, BC33, BC35, BC37, BC39, BC41, BC43, BD14, BD16, BD18, BD20, BD22, BD24, BD26, BD48, BD50, BE3, BE45, BE7, BE9, BF26, BF28, BF30, BF32, BF34, BF36, BF38, BF4, BF40, BF42, BF44, BF52, BG11, BG13, BG15, BG17, BG19, BG21, BG23, BG47, BG7, BH22, BH4, BJ25, BJ27, BJ29, BJ3, BJ31, BJ33, BJ35, BJ37, BJ39, BJ41, BJ43, BJ45, BJ47, BJ49, BJ5, BJ51, BK10, BK12, BK14, BK16, BK18, BK20, BK22, BK46, BK6, BK8, BL1, BL21, BL53, BM10, BM46, BN21, BN3, C1, C11, C15, C19, C21, C23, C29, C31, C33, C41, C43, C49, C53, C9, D16, D18, D24, D26, D28, D34, D36, D38, D40, D6, E19, E21, E47, E9, F12, F2, F24, F32, F36, F4, F44, F50, F52, G15, G21, G23, G27, G33, G39, G49, G5, G9, J1, J13, J15, J17, J19, J21, J23, J25, J29, J3, J31, J35, J37, J41, J47, J49, J5, J51, J53, J7, K12, K14, K16, K18, K20, K22, K24, K26, K28, K30, K32, K34, K36, K38, K40, K42, K46, K8, L11, L13, L15, L17, L19, L21, L23, L25, L27, L29, L31, L33, L35, L37, L39, L41, L43, M10, M2, M4, M44, M46, M48, M50, M52, M6, M8, N13, N41, P12, P42, R1, R11, R15, R17, R19, R21, R23, R25, R27, R29, R3, R31, R33, R35, R37, R39, R43, R45, R47, R49, R5, R51, R53, R7, R9, T12, T16, T20, T24, T28, T32, T36, T42, U17, U21, U33, U37, V10, V12, V18, V2, V22, V30, V34, V4, V42, V44, V46, V48, V50, V52, V6, V8, W19, W23, W27, W31, W35, Y12, Y20, Y24, Y28, Y32, Y36, Y42
VSS_SCU_XTAL	BK48, BM48, BM50, BN51

1 HDMI-RX is not fully supported. See restrictions in Section 4.10.8.

2 MLB is not supported on this product. The MLB power rail must be tied to the voltage specified in Table 8 or may be terminated, per the Hardware Developer's Guide power supplies of unused functions.

3 MLB is not supported on this product. This MLB power rail must be tied to the voltage specified in Table 8 if other I/O functions are used, as determined by IOMUX selection. Alternately, terminate the MLB supply, per the Hardware Developer's Guide power supplies of unused functions.

The following table shows functional contact assignments for the 29 × 29 mm package.

Table 127. 29 × 29 mm functional contact assignments

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
AP10	ADC_IN0	VDD_ADC_1P8	GPIO	ALT0	ADC_IN0	PD
AN11	ADC_IN1				ADC_IN1	
AP8	ADC_IN2				ADC_IN2	
AR9	ADC_IN3				ADC_IN3	
AN9	ADC_IN4				ADC_IN4	
AR7	ADC_IN5				ADC_IN5	
AL9	ADC_IN6				ADC_IN6	
AP6	ADC_IN7				ADC_IN7	
BH52	ANA_TEST_OUT0_N	VDD_SCU_ANA_1P8	ANA	NXP Internal Use Only (Leave Unconnected)		
BG53	ANA_TEST_OUT0_P					
BD2	ANA_TEST_OUT1_N	VDD_SCU_ANA_1P8				
BE1	ANA_TEST_OUT1_P					
H28	EMMC0_CLK	VDD_EMMC0_1P8_3P3	FASTD	ALT1	NAND_READY_B	PU
J27	EMMC0_CMD			ALT0	EMMC0_CMD	PD
G29	EMMC0_DATA0				EMMC0_DATA0	
H30	EMMC0_DATA1				EMMC0_DATA1	
G31	EMMC0_DATA2				EMMC0_DATA2	
H32	EMMC0_DATA3				EMMC0_DATA3	
J33	EMMC0_DATA4				EMMC0_DATA4	
H34	EMMC0_DATA5				EMMC0_DATA5	
H36	EMMC0_DATA6				EMMC0_DATA6	
G35	EMMC0_DATA7				EMMC0_DATA7	
H38	EMMC0_RESET_B		GPIO	ALT3	LSIO.GPIO5.IO13	PU
G37	EMMC0_STROBE		FASTD	ALT0	EMMC0_STROBE	PD
A9	ENET0_MDC	VDD_ENET_MDIO_1P8_3P3	GPIO	ALT3	LSIO.GPIO4.IO14	PD
D10	ENET0_MDIO			ALT0	ENET0_MDIO	PU
B10	ENET0_REFCLK_125M_25M			ALT3	LSIO.GPIO4.IO15	PD
E43	ENET0_RGMII_RX_CTL	VDD_ENET0_1P8_3P3	FASTD	ALT0	ENET0_RGMII_RX_CTL	PD
B44	ENET0_RGMII_RXC				ENET0_RGMII_RXC	
A47	ENET0_RGMII_RXD0				ENET0_RGMII_RXD0	

Table 127. 29 × 29 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
D44	ENET0_RGMII_RXD1	VDD_ENET0_1P8_3P3	FASTD	ALT0	ENET0_RGMII_RXD1	PD
C45	ENET0_RGMII_RXD2				ENET0_RGMII_RXD2	
E45	ENET0_RGMII_RXD3				ENET0_RGMII_RXD3	
E41	ENET0_RGMII_TX_CTL			ALT3	LSIO.GPIO5.IO31	PD
A41	ENET0_RGMII_TXC				LSIO.GPIO5.IO30	
A43	ENET0_RGMII_TXD0				LSIO.GPIO6.IO00	
B42	ENET0_RGMII_TXD1				LSIO.GPIO6.IO01	
A45	ENET0_RGMII_TXD2				LSIO.GPIO6.IO02	
D42	ENET0_RGMII_TXD3				LSIO.GPIO6.IO03	
A13	ENET1_MDC	VDD_ENET_MDIO_1P8_3P3	GPIO	ALT3	LSIO.GPIO4.IO18	PD
C13	ENET1_MDIO			ALT0	ENET1_MDIO	PU
A11	ENET1_REFCLK_125M_25M			ALT3	LSIO.GPIO4.IO16	PD
E49	ENET1_RGMII_RX_CTL	VDD_ENET1_1P8_2P5_3P3	FASTD	ALT0	ENET1_RGMII_RX_CTL	PD
B50	ENET1_RGMII_RXC				ENET1_RGMII_RXC	
E51	ENET1_RGMII_RXD0				ENET1_RGMII_RXD0	
C51	ENET1_RGMII_RXD1				ENET1_RGMII_RXD1	
D52	ENET1_RGMII_RXD2				ENET1_RGMII_RXD2	
E53	ENET1_RGMII_RXD3				ENET1_RGMII_RXD3	
B48	ENET1_RGMII_TX_CTL			ALT3	LSIO.GPIO6.IO11	PD
D46	ENET1_RGMII_TXC				LSIO.GPIO6.IO10	
A49	ENET1_RGMII_TXD0				LSIO.GPIO6.IO12	
C47	ENET1_RGMII_TXD1				LSIO.GPIO6.IO13	
G47	ENET1_RGMII_TXD2				LSIO.GPIO6.IO14	
D48	ENET1_RGMII_TXD3				LSIO.GPIO6.IO15	
AW9	ESAI0_FSR	VDD_ESAI0_MCLK_1P8_3P3	GPIO	ALT0	ESAI0_FSR	PD
BG9	ESAI0_FST				ESAI0_FST	
BB8	ESAI0_SCKR				ESAI0_SCKR	
AY8	ESAI0_SCKT				ESAI0_SCKT	
BA9	ESAI0_TX0				ESAI0_TX0	
BA7	ESAI0_TX1				ESAI0_TX1	
AU9	ESAI0_TX2_RX3				ESAI0_TX2_RX3	
BC5	ESAI0_TX3_RX2				ESAI0_TX3_RX2	

Table 127. 29 × 29 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
AV8	ESAI0_TX4_RX1	VDD_ESAI0_MCLK_1P8_3P3	GPIO	ALT0	ESAI0_TX4_RX1	PD
AU7	ESAI0_TX5_RX0				ESAI0_TX5_RX0	
BE11	ESAI1_FSR	VDD_ESAI1_SPDIF_SPI_1P8_3P3	GPIO	ALT0	ESAI1_FSR	PD
BF12	ESAI1_FST				ESAI1_FST	
BD12	ESAI1_SCKR				ESAI1_SCKR	
AY10	ESAI1_SCKT				ESAI1_SCKT	
BF10	ESAI1_TX0				ESAI1_TX0	
BA11	ESAI1_TX1				ESAI1_TX1	
AU11	ESAI1_TX2_RX3				ESAI1_TX2_RX3	
AV10	ESAI1_TX3_RX2				ESAI1_TX3_RX2	
AY12	ESAI1_TX4_RX1				ESAI1_TX4_RX1	
AT10	ESAI1_TX5_RX0				ESAI1_TX5_RX0	
C5	FLEXCAN0_RX	VDD_FLEXCAN_1P8_3P3	GPIO	ALT0	FLEXCAN0_RX	PD
H6	FLEXCAN0_TX			ALT3	LSIO.GPIO3.IO30	PD
E5	FLEXCAN1_RX			ALT0	FLEXCAN1_RX	PD
G7	FLEXCAN1_TX			ALT3	LSIO.GPIO4.IO00	PD
C3	FLEXCAN2_RX			ALT0	FLEXCAN2_RX	PD
E7	FLEXCAN2_TX			ALT3	LSIO.GPIO4.IO02	PD
AV52	GPT0_CAPTURE	VDD_M4_GPT_UART_1P8_3P3	GPIO	ALT0	GPT0_CAPTURE	PD
AY52	GPT0_CLK				GPT0_CLK	
AW53	GPT0_COMPARE				GPT0_COMPARE	
AY50	GPT1_CAPTURE				GPT1_CAPTURE	
BA53	GPT1_CLK				GPT1_CLK	
BA51	GPT1_COMPARE				GPT1_COMPARE	
BL13	HDMI_RX0_ARC_N[3]	VDD_HDMI_RX0_1P8	HDMI	Not muxed		
BM14	HDMI_RX0_ARC_P[3]					
BJ9	HDMI_RX0_CEC[3]					
BL11	HDMI_RX0_CLK_N[3]					
BM12	HDMI_RX0_CLK_P[3]					
BL15	HDMI_RX0_DATA0_N[3]					
BM16	HDMI_RX0_DATA0_P[3]					
BL17	HDMI_RX0_DATA1_N[3]					
BM18	HDMI_RX0_DATA1_P[3]					

Table 127. 29 × 29 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
BL19	HDMI_RX0_DATA2_N[3]	VDD_HDMI_RX0_1P8	HDMI	Not muxed		
BM20	HDMI_RX0_DATA2_P[3]					
BH10	HDMI_RX0_DDC_SCL[3]					
BE13	HDMI_RX0_DDC_SDA[3]					
BF14	HDMI_RX0_HPD[3]					
BN11	HDMI_RX0_MON_5V[3]					
BJ11	HDMI_RX0_REXT[3]					
BG3	HDMI_TX0_AUX_N	VDD_HDMI_TX0_1P8	HDMI	Not muxed		
BH2	HDMI_TX0_AUX_P					
BJ1	HDMI_TX0_CEC					
BK2	HDMI_TX0_CLK_EDP3_N					
BL3	HDMI_TX0_CLK_EDP3_P					
BM4	HDMI_TX0_DATA0_EDP2_N					
BL5	HDMI_TX0_DATA0_EDP2_P					
BM6	HDMI_TX0_DATA1_EDP1_N					
BL7	HDMI_TX0_DATA1_EDP1_P					
BM8	HDMI_TX0_DATA2_EDP0_N					
BL9	HDMI_TX0_DATA2_EDP0_P					
BG1	HDMI_TX0_DDC_SCL					
BN5	HDMI_TX0_DDC_SDA					
BH8	HDMI_TX0_HPD					
BJ7	HDMI_TX0_REXT					
BN9	HDMI_TX0_TS_SCL	VDD_HDMI_TX0_DIG_3P3	GPIO	ALT0	HDMI_TX0_TS_SCL	PU
BN7	HDMI_TX0_TS_SDA				HDMI_TX0_TS_SDA	
BC51	JTAG_TCK	VDD_SCU_1P8	TEST	Not muxed		PD
BE51	JTAG_TDI					PU
BD52	JTAG_TDO					Drive-0
BA49	JTAG_TMS					PU
BE53	JTAG_TRST_B					

Table 127. 29 × 29 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
BL41	LVDS0_CH0_CLK_N	VDD_LVDS0_1P8	LVDS	Not muxed		
BN41	LVDS0_CH0_CLK_P					
BK42	LVDS0_CH0_TX0_N					
BM42	LVDS0_CH0_TX0_P					
BL43	LVDS0_CH0_TX1_N	VDD_LVDS0_1P8	LVDS	Not muxed		
BN43	LVDS0_CH0_TX1_P					
BK44	LVDS0_CH0_TX2_N					
BM44	LVDS0_CH0_TX2_P					
BL45	LVDS0_CH0_TX3_N					
BN45	LVDS0_CH0_TX3_P					
BG45	LVDS0_CH1_CLK_N					
BH46	LVDS0_CH1_CLK_P					
BG43	LVDS0_CH1_TX0_N					
BH44	LVDS0_CH1_TX0_P					
BG41	LVDS0_CH1_TX1_N					
BH42	LVDS0_CH1_TX1_P					
BG39	LVDS0_CH1_TX2_N					
BH40	LVDS0_CH1_TX2_P					
BG37	LVDS0_CH1_TX3_N					
BH38	LVDS0_CH1_TX3_P					
BE39	LVDS0_GPIO00	VDD_LVDS_DIG_1P8_3P3	GPIO	ALT0	LVDS0_GPIO00	PD
BD40	LVDS0_GPIO01				LVDS0_GPIO01	
BD38	LVDS0_I2C0_SCL				LVDS0_I2C0_SCL	PU
BD36	LVDS0_I2C0_SDA				LVDS0_I2C0_SDA	
BE37	LVDS0_I2C1_SCL				LVDS0_I2C1_SCL	
BE35	LVDS0_I2C1_SDA				LVDS0_I2C1_SDA	

Table 127. 29 × 29 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
BK36	LVDS1_CH0_CLK_N	VDD_LVDS1_1P8	LVDS	Not muxed		
BM36	LVDS1_CH0_CLK_P					
BL37	LVDS1_CH0_TX0_N					
BN37	LVDS1_CH0_TX0_P					
BK38	LVDS1_CH0_TX1_N					
BM38	LVDS1_CH0_TX1_P					
BL39	LVDS1_CH0_TX2_N					
BN39	LVDS1_CH0_TX2_P					
BK40	LVDS1_CH0_TX3_N					
BM40	LVDS1_CH0_TX3_P					
BK34	LVDS1_CH1_CLK_N					
BM34	LVDS1_CH1_CLK_P	VDD_LVDS1_1P8	LVDS	Not muxed		
BL33	LVDS1_CH1_TX0_N					
BN33	LVDS1_CH1_TX0_P					
BK32	LVDS1_CH1_TX1_N					
BM32	LVDS1_CH1_TX1_P					
BL31	LVDS1_CH1_TX2_N					
BN31	LVDS1_CH1_TX2_P					
BK30	LVDS1_CH1_TX3_N					
BM30	LVDS1_CH1_TX3_P					
BD34	LVDS1_GPIO00	VDD_LVDS_DIG_1P8_3P3	GPIO	ALT0	LVDS1_GPIO00	PD
BH36	LVDS1_GPIO01				LVDS1_GPIO01	
BL35	LVDS1_I2C0_SCL				LVDS1_I2C0_SCL	PU
BE33	LVDS1_I2C0_SDA				LVDS1_I2C0_SDA	
BD32	LVDS1_I2C1_SCL				LVDS1_I2C1_SCL	
BN35	LVDS1_I2C1_SDA				LVDS1_I2C1_SDA	

Table 127. 29 × 29 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
AR47	M40_GPIO0_00	VDD_M4_GPT_UART_1P8_3P3	GPIO	ALT0	M40_GPIO0_00	PD
AU53	M40_GPIO0_01				M40_GPIO0_01	
AM44	M40_I2C0_SCL				M40_I2C0_SCL	PU
AU51	M40_I2C0_SDA				M40_I2C0_SDA	
AP44	M41_GPIO0_00				M41_GPIO0_00	PD
AU47	M41_GPIO0_01				M41_GPIO0_01	
AR45	M41_I2C0_SCL				M41_I2C0_SCL	PU
AU49	M41_I2C0_SDA				M41_I2C0_SDA	
BC3	MCLK_IN0	VDD_ESAI0_MCLK_1P8_3P3	GPIO	ALT0	MCLK_IN0	PD
BD4	MCLK_OUT0			ALT3	LSIO.GPIO3.IO01	PD
BE21	MIPI_CSI0_CLK_N	VDD_MIPI_CSI0_1P8	CSI	Not muxed		
BF20	MIPI_CSI0_CLK_P					
BE23	MIPI_CSI0_DATA0_N					
BF22	MIPI_CSI0_DATA0_P					
BE19	MIPI_CSI0_DATA1_N					
BF18	MIPI_CSI0_DATA1_P					
BE25	MIPI_CSI0_DATA2_N					
BF24	MIPI_CSI0_DATA2_P					
BE17	MIPI_CSI0_DATA3_N	VDD_MIPI_CSI0_1P8	CSI	Not muxed		
BF16	MIPI_CSI0_DATA3_P					
BL23	MIPI_CSI0_GPIO0_00	VDD_MIPI_CSI_DIG	GPIO	ALT0	MIPI_CSI0_GPIO0_00	PD
BM22	MIPI_CSI0_GPIO0_01				MIPI_CSI0_GPIO0_01	
BH24	MIPI_CSI0_I2C0_SCL				MIPI_CSI0_I2C0_SCL	PU
BN19	MIPI_CSI0_I2C0_SDA				MIPI_CSI0_I2C0_SDA	
BJ23	MIPI_CSI0_MCLK_OUT			ALT3	LSIO.GPIO1.IO29	PD

Table 127. 29 × 29 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
BH16	MIPI_CSI1_CLK_N	VDD_MIPI_CSI1_1P8	CSI	Not muxed		
BJ17	MIPI_CSI1_CLK_P					
BH18	MIPI_CSI1_DATA0_N					
BJ19	MIPI_CSI1_DATA0_P					
BH14	MIPI_CSI1_DATA1_N					
BJ15	MIPI_CSI1_DATA1_P					
BH20	MIPI_CSI1_DATA2_N					
BJ21	MIPI_CSI1_DATA2_P					
BH12	MIPI_CSI1_DATA3_N					
BJ13	MIPI_CSI1_DATA3_P					
BN15	MIPI_CSI1_GPIO0_00	VDD_MIPI_CSI_DIG	GPIO	ALT0	MIPI_CSI1_GPIO0_00	PD
BN13	MIPI_CSI1_GPIO0_01				MIPI_CSI1_GPIO0_01	
BN17	MIPI_CSI1_I2C0_SCL				MIPI_CSI1_I2C0_SCL	PU
BE15	MIPI_CSI1_I2C0_SDA				MIPI_CSI1_I2C0_SDA	
BN23	MIPI_CSI1_MCLK_OUT			ALT3	LSIO.GPIO1.IO29	PD
BN27	MIPI_DSI0_CLK_N	VDD_MIPI_DSI0_1P8	DSI	Not muxed		
BL27	MIPI_DSI0_CLK_P					
BM28	MIPI_DSI0_DATA0_N					
BK28	MIPI_DSI0_DATA0_P					
BM26	MIPI_DSI0_DATA1_N					
BK26	MIPI_DSI0_DATA1_P					
BN29	MIPI_DSI0_DATA2_N					
BL29	MIPI_DSI0_DATA2_P					
BN25	MIPI_DSI0_DATA3_N					
BL25	MIPI_DSI0_DATA3_P					
BD30	MIPI_DSI0_GPIO0_00	VDD_MIPI_DSI_DIG_1P8_3P3	GPIO	ALT0	MIPI_DSI0_GPIO0_00	PD
BD28	MIPI_DSI0_GPIO0_01	VDD_MIPI_DSI_DIG_1P8_3P3	GPIO	ALT0	MIPI_DSI0_GPIO0_01	PD
BE29	MIPI_DSI0_I2C0_SCL				MIPI_DSI0_I2C0_SCL	PU
BE31	MIPI_DSI0_I2C0_SDA				MIPI_DSI0_I2C0_SDA	

Table 127. 29 × 29 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
BH30	MIPI_DSI1_CLK_N	VDD_MIPI_DSI1_1P8	DSI	Not muxed		
BG31	MIPI_DSI1_CLK_P					
BH32	MIPI_DSI1_DATA0_N					
BG33	MIPI_DSI1_DATA0_P					
BH28	MIPI_DSI1_DATA1_N					
BG29	MIPI_DSI1_DATA1_P					
BH34	MIPI_DSI1_DATA2_N					
BG35	MIPI_DSI1_DATA2_P					
BH26	MIPI_DSI1_DATA3_N					
BG27	MIPI_DSI1_DATA3_P					
BM24	MIPI_DSI1_GPIO0_00	VDD_MIPI_DSI_DIG_1P8_3P3	GPIO	ALT0	MIPI_DSI1_GPIO0_00	PD
BK24	MIPI_DSI1_GPIO0_01				MIPI_DSI1_GPIO0_01	
BE27	MIPI_DSI1_I2C0_SCL				MIPI_DSI1_I2C0_SCL	PU
BG25	MIPI_DSI1_I2C0_SDA				MIPI_DSI1_I2C0_SDA	
D2	MLB_CLK[4]	VDD_MLB_DIG_1P8_3P3	GPIO	ALT0	MLB_CLK	PD
E3	MLB_DATA[4]				MLB_DATA	
E1	MLB_SIG[4]				MLB_SIG	
E33	MLB_CLK_N[5]	VDD_MLB_1P8	MLB	Not muxed		PD
D32	MLB_CLK_P[5]					
E35	MLB_DATA_N[5]					
F34	MLB_DATA_P[5]					
E31	MLB_SIG_N[5]					
D30	MLB_SIG_P[5]					
BE47	ON_OFF_BUTTON	VDD_SNVS_LDO_1P8_CAP	ANA	Not muxed		PU
A17	PCIE_CTRL0_CLKREQ_B	VDD_PCIE_DIG_1P8_3P3	GPIO	ALT0	PCIE_CTRL0_CLKREQ_B	PD
D20	PCIE_CTRL0_PERST_B				PCIE_CTRL0_PERST_B	
A15	PCIE_CTRL0_WAKE_B				PCIE_CTRL0_WAKE_B	PU
A25	PCIE_CTRL1_CLKREQ_B				PCIE_CTRL1_CLKREQ_B	PD
G25	PCIE_CTRL1_PERST_B				PCIE_CTRL1_PERST_B	
A27	PCIE_CTRL1_WAKE_B				PCIE_CTRL1_WAKE_B	PU

Table 127. 29 × 29 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
E23	PCIE_REF_QR	VDD_PCIE_LDO_1P8	PCIE	Not muxed		
D22	PCIE_REXT					
M20	PCIE_SATA0_PHY_PLL_REF_RETURN[3]					
M28	PCIE0_PHY_PLL_REF_RETURN					
N23	PCIE1_PHY_PLL_REF_RETURN					
E25	PCIE_SATA_REFCLK100M_N[3]	VDD_PCIE_LDO_1P0_CAP	PCIE	HCSL compatiable clock Not muxed		
F26	PCIE_SATA_REFCLK100M_P[3]					
B20	PCIE_SATA0_RX0_N[3]			Not muxed		
A19	PCIE_SATA0_RX0_P[3]					
C17	PCIE_SATA0_TX0_N[3]					
B16	PCIE_SATA0_TX0_P[3]					
B30	PCIE0_RX0_N					
A29	PCIE0_RX0_P					
C27	PCIE0_TX0_N					
B26	PCIE0_TX0_P					
B22	PCIE1_RX0_N					
A21	PCIE1_RX0_P					
C25	PCIE1_TX0_N					
B24	PCIE1_TX0_P					
BF50	PMIC_EARLY_WARNING	VDD_SCU_1P8	SCU	ALT0	PMIC_EARLY_WARNING	PD
AY46	PMIC_I2C_SCL				PMIC_I2C_SCL	PU
BG51	PMIC_I2C_SDA				PMIC_I2C_SDA	
BH50	PMIC_INT_B				PMIC_INT_B	
BL51	PMIC_ON_REQ	VDD_SNVS_LDO_1P8_CAP	ANA	Not muxed		Drive-1
BE49	POR_B	VDD_SCU_1P8	SCU			PU

Table 127. 29 × 29 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
G13	QSPI0A_DATA0	VDD_QSPI0_1P8_3P3	FASTD	ALT0	QSPI0A_DATA0	PD
F14	QSPI0A_DATA1				QSPI0A_DATA1	
H14	QSPI0A_DATA2				QSPI0A_DATA2	
H16	QSPI0A_DATA3				QSPI0A_DATA3	
G17	QSPI0A_DQS				QSPI0A_DQS	
E17	QSPI0A_SCLK				QSPI0A_SCLK	
E15	QSPI0A_SS0_B				QSPI0A_SS0_B	
F16	QSPI0A_SS1_B				QSPI0A_SS1_B	
H18	QSPI0B_DATA0	VDD_QSPI0_1P8_3P3	FASTD	ALT0	QSPI0B_DATA0	PD
H20	QSPI0B_DATA1				QSPI0B_DATA1	
G19	QSPI0B_DATA2				QSPI0B_DATA2	
F20	QSPI0B_DATA3				QSPI0B_DATA3	
H22	QSPI0B_DQS				QSPI0B_DQS	
F18	QSPI0B_SCLK				QSPI0B_SCLK	
F22	QSPI0B_SS0_B				QSPI0B_SS0_B	PU
H24	QSPI0B_SS1_B				QSPI0B_SS1_B	
D12	QSPI1A_DATA0	VDD_QSPI1A_1P8_3P3	FASTD	ALT0	QSPI1A_DATA0	PD
D14	QSPI1A_DATA1				QSPI1A_DATA1	
E13	QSPI1A_DATA2				QSPI1A_DATA2	
E11	QSPI1A_DATA3				QSPI1A_DATA3	
H12	QSPI1A_DQS				QSPI1A_DQS	
F10	QSPI1A_SCLK				QSPI1A_SCLK	
J11	QSPI1A_SS0_B				QSPI1A_SS0_B	PU
G11	QSPI1A_SS1_B				QSPI1A_SS1_B	
BN47	RTC_XTALI	VDD_SNVS_LDO_1P8_CAP	ANA	Not muxed		
BL47	RTC_XTALO					
AV6	SAI1_RXC	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	SAI1_RXC	PD
AV4	SAI1_RXD				SAI1_RXD	
AU3	SAI1_RXFS				SAI1_RXFS	
AU5	SAI1_TXC				SAI1_TXC	
AU1	SAI1_TXD				SAI1_TXD	
AV2	SAI1_TXFS				SAI1_TXFS	

Table 127. 29 × 29 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
BB44	SCU_BOOT_MODE0	VDD_SCU_1P8	SCU	Not muxed		PD
BC45	SCU_BOOT_MODE1					
BJ53	SCU_BOOT_MODE2					
BA43	SCU_BOOT_MODE3					
AY42	SCU_BOOT_MODE4			ALT0	SCU_BOOT_MODE4	
BK52	SCU_BOOT_MODE5				SCU_BOOT_MODE5	
AU43	SCU_GPIO0_00	VDD_SCU_1P8	GPIO	ALT0	SCU_GPIO0_00	PD
AV44	SCU_GPIO0_01				SCU_GPIO0_01	PU
AW45	SCU_GPIO0_02				SCU_GPIO0_02	PD
BB46	SCU_GPIO0_03	VDD_SCU_1P8	GPIO	ALT0	SCU_GPIO0_03	PD
BC47	SCU_GPIO0_04				SCU_GPIO0_04	
AY44	SCU_GPIO0_05				SCU_GPIO0_05	
BG49	SCU_GPIO0_06				SCU_GPIO0_06	
BF48	SCU_GPIO0_07				SCU_GPIO0_07	
BC53	SCU_PMIC_MEMC_ON	VDD_SCU_1P8	SCU	Not muxed		PD
BA47	SCU_PMIC_STANDBY					Drive-0
BB50	SCU_WDOG_OUT					
AL45	SIM0_CLK	**VDD_SIM0_1P8_3P3**	GPIO	ALT3	LSIO.GPIO0.IO00	PD
AP46	SIM0_GPIO0_00				LSIO.GPIO0.IO05	
AN45	SIM0_IO				LSIO.GPIO0.IO02	
AL43	SIM0_PD				SIM0_PD	PD
AT48	SIM0_POWER_EN				LSIO.GPIO0.IO04	PD
AP48	SIM0_RST				SIM0_RST	
BE41	SNVS_TAMPER_IN0	VDD_SNVS_LDO_1P8_CAP	ANA	Not muxed		Hi-Z
BE43	SNVS_TAMPER_IN1					
BD46	SNVS_TAMPER_OUT0					
BD42	SNVS_TAMPER_OUT1					
BD6	SPDIF0_EXT_CLK	VDD_ESAI1_SPDIF_SPI_1P8_3P3	GPIO	ALT0	SPDIF0_EXT_CLK	PD
BC7	SPDIF0_RX				SPDIF0_RX	
BC9	SPDIF0_TX			ALT3	LSIO.GPIO2.IO15	PD

Table 127. 29 × 29 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
BC1	SPI0_CS0	VDD_SPI_SAI_1P8_3P3	GPIO	ALT0	SPI0_CS0	PD
BA3	SPI0_CS1				SPI0_CS1	
BB4	SPI0_SCK				SPI0_SCK	
BA5	SPI0_SDI				SPI0_SDI	
AY6	SPI0_SDO			ALT3	LSIO.GPIO3.IO03	PD
AW1	SPI2_CS0			ALT0	SPI2_CS0	PD
AY2	SPI2_CS1				SPI2_CS1	
AW5	SPI2_SCK				SPI2_SCK	
AY4	SPI2_SDI				SPI2_SDI	
BA1	SPI2_SDO			ALT3	LSIO.GPIO3.IO08	PD
BG5	SPI3_CS0	VDD_ESAI1_SPDIF_SPI_1P8_3P3	GPIO	ALT0	SPI3_CS0	PD
BD8	SPI3_CS1				SPI3_CS1	
BF6	SPI3_SCK	VDD_ESAI1_SPDIF_SPI_1P8_3P3	GPIO	ALT0	SPI3_SCK	PD
BE5	SPI3_SDI				SPI3_SDI	
BF2	SPI3_SDO			ALT3	LSIO.GPIO2.IO18	PD
BC49	TEST_MODE_SELECT	VDD_SCU_1P8	SCU	Not muxed		PD
AW49	UART0_CTS_B	VDD_M4_GPT_UART_1P8_3P3	GPIO	ALT0	UART0_CTS_B	PD
AU45	UART0_RTS_B			ALT3	LSIO.GPIO0.IO22	PD
AV50	UART0_RX			ALT0	UART0_RX	PD
AV48	UART0_TX			ALT3	LSIO.GPIO0.IO21	PD
AV46	UART1_CTS_B			ALT0	UART1_CTS_B	PD
AR43	UART1_RTS_B			ALT3	LSIO.GPIO0.IO26	PD
AT44	UART1_RX			ALT0	UART1_RX	PD
AY48	UART1_TX			ALT3	LSIO.GPIO0.IO24	PD
H26	USB_HSIC0_DATA	VDD_USB_HSIC0_1P2	FASTD	ALT0	USB_HSIC0_DATA	Hi-Z
F28	USB_HSIC0_STROBE				USB_HSIC0_STROBE	
C39	USB_OTG1_DN	VDD_USB_OTG1_3P3	OTG	Not muxed		
B40	USB_OTG1_DP					
A37	USB_OTG1_ID					
A39	USB_OTG1_VBUS					

Table 127. 29 × 29 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
C37	USB_OTG2_DN	VDD_USB_OTG2_3P3	OTG	Not muxed		
B38	USB_OTG2_DP					
F30	USB_OTG2_ID					
E29	USB_OTG2_REXT					
A35	USB_OTG2_VBUS					
E27	USB_SS3_REXT	VDD_USB_SS3_LDO_1P0_CAP	USB3	Not muxed		
B34	USB_SS3_RX_N					
C35	USB_SS3_RX_P					
B32	USB_SS3_TX_N					
A33	USB_SS3_TX_P					
J9	USB_SS3_TC0	VDD_USB_SS3_TC_3P3	GPIO	ALT0	USB_SS3_TC0	PU
L9	USB_SS3_TC1				USB_SS3_TC1	
F8	USB_SS3_TC2				USB_SS3_TC2	
H10	USB_SS3_TC3				USB_SS3_TC3	
J39	USDHC1_CLK	VDD_USDHC1_1P8_3P3	FASTD	ALT0	USDHC1_CLK	Drive-0
G41	USDHC1_CMD	VDD_USDHC1_1P8_3P3	FASTD	ALT0	USDHC1_CMD	PD
E37	USDHC1_DATA0				USDHC1_DATA0	PU
F38	USDHC1_DATA1				USDHC1_DATA1	
E39	USDHC1_DATA2				USDHC1_DATA2	
F40	USDHC1_DATA3				USDHC1_DATA3	
H40	USDHC1_DATA4				USDHC1_DATA4	
G43	USDHC1_DATA5				USDHC1_DATA5	
F42	USDHC1_DATA6				USDHC1_DATA6	
H42	USDHC1_DATA7				USDHC1_DATA7	
J43	USDHC1_STROBE				USDHC1_STROBE	
A5	USDHC1_RESET_B	VDD_USDHC_VSELECT_1P8_3P3	GPIO	ALT3	LSIO.GPIO4.IO07	PU
B4	USDHC1_VSELECT				LSIO.GPIO4.IO07	
B8	USDHC2_CD_B			ALT0	USDHC2_CD_B	PU

Table 127. 29 × 29 mm functional contact assignments (continued)

Ball	Ball Name	Power Domain	Ball Type[1]	Reset Condition		
				Default mode	Default function	State[2]
F46	USDHC2_CLK	VDD_USDHC2_1P8_3P3	FASTD	ALT3	LSIO.GPIO5.IO24	PD
H44	USDHC2_CMD			ALT0	USDHC2_CMD	PD
H48	USDHC2_DATA0				USDHC2_DATA0	PU
G45	USDHC2_DATA1				USDHC2_DATA1	
L45	USDHC2_DATA2				USDHC2_DATA2	
J45	USDHC2_DATA3				USDHC2_DATA3	
C7	USDHC2_RESET_B	VDD_USDHC_VSELECT_1P8_3P3	GPIO	ALT3	LSIO.GPIO4.IO09	PU
A7	USDHC2_VSELECT				LSIO.GPIO4.IO10	
D8	USDHC2_WP			ALT0	USDHC2_WP	PD
BN49	XTALI	VDD_SCU_XTAL_1P8	ANA	Not muxed		
BL49	XTALO					

1 FASTD are GPIO balls configured for high speed operation using the FASTFRZ control.

2 Reset condition shown is before boot code execution. For pad changes after boot code execution, see the “System Boot” chapter of the device reference manual,

3 HDMI-RX is not fully supported. See restrictions in Section 4.10.8.

4 MLB is not supported on this device. Users may choose alternate functions as determined by the IOMUX.

5 MLB is not supported on this device. Terminate these outputs per the Hardware Developer’s Guide for unused I/O signals.

The following table shows the DRAM pin function for the 29 x 29 mm package.

Table 128. 29 x 29 mm DRAM pin function

Ball Name	x = 0	x = 1	LPDDR4 Function	Notes
DDR_CHx_ATO	AF46	AF8	—	NXP Internal Use Only (Leave Unconnected)
DDR_CHx_CK0_N	Y50	Y4	CK_c_A	The exact clock and control line connections will be dependent on the memory configuration in use. Refer to the Hardware Developers Guide (HDG) for further details.
DDR_CHx_CK0_P	W49	W5	CK_t_A	
DDR_CHx_CK1_N	AB50	AB4	CK_c_B	
DDR_CHx_CK1_P	AC49	AC5	CK_t_B	
DDR_CHx_DCF00	U47	U7	CA2_A	
DDR_CHx_DCF01	W47	W7	CA4_A	
DDR_CHx_DCF02	Y48	Y6	—	
DDR_CHx_DCF03	Y46	Y8	CA5_A	
DDR_CHx_DCF04	W43	W11	—	
DDR_CHx_DCF05	Y44	Y10	—	
DDR_CHx_DCF06	W45	W9	—	
DDR_CHx_DCF07	W51	W3	—	
DDR_CHx_DCF08	T48	T6	CA3_A	
DDR_CHx_DCF09	T52	T2	—	
DDR_CHx_DCF10	T50	T4	CS0_A	
DDR_CHx_DCF11	U51	U3	CA0_A	
DDR_CHx_DCF12	U49	U5	CS1_A	
DDR_CHx_DCF13	T46	T8	—	
DDR_CHx_DCF14	W53	W1	CKE0_A	
DDR_CHx_DCF15	Y52	Y2	CKE1_A	
DDR_CHx_DCF16	U53	U1	CA1_A	
DDR_CHx_DCF17	AC47	AC7	CA4_B	
DDR_CHx_DCF18	AB48	AB6	RESET_N	
DDR_CHx_DCF19	AB46	AB8	CA5_B	
DDR_CHx_DCF20	AC43	AC11	—	
DDR_CHx_DCF21	AE45	AE9	—	
DDR_CHx_DCF22	AC51	AC3	—	
DDR_CHx_DCF23	AC45	AC9	—	
DDR_CHx_DCF24	AB44	AB10	—	

Table 128. 29 x 29 mm DRAM pin function (continued)

Ball Name	x = 0	x = 1	LPDDR4 Function	Notes
DDR_CHx_DCF25	AF52	AF2	—	The exact clock and control line connections will be dependent on the memory configuration in use. Refer to the Hardware Developers Guide (HDG) for further details.
DDR_CHx_DCF26	AE47	AE7	CA3_B	
DDR_CHx_DCF27	AE51	AE3	CA0_B	
DDR_CHx_DCF28	AF50	AF4	CS0_B	
DDR_CHx_DCF29	AE49	AE5	CS1_B	
DDR_CHx_DCF30	AC53	AC1	CKE0_B	
DDR_CHx_DCF31	AB52	AB2	CKE1_B	
DDR_CHx_DCF32	AE53	AE1	CA1_B	
DDR_CHx_DCF33	AF48	AF6	CA2_B	
DDR_CHx_DM0	H52	H2	DMI[3..0]	The exact mask, strobe and data connections to memory are flexible as long as the correct byte mapping is used, there is no restriction on the bit connections within each byte. DM0 -> DQS0(_N/P) -> DQ[7..0] DM1 -> DQS1(_N/P) -> DQ[15..8] DM2 -> DQS2(_N/P) -> DQ[23..16] DM3 -> DQS3(_N/P) -> DQ[31..24]
DDR_CHx_DM1	N47	N7		
DDR_CHx_DM2	AJ47	AJ7		
DDR_CHx_DM3	AP52	AP2		
DDR_CHx_DQ00	P44	P10	DQ[31..0]	
DDR_CHx_DQ01	N45	N9		
DDR_CHx_DQ02	L47	L7		
DDR_CHx_DQ03	K48	K6		
DDR_CHx_DQ04	H50	H4		
DDR_CHx_DQ05	G53	G1		
DDR_CHx_DQ06	G51	G3		
DDR_CHx_DQ07	N43	N11		
DDR_CHx_DQ08	L49	L5		
DDR_CHx_DQ09	K50	K4		
DDR_CHx_DQ10	N51	N3		
DDR_CHx_DQ11	L51	L3		
DDR_CHx_DQ12	P46	P8		
DDR_CHx_DQ13	N49	N5		
DDR_CHx_DQ14	P50	P4		
DDR_CHx_DQ15	P48	P6		
DDR_CHx_DQ16	AM50	AM4		
DDR_CHx_DQ17	AL49	AL5		
DDR_CHx_DQ18	AL51	AL3		
DDR_CHx_DQ19	AJ51	AJ3		

Table 128. 29 x 29 mm DRAM pin function (continued)

Ball Name	x = 0	x = 1	LPDDR4 Function	Notes
DDR_CHx_DQ20	AJ49	AJ5	DQ[31..0]	The exact mask, strobe and data connections to memory are flexible as long as the correct byte mapping is used, there is no restriction on the bit connections within each byte. DM0 -> DQS0(_N/P) -> DQ[7..0] DM1 -> DQS1(_N/P) -> DQ[15..8] DM2 -> DQS2(_N/P) -> DQ[23..16] DM3 -> DQS3(_N/P) -> DQ[31..24]
DDR_CHx_DQ21	AH46	AH8		
DDR_CHx_DQ22	AH48	AH6		
DDR_CHx_DQ23	AH50	AH4		
DDR_CHx_DQ24	AJ45	AJ9		
DDR_CHx_DQ25	AH44	AH10		
DDR_CHx_DQ26	AM48	AM6		
DDR_CHx_DQ27	AL47	AL7		
DDR_CHx_DQ28	AR53	AR1		
DDR_CHx_DQ29	AP50	AP4		
DDR_CHx_DQ30	AJ43	AJ11		
DDR_CHx_DQ31	AR51	AR3		
DDR_CHx_DQS0_N	L53	L1	DQS[3..0]_c maps to _N DQS[3..0]_t maps to _P	
DDR_CHx_DQS0_P	K52	K2		
DDR_CHx_DQS1_N	P52	P2		
DDR_CHx_DQS1_P	N53	N1		
DDR_CHx_DQS2_N	AH52	AH2		
DDR_CHx_DQS2_P	AJ53	AJ1		
DDR_CHx_DQS3_N	AL53	AL1		
DDR_CHx_DQS3_P	AM52	AM2		
DDR_CHx_DTO0	U45	U9	—	NXP Internal Use Only (Leave Unconnected)
DDR_CHx_DTO1	T44	T10	—	
DDR_CHx_VREF	U43	U11	—	—
DDR_CHx_ZQ	AF44	AF10	—	—

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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