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Freescale Semiconductor
Technical Data

MPC866EC
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# MPC866/MPC859 Hardware Specifications

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MPC866/859 family (refer to Table 1 for a list of devices). The MPC866P is the superset device of the MPC866/859 family.This document describes pertinent electrical and physical characteristics of the MPC8245. For functional characteristics of the processor, refer to the *MPC866 PowerQUICC Family Users Manual* (MPC866UM/D).

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## 1 Overview

The MPC866/859 is a derivative of Freescale's MPC860 PowerQUICC™ family of devices. It is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications and communications and networking systems. The MPC866/859/859DSL provides enhanced ATM functionality over that of other ATM-enabled members of the MPC860 family.

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Table 1 shows the functionality supported by the members of the MPC866/859 family.

# 2 Features

**Table 1. MPC866 Family Functionality**

| Part | Cache | | Ethernet | | SCC | SMC |
|---|---|---|---|---|---|---|
| | Instruction | Data | 10T | 10/100 | | |
| MPC866P | 16 Kbytes | 8 Kbytes | Up to 4 | 1 | 4 | 2 |
| MPC866T | 4 Kbytes | 4 Kbytes | Up to 4 | 1 | 4 | 2 |
| MPC859P | 16 Kbytes | 8 Kbytes | 1 | 1 | 1 | 2 |
| MPC859T | 4 Kbytes | 4 Kbytes | 1 | 1 | 1 | 2 |
| MPC859DSL | 4 Kbytes | 4 Kbytes | 1 | 1 | 1 [1] | 1 [2] |
| MPC852T [3] | 4 KBytes | 4 Kbytes | 2 | 1 | 2 | 1 |

1 On the MPC859DSL, the SCC (SCC1) is for ethernet only. Also, the MPC859DSL does not support the Time Slot Assigner (TSA).

2 On the MPC859DSL, the SMC (SMC1) is for UART only.

3 For more details on the MPC852T, please refer to the *MPC852T Hardware Specifications.*

The following list summarizes the key MPC866/859 features:

- Embedded single-issue, 32-bit PowerPC™ core (implementing the PowerPC architecture) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch, without conditional execution
  - 4- or 8-Kbyte data cache and 4- or 16-Kbyte instruction cache (see Table 1)
    - 16-Kbyte instruction cache (MPC866P and MPC859P) is four-way, set-associative with 256 sets; 4-Kbyte instruction cache (MPC866T, MPC859T, and MPC859DSL) is two-way, set-associative with 128 sets.
    - 8-Kbyte data cache (MPC866P and MPC859P) is two-way, set-associative with 256 sets; 4-Kbyte data cache(MPC866T, MPC859T, and MPC859DSL) is two-way, set-associative with 128 sets.
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully associative instruction and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups.
  - Advanced on-chip-emulation debug mode
- The MPC866/859 provides enhanced ATM functionality over that of the MPC860SAR. The MPC866/859 adds major new features available in 'enhanced SAR' (ESAR) mode, including the following:
  - Improved operation, administration, and maintenance (OAM) support
  - OAM performance monitoring (PM) support
  - Multiple APC priority levels available to support a range of traffic pace requirements

  - ATM port-to-port switching capability without the need for RAM-based microcode
  - Simultaneous MII (10/100Base-T) and UTOPIA (half-duplex) capability
  - Optional statistical cell counters per PHY
  - UTOPIA level 2 compliant interface with added FIFO buffering to reduce the total cell transmission time. (The earlier UTOPIA level 1 specification is also supported.)
    - Multi-PHY support on the MPC866, MPC859P, and MPC859T
    - Four PHY support on the MPC866/859
  - Parameter RAM for both SPI and $I^2C$ can be relocated without RAM-based microcode
  - Supports full-duplex UTOPIA both master (ATM side) and slave (PHY side) operation using a 'split' bus
  - AAL2/VBR functionality is ROM-resident.
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- Thirty-two address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to page mode/EDO/SDRAM, SRAM, EPROMs, flash EPROMs, and other memory devices.
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbytes–256 Mbytes)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers cascadable to be two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Fast Ethernet controller (FEC)
  - Simultaneous MII (10/100Base-T) and UTOPIA operation when using the UTOPIA multiplexed bus
- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Low-power stop mode
  - Clock synthesizer
  - Decrementer and time base from the PowerPC architecture
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)

- Interrupts
  - Seven external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - The MPC866P and MPC866T have 23 internal interrupt sources; the MPC859P, MPC859T, and MPC859DSL have 20 internal interrupt sources.
  - Programmable priority between SCCs (MPC866P and MPC866T)
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - Up to 8-Kbytes of dual-port RAM
  - MPC866P and MPC866T have 16 serial DMA (SDMA) channels; MPC859P, MPC859T, and MPC859DSL have 10 serial DMA (SDMA) channels.
  - Three parallel I/O registers with open-drain capability
- Four baud rate generators
  - Independent (can be connected to any SCC or SMC)
  - Allow changes during operation
  - Autobaud support option
- MPC866P and MPC866T have four SCCs (serial communication controller); MPC859P, MPC859T, and MPC859DSL have one SCC; and SCC1 on MPC859DSL supports Ethernet only.
  - Serial ATM capability on all SCCs
  - Optional UTOPIA port on SCC4
  - Ethernet/IEEE 802.3 optional on SCC1–4, supporting full 10-Mbps operation
  - HDLC/SDLC
  - HDLC bus (implements an HDLC-based local area network (LAN))
  - Asynchronous HDLC to support PPP (point-to-point protocol)
  - AppleTalk
  - Universal asynchronous receiver transmitter (UART)
  - Synchronous UART
  - Serial infrared (IrDA)
  - Binary synchronous communication (BISYNC)
  - Totally transparent (bit streams)
  - Totally transparent (frame based with optional cyclic redundancy check (CRC)
- Two SMCs (serial management channels) (MPC859DSL has one SMC (SMC1) for UART.)
  - UART
  - Transparent
  - General circuit interface (GCI) controller
  - Can be connected to the time-division multiplexed (TDM) channels

- One serial peripheral interface (SPI)
  - Supports master and slave modes
  - Supports multiple-master operation on the same bus
- One inter-integrated circuit ($I^2C$) port
  - Supports master and slave modes
  - Multiple-master environment support
- Time slot assigner (TSA) (MPC859DSL does not have TSA.)
  - Allows SCCs and SMCs to run in multiplexed and/or non-multiplexed operation
  - Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user-defined
  - 1- or 8-bit resolution
  - Allows independent transmit and receive routing, frame synchronization, and clocking
  - Allows dynamic changes
  - On MPC866P and MPC866T, can be internally connected to six serial channels (four SCCs and two SMCs); on MPC859P and MPC859T, can be connected to three serial channels (one SCC and two SMCs).
- Parallel interface port (PIP)
  - Centronics interface support
  - Supports fast connection between compatible ports on MPC866/859 or MC68360
- PCMCIA interface
  - Master (socket) interface, compliant with PCI Local Bus Specification (Rev 2.1)
  - Supports one or two PCMCIA sockets whether ESAR functionality is enabled
  - Eight memory or I/O windows supported
- Debug interface
  - Eight comparators: four operate on instruction address, two operate on data address, and two operate on data.
  - Supports conditions: = ≠ < >
  - Each watchpoint can generate a breakpoint internally
- Normal high and normal low power modes to conserve power
- 1.8 V core and 3.3 V I/O operation with 5-V TTL compatibility; refer to Table 6 for a listing of the 5-V tolerant pins.
- 357-pin plastic ball grid array (PBGA) package
- Operation up to 133 MHz

The MPC866/859 is comprised of three modules that each use a 32-bit internal bus: MPC8xx core, system integration unit (SIU), and communication processor module (CPM). The MPC866P block diagram is shown in Figure 1. The MPC859P/859T/859DSL block diagram is shown in Figure 2.

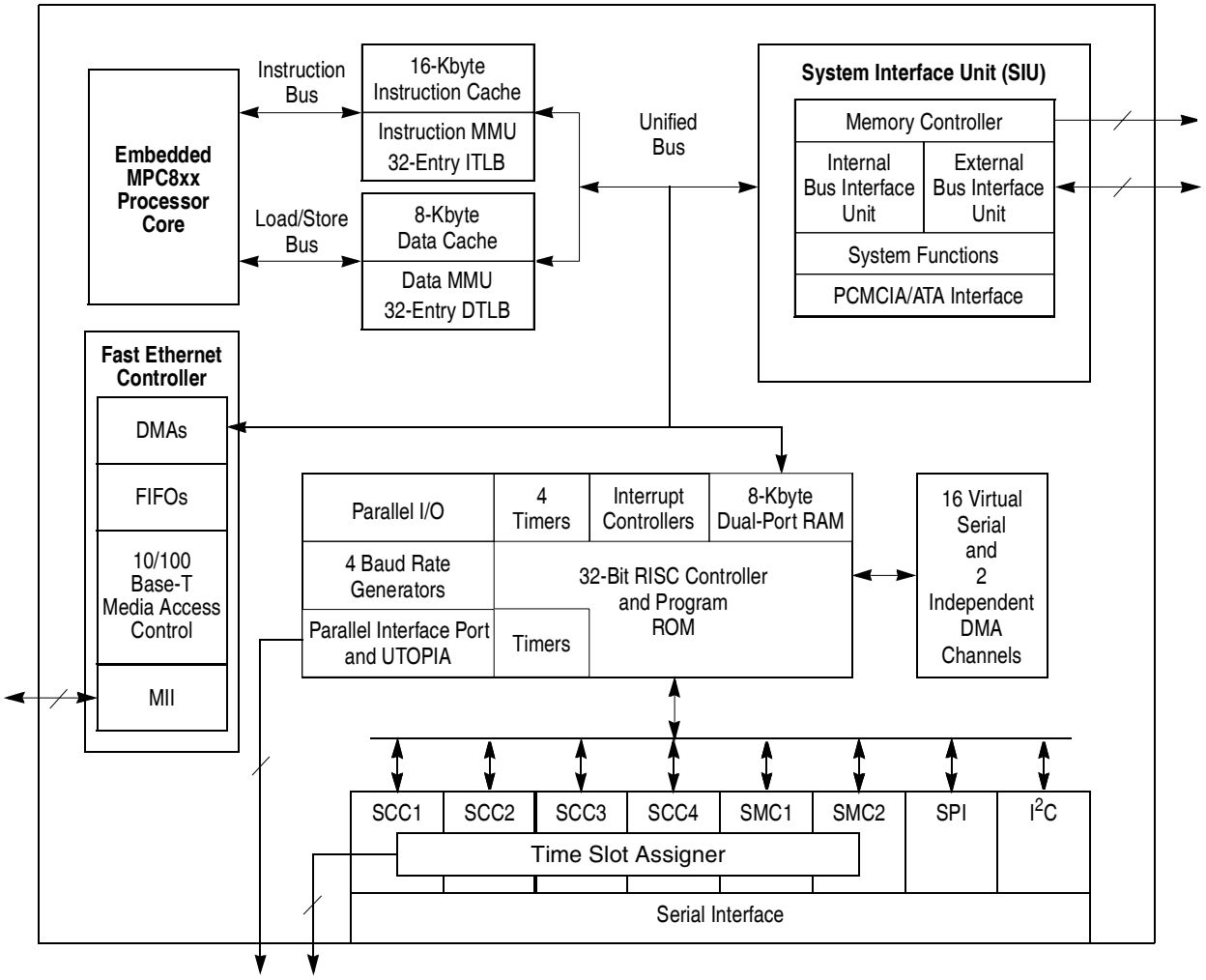
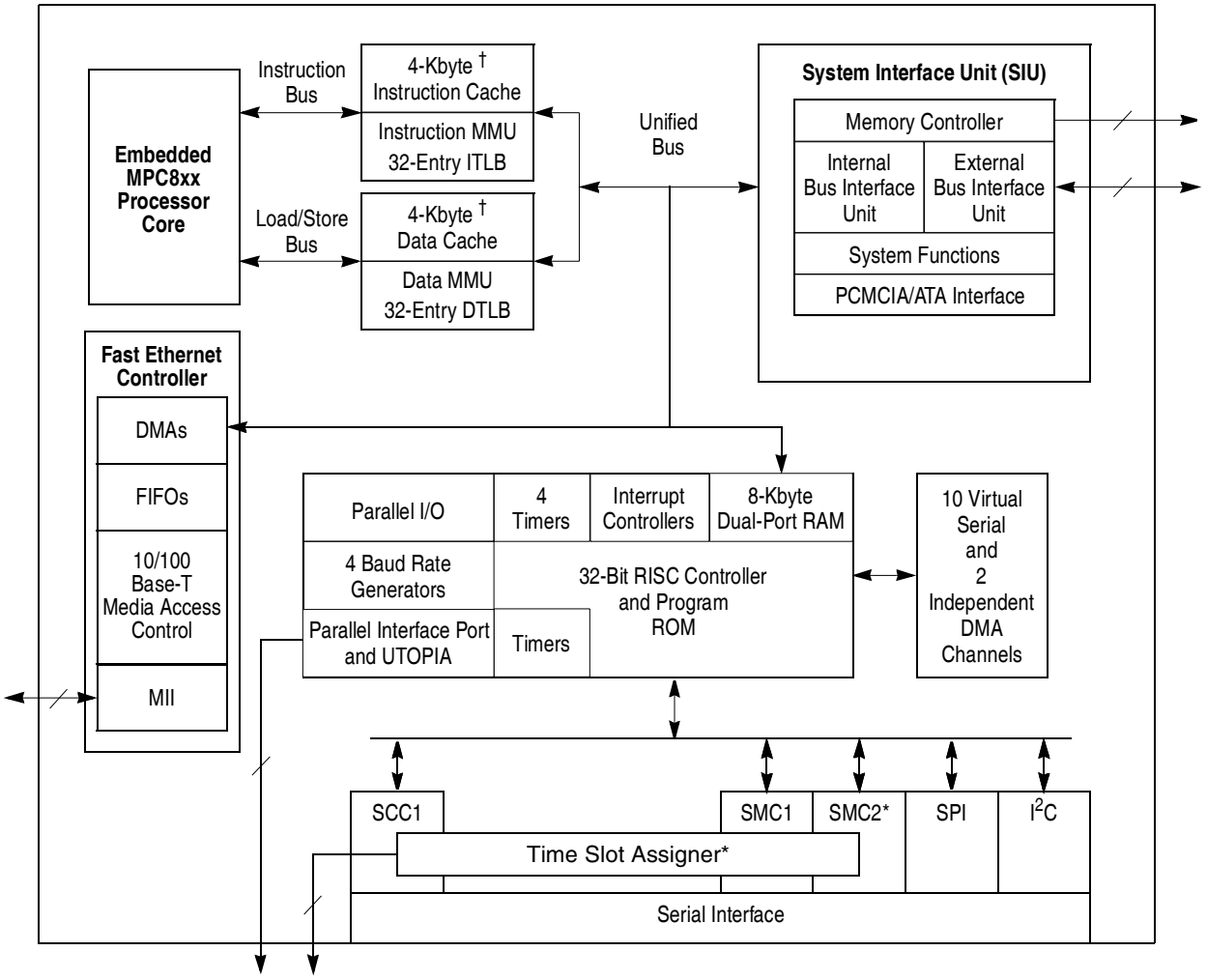



**Figure 1. MPC866P Block Diagram**




† The MPC859P has a 16-Kbyte instruction cache and a 8-Kbyte data cache.

* The MPC859DSL does not contain SMC2 nor the time slot assigner, and provides eight SDMA controllers.

**Figure 2. MPC859P/859T/MPC859DSL Block Diagram**

# 3 Maximum Tolerated Ratings

This section provides the maximum tolerated voltage and temperature ranges for the MPC866/859. Table 2 shows the maximum tolerated ratings, and Table 3 shows the operating temperatures.

**Table 2. Maximum Tolerated Ratings**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage [1] | VDDH | – 0.3 to 4.0 | V |
| | VDDL | – 0.3 to 2.0 | V |
| | VDDSYN | – 0.3 to 2.0 | V |
| | Difference between VDDL to VDDSYN | 100 | mV |
| Input voltage [2] | $V_{in}$ | GND – 0.3 to VDDH | V |
| Storage temperature range | $T_{stg}$ | –55 to +150 | °C |

1 The power supply of the device must start its ramp from 0.0 V.

2 Functional operating conditions are provided with the DC electrical specifications in Table 6. Absolute maximum ratings are stress ratings only; functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device. See page 15.
**Caution**: All inputs that tolerate 5 V cannot be more than 2.5 V greater than VDDH. This restriction applies to power-up and normal operation (that is, if the MPC866/859 is unpowered, a voltage greater than 2.5 V must not be applied to its inputs).

**Table 3. Operating Temperatures**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Temperature [1] (standard) | $T_{A(min)}$ | 0 | °C |
| | $T_{j(max)}$ | 95 | °C |
| Temperature (extended) | $T_{A(min)}$ | –40 | °C |
| | $T_{j(max)}$ | 100 | °C |

1 Minimum temperatures are guaranteed as ambient temperature, $T_A$. Maximum temperatures are guaranteed as junction temperature, $T_j$.

This device contains circuitry protecting against damage due to high-static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or $V_{DD}$).

# 4 Thermal Characteristics

Table 4 shows the thermal characteristics for the MPC866/859.

**Table 4. MPC866/859 Thermal Resistance Data**

| Rating | Environment | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Junction-to-ambient [1] | Natural Convection | Single-layer board (1s) | $R_{\theta JA}$ [2] | 37 | °C/W |
| | | Four-layer board (2s2p) | $R_{\theta JMA}$ [3] | 23 | |
| | Airflow (200 ft/min) | Single-layer board (1s) | $R_{\theta JMA}$ [3] | 30 | |
| | | Four-layer board (2s2p) | $R_{\theta JMA}$ [3] | 19 | |
| Junction-to-board [4] | | | $R_{\theta JB}$ | 13 | |
| Junction-to-case [5] | | | $R_{\theta JC}$ | 6 | |
| Junction-to-package top [6] | Natural Convection | | $\Psi_{JT}$ | 2 | |
| | Airflow (200 ft/min) | | $\Psi_{JT}$ | 2 | |

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. For exposed pad packages where the pad would be expected to be soldered, junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.

6 Thermal characterization parameter indicating the temperature difference between package top and junction temperature per JEDEC JESD51-2.

# 5 Power Dissipation

Table 5 shows power dissipation information. The modes are 1:1, where CPU and bus speeds are equal, and 2:1 mode, where CPU frequency is twice the bus speed.

**Table 5. Power Dissipation ($P_D$)**

| Die Revision | Bus Mode | CPU Frequency | Typical [1] | Maximum [2] | Unit |
|---|---|---|---|---|---|
| 0 | 1:1 | 50 MHz | 110 | 140 | mW |
| | | 66 MHz | 150 | 180 | mW |
| | 2:1 | 66 MHz | 140 | 160 | mW |
| | | 80 MHz | 170 | 200 | mW |
| | | 100 MHz | 210 | 250 | mW |
| | | 133 MHz | 260 | 320 | mW |

1 Typical power dissipation at VDDL and VDDSYN is at 1.8 V. and VDDH is at 3.3 V.

2 Maximum power dissipation at VDDL and VDDSYN is at 1.9 V, and VDDH is at 3.465 V.

**NOTE**

Values in Table 5 represent VDDL based power dissipation and do not include I/O power dissipation over VDDH. I/O power dissipation varies widely by application due to buffer current, depending on external circuitry. The VDDSYN power dissipation is negligible.

# 6 DC Characteristics

Table 6 shows the DC electrical characteristics for the MPC866/859.

**Table 6. DC Electrical Specifications**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating voltage | VDDL (core) | 1.7 | 1.9 | V |
| | VDDH (I/O) | 3.135 | 3.465 | V |
| | VDDSYN [1] | 1.7 | 1.9 | V |
| | Difference between VDDL to VDDSYN | — | 100 | mV |
| Input high voltage (all inputs except EXTAL and EXTCLK) [2] | VIH | 2.0 | 3.465 | V |

**Table 6. DC Electrical Specifications (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input low voltage | VIL | GND | 0.8 | V |
| EXTAL, EXTCLK input high voltage | VIHC | 0.7*(VDDH) | VDDH | V |
| Input leakage current, Vin = 5.5V (except TMS, TRST, DSCK and DSDI pins) for 5 Volts Tolerant Pins [2] | $I_{in}$ | — | 100 | µA |
| Input leakage current, Vin = VDDH (except TMS, TRST, DSCK, and DSDI) | $I_{In}$ | — | 10 | µA |
| Input leakage current, Vin = 0 V (except TMS, TRST, DSCK and DSDI pins) | $I_{In}$ | — | 10 | µA |
| Input capacitance [3] | $C_{in}$ | — | 20 | pF |
| Output high voltage, IOH = – 2.0 mA, except XTAL, and Open drain pins | VOH | 2.4 | — | V |
| Output low voltage<br>• IOL = 2.0 mA (CLKOUT)<br>• IOL = 3.2 mA [4]<br>• IOL = 5.3 mA [5]<br>• IOL = 7.0 mA (TXD1/PA14, TXD2/PA12)<br>• IOL = 8.9 mA (TS, TA, TEA, BI, BB, HRESET, SRESET) | VOL | — | 0.5 | V |

1 The difference between VDDL and VDDSYN can not be more than 100 m V.

2 The signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], TDI, TDO, TCK, TRST_B, TMS, MII_TXEN, MII_MDIO are 5 V tolerant.

3 Input capacitance is periodically sampled.

4 A(0:31), TSIZ0/REG, TSIZ1, D(0:31), DP(0:3)/IRQ(3:6), RD/WR, BURST, RSV/IRQ2, IP_B(0:1)/IWP(0:1)/VFLS(0:1), IP_B2/IOIS16_B/AT2, IP_B3/IWP2/VF2, IP_B4/LWP0/VF0, IP_B5/LWP1/VF1, IP_B6/DSDI/AT0, IP_B7/PTR/AT3, RXD1 /PA15, RXD2/PA13, L1TXDB/PA11, L1RXDB/PA10, L1TXDA/PA9, L1RXDA/PA8, TIN1/L1RCLKA/BRGO1/CLK1/PA7, BRGCLK1/TOUT1/CLK2/PA6, TIN2/L1TCLKA/BRGO2/CLK3/PA5, TOUT2/CLK4/PA4, TIN3/BRGO3/CLK5/PA3, BRGCLK2/L1RCLKB/TOUT3/CLK6/PA2, TIN4/BRGO4/CLK7/PA1, L1TCLKB/TOUT4/CLK8/PA0, REJCT1/SPISEL/PB31, SPICLK/PB30, SPIMOSI/PB29, BRGO4/SPIMISO/PB28, BRGO1/I2CSDA/PB27, BRGO2/I2CSCL/PB26, SMTXD1/PB25, SMRXD1/PB24, SMSYN1/SDACK1/PB23, SMSYN2/SDACK2/PB22, SMTXD2/L1CLKOB/PB21, SMRXD2/L1CLKOA/PB20, L1ST1/RTS1/PB19, L1ST2/RTS2/PB18, L1ST3/L1RQB/PB17, L1ST4/L1RQA/PB16, BRGO3/PB15, RSTRT1/PB14, L1ST1/RTS1/DREQ0/PC15, L1ST2/RTS2/DREQ1/PC14, L1ST3/L1RQB/PC13, L1ST4/L1RQA/PC12, CTS1/PC11, TGATE1/CD1/PC10, CTS2/PC9, TGATE2/CD2/PC8, CTS3/SDACK2/L1TSYNCB/PC7, CD3/L1RSYNCB/PC6, CTS4/SDACK1/L1TSYNCA/PC5, CD4/L1RSYNCA/PC4, PD15/L1TSYNCA, PD14/L1RSYNCA, PD13/L1TSYNCB, PD12/L1RSYNCB, PD11/RXD3, PD10/TXD3, PD9/RXD4, PD8/TXD4, PD5/REJECT2, PD6/RTS4, PD7/RTS3, PD4/REJECT3, PD3, MII_MDC, MII_TX_ER, MII_EN, MII_MDIO, MII_TXD[0:3].

5 BDIP/GPL_B(5), BR, BG, FRZ/IRQ6, CS(0:5), CS(6)/CE(1)_B, CS(7)/CE(2)_B, WE0/BS_B0/IORD, WE1/BS_B1/IOWR, WE2/BS_B2/PCOE, WE3/BS_B3/PCWE, BS_A(0:3), GPL_A0/GPL_B0, OE/GPL_A1/GPL_B1, GPL_A(2:3)/GPL_B(2:3)/CS(2:3), UPWAITA/GPL_A4, UPWAITB/GPL_B4, GPL_A5, ALE_A, CE1_A, CE2_A, ALE_B/DSCK/AT1, OP(0:1), OP2/MODCK1/STS, OP3/MODCK2/DSDO, BADDR(28:30).

# 7 Thermal Calculation and Measurement

For the following discussions, $P_D$ = (VDDL x IDDL) + PI/O, where PI/O is the power dissipation of the I/O drivers. The VDDSYN power dissipation is negligible.

## 7.1 Estimation with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, $T_J$, in °C can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_A$ = ambient temperature (ºC)

$R_{\theta JA}$ = package junction-to-ambient thermal resistance (ºC/W)

$P_D$ = power dissipation in package

The junction-to-ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. However, the answer is only an estimate; test cases have demonstrated that errors of a factor of two (in the quantity $T_J$-$T_A$) are possible.

## 7.2 Estimation with Junction-to-Case Thermal Resistance

Historically, the thermal resistance has frequently been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (ºC/W)

$R_{\theta CA}$ = case-to-ambient thermal resistance (ºC/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user adjusts the thermal environment to affect the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the airflow around the device, add a heat sink, change the mounting arrangement on the printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device. This thermal model is most useful for ceramic packages with heat sinks where some 90% of the heat flows through the case and the heat sink to the ambient environment. For most packages, a better model is required.

## 7.3 Estimation with Junction-to-Board Thermal Resistance

A simple package thermal model that has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board. It has been observed that the thermal performance of most plastic packages and especially PBGA packages is strongly dependent on the board temperature; see Figure 3.

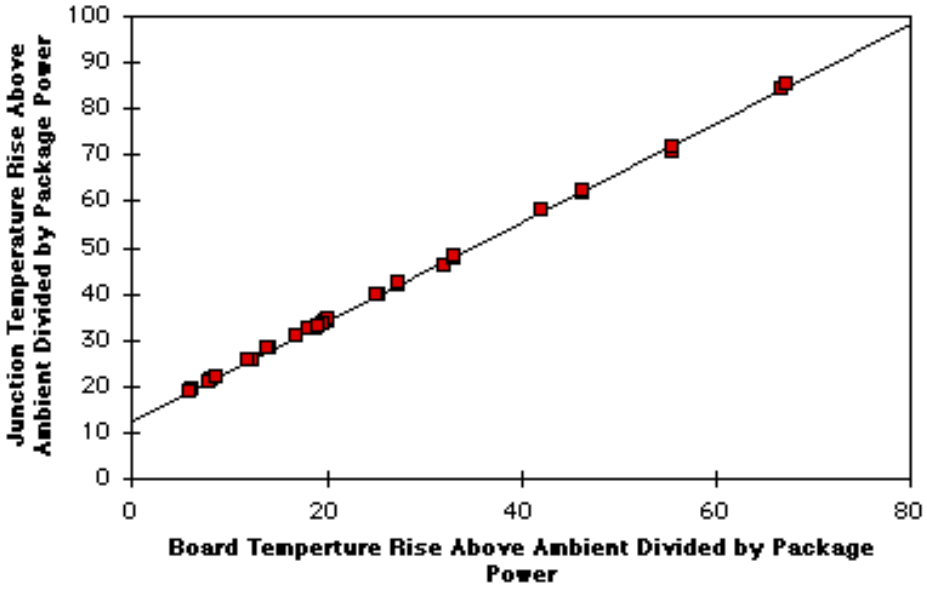



**Figure 3. Effect of Board Temperature Rise on Thermal Behavior**

If the board temperature is known, an estimate of the junction temperature in the environment can be made using the following equation:

$T_J = T_B + (R_{\theta JB} \times P_D)$

where:

$R_{\theta JB}$ = junction-to-board thermal resistance (ºC/W)

$T_B$ = board temperature ºC

$P_D$ = power dissipation in package

If the board temperature is known and the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. For this method to work, the board and board mounting must be similar to the test board used to determine the junction-to-board thermal resistance, namely a 2s2p (board with a power and a ground plane) and vias attaching the thermal balls to the ground plane.

## 7.4 Estimation Using Simulation

When the board temperature is not known, a thermal simulation of the application is needed. The simple two-resistor model can be used with the thermal simulation of the application [2], or a more accurate and complex model of the package can be used in the thermal simulation.

## 7.5 Experimental Determination

To determine the junction temperature of the device in the application after prototypes are available, the thermal characterization parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

$\Psi_{JT}$ = thermal characterization parameter

$T_T$ = thermocouple temperature on top of package

$P_D$ = power dissipation in package

The thermal characterization parameter is measured per JESD51-2 specification published by JEDEC using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 7.6 References

Semiconductor Equipment and Materials International(415) 964-5111
805 East Middlefield Rd.
Mountain View, CA 94043

MIL-SPEC and EIA/JESD (JEDEC) specifications800-854-7179 or
(Available from Global Engineering Documents)303-397-7956

JEDEC Specifications http://www.jedec.org

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.

2. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

# 8 Power Supply and Power Sequencing

This section provides design considerations for the MPC866/859 power supply. The MPC866/859 has a core voltage (VDDL) and PLL voltage (VDDSYN) that operates at a lower voltage than the I/O voltage VDDH. The I/O section of the MPC866/859 is supplied with 3.3 V across VDDH and $V_{SS}$ (GND).

Signals PA[0:15], PB[14:31], PC[4:15], PD[3:15], TDI, TDO, TCK, TRST_B, TMS, MII_TXEN, and MII_MDIO are 5-V tolerant. All inputs cannot be more than 2.5 V greater than VDDH. In addition, 5-V tolerant pins cannot exceed 5.5 V and the remaining input pins cannot exceed 3.465 V. This restriction applies to power up/down and normal operation.

One consequence of multiple power supplies is that when power is initially applied the voltage rails ramp up at different rates. The rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply:

- VDDL must not exceed VDDH during power up and power down.
- VDDL must not exceed 1.9 V and VDDH must not exceed 3.465 V.

These cautions are necessary for the long term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes are forward-biased and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit shown in Figure 4 can be added to meet these requirements. The MUR420 Schottky diodes control the maximum potential difference between the external bus and core power supplies on powerup and the 1N5820 diodes regulate the maximum potential difference on powerdown.

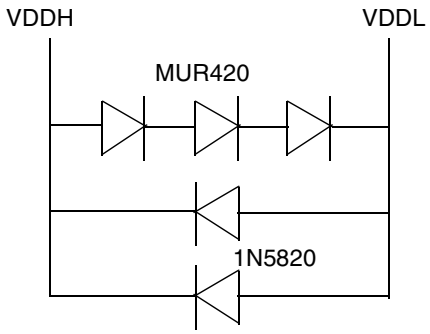



**Figure 4. Example Voltage Sequencing Circuit**

# 9 Layout Practices

Each $V_{DD}$ pin on the MPC866/859 should be provided with a low-impedance path to the board's supply. Furthermore, each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The $V_{DD}$ power supply should be bypassed to ground using at least four 0.1 µF bypass capacitors located as close as possible to the four sides of the package. Each board designed should be characterized and additional appropriate decoupling capacitors should be used if required. The capacitor leads and associated printed-circuit traces connecting to chip $V_{DD}$ and GND should be kept to less than 1/2" per capacitor lead. At a minimum, a four-layer board employing two inner layers as $V_{DD}$ and GND planes should be used.

All output pins on the MPC866/859 have fast rise and fall times. Printed-circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times.

This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of 6” are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the $V_{DD}$ and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins. For more information, please refer to Section 14.4.3, Clock Synthesizer Power (VDDSYN, VSSSYN, VSSSYN1), in the *MPC866 User’s Manual*.

# 10 Bus Signal Timing

The maximum bus speed supported by the MPC866/859 is 66 MHz. Higher-speed parts must be operated in half-speed bus mode (for example, an MPC866/859 used at 100 MHz must be configured for a 50-MHz bus). Table 7 and Table 8 show the frequency ranges for standard part frequencies.

**Table 7. Frequency Ranges for Standard Part Frequencies (1:1 Bus Mode)**

| Part Freq | 50 MHz | | 66 MHz | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| Core | 40 | 50 | 40 | 66.67 |
| Bus | 40 | 50 | 40 | 66.67 |

**Table 8. Frequency Ranges for Standard Part Frequencies (2:1 Bus Mode)**

| Part Freq | 50 MHz | | 66 MHz | | 100 MHz | | 133 MHz | |
|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min | Max |
| Core | 40 | 50 | 40 | 66.67 | 40 | 100 | 40 | 133.34 |
| Bus | 20 | 25 | 20 | 33.33 | 20 | 50 | 20 | 66.67 |

Table 9 shows the timings for the MPC866/859 at 33, 40, 50, and 66 MHz bus operation. The timing for the MPC866/859 bus shown in this table assumes a 50-pF load for maximum delays and a 0-pF load for minimum delays. CLKOUT assumes a 100-pF load maximum delay.

**Table 9. Bus Operation Timings**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B1 | Bus Period (CLKOUT) See Table 7 | — | — | — | — | — | — | — | — | ns |
| B1a | EXTCLK to CLKOUT phase skew | – 2 | +2 | – 2 | +2 | – 2 | +2 | – 2 | +2 | ns |
| B1b | CLKOUT frequency jitter peak-to-peak | — | 1 | — | 1 | — | 1 | — | 1 | ns |
| B1c | Frequency jitter on EXTCLK | — | 0.50 | — | 0.50 | — | 0.50 | — | 0.50 | % |

**Table 9. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B1d | CLKOUT phase jitter peak-to-peak for OSCLK ≥ 15 MHz | — | 4 | — | 4 | — | 4 | — | 4 | ns |
| | CLKOUT phase jitter peak-to-peak for OSCLK < 15 MHz | — | 5 | — | 5 | — | 5 | — | 5 | ns |
| B2 | CLKOUT pulse width low (MIN = 0.4 x B1, MAX = 0.6 x B1) | 12.1 | 18.2 | 10.0 | 15.0 | 8.0 | 12.0 | 6.1 | 9.1 | ns |
| B3 | CLKOUT pulse width high (MIN = 0.4 x B1, MAX = 0.6 x B1) | 12.1 | 18.2 | 10.0 | 15.0 | 8.0 | 12.0 | 6.1 | 9.1 | ns |
| B4 | CLKOUT rise time | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |
| B5 | CLKOUT fall time | — | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | ns |
| B7 | CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3) output hold (MIN = 0.25 x B1) | 7.60 | — | 6.30 | — | 5.00 | — | 3.80 | — | ns |
| B7a | CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), $\overline{BDIP}$, PTR output hold (MIN = 0.25 x B1) | 7.60 | — | 6.30 | — | 5.00 | — | 3.80 | — | ns |
| B7b | CLKOUT to $\overline{BR}$, $\overline{BG}$, FRZ, VFLS(0:1), VF(0:2), IWP(0:2), LWP(0:1), $\overline{STS}$ output hold (MIN = 0.25 x B1) | 7.60 | — | 6.30 | — | 5.00 | — | 3.80 | — | ns |
| B8 | CLKOUT to A(0:31), BADDR(28:30) RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), valid (MAX = 0.25 x B1 + 6.3) | — | 13.80 | — | 12.50 | — | 11.30 | — | 10.00 | ns |
| B8a | CLKOUT to TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), $\overline{BDIP}$, PTR valid (MAX = 0.25 x B1 + 6.3) | — | 13.80 | — | 12.50 | — | 11.30 | — | 10.00 | ns |
| B8b | CLKOUT to $\overline{BR}$, $\overline{BG}$, VFLS(0:1), VF(0:2), IWP(0:2), FRZ, LWP(0:1), $\overline{STS}$ valid [4] (MAX = 0.25 x B1 + 6.3) | — | 13.80 | — | 12.50 | — | 11.30 | — | 10.00 | ns |
| B9 | CLKOUT to A(0:31), BADDR(28:30), RD/$\overline{WR}$, $\overline{BURST}$, D(0:31), DP(0:3), TSIZ(0:1), $\overline{REG}$, $\overline{RSV}$, AT(0:3), PTR High-Z (MAX = 0.25 x B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 5.00 | 11.30 | 3.80 | 10.00 | ns |
| B11 | CLKOUT to $\overline{TS}$, $\overline{BB}$ assertion (MAX = 0.25 x B1 + 6.0) | 7.60 | 13.60 | 6.30 | 12.30 | 5.00 | 11.00 | 3.80 | 9.80 | ns |
| B11a | CLKOUT to $\overline{TA}$, $\overline{BI}$ assertion (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.30 [1]) | 2.50 | 9.30 | 2.50 | 9.30 | 2.50 | 9.30 | 2.50 | 9.80 | ns |
| B12 | CLKOUT to $\overline{TS}$, $\overline{BB}$ negation (MAX = 0.25 x B1 + 4.8) | 7.60 | 12.30 | 6.30 | 11.00 | 5.00 | 9.80 | 3.80 | 8.50 | ns |

**Table 9. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B12a | CLKOUT to $\overline{TA}$, $\overline{BI}$ negation (when driven by the memory controller or PCMCIA interface) (MAX = 0.00 x B1 + 9.00) | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | ns |
| B13 | CLKOUT to $\overline{TS}$, $\overline{BB}$ High-Z (MIN = 0.25 x B1) | 7.60 | 21.60 | 6.30 | 20.30 | 5.00 | 19.00 | 3.80 | 14.00 | ns |
| B13a | CLKOUT to $\overline{TA}$, $\overline{BI}$ High-Z (when driven by the memory controller or PCMCIA interface) (MIN = 0.00 x B1 + 2.5) | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | ns |
| B14 | CLKOUT to $\overline{TEA}$ assertion (MAX = 0.00 x B1 + 9.00) | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | 2.50 | 9.00 | ns |
| B15 | CLKOUT to $\overline{TEA}$ High-Z (MIN = 0.00 x B1 + 2.50) | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | 2.50 | 15.00 | ns |
| B16 | $\overline{TA}$, $\overline{BI}$ valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 6.00) | 6.00 | — | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| B16a | $\overline{TEA}$, $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid to CLKOUT (setup time) (MIN = 0.00 x B1 + 4.5) | 4.50 | — | 4.50 | — | 4.50 | — | 4.50 | — | ns |
| B16b | $\overline{BB}$, $\overline{BG}$, $\overline{BR}$, valid to CLKOUT (setup time) [2] (4 MIN = 0.00 x B1 + 0.00 ) | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | — | ns |
| B17 | CLKOUT to $\overline{TA}$, $\overline{TEA}$, $\overline{BI}$, $\overline{BB}$, $\overline{BG}$, $\overline{BR}$ valid (hold time) (MIN = 0.00 x B1 + 1.00 [3]) | 1.00 | — | 1.00 | — | 1.00 | — | 2.00 | — | ns |
| B17a | CLKOUT to $\overline{KR}$, $\overline{RETRY}$, $\overline{CR}$ valid (hold time) (MIN = 0.00 x B1 + 2.00) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B18 | D(0:31), DP(0:3) valid to CLKOUT rising edge (setup time) [4] (MIN = 0.00 x B1 + 6.00) | 6.00 | — | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| B19 | CLKOUT rising edge to D(0:31), DP(0:3) valid (hold time) [4] (MIN = 0.00 x B1 + 1.00 [5]) | 1.00 | — | 1.00 | — | 1.00 | — | 2.00 | — | ns |
| B20 | D(0:31), DP(0:3) valid to CLKOUT falling edge (setup time) [6](MIN = 0.00 x B1 + 4.00) | 4.00 | — | 4.00 | — | 4.00 | — | 4.00 | — | ns |
| B21 | CLKOUT falling edge to D(0:31), DP(0:3) valid (hold Time) [6] (MIN = 0.00 x B1 + 2.00) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B22 | CLKOUT rising edge to $\overline{CS}$ asserted GPCM ACS = 00 (MAX = 0.25 x B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 5.00 | 11.30 | 3.80 | 10.00 | ns |
| B22a | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MAX = 0.00 x B1 + 8.00) | — | 8.00 | — | 8.00 | — | 8.00 | — | 8.00 | ns |

**Table 9. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B22b | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 0 (MAX = 0.25 x B1 + 6.3) | 7.60 | 13.80 | 6.30 | 12.50 | 5.00 | 11.30 | 3.80 | 10.00 | ns |
| B22c | CLKOUT falling edge to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0, EBDF = 1 (MAX = 0.375 x B1 + 6.6) | 10.90 | 18.00 | 10.90 | 16.00 | 7.00 | 14.10 | 5.20 | 12.30 | ns |
| B23 | CLKOUT rising edge to $\overline{CS}$ negated GPCM read access, GPCM write access ACS = 00, TRLX = 0 & CSNT = 0 (MAX = 0.00 x B1 + 8.00) | 2.00 | 8.00 | 2.00 | 8.00 | 2.00 | 8.00 | 2.00 | 8.00 | ns |
| B24 | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 0 (MIN = 0.25 x B1 - 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |
| B24a | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 0 (MIN = 0.50 x B1 - 2.00) | 13.20 | — | 10.50 | — | 8.00 | — | 5.60 | — | ns |
| B25 | CLKOUT rising edge to $\overline{OE}$, $\overline{WE}$(0:3) asserted (MAX = 0.00 x B1 + 9.00) | — | 9.00 | — | 9.00 | — | 9.00 | — | 9.00 | ns |
| B26 | CLKOUT rising edge to $\overline{OE}$ negated (MAX = 0.00 x B1 + 9.00) | 2.00 | 9.00 | 2.00 | 9.00 | 2.00 | 9.00 | 2.00 | 9.00 | ns |
| B27 | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 10, TRLX = 1 (MIN = 1.25 x B1 - 2.00) | 35.90 | — | 29.30 | — | 23.00 | — | 16.90 | — | ns |
| B27a | A(0:31) and BADDR(28:30) to $\overline{CS}$ asserted GPCM ACS = 11, TRLX = 1 (MIN = 1.50 x B1 - 2.00) | 43.50 | — | 35.50 | — | 28.00 | — | 20.70 | — | ns |
| B28 | CLKOUT rising edge to $\overline{WE}$(0:3) negated GPCM write access CSNT = 0 (MAX = 0.00 x B1 + 9.00) | — | 9.00 | — | 9.00 | — | 9.00 | — | 9.00 | ns |
| B28a | CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0,1, CSNT = 1, EBDF = 0 (MAX = 0.25 x B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 5.00 | 11.80 | 3.80 | 10.50 | ns |
| B28b | CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 0 (MAX = 0.25 x B1 + 6.80) | — | 14.30 | — | 13.00 | — | 11.80 | — | 10.50 | ns |
| B28c | CLKOUT falling edge to $\overline{WE}$(0:3) negated GPCM write access TRLX = 0, CSNT = 1 write access TRLX = 0,1, CSNT = 1, EBDF = 1 (MAX = 0.375 x B1 + 6.6) | 10.90 | 18.00 | 10.90 | 18.00 | 7.00 | 14.30 | 5.20 | 12.30 | ns |

**Table 9. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B28d | CLKOUT falling edge to $\overline{CS}$ negated GPCM write access TRLX = 0,1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 1 (MAX = 0.375 x B1 + 6.6) | — | 18.00 | — | 18.00 | — | 14.30 | — | 12.30 | ns |
| B29 | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, CSNT = 0, EBDF = 0 (MIN = 0.25 x B1 - 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |
| B29a | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 0 (MIN = 0.50 x B1 – 2.00) | 13.20 | — | 10.50 | — | 8.00 | — | 5.60 | — | ns |
| B29b | $\overline{CS}$ negated to D(0:31), DP(0:3), High Z GPCM write access, ACS = 00, TRLX = 0,1 & CSNT = 0 (MIN = 0.25 x B1– 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |
| B29c | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0 (MIN = 0.50 x B1 – 2.00) | 13.20 | — | 10.50 | — | 8.00 | — | 5.60 | — | ns |
| B29d | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 0 (MIN = 1.50 x B1 – 2.00) | 43.50 | — | 35.50 | — | 28.00 | — | 20.70 | — | ns |
| B29e | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10, or ACS = 11, EBDF = 0 (MIN = 1.50 x B1 – 2.00) | 43.50 | — | 35.50 | — | 28.00 | — | 20.70 | — | ns |
| B29f | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 0, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 – 6.30) | 5.00 | — | 3.00 | — | 1.10 | — | 0.00 | — | ns |
| B29g | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 0, CSNT = 1 ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 – 6.30) | 5.00 | — | 3.00 | — | 1.10 | — | 0.00 | — | ns |
| B29h | $\overline{WE}$(0:3) negated to D(0:31), DP(0:3) High Z GPCM write access, TRLX = 1, CSNT = 1, EBDF = 1 (MIN = 0.375 x B1 – 3.30) | 38.40 | — | 31.10 | — | 24.20 | — | 17.50 | — | ns |
| B29i | $\overline{CS}$ negated to D(0:31), DP(0:3) High-Z GPCM write access, TRLX = 1, CSNT = 1, ACS = 10 or ACS = 11, EBDF = 1 (MIN = 0.375 x B1 – 3.30) | 38.40 | — | 31.10 | — | 24.20 | — | 17.50 | — | ns |

**Table 9. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B30 | $\overline{CS}$, $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access [7] (MIN = 0.25 x B1 – 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |
| B30a | $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM, write access, TRLX = 0, CSNT = 1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 0, CSNT =1 ACS = 10, or ACS == 11, EBDF = 0 (MIN = 0.50 x B1 – 2.00) | 13.20 | — | 10.50 | — | 8.00 | — | 5.60 | — | ns |
| B30b | $\overline{WE}$(0:3) negated to A(0:31) invalid GPCM BADDR(28:30) invalid GPCM write access, TRLX = 1, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10, or ACS == 11 EBDF = 0 (MIN = 1.50 x B1 – 2.00) | 43.50 | — | 35.50 | — | 28.00 | — | 20.70 | — | ns |
| B30c | $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access, TRLX = 0, CSNT = 1. $\overline{CS}$ negated to A(0:31) invalid GPCM write access, TRLX = 0, CSNT = 1 ACS = 10, ACS == 11, EBDF = 1 (MIN = 0.375 x B1 – 3.00) | 8.40 | — | 6.40 | — | 4.50 | — | 2.70 | — | ns |
| B30d | $\overline{WE}$(0:3) negated to A(0:31), BADDR(28:30) invalid GPCM write access TRLX = 1, CSNT =1, $\overline{CS}$ negated to A(0:31) invalid GPCM write access TRLX = 1, CSNT = 1, ACS = 10 or 11, EBDF = 1 | 38.67 | — | 31.38 | — | 24.50 | — | 17.83 | — | ns |
| B31 | CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MAX = 0.00 X B1 + 6.00) | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B31a | CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 5.00 | 11.80 | 3.80 | 10.50 | ns |
| B31b | CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00) | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | ns |
| B31c | CLKOUT rising edge to $\overline{CS}$ valid, as requested by control bit CST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.30) | 7.60 | 13.80 | 6.30 | 12.50 | 5.00 | 11.30 | 3.80 | 10.00 | ns |

**Table 9. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B31d | CLKOUT falling edge to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM EBDF = 1 (MAX = 0.375 x B1 + 6.6) | 13.30 | 18.00 | 11.30 | 16.00 | 9.40 | 14.10 | 7.60 | 12.30 | ns |
| B32 | CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00) | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B32a | CLKOUT falling edge to $\overline{BS}$ valid, as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 0 (MAX = 0.25 x B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 5.00 | 11.80 | 3.80 | 10.50 | ns |
| B32b | CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MAX = 0.00 x B1 + 8.00) | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | 1.50 | 8.00 | ns |
| B32c | CLKOUT rising edge to $\overline{BS}$ valid, as requested by control bit BST3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 5.00 | 11.80 | 3.80 | 10.50 | ns |
| B32d | CLKOUT falling edge to $\overline{BS}$ valid- as requested by control bit BST1 in the corresponding word in the UPM, EBDF = 1 (MAX = 0.375 x B1 + 6.60) | 13.30 | 18.00 | 11.30 | 16.00 | 9.40 | 14.10 | 7.60 | 12.30 | ns |
| B33 | CLKOUT falling edge to $\overline{GPL}$ valid, as requested by control bit GxT4 in the corresponding word in the UPM (MAX = 0.00 x B1 + 6.00) | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | 1.50 | 6.00 | ns |
| B33a | CLKOUT rising edge to $\overline{GPL}$ valid, as requested by control bit GxT3 in the corresponding word in the UPM (MAX = 0.25 x B1 + 6.80) | 7.60 | 14.30 | 6.30 | 13.00 | 5.00 | 11.80 | 3.80 | 10.50 | ns |
| B34 | A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by control bit CST4 in the corresponding word in the UPM (MIN = 0.25 x B1 - 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |
| B34a | A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by control bit CST1 in the corresponding word in the UPM (MIN = 0.50 x B1 – 2.00) | 13.20 | — | 10.50 | — | 8.00 | — | 5.60 | — | ns |
| B34b | A(0:31), BADDR(28:30), and D(0:31) to $\overline{CS}$ valid, as requested by CST2 in the corresponding word in UPM (MIN = 0.75 x B1 – 2.00) | 20.70 | — | 16.70 | — | 13.00 | — | 9.40 | — | ns |

**Table 9. Bus Operation Timings (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| B35 | A(0:31), BADDR(28:30) to $\overline{CS}$ valid, as requested by control bit BST4 in the corresponding word in the UPM (MIN = 0.25 x B1 – 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |
| B35a | A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as Requested by BST1 in the corresponding word in the UPM (MIN = 0.50 x B1 – 2.00) | 13.20 | — | 10.50 | — | 8.00 | — | 5.60 | — | ns |
| B35b | A(0:31), BADDR(28:30), and D(0:31) to $\overline{BS}$ valid, as requested by control bit BST2 in the corresponding word in the UPM (MIN = 0.75 x B1 – 2.00) | 20.70 | — | 16.70 | — | 13.00 | — | 9.40 | — | ns |
| B36 | A(0:31), BADDR(28:30), and D(0:31) to $\overline{GPL}$ valid as requested by control bit GxT4 in the corresponding word in the UPM (MIN = 0.25 x B1 – 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |
| B37 | UPWAIT valid to CLKOUT falling edge [8] (MIN = 0.00 x B1 + 6.00) | 6.00 | — | 6.00 | — | 6.00 | — | 6.00 | — | ns |
| B38 | CLKOUT falling edge to UPWAIT valid[8] (MIN = 0.00 x B1 + 1.00) | 1.00 | — | 1.00 | — | 1.00 | — | 1.00 | — | ns |
| B39 | $\overline{AS}$ valid to CLKOUT rising edge [9] (MIN = 0.00 x B1 + 7.00) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B40 | A(0:31), TSIZ(0:1), RD/$\overline{WR}$, $\overline{BURST}$, valid to CLKOUT rising edge (MIN = 0.00 x B1 + 7.00) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B41 | $\overline{TS}$ valid to CLKOUT rising edge (setup time) (MIN = 0.00 x B1 + 7.00) | 7.00 | — | 7.00 | — | 7.00 | — | 7.00 | — | ns |
| B42 | CLKOUT rising edge to $\overline{TS}$ valid (hold time) (MIN = 0.00 x B1 + 2.00) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |
| B43 | $\overline{AS}$ negation to memory controller signals negation (MAX = TBD) | — | TBD | — | TBD | — | TBD | — | TBD | ns |

1 For part speeds above 50 MHz, use 9.80 ns for B11a.

2 The timing required for $\overline{BR}$ input is relevant when the MPC866/859 is selected to work with the internal bus arbiter. The timing for $\overline{BG}$ input is relevant when the MPC866/859 is selected to work with the external bus arbiter.

3 For part speeds above 50 MHz, use 2 ns for B17.

4 The D(0:31) and DP(0:3) input timings B18 and B19 refer to the rising edge of CLKOUT, in which the $\overline{TA}$ input signal is asserted.

5 For part speeds above 50 MHz, use 2 ns for B19.

6 The D(0:31) and DP(0:3) input timings B20 and B21 refer to the falling edge of CLKOUT. This timing is valid only for read accesses controlled by chip-selects under control of the UPM in the memory controller, for data beats, where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

7 The timing B30 refers to $\overline{CS}$ when ACS = 00 and to $\overline{WE}$(0:3) when CSNT = 0.

8 The signal UPWAIT is considered asynchronous to CLKOUT and synchronized internally. The timings specified in B37 and B38 are specified to enable the freeze of the UPM output signals as described in Figure 20.

9 The $\overline{AS}$ signal is considered asynchronous to CLKOUT. The timing B39 is specified in order to allow the behavior specified in Figure 23.

Figure 5 shows the control timing diagram.

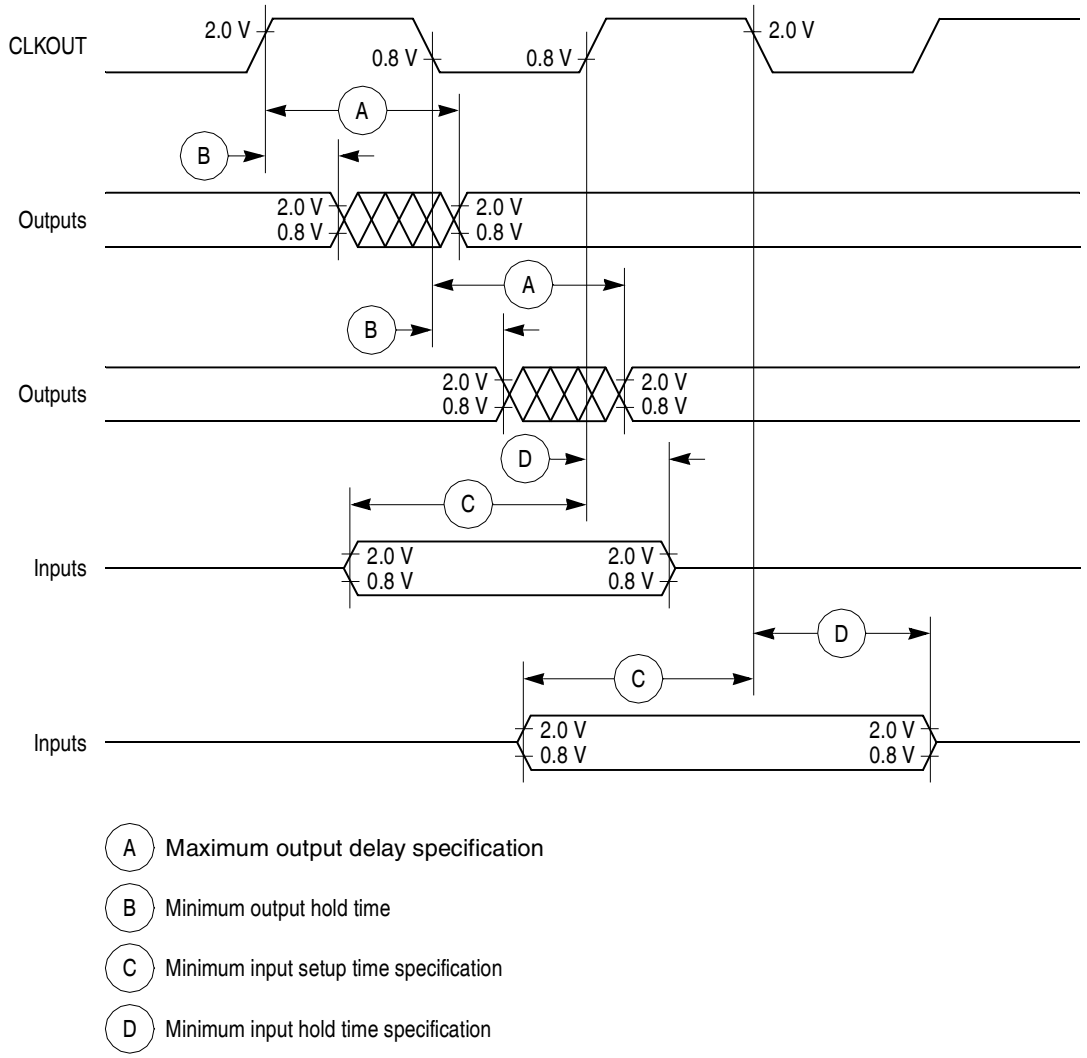



**Figure 5. Control Timing**

Figure 6 shows the timing for the external clock.

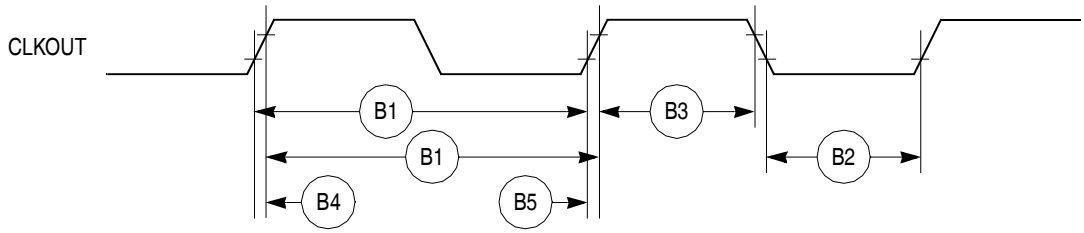



**Figure 6. External Clock Timing**

Figure 7 shows the timing for the synchronous output signals.

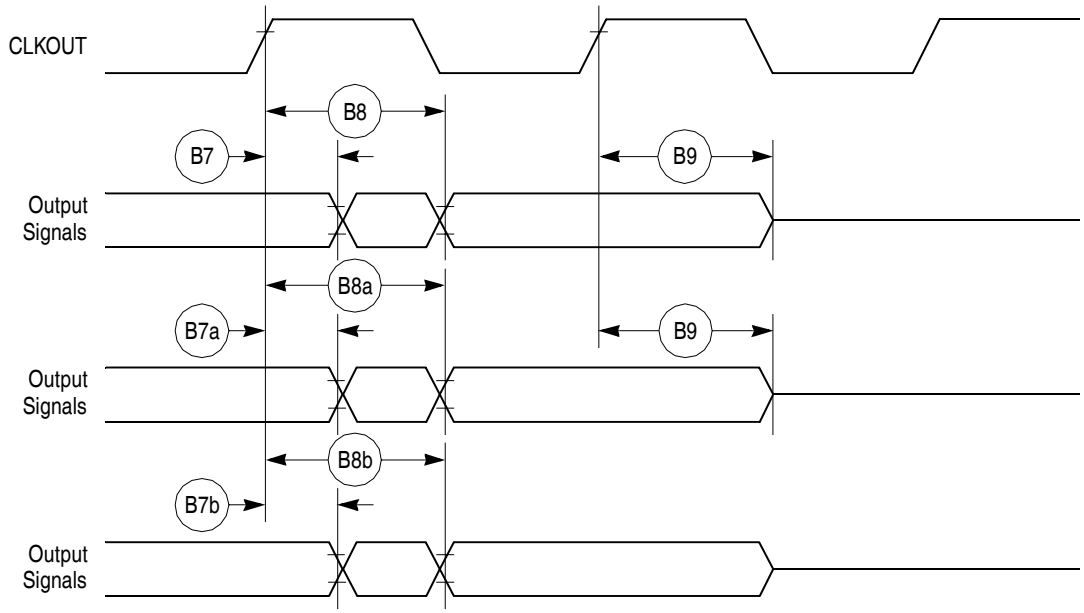



**Figure 7. Synchronous Output Signals Timing**

Figure 8 shows the timing for the synchronous active pull-up and open-drain output signals.

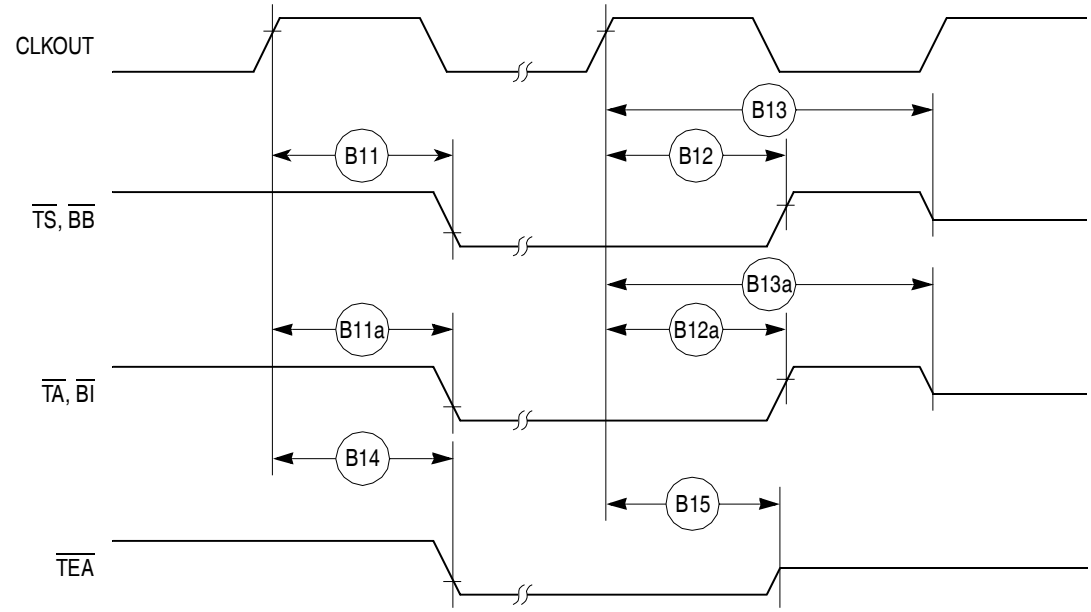



**Figure 8. Synchronous Active Pull-Up Resistor and Open-Drain Output Signals Timing**

Figure 9 shows the timing for the synchronous input signals.

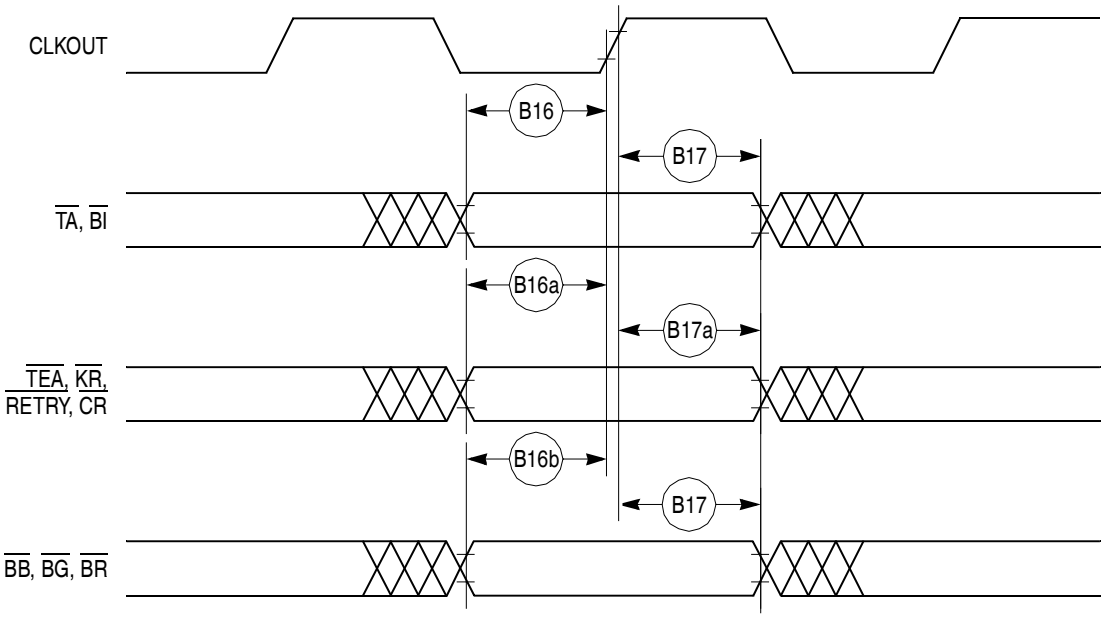



**Figure 9. Synchronous Input Signals Timing**

Figure 10 shows normal case timing for input data. It also applies to normal read accesses under the control of the UPM in the memory controller.

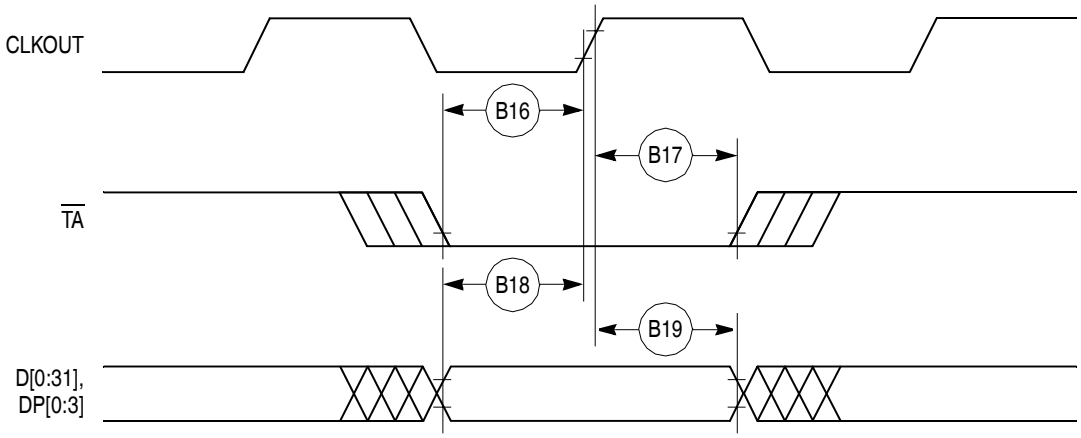



**Figure 10. Input Data Timing in Normal Case**

Figure 11 shows the timing for the input data controlled by the UPM for data beats where DLT3 = 1 in the UPM RAM words. (This is only the case where data is latched on the falling edge of CLKOUT.)

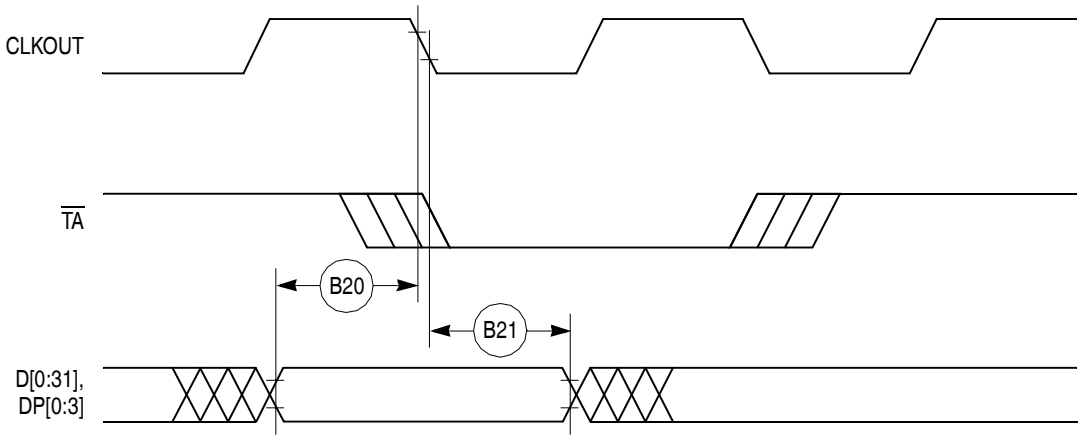



**Figure 11. Input Data Timing when Controlled by UPM in the Memory Controller and DLT3 = 1**

Figure 12 through Figure 15 show the timing for the external bus read controlled by various GPCM factors.

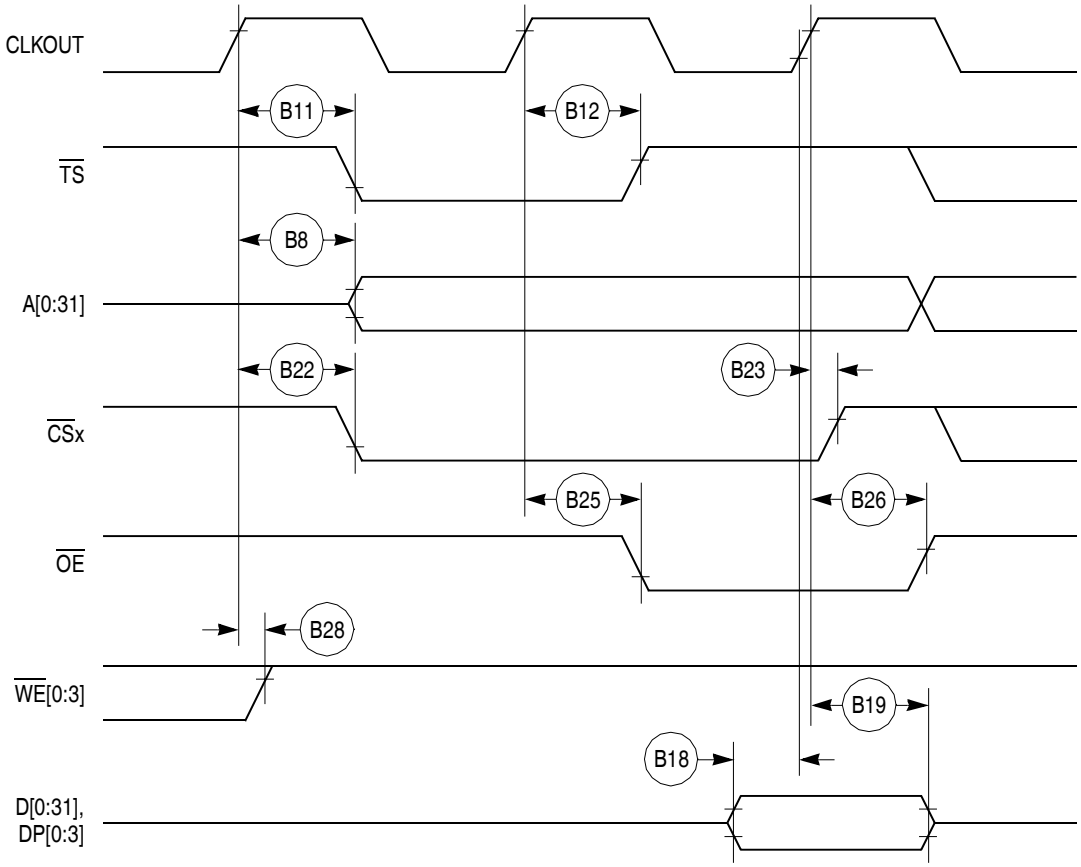



**Figure 12. External Bus Read Timing (GPCM Controlled—ACS = 00)**

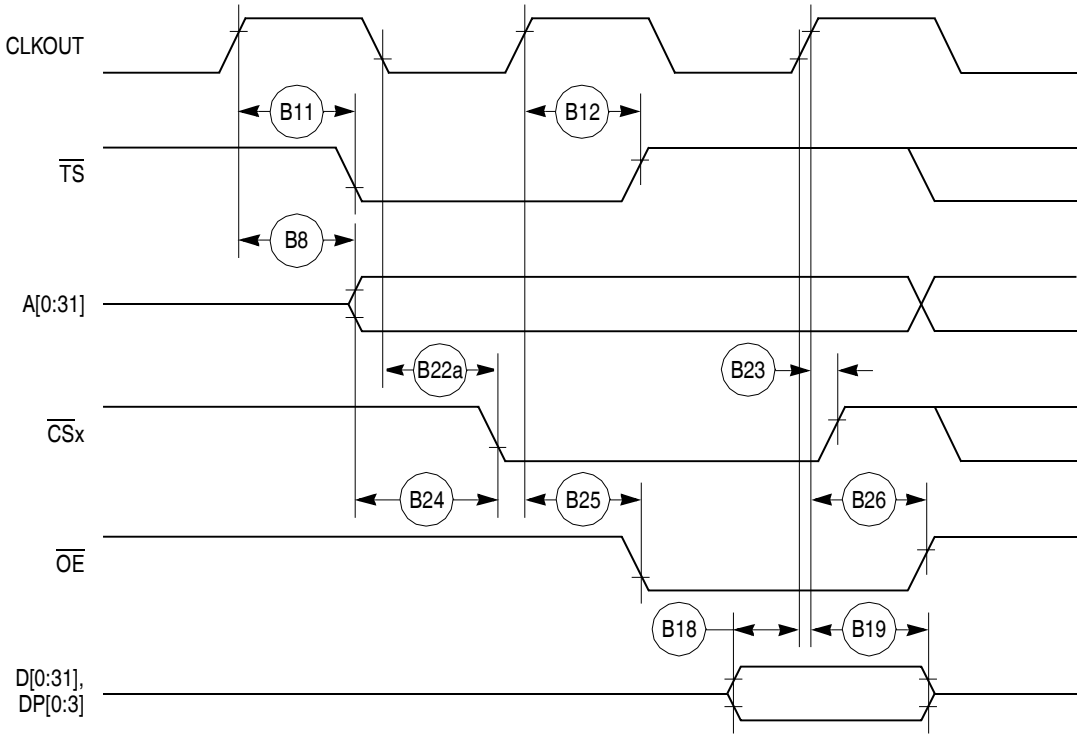



**Figure 13. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10)**

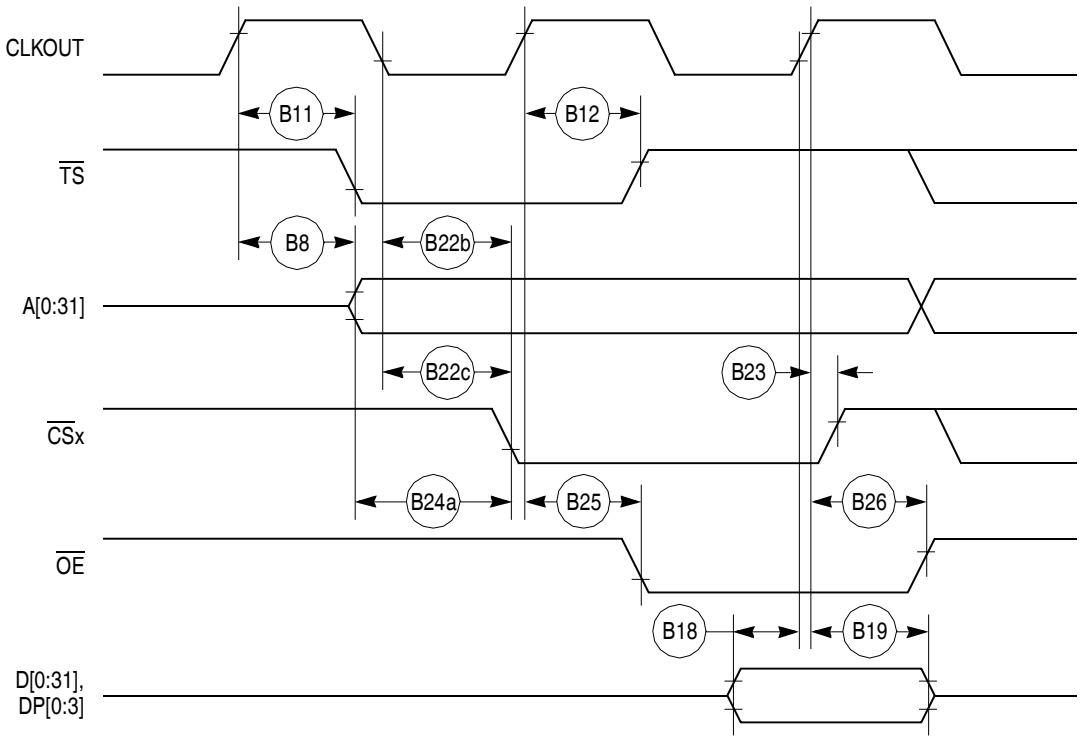



**Figure 14. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 11)**

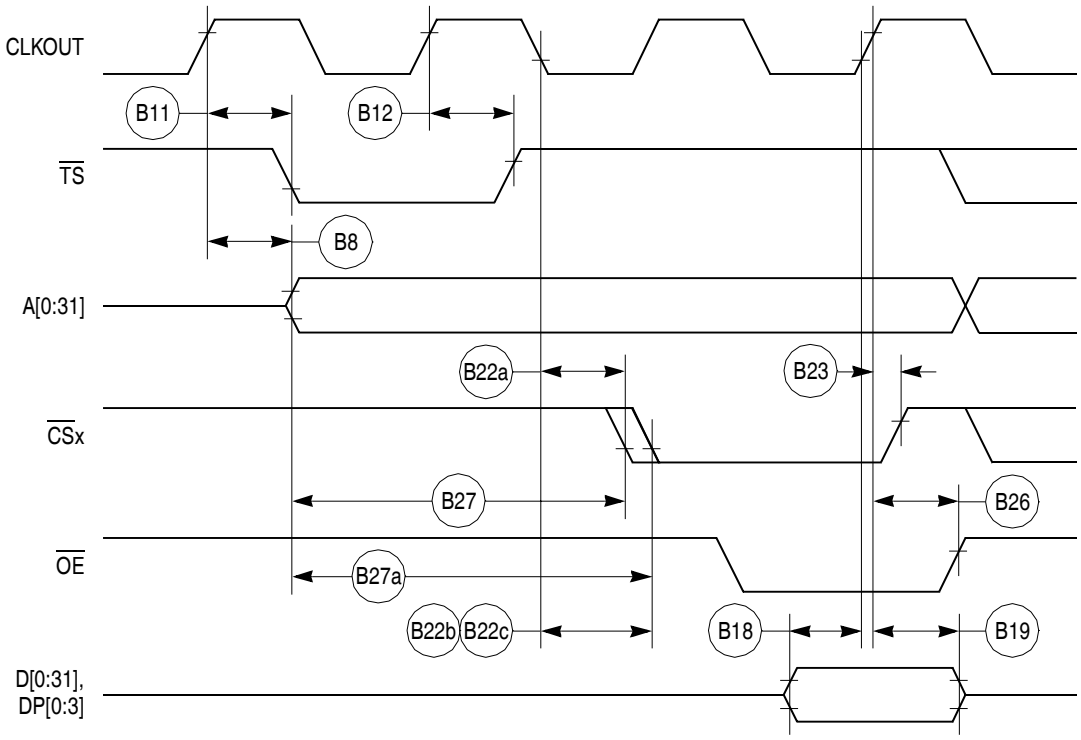



**Figure 15. External Bus Read Timing (GPCM Controlled—TRLX = 0 or 1, ACS = 10, ACS = 11)**

Figure 16 through Figure 18 show the timing for the external bus write controlled by various GPCM factors.

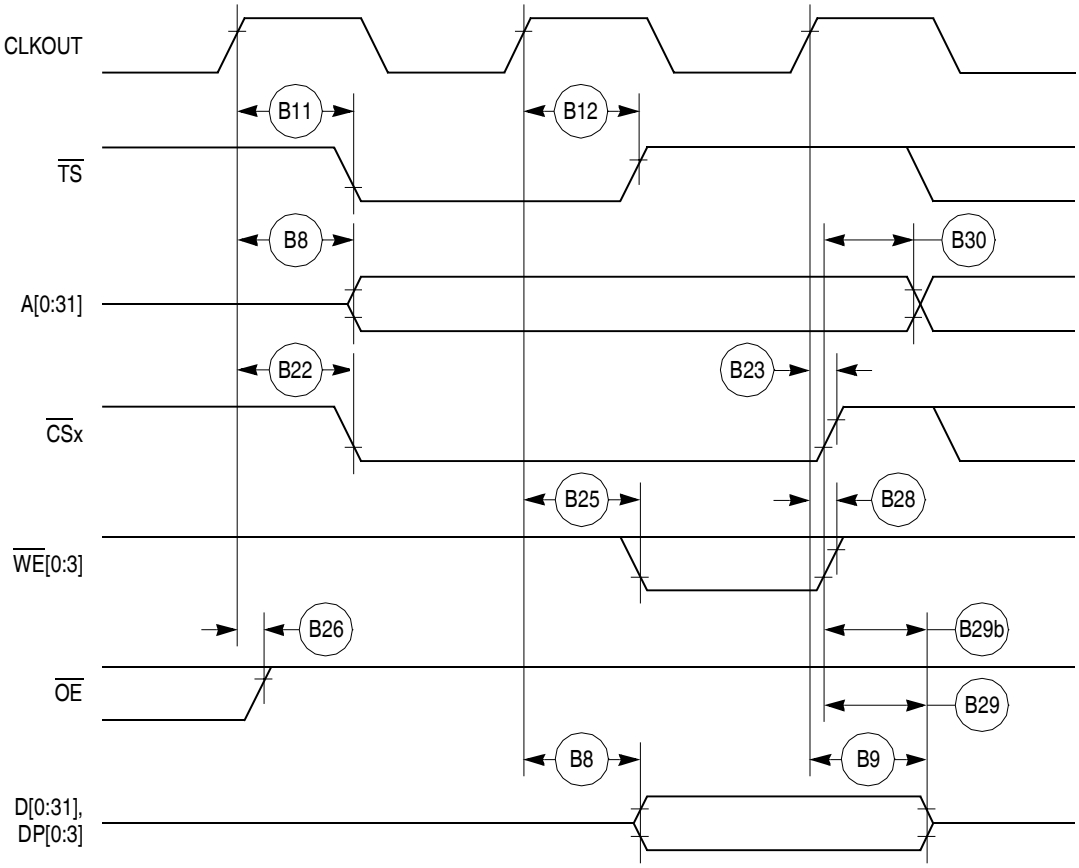



**Figure 16. External Bus Write Timing (GPCM Controlled—TRLX = 0 or 1, CSNT = 0)**

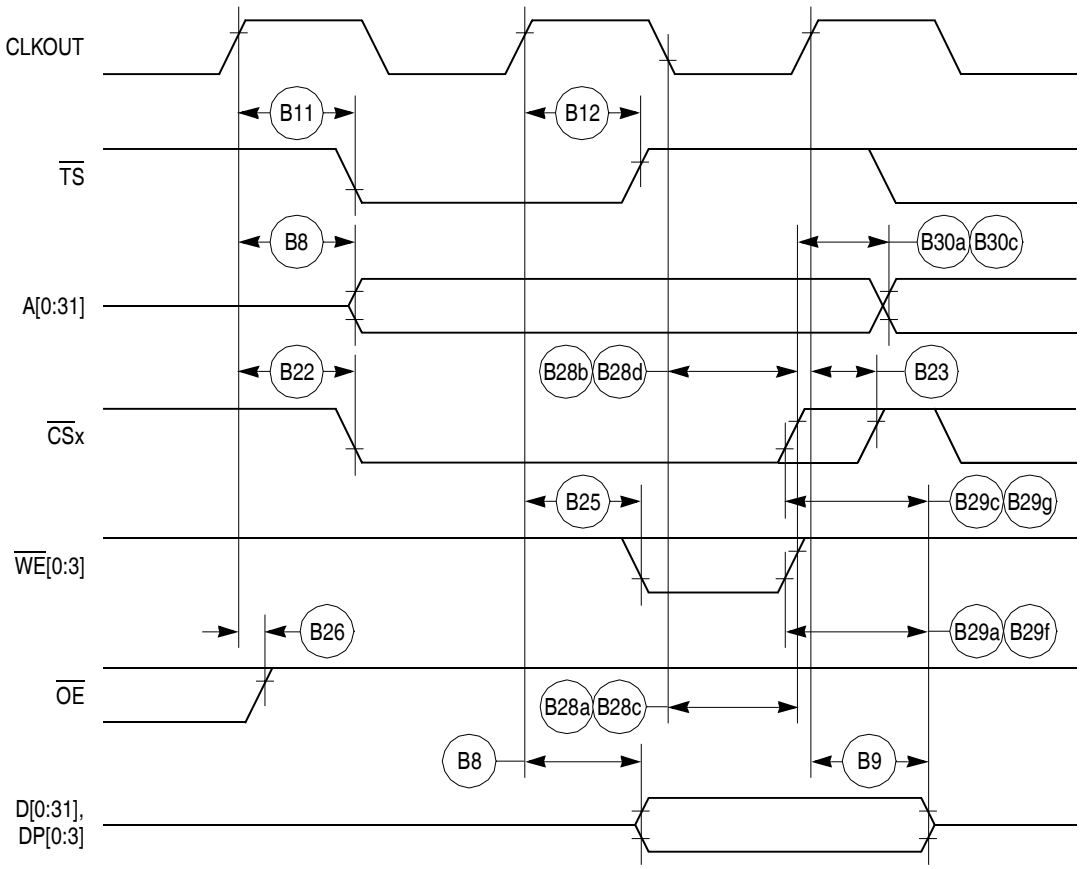



**Figure 17. External Bus Write Timing (GPCM Controlled—TRLX = 0, CSNT = 1)**

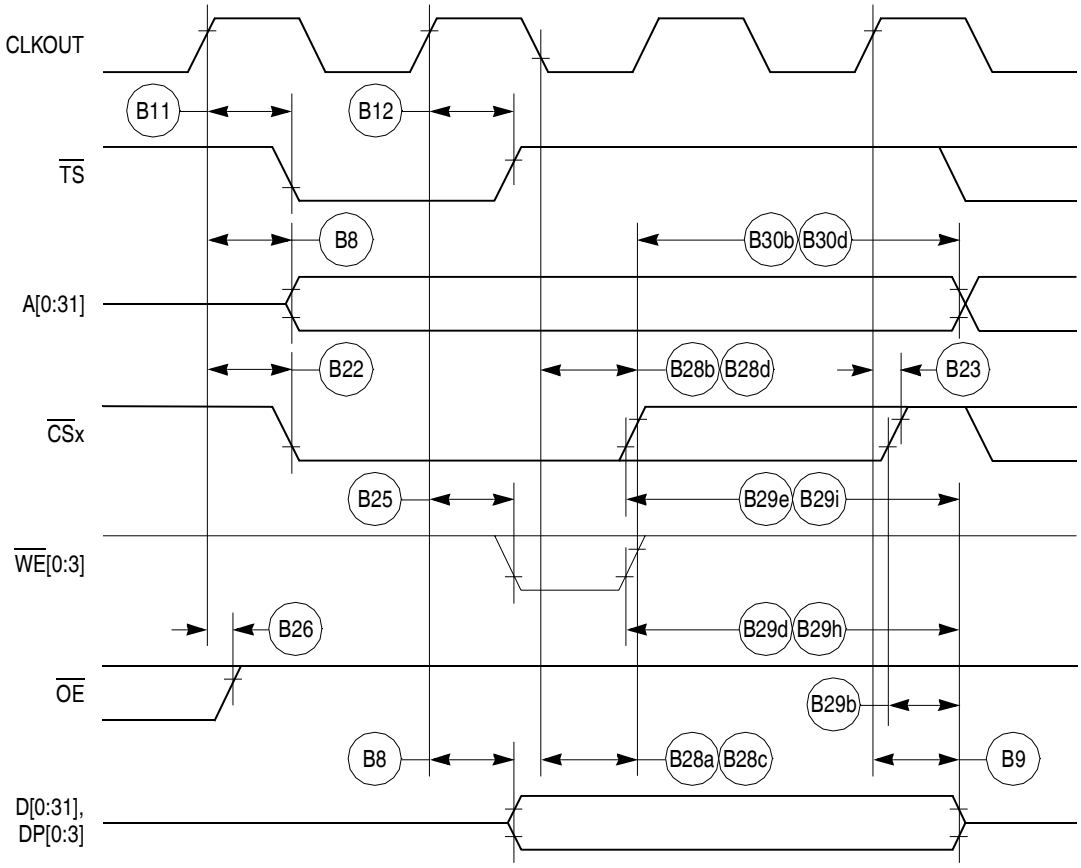



**Figure 18. External Bus Write Timing (GPCM Controlled—TRLX = 1, CSNT = 1)**

Figure 19 shows the timing for the external bus controlled by the UPM.

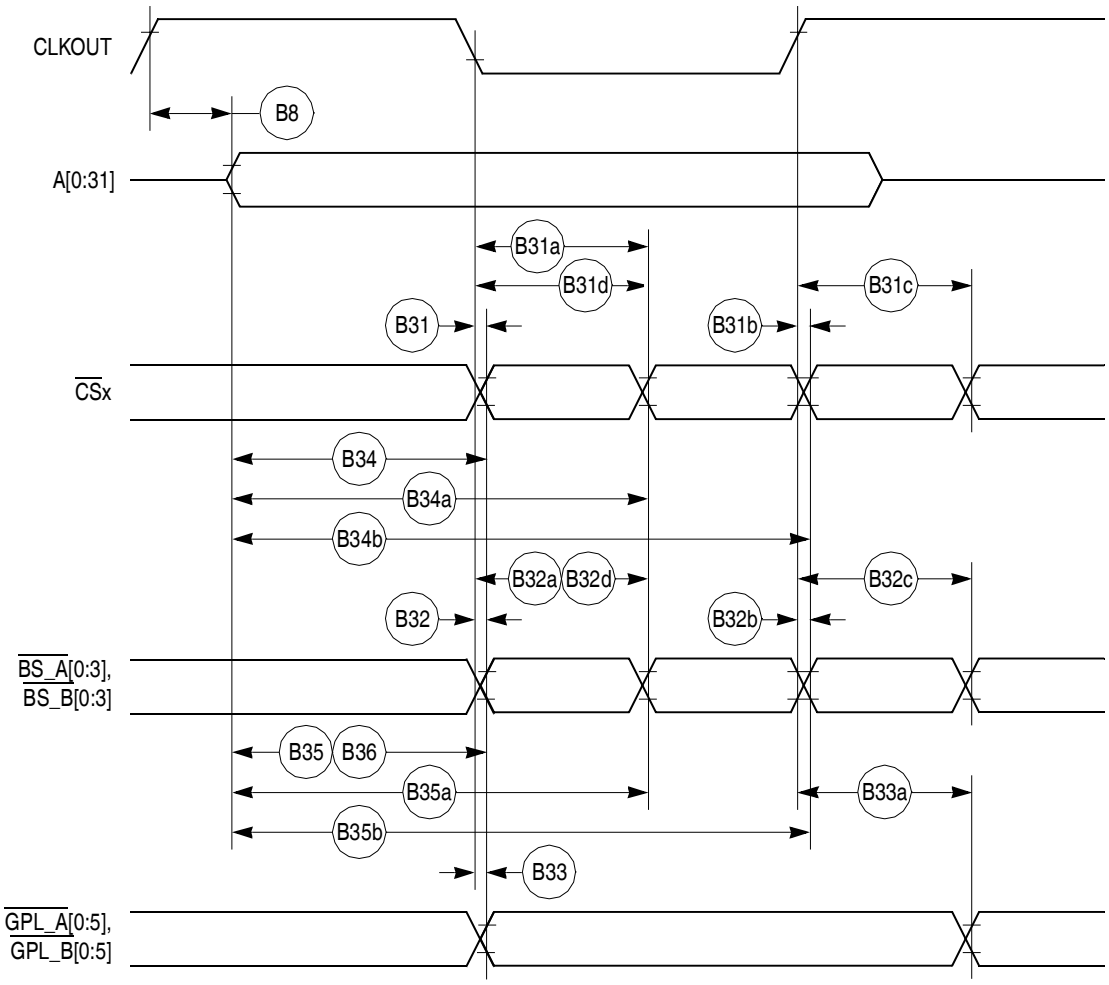



**Figure 19. External Bus Timing (UPM Controlled Signals)**

Figure 20 shows the timing for the asynchronous asserted UPWAIT signal controlled by the UPM.

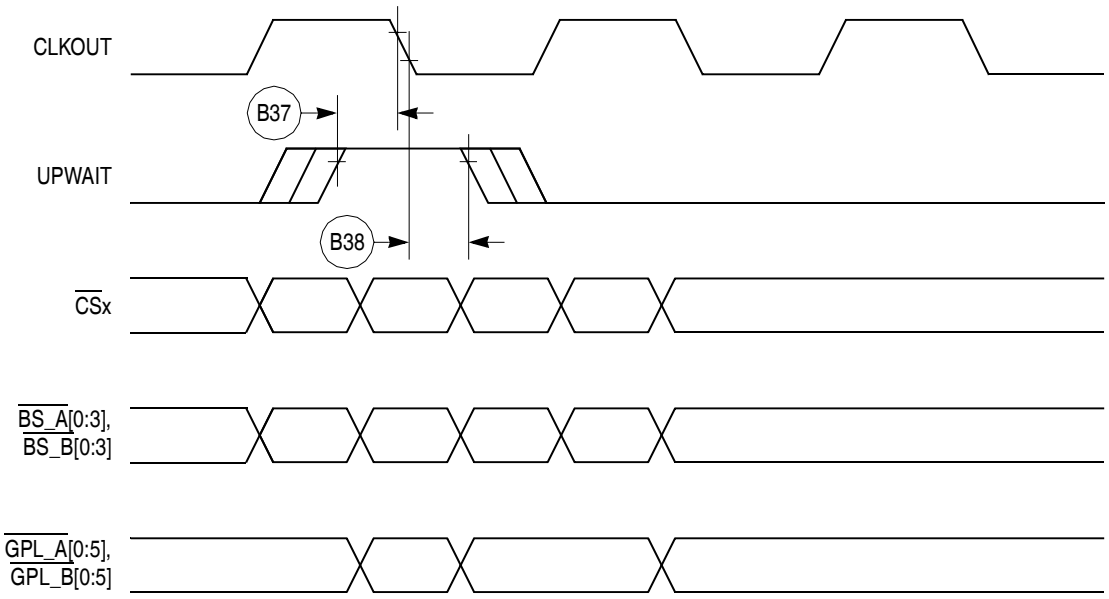



**Figure 20. Asynchronous UPWAIT Asserted Detection in UPM Handled Cycles Timing**

Figure 21 shows the timing for the asynchronous negated UPWAIT signal controlled by the UPM.

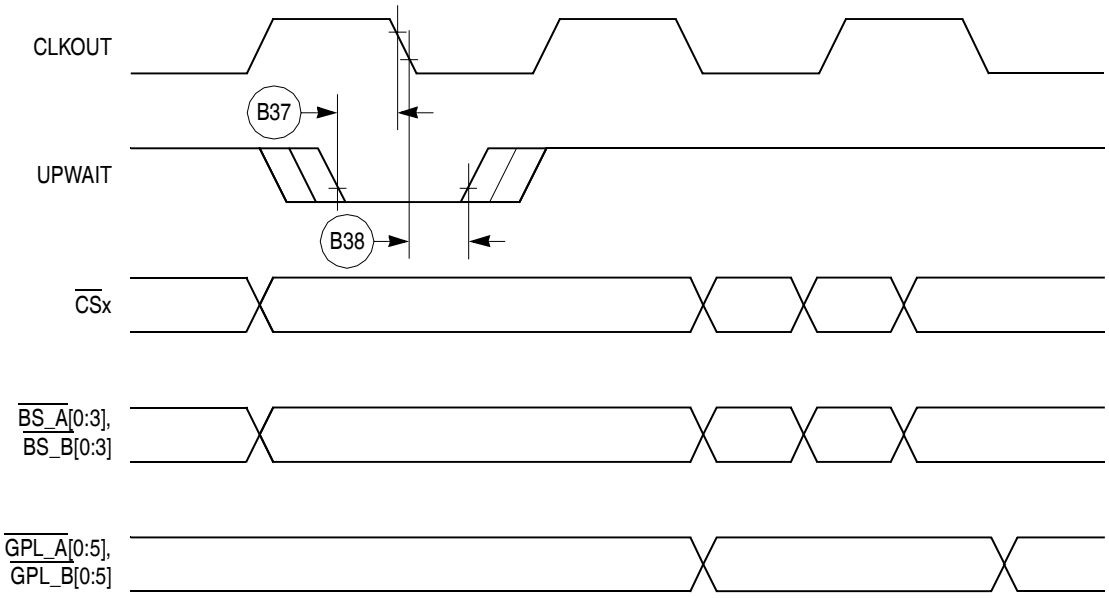



**Figure 21. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing**

Figure 22 shows the timing for the synchronous external master access controlled by the GPCM.

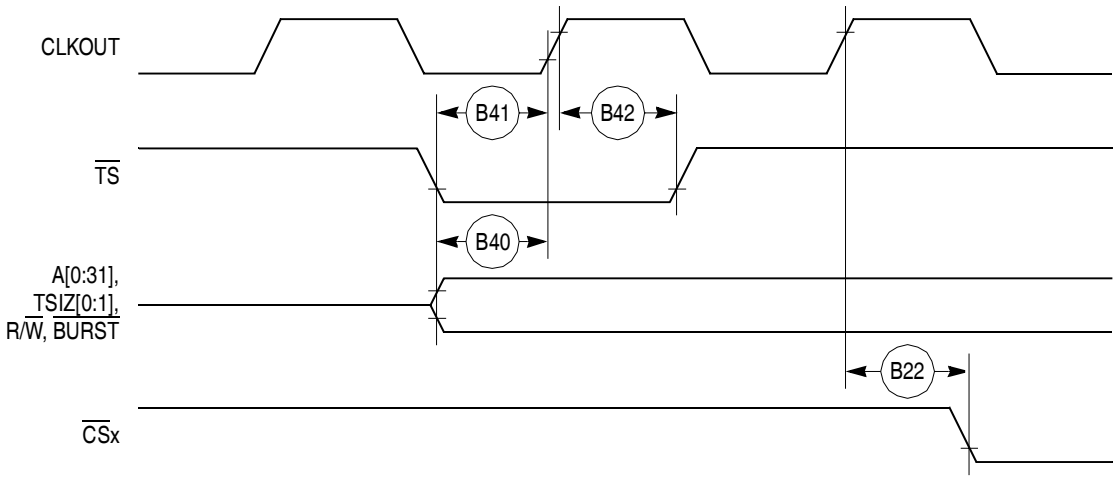



**Figure 22. Synchronous External Master Access Timing (GPCM Handled ACS = 00)**

Figure 23 shows the timing for the asynchronous external master memory access controlled by the GPCM.

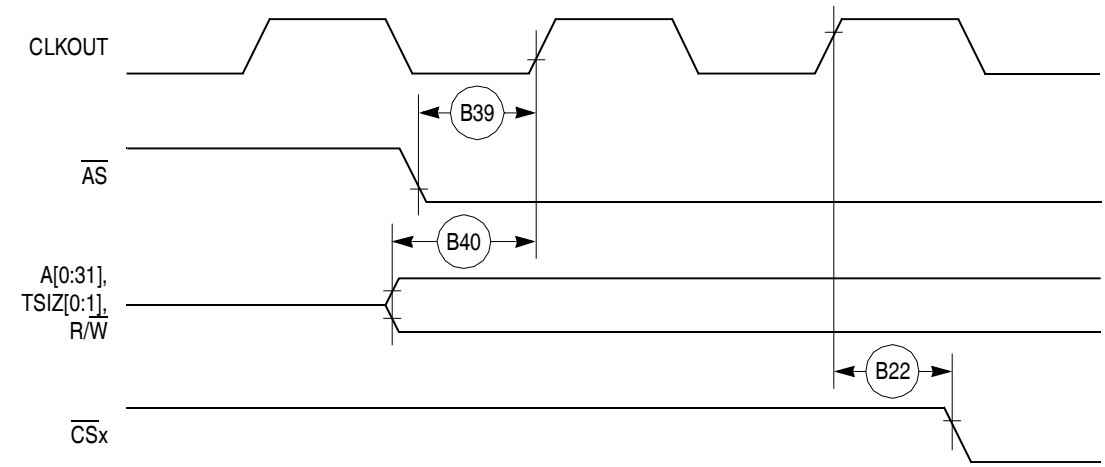



**Figure 23. Asynchronous External Master Memory Access Timing (GPCM Controlled—ACS = 00)**

Figure 24 shows the timing for the asynchronous external master control signals negation.

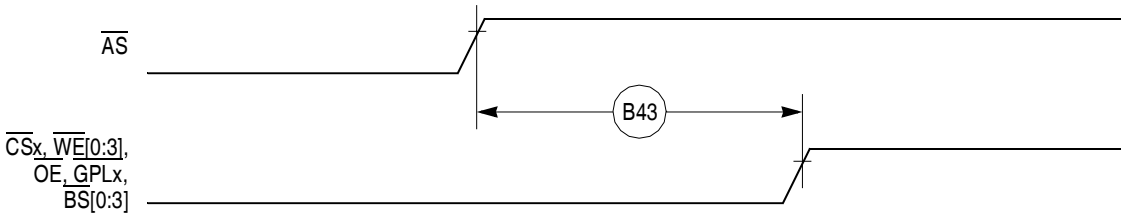



**Figure 24. Asynchronous External Master—Control Signals Negation Timing**

Table 10 shows the interrupt timing for the MPC866/859.

**Table 10. Interrupt Timing**

| Num | Characteristic [1] | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| I39 | $\overline{IRQ}$x valid to CLKOUT rising edge (setup time) | 6.00 | — | ns |
| I40 | $\overline{IRQ}$x hold time after CLKOUT | 2.00 | — | ns |
| I41 | $\overline{IRQ}$x pulse width low | 3.00 | — | ns |
| I42 | $\overline{IRQ}$x pulse width high | 3.00 | — | ns |
| I43 | $\overline{IRQ}$x edge-to-edge time | $4xT_{CLOCKOUT}$ | — | — |

[1] The timings I39 and I40 describe the testing conditions under which the $\overline{IRQ}$ lines are tested when being defined as level sensitive. The $\overline{IRQ}$ lines are synchronized internally and do not have to be asserted or negated with reference to the CLKOUT.
The timings I41, I42, and I43 are specified to allow the correct function of the $\overline{IRQ}$ lines detection circuitry, and has no direct relation with the total system interrupt latency that the MPC866/859 is able to support.

Figure 25 shows the interrupt detection timing for the external level-sensitive lines.

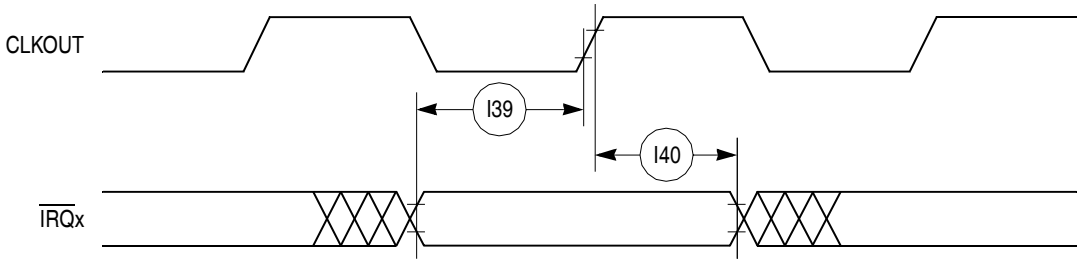



**Figure 25. Interrupt Detection Timing for External Level Sensitive Lines**

Figure 26 shows the interrupt detection timing for the external edge-sensitive lines.

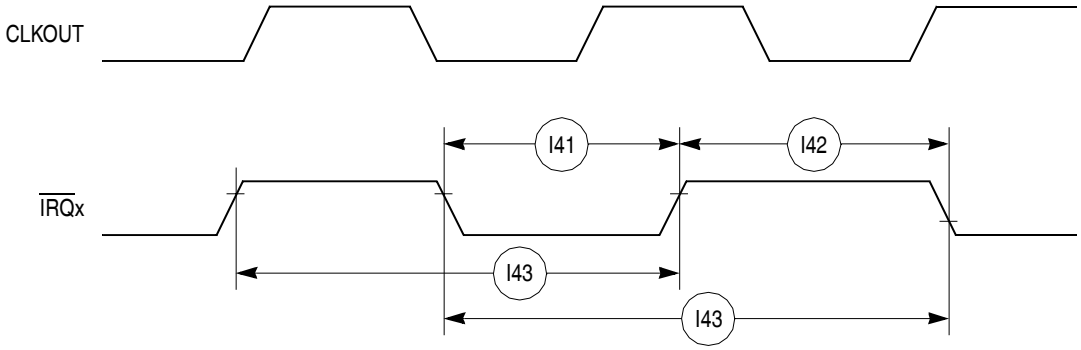



**Figure 26. Interrupt Detection Timing for External Edge Sensitive Lines**

Table 11 shows the PCMCIA timing for the MPC866/859.

**Table 11. PCMCIA Timing**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| P44 | A(0:31), $\overline{REG}$ valid to PCMCIA Strobe asserted [1] (MIN = 0.75 x B1 – 2.00) | 20.70 | — | 16.70 | — | 13.00 | — | 9.40 | — | ns |
| P45 | A(0:31), $\overline{REG}$ valid to ALE negation [1] (MIN = 1.00 x B1 – 2.00) | 28.30 | — | 23.00 | — | 18.00 | — | 13.20 | — | ns |
| P46 | CLKOUT to $\overline{REG}$ valid (MAX = 0.25 x B1 + 8.00) | 7.60 | 15.60 | 6.30 | 14.30 | 5.00 | 13.00 | 3.80 | 11.80 | ns |
| P47 | CLKOUT to $\overline{REG}$ invalid (MIN = 0.25 x B1 + 1.00) | 8.60 | — | 7.30 | — | 6.00 | — | 4.80 | — | ns |
| P48 | CLKOUT to $\overline{CE1}$, $\overline{CE2}$ asserted (MAX = 0.25 x B1 + 8.00) | 7.60 | 15.60 | 6.30 | 14.30 | 5.00 | 13.00 | 3.80 | 11.80 | ns |
| P49 | CLKOUT to $\overline{CE1}$, $\overline{CE2}$ negated (MAX = 0.25 x B1 + 8.00) | 7.60 | 15.60 | 6.30 | 14.30 | 5.00 | 13.00 | 3.80 | 11.80 | ns |

**Table 11. PCMCIA Timing (continued)**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| P50 | CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ assert time (MAX = 0.00 x B1 + 11.00) | — | 11.00 | — | 11.00 | — | 11.00 | — | 11.00 | ns |
| P51 | CLKOUT to $\overline{\text{PCOE}}$, $\overline{\text{IORD}}$, $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negate time (MAX = 0.00 x B1 + 11.00) | 2.00 | 11.00 | 2.00 | 11.00 | 2.00 | 11.00 | 2.00 | 11.00 | ns |
| P52 | CLKOUT to ALE assert time (MAX = 0.25 x B1 + 6.30) | 7.60 | 13.80 | 6.30 | 12.50 | 5.00 | 11.30 | 3.80 | 10.00 | ns |
| P53 | CLKOUT to ALE negate time (MAX = 0.25 x B1 + 8.00) | — | 15.60 | — | 14.30 | — | 13.00 | — | 11.80 | ns |
| P54 | $\overline{\text{PCWE}}$, $\overline{\text{IOWR}}$ negated to D(0:31) invalid[1] (MIN = 0.25 x B1 – 2.00) | 5.60 | — | 4.30 | — | 3.00 | — | 1.80 | — | ns |
| P55 | $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ valid to CLKOUT rising edge[1] (MIN = 0.00 x B1 + 8.00) | 8.00 | — | 8.00 | — | 8.00 | — | 8.00 | — | ns |
| P56 | CLKOUT rising edge to $\overline{\text{WAITA}}$ and $\overline{\text{WAITB}}$ invalid[1] (MIN = 0.00 x B1 + 2.00) | 2.00 | — | 2.00 | — | 2.00 | — | 2.00 | — | ns |

1 PSST = 1. Otherwise, add PSST times cycle time.
PSHT = 0. Otherwise, add PSHT times cycle time.
These synchronous timings define when the $\overline{\text{WAITx}}$ signals are detected in order to freeze (or relieve) the PCMCIA current cycle. The $\overline{\text{WAITx}}$ assertion will be effective only if it is detected 2 cycles before the PSL timer expiration. See PCMCIA Interface in the *MPC866 PowerQUICC User's Manual*.

Figure 27 shows the PCMCIA access cycle timing for the external bus read.

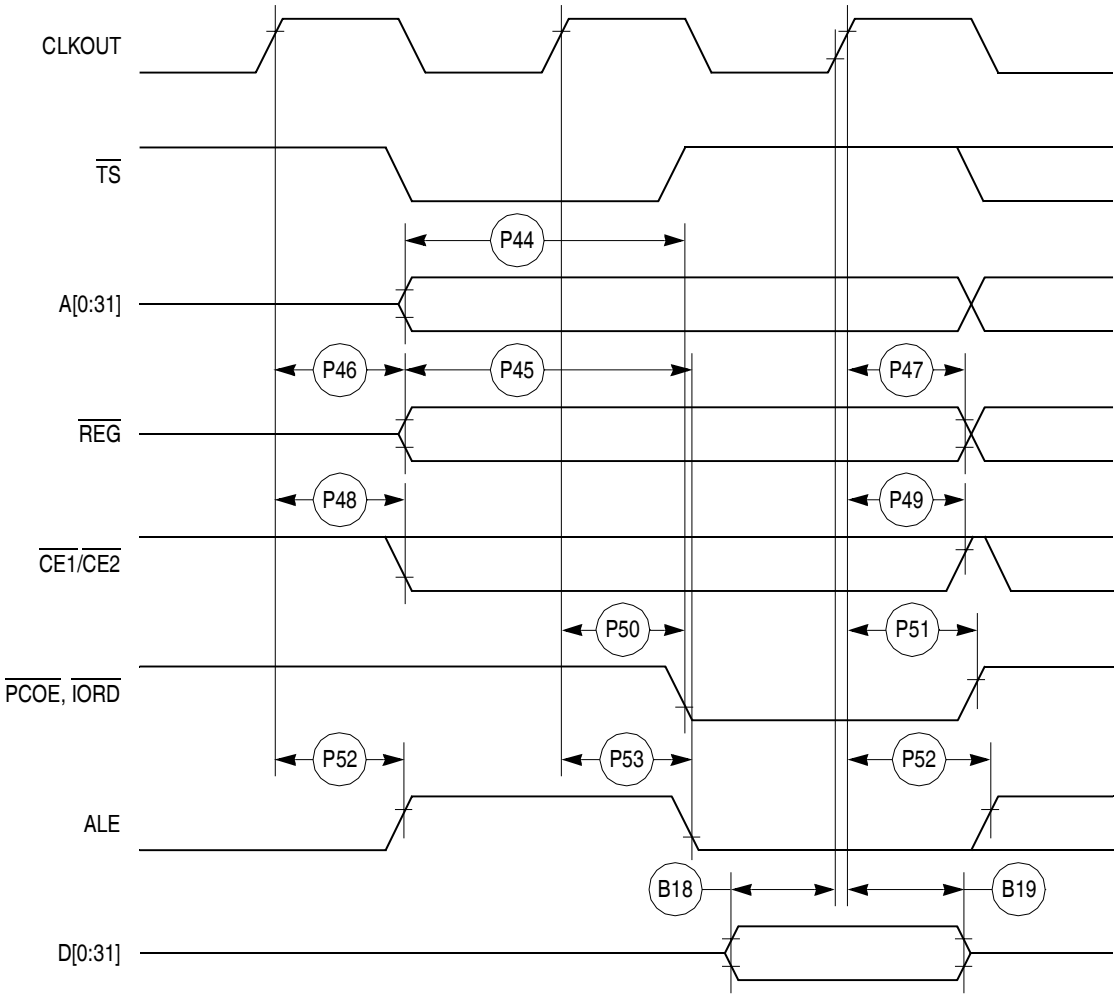



**Figure 27. PCMCIA Access Cycles Timing External Bus Read**

Figure 28 shows the PCMCIA access cycle timing for the external bus write.

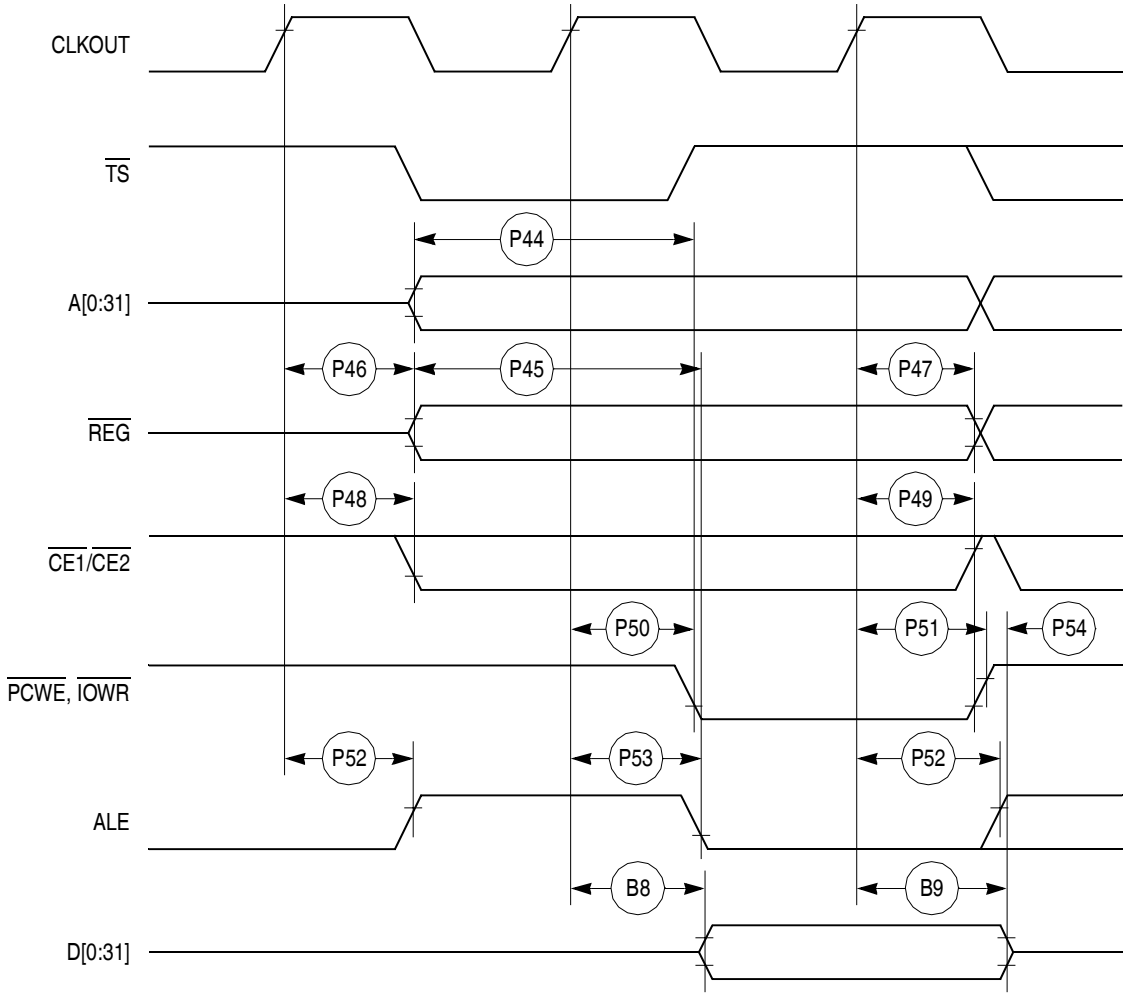



**Figure 28. PCMCIA Access Cycles Timing External Bus Write**

Figure 29 shows the PCMCIA WAIT signals detection timing.

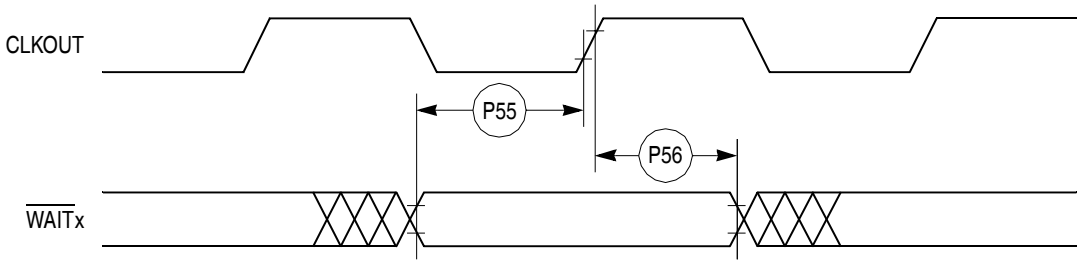



**Figure 29. PCMCIA WAIT Signals Detection Timing**

Table 12 shows the PCMCIA port timing for the MPC866/859.

**Table 12. PCMCIA Port Timing**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| P57 | CLKOUT to OPx, valid (MAX = 0.00 x B1 + 19.00) | — | 19.00 | — | 19.00 | — | 19.00 | — | 19.00 | ns |
| P58 | $\overline{\text{HRESET}}$ negated to OPx drive [1](MIN = 0.75 x B1 + 3.00) | 25.70 | — | 21.70 | — | 18.00 | — | 14.40 | — | ns |
| P59 | IP_Xx valid to CLKOUT rising edge (MIN = 0.00 x B1 + 5.00) | 5.00 | — | 5.00 | — | 5.00 | — | 5.00 | — | ns |
| P60 | CLKOUT rising edge to IP_Xx invalid (MIN = 0.00 x B1 + 1.00) | 1.00 | — | 1.00 | — | 1.00 | — | 1.00 | — | ns |

1 OP2 and OP3 only.

Figure 30 shows the PCMCIA output port timing for the MPC866/859.

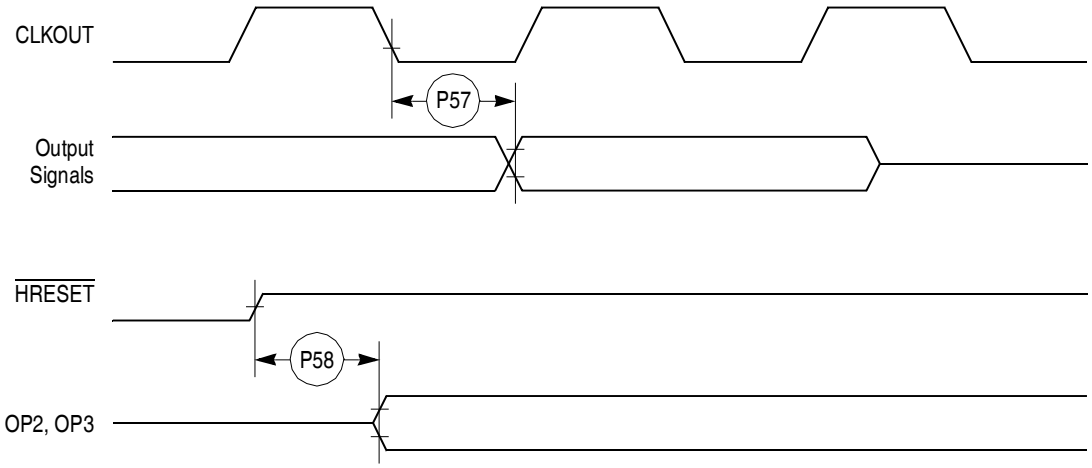



**Figure 30. PCMCIA Output Port Timing**

Figure 31 shows the PCMCIA output port timing for the MPC866/859.

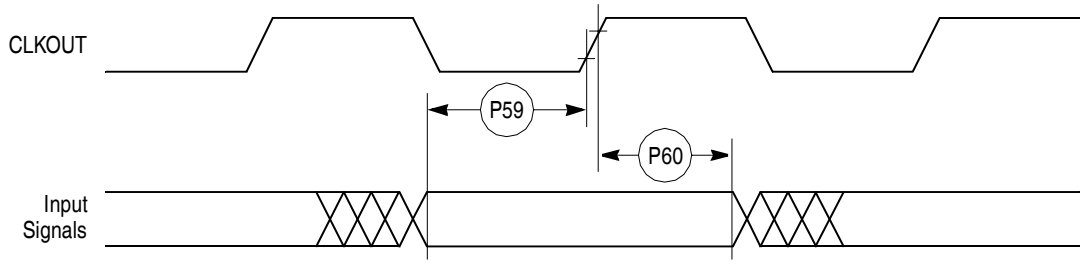



**Figure 31. PCMCIA Input Port Timing**

Table 13 shows the debug port timing for the MPC866/859.

**Table 13. Debug Port Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| D61 | DSCK cycle time | $3xT_{CLOCKOUT}$ | — | |
| D62 | DSCK clock pulse width | $1.25xT_{CLOCKOUT}$ | — | |
| D63 | DSCK rise and fall times | 0.00 | 3.00 | ns |
| D64 | DSDI input data setup time | 8.00 | — | ns |
| D65 | DSDI data hold time | 5.00 | — | ns |
| D66 | DSCK low to DSDO data valid | 0.00 | 15.00 | ns |
| D67 | DSCK low to DSDO invalid | 0.00 | 2.00 | ns |

Figure 32 shows the input timing for the debug port clock.

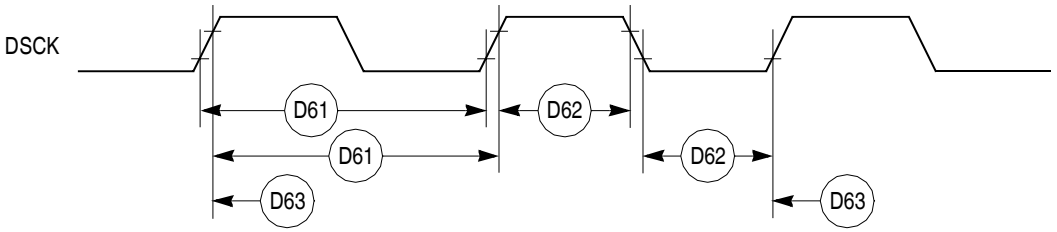



**Figure 32. Debug Port Clock Input Timing**

Figure 33 shows the timing for the debug port.

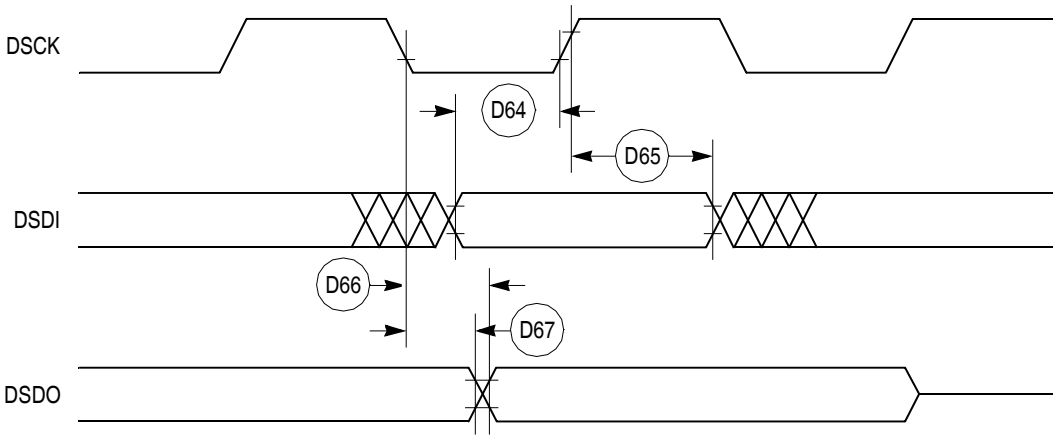



**Figure 33. Debug Port Timings**

Table 14 shows the reset timing for the MPC866/859.

**Table 14. Reset Timing**

| Num | Characteristic | 33 MHz | | 40 MHz | | 50 MHz | | 66 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| R69 | CLKOUT to $\overline{\text{HRESET}}$ high impedance (MAX = 0.00 x B1 + 20.00) | — | 20.00 | — | 20.00 | — | 20.00 | — | 20.00 | ns |
| R70 | CLKOUT to $\overline{\text{SRESET}}$ high impedance (MAX = 0.00 x B1 + 20.00) | — | 20.00 | — | 20.00 | — | 20.00 | — | 20.00 | ns |
| R71 | $\overline{\text{RSTCONF}}$ pulse width (MIN = 17.00 x B1) | 515.20 | — | 425.00 | — | 340.00 | — | 257.60 | — | ns |
| R72 | — | — | — | — | — | — | — | — | — | — |
| R73 | Configuration data to HRESET rising edge setup time (MIN = 15.00 x B1 + 50.00) | 504.50 | — | 425.00 | — | 350.00 | — | 277.30 | — | ns |
| R74 | Configuration data to $\overline{\text{RSTCONF}}$ rising edge setup time (MIN = 0.00 x B1 + 350.00) | 350.00 | — | 350.00 | — | 350.00 | — | 350.00 | — | ns |
| R75 | Configuration data hold time after $\overline{\text{RSTCONF}}$ negation (MIN = 0.00 x B1 + 0.00) | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| R76 | Configuration data hold time after $\overline{\text{HRESET}}$ negation (MIN = 0.00 x B1 + 0.00) | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| R77 | $\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$ asserted to data out drive (MAX = 0.00 x B1 + 25.00) | — | 25.00 | — | 25.00 | — | 25.00 | — | 25.00 | ns |
| R78 | $\overline{\text{RSTCONF}}$ negated to data out high impedance (MAX = 0.00 x B1 + 25.00) | — | 25.00 | — | 25.00 | — | 25.00 | — | 25.00 | ns |
| R79 | CLKOUT of last rising edge before chip three-states $\overline{\text{HRESET}}$ to data out high impedance (MAX = 0.00 x B1 + 25.00) | — | 25.00 | — | 25.00 | — | 25.00 | — | 25.00 | ns |
| R80 | DSDI, DSCK setup (MIN = 3.00 x B1) | 90.90 | — | 75.00 | — | 60.00 | — | 45.50 | — | ns |
| R81 | DSDI, DSCK hold time (MIN = 0.00 x B1 + 0.00) | 0.00 | — | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| R82 | $\overline{\text{SRESET}}$ negated to CLKOUT rising edge for DSDI and DSCK sample (MIN = 8.00 x B1) | 242.40 | — | 200.00 | — | 160.00 | — | 121.20 | — | ns |

Figure 34 shows the reset timing for the data bus configuration.

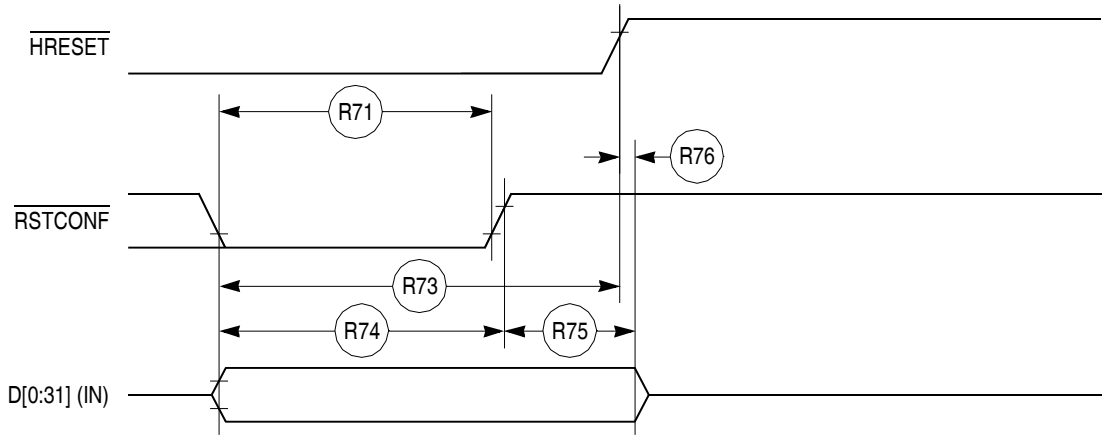



**Figure 34. Reset Timing—Configuration from Data Bus**

Figure 35 shows the reset timing for the data bus weak drive during configuration.

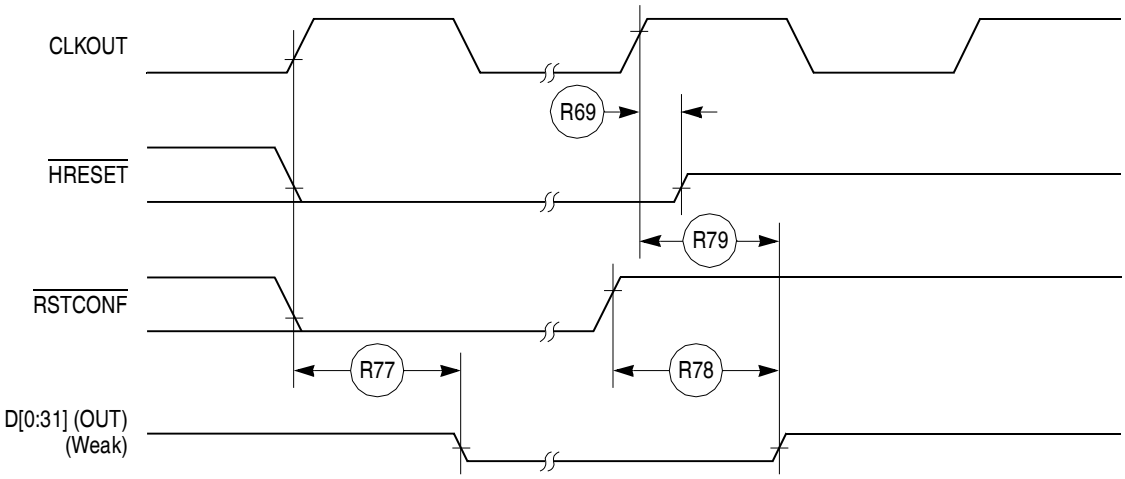



**Figure 35. Reset Timing—Data Bus Weak Drive During Configuration**

Figure 36 shows the reset timing for the debug port configuration.

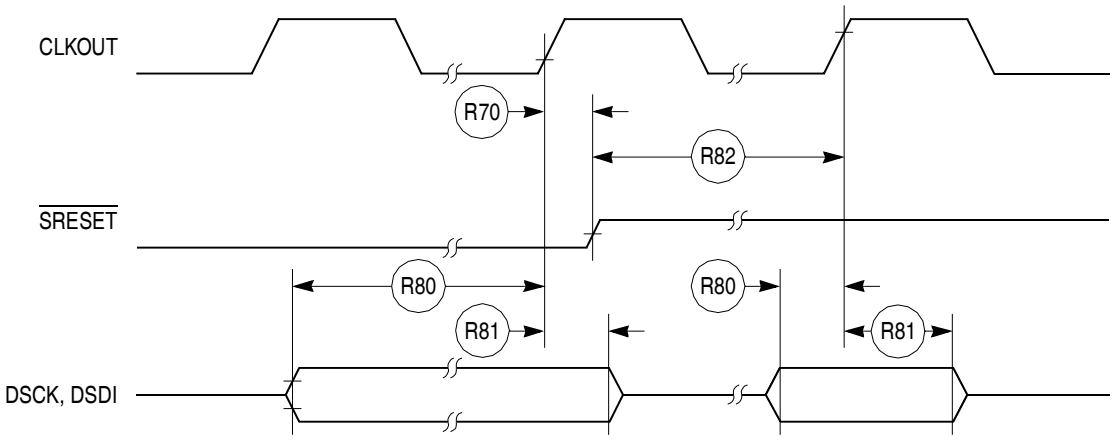



**Figure 36. Reset Timing—Debug Port Configuration**

# 11 IEEE 1149.1 Electrical Specifications

Table 15 shows the JTAG timings for the MPC866/859 shown in Figure 37 through Figure 40.

**Table 15. JTAG Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| J82 | TCK cycle time | 100.00 | — | ns |
| J83 | TCK clock pulse width measured at 1.5 V | 40.00 | — | ns |
| J84 | TCK rise and fall times | 0.00 | 10.00 | ns |
| J85 | TMS, TDI data setup time | 5.00 | — | ns |
| J86 | TMS, TDI data hold time | 25.00 | — | ns |
| J87 | TCK low to TDO data valid | — | 27.00 | ns |
| J88 | TCK low to TDO data invalid | 0.00 | — | ns |
| J89 | TCK low to TDO high impedance | — | 20.00 | ns |
| J90 | $\overline{\text{TRST}}$ assert time | 100.00 | — | ns |
| J91 | $\overline{\text{TRST}}$ setup time to TCK low | 40.00 | — | ns |
| J92 | TCK falling edge to output valid | — | 50.00 | ns |
| J93 | TCK falling edge to output valid out of high impedance | — | 50.00 | ns |
| J94 | TCK falling edge to output high impedance | — | 50.00 | ns |
| J95 | Boundary scan input valid to TCK rising edge | 50.00 | — | ns |
| J96 | TCK rising edge to boundary scan input invalid | 50.00 | — | ns |

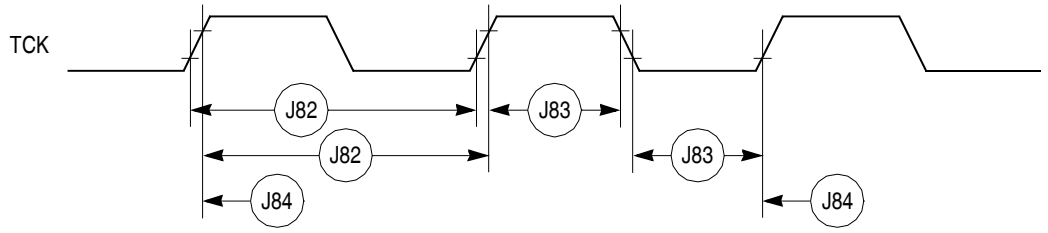



**Figure 37. JTAG Test Clock Input Timing**

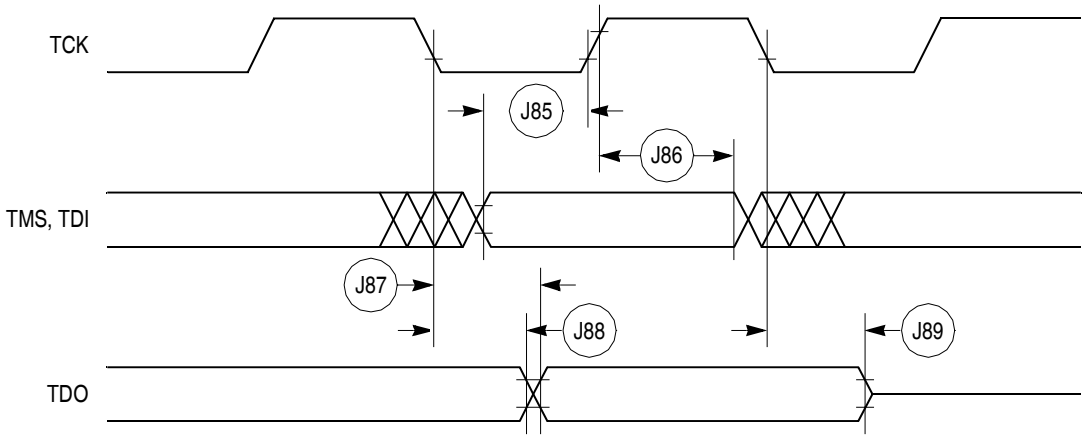



**Figure 38. JTAG Test Access Port Timing Diagram**

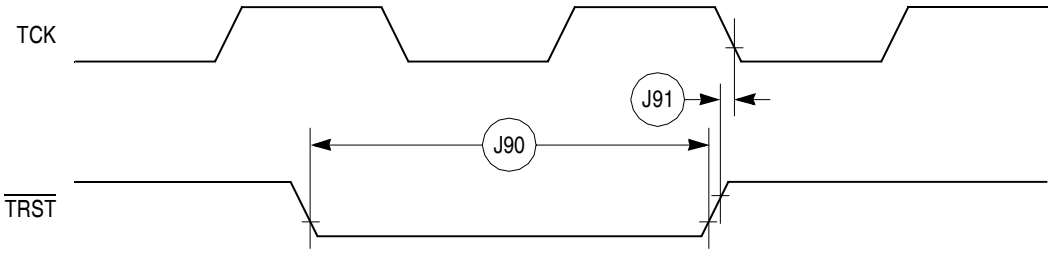



**Figure 39. JTAG $\overline{\text{TRST}}$ Timing Diagram**

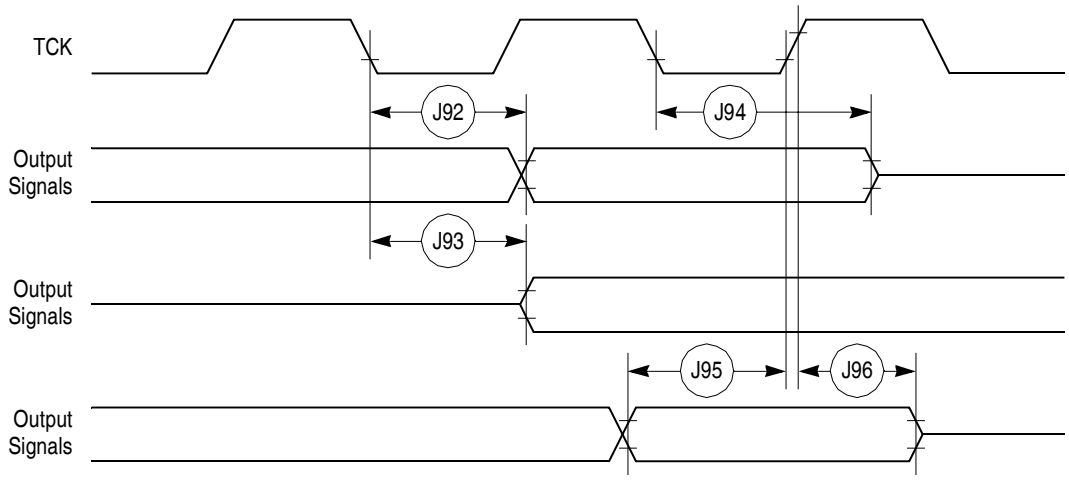



**Figure 40. Boundary Scan (JTAG) Timing Diagram**

# 12 CPM Electrical Characteristics

This section provides the AC and DC electrical specifications for the communications processor module (CPM) of the MPC866/859.

## 12.1 PIP/PIO AC Electrical Specifications

Table 16 shows the PIP/PIO AC timings as shown in Figure 41 through Figure 45.

**Table 16. PIP/PIO Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 21 | Data-in setup time to STBI low | 0 | — | ns |
| 22 | Data-In hold time to STBI high | 2.5 – t3 [1] | — | clk |
| 23 | STBI pulse width | 1.5 | — | clk |
| 24 | STBO pulse width | 1 clk – 5ns | — | ns |
| 25 | Data-out setup time to STBO low | 2 | — | clk |
| 26 | Data-out hold time from STBO high | 5 | — | clk |
| 27 | STBI low to STBO low (Rx interlock) | — | 2 | clk |
| 28 | STBI low to STBO high (Tx interlock) | 2 | — | clk |
| 29 | Data-in setup time to clock high | 15 | — | ns |
| 30 | Data-in hold time from clock high | 7.5 | — | ns |
| 31 | Clock low to data-out valid (CPU writes data, control, or direction) | — | 25 | ns |

1 t3 = Specification 23

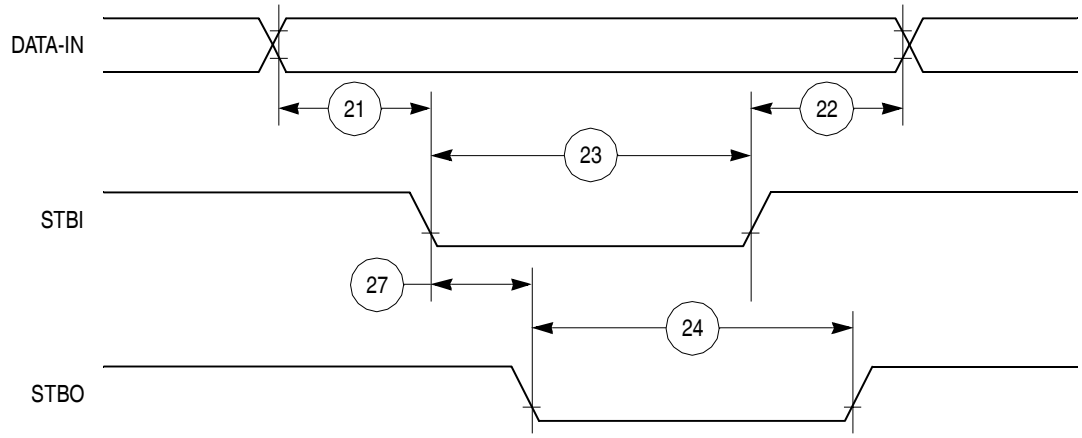



**Figure 41. PIP Rx (Interlock Mode) Timing Diagram**

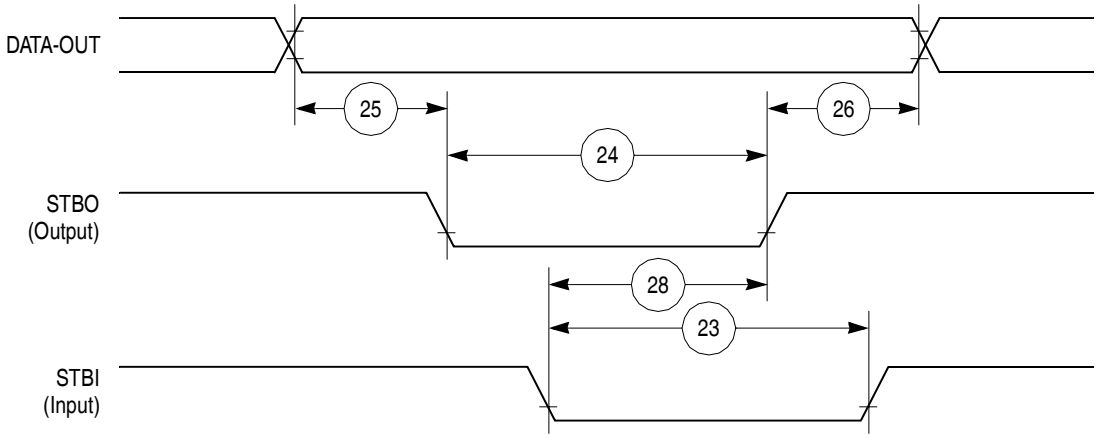



**Figure 42. PIP Tx (Interlock Mode) Timing Diagram**

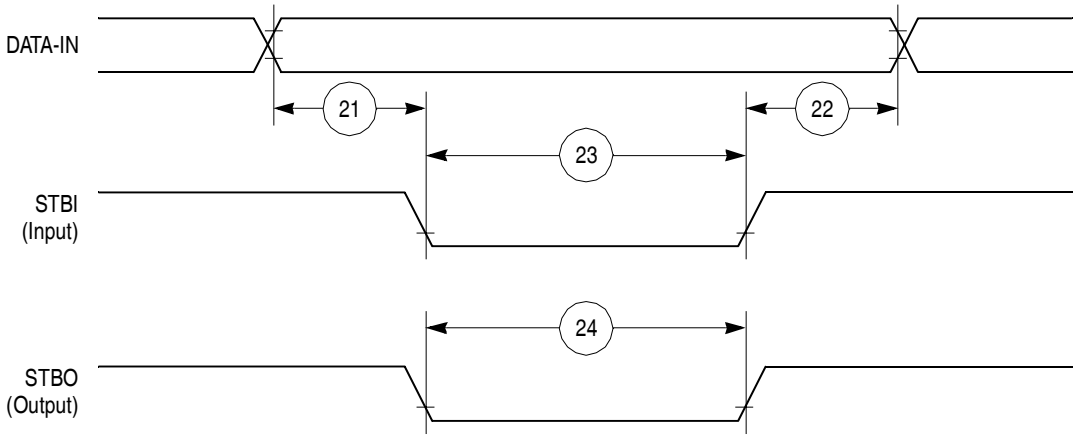



**Figure 43. PIP Rx (Pulse Mode) Timing Diagram**

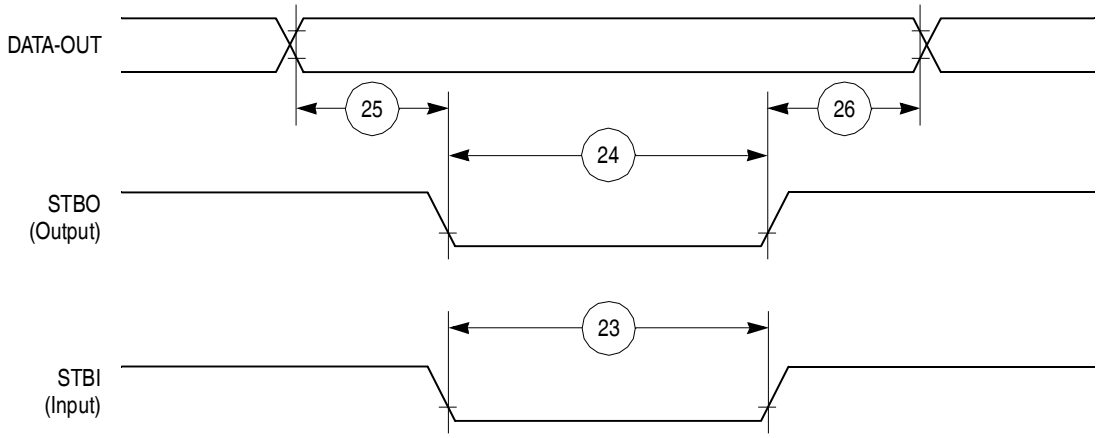



**Figure 44. PIP TX (Pulse Mode) Timing Diagram**

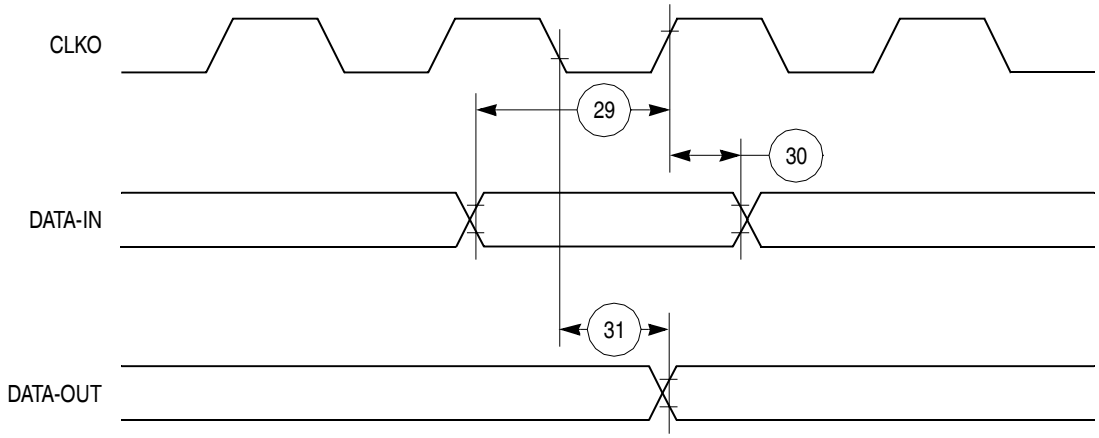



**Figure 45. Parallel I/O Data-In/Data-Out Timing Diagram**

## 12.2 Port C Interrupt AC Electrical Specifications

Table 17 shows timings for port C interrupts.

**Table 17. Port C Interrupt Timing**

| Num | Characteristic | 33.34 MHz | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 35 | Port C interrupt pulse width low (edge-triggered mode) | 55 | — | ns |
| 36 | Port C interrupt minimum time between active edges | 55 | — | ns |

Figure 46 shows the port C interrupt detection timing.

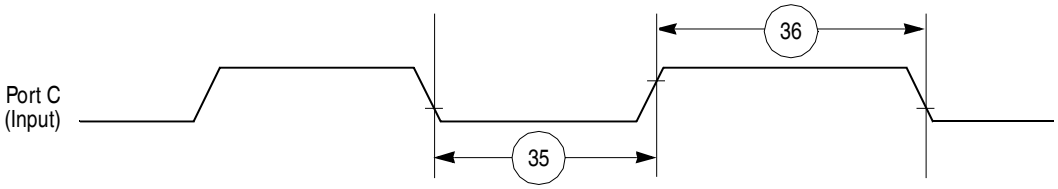



**Figure 46. Port C Interrupt Detection Timing**

## 12.3 IDMA Controller AC Electrical Specifications

Table 18 shows the IDMA controller timings as shown in Figure 47 through Figure 50.

**Table 18. IDMA Controller Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 40 | $\overline{\text{DREQ}}$ setup time to clock high | 7 | — | ns |
| 41 | $\overline{\text{DREQ}}$ hold time from clock high | 3 | — | ns |
| 42 | $\overline{\text{SDACK}}$ assertion delay from clock high | — | 12 | ns |
| 43 | $\overline{\text{SDACK}}$ negation delay from clock low | — | 12 | ns |
| 44 | $\overline{\text{SDACK}}$ negation delay from $\overline{\text{TA}}$ low | — | 20 | ns |
| 45 | $\overline{\text{SDACK}}$ negation delay from clock high | — | 15 | ns |
| 46 | $\overline{\text{TA}}$ assertion to falling edge of the clock setup time (applies to external $\overline{\text{TA}}$) | 7 | — | ns |

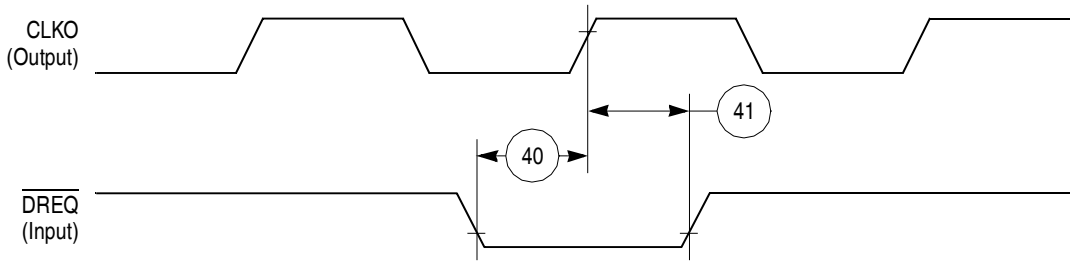



**Figure 47. IDMA External Requests Timing Diagram**

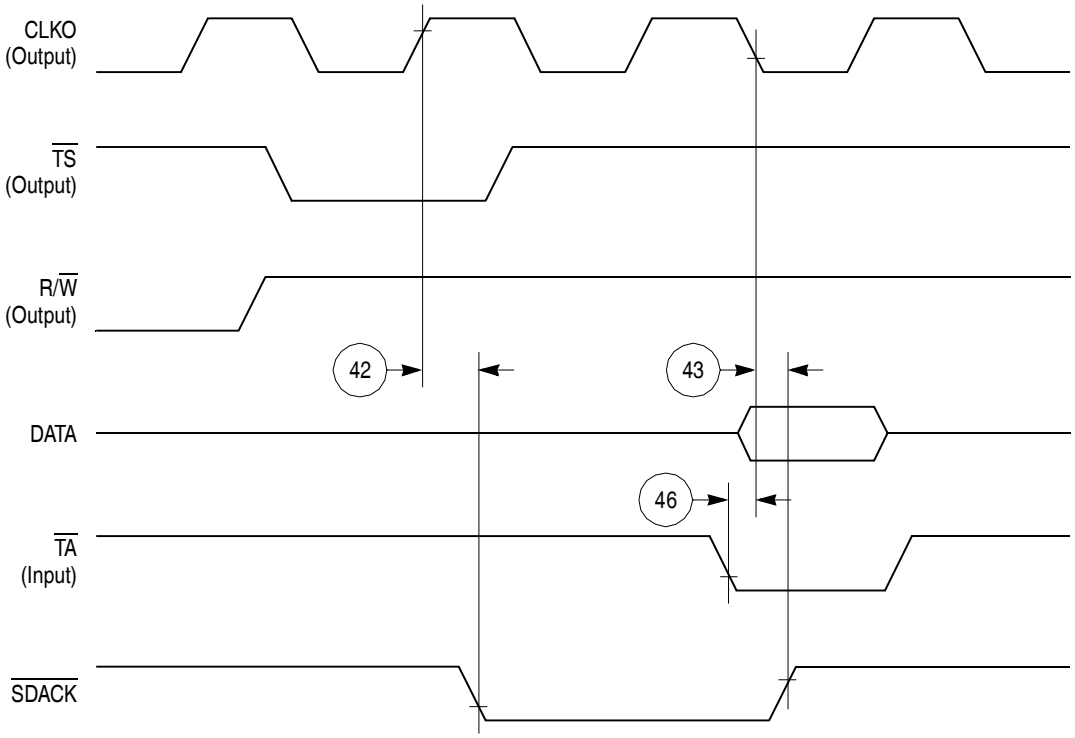



**Figure 48. SDACK Timing Diagram—Peripheral Write, Externally-Generated TA**

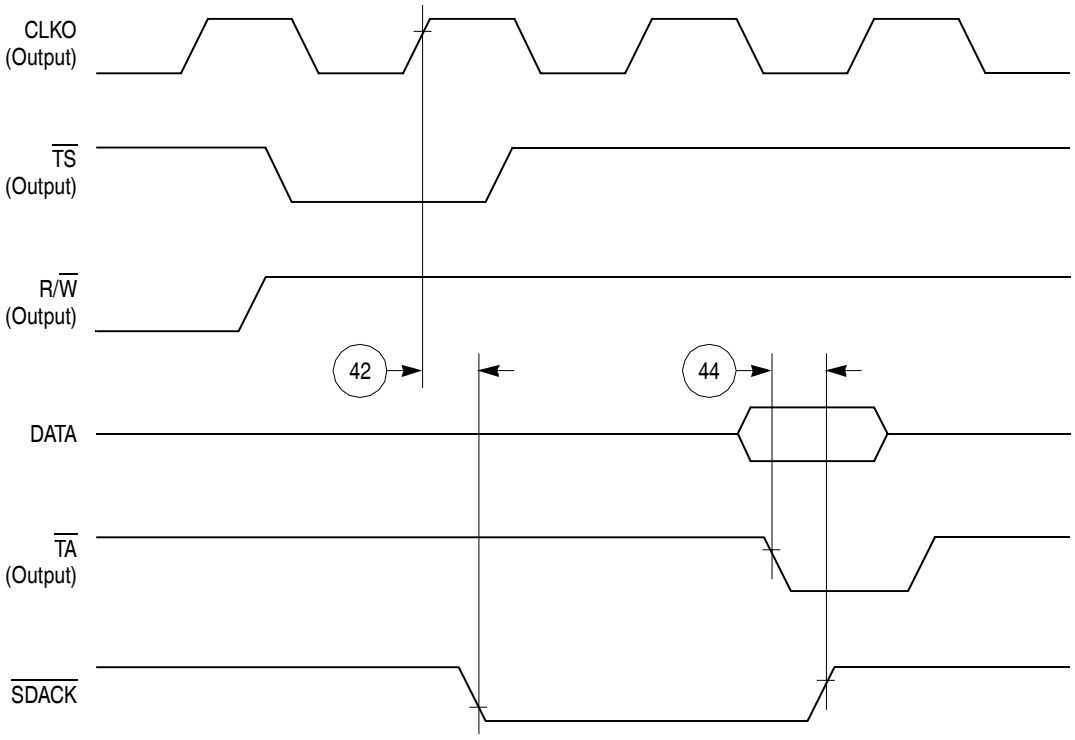



**Figure 49. SDACK Timing Diagram—Peripheral Write, Internally-Generated TA**

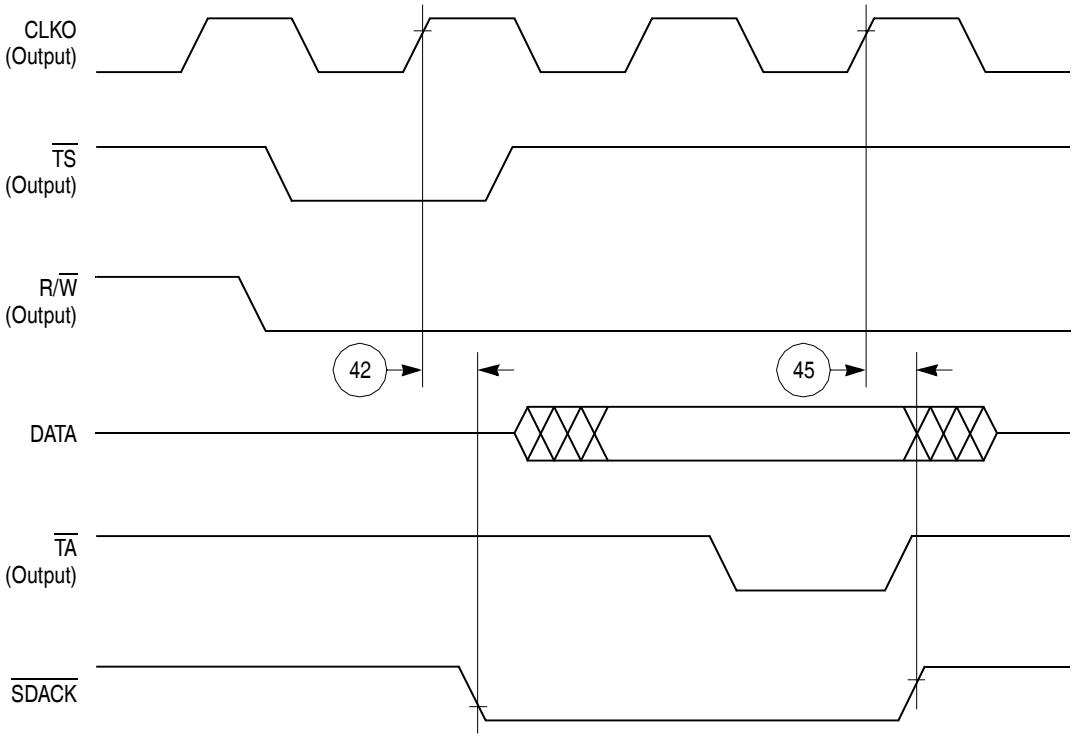



**Figure 50. SDACK Timing Diagram—Peripheral Read, Internally-Generated TA**

## 12.4 Baud Rate Generator AC Electrical Specifications

Table 19 shows the baud rate generator timings as shown in Figure 51.

**Table 19. Baud Rate Generator Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 50 | BRGO rise and fall time | — | 10 | ns |
| 51 | BRGO duty cycle | 40 | 60 | % |
| 52 | BRGO cycle | 40 | — | ns |

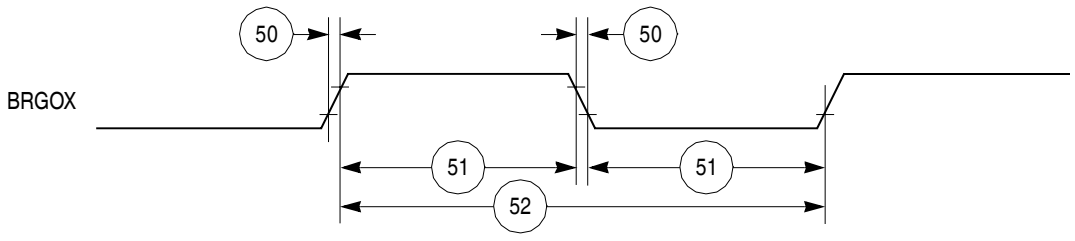



**Figure 51. Baud Rate Generator Timing Diagram**

## 12.5 Timer AC Electrical Specifications

Table 20 shows the general-purpose timer timings as shown in Figure 52.

**Table 20. Timer Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 61 | TIN/$\overline{\text{TGATE}}$ rise and fall time | 10 | — | ns |
| 62 | TIN/$\overline{\text{TGATE}}$ low time | 1 | — | clk |
| 63 | TIN/$\overline{\text{TGATE}}$ high time | 2 | — | clk |
| 64 | TIN/$\overline{\text{TGATE}}$ cycle time | 3 | — | clk |
| 65 | CLKO low to $\overline{\text{TOUT}}$ valid | 3 | 25 | ns |

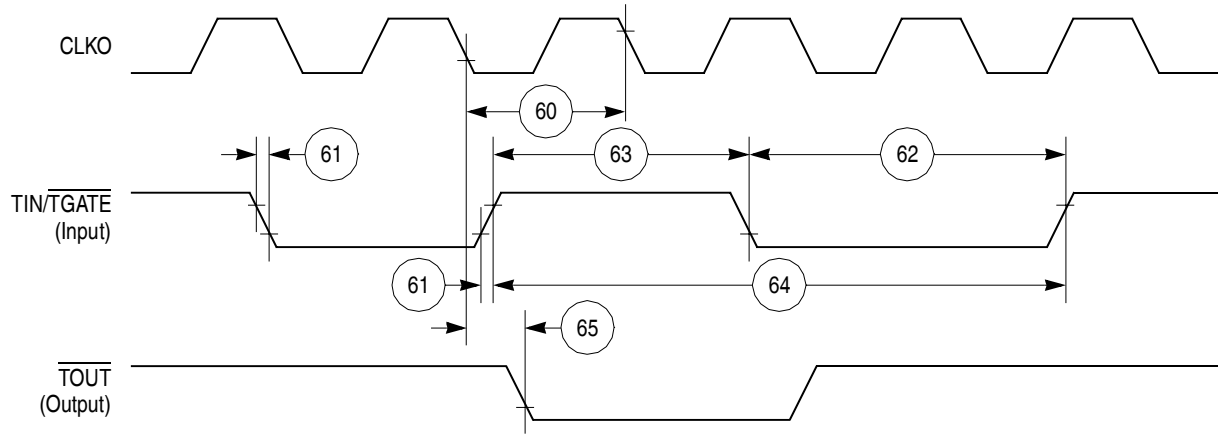



**Figure 52. CPM General-Purpose Timers Timing Diagram**

## 12.6 Serial Interface AC Electrical Specifications

Table 21 shows the serial interface timings as shown in Figure 53 through Figure 57.

**Table 21. SI Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 70 | L1RCLK, L1TCLK frequency (DSC = 0) [1, 2] | — | SYNCCLK/2.5 | MHz |
| 71 | L1RCLK, L1TCLK width low (DSC = 0) [2] | P + 10 | — | ns |
| 71a | L1RCLK, L1TCLK width high (DSC = 0) [3] | P + 10 | — | ns |
| 72 | L1TXD, L1ST(1–4), $\overline{\text{L1RQ}}$, L1CLKO rise/fall time | — | 15.00 | ns |
| 73 | L1RSYNC, L1TSYNC valid to L1CLK edge (SYNC setup time) | 20.00 | — | ns |

**Table 21. SI Timing (continued)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 74 | L1CLK edge to L1RSYNC, L1TSYNC, invalid (SYNC hold time) | 35.00 | — | ns |
| 75 | L1RSYNC, L1TSYNC rise/fall time | — | 15.00 | ns |
| 76 | L1RXD valid to L1CLK edge (L1RXD setup time) | 17.00 | — | ns |
| 77 | L1CLK edge to L1RXD invalid (L1RXD hold time) | 13.00 | — | ns |
| 78 | L1CLK edge to L1ST(1–4) valid [4] | 10.00 | 45.00 | ns |
| 78A | L1SYNC valid to L1ST(1–4) valid | 10.00 | 45.00 | ns |
| 79 | L1CLK edge to L1ST(1–4) invalid | 10.00 | 45.00 | ns |
| 80 | L1CLK edge to L1TXD valid | 10.00 | 55.00 | ns |
| 80A | L1TSYNC valid to L1TXD valid [4] | 10.00 | 55.00 | ns |
| 81 | L1CLK edge to L1TXD high impedance | 0.00 | 42.00 | ns |
| 82 | L1RCLK, L1TCLK frequency (DSC =1) | — | 16.00 or SYNCCLK/2 | MHz |
| 83 | L1RCLK, L1TCLK width low (DSC =1) | P + 10 | — | ns |
| 83a | L1RCLK, L1TCLK width high (DSC = 1)[3] | P + 10 | — | ns |
| 84 | L1CLK edge to L1CLKO valid (DSC = 1) | — | 30.00 | ns |
| 85 | $\overline{\text{L1RQ}}$ valid before falling edge of L1TSYNC[4] | 1.00 | — | L1TCLK |
| 86 | L1GR setup time[2] | 42.00 | — | ns |
| 87 | L1GR hold time | 42.00 | — | ns |
| 88 | L1CLK edge to L1SYNC valid (FSD = 00) CNT = 0000, BYT = 0, DSC = 0) | — | 0.00 | ns |

1 The ratio SyncCLK/L1RCLK must be greater than 2.5/1.

2 These specs are valid for IDL mode only.

3 Where P = 1/CLKOUT. Thus, for a 25-MHz CLKO1 rate, P = 40 ns.

4 These strobes and TxD on the first bit of the frame become valid after L1CLK edge or L1SYNC, whichever is later.

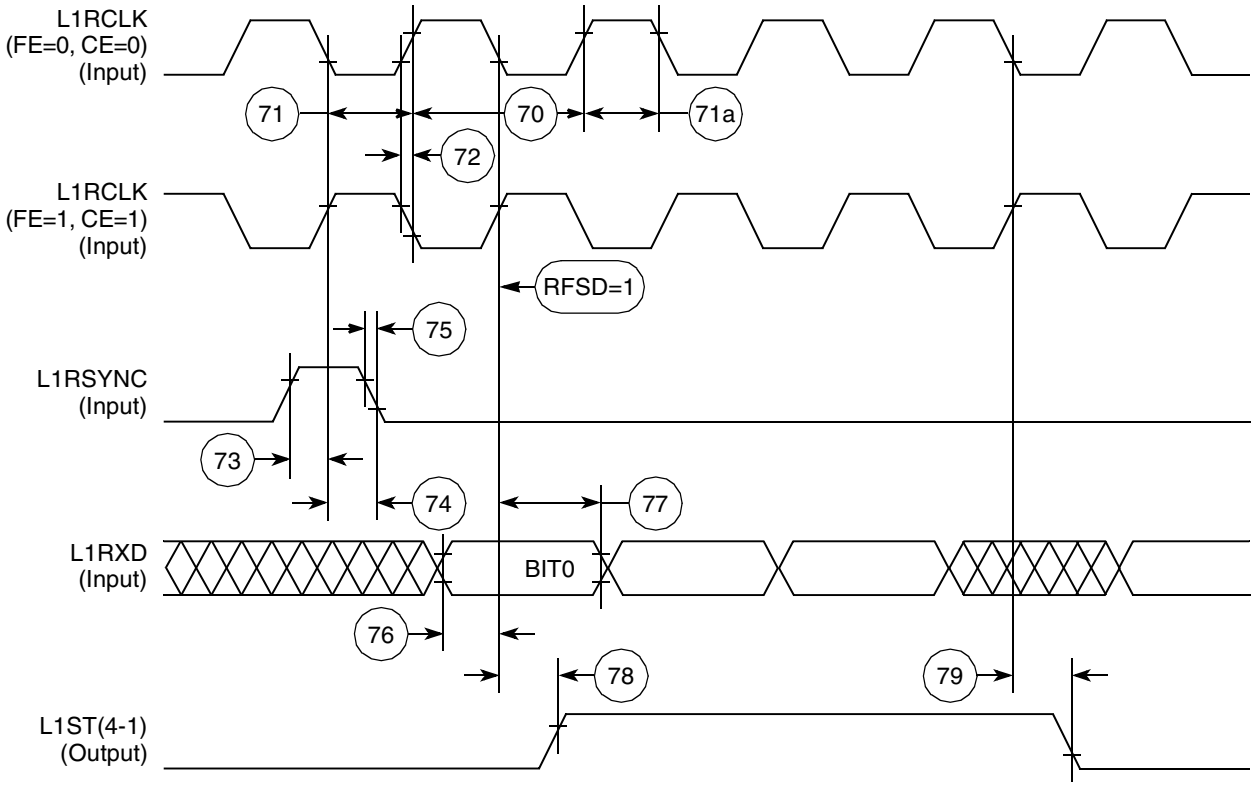



**Figure 53. SI Receive Timing Diagram with Normal Clocking (DSC = 0)**

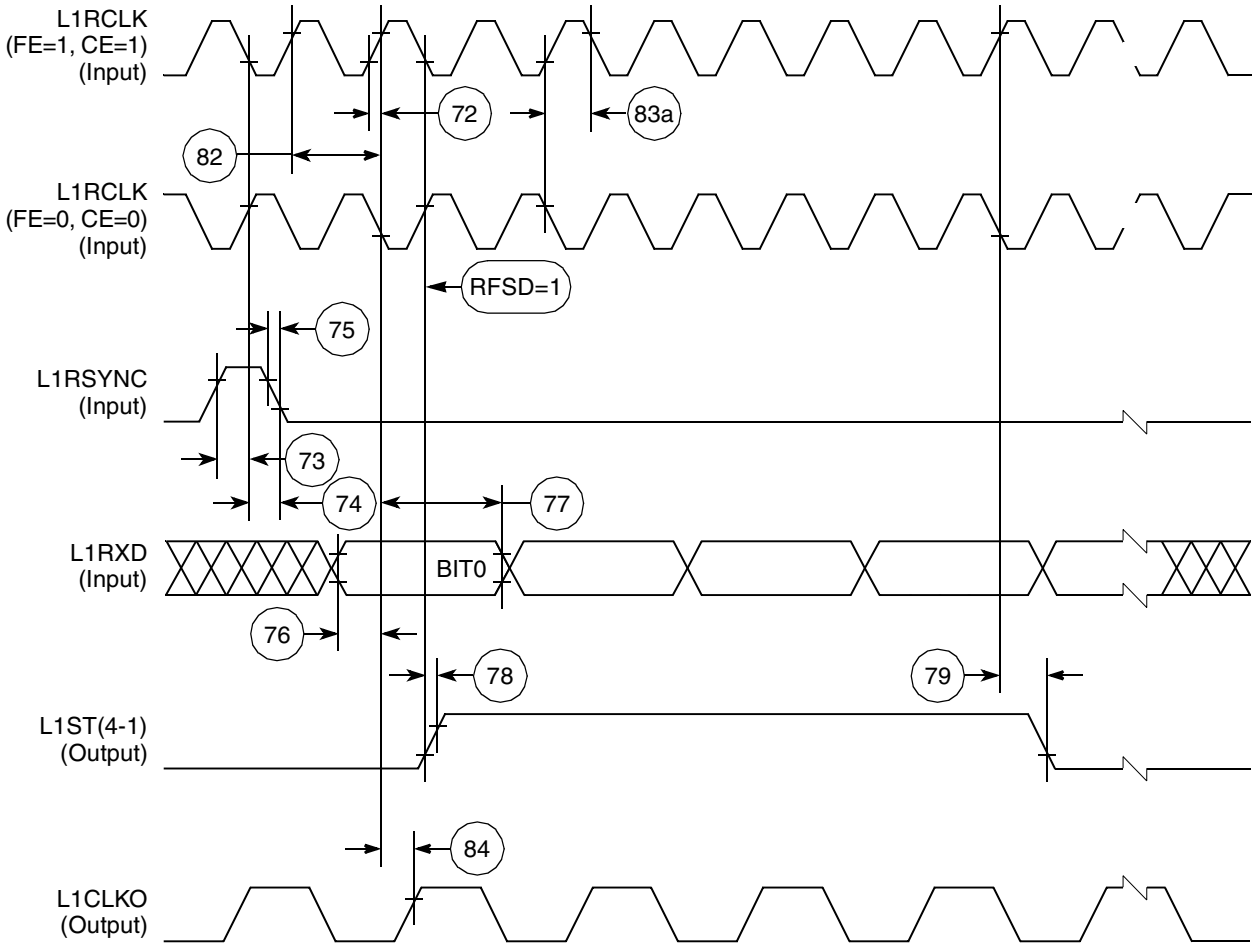



**Figure 54. SI Receive Timing with Double-Speed Clocking (DSC = 1)**

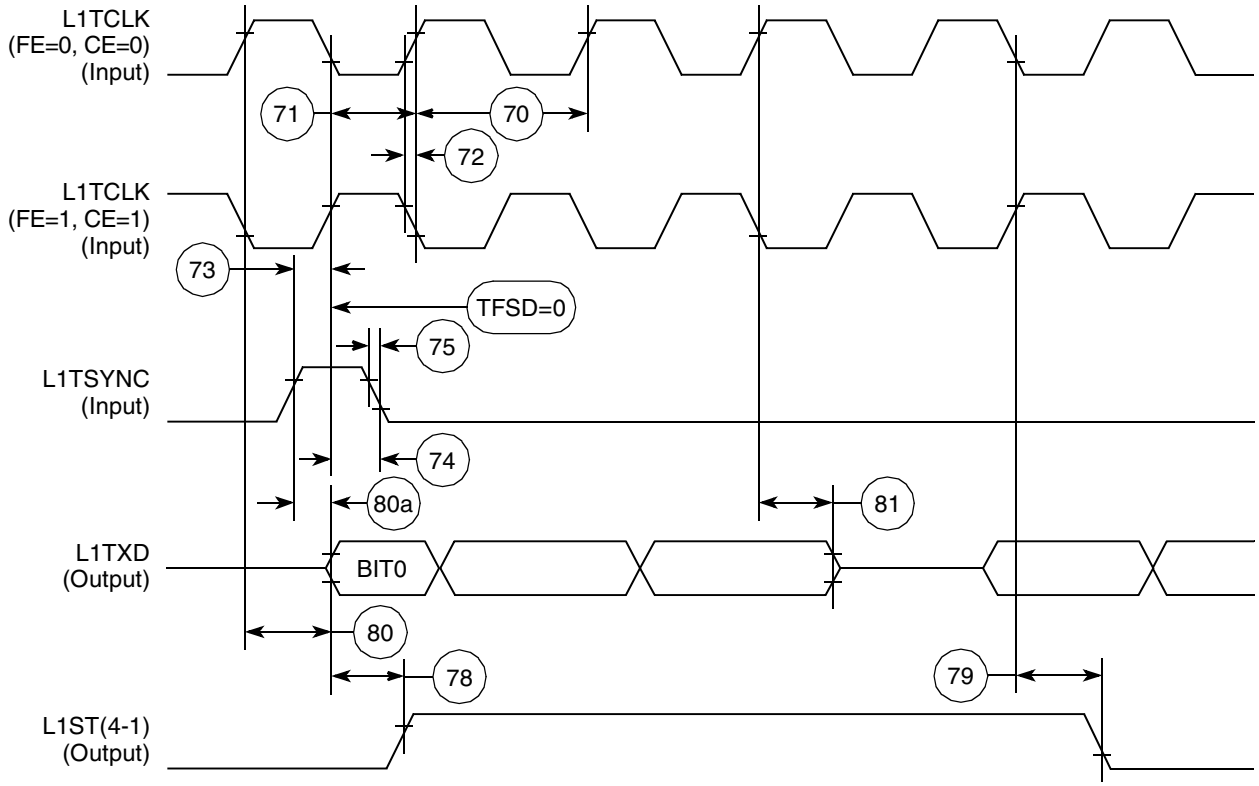



**Figure 55. SI Transmit Timing Diagram (DSC = 0)**

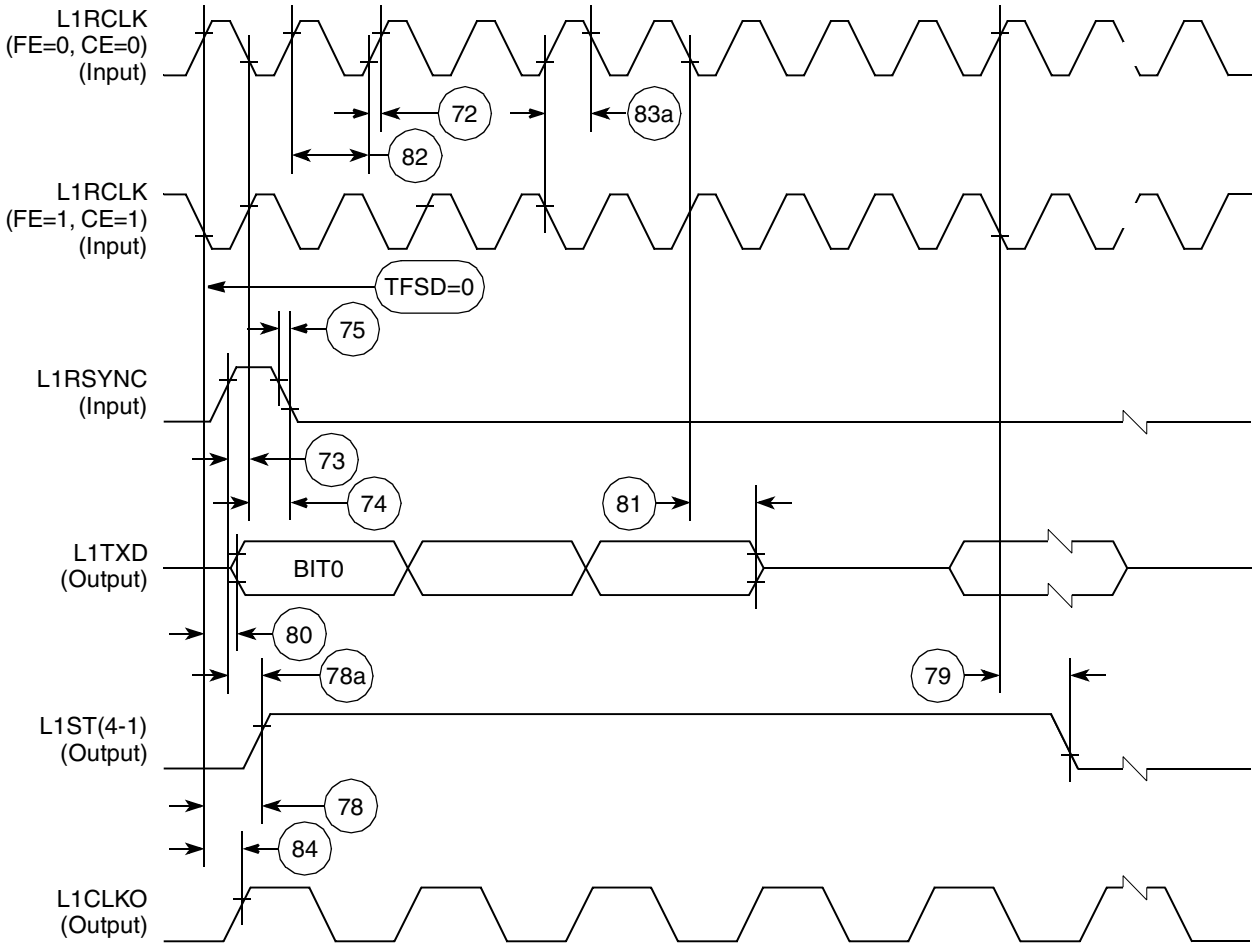



**Figure 56. SI Transmit Timing with Double Speed Clocking (DSC = 1)**

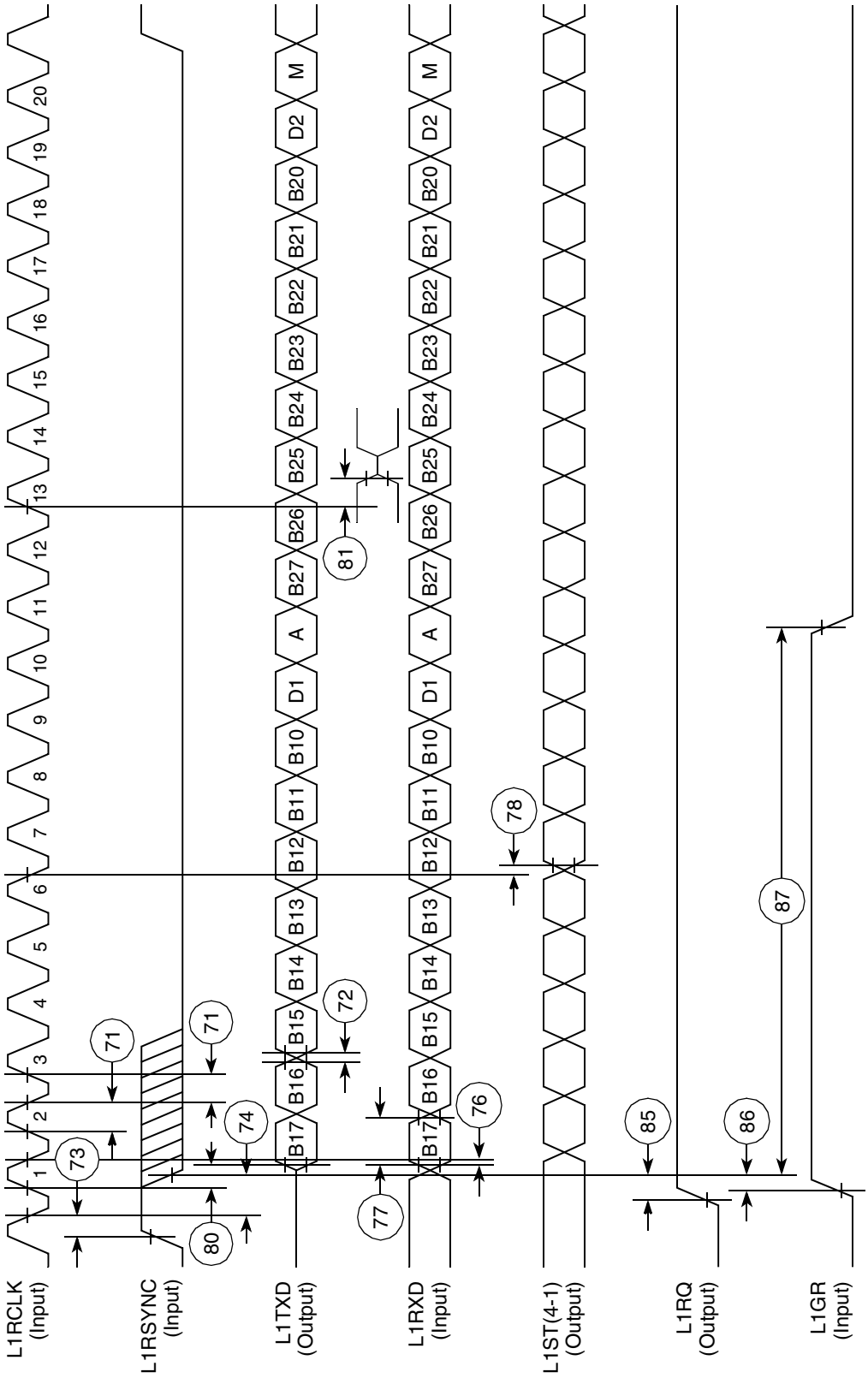



**Figure 57. IDL Timing**

## 12.7 SCC in NMSI Mode Electrical Specifications

Table 22 shows the NMSI external clock timings.

**Table 22. NMSI External Clock Timings**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLK1 and TCLK1 width high [1] | 1/SYNCCLK | — | ns |
| 101 | RCLK1 and TCLK1 width low | 1/SYNCCLK +5 | — | ns |
| 102 | RCLK1 and TCLK1 rise/fall time | — | 15.00 | ns |
| 103 | TXD1 active delay (from TCLK1 falling edge) | 0.00 | 50.00 | ns |
| 104 | $\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge) | 0.00 | 50.00 | ns |
| 105 | $\overline{\text{CTS1}}$ setup time to TCLK1 rising edge | 5.00 | — | ns |
| 106 | RXD1 setup time to RCLK1 rising edge | 5.00 | — | ns |
| 107 | RXD1 hold time from RCLK1 rising edge [2] | 5.00 | — | ns |
| 108 | $\overline{\text{CD1}}$ setup time to RCLK1 rising edge | 5.00 | — | ns |

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater than or equal to 2.25/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signal.

Table 23 shows the NMSI internal clock timings.

**Table 23. NMSI Internal Clock Timings**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 100 | RCLK1 and TCLK1 frequency [1] | 0.00 | SYNCCLK/3 | MHz |
| 102 | RCLK1 and TCLK1 rise/fall time | — | — | ns |
| 103 | TXD1 active delay (from TCLK1 falling edge) | 0.00 | 30.00 | ns |
| 104 | $\overline{\text{RTS1}}$ active/inactive delay (from TCLK1 falling edge) | 0.00 | 30.00 | ns |
| 105 | $\overline{\text{CTS1}}$ setup time to TCLK1 rising edge | 40.00 | — | ns |
| 106 | RXD1 setup time to RCLK1 rising edge | 40.00 | — | ns |
| 107 | RXD1 hold time from RCLK1 rising edge [2] | 0.00 | — | ns |
| 108 | $\overline{\text{CD1}}$ setup time to RCLK1 rising edge | 40.00 | — | ns |

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 3/1.

2 Also applies to $\overline{\text{CD}}$ and $\overline{\text{CTS}}$ hold time when they are used as an external sync signals.

Figure 58 through Figure 60 show the NMSI timings.

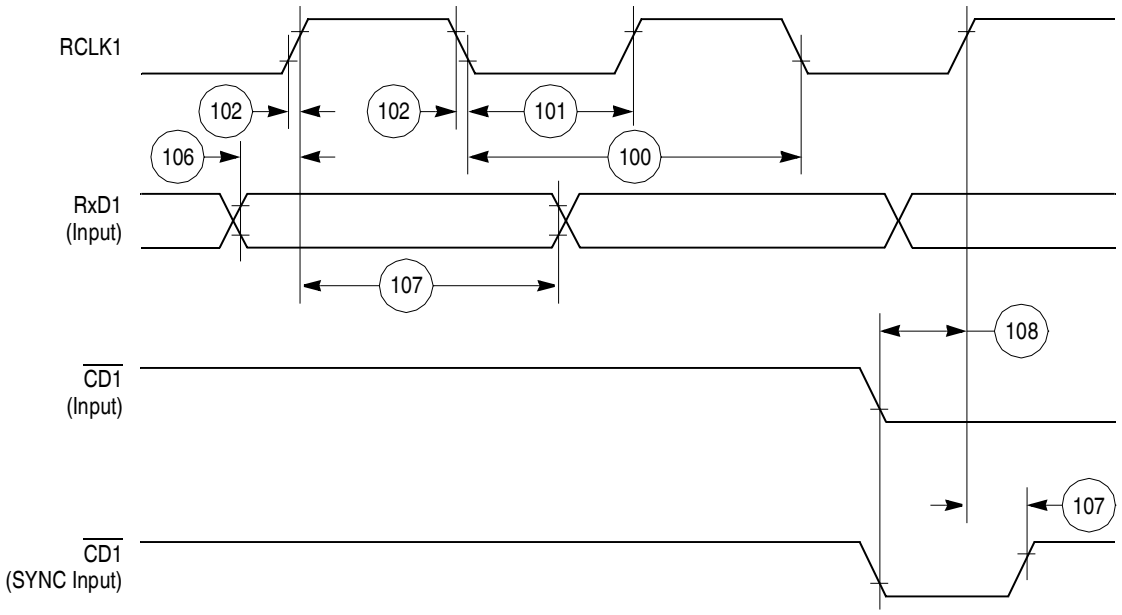



**Figure 58. SCC NMSI Receive Timing Diagram**

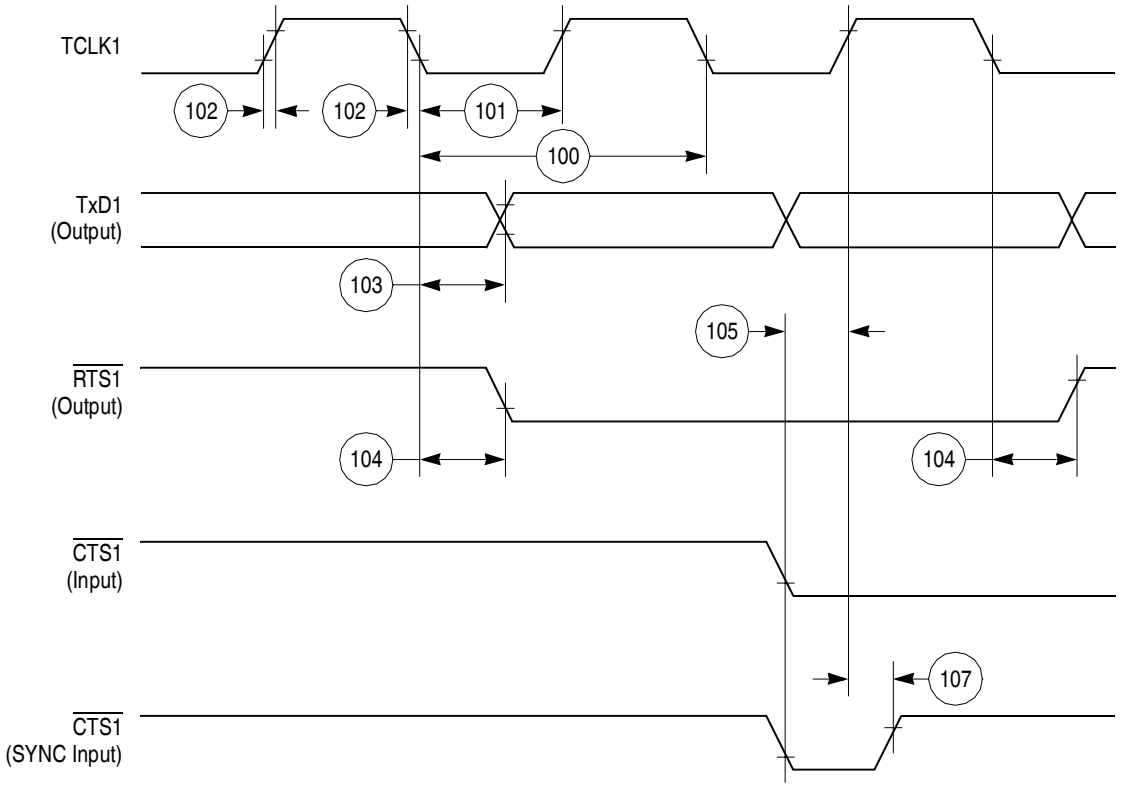



**Figure 59. SCC NMSI Transmit Timing Diagram**

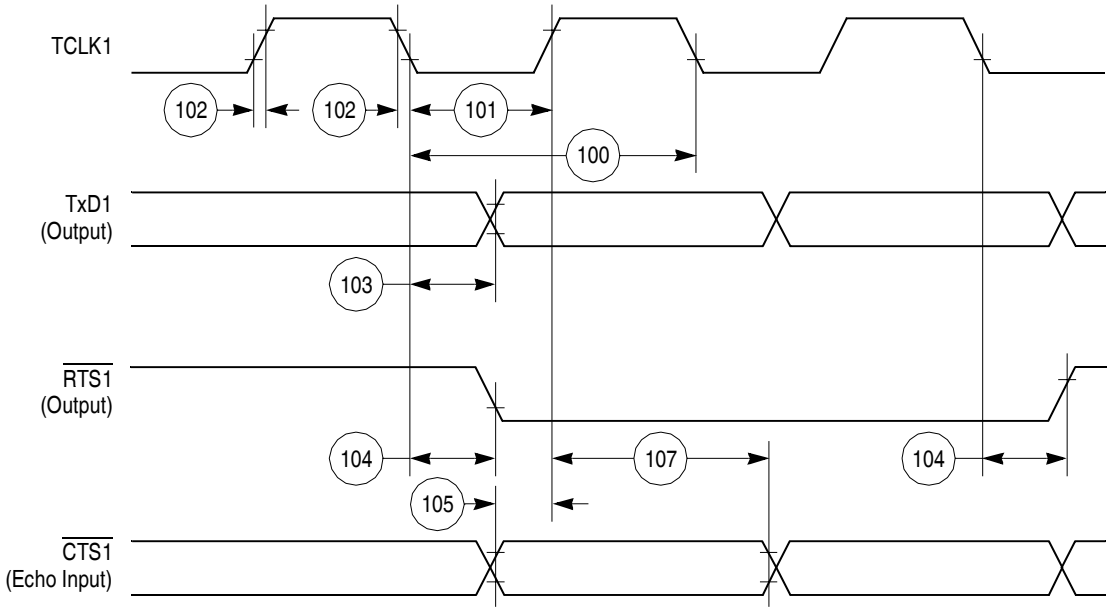



**Figure 60. HDLC Bus Timing Diagram**

## 12.8 Ethernet Electrical Specifications

Table 24 shows the Ethernet timings as shown in Figure 61 through Figure 65.

**Table 24. Ethernet Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 120 | CLSN width high | 40 | — | ns |
| 121 | RCLK1 rise/fall time | — | 15 | ns |
| 122 | RCLK1 width low | 40 | — | ns |
| 123 | RCLK1 clock period [1] | 80 | 120 | ns |
| 124 | RXD1 setup time | 20 | — | ns |
| 125 | RXD1 hold time | 5 | — | ns |
| 126 | RENA active delay (from RCLK1 rising edge of the last data bit) | 10 | — | ns |
| 127 | RENA width low | 100 | — | ns |
| 128 | TCLK1 rise/fall time | — | 15 | ns |
| 129 | TCLK1 width low | 40 | — | ns |
| 130 | TCLK1 clock period [1] | 99 | 101 | ns |
| 131 | TXD1 active delay (from TCLK1 rising edge) | — | 50 | ns |
| 132 | TXD1 inactive delay (from TCLK1 rising edge) | 6.5 | 50 | ns |
| 133 | TENA active delay (from TCLK1 rising edge) | 10 | 50 | ns |

**Table 24. Ethernet Timing (continued)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 134 | TENA inactive delay (from TCLK1 rising edge) | 10 | 50 | ns |
| 135 | $\overline{\text{RSTRT}}$ active delay (from TCLK1 falling edge) | 10 | 50 | ns |
| 136 | $\overline{\text{RSTRT}}$ inactive delay (from TCLK1 falling edge) | 10 | 50 | ns |
| 137 | $\overline{\text{REJECT}}$ width low | 1 | — | CLK |
| 138 | CLKO1 low to $\overline{\text{SDACK}}$ asserted [2] | — | 20 | ns |
| 139 | CLKO1 low to $\overline{\text{SDACK}}$ negated [2] | — | 20 | ns |

1 The ratios SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2/1.

2 $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

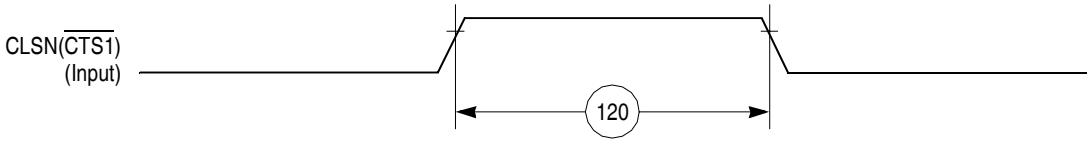



**Figure 61. Ethernet Collision Timing Diagram**

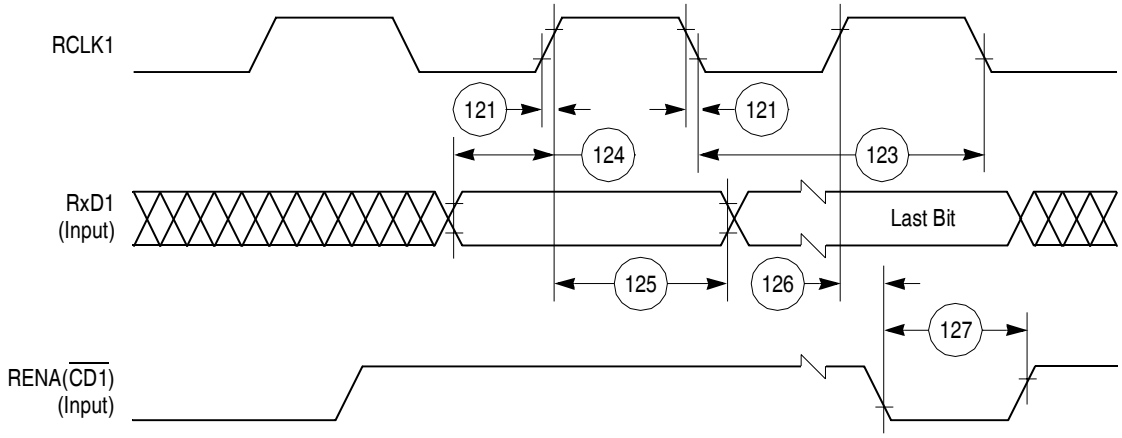
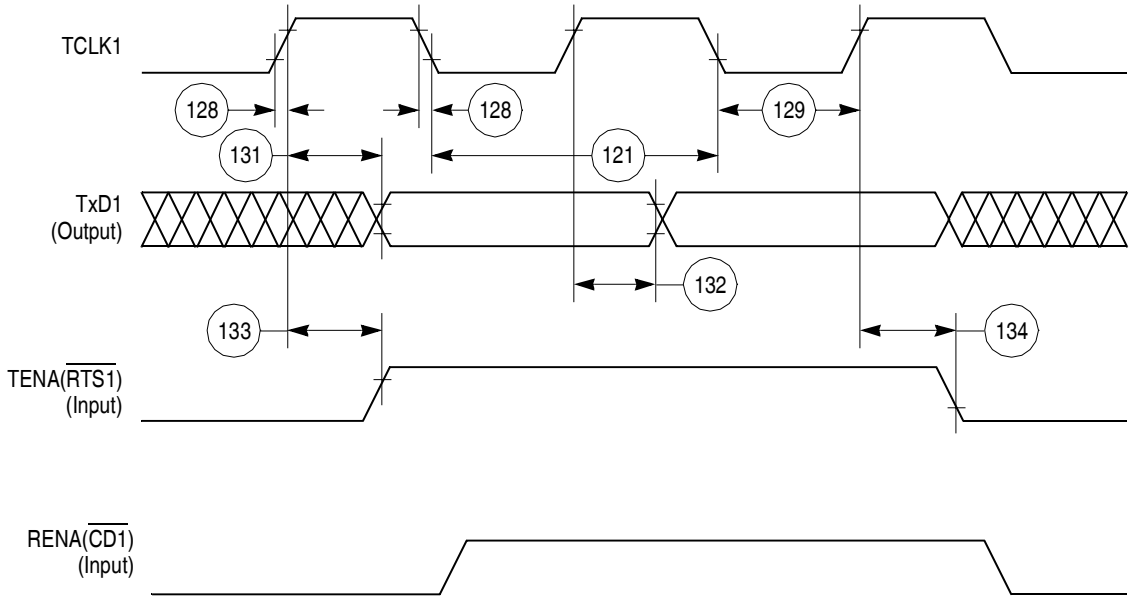



**Figure 62. Ethernet Receive Timing Diagram**




Notes:
1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transmit, then the CSL bit is set in the buffer descriptor at the end of the frame transmission.

**Figure 63. Ethernet Transmit Timing Diagram**

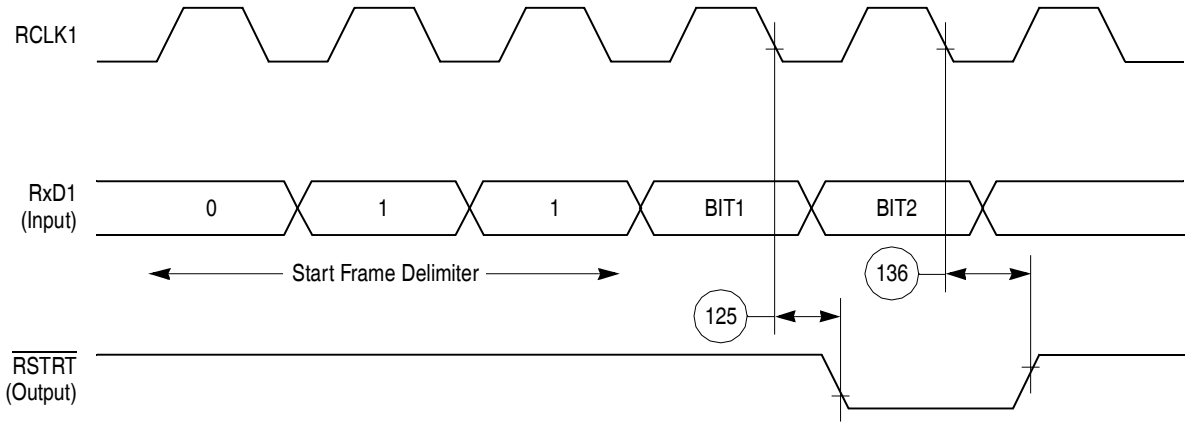



**Figure 64. CAM Interface Receive Start Timing Diagram**

**Figure 65. CAM Interface REJECT Timing Diagram**

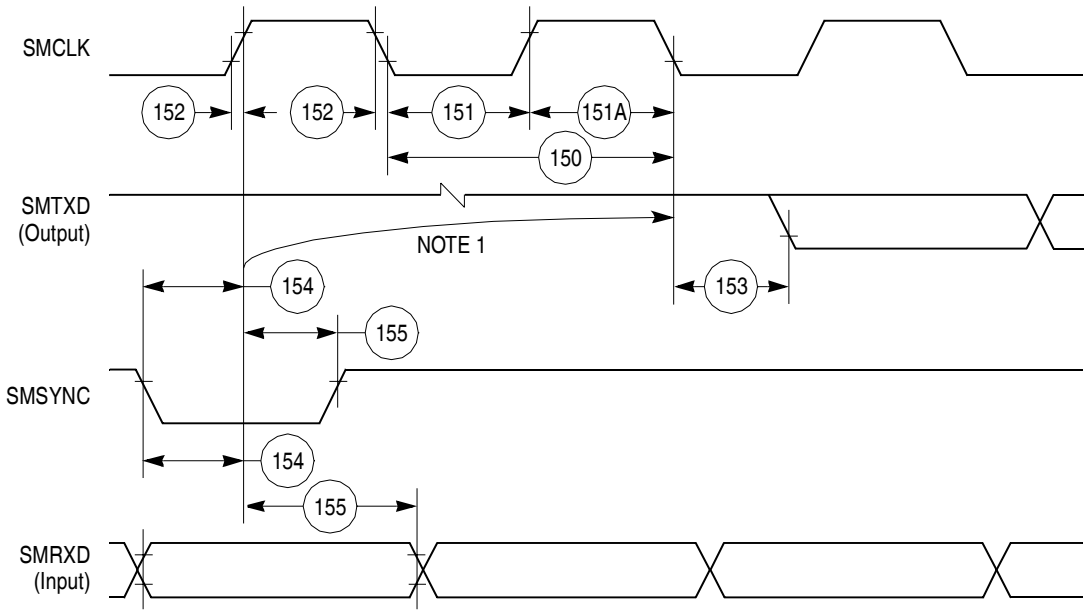
## 12.9 SMC Transparent AC Electrical Specifications

Table 25 shows the SMC transparent timings as shown in Figure 66.

**Table 25. SMC Transparent Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 150 | SMCLK clock period [1] | 100 | — | ns |
| 151 | SMCLK width low | 50 | — | ns |
| 151A | SMCLK width high | 50 | — | ns |
| 152 | SMCLK rise/fall time | — | 15 | ns |
| 153 | SMTXD active delay (from SMCLK falling edge) | 10 | 50 | ns |
| 154 | SMRXD/SMSYNC setup time | 20 | — | ns |
| 155 | RXD1/SMSYNC hold time | 5 | — | ns |

1 Sync CLK must be at least twice as fast as SMCLK.




NOTE:
1. This delay is equal to an integer number of character-length clocks.

**Figure 66. SMC Transparent Timing Diagram**

## 12.10SPI Master AC Electrical Specifications

Table 26 shows the SPI master timings as shown in Figure 67 and Figure 68.

**Table 26. SPI Master Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 160 | MASTER cycle time | 4 | 1024 | $t_{cyc}$ |
| 161 | MASTER clock (SCK) high or low time | 2 | 512 | $t_{cyc}$ |
| 162 | MASTER data setup time (inputs) | 15 | — | ns |
| 163 | Master data hold time (inputs) | 0 | — | ns |
| 164 | Master data valid (after SCK edge) | — | 10 | ns |
| 165 | Master data hold time (outputs) | 0 | — | ns |
| 166 | Rise time output | — | 15 | ns |
| 167 | Fall time output | — | 15 | ns |

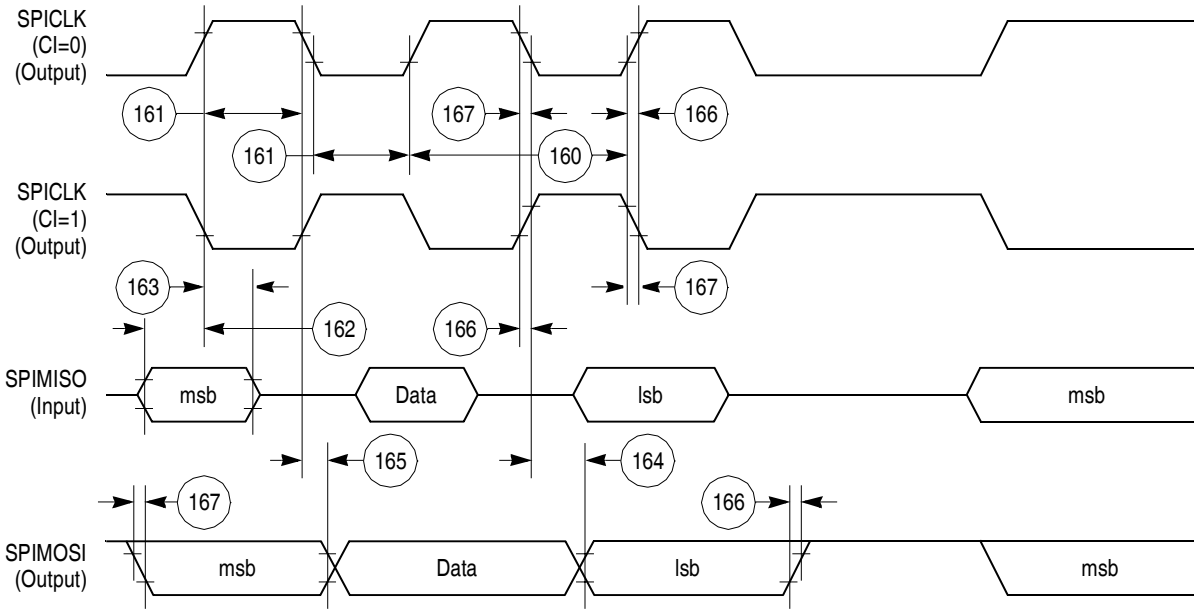



**Figure 67. SPI Master (CP = 0) Timing Diagram**

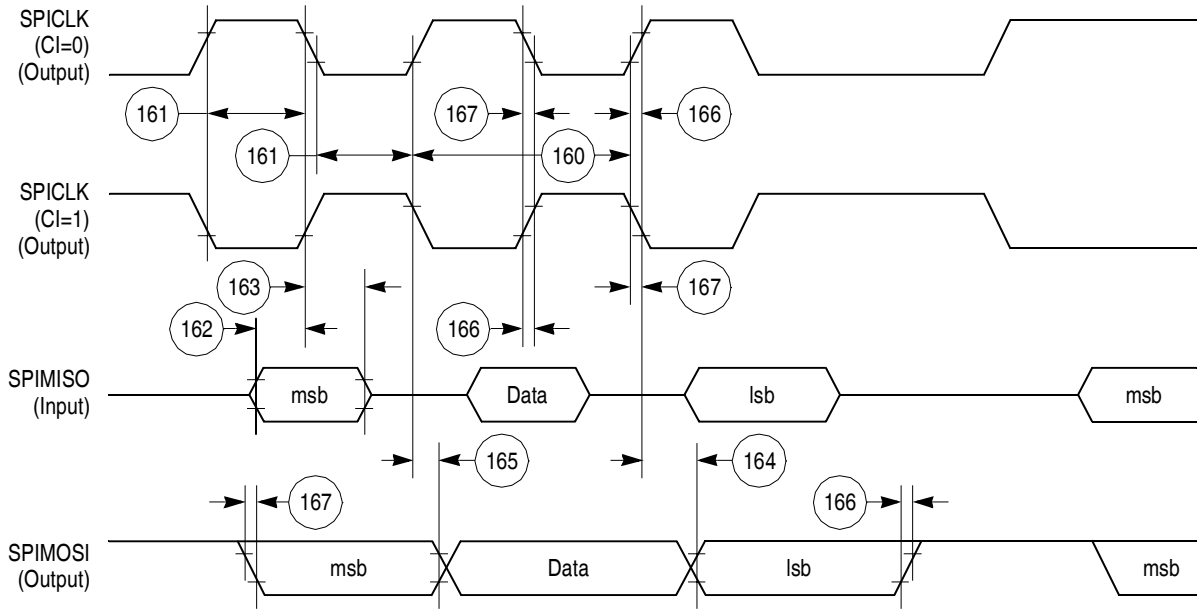



**Figure 68. SPI Master (CP = 1) Timing Diagram**

## 12.11SPI Slave AC Electrical Specifications

Table 27 shows the SPI slave timings as shown in Figure 69 and Figure 70.

**Table 27. SPI Slave Timing**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 170 | Slave cycle time | 2 | — | $t_{cyc}$ |
| 171 | Slave enable lead time | 15 | — | ns |
| 172 | Slave enable lag time | 15 | — | ns |
| 173 | Slave clock (SPICLK) high or low time | 1 | — | $t_{cyc}$ |
| 174 | Slave sequential transfer delay (does not require deselect) | 1 | — | $t_{cyc}$ |
| 175 | Slave data setup time (inputs) | 20 | — | ns |
| 176 | Slave data hold time (inputs) | 20 | — | ns |
| 177 | Slave access time | — | 50 | ns |

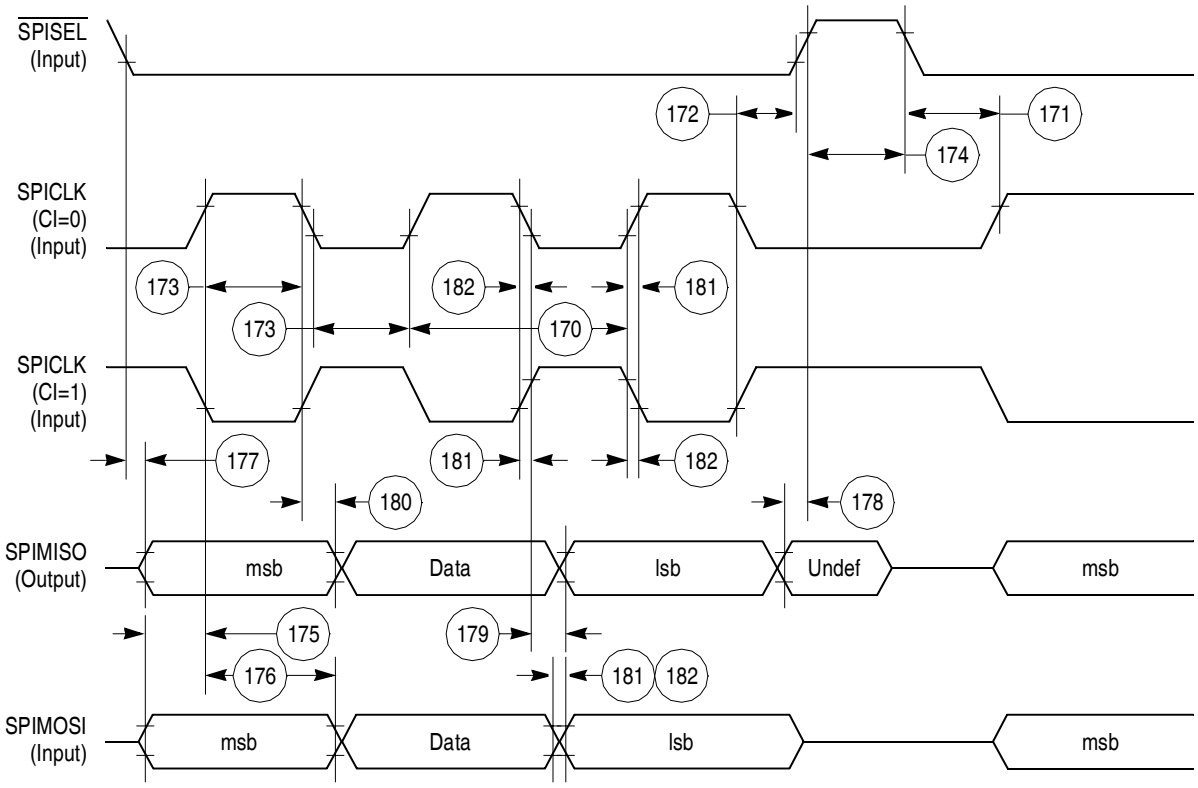



**Figure 69. SPI Slave (CP = 0) Timing Diagram**

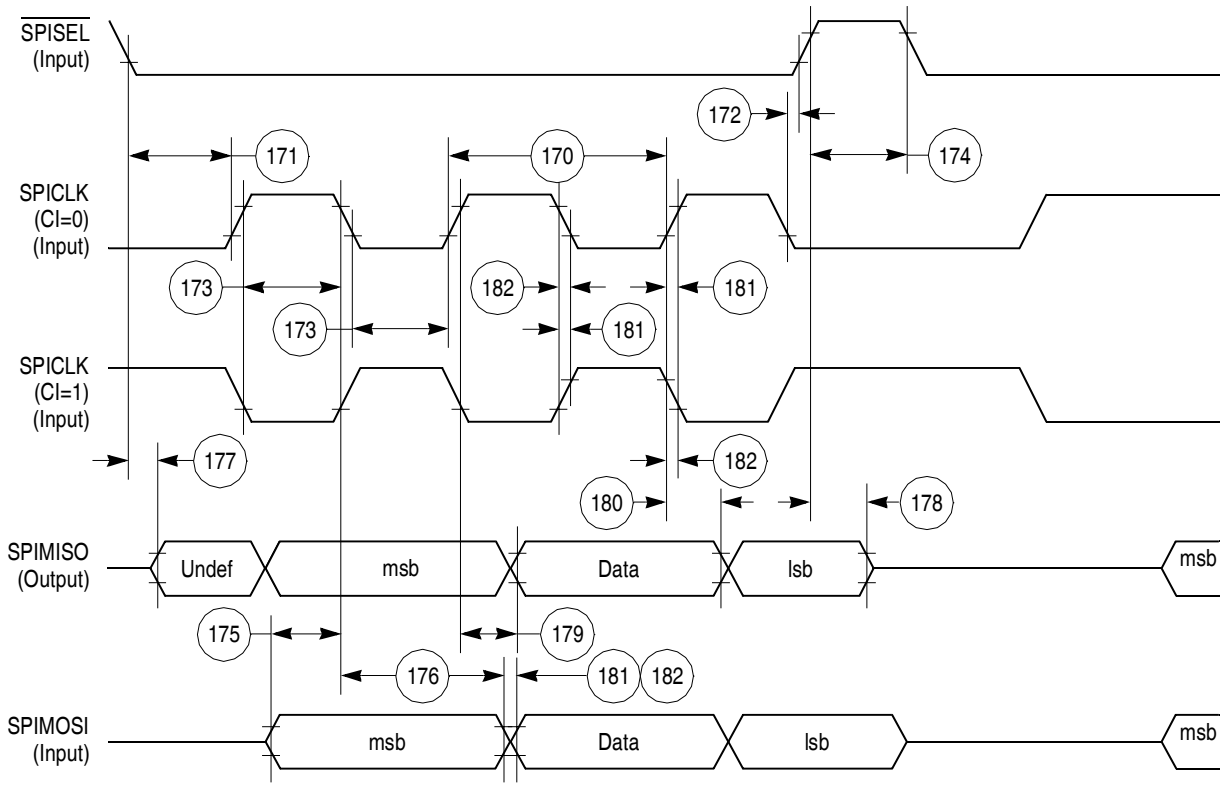



**Figure 70. SPI Slave (CP = 1) Timing Diagram**

# 12.12 I²C AC Electrical Specifications

Table 28 shows the $I^2C$ (SCL < 100 kHz) timings.

**Table 28. $I^2C$ Timing (SCL < 100 kHz)**

| Num | Characteristic | All Frequencies | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| 200 | SCL clock frequency (slave) | 0 | 100 | kHz |
| 200 | SCL clock frequency (master) [1] | 1.5 | 100 | kHz |
| 202 | Bus free time between transmissions | 4.7 | — | µs |
| 203 | Low period of SCL | 4.7 | — | µs |
| 204 | High period of SCL | 4.0 | — | µs |
| 205 | Start condition setup time | 4.7 | — | µs |
| 206 | Start condition hold time | 4.0 | — | µs |
| 207 | Data hold time | 0 | — | µs |
| 208 | Data setup time | 250 | — | ns |
| 209 | SDL/SCL rise time | — | 1 | µs |
| 210 | SDL/SCL fall time | — | 300 | ns |
| 211 | Stop condition setup time | 4.7 | — | µs |

1 SCL frequency is given by SCL = BRGCLK_frequency / ((BRG register + 3) * pre_scaler * 2).
The ratio SyncClk/(BRGCLK/pre_scaler) must be greater or equal to 4/1.

Table 29 shows the $I^2C$ (SCL > 100 kHz) timings.

**Table 29. $I^2C$ Timing (SCL > 100 kHz)**

| Num | Characteristic | Expression | All Frequencies | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 200 | SCL clock frequency (slave) | fSCL | 0 | BRGCLK/48 | Hz |
| 200 | SCL clock frequency (master) [1] | fSCL | BRGCLK/16512 | BRGCLK/48 | Hz |
| 202 | Bus free time between transmissions | — | 1/(2.2 * fSCL) | — | s |
| 203 | Low period of SCL | — | 1/(2.2 * fSCL) | — | s |
| 204 | High period of SCL | — | 1/(2.2 * fSCL) | — | s |
| 205 | Start condition setup time | — | 1/(2.2 * fSCL) | — | s |
| 206 | Start condition hold time | — | 1/(2.2 * fSCL) | — | s |
| 207 | Data hold time | — | 0 | — | s |
| 208 | Data setup time | — | 1/(40 * fSCL) | — | s |
| 209 | SDL/SCL rise time | — | — | 1/(10 * fSCL) | s |
| 210 | SDL/SCL fall time | — | — | 1/(33 * fSCL) | s |
| 211 | Stop condition setup time | — | 1/2(2.2 * fSCL) | — | s |

1 SCL frequency is given by SCL = BrgClk_frequency / ((BRG register + 3) * pre_scaler * 2).
The ratio SyncClk/(Brg_Clk/pre_scaler) must be greater or equal to 4/1.

Figure 71 shows the $I^2C$ bus timing.

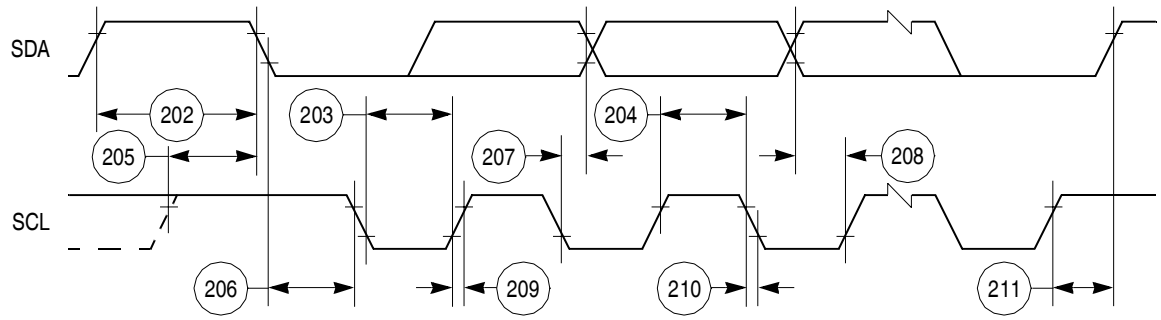



**Figure 71. $I^2C$ Bus Timing Diagram**

# 13 UTOPIA AC Electrical Specifications

Table 30 through Table 32 show the AC electrical specifications for the UTOPIA interface.

**Table 30. UTOPIA Master (Muxed Mode) Electrical Specifications**

| Num | Signal Characteristic | Direction | Min | Max | Unit |
|---|---|---|---|---|---|
| U1 | UtpClk rise/fall time (Internal clock option) | Output | — | 4 | ns |
| | Duty cycle | | 50 | 50 | % |
| | Frequency | | — | 33 | MHz |
| U2 | UTPB, SOC, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr-active delay (and PHREQ and PHSEL active delay in MPHY mode) | Output | 2 | 16 | ns |
| U3 | UTPB, SOC, Rxclav and Txclav setup time | Input | 4 | — | ns |
| U4 | UTPB, SOC, Rxclav and Txclav hold time | Input | 1 | — | ns |

**Table 31. UTOPIA Master (Split Bus Mode) Electrical Specifications**

| Num | Signal Characteristic | Direction | Min | Max | Unit |
|---|---|---|---|---|---|
| U1 | UtpClk rise/fall time (Internal clock option) | Output | — | 4 | ns |
| | Duty cycle | | 50 | 50 | % |
| | Frequency | | — | 33 | MHz |
| U2 | UTPB, SOC, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr and TxAddr active delay (PHREQ and PHSEL active delay in MPHY mode) | Output | 2 | 16 | ns |
| U3 | UTPB_Aux, SOC_Aux, Rxclav, and Txclav setup time | Input | 4 | — | ns |
| U4 | UTPB_Aux, SOC_Aux, Rxclav, and Txclav hold time | Input | 1 | — | ns |

**Table 32. UTOPIA Slave (Split Bus Mode) Electrical Specifications**

| Num | Signal Characteristic | Direction | Min | Max | Unit |
|---|---|---|---|---|---|
| U1 | UtpClk rise/fall time (external clock option) | Input | — | 4 | ns |
| | Duty cycle | | 40 | 60 | % |
| | Frequency | | — | 33 | MHz |
| U2 | UTPB, SOC, Rxclav and Txclav active delay | Output | 2 | 16 | ns |
| U3 | UTPB_AUX, SOC_Aux, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr setup time | Input | 4 | — | ns |
| U4 | UTPB_AUX, SOC_Aux, $\overline{\text{RxEnb}}$, $\overline{\text{TxEnb}}$, RxAddr, and TxAddr hold time | Input | 1 | — | ns |

Figure 72 shows signal timings during UTOPIA receive operations.

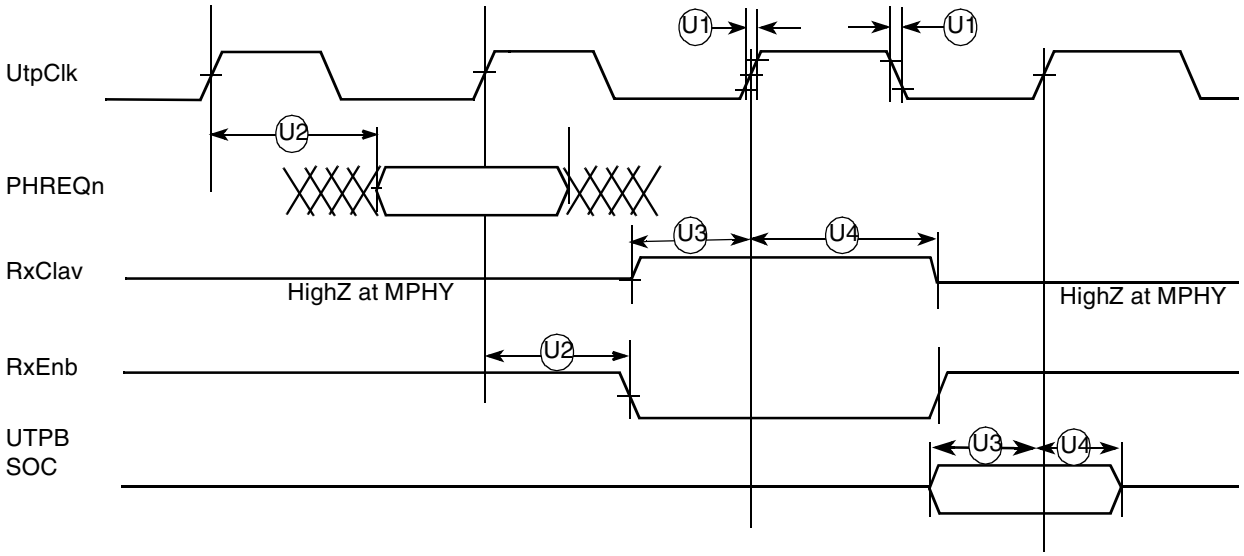



**Figure 72. UTOPIA Receive Timing**

Figure 73 shows signal timings during UTOPIA transmit operations.

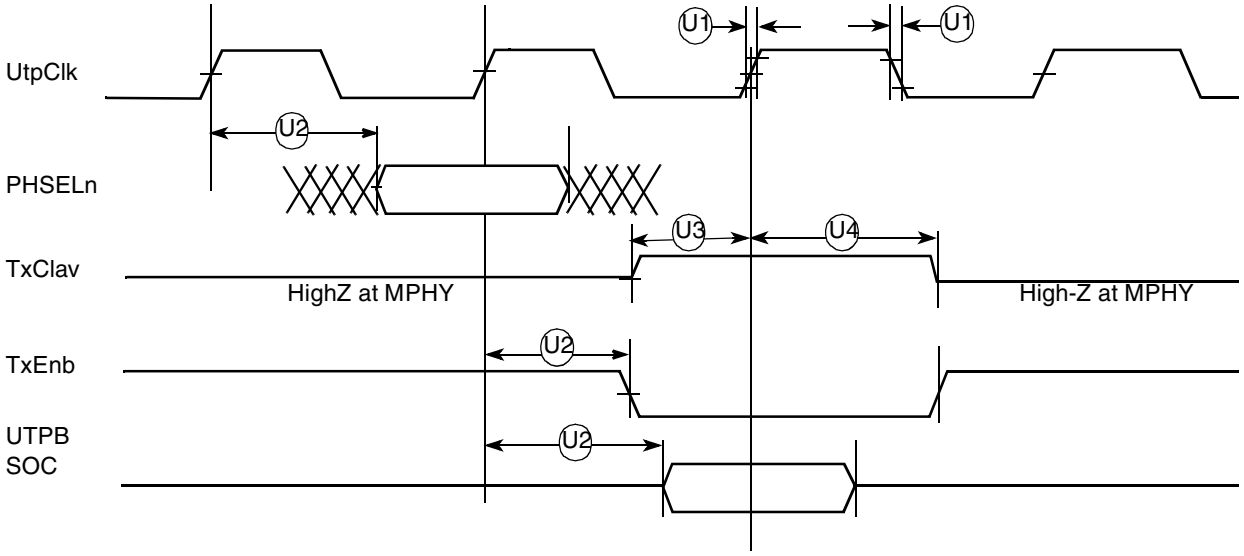



**Figure 73. UTOPIA Transmit Timing**

# 14 FEC Electrical Characteristics

This section provides the AC electrical specifications for the fast Ethernet controller (FEC). Note that the timing specifications for the MII signals are independent of system clock frequency (part speed designation). Also, MII signals use TTL signal levels compatible with devices operating at either 5.0 or 3.3 V.

## 14.1 MII Receive Signal Timing (MII_RXD [3:0], MII_RX_DV, MII_RX_ER, MII_RX_CLK)

The receiver functions correctly up to a MII_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_RX_CLK frequency – 1%. Table 33 shows the timings for MII receive signal.

**Table 33. MII Receive Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M1 | MII_RXD[3:0], MII_RX_DV, MII_RX_ER to MII_RX_CLK setup | 5 | — | ns |
| M2 | MII_RX_CLK to MII_RXD[3:0], MII_RX_DV, MII_RX_ER hold | 5 | — | ns |
| M3 | MII_RX_CLK pulse width high | 35% | 65% | MII_RX_CLK period |
| M4 | MII_RX_CLK pulse width low | 35% | 65% | MII_RX_CLK period |

Figure 74 shows the timings for MII receive signal.

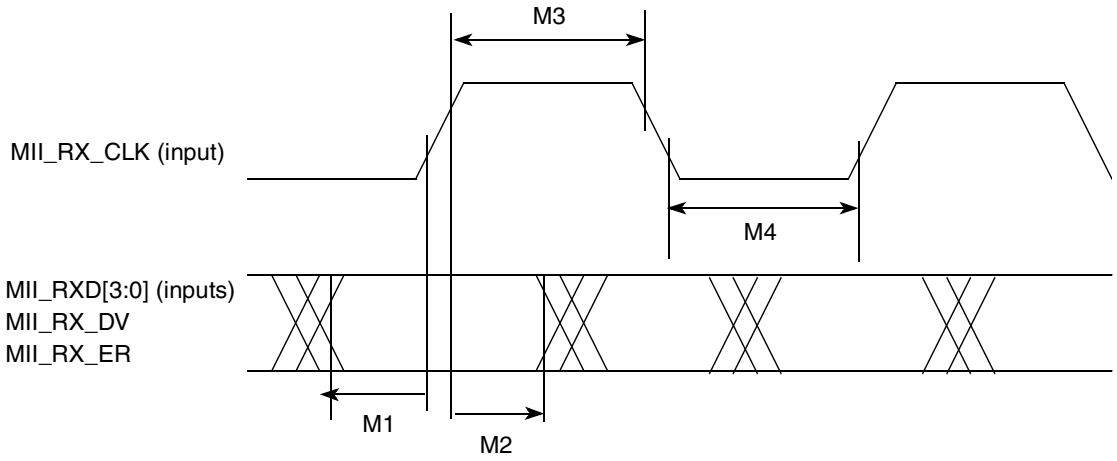



**Figure 74. MII Receive Signal Timing Diagram**

## 14.2 MII Transmit Signal Timing (MII_TXD[3:0], MII_TX_EN, MII_TX_ER, MII_TX_CLK)

The transmitter functions correctly up to a MII_TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed the MII_TX_CLK frequency - 1%.

Table 34 shows information on the MII transmit signal timing.

**Table 34. MII Transmit Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M5 | MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER invalid | 5 | — | ns |
| M6 | MII_TX_CLK to MII_TXD[3:0], MII_TX_EN, MII_TX_ER valid | — | 25 | — |
| M7 | MII_TX_CLK pulse width high | 35% | 65% | MII_TX_CLK period |
| M8 | MII_TX_CLK pulse width low | 35% | 65% | MII_TX_CLK period |

Figure 75 shows the MII transmit signal timing diagram.

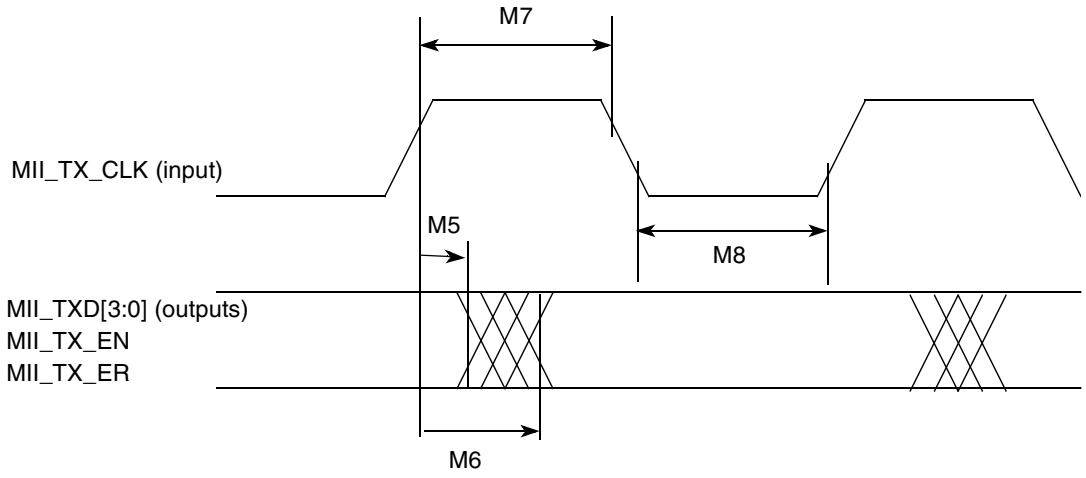



**Figure 75. MII Transmit Signal Timing Diagram**

## 14.3 MII Async Inputs Signal Timing (MII_CRS, MII_COL)

Table 35 shows the timing for on the MII async inputs signal.

**Table 35. MII Async Inputs Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M9 | MII_CRS, MII_COL minimum pulse width | 1.5 | — | MII_TX_CLK period |

Figure 76 shows the MII asynchronous inputs signal timing diagram.

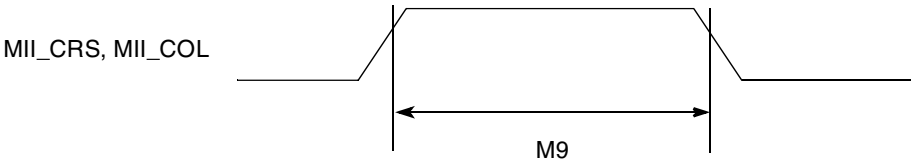



**Figure 76. MII Async Inputs Timing Diagram**

## 14.4 MII Serial Management Channel Timing (MII_MDIO, MII_MDC)

Table 36 shows the timing for the MII serial management channel signal. The FEC functions correctly with a maximum MDC frequency in excess of 2.5 MHz. The exact upper bound is under investigation.

**Table 36. MII Serial Management Channel Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M10 | MII_MDC falling edge to MII_MDIO output invalid (minimum propagation delay) | 0 | — | ns |
| M11 | MII_MDC falling edge to MII_MDIO output valid (maximum propagation delay) | — | 25 | ns |
| M12 | MII_MDIO (input) to MII_MDC rising edge setup | 10 | — | ns |

**Table 36. MII Serial Management Channel Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M13 | MII_MDIO (input) to MII_MDC rising edge hold | 0 | — | ns |
| M14 | MII_MDC pulse width high | 40% | 60% | MII_MDC period |
| M15 | MII_MDC pulse width low | 40% | 60% | MII_MDC period |

Figure 77 shows the MII serial management channel timing diagram.

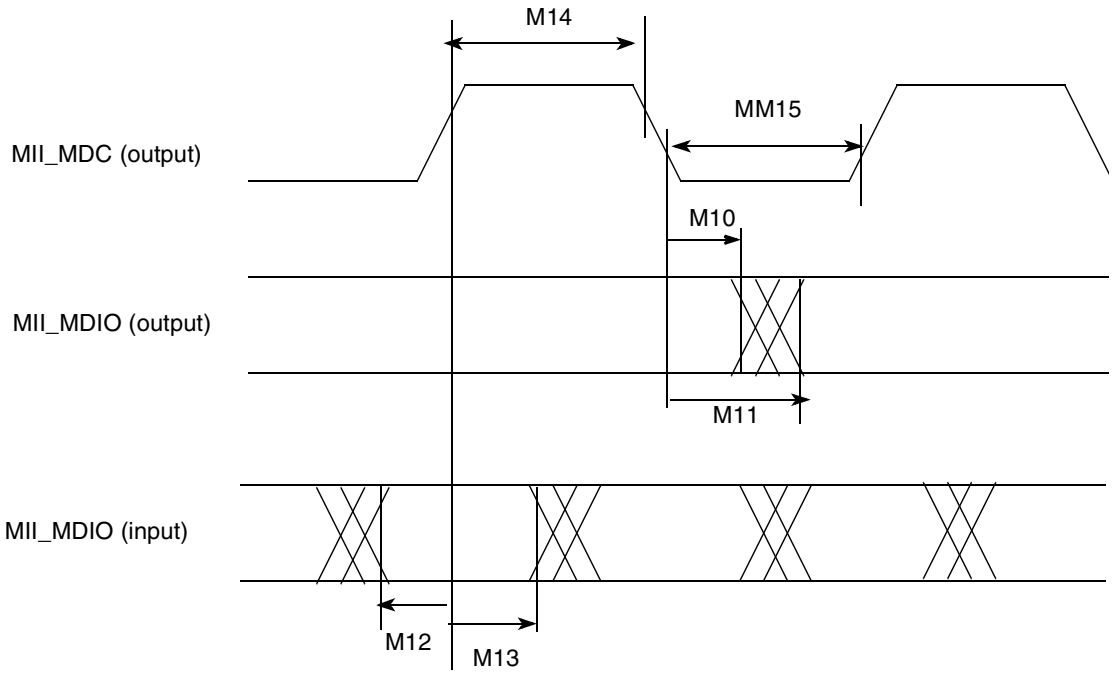



**Figure 77. MII Serial Management Channel Timing Diagram**

# 15 Mechanical Data and Ordering Information

Table 37 shows information on the MPC866/859 derivative devices.

**Table 37. MPC866/859 Derivatives**

| Device | Number of SCCs [1] | Ethernet Support | Multi-Channel HDLC Support | ATM Support | Cache Size | |
|---|---|---|---|---|---|---|
| | | | | | Instruction | Data |
| MPC866T | 4 | 10/100 Mbps | Yes | Yes | 4 Kbyte | 4 Kbytes |
| MPC866P | 4 | 10/100 Mbps | Yes | Yes | 16 Kbyte | 8 Kbytes |
| MPC859T | 1 (SCC1) | 10/100 Mbps | Yes | Yes | 4 Kbyte | 4 Kbytes |
| MPC859DSL | 1 (SCC1) | 10/100 Mbps | No | Up to 4 addresses | 4 Kbyte | 4 Kbytes |

[1] Serial communications controller (SCC).

Table 38 identifies the packages and operating frequencies orderable for the MPC866/859 derivative devices.

**Table 38. MPC866/859 Package/Frequency Orderable**

| Package Type | Temperature (Tj) | Frequency (MHz) | Order Number |
|---|---|---|---|
| Plastic ball grid array<br>(ZP suffix)<br>Non lead free | 0° to 95°C | 50 | MPC859DSLZP50A |
| | | 66 | MPC859DSLZP66A |
| | | 100 | MPC859PZP100A<br>MPC859TZP100A<br>MPC866PZP100A<br>MPC866TZP100A |
| | | 133 | MPC859PZP133A<br>MPC859TZP133A<br>MPC866PZP133A<br>MPC866TZP133A |
| Plastic ball grid array<br>(CZP suffix)<br>Non lead free | –40° to 100°C | 50 | MPC859DSLCZP50A |
| | | 66 | MPC859DSLCZP66A |
| | | 100 | MPC859PCZP100A<br>MPC859TCZP100A<br>MPC866PCZP100A<br>MPC866TCZP100A |

**Table 38. MPC866/859 Package/Frequency Orderable (continued)**

| | | | |
|---|---|---|---|
| Plastic ball grid array<br>(VR suffix)<br>Lead free | 0° to 95°C | 50 | MPC859DSLVR50A |
| | | 66 | MPC859DSLVR66A |
| | | 100 | MPC859PVR100A<br>MPC859TVR100A<br>MPC866PVR100A<br>MPC866TVR100A |
| | | 133 | MPC859PVR133A<br>MPC859TVR133A<br>MPC866PVR133A<br>MPC866TVR133A |
| Plastic ball grid array<br>(CVR suffix)<br>Lead free | –40° to 100°C | 50 | MPC859DSLCVR50A |
| | | 66 | MPC859DSLCVR66A |
| | | 100 | MPC859PCVR100A<br>MPC859TCVR100A<br>MPC866PCVR100A<br>MPC866TCVR100A |

# 15.1 Pin Assignments

Figure 78 shows the top view pinout of the PBGA package. For additional information, see the *MPC866 PowerQUICC Family User's Manual*.

**NOTE: This is the top view of the device.**

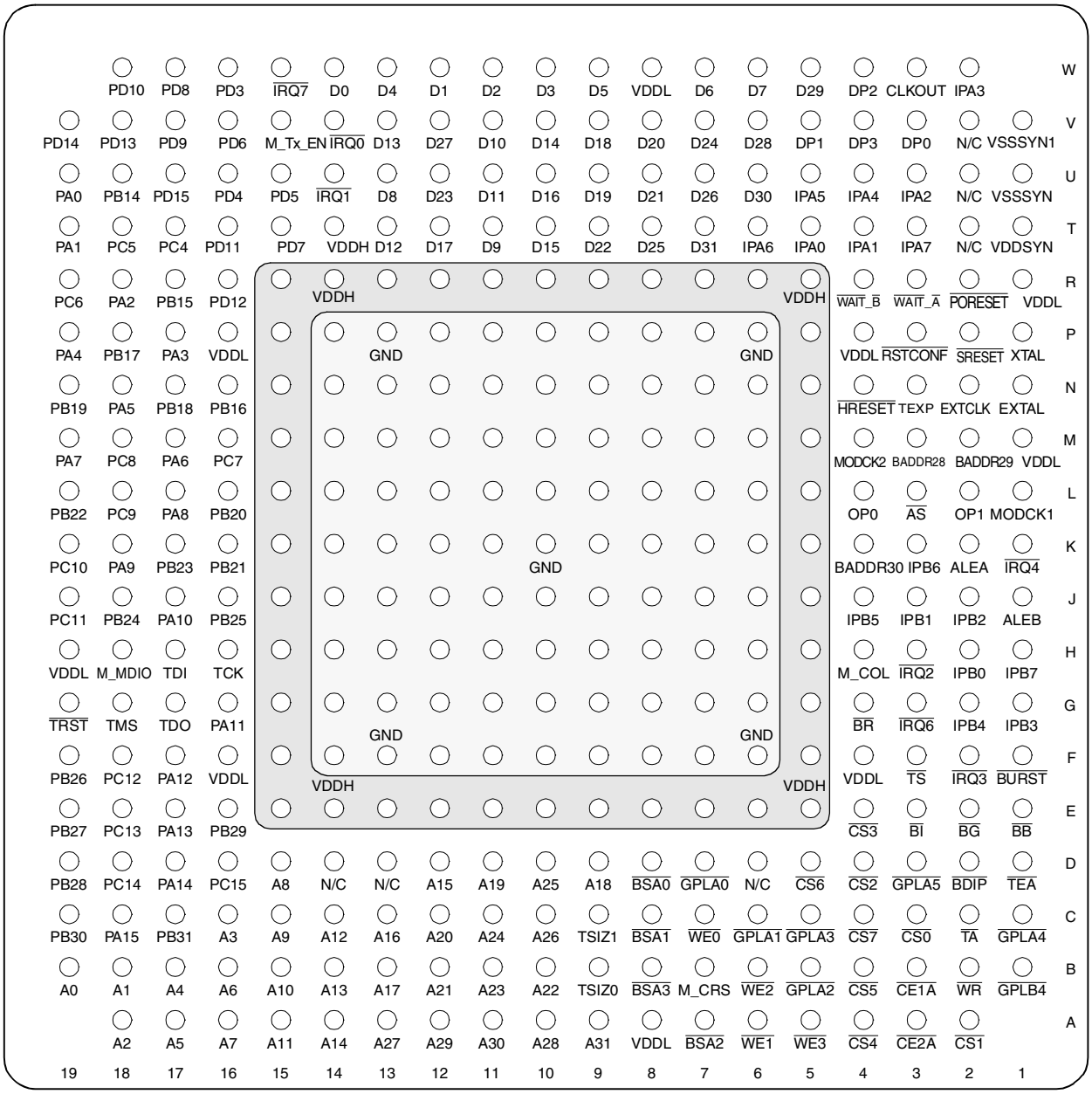



**Figure 78. Pinout of the PBGA Package**

Table 39 contains a list of the MPC866 input and output signals and shows multiplexing and pin assignments.

**Table 39. Pin Assignments**

| Name | Pin Number | Type |
|---|---|---|
| A[0:31] | B19, B18, A18, C16, B17, A17, B16, A16, D15, C15, B15, A15, C14, B14, A14, D12, C13, B13, D9, D11, C12, B12, B10, B11, C11, D10, C10, A13, A10, A12, A11, A9 | Bidirectional Three-state |
| TSIZ0<br>$\overline{\text{REG}}$ | B9 | Bidirectional Three-state |
| TSIZ1 | C9 | Bidirectional Three-state |
| RD/$\overline{\text{WR}}$ | B2 | Bidirectional Three-state |
| $\overline{\text{BURST}}$ | F1 | Bidirectional Three-state |
| $\overline{\text{BDIP}}$<br>$\overline{\text{GPL_B5}}$ | D2 | Output |
| $\overline{\text{TS}}$ | F3 | Bidirectional Active Pull-up |
| $\overline{\text{TA}}$ | C2 | Bidirectional Active Pull-up |
| $\overline{\text{TEA}}$ | D1 | Open-drain |
| $\overline{\text{BI}}$ | E3 | Bidirectional Active Pull-up |
| $\overline{\text{IRQ2}}$<br>$\overline{\text{RSV}}$ | H3 | Bidirectional Three-state |
| $\overline{\text{IRQ4}}$<br>$\overline{\text{KR}}$<br>$\overline{\text{RETRY}}$<br>SPKROUT | K1 | Bidirectional Three-state |
| $\overline{\text{CR}}$<br>$\overline{\text{IRQ3}}$ | F2 | Input |
| D[0:31] | W14, W12, W11, W10, W13, W9, W7, W6, U13, T11, V11, U11, T13, V13, V10, T10, U10, T12, V9, U9, V8, U8, T9, U12, V7, T8, U7, V12, V6, W5, U6, T7 | Bidirectional Three-state |
| DP0<br>$\overline{\text{IRQ3}}$ | V3 | Bidirectional Three-state |
| DP1<br>$\overline{\text{IRQ4}}$ | V5 | Bidirectional Three-state |
| DP2<br>$\overline{\text{IRQ5}}$ | W4 | Bidirectional Three-state |
| DP3<br>$\overline{\text{IRQ6}}$ | V4 | Bidirectional Three-state |

**Table 39. Pin Assignments (continued)**

| Name | Pin Number | Type |
|---|---|---|
| $\overline{BR}$ | G4 | Bidirectional |
| $\overline{BG}$ | E2 | Bidirectional |
| $\overline{BB}$ | E1 | Bidirectional<br>Active Pull-up |
| FRZ<br>$\overline{IRQ6}$ | G3 | Bidirectional |
| $\overline{IRQ0}$ | V14 | Input |
| $\overline{IRQ1}$ | U14 | Input |
| M_TX_CLK<br>$\overline{IRQ7}$ | W15 | Input |
| $\overline{CS}$[0:5] | C3, A2, D4, E4, A4, B4 | Output |
| $\overline{CS6}$<br>$\overline{CE1_B}$ | D5 | Output |
| $\overline{CS7}$<br>$\overline{CE2_B}$ | C4 | Output |
| $\overline{WE0}$<br>$\overline{BS_B0}$<br>$\overline{IORD}$ | C7 | Output |
| $\overline{WE1}$<br>$\overline{BS_B1}$<br>$\overline{IOWR}$ | A6 | Output |
| $\overline{WE2}$<br>$\overline{BS_B2}$<br>$\overline{PCOE}$ | B6 | Output |
| $\overline{WE3}$<br>$\overline{BS_B3}$<br>$\overline{PCWE}$ | A5 | Output |
| $\overline{BS_A}$[0:3] | D8, C8, A7, B8 | Output |
| $\overline{GPL_A0}$<br>$\overline{GPL_B0}$ | D7 | Output |
| $\overline{OE}$<br>$\overline{GPL_A1}$<br>$\overline{GPL_B1}$ | C6 | Output |
| $\overline{GPL_A}$[2:3]<br>$\overline{GPL_B}$[2:3]<br>$\overline{CS}$[2–3] | B5, C5 | Output |
| UPWAITA<br>$\overline{GPL_A4}$ | C1 | Bidirectional |

**Table 39. Pin Assignments (continued)**

| Name | Pin Number | Type |
|---|---|---|
| UPWAITB<br>GPL_B4 | B1 | Bidirectional |
| GPL_A5 | D3 | Output |
| PORESET | R2 | Input |
| RSTCONF | P3 | Input |
| HRESET | N4 | Open-drain |
| SRESET | P2 | Open-drain |
| XTAL | P1 | Analog Output |
| EXTAL | N1 | Analog Input (3.3V only) |
| CLKOUT | W3 | Output |
| EXTCLK | N2 | Input (3.3V only) |
| TEXP | N3 | Output |
| ALE_A<br>MII-TXD1 | K2 | Output |
| CE1_A<br>MII-TXD2 | B3 | Output |
| CE2_A<br>MII-TXD3 | A3 | Output |
| WAIT_A<br>SOC_Split[2] | R3 | Input |
| WAIT_B | R4 | Input |
| IP_A0<br>UTPB_Split0[2]<br>MII-RXD3 | T5 | Input |
| IP_A1<br>UTPB_Split1[2]<br>MII-RXD2 | T4 | Input |
| IP_A2<br>IOIS16_A<br>UTPB_Split2[2]<br>MII-RXD1 | U3 | Input |
| IP_A3<br>UTPB_Split3[2]<br>MII-RXD0 | W2 | Input |
| IP_A4<br>UTPB_Split4[2]<br>MII-RXCLK | U4 | Input |

**Table 39. Pin Assignments (continued)**

| Name | Pin Number | Type |
|---|---|---|
| IP_A5<br>UTPB_Split5[2]<br>MII-RXERR | U5 | Input |
| IP_A6<br>UTPB_Split6[2]<br>MII-TXERR | T6 | Input |
| IP_A7<br>UTPB_Split7[2]<br>MII-RXDV | T3 | Input |
| ALE_B<br>DSCK/AT1 | J1 | Bidirectional<br>Three-state |
| IP_B[0:1]<br>IWP[0:1]<br>VFLS[0:1] | H2, J3 | Bidirectional |
| IP_B2<br>$\overline{\text{IOIS16_B}}$<br>AT2 | J2 | Bidirectional<br>Three-state |
| IP_B3<br>IWP2<br>VF2 | G1 | Bidirectional |
| IP_B4<br>LWP0<br>VF0 | G2 | Bidirectional |
| IP_B5<br>LWP1<br>VF1 | J4 | Bidirectional |
| IP_B6<br>DSDI<br>AT0 | K3 | Bidirectional<br>Three-state |
| IP_B7<br>$\overline{\text{PTR}}$<br>AT3 | H1 | Bidirectional<br>Three-state |
| OP0<br>MII-TXD0<br>UtpClk_Split[2] | L4 | Bidirectional |
| OP1 | L2 | Output |
| OP2<br>MODCK1<br>$\overline{\text{STS}}$ | L1 | Bidirectional |

**Table 39. Pin Assignments (continued)**

| Name | Pin Number | Type |
|---|---|---|
| OP3<br>MODCK2<br>DSDO | M4 | Bidirectional |
| BADDR30<br>$\overline{\text{REG}}$ | K4 | Output |
| BADDR[28:29] | M3, M2 | Output |
| $\overline{\text{AS}}$ | L3 | Input |
| PA15<br>RXD1<br>RXD4 | C18 | Bidirectional |
| PA14<br>TXD1<br>TXD4 | D17 | Bidirectional<br>(Optional: Open-drain) |
| PA13<br>RXD2 | E17 | Bidirectional |
| PA12<br>TXD2 | F17 | Bidirectional<br>(Optional: Open-drain) |
| PA11<br>L1TXDB<br>RXD3 | G16 | Bidirectional<br>(Optional: Open-drain) |
| PA10<br>L1RXDB<br>TXD3 | J17 | Bidirectional<br>(Optional: Open-drain) |
| PA9<br>L1TXDA<br><br>RXD4 | K18 | Bidirectional<br>(Optional: Open-drain) |
| PA8<br>L1RXDA<br>TXD4 | L17 | Bidirectional<br>(Optional: Open-drain) |
| PA7<br>CLK1<br>L1RCLKA<br>BRGO1<br>TIN1 | M19 | Bidirectional |
| PA6<br>CLK2<br>$\overline{\text{TOUT1}}$ | M17 | Bidirectional |

**Table 39. Pin Assignments (continued)**

| Name | Pin Number | Type |
|---|---|---|
| PA5<br>CLK3<br>L1TCLKA<br>BRGO2<br>TIN2 | N18 | Bidirectional |
| PA4<br>CLK4<br>$\overline{\text{TOUT2}}$ | P19 | Bidirectional |
| PA3<br>CLK5<br>BRGO3<br>TIN3 | P17 | Bidirectional |
| PA2<br>CLK6<br>$\overline{\text{TOUT3}}$<br>L1RCLKB | R18 | Bidirectional |
| PA1<br>CLK7<br>BRGO4<br>TIN4 | T19 | Bidirectional |
| PA0<br>CLK8<br>$\overline{\text{TOUT4}}$<br>L1TCLKB | U19 | Bidirectional |
| PB31<br>$\overline{\text{SPISEL}}$<br>$\overline{\text{REJECT1}}$ | C17 | Bidirectional<br>(Optional: Open-drain) |
| PB30<br>SPICLK<br>$\overline{\text{RSTRT2}}$ | C19 | Bidirectional<br>(Optional: Open-drain) |
| PB29<br>SPIMOSI | E16 | Bidirectional<br>(Optional: Open-drain) |
| PB28<br>SPIMISO<br>BRGO4 | D19 | Bidirectional<br>(Optional: Open-drain) |
| PB27<br>I2CSDA<br>BRGO1 | E19 | Bidirectional<br>(Optional: Open-drain) |
| PB26<br>I2CSCL<br>BRGO2 | F19 | Bidirectional<br>(Optional: Open-drain) |

**Table 39. Pin Assignments (continued)**

| Name | Pin Number | Type |
|---|---|---|
| PB25<br>RXADDR3[2]<br>SMTXD1 | J16 | Bidirectional<br>(Optional: Open-drain) |
| PB24<br>TXADDR3[2]<br>SMRXD1 | J18 | Bidirectional<br>(Optional: Open-drain) |
| PB23<br>TXADDR2[2]<br>$\overline{\text{SDACK1}}$<br>$\overline{\text{SMSYN1}}$ | K17 | Bidirectional<br>(Optional: Open-drain) |
| PB22<br>TXADDR4[2]<br>$\overline{\text{SDACK2}}$<br>$\overline{\text{SMSYN2}}$ | L19 | Bidirectional<br>(Optional: Open-drain) |
| PB21<br>SMTXD2<br>L1CLKOB<br>PHSEL1[1]<br>TXADDR1[2] | K16 | Bidirectional<br>(Optional: Open-drain) |
| PB20<br>SMRXD2<br>L1CLKOA<br>PHSEL0[1]<br>TXADDR0[2] | L16 | Bidirectional<br>(Optional: Open-drain) |
| PB19<br>$\overline{\text{RTS1}}$<br>L1ST1 | N19 | Bidirectional<br>(Optional: Open-drain) |
| PB18<br>RXADDR4[2]<br>$\overline{\text{RTS2}}$<br>L1ST2 | N17 | Bidirectional<br>(Optional: Open-drain) |
| PB17<br>$\overline{\text{L1RQb}}$<br>L1ST3<br>$\overline{\text{RTS3}}$<br>PHREQ1[1]<br>RXADDR1[2] | P18 | Bidirectional<br>(Optional: Open-drain) |

**Table 39. Pin Assignments (continued)**

| Name | Pin Number | Type |
|---|---|---|
| PB16<br>$\overline{\text{L1RQa}}$<br>L1ST4<br>$\overline{\text{RTS4}}$<br>PHREQ0[1]<br>RXADDR0[2] | N16 | Bidirectional<br>(Optional: Open-drain) |
| PB15<br>BRGO3<br>TxClav<br>RxClav | R17 | Bidirectional |
| PB14<br>RXADDR2[2]<br>$\overline{\text{RSTRT1}}$ | U18 | Bidirectional |
| PC15<br>$\overline{\text{DREQ0}}$<br>$\overline{\text{RTS1}}$<br>L1ST1<br>RxClav<br>TxClav | D16 | Bidirectional |
| PC14<br>$\overline{\text{DREQ1}}$<br>$\overline{\text{RTS2}}$<br>L1ST2 | D18 | Bidirectional |
| PC13<br>$\overline{\text{L1RQb}}$<br>L1ST3<br>RTS3 | E18 | Bidirectional |
| PC12<br>$\overline{\text{L1RQa}}$<br>L1ST4<br>RTS4 | F18 | Bidirectional |
| PC11<br>$\overline{\text{CTS1}}$ | J19 | Bidirectional |
| PC10<br>$\overline{\text{CD1}}$<br>$\overline{\text{TGATE1}}$ | K19 | Bidirectional |
| PC9<br>$\overline{\text{CTS2}}$ | L18 | Bidirectional |
| PC8<br>$\overline{\text{CD2}}$<br>$\overline{\text{TGATE2}}$ | M18 | Bidirectional |

**Table 39. Pin Assignments (continued)**

| Name | Pin Number | Type |
|---|---|---|
| PC7<br>$\overline{\text{CTS3}}$<br>L1TSYNCB<br>$\overline{\text{SDACK2}}$ | M16 | Bidirectional |
| PC6<br>$\overline{\text{CD3}}$<br>L1RSYNCB | R19 | Bidirectional |
| PC5<br>$\overline{\text{CTS4}}$<br>L1TSYNCA<br>SDACK1 | T18 | Bidirectional |
| PC4<br>$\overline{\text{CD4}}$<br>L1RSYNCA | T17 | Bidirectional |
| PD15<br>L1TSYNCA<br>MII-RXD3<br>UTPB0 | U17 | Bidirectional |
| PD14<br>L1RSYNCA<br>MII-RXD2<br>UTPB1 | V19 | Bidirectional |
| PD13<br>L1TSYNCB<br>MII-RXD1<br>UTPB2 | V18 | Bidirectional |
| PD12<br>L1RSYNCB<br>MII-MDC<br>UTPB3 | R16 | Bidirectional |
| PD11<br>RXD3<br>MII-TXERR<br>$\overline{\text{RXENB}}$ | T16 | Bidirectional |
| PD10<br>TXD3<br>MII-RXD0<br>$\overline{\text{TXENB}}$ | W18 | Bidirectional |

**Table 39. Pin Assignments (continued)**

| Name | Pin Number | Type |
|---|---|---|
| PD9<br>RXD4<br>MII-TXD0<br>UTPCLK | V17 | Bidirectional |
| PD8<br>TXD4<br>MII-MDC<br>MII-RXCLK | W17 | Bidirectional |
| PD7<br>$\overline{\text{RTS3}}$<br>MII-RXERR<br>UTPB4 | T15 | Bidirectional |
| PD6<br>$\overline{\text{RTS4}}$<br>MII-RXDV<br>UTPB5 | V16 | Bidirectional |
| PD5<br>$\overline{\text{REJECT2}}$<br>MII-TXD3<br>UTPB6 | U15 | Bidirectional |
| PD4<br>$\overline{\text{REJECT3}}$<br>MII-TXD2<br>UTPB7 | U16 | Bidirectional |
| PD3<br>$\overline{\text{REJECT4}}$<br>MII-TXD1<br>SOC | W16 | Bidirectional |
| TMS | G18 | Input |
| TDI<br>DSDI | H17 | Input |
| TCK<br>DSCK | H16 | Input |
| $\overline{\text{TRST}}$ | G19 | Input |
| TDO<br>DSDO | G17 | Output |
| MII_CRS | B7 | Input |
| MII_MDIO | H18 | Bidirectional |
| MII_TXEN | V15 | Output |

**Table 39. Pin Assignments (continued)**

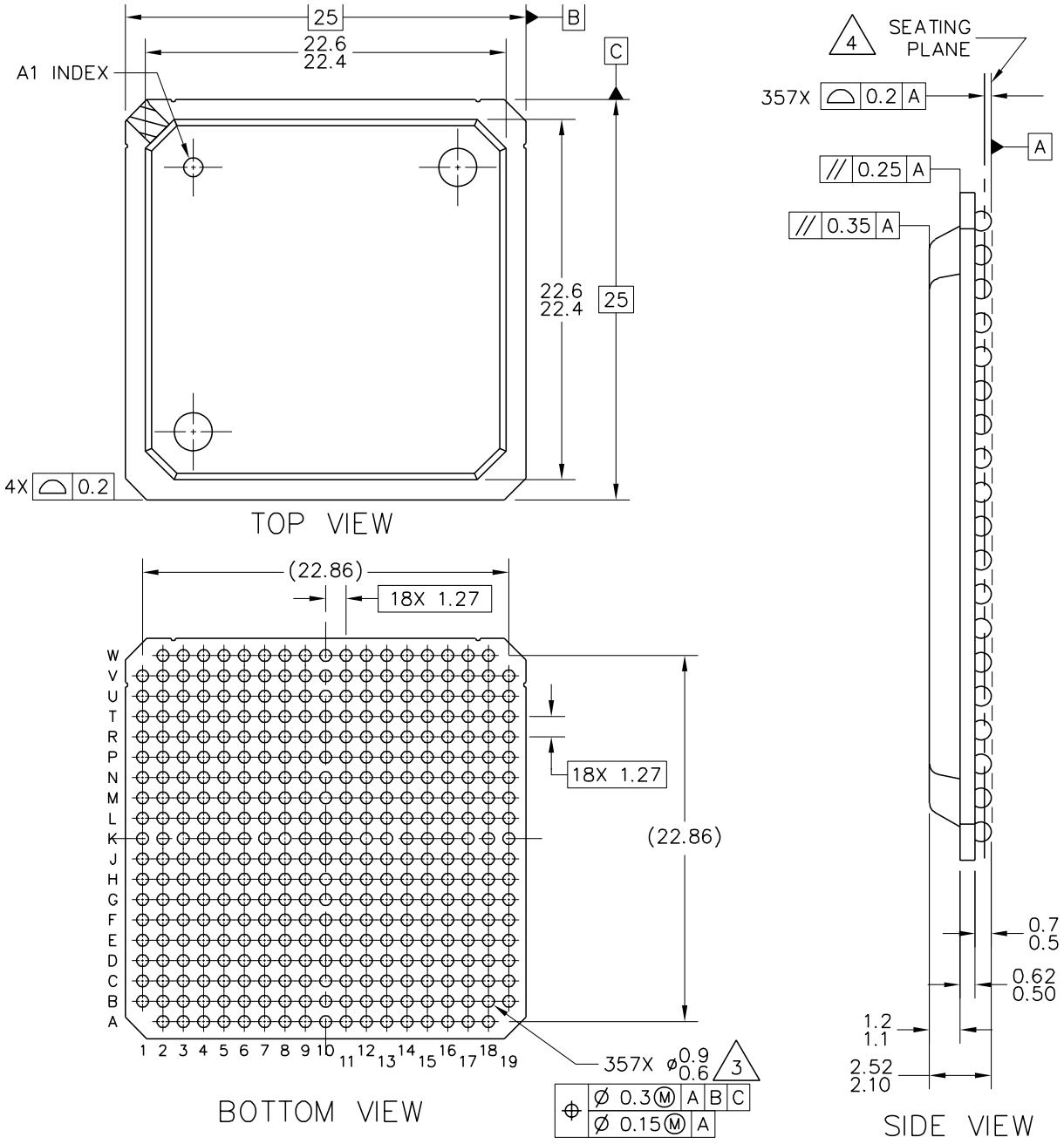
| Name | Pin Number | Type |
|---|---|---|
| MII_COL | H4 | Input |
| VSSSYN1 | V1 | PLL analog VDD and GND |
| VSSSYN | U1 | Power |
| VDDSYN | T1 | Power |
| GND | F6, F7, F8, F9, F10, F11, F12, F13, F14, G6, G7, G8, G9, G10, G11, G12, G13, G14, H6, H7, H8, H9, H10, H11, H12, H13, H14, J6, J7, J8, J9, J10, J11, J12, J13, J14, K6, K7, K8, K9, K10, K11, K12, K13, K14, L6, L7, L8, L9, L10, L11, L12, L13, L14, M6, M7, M8, M9, M10, M11, M12, M13, M14, N6, N7, N8, N9, N10, N11, N12, N13, N14, P6, P7, P8, P9, P10, P11, P12, P13, P14 | Power |
| VDDL | A8, M1, W8, H19, F4, F16, P4, P16, R1 | Power |
| VDDH | E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P5, P15, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, T14 | Power |
| N/C | D6, D13, D14, U2, V2, T2 | No-connect |

1 Classic SAR mode only

2 ESAR mode only

## 15.2 Mechanical Dimensions of the PBGA Package

For more information on the printed-circuit board layout of the PBGA package, including thermal via design and suggested pad layout, please refer to *Plastic Ball Grid Array Application Note* (order number: AN1231/D) available from your local Freescale sales office. Figure 79 shows the mechanical dimensions of the PBGA package.




**Note:** Solder sphere composition for MPC866XZP, MPC859PZP, MPC859DSLZP, and MPC859TZP is 62%Sn 36%Pb 2%Ag

**Figure 79. Mechanical Dimensions and Bottom Surface Nomenclature of the PBGA Package**

# 16 Document Revision History

Table 40 lists significant changes between revisions of this document.

**Table 40. Document Revision History**

| Revision Number | Date | Substantive Changes |
|---|---|---|
| 0 | 5/2002 | Initial revision |
| 1 | 11/2002 | Added the 5-V tolerant pins, new package dimensions, and other changes. |
| 1.1 | 4/2003 | Added the Spec. B1d and changed spec. B1a. Added the Note Solder sphere composition for MPC866XZP, MPC859DSLZP, and MPC859TZP is 62%Sn 36%Pb 2%Ag to Figure 15-79. |
| 1.2 | 4/2003 | Added the MPC859P. |
| 1.3 | 5/2003 | Changed the SPI Master Timing Specs. 162 and 164. |
| 1.4 | 7-8/2003 | • Added TxClav and RxClav to PB15 and PC15. Changed B28a through B28d and B29b to show that TRLX can be 0 or 1.<br>• Added nontechnical reformatting. |
| 1.5 | 3/14/2005 | • Updated document template. |
| 2 | 2/10/2006 | • Updated orderable parts table. |

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