THE DATASHEET OF

AX250-PQ208M

www.win-source.net 0086-755-83957316

Axcelerator Family FPGAs Datasheet

Introduction

This datasheet covers Antifuse family of FPGAs and Axcelerator devices, which provides exceptional design security and outstanding performance at densities of up to two million equivalent system gates. Axcelerator devices, which use our AX architecture, have a number of system-level capabilities including segmentable clocks, PLLs, chip-wide highway routing, embedded SRAM (with embedded FIFO control logic), and the capacity to carry logic. Axcelerator devices, which are developed using a CMOS antifuse process technique based on 0.15 µm and seven layers of metal, provide a higher level of performance that was previously limited to ASIC technology.

Benefits

The following are the benefits of Axcelerator devices:

- 350+ MHz System Performance
- 500+ MHz Internal Performance
- High-Performance Embedded FIFOs
- 700 Mb/s LVDS Capable I/Os

Specifications

The following are the specifications of the Axcelerator devices:

- Up to 2 Million Equivalent System Gates
- Up to 684 I/Os
- Up to 10,752 Dedicated Flip-Flops
- Up to 295 kbits Embedded SRAM/FIFO
- Manufactured on Advanced 0.15 µm CMOS Antifuse Process Technology, 7 Layers of Metal

Features

The following are the features of the Axcelerator devices:

- Single-Chip, Nonvolatile Solution
- Up to 100% Resource Utilization with 100% Pin Locking
- 1.5V Core Voltage for Low Power
- Footprint Compatible Packaging
- Flexible, Multi-Standard I/Os:
  - 1.5V, 1.8V, 2.5V, 3.3V mixed voltage operation
  - Bank-selectable I/Os—8 banks per chip
  - Single-ended I/O standards: LVTTL, LVCMOS, 3.3V PCI, and 3.3V PCI-X
  - Differential I/O standards: LVPECL and LVDS

© 2024 Microchip Technology Inc. and its subsidiaries

  - Voltage-referenced I/O standards: GTL+, HSTL Class 1, SSTL2 Class 1 and 2, and SSTL3 Class 1 and 2
  - Registered I/Os
  - Hot-swap compliant I/Os (except PCI)
  - Programmable slew rate and drive strength on outputs
  - Programmable delay and weak pull-up/pull-down circuits on inputs
- Embedded Memory:
  - Variable-aspect 4,608-bit RAM blocks (x1, x2, x4, x9, x18, and x36 organizations available)
  - Independent, width-configurable read and write ports
  - Programmable embedded FIFO control logic
- Segmentable Clock Resources
- Embedded Phase-Locked Loop:
  - 14–200 MHz input range
  - Frequency synthesis capabilities up to 1 GHz
- Deterministic and User-Controllable Timing
- Unique In-System Diagnostic and Debug Capability with Microchip Silicon Explorer II
- Boundary-Scan Testing Compliant with IEEE Standard 1149.1 (JTAG)
- FuseLock™ Programming Technology Protects Against Reverse Engineering and Design Theft

The following table shows the Axcelerator family product profile.

Table 1. Axcelerator Family Product Profile

Device		AX125[1]	AX250	AX500	AX1000	AX2000
Capacity (in equivalent system gates)	Typical Gates	125,00 82,000	250,000 154,000	500,000 286,000	1,000,000 612,000	2,000,000 1,060,000
Modules	Register (R-cells)	672	1,408	2,688	6,048	10,752
	Combinatorial (C-cells)	1,344	2,816	5,376	12,096	21,504
	Maximum Flip-Flops	1,344	2,816	5,376	12,096	21,504
Embedded RAM/ FIFO	Number of Core RAM Blocks	4	12	16	36	64
	Total Bits of Core RAM	18,432	55,296	73,728	165,888	294,912
Clocks (segmentable)	Hardwired	4	4	4	4	4
	Routed	4	4	4	4	4
PLLs	—	8	8	8	8	8
I/Os	I/O Banks	8	8	8	8	8
	Maximum User I/Os	168	248	336	516	684
	Maximum LVDS Channels	84	124	168	258	342
	Total I/O Registers	504	744	1,008	1,548	2,052
Package	PQ	—	208	208	—	—
	BG	—	—	—	729[2]	—
	FG	256, 324	256, 484	484, 676[2]	484, 676, 896[2]	896, 1,152[2]
	CQ	—	208, 352	208, 352[2]	352	256, 352
	CG	—	—	—	624[2]	624

© 2024 Microchip Technology Inc. and its subsidiaries

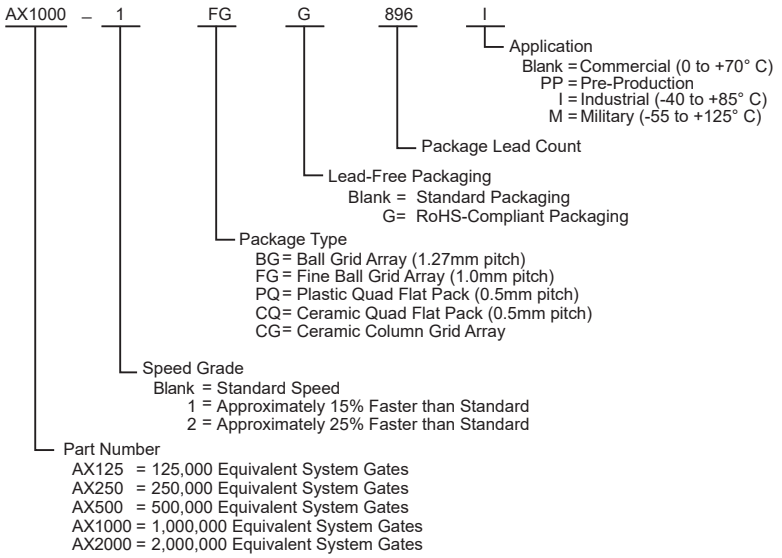
Notes:

1. Device has been discontinued.
2. Package has been discontinued.

Ordering Information

The following figure shows ordering information.

Figure 1. Ordering Information



Device Resources

The following table lists the device resources.

Table 2. Device Resources

User I/Os (Including Clock Buffers)					
Package	AX125[1]	AX250	AX500	AX1000	AX2000
PQ208	—	115	115	—	—
CQ208	—	115	115	—	—
CQ256	—	—	—	—	136
FG256	138	138	—	—	—
FG324	168	—	—	—	—
CQ352	—	198	198[2]	198	198
FG484	—	248	317	317	—
CG624	—	—	—	418[2]	418
FG676	—	—	336[2]	418	—
BG729	—	—	—	516[2]	—
FG896	—	—	—	516[2]	586
FG1152	—	—	—	—	684[2]

© 2024 Microchip Technology Inc. and its subsidiaries

Notes:

1. Device has been discontinued.
2. Package has been discontinued.
3. The FG256, FG324, and FG484 are footprint compatible with one another. The FG676, FG896, and FG1152 are also footprint compatible with one another.

Axcelerator Family Device Status

The following table lists the status of axcelerator family devices.

Table 3. Axcelerator Family Device Status

Axcelerator® Devices	Status
AX125	Discontinued
AX250	Production
AX500	Production
AX1000	Production
AX2000	Production

Temperature Grade Offerings

The following table lists the temperature grade offerings.

Table 4. Temperature Grade Offerings

Package	AX125[1]	AX250	AX500	AX1000	AX2000
PQ208	—	C[2], I[2], M	C, I, M	—	—
CQ208	—	M	M	—	—
CQ256	—	—	—	—	M
FG256	C, I	C, I, M	—	—	—
FG324	C, I	—	—	—	—
CQ352	—	M	M[2]	M	M
FG484	—	C, I, M	C, I, M	C, I, M	—
CG624	—	—	—	M[2]	M
FG676	—	—	C[2], I[2], M[2]	C, I, M	—
BG729	—	—	—	C[2], I[2], M[2]	—
FG896	—	—	—	C[2], I[2], M[2]	C, I, M
FG1152	—	—	—	—	C[2], I[2], M[2]

Notes:

- C = Commercial
- I = Industrial
- M = Military

Notes:

1. Device has been discontinued.
2. Package has been discontinued.

Speed Grade and Temperature Grade Matrix

The following table lists the speed grade and temperature grade matrix.

© 2024 Microchip Technology Inc. and its subsidiaries

Table 5. Speed Grade and Temperature Grade Matrix

Temperature Grade	Std	–1	–2
C	✓	✓	✓
I	✓	✓	✓
M	✓	✓	—

Notes:

- C = Commercial
- I = Industrial
- M = Military

Packaging Data

See the following documents located on the Microchip SoC Products Group website for additional packaging information.

- Package Mechanical Drawings
- Package Thermal Characteristics and Weights
- Hermatic Package Mechanical Information

© 2024 Microchip Technology Inc. and its subsidiaries

Table of Contents

Introduction 1

Benefits 1
Specifications 1
Features 1
Ordering Information 3
Device Resources 3
Axcelerator Family Device Status 4
Temperature Grade Offerings 4
Speed Grade and Temperature Grade Matrix 4
Packaging Data 5

1. General Description 8
   1.1. Device Architecture 8
   1.2. Design Environment 13
   1.3. Summary 15
   1.4. Related Documents 15

2. Electrical Specifications 16
   2.1. Operating Conditions 16
   2.2. Thermal Characteristics 20
   2.3. I/O Specifications 22
   2.4. Voltage-Referenced I/O Standards 49
   2.5. Differential Standards 57
   2.6. Module Specifications 60
   2.7. Routing Specifications 66
   2.8. Global Resources 70
   2.9. Axcelerator Clock Management System 78
   2.10. Embedded Memory 87
   2.11. Other Architectural Features 103
   2.12. Programming 106

3. Package Pin Assignments 107
   3.1. BG729 107
   3.2. FG256 124
   3.3. FG324 137
   3.4. FG484 146
   3.5. FG676 180
   3.6. FG896 212
   3.7. FG1152 254
   3.8. PQ208 282
   3.9. CQ208 292
   3.10. CQ256 303
   3.11. CQ352 310
   3.12. CG624 344

4. Revision History 375

Microchip Information 380

© 2024 Microchip Technology Inc. and its subsidiaries

The Microchip Website.....380
Product Change Notification Service.....380
Customer Support.....380
Microchip Devices Code Protection Feature.....380
Legal Notice.....380
Trademarks.....381
Quality Management System.....382
Worldwide Sales and Service.....383

© 2024 Microchip Technology Inc. and its subsidiaries

1. General Description

Axcelerator devices offer high performance at densities of up to two million equivalent system gates. Based upon the Microchip AX architecture, Axcelerator has several system-level features such as embedded SRAM (with complete FIFO control logic), PLLs, segmentable clocks, chip-wide highway routing, and carry logic.

1.1 Device Architecture

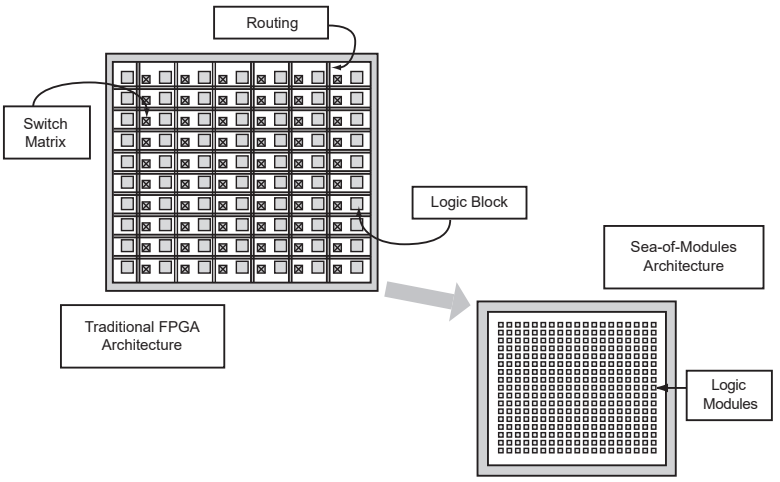
AX architecture, derived from the highly-successful SX-A sea-of-modules architecture, has been designed for high performance and total logic module utilization (see Figure 1-1). Unlike in traditional FPGAs, the entire floor of the Axcelerator device is covered with a grid of logic modules, with virtually no chip area lost to interconnect elements or routing.

1.1.1 Programmable Interconnect Element

The Axcelerator family uses a patented metal-to-metal antifuse programmable interconnect element that resides between the upper two layers of metal (see the following figures). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on traditional FPGAs) and enables the efficient sea-of-modules architecture. The antifuses are normally open circuit and, when programmed, form a permanent, passive, low-impedance connection, leading to the fastest signal propagation in the industry. In addition, the extremely small size of these interconnect elements gives the Axcelerator family abundant routing resources.

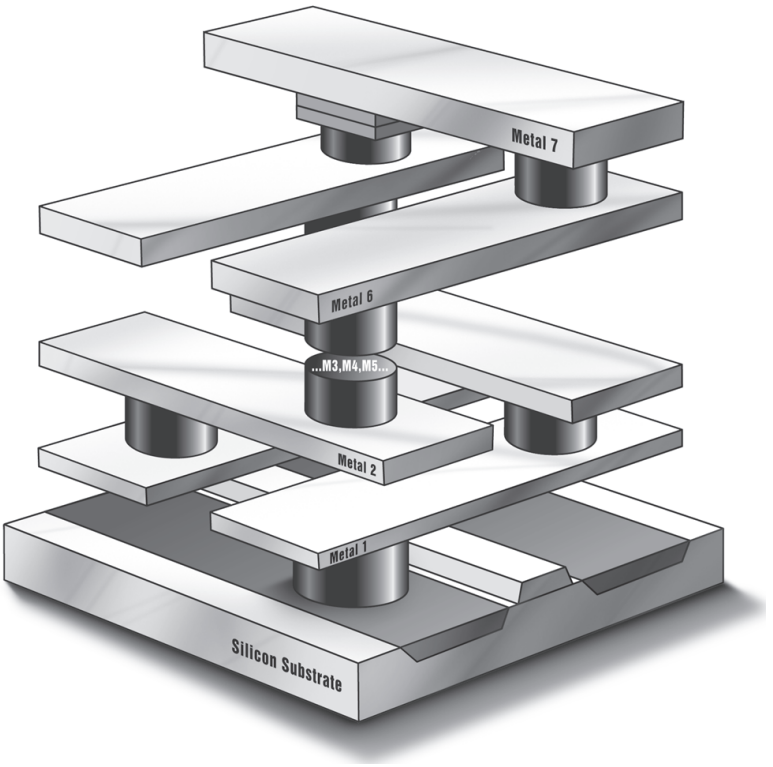
The very nature of Microchip's nonvolatile antifuse technology provides excellent protection against design pirating and cloning (FuseLock technology). Typical cloning attempts are impossible (even if the security fuse is left unprogrammed), as no bitstream or programming file is ever downloaded or stored in the device. Reverse engineering is virtually impossible due to the difficulty of trying to distinguish between programmed and unprogrammed antifuses and also due to the programming methodology of antifuse devices (see Security).

Figure 1-1. Sea-of-Modules Comparison



© 2024 Microchip Technology Inc. and its subsidiaries

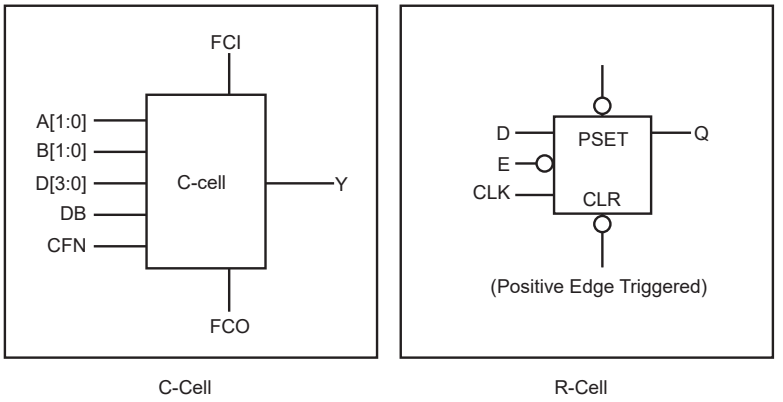
Figure 1-2. Axcelerator Family Interconnect Elements



1.1.2 Logic Modules

Microchip's Axcelerator family provides two types of logic modules: The register cell (R-cell) and the combinatorial cell (C-cell). The Axcelerator device can implement more than 4,000 combinatorial functions of up to five inputs (see the following figure).

Figure 1-3. AX C-Cell and R-Cell



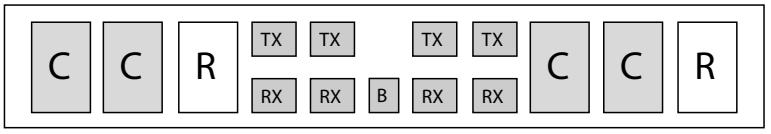
The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and active-low enable control signals (see the preceeding figure). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility (for example, easy mapping of dual-data-rate functions into the FPGA), while conserving valuable clock resources. The clock source for the R-cell can be chosen from the hardwired clocks, routed clocks, or internal logic.

Two C-cells, a single R-cell, two Transmit (TX), and two Receive (RX) routing buffers form a Cluster, while two Clusters comprise a SuperCluster (see the following figure). Each SuperCluster also

© 2024 Microchip Technology Inc. and its subsidiaries

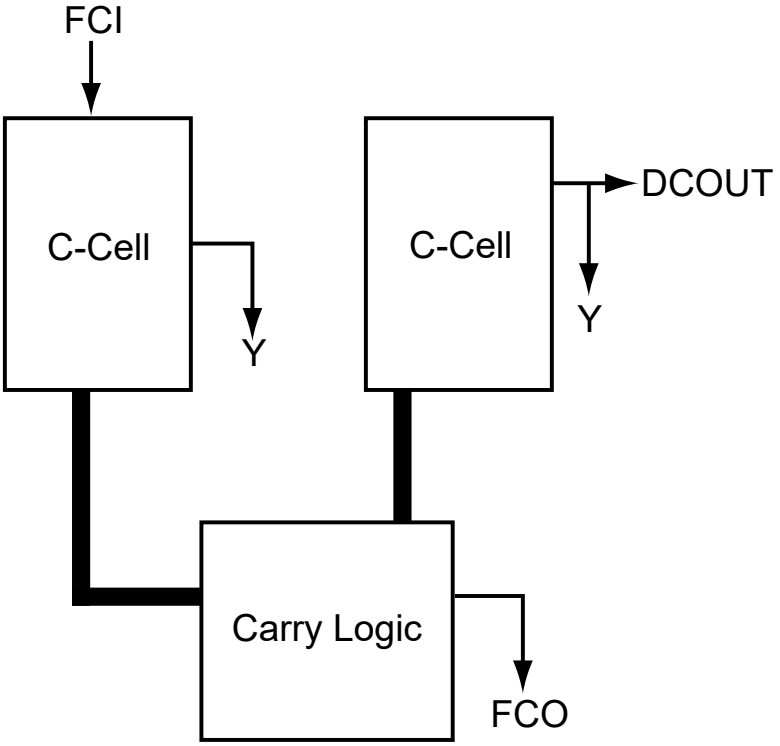
contains an independent Buffer (B) module, which supports buffer insertion on high-fanout nets by the place-and-route tool, minimizing system delays while improving logic utilization.

Figure 1-4. AX SuperCluster



The logic modules within the SuperCluster are arranged so that two combinatorial modules are side by side, giving a C–C–R – C–C–R pattern to the SuperCluster. This C–C–R pattern enables efficient implementation (minimum delay) of two-bit carry logic for improved arithmetic performance (see the following figure).

Figure 1-5. AX 2-Bit Carry Logic



The AX architecture is fully fracturable, meaning that if one or more of the logic modules in a SuperCluster are used by a particular signal path, the other logic modules are still available for use by other paths.

At the chip level, SuperClusters are organized into core tiles, which are arrayed to build up the full chip. For example, the AX1000 is composed of a 3x3 array of nine core tiles. The array of core tiles is surrounded by blocks of I/O Clusters and the I/O bank ring (see the following table). Each core tile consists of an array of 336 SuperClusters and four SRAM blocks (176 SuperClusters and three SRAM blocks for the AX250).

The following table shows the number of core tiles per device.

Table 1-1. Number of Core Tiles per Device

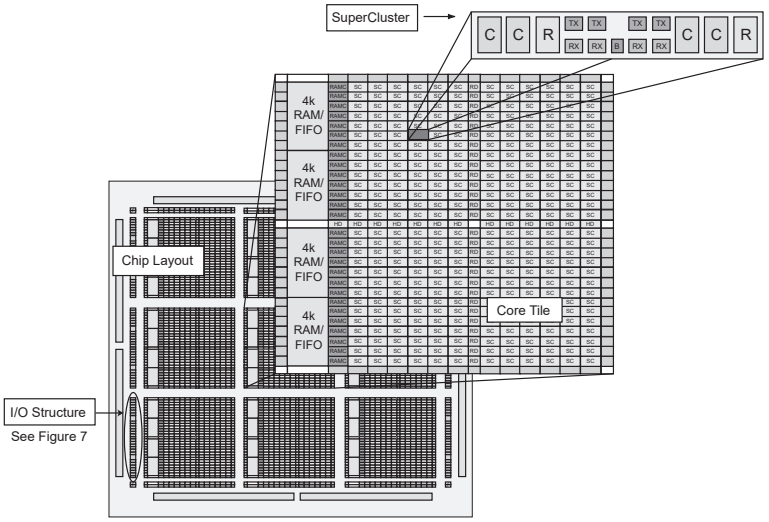
Device	Number of Core Tiles
AX125	1 regular tile

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued	
Device	**Number of Core Tiles**
AX250	4 smaller tiles
AX500	4 regular tiles
AX1000	9 regular tiles
AX2000	16 regular tiles

The SRAM blocks are arranged in a column on the west side of the tile (see the following figure).

Figure 1-6. AX Device Architecture (AX1000 shown)



1.1.3 Embedded Memory

As mentioned earlier, each core tile has either three (in a smaller tile) or four (in the regular tile) embedded SRAM blocks along the west side, and each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2, or 4kx1 bits. The individual blocks have separate read and write ports that can be configured with different bit widths on each port. For example, data can be written in by eight and read out by one.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using core logic modules. The FIFO width and depth are programmable. The FIFO also features programmable ALMOST-EMPTY (AEMPTY) and ALMOST-FULL (AFULL) flags in addition to the normal EMPTY and FULL flags. In addition to the flag logic, the embedded FIFO control unit also contains the counters necessary for the generation of the read and write address pointers as well as control circuitry to prevent metastability and erroneous operation. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

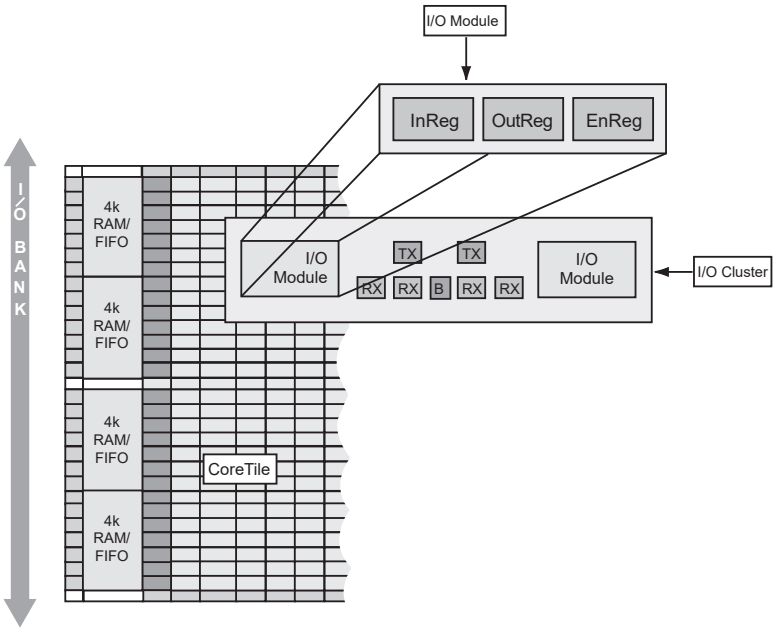
1.1.4 I/O Logic

The Axcelerator family of FPGAs features a flexible I/O structure, supporting a range of mixed voltages with its bank-selectable I/Os: 1.5V, 1.8V, 2.5V, and 3.3V. In all, Axcelerator FPGAs support at least 14 different I/O standards (single-ended, differential, and voltage-referenced). The I/Os are organized into banks with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported (For more information, see User I/Os2). All I/O standards are available in each bank.

Each I/O module has an input register (InReg), an output register (OutReg), and an enable register (EnReg) (see the following figure). An I/O Cluster includes two I/O modules, four RX modules, two TX modules, and a buffer (B) module.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 1-7. I/O Cluster Arrangement



1.1.5 Routing

The AX hierarchical routing structure ties the logic modules, the embedded memory blocks, and the I/O modules together (see the following figure). At the lowest level, in and between SuperClusters, there are three local routing structures: FastConnect, DirectConnect, and CarryConnect routing. DirectConnects provide the highest performance routing inside the SuperClusters by connecting a C-cell to the adjacent R-cell. DirectConnects do not require an antifuse to make the connection and achieve a signal propagation time of less than 0.1 ns.

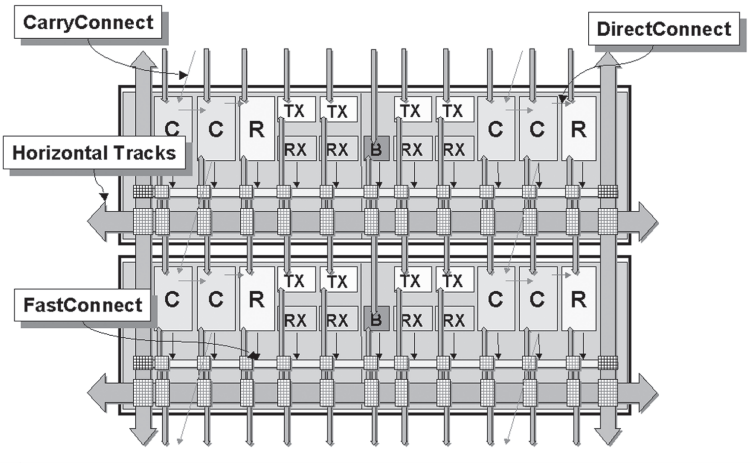
FastConnects provide high-performance, horizontal routing inside the SuperCluster and vertical routing to the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum routing delay of 0.4 ns.

CarryConnects are used for routing carry logic between adjacent SuperClusters. They connect the FCO output of one two-bit, C-cell carry logic to the FCI input of the two-bit, C-cell carry logic of the SuperCluster below it. CarryConnects do not require an antifuse to make the connection and achieve a signal propagation time of less than 0.1 ns.

The next level contains the core tile routing. Over the SuperClusters within a core tile, both vertical and horizontal tracks run across rows or columns, respectively. At the chip level, vertical and horizontal tracks extend across the full length of the device, both north to south and east to west. These tracks are composed of highway routing that extend the entire length of the device (segmented at core tile boundaries), as well as segmented routing of varying lengths.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 1-8. AX Routing Structures



1.1.6 Global Resources

Each family member has three types of global signals available to the designer: HCLK, CLK, and GCLR/GPSET. There are four Hardwired Clocks (HCLK) per device that can directly drive the clock input of each R-cell. Each of the four Routed Clocks (CLK) can drive the clock, clear, preset, or enable pin of an R-cell or any input of a C-cell (see Figure 1-3).

Global Clear (GCLR) and Global Preset (GPSET) drive the clear and preset inputs of each R-cell as well as each I/O Register on a chip-wide basis at power-up.

Each HCLK and CLK has an associated analog PLL (a total of eight per chip). Each embedded PLL can be used for clock delay minimization, clock delay adjustment, or clock frequency synthesis. The PLL is capable of operating with input frequencies ranging from 14 MHz to 200 MHz and can generate output frequencies between 20 MHz and 1 GHz. The clock can be either divided or multiplied by factors ranging from 1 to 64. Additionally, multiply and divide settings can be used in any combination as long as the resulting clock frequency is between 20 MHz and 1 GHz. Adjacent PLLs can be cascaded to create complex frequency combinations.

The PLL can be used to introduce either a positive or a negative clock delay of up to 3.75 ns in 250 ps increments. The reference clock required to drive the PLL can be derived from three sources: external input pad (either single-ended or differential), internal logic, or the output of an adjacent PLL.

1.1.7 Low Power (LP) Mode

The AX architecture was created for high-performance designs but also includes a low power mode (activated via the LP pin). When the low power mode is activated, I/O banks can be disabled (inputs disabled and outputs tristated), and PLLs can be placed in a power-down mode. All internal register states are maintained in this mode. Furthermore, individual I/O banks can be configured to opt out of the LP mode, thereby giving the designer access to critical signals while the rest of the chip is in low power mode.

The power can be further reduced by providing an external voltage source (VPUMP) to the device to bypass the internal charge pump. For more information, see Low Power Mode.

1.2 Design Environment

The Axcelerator family of FPGAs is fully supported by both Microchip's Libero® Integrated Design Environment and Designer FPGA Development software. Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design

© 2024 Microchip Technology Inc. and its subsidiaries

in a single environment (see the Libero IDE Flow diagram located on the Microchip website). Libero IDE includes Synplify® Actel Edition (AE) from Synplicity®, ViewDraw® AE from Mentor Graphics®, ModelSim® HDL Simulator from Mentor Graphics, WaveFormer Lite™ AE from SynaptiCAD®, and Designer software from Microchip.

Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes the following:

- Timer: a world-class integrated static timing analyzer and constraints editor which support timing-driven place-and-route
- NetlistViewer: a design netlist schematic viewer
- ChipPlanner: a graphical floorplanner viewer and editor
- SmartPower: allows the designer to quickly estimate the power consumption of a design
- PinEditor: a graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor: displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, Microchip's back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microchip's integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors, such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows® and UNIX® operating systems.

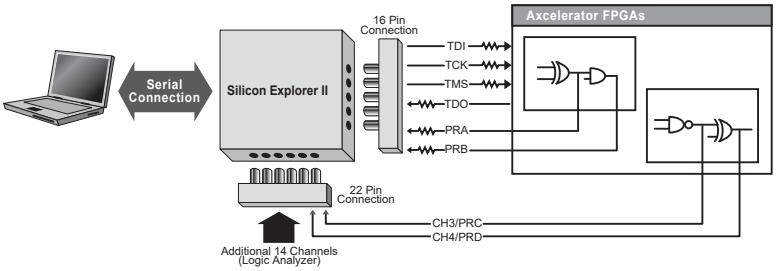
1.2.1 Programming

Programming support is provided through Silicon Sculptor II, a single-site programmer driven through a PC-based GUI. In addition, BP Microsystems offers multi-site programmers that provide qualified support for Microchip devices. Factory programming is available for high-volume production needs.

1.2.2 In-System Diagnostic and Debug Capabilities

The Axcelerator family of FPGAs includes internal probe circuitry, allowing the designer to dynamically observe and analyze any signal inside the FPGA without disturbing normal device operation (see the following figure).

Figure 1-9. Probe Setup



Up to four individual signals can be brought out to dedicated probe pins (PRA/B/C/D) on the device. The probe circuitry is accessed and controlled through Silicon Explorer II, Microchip's integrated verification and logic analysis tool that attaches to the serial port of a PC and communicates with the FPGA through the JTAG port. For more information, see Silicon Explorer II Probe Interface.

© 2024 Microchip Technology Inc. and its subsidiaries

1.3 Summary

Microchip's Axcelerator family of FPGAs extends the successful SX-A architecture, adding embedded RAM/FIFOs, PLLs, and high-speed I/Os. With the support of a suite of robust software tools, design engineers can incorporate high gate counts and fixed pins into an Axcelerator design yet still achieve high performance and efficient device utilization.

1.4 Related Documents

1.4.1 Application Notes

The following is the list of related application notes:

- Simultaneous Switching Noise and Signal Integrity
- Axcelerator Family PLL and Clock Management
- Implementation of Security in Actel Antifuse FPGAs

1.4.2 User's Guides and Manuals

The following is the list of related user's guides and manuals:

- Antifuse Macro Library Guide
- SmartGen, FlashROM, Analog System Builder, and Flash Memory System Builder
- Silicon Sculptor II User's Guide

1.4.3 White Paper

The following is the list of related white papers:

- Design Security in Nonvolatile Flash and Antifuse FPGAs
- Understanding Actel Antifuse Device Security

1.4.4 Libero

The following is list of related Libero design suite:

- Libero SoC Design Suite
- Libero® SoC Design Suite Brochure

© 2024 Microchip Technology Inc. and its subsidiaries

2. Electrical Specifications

This section decribes the detailed electrical specifications.

2.1 Operating Conditions

The following table lists the absolute maximum ratings of Axcelerator devices. Stresses beyond the ratings may cause permanent damage to the device. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability.

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCCA	DC core supply voltage	–0.3 to 1.7	V
VCCI	DC I/O supply voltage	–0.3 to 3.75	V
VREF	DC I/O reference voltage	–0.3 to 3.75	V
VI	Input voltage	–0.5 to 4.1	V
VO	Output voltage	–0.5 to 3.75	V
TSTG	Storage temperature	–60 to +150	°C
VCCDA[1]	Supply voltage for differential I/Os	–0.3 to 3.75	V

Note:

1. Should be the maximum of all VCCI.

Devices should not be operated outside the recommendations given in the following table.

Table 2-2. Recommended Operating Conditions

Parameter Range	Commercial	Industrial	Military	Units
Junction temperature	0 to +70	–40 to +85	–55 to +125	°C
1.5V Core Supply voltage	1.425 to 1.575	1.425 to 1.575	1.425 to 1.575	V
1.5V I/O Supply voltage	1.425 to 1.575	1.425 to 1.575	1.425 to 1.575	V
1.8V I/O Supply voltage	1.71 to 1.89	1.71 to 1.89	1.71 to 1.89	V
2.5V I/O Supply voltage	2.375 to 2.625	2.375 to 2.625	2.375 to 2.625	V
3.3V I/O Supply voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VCCDA Supply voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V
VPUMP Supply voltage	3.0 to 3.6	3.0 to 3.6	3.0 to 3.6	V

2.1.1 Power-Up/Down Sequence

All Axcelerator I/Os are tristated during power-up until normal device operating conditions are reached, when I/Os enter user mode. VCCDA should be powered up before (or coincidentally with) VCCA and VCCI to ensure the behavior of user I/Os at system start-up. Conversely, VCCDA should be powered down after (or coincidentally with) VCCA and VCCI. The VCCI and VCCA can be powered up in any sequence with respect to each other, provided the requirement with respect to VCCDA is satisfied.

2.1.2 Calculating Power Dissipation

The following table lists the standby current values.

© 2024 Microchip Technology Inc. and its subsidiaries

Table 2-3. Standby Current

Device	Temperature	ICCA	ICCDA	ICCBANK		ICCPLL	ICCCP[1]		IIH, IIL, IOZ[2]	Units
		Standby Current (Core)	Standby Current, Differential I/O	Standby Current per I/O Bank		Standby Current per PLL	Standby Current, Charge Pump			
				2.5V VCCI	3.3V VCCI		Active	Bypassed Mode		
AX125	Typical at 25 °C	1.5	1.5	0.2	0.3	0.2	0.3	0.01	±0.01	mA
	70 °C	15	6	0.5	0.75	1	0.4	0.01	±0.01	mA
	85 °C	25	6	0.6	0.8	1	0.4	0.2	±0.01	mA
	125 °C	50	8	1	1.5	2	0.4	0.5	±0.01	mA
AX250	Typical at 25 °C	1.5	1.4	0.25	0.4	0.2	0.3	0.01	±0.01	mA
	70 °C	30	7	0.8	0.9	1	0.4	0.01	±0.01	mA
	85 °C	40	7	0.8	1	1	0.4	0.2	±0.01	mA
	125 °C	70	9	1.3	1.8	2	0.4	0.5	±0.01	mA
AX500	Typical at 25 °C	5	1.4	0.4	0.75	0.2	0.3	0.01	±0.01	mA
	70 °C	60	7	1	1.5	1	0.4	0.01	±0.01	mA
	85 °C	80	7	1	1.9	1	0.4	0.2	±0.01	mA
	125 °C	180	9	1.75	2.5	1.5	0.4	0.5	±0.01	mA
AX1000	Typical at 25 °C	7.5	1.5	0.5	1.25	0.2	0.3	0.01	±0.01	mA
	70 °C	80	8	1.5	3	1	0.4	0.01	±0.01	mA
	85 °C	120	8	1.5	3.4	1	0.4	0.2	±0.01	mA
	125 °C	200	10	3	4	1.5	0.4	0.5	±0.01	mA
AX2000	Typical at 25 °C	20	1.6	0.7	1.5	0.2	0.3	0.01	±0.01	mA
	70 °C	160	10	2	7	1	0.4	0.01	±0.01	mA
	85 °C	200	10	3	8	1	0.4	0.2	±0.01	mA
	125 °C	500	15	4	10	1.5	0.4	0.5	±0.01	mA

Notes:

1. ICCCP Active is the ICCDA or the Internal Charge Pump current. ICCCP Bypassed mode is the External Charge Pump current IIH (VPUMP pin).
2. IIH, IIL, or IOZ values are measured with inputs at the same level as VCCI for IIH and GND for IIL and IOZ.

The following table lists the default values (C_{LOAD}, VCCI, P_{LOAD}, P10, and PI/O) of I/O standard.

Table 2-4. Default Values of I/O Standard

I/O Standard	C_{LOAD} (pF)	VCCI (V)	P_{LOAD} (mw/MHz)	P10 (mw/MHz)	PI/O (mW/MHz)[1]
Single-Ended without VREF					
LVTTL 24 mA High Slew	35	3.3	381.2	267.5	648.7
LVTTL 16 mA High Slew	35	3.3	381.2	225.1	606.3
LVTTL 12 mA High Slew	35	3.3	381.2	165.9	547.1
LVTTL 8 mA High Slew	35	3.3	381.2	130.3	511.5
LVTTL 24 mA Low Slew	35	3.3	381.2	169.2	550.4
LVTTL 16 mA Low Slew	35	3.3	381.2	150.8	532.0
LVTTL 12 mA Low Slew	35	3.3	381.2	138.6	519.8
LVTTL 8 mA Low Slew	35	3.3	381.2	118.7	499.9
LVCMOS—25	35	2.5	218.8	148.0	366.8
LVCMOS—18	35	1.8	113.4	73.4	186.8

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

I/O Standard	C_{LOAD} (pF)	VCCI (V)	P_{LOAD} (mw/MHz)	P10 (mw/MHz)	PI/O (mW/MHz)[1]
LVCMOS—15 (JESD8-11)	35	1.5	78.8	49.5	128.3
PCI	10	3.3	108.9	218.5	327.4
PCI-X	10	3.3	108.9	162.9	271.8
Single-Ended with VREF					
HSTL-I	20	1.5	—	40.9	40.9
SSTL2-I	30	2.5	—	171.2	171.2
SSTL2-II	30	2.5	—	147.8	147.8
SSTL3-I	30	3.3	—	327.2	327.2
SSTL3-II	30	3.3	—	288.4	288.4
GTLP—25	10	2.5	—	61.5	61.5
GTLP—33	10	3.3	—	68.5	68.5
Differential					
LVPECL—33	N/A	3.3	—	260.6	260.6
LVDS—25	N/A	2.5	—	145.8	145.8

Note:

1. $PI/O = P10 + C_{LOAD} \times VCCI^2$

The following table lists the different components contributing to the total power consumption in axcelerator devices.

Table 2-5. Different Components Contributing to the Total Power Consumption in Axcelerator Devices

Component	Definition	Device Specific Value (in µW/MHz)				
		AX125	AX250	AX500	AX1000	AX2000
P1	Core tile HCLK power component	33	49	71	130	216
P2	R-cell power component	0.2	0.2	0.2	0.2	0.2
P3	HCLK signal power dissipation	4.5	4.5	9	13.5	18
P4	Core tile RCLK power component	33	49	71	130	216
P5	R-cell power component	0.3	0.3	0.3	0.3	0.3
P6	RCLK signal power dissipation	6.5	6.5	13	19.5	26
P7	Power dissipation due to the switching activity on the R-cell	1.6	1.6	1.6	1.6	1.6
P8	Power dissipation due to the switching activity on the C-cell	1.4	1.4	1.4	1.4	1.4
P9	Power component associated with the input voltage	10	10	10	10	10
P10	Power component associated with the output voltage	See Package Pin Assignments				
P11	Power component associated with the read operation in the RAM block	25	25	25	25	25
P12	Power component associated with the write operation in the RAM block	30	30	30	30	30
P13	Core PLL power component	1.5	1.5	1.5	1.5	1.5

Power Dissipation is calculated using the following equations.

- $P_{total} = P_{dc} + P_{ac}$
  - $P_{dc} = I_{CCA} \times VCCA$
  - $P_{ac} = P_{HCLK} + P_{CLK} + P_{R\text{-}cells} + P_{C\text{-}cells} + P_{inputs} + P_{outputs} + P_{memory} + P_{PLL}$
- $P_{HCLK} = (P1 + P2 \times s + P3 \times sqrt[s]) \times Fs$
  - s = the number of R-cells clocked by this clock
  - Fs = the clock frequency

© 2024 Microchip Technology Inc. and its subsidiaries

- P_{CLK} = (P4 + P5 × s + P6 × sqrt[s]) × Fs
  - s = the number of R-cells clocked by this clock
  - Fs = the clock frequency
- $P_{R\text{-}cells}$ = P7 × ms × Fs
  - ms = the number of R-cells switching at each Fs cycle
  - Fs = the clock frequency
- $P_{C\text{-}cells}$ = P8 × mc × Fs
  - Fs = the clock frequency
  - mc = the number of C-cells switching at each Fs cycle
- P_{inputs} = P9 × pi × Fpi
  - pi = the number of inputs
  - Fpi = the average input frequency
- $P_{outputs}$ = PI/O × po × Fpo
  - C_{load} = the output load (technology dependent)
  - VCCI = the output voltage (technology dependent)
  - po = the number of outputs
  - F_{po} = the average output frequency
- P_{memory} = P11 × N_{block} × F_{RCLK} + P12 × N_{block} × F_{WCLK}
  - N_{block} = the number of RAM/FIFO blocks (1 block = 4k)
  - F_{RCLK} = the read-clock frequency of the memory
  - F_{WCLK} = the write-clock frequency of the memory
- P_{PLL} = P13 × F_{CLK}
  - F_{RefCLK} = the clock frequency of the clock input of the PLL
  - F_{CLK} = the clock frequency of the first clock output of the PLL

2.1.3 Power Estimation Example

This example employs an AX1000 shift-register design with 1,080 R-cells, one C-cell, one reset input, and one LVTTL 12 mA output, with high slew.

This design uses one HCLK at 100 MHz.

The following shows the example of power estimation.

- ms = 1,080 (in a shift register—100% of R-cells are toggling at each clock cycle)
- Fs = 100 MHz
- s = 1080
  => P_{HCLK} = (P1 + P2 × s + P3 × sqrt[s]) × Fs = 79 mW
  and Fs = 100 MHz
  => $P_{R\text{-}cells}$ = P7 × ms × Fs = 173 mW
- mc = 1 (1 C-cell in this shift-register)
  and Fs = 100 MHz
  => $P_{C\text{-}cells}$ = P8 × mc × Fs = 0.14 mW
- F_{pi} ~ 0 MHz
  and pi = 1 (1 reset input => this is why Fpi = 0)
  => P_{inputs} = P9 × pi × F_{pi} = 0 mW
- F_{po} = 50 MHz

© 2024 Microchip Technology Inc. and its subsidiaries

and po = 1

=> $P_{outputs}$ = PI/O × po × F_{po} = 27.10 mW

- No RAM/FIFO in this shift-register
  => P_{memory} = 0 mW
- No PLL in this shift-register
  => P_{PLL} = 0 mW
- $P_{ac} = P_{HCLK} + P_{CLK} + P_{R\text{-}cells} + P_{C\text{-}cells} + P_{inputs} + P_{outputs} + P_{memory} + P_{PLL}$ = 276 mW
- P_{dc} = 7.5 mA × 1.5V = 11.25 mW
- $P_{total} = P_{dc} + P_{ac}$ = 11.25 mW + 276 mW = 290.30 mW

2.2 Thermal Characteristics

The temperature variable in Microchip's Designer software refers to the junction temperature, but not to the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature. The following equation can be used to calculate junction temperature.

T_J = Junction Temperature = $\Delta T + T_a$

Where,

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient

ΔT = θja × P

Where,

P = Power

θja = Junction to ambient of package.

θja numbers are located in Table 2-6

2.2.1 Package Thermal Characteristics

The device junction-to-case thermal characteristic is θjc, and the junction-to-ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates. θjc values are provided for reference. The absolute maximum junction temperature is 125 °C.

The maximum power dissipation allowed for commercial and industrial grade devices is a function of θja. A sample calculation of the absolute maximum power dissipation allowed for an 896-pin FBGA package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (°C) - \text{Max. ambient temp. } (°C)}{\theta_{ja}(°C/W)} = \frac{125°C - 70°C}{13.6°C/W} = 4.04\ W$$

The maximum power dissipation allowed for military temperature and Mil-Std 883B devices is specified as a function of θjc.

The following table lists the package thermal characteristics.

Table 2-6. Package Thermal Characteristics

Package Type	Pin Count	θjc	θja Still Air	θja 1.0m/s	θja 2.5m/s	Units
Chip Scale Package (CSP)	180	N/A	57.8	51.0	50	°C/W
Plastic Quad Flat Pack (PQFP)	208	8.0	26	23.5	20.9	°C/W
Plastic Ball Grid Array (PBGA)	729	2.2	13.7	10.6	9.6	°C/W

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Package Type	Pin Count	θjc	θja Still Air	θja 1.0m/s	θja 2.5m/s	Units
Fine Pitch Ball Grid Array (FBGA)	256	3.0	26.6	22.8	21.5	°C/W
Fine Pitch Ball Grid Array (FBGA)	324	3.0	25.8	22.1	20.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	484	3.2	20.5	17.0	15.9	°C/W
Fine Pitch Ball Grid Array (FBGA)	676	3.2	16.4	13.0	12.0	°C/W
Fine Pitch Ball Grid Array (FBGA)	896	2.4	13.6	10.4	9.4	°C/W
Fine Pitch Ball Grid Array (FBGA)	1152	1.8	12.0	8.9	7.9	°C/W
Ceramic Quad Flat Pack (CQFP)[1]	208	2.0	22	19.8	18.0	°C/W
Ceramic Quad Flat Pack (CQFP)[1]	352	2.0	17.9	16.1	14.7	°C/W
Ceramic Column Grid Array (CCGA)[2]	624	6.5	8.9	8.5	8	°C/W

Notes:

1. θjc for the 208-pin and 352-pin CQFP refers to the thermal resistance between the junction and the bottom of the package.
2. θjc for the 624-pin CCGA refers to the thermal resistance between the junction and the top surface of the package. Thermal resistance from junction to board (θjb) for CCGA 624 package is 3.4 °C/W.

2.2.2 Timing Characteristics

Axcelerator devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing. The derating factors shown in the following table should be applied to all timing data within this datasheet.

Table 2-7. Temperature and Voltage Timing Derating Factors (Normalized to Worst-Case Commercial, T_J = 70 °C, VCCA = 1.425V)

VCCA	Junction Temperature						
	–55 °C	–40 °C	0 °C	25 °C	70 °C	85 °C	125 °C
1.4V	0.83	0.86	0.91	0.96	1.02	1.05	1.15
1.425V	0.82	0.84	0.90	0.94	**1.00**	1.04	1.13
1.5V	0.78	0.80	0.85	0.89	0.95	0.98	1.07
1.575V	0.74	0.76	0.81	0.85	0.90	0.94	1.02
1.6V	0.73	0.75	0.80	0.84	0.89	0.92	1.01

Notes:

- The user can set the junction temperature in Designer software to any integer value in the range of –55 °C to 125 °C.
- The user can set the core voltage in Designer software to any value between 1.4V and 1.6V.

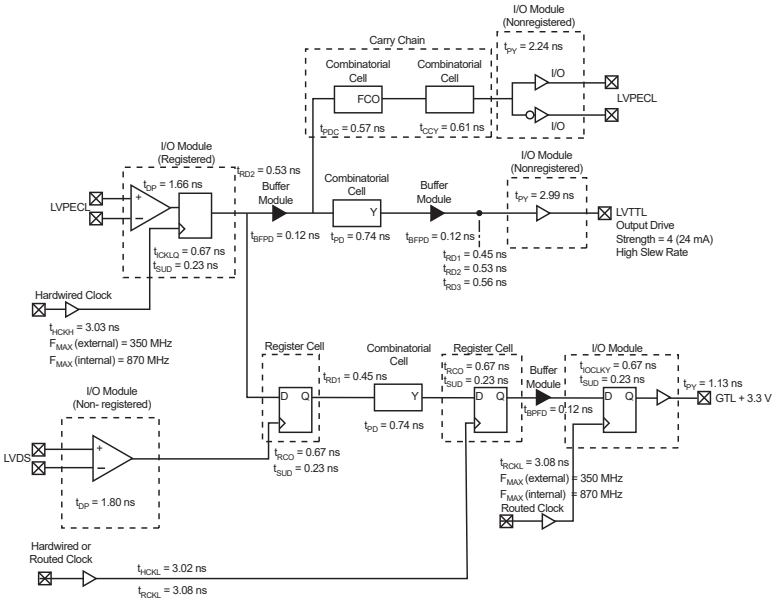
All timing numbers listed in this datasheet represent sample timing characteristics of Axcelerator devices. Actual timing delay values are design-specific and can be derived from the Timer tool in Microchip's Designer software after place-and-route.

2.2.3 Timing Model

The following figure shows the worst case timing data.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-1. Worst Case Timing Data



2.2.3.1 Hardwired Clock—Using LVTTL 24 mA High Slew Clock I/O

- External Setup
  $= (t_{DP} + t_{RD2} + t_{SUD}) - t_{HCKL}$
  $= (1.72 + 0.53 + 0.23) - 3.02 = -0.54$ ns
- Clock-to-Out (Pad-to-Pad)
  $= t_{HCKL} + t_{RCO} + t_{RD1} + t_{PY}$
  $= 3.02 + 0.67 + 0.45 + 2.99 = 7.13$ ns

2.2.3.2 Routed Clock—Using LVTTL 24 mA High Slew Clock I/O

- External Setup
  $= (t_{DP} + t_{RD2} + t_{SUD}) - t_{RCKH}$
  $= (1.72 + 0.53 + 0.23) - 3.13 = -0.65$ ns
- Clock-to-Out (Pad-to-Pad)
  $= t_{RCKH} + t_{RCO} + t_{RD1} + t_{PY}$
  $= 3.13 + 0.67 + 0.45 + 3.03 = 7.24$ ns

2.3 I/O Specifications

2.3.1 Pin Descriptions

This section describes the pin descriptions.

2.3.1.1 Supply Pins

The following table lists the supply pins.

Table 2-8. Supply Pins

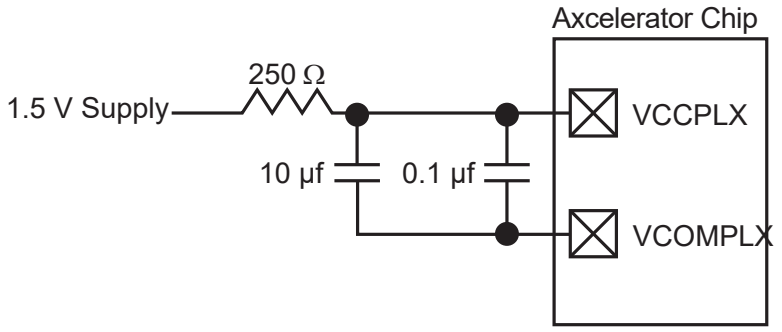
Name	Type	Description
GND	Ground	Low supply voltage
VCCA	Supply voltage	Supply voltage for array (1.5V). See Operating Conditions for more information.

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Name	Type	Description
VCCIBx	Supply voltage	Supply voltage for I/Os. Bx is the I/O Bank ID—0 to 7. See Operating Conditions for more information.
VCCDA	Supply voltage	Supply voltage for the I/O differential amplifier and JTAG and probe interfaces. See Operating Conditions for more information. VCCDA should be tied to 3.3V.
VCCPLA/B/C/D/E/F/G/H	Supply voltage	PLL analog power supply (1.5V) for internal PLL. There are eight in each device. VCCPLA supports the PLL associated with global resource HCLKA, VCCPLB supports the PLL associated with global resource HCLKB, and so on. The PLL analog power supply pins should be connected to 1.5V whether PLL is used or not.
VCOMPLA/B/C/D/E/F/G/H	Supply voltage	Compensation reference signals for internal PLL. There are eight in each device. VCOMPLA supports the PLL associated with global resource HCLKA, VCOMPLE supports the PLL associated with global resource CLKE, and so on. (see the following figure for correct external connection to the supply). The VCOMPLX pins should be left floating if PLL is not used.
VPUMP	Supply voltage (external pump)	In the low power mode, VPUMP will be used to access an external charge pump (if the user desires to bypass the internal charge pump to further reduce power). The device starts using the external charge pump when the voltage level on VPUMP reaches VIH[1]. In normal device operation, when using the internal charge pump, VPUMP should be tied to GND.

Figure 2-2. VCCPLX and VCOMPLX Power Supply Connect



2.3.1.2 User-Defined Supply Pins

The following table lists the user-defined supply pins.

[1] When VPUMP = VIH, it shuts off the internal charge pump. See Low Power Mode

© 2024 Microchip Technology Inc. and its subsidiaries

Table 2-9. User-Defined Supply Pins

Name	Type	Description
VREF	Supply voltage	Reference voltage for I/O banks. VREF pins are configured by the user from regular I/O pins, VREF pins are not in fixed locations. There can be one or more VREF pins in an I/O bank.

2.3.1.3 Global Pins

The following table lists the global pins.

Table 2-10. Global Pins

Name	Type	Description
HCLKA/B/C/D	Dedicated (hardwired) clocks A, B, C, and D	These pins are the clock inputs for sequential modules or north PLLs. Input levels are compatible with all supported I/O standards. There is a P/N pin pair for support of differential I/O standards. Single-ended clock I/Os can only be assigned to the P side of a paired I/O. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When the HCLK pins are unused, it is recommended that they are tied to ground.
CLKE/F/G/H	Routed clocks E, F, G, and H	These pins are clock inputs for clock distribution networks or south PLLs. Input levels are compatible with all supported I/O standards. There is a P/N pin pair for support of differential I/O standards. Single-ended clock I/Os can only be assigned to the P side of a paired I/O. The clock input is buffered prior to clocking the R-cells. When the CLK pins are unused, Microchip recommends to tie the CLK pins to the ground.

2.3.1.4 JTAG/Probe Pins

The following table lists the JTAG/Probe pins.

Table 2-11. JTAG/Probe Pins

Name	Type	Description
PRA/B/C/D	Probe A, B, C, and D	The Probe pins are used to output data from any user-defined design node within the device (controlled with Silicon Explorer II). These independent diagnostic pins can be used to allow real-time diagnostic output of any signal path within the device. The pins' probe capabilities can be permanently disabled to protect programmed design confidentiality. The probe pins are of LVTTL output levels.
TCK	Test clock	Test clock input for JTAG boundary-scan testing and diagnostic probe (Silicon Explorer II).

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Name	Type	Description
TDI	Test data input	Serial input for JTAG boundary-scan testing and diagnostic probe. TDI is equipped with an internal 10 kΩ pull-up resistor.
TDO	Test data output	Serial output for JTAG boundary-scan testing.
TMS	Test mode select	The TMS pin controls the use of the IEEE 1149.1 boundary-scan pins (TCK, TDI, TDO, and TRST). TMS is equipped with an internal 10 kΩ pull-up resistor.
TRST	Boundary scan reset pin	The TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with a 10 kΩ pull-up resistor.

2.3.1.5 Special Functions

The following table lists the special functions.

Table 2-12. Special Functions

Name	Type	Description
LP	Low power pin	The LP pin controls the low power mode of Axcelerator devices. The device is placed in the low power mode by connecting the LP pin to logic high. To exit the low power mode, the LP pin must be set Low. Additionally, the LP pin must be set Low during chip powering-up or chip powering-down operations. See Low Power Mode for more details.
NC	No connection	This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

2.3.2 User I/Os[2]

The Axcelerator family features a flexible I/O structure, supporting a range of mixed voltages (1.5V, 1.8V, 2.5V, and 3.3V) with its bank-selectable I/Os.

Each I/O provides programmable slew rates, drive strengths, and weak pull-up and weak pull-down circuits. The slew rate setting is effective for both rising and falling edges.

I/O standards, except 3.3V PCI and 3.3V PCI-X, are capable of hot insertion. 3.3V PCI and 3.3V PCI- X are 5V tolerant with the aid of an external resistor.

The input buffer has an optional user-configurable delay element. The element can reduce or eliminate thehold time requirement for input signals registered within the I/O cell. The value for the delay is set on a bank-wide basis. The delay Will be a function of process variations as well as temperature and voltage changes.

[2] Do not use an external resister to pull the I/O above VCCI for a higher logic “1” voltage level. The desired higher logic “1” voltage level will be degraded due to a small I/O current, which exists when the I/O is pulled up above VCCI.

© 2024 Microchip Technology Inc. and its subsidiaries

Each I/O includes three registers: an input (InReg), an output (OutReg), and an enable register (EnReg). I/Os are organized into banks, and there are eight banks per device—two per side (see Figure 2-6). Each I/O bank has a common VCCI, the supply voltage for its I/Os.

For voltage-referenced I/Os, each bank also has a common reference-voltage bus, VREF. While VREF must have a common voltage for an entire I/O bank, its location is user-selectable. In other words, any user I/O in the bank can be selected to be a VREF.

The location of the VREF pin should be selected according to the following rules.

- Any pin that is assigned as a VREF can control a maximum of eight user I/O pad locations in each direction (16 total maximum) within the same I/O bank
- I/O pad locations listed as no connects are counted as part of the 16 maximum. In many cases, thisleads to fewer than eight user I/O package pins in each direction being controlled by a VREF pin.
- Dedicated I/O pins such as GND and VCCI are counted as part of the 16
- The two user I/O pads immediately adjacent on each side of the VREF pin (four in total) may only be used as inputs. The exception is when there is a VCCI/GND pair separating the VREF pin and the user I/O pad location.
- The user does not need to assign VREF pins for OUTBUF and TRIBUF. VREF pins are needed only for input and bidirectional I/Os.

The differential amplifier supply voltage VCCDA should be connected to 3.3V. A user can gain access to the various I/O standards in three ways.

- Instantiate specific library macros that represent the desired specific standard
- Use generic I/O macros and then use Designer's PinEditor to specify the desired I/O standards (this is not applicable to differential standards)
- A combination of the first two methods

For more details, see the I/O Features in Axcelerator Family Devices application note and the Antifuse Macro Library Guide .

Table 2-13. I/O Standards Supported by the Axcelerator Family

I/O Standard	Input/Output Supply Voltage (VCCI)	Input Reference Voltage (VREF)	Board Termination Voltage (VTT)
LVTTL	3.3	N/A	N/A
LVCMOS 2.5V	2.5	N/A	N/A
LVCMOS 1.8V	1.8	N/A	N/A
LVCMOS 1.5V (JDEC8-11)	1.5	N/A	N/A
3.3V PCI/PCI-X	3.3	N/A	N/A
GTL+ 3.3V	3.3	1.0	1.2
GTL+ 2.5V[1]	2.5	1.0	1.2
HSTL Class 1	1.5	0.75	0.75
SSTL3 Class 1 and II	3.3	1.5	1.5
SSTL2 Class1 and II	2.5	1.25	1.25
LVDS	2.5	N/A	N/A
LVPECL	3.3	N/A	N/A

Note:

1. 2.5V GTL+ is not supported across the full military temperature range.

© 2024 Microchip Technology Inc. and its subsidiaries

Table 2-14. Supply Voltages

VCCA	VCCI	Input Tolerance	Output Drive Level
1.5V	1.5V	3.3V	1.5V
1.5V	1.8V	3.3V	1.8V
1.5V	2.5V	3.3V	2.5V
1.5V	3.3V	3.3V	3.3V

The following table compares the features of the different I/O standards.

Table 2-15. I/OFeatures Comparison

I/O Assignment	Clamp Diode	Hot Insertion	5V Tolerance	Input Buffer	Output Buffer
LVTTL	No	Yes	Yes[1]	Enabled/Disabled	
3.3V PCI, 3.3V PCI-X	Yes	No	Yes[1], [2]	Enabled/Disabled	
LVCMOS 2.5V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.8V	No	Yes	No	Enabled/Disabled	
LVCMOS 1.5V (JESD8-11)	No	Yes	No	Enabled/Disabled	
Voltage-referenced input buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/LVPECL, input	No	Yes	No	Enabled	Disabled[3]
Differential, LVDS/LVPECL, output	No	Yes	No	Disabled	Enabled[4]

Notes:

1. Can be implemented with an IDT bus switch.
2. Can be implemented with an external resistor.
3. The OE input of the output buffer must be deasserted permanently (handled by software).
4. The OE input of the output buffer must be asserted permanently (handled by software).

2.3.2.1 5V Tolerance

There are two schemes to achieve 5V tolerance.

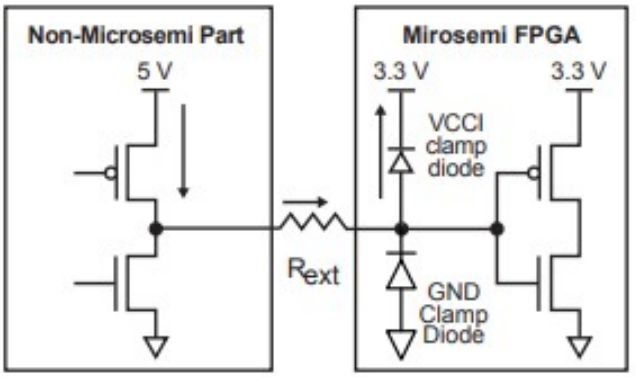
3.3V PCI and 3.3V PCI-X are the only I/O standards that directly allow 5V tolerance. To implement this, an internal clamp diode between the input pad and the VCCI pad is enabled so that the voltage at the input pin is clamped, as shown in the following equation:

V_{input} = VCCI + V_{diode} = 3.3V + 0.7V = 4.0V

The internal VCCI clamp diode is only enabled while the device is powered on, so the voltage at the input will not be clamped if the VCCI or VCCA are powered off. An external series resistor (~100 ?) is required between the input pin and the 5V signal source to limit the current to less than 20 mA (see the following figure). The 100 ? resistor was chosen to meet the input Tr/Tf requirement (see Table 2-24). The GND clamp diode is available for all I/O standards and always enabled.

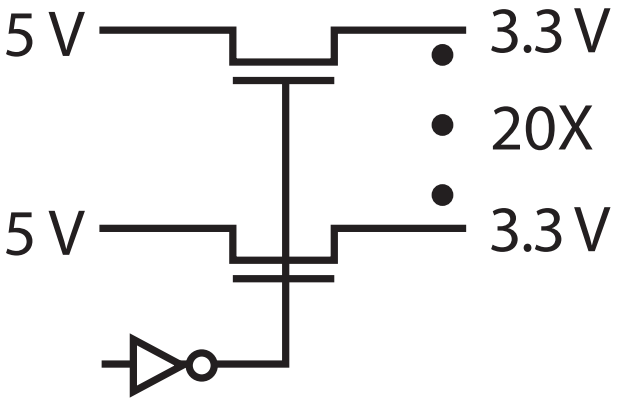
© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-3. Use of an External Resistor for 5V Tolerance



5V tolerance can also be achieved with 3.3V I/O standards (3.3V PCI, 3.3V PCI-X, and LVTTL) using a bus-switch product (for example, IDTQS32X2384). This will convert the 5V signal to a 3.3V signal with minimum delay (see the following figure).

Figure 2-4. Bus Switch IDTQS32X2384



2.3.2.2 Simultaneous Switching Outputs (SSO)

When multiple output drivers switch simultaneously, they induce a voltage drop in the chip/package power distribution. This simultaneous switching momentarily raises the ground voltage within the device relative to the system ground. This apparent shift in the ground potential to a non-zero value is known as Simultaneous Switching Noise (SSN) or more commonly, ground bounce.

SSN becomes more of an issue in high pin count packages and when using high performance devices such as the Axcelerator family. Based upon testing, Microchip recommends users not to exceed eight Simultaneous Switching Outputs (SSO) per each VCCI/GND pair. To ease this potential burden on designers, Microchip has designed all of the Axcelerator BGAs[3] to not exceed this limit with the exception of the CS180, which has an I/O to VCCI/GND pair ratio of nine to one.

For more information, see the Simultaneous Switching Noise and Signal Integrity application note.

2.3.3 I/O Banks and Compatibility

Since each I/O bank has its own user-assigned input reference voltage (VREF) and an input/output supply voltage (VCCI), only I/Os with compatible standards can be assigned to the same bank.

[3] The user should note that in Bank 8 of both AX1000-FG484 and AX500-FG484, there are local violations of this 8:1 ratio.

© 2024 Microchip Technology Inc. and its subsidiaries

The following table shows the compatible I/O standards for a common VREF (for voltage-referenced standards).

Table 2-16. Compatible I/O Standards for Different VREF Values

VREF	Compatible Standards
1.5V	SSTL 3 (Class I and II)
1.25V	SSTL 2 (Class I and II)
1.0V	GTL+ (2.5V and 3.3V Outputs)
0.75V	HSTL (Class I)

The following table shows compatible standards for a common VCCI.

Table 2-17. Compatible I/O Standards for Different VCCI Values

VCCI[1]	Compatible Standards	VREF
3.3V	LVTTL, PCI, PCI-X, LVPECL, GTL+ 3.3V	1.0
3.3V	SSTL 3 (Class I and II), LVTTL, PCI, LVPECL	1.5
2.5V	LVCMOS 2.5V, GTL+ 2.5V, LVDS[2]	1.0
2.5V	LVCMOS 2.5V, SSTL 2 (Classes I and II), LVDS[2]	1.25
1.8V	LVCMOS 1.8V	N/A
1.5V	LVCMOS 1.5V, HSTL Class I	0.75

Notes:

1. VCCI is used for both inputs and outputs
2. VCCI tolerance is ±5%

The following table summarizes the different combinations of voltages and I/O standards that can be used together in the same I/O bank.

Table 2-18. Legal I/O Usage Matrix

I/O Standard	LVTTL 3.3V	LVCMOS 2.5V	LVCMOS 1.8V	LVCMOS 1.5V (JESD8-11)	3.3V PCI/ PCI-X	GTL+ (3.3V)	GTL+ (2.5V)	HSTL Class I (1. 5V)	SSTL2 Class I & II (2.5V)	SSTL3 Class I & II (3.3V)	LVDS (2.5V)	LVPECL (3.3V)
LVTTL 3.3V (VREF=1.0V)	✓	—	—	—	✓	✓	—	—	—	—	—	✓
LVTTL 3.3V (VREF=1.5V)	✓	—	—	—	✓	—	—	—	—	✓	—	✓
LVCMOS 2.5V (VREF=1.0V)	—	✓	—	—	—	—	✓	—	—	—	✓	—
LVCMOS 2.5V (VREF=1.25V)	—	✓	—	—	—	—	—	—	✓	—	✓	—
LVCMOS 1.8V	—	—	✓	—	—	—	—	—	—	—	—	—
LVCMOS 1.5V (VREF = 1.75V) (JESD8-11)	—	—	—	✓	—	—	—	✓	—	—	—	—
3.3V PCI/PCI-X (VREF = 1.0V)	✓	—	—	—	✓	✓	—	—	—	—	—	✓
3.3V PCI/PCI-X (VREF = 1.5V)	✓	—	—	—	✓	—	—	—	—	✓	—	✓
GTL+ (3.3V)	✓	—	—	—	✓	✓	—	—	—	—	—	✓
GTL+ (2.5V)	—	✓	—	—	—	—	✓	—	—	—	—	—
HSTL Class I	—	—	—	✓	—	—	—	✓	—	—	—	—

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

I/O Standard	LVTTL 3.3V	LVCMOS 2.5V	LVCMOS 1.8V	LVCMOS 1.5V (JESD8-11)	3.3V PCI/ PCI-X	GTL+ (3.3V)	GTL+ (2.5V)	HSTL Class I (1. 5V)	SSTL2 Class I & II (2.5V)	SSTL3 Class I & II (3.3V)	LVDS (2.5V)	LVPECL (3.3V)
SSTL2 Class I & II	—	✓	—	—	—	—	—	—	✓	—	✓	—
SSTL3 Class I & II	✓	—	—	—	✓	—	—	—	—	✓	—	✓
LVDS (VREF = 1.0V)	—	✓	—	—	—	—	✓	—	—	—	✓	—
LVDS (VREF = 1.25V)	—	✓	—	—	—	—	—	—	✓	—	✓	—
LVPECL (VREF = 1.0V)	✓	—	—	—	✓	✓	—	—	—	—	—	✓
LVPECL (VREF = 1.5V)	✓	—	—	—	✓	—	—	—	—	✓	—	✓

Notes:
The GTL+ 2.5V is not supported across the full military temperature range.

A tick symbol indicates whether standards can be used within a bank at the same time
Examples:

- LVTTL can be used with 3.3V PCI and GTL+ (3.3V), when VREF = 1.0V (GTL+ requirement).
- LVTTL can be used with 3.3V PCI and SSTL3 Class I and II, when VREF = 1.5V (SSTL3 requirement).

The two I/O standards are compatible if:

- Their VCCI values are identical
- Their VREF standards are identical (if applicable)

For example, if LVTTL 3.3V (VREF= 1.0V) is used, then the other available (that is compatible) I/O standards in the same bank are LVTTL 3.3V PCI/PCI-X, GTL+, and LVPECL.

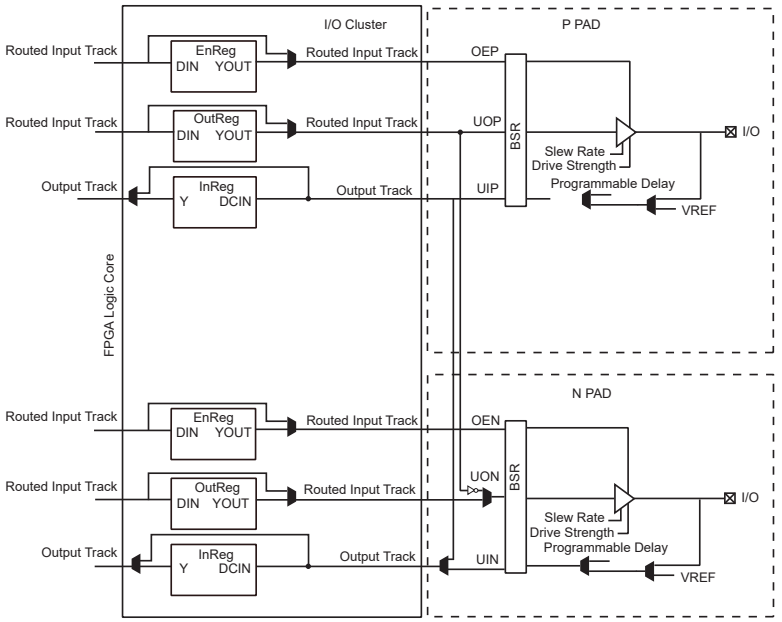
Also, when multiple I/O standards are used within a bank, the voltage tolerance will be limited to the minimum tolerance of all I/O standards used in the bank.

2.3.3.1 I/O Clusters

Each I/O cluster incorporates two I/O modules, four RX modules, two TX modules, and a buffer module. In turn, each I/O module contains one Input Register (InReg), one Output Register (OutReg), and one Enable Register (EnReg) (see the following figure).

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-5. I/O Cluster Interface



2.3.3.2 Using an I/O Register

To access the I/O registers, registers must be instantiated in the netlist and then connected to the I/Os. Usage of each I/O register (register combining) is individually controlled and can be selected/deselected using the PinEditor tool in the Designer software. I/O register combining can also be controlled at the device level, affecting all I/Os. The I/O register option is deselected by default in any given design.[4]

In addition, Designer software provides a global option to enable/disable the usage of registers in the I/Os. This option is design-specific. The setting for each individual I/O overrides this global option. Furthermore, the global set fuse option in the Designer software, when checked, causes all I/O registers to output logic High at device power-up.

2.3.3.3 Using the Weak Pull-Up and Pull-Down Circuits

Each Axcelerator I/O comes with a weak pull-up/down circuit (on the order of 10 kΩ). These are weak transistors with the gates tied on, so the resistance of the transistor emulates a resistor. The weak pull-up and pull-down is active only when the device is powered up, and they must be biased to be on. When the rails are coming up, they are not biased fully, so they do not behave as resistors until the voltage is at sufficient levels to bias the transistors. The key is they really are transistors, they are not traces of poly silicon, which is another way to do an on-chip resistor (those take much more room). I/O macros are provided for combinations of pull up/down for LVTTL, LVCMOS (2.5V, 1.8V, and 1.5V) standards. These macros can be instantiated if a keeper circuit for any input buffer is required.

2.3.3.4 Customizing the I/O

A five-bit programmable input delay element is associated with each I/O. The value of this delay is set on a bank-wide basis (see the following table). It is optional for each input buffer within the bank (that is, the user can enable or disable the delay element for the I/O). When the input buffer drives a register within the I/O, the delay element is activated by default to ensure a zero hold-time. The default setting for this property can be set in Designer. When the input buffer does not drive a register, the delay element is deactivated to provide higher performance. Again, this can be overridden by changing the default setting for this property in Designer.

[4] Please note that register combining for multi fanout nets is not supported.

© 2024 Microchip Technology Inc. and its subsidiaries

The slew-rate value for the LVTTL output buffer can be programmed and can be set to either slow or fast.

The drive strength value for LVTTL output buffers can be programmed as well. There are four different drive strength values (8 mA, 12 mA, 16 mA, or 24 mA) that can be specified in Designer.[5]

The following table lists the values of bank-wide delay.

Table 2-19. Bank-Wide Delay Values

Bits Setting	Delay (ns)
0	0.54
1	0.65
2	0.71
3	0.83
4	0.9
5	1.01
6	1.08
7	1.19
8	1.27
9	1.39
10	1.45
11	1.56
12	1.64
13	1.75
14	1.81
15	1.93
16	2.01
17	2.13
18	2.19
19	2.3
20	2.38
21	2.49
22	2.55
23	2.67
24	2.75
25	2.87
26	2.93
27	3.04
28	3.12
29	3.23
30	3.29
31	3.41

Note: Delay values are approximate and will vary with process, temperature, and voltage.

2.3.3.5 Using the Differential I/O Standards

Differential I/O macros should be instantiated in the netlist. The settings for these I/O standards cannot be changed inside Designer. Note that there are no tristated or bidirectional I/O buffers for differential standards.

[5] These values are minimum drive strengths.

© 2024 Microchip Technology Inc. and its subsidiaries

2.3.3.6 Using the Voltage-Referenced I/O Standards

Using these I/O standards is similar to that of single-ended I/O standards. Their settings can be changed in Designer.

2.3.3.7 Using Double Data Rate (DDR)

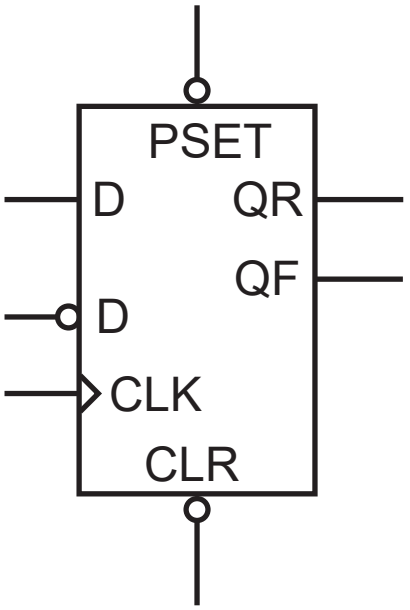
In Double Data Rate mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidth and signal integrity requirements, making it very efficient for implementing very high-speed systems.

To implement a DDR, users need to:

- Instantiate an input buffer (with the required I/O standard).
- Instantiate the DDR_REG macro (see the following figure).
- Connect the output from the input buffer to the input of the DDR macro.

The following figure shows DDR register.

Figure 2-6. DDR Register



2.3.3.8 Macros for Specific I/O Standards

There are different macro types for any I/O standard or feature that determine the required VCCI and VREF voltages for an I/O. The generic buffer macros require the LVTTL standard with slow slew rate and 24 mA-drive strength. LVTTL can support high slew rate but this should only be used for critical signals.

Most of the macro symbols represent variations of the six generic symbol types:

- CLKBUF: Clock Buffer
- HCLKBUF: Hardwired Clock Buffer
- INBUF: Input Buffer
- OUTBUF: Output Buffer
- TRIBUF: Tristate Buffer
- BIBUF: Bidirectional Buffer

Other macros include the following:

© 2024 Microchip Technology Inc. and its subsidiaries

- Differential I/O standard macros: The LVDS and LVPECL macros either have a pair of differential inputs (for example, INBUF_LVDS) or a pair of differential outputs (for example, OUTBUF_LVPECL).
- Pull-up and pull-down variations of the INBUF, BIBUF, and TRIBUF macros. These are available only with TTL and LVCMOS thresholds. They can be used to model the behavior of the pull-up and pull-down resistors available in the architecture. Whenever an input pin is left unconnected, the output pin will either go high or low rather than unknown. This allows users to leave inputs unconnected without having the negative effect on simulation of propagating unknowns.
- DDR_REG macro. It can be connected to any I/O standard input buffers (that is, INBUF) to implement a double data rate register. Designer software will map it to the I/O module in the same way it maps the other registers to the I/O module.

The followings tables list all the available macro names differentiated by I/O standard, type, slew rate, and drive strength.

Table 2-20. Macros for Single-Ended I/O Standards

Standard	VCCI	Macro Names
LVTTL	3.3V	CLKBUF, HCLKBUF INBUF, OUTBUF, OUTBUF_S_8, OUTBUF_S_12, OUTBUF_S_16, OUTBUF_S_24, OUTBUF_H_8, OUTBUF_H_12, OUTBUF_H_16, OUTBUF_H_24, TRIBUF, TRIBUF_S_8, TRIBUF_S_12, TRIBUF_S_16, TRIBUF_S_24, TRIBUF_H_8, TRIBUF_H_12, TRIBUF_H_16, TRIBUF_H_24, BIBUF, BIBUF_S_8, BIBUF_S_12, BIBUF_S_16, BIBUF_S_24, BIBUF_H_8, BIBUF_H_12, BIBUF_H_16, BIBUF_H_24
3.3V PCI	3.3V	CLKBUF_PCI, HCLKBUF_PCI, INBUF_PCI, OUTBUF_PCI, TRIBUF_PCI, BIBUF_PCI
3.3V PCI-X	3.3V	CLKBUF_PCI-X, HCLKBUF_PCI-X, INBUF_PCI-X, OUTBUF_PCI-X, TRIBUF_PCI-X, BIBUF_PCI-X
LVCMOS25	2.5V	CLKBUF_LVCMOS25, HCLKBUF_LVCMOS25, INBUF_LVCMOS25, OUTBUF_LVCMOS25, TRIBUF_LVCMOS25, BIBUF_LVCMOS25
LVCMOS18	1.8V	CLKBUF_LVCMOS18, HCLKBUF_LVCMOS18, INBUF_LVCMOS18, OUTBUF_LVCMOS18, TRIBUF_LVCMOS18, BIBUF_LVCMOS18
LVCMOS15 (JESD8-11)	1.5V	CLKBUF_LVCMOS15, HCLKBUF_LVCMOS15, INBUF_LVCMOS15, OUTBUF_LVCMOS15, TRIBUF_LVCMOS15, BIBUF_LVCMOS15

Table 2-21. I/O Macros for Differential I/O Standards

Standard	VCCI	Macro Names
LVPECL	3.3V	CLKBUF_LVPECL, HCLKBUF_LVPECL, INBUF_LVPECL, OUTBUF_LVPECL
LVDS	2.5V	CLKBUF_LVDS, HCLKBUF_LVDS, INBUF_LVDS, OUTBUF_LVDS

Table 2-22. I/O Macros for Voltage-Referenced I/O Standards

Standard	VCCI	VREF	Macro Names
GTL+	3.3V	1.0V	CLKBUF_GTP33, HCLKBUF_GTP33, INBUF_GTP33, OUTBUF_GTP33, TRIBUF_GTP33, BIBUF_GTP33
GTL+	2.5V	1.0V	CLKBUF_GTP25, HCLKBUF_GTP25, INBUF_GTP25, OUTBUF_GTP25, TRIBUF_GTP25, BIBUF_GTP25
SSTL2 Class I	2.5V	1.25V	CLKBUF_SSTL2_I, HCLKBUF_SSTL2_I, INBUF_SSTL2_I, OUTBUF_SSTL2_I, TRIBUF_SSTL2_I, BIBUF_SSTL2_I
SSTL2 Class II	2.5V	1.25V	CLKBUF_SSTL2_II, HCLKBUF_SSTL2_II, INBUF_SSTL2_II, OUTBUF_SSTL2_II, TRIBUF_SSTL2_II, BIBUF_SSTL2_II
SSTL3 Class I	3.3V	1.5V	CLKBUF_SSTL3_I, HCLKBUF_SSTL3_I, INBUF_SSTL3_I, OUTBUF_SSTL3_I, TRIBUF_SSTL3_I, BIBUF_SSTL3_I

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued			
Standard	VCCI	VREF	Macro Names
SSTL3 Class II	3.3V	1.5V	CLKBUF_SSTL3_II, HCLKBUF_SSTL3_II, INBUF_SSTL3_II, OUTBUF_SSTL3_II, TRIBUF_SSTL3_II, BIBUF_SSTL3_II
HSTL Class I	1.5V	0.75V	CLKBUF_HSTL_I, HCLKBUF_HSTL_I, INBUF_HSTL_I, OUTBUF_HSTL_I, TRIBUF_HSTL_I, BIBUF_HSTL_I

2.3.4 User I/O Naming Conventions

Due to the complex and flexible nature of the Axcelerator family's user I/Os, a naming scheme is used to show the details of the I/O. The naming scheme explains to which bank an I/O belongs, as well as the pairing and pin polarity for differential I/Os (see the following figures).

Figure 2-7. I/O Bank and Dedicated Pin Layout

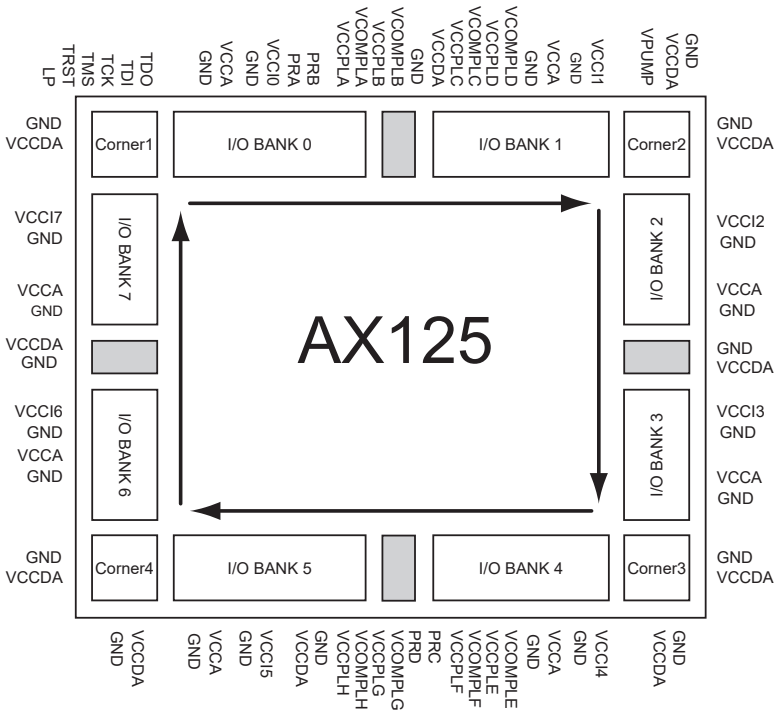
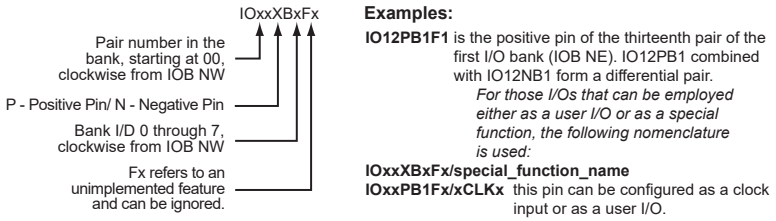


Figure 2-8. General Naming Schemes



2.3.5 I/O Standard Electrical Specifications

The following tables show the I/O standard electrical specifications.

Table 2-23. Input Capacitance

Symbol	Parameter	Conditions	Min.	Max.	Units
CIN	Input capacitance	VIN = 0, f = 1.0 MHz	—	10	pF
CINCLK	Input capacitance on HCLK and RCLK pin	VIN = 0, f = 1.0 MHz	—	10	pF

© 2024 Microchip Technology Inc. and its subsidiaries

Table 2-24. I/O Input Rise Time and Fall Time[1]

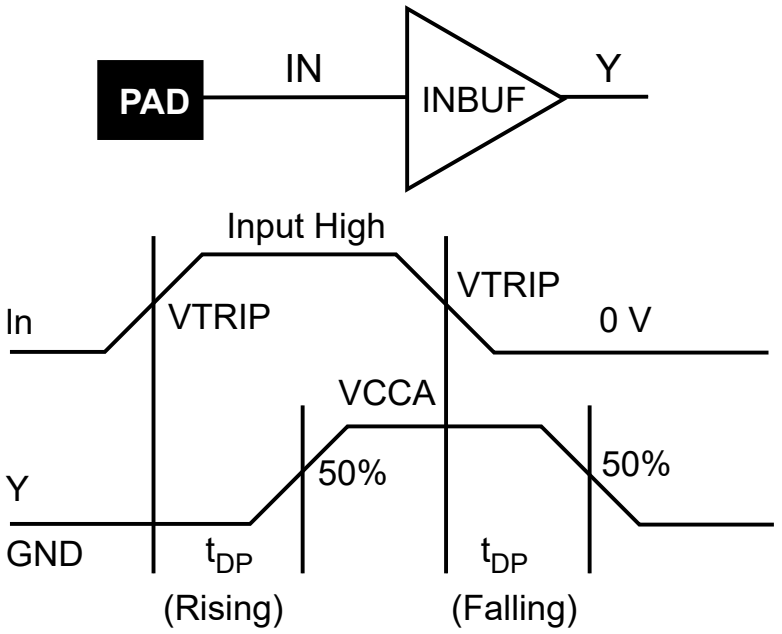
Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)
LVTTL	No requirement	50 ns
LVCMOS 2.5V	No requirement	50 ns
LVCMOS 1.8V	No requirement	50 ns
LVCMOS 1.5V	No requirement	50 ns
PCI	No requirement	50 ns
PCIX	No requirement	50 ns
GTL+	No requirement	50 ns
HSTL	No requirement	50 ns
SSTL2	No requirement	50 ns
HSTL3	No requirement	50 ns
LVDS	No requirement	50 ns
LVPECL	No requirement	50 ns

Note:

1. Input Rise/Fall time applies to all inputs, be it clock or data. Inputs have to ramp up/down linearly, in a monotonic way. Glitches or a plateau may cause double clocking. They must be avoided. For output rise/fall time, see the IBIS models for extraction.

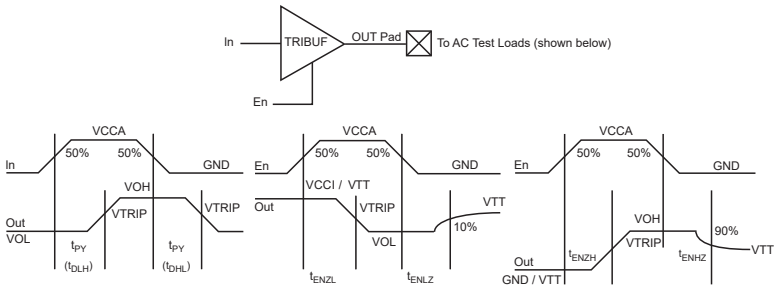
The following figure shows the input and output buffer delays.

Figure 2-9. Input Buffer Delays



© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-10. Output Buffer Delays



2.3.6 I/O Module Timing Characteristics

The following figure shows the timing model.

Figure 2-11. Timing Model

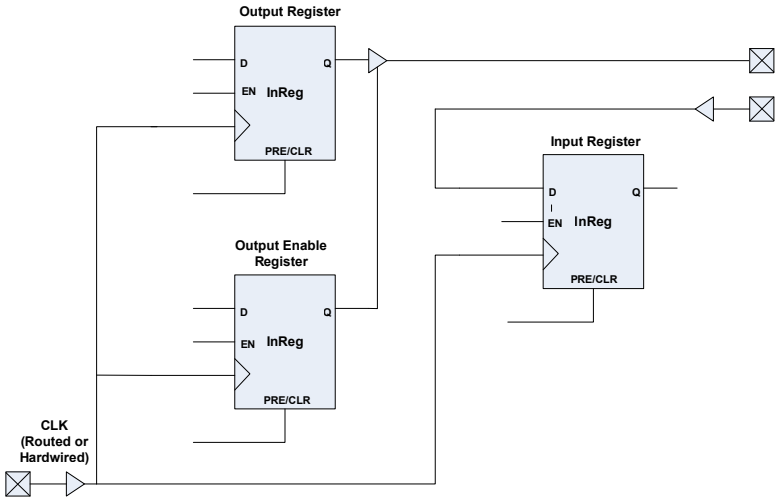
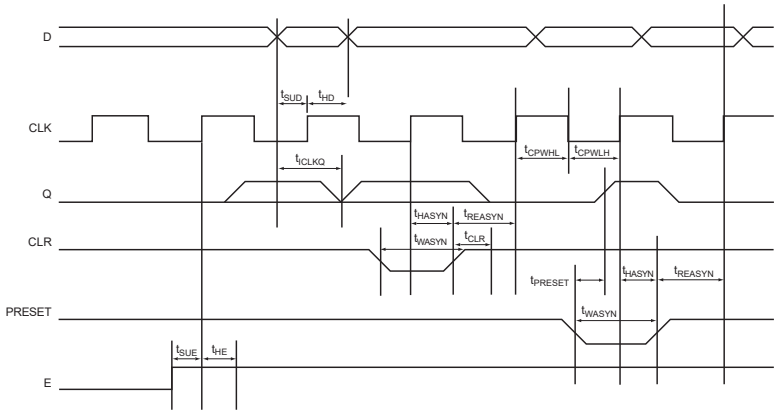


Figure 2-12. Input Register Timing Characteristics



© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-13. Output Register Timing Characteristics

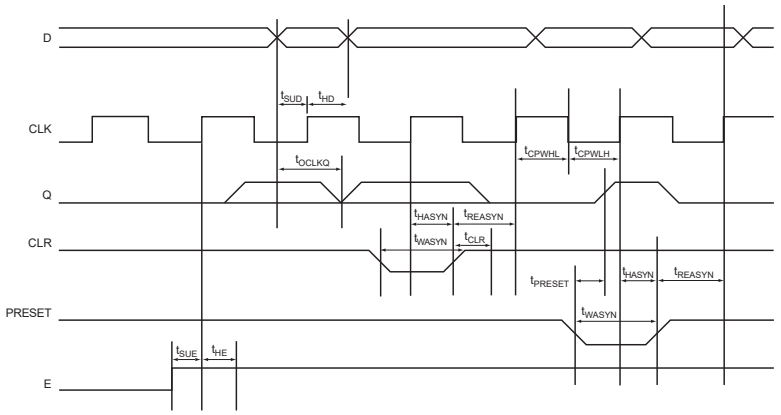
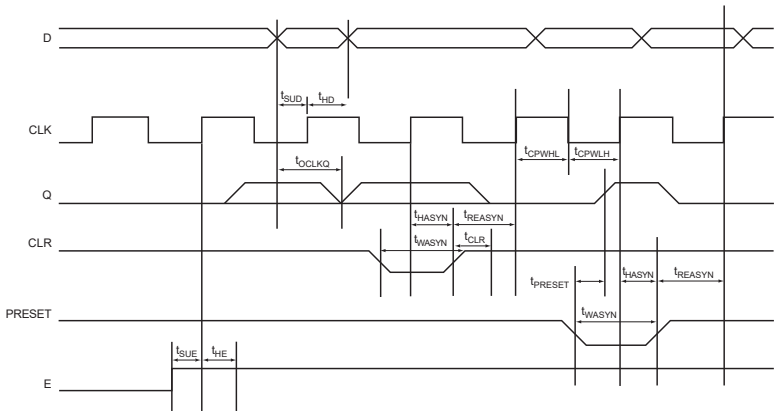


Figure 2-14. Output Enable Register Timing Characteristics



2.3.7 3.3V LVTTL

Low-Voltage Transistor-Transistor Logic (LVTTL) is a general purpose standard (EIA/JESD) for 3.3V applications. It uses an LVTTL input buffer and push-pull output buffer.

The following table lists the DC input and output levels of 3.3V LVTTL.

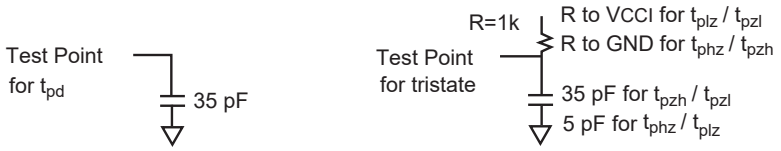
Table 2-25. DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
–0.3	0.8	2.0	3.6	0.4	2.4	24	–24

2.3.7.1 AC Loadings

The following figure shows AC test loads.

Figure 2-15. AC Test Loads



The following table lists the AC loading values.

© 2024 Microchip Technology Inc. and its subsidiaries

Table 2-26. AC Waveforms, Measuring Points, and Capacitive Load

Input Low (V)	Input High (V)	Measuring Point[1] (V)	VREF (typ) (V)	Cload (pF)
0	3.0	1.40	N/A	35

Note:

1. Measuring Point = VTRIP

2.3.7.2 Timing Characteristics

The following table lists the timing characterisitics of 3.3V LVTTL.

Table 2-27. 3.3V LVTTL I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVTTL Output Drive Strength = 1 (8 mA)/Low Slew Rate								
t_{DP}	Input buffer	—	1.68	—	1.92	—	2.26	ns
t_{PY}	Output buffer	—	14.28	—	16.27	—	19.13	ns
t_{ENZL}	Enable to pad delay through the output buffer—Z to low	—	15.25	—	17.37	—	20.42	ns
t_{ENZH}	Enable to pad delay through the output buffer—Z to high	—	14.26	—	16.24	—	19.09	ns
t_{ENLZ}	Enable to pad delay through the output buffer—low to Z	—	1.56	—	1.57	—	1.58	ns
t_{ENHZ}	Enable to pad delay through the output buffer—high to Z	—	1.95	—	1.96	—	1.97	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	039	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{DP}	Input buffer	—	1.68	—	1.92	—	2.26	ns
t_{PY}	Output buffer	—	12.14	—	13.83	—	16.26	ns
t_{ENZL}	Enable to pad delay through the output buffer—Z to low	—	12.43	—	14.16	—	16.65	ns
t_{ENZH}	Enable to pad delay through the output buffer—Z to high	—	12.17	—	13.86	—	16.30	ns
t_{ENLZ}	Enable to pad delay through the output buffer—low to Z	—	1.73	—	1.74	—	1.75	ns
t_{ENHZ}	Enable to pad delay through the output buffer—high to Z	—	2.22	—	2.23	—	2.24	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{IOCLKY}	Clock-to-Output Y for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVTTL Output Drive Strength = 1 (8 mA)/Low Slew Rate								
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.38	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{DP}	Input buffer	—	1.68	—	1.92	—	2.26	ns
t_{PY}	Output buffer	—	11.03	—	12.56	—	14.77	ns
t_{ENZL}	Enable to pad delay through the output buffer—Z to low	—	11.42	—	13.01	—	15.29	ns
t_{ENZH}	Enable to pad delay through the output buffer—Z to high	—	11.04	—	12.58	—	14.79	ns
t_{ENLZ}	Enable to pad delay through the output buffer—low to Z	—	1.86	—	1.88	—	1.88	ns
t_{ENHZ}	Enable to pad delay through the output buffer—high to Z	—	2.50	—	2.51	—	2.52	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{IOCLKY}	Clock-to-Output Y for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{DP}	Input buffer	—	1.68	—	1.92	—	2.26	ns
t_{PY}	Output buffer	—	10.45	—	11.90	—	13.99	ns
t_{ENZL}	Enable to pad delay through the output buffer—Z to low	—	10.61	—	12.08	—	14.21	ns
t_{ENZH}	Enable to pad delay through the output buffer—Z to high	—	10.47	—	11.93	—	14.02	ns
t_{ENLZ}	Enable to pad delay through the output buffer—low to Z	—	1.92	—	1.94	—	1.94	ns
t_{ENHZ}	Enable to pad delay through the output buffer—high to Z	—	2.57	—	2.58	—	2.59	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{IOCLKY}	Clock-to-Output Y for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVTTL Output Drive Strength = 1 (8 mA)/Low Slew Rate								
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{DP}	Input buffer	—	1.68	—	1.92	—	2.26	ns
t_{PY}	Output buffer	—	4.23	—	4.81	—	5.66	ns
t_{ENZL}	Enable to pad delay through the output buffer—Z to low	—	4.64	—	5.28	—	6.21	ns
t_{ENZH}	Enable to pad delay through the output buffer—Z to high	—	4.23	—	4.81	—	5.66	ns
t_{ENLZ}	Enable to pad delay through the output buffer—low to Z	—	1.89	—	1.91	—	1.91	ns
t_{ENHZ}	Enable to pad delay through the output buffer—high to Z	—	2.01	—	2.02	—	2.03	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{DP}	Input buffer	—	1.68	—	1.92	—	2.26	ns
t_{PY}	Output buffer	—	3.30	—	3.76	—	4.42	ns
t_{ENZL}	Enable to pad delay through the output buffer—Z to low	—	3.74	—	4.26	—	5.00	ns
t_{ENZH}	Enable to pad delay through the output buffer—Z to high	—	3.06	—	3.49	—	4.10	ns
t_{ENLZ}	Enable to pad delay through the output buffer—low to Z	—	1.89	—	1.91	—	1.91	ns
t_{ENHZ}	Enable to pad delay through the output buffer—high to Z	—	2.29	—	2.30	—	2.31	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVTTL Output Drive Strength = 1 (8 mA)/Low Slew Rate								
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{DP}	Input buffer	—	1.68	—	1.92	—	2.26	ns
t_{PY}	Output buffer	—	3.12	—	3.56	—	4.18	ns
t_{ENZL}	Enable to pad delay through the output buffer—Z to low	—	3.54	—	4.04	—	4.75	ns
t_{ENZH}	Enable to pad delay through the output buffer—Z to high	—	2.78	—	3.17	—	3.72	ns
t_{ENLZ}	Enable to pad delay through the output buffer—low to Z	—	1.91	—	1.93	—	1.93	ns
t_{ENHZ}	Enable to pad delay through the output buffer—high to Z	—	2.58	—	2.59	—	2.60	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{DP}	Input buffer	—	1.68	—	1.92	—	2.26	ns
t_{PY}	Output buffer	—	2.99	—	3.41	—	4.01	ns
t_{ENZL}	Enable to pad delay through the output buffer—Z to low	—	2.49	—	2.51	—	2.51	ns
t_{ENZH}	Enable to pad delay through the output buffer—Z to high	—	2.59	—	2.95	—	3.46	ns
t_{ENLZ}	Enable to pad delay through the output buffer—low to Z	—	1.91	—	1.93	—	1.93	ns
t_{ENHZ}	Enable to pad delay through the output buffer—high to Z	—	3.56	—	4.06	—	4.77	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVTTL Output Drive Strength = 1 (8 mA)/Low Slew Rate								
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

2.3.8 2.5V LVCMOS

Low-Voltage Complementary Metal-Oxide Semiconductor (LVCMOS) for 2.5V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5V applications. It uses a 3.3V tolerant CMOS input buffer and a push-pull output buffer.

The following table lists the DC input and output levels of 2.5V LVCMOS.

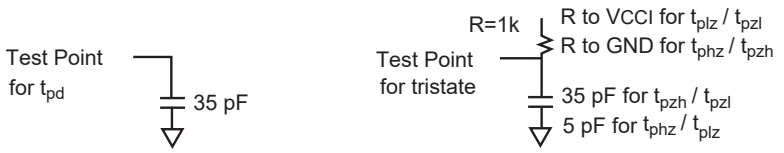
Table 2-28. DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
–0.3	0.7	1.7	3.6	0.4	2.0	12	–12

2.3.8.1 AC Loadings

The following figure shows AC test loads.

Figure 2-16. AC Test Loads



The following table lists the AC loading values.

Table 2-29. AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point[1] (V)	VREF (typ) (V)	Cload (pF)
0	2.5	1.25	N/A	35

Note:

1. Measuring Point = VTRIP

2.3.8.2 Timing Characteristics

The following table lists the timing characteristics of 2.5V LVCMOS.

Table 2-30. 2.5V LVCMOS I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 2.3V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS25 I/O Module Timing								
t_{DP}	Input buffer	—	1.95	—	2.22	—	2.61	ns
t_{PY}	Output buffer	—	3.29	—	3.74	—	4.40	ns
t_{ENZL}	Enable to pad delay through the output buffer —Z to low	—	2.48	—	2.50	—	2.51	ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS25 I/O Module Timing								
t_{ENZH}	Enable to pad delay through the output buffer —Z to high	—	2.48	—	2.50	—	2.51	ns
t_{ENLZ}	Enable to pad delay through the output buffer —low to Z	—	5.74	—	6.54	—	7.69	ns
t_{ENHZ}	Enable to pad delay through the output buffer —high to Z	—	6.60	—	7.51	—	8.83	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

2.3.9 1.8V LVCMOS

Low-Voltage Complementary Metal-Oxide Semiconductor (LVCMOS) for 1.8V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.8V applications. It uses a 3.3V tolerant CMOS input buffer and a push-pull output buffer.

The following table lists the DC input and output levels of 1.8V LVCMOS.

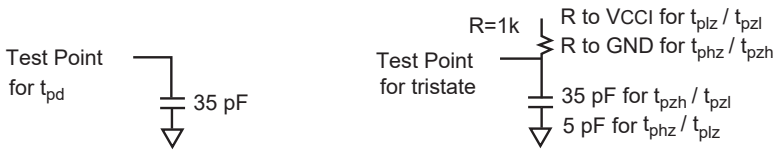
Table 2-31. DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
–0.3	0.2 VCCI	0.7 VCCI	3.6	0.2	VCCI – 0.2	8 mA	–8 mA

2.3.9.1 AC Loadings

The following figure shows AC test loads.

Figure 2-17. AC Test Loads



The following table lists the AC loading values.

Table 2-32. AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point[1] (V)	VREF (typ) (V)	Cload (pF)
0	1.8	0.5 VCCI	N/A	35

© 2024 Microchip Technology Inc. and its subsidiaries

Note:

1. Measuring Point = VTRIP

2.3.9.2 Timing Characteristics

The following table lists the timing characteristics of 1.8V LVCMOS.

Table 2-33. 1.8V LVCMOS I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 1.7V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS18 Output Module Timing								
t_{DP}	Input buffer	—	3.26	—	3.71	—	4.37	ns
t_{PY}	Output buffer	—	4.55	—	5.18	—	6.09	ns
t_{ENZL}	Enable to pad delay through the output buffer —Z to low	—	2.82	—	2.83	—	2.84	ns
t_{ENZH}	Enable to pad delay through the output buffer —Z to high	—	3.43	—	3.45	—	3.46	ns
t_{ENLZ}	Enable to pad delay through the output buffer —low to Z	—	6.01	—	6.85	—	8.05	ns
t_{ENHZ}	Enable to pad delay through the output buffer —high to Z	—	6.73	—	7.67	—	9.01	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

2.3.10 1.5V LVCMOS (JESD8-11)

Low-Voltage Complementary Metal-Oxide Semiconductor (LVCMOS) for 1.5V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 1.5V applications. It uses a 3.3V tolerant CMOS input buffer and a push-pull output buffer.

The following table lists the DC input and output levels of 1.5V LVCMOS.

Table 2-34. DC Input and Output Levels

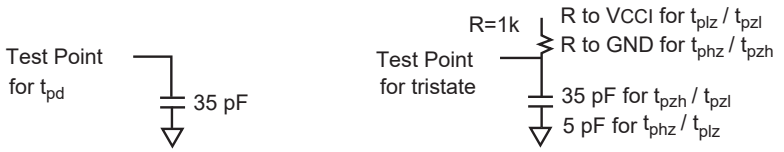
VIL		VIH		VOL	VOH	IOL	IOH
Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
–0.3	0.35 VCCI	0.65 VCCI	3.6	0.4	VCCI – 0.4	8 mA	–8 mA

2.3.10.1 AC Loadings

The following figure shows AC test loads.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-18. AC Test Loads



The following table lists the AC loading values.

Table 2-35. AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point[1] (V)	VREF (typ) (V)	Cload (pF)
0	1.5	0.5VCCI	N/A	35

Note:

1. Measuring Point = VTRIP

2.3.10.2 Timing Characteristics

The following table lists the timing characteristics of 1.5V LVCMOS.

Table 2-36. 1.5V LVCMOS I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 1.4V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS15 (JESD8-11) I/O Module Timing								
t_{DP}	Input buffer	—	3.59	—	4.09	—	4.81	ns
t_{PY}	Output buffer	—	6.05	—	6.89	—	8.10	ns
t_{ENZL}	Enable to pad delay through the output buffer —Z to low	—	3.31	—	3.34	—	3.34	ns
t_{ENZH}	Enable to pad delay through the output buffer —Z to high	—	4.56	—	4.58	—	4.59	ns
t_{ENLZ}	Enable to pad delay through the output buffer —low to Z	—	6.37	—	7.25	—	8.52	ns
t_{ENHZ}	Enable to pad delay through the output buffer —high to Z	—	6.94	—	7.90	—	9.29	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

2.3.11 3.3V PCI, 3.3V PCI-X

Peripheral Component Interface (PCI) for 3.3V standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTL input buffer and a push-pull output buffer. The input and

© 2024 Microchip Technology Inc. and its subsidiaries

output buffers are 5V tolerant with the aid of external components. Axcelerator 3.3V PCI and 3.3V PCI-X buffers are compliant with the PCI Local Bus Specification Rev. 2.1.

The PCI Compliance Specification requires the clamp diodes to be able to withstand for 11 ns, –3.5V in undershoot, and 7.1V in overshoot.

The following table lists the DC input and output levels of 3.3V PCI and 3.3V PCI-X.

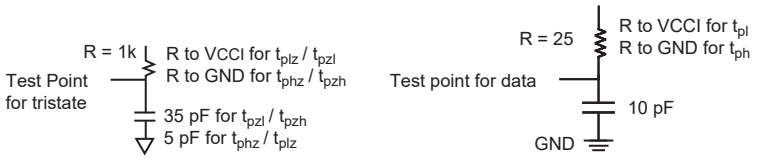
Table 2-37. DC Input and Output Levels

Standard	VIL		VIH		VOL	VOH	IOL	IOH
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
PCI	–0.3	0.3 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			
PCI-X	–0.5	0.35 VCCI	0.5 VCCI	VCCI + 0.5	(per PCI specification)			

2.3.11.1 AC Loadings

The following figure shows AC test loads.

Figure 2-19. AC Test Loads



The following table lists the AC loading values.

Table 2-38. AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point[1] (V)	VREF (typ) (V)	Cload (pF)
(Per PCI Spec and PCI-X Spec)			N/A	10

Note:

1. Measuring Point = VTRIP

2.3.11.2 Timing Characteristics

The following table lists the timing characteristics of 3.3V PCI.

Table 2-39. 3.3V PCI I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
3.3V PCI Output Module Timing								
t_{DP}	Input buffer	—	1.57	—	1.79	—	2.10	ns
t_{PY}	Output buffer	—	1.91	—	2.18	—	2.56	ns
t_{ENZL}	Enable to pad delay through the output buffer—Z to low	—	1.61	—	1.62	—	1.63	ns
t_{ENZH}	Enable to pad delay through the output buffer—Z to high	—	1.45	—	1.47	—	1.47	ns
t_{ENLZ}	Enable to pad delay through the output buffer—low to Z	—	2.55	—	2.90	—	3.41	ns
t_{ENHZ}	Enable to pad delay through the output buffer—high to Z	—	3.52	—	4.01	—	4.72	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
3.3V PCI Output Module Timing								
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39		0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39		0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37		0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	—
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

The following table lists the timing characteristics of 3.3V PCI-X.

Table 2-40. 3.3V PCI-X I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

—		–2 Speed		–1 Speed		Std Speed		Units
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	
3.3V PCI-X Output Module Timing								
t_{DP}	Input buffer	—	1.57	—	1.79	—	2.10	ns
t_{PY}	Output buffer	—	2.10	—	2.40	—	2.82	ns
t_{ENZL}	Enable to pad delay through the output buffer —Z to low	—	1.61	—	1.62	—	1.63	ns
t_{ENZH}	Enable to pad delay through the output buffer —Z to high	—	1.59	—	1.60	—	1.61	ns
t_{ENLZ}	Enable to pad delay through the output buffer —low to Z	—	2.65	—	3.02	—	3.55	ns
t_{ENHZ}	Enable to pad delay through the output buffer —high to Z	—	3.11	—	3.55	—	4.17	ns
t_{IOCLKQ}	Sequential Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{IOCLKY}	Clock-to-output Y for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

© 2024 Microchip Technology Inc. and its subsidiaries

2.4 Voltage-Referenced I/O Standards

2.4.1 GTL+

Gunning Transceiver Logic Plus (GTL+) is a high-speed bus standard (JESD8-3). It requires a differential amplifier input buffer and an Open Drain output buffer. The VCCI pin should be connected to 2.5V or 3.3V. Note that 2.5V GTL+ is not supported across the full military temperature range.

The following table lists the DC input and output levels of GTL+.

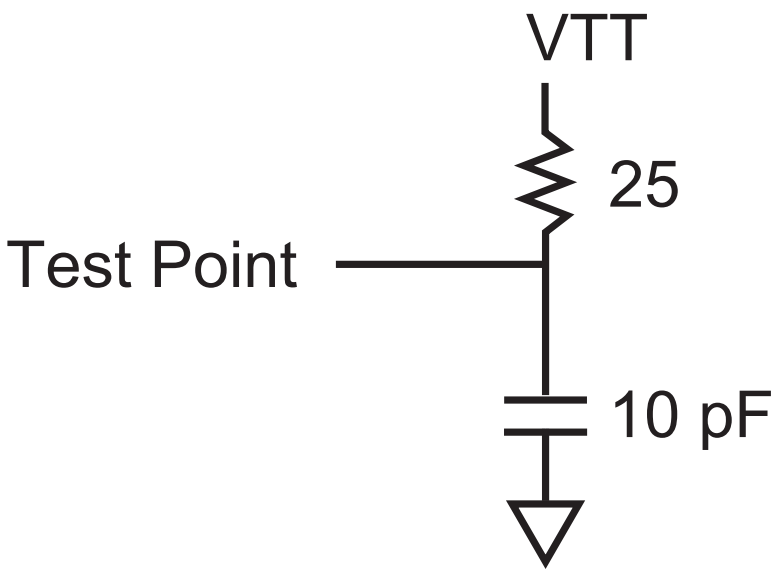
Table 2-41. DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
N/A	VREF – 0.1	VREF + 0.1	N/A	0.6	NA	NA	NA

2.4.1.1 AC Loadings

The following figure shows AC test loads.

Figure 2-20. AC Test Loads



The following table lists the AC loading values.

Table 2-42. AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point[1] (V)	VREF (typ) (V)	Cload (pF)
VREF – 0.2	VREF + 0.2	VREF	1.0	10

Note:

1. Measuring Point = VTRIP

2.4.1.2 Timing Characteristics

The following table lists the timing characteristics of 2.5V GTL+.

© 2024 Microchip Technology Inc. and its subsidiaries

Table 2-43. 2.5V GTL+ I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 2.3V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
2.5V GTL+ I/O Module Timing								
t_{DP}	Input buffer	—	1.71	—	1.95	—	2.29	ns
t_{PY}	Output buffer	—	1.13	—	1.29	—	1.52	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

The following table lists the timing characteristics of 3.3V GTL+.

Table 2-44. 3.3V GTL+ I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
3.3V GTL+I/O Module Timing								
t_{DP}	Input buffer	—	1.71	—	1.95	—	2.29	ns
t_{PY}	Output buffer	—	1.13	—	1.29	—	1.52	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

2.4.2 HSTL Class I

High-Speed Transceiver Logic (HSTL) is a general purpose high-speed 1.5V bus standard (EIA/JESD8-6). The Axcelerator devices support Class I. This requires a differential amplifier input buffer and a push-pull output buffer.

The following table lists the DC input and output levels of HSTL Class I.

© 2024 Microchip Technology Inc. and its subsidiaries

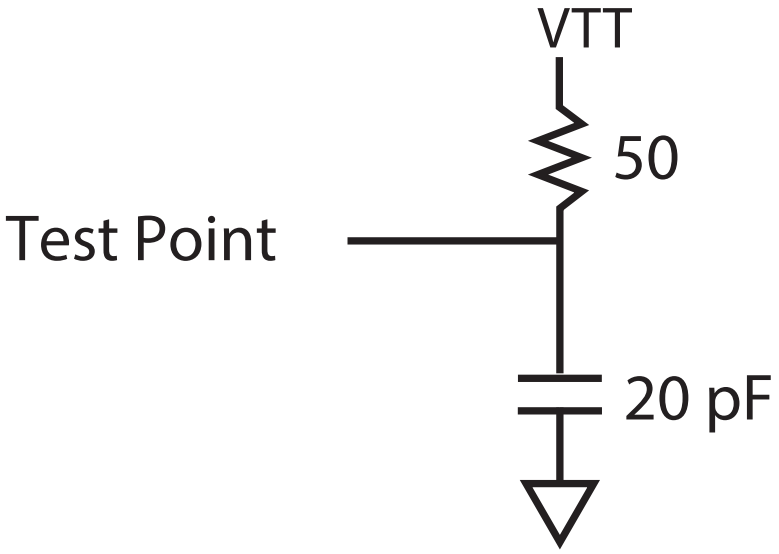
Table 2-45. DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
–0.3	VREF – 0.1	VREF + 0.1	3.6	0.4	VCC – 0.4	8	–8

2.4.2.1 AC Loadings

The following figure shows AC test loads.

Figure 2-21. AC Test Loads



The following table lists the AC loading values.

Table 2-46. AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point[1] (V)	VREF (typ) (V)	Cload (pF)
VREF –0.5	VREF + 0.5	VREF	0.75	20

Note:

1. Measuring Point = VTRIP

2.4.2.2 Timing Characteristics

The following table lists the timing characteristics of 1.5V HSTL Class I.

Table 2-47. 1.5V HSTL Class I I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 1.425V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
1.5V HSTL Class I I/O Module Timing								
t_{DP}	Input buffer	—	1.80	—	2.05	—	2.41	ns
t_{PY}	Output buffer	—	4.90	—	5.58	—	6.56	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
1.5V HSTL Class I I/O Module Timing								
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

2.4.3 SSTL2

Stub Series Terminated Logic (SSTL) for 2.5V is a general purpose 2.5V memory bus standard (JESD8-9). The Axcelerator devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

2.4.3.1 Class I

The following table lists the DC input and output levels of SSTL2 Class I.

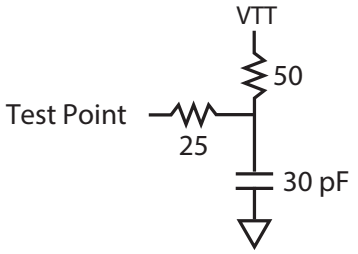
Table 2-48. DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
–0.3	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.57	VREF + 0.57	7.6	–7.6

2.4.3.1.1 AC Loadings

The following figure shows AC test loads.

Figure 2-22. AC Test Loads



The following table lists the AC loading values.

Table 2-49. AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point[1] (V)	VREF (typ) (V)	Cload (pF)
VREF – 0.75	VREF + 0.75	VREF	1.25	30

Note:

1. Measuring Point = VTRIP

2.4.3.1.2 Timing Characteristics

The following table lists the timing characteristics of 2.5V SSTL2 Class I.

© 2024 Microchip Technology Inc. and its subsidiaries

Table 2-50. 2.5V SSTL2 Class I I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 2.3V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
2.5V SSTL2 Class I I/O Module Timing								
t_{DP}	Input buffer	—	1.83	—	2.08	—	2.45	ns
t_{PY}	Output buffer	—	2.39	—	2.72	—	3.20	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

2.4.3.2 Class II

The following table lists the DC input and output levels of SSTL2 Class II.

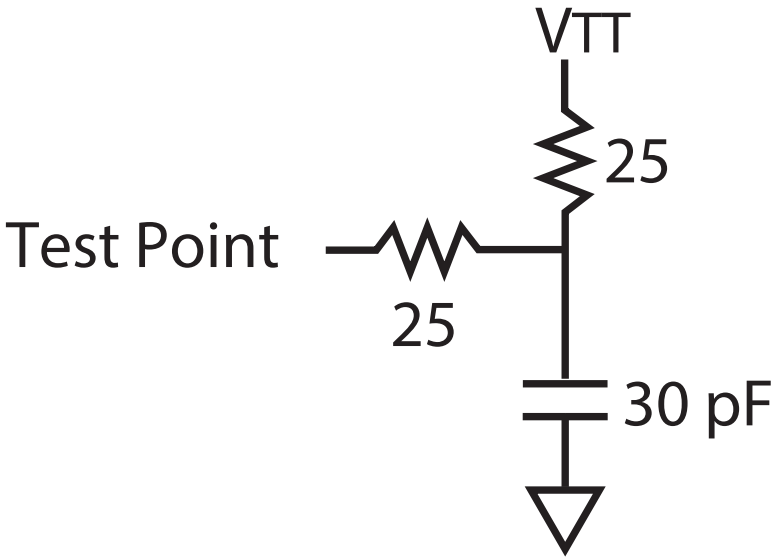
Table 2-51. DC Input and Output Levels

VIL		VIH		VOL	VOH	IOL	IOH
Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
-0.3	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.8	VREF + 0.8	15.2	-15.2

2.4.3.2.1 AC Loadings

The following figure shows AC test loads.

Figure 2-23. AC Test Loads



© 2024 Microchip Technology Inc. and its subsidiaries

The following table lists the AC loading values.

Table 2-52. AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point[1] (V)	VREF (typ) (V)	Cload (pF)
VREF – 0.75	VREF + 0.75	VREF	1.25	30

Note:

1. Measuring Point = Vtrip

2.4.3.2.2 Timing Characteristics

The following table lists the timing characteristics of 2.5V SSTL2 Class II.

Table 2-53. 2.5V SSTL2 Class II I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 2.3V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
2.5V SSTL2 Class II I/O Module Timing								
t_{DP}	Input buffer	—	1.89	—	2.16	—	2.53	ns
t_{PY}	Output buffer	—	2.39	—	2.72	—	3.20	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

2.4.4 SSTL3

Stub Series Terminated Logic (SSTL) for 3.3V is a general-purpose 3.3V memory bus standard (JESD8-8). The Axcelerator devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

2.4.4.1 Class I

The following table lists the DC input and output levels of SSTL3 Class I.

Table 2-54. DC Input and Output Levels

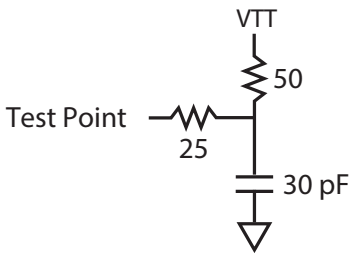
VIL		VIH		VOL	VOH	IOL	IOH
Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
-0.3	VREF – 0.2	VREF +0.2	3.6	VREF – 0.6	VREF + 0.6	8	–8

2.4.4.1.1 AC Loadings

The following figure shows AC test loads.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-24. AC Test Loads



The following table lists the AC loading values.

Table 2-55. AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point[1] (V)	VREF (typ) (V)	Cload (pF)
VREF – 1.0	VREF + 1.0	VREF	1.50	30

Note:

1. Measuring Point = VTRIP

2.4.4.1.2 Timing Characteristics

The following table lists the timing characteristics of 3.3V SSTL3 Class I.

Table 2-56. 3.3V SSTL3 Class I I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
3.3V SSTL3 Class I I/O Module Timing								
t_{DP}	Input buffer	—	1.78	—	2.03	—	2.39	ns
t_{PY}	Output buffer	—	2.17	—	2.47	—	2.91	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

2.4.4.2 Class II

The following table lists the DC input and output levels of SSTL3 Class II.

Table 2-57. DC Input and Output Levels

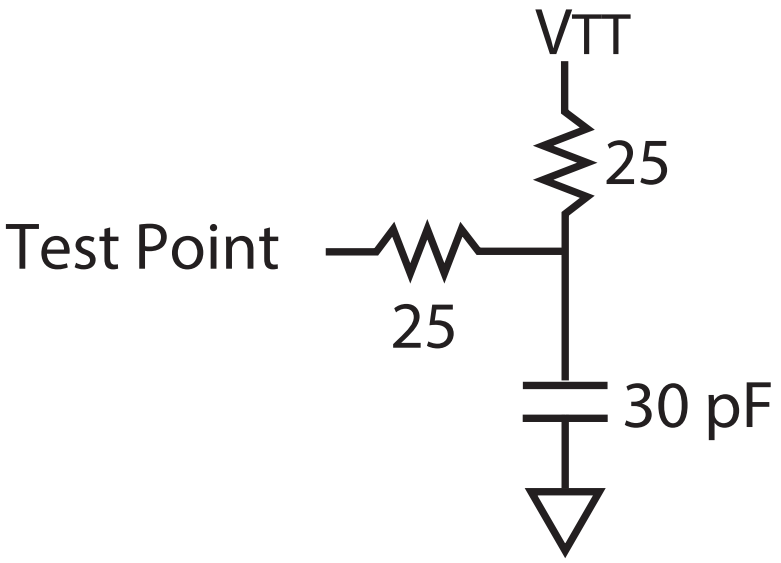
VIL		VIH		VOL	VOH	IOL	IOH
Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
-0.3	VREF – 0.2	VREF + 0.2	3.6	VREF – 0.8	VREF + 0.8	16	–16

© 2024 Microchip Technology Inc. and its subsidiaries

2.4.4.2.1 AC Loadings

The following figure shows AC test loads.

Figure 2-25. AC Test Loads



The following table lists the AC loading values.

Table 2-58. AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point[1] (V)	VREF (typ) (V)	Cload (pF)
VREF – 1.0	VREF + 1.0	VREF	1.50	30

Note:

1. Measuring Point = VTRIP

2.4.4.2.2 Timing Characteristics

The following table lists the timing characteristics of 3.3V SSTL3 Class II.

Table 2-59. 3.3V SSTL3 Class II I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
3.3V SSTL3 Class II I/O Module Timing								
t_{DP}	Input buffer	—	1.85	—	2.10	—	2.47	ns
t_{PY}	Output buffer	—	2.17	—	2.47	—	2.91	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
3.3V SSTL3 Class II I/O Module Timing								
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

2.5 Differential Standards

2.5.1 Physical Implementation

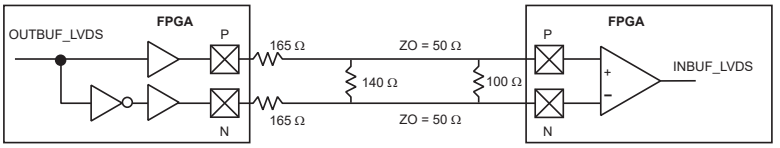
Implementing differential I/O standards requires the configuration of a pair of external I/O pads, resulting in a single internal signal. To facilitate construction of the differential pair, a single I/O Cluster contains the resources for a pair of I/Os. Configuration of the I/O Cluster as a differential pair is handled by Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with these standards.

2.5.2 LVDS

Low-Voltage Differential Signal (LVDS) (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit is carried through two signal lines, so two pins are needed. It also requires an external resistor termination. The voltage swing between these two signal lines is approximately 350 mV.

Figure 2-26. LVDS Board-Level Implementation



The LVDS circuit consists of a differential driver connected to a terminated receiver through a constant-impedance transmission line. The receiver is a wide-common-mode-range differential amplifier. The common-mode range is from 0.2V to 2.2V for a differential input with 400 mV swing.

To implement the driver for the LVDS circuit, drivers from two adjacent I/O cells are used to generate the differential signals (note that the driver is not a current-mode driver). This driver provides a nominal constant current of 3.5 mA. When this current flows through a 100Ω termination resistor on the receiver side, a voltage swing of 350 mV is developed across the resistor. The direction of the current flow is controlled by the data fed to the driver.

An external-resistor network (three resistors) is needed to reduce the voltage swing to about 350 mV. Therefore, four external resistors are required, three for the driver and one for the receiver.

The following table lists the DC input and output levels of LVDS.

Table 2-60. DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI[1]	Supply voltage	2.375	2.5	2.625	V
VOH	Output high voltage	1.25	1.425	1.6	V
VOL	Output low voltage	0.9	1.075	1.25	V

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued					
DC Parameter	Description	Min.	Typ.	Max.	Units
VODIFF	Differential output voltage	250	350	450	mV
VOCM	Output common mode voltage	1.125	1.25	1.375	V
VICM2	Input common mode voltage	0.2	1.25	2.2	V

Notes:

1. ±5%
2. Differential input voltage = ±350 mV.

The following table lists the AC loading values.

Table 2-61. AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point[1] (V)
1.2 – 0.125	1.2 + 0.125	1.2

Note:

1. Measuring Point = VTRIP

2.5.2.1 Timing Characteristics

The following table lists the timing characteristics of LVDS.

Table 2-62. LVDS I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 2.3V, T_J = 70 °C

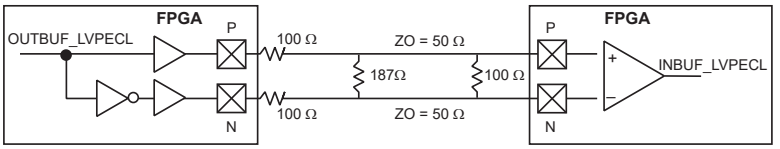
Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVDS Output Module Timing								
t_{DP}	Input buffer	—	1.80	—	2.05	—	2.41	ns
t_{PY}	Output buffer	—	2.32	—	2.64	—	3.11	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

2.5.3 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit is carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination. The voltage swing between these two signal lines is approximately 850 mV.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-27. LVPECL Board-Level Implementation



The LVPECL circuit is similar to the LVDS scheme. It requires four external resistors, three for the driver and one for the receiver. The values for the three driver resistors are different from that of LVDS since the output voltage levels are different. The VOH levels are 200 mV below the standard LVPECL levels.

The following table lists the DC input and output levels of LVPECL.

Table 2-63. DC Input and Output Levels

DC Parameter	Min.		Typ.		Max.		Units
	Min.	Max.	Min.	Max.	Min.	Max.	
VCCI	3		3.3		3.6		V
VOH	1.8	2.11	1.92	2.28	2.13	2.41	V
VOL	0.96	1.27	1.06	1.43	1.3	1.57	V
VIH	1.49	2.72	1.49	2.72	1.49	2.72	V
VIL	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential input voltage	0.3		0.3		0.3		V

The following table lists the AC loading values.

Table 2-64. AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point[1] (V)
1.6 – 0.3	1.6 + 0.3	1.6

Note:

1. Measuring Point = VTRIP

2.5.3.1 Timing Characteristics

The following table lists the timing characteristics of LVPECL.

Table 2-65. LVPECL I/O Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVPECL Output Module Timing								
t_{DP}	Input buffer	—	1.66	—	1.89	—	2.22	ns
t_{PY}	Output buffer	—	2.24	—	2.55	—	3.00	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register	—	0.67	—	0.77	—	0.90	ns
t_{OCLKQ}	Clock-to-Q for the I/O output register and the I/O enable register	—	0.67	—	0.77	—	0.90	ns
t_{SUD}	Data input set-up	—	0.23	—	0.27	—	0.31	ns
t_{SUE}	Enable input set-up	—	0.26	—	0.30	—	0.35	ns
t_{HD}	Data input hold	—	0.00	—	0.00	—	0.00	ns
t_{HE}	Enable input hold	—	0.00	—	0.00	—	0.00	ns
t_{CPWHL}	Clock pulse width high to low	0.39	—	0.39	—	0.39	—	ns
t_{CPWLH}	Clock pulse width low to high	0.39	—	0.39	—	0.39	—	ns
t_{WASYN}	Asynchronous pulse width	0.37	—	0.37	—	0.37	—	ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVPECL Output Module Timing								
t_{REASYN}	Asynchronous recovery time	—	0.13	—	0.15	—	0.17	ns
t_{HASYN}	Asynchronous removal time	—	0.00	—	0.00	—	0.00	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.23	—	0.27	—	0.31	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.23	—	0.27	—	0.31	ns

2.6 Module Specifications

2.6.1 C-Cell

The C-cell is one of the two logic module types in the AX architecture. It is the combinatorial logic resource in the Axcelerator device. The AX architecture implements a new combinatorial cell that is an extension of the C-cell implemented in the SX-A family. The main enhancement of the new C-cell is the addition of carry-chain logic.

The C-cell can be used in a carry-chain mode to construct arithmetic functions. If carry-chain logic is not required, it can be disabled.

The following is the list of C-cell features.

- Eight-input MUX (data: D0-D3, select: A0, A1, B0, B1). User signals can be routed to any one of these inputs. Any of the C-cell inputs (D0-D3, A0, A1, B0, B1) can be tied to one of the four routed clocks (CLKE/F/G/H).
- Inverter (DB input) can be used to drive a complement signal of any of the inputs to the C-cell
- A carry input and a carry output. The carry input signal of the C-cell is the carry output from the C-cell directly to the north.
- Carry connect for carry-chain logic with a signal propagation time of less than 0.1 ns
- A hardwired connection (direct connect) to the adjacent R-cell (Register Cell) for all C-cells on the east side of a SuperCluster with a signal propagation time of less than 0.1 ns

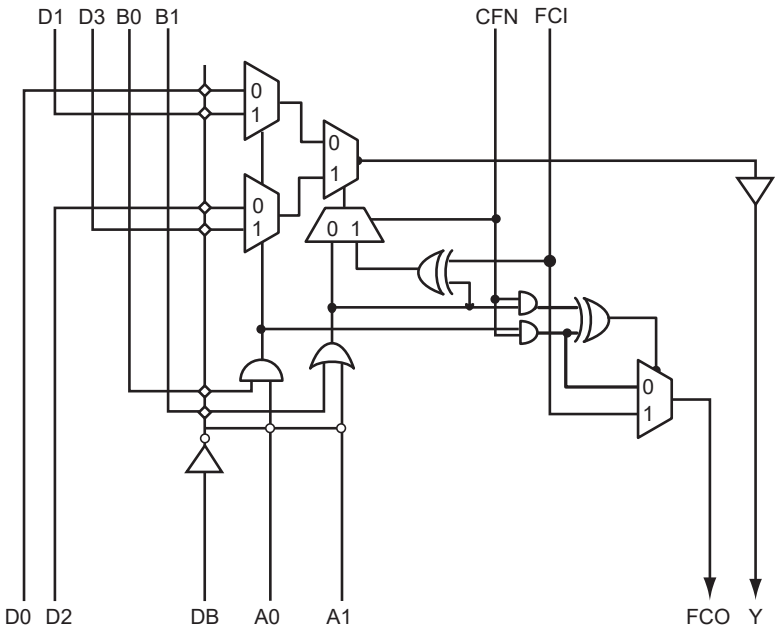
This layout of the C-cell (and the C-cell Cluster) enables the implementation of over 4,000 functions of up to five bits. For example, two C-cells can be used together to implement a four-input XOR function in a single cell delay.

The carry-chain configuration is handled automatically for the user with Microchip's extensive macro library (For a complete listing of available Axcelerator macros, see the Antifuse Macro Library Guide Macro Library Guide).

The following figure shows C-Cell.

© 2024 Microchip Technology Inc. and its subsidiaries

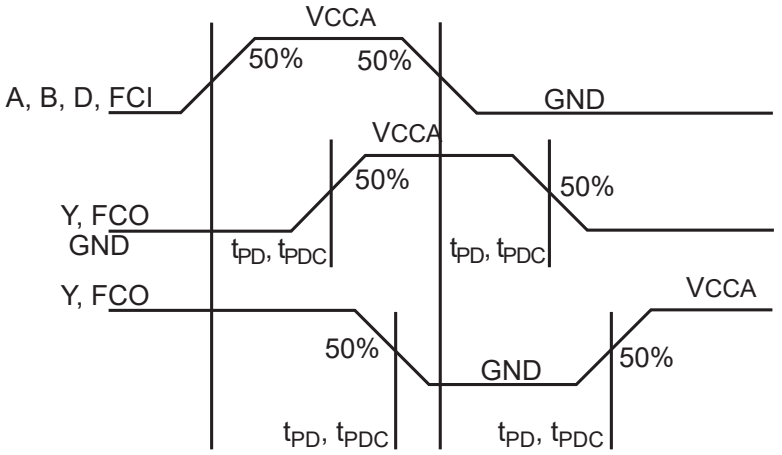
Figure 2-28. C-Cell



2.6.1.1 Timing Model and Waveforms

The following figure shows C-Cell timing model and waveforms.

Figure 2-29. C-Cell Timing Model and Waveforms



2.6.1.2 Timing Characteristics

The following table lists the timing characteristics of C-Cell.

Table 2-66. C-Cell Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays								
t_{PD}	Any input to output Y	—	0.74	—	0.84	—	0.99	ns
t_{PDC}	Any input to carry chain output (FCO)	—	0.57	—	0.64	—	0.76	ns
t_{PDB}	Any input through DB when one input is used	—	0.95	—	1.09	—	1.28	ns
t_{CCY}	Input to carry chain (FCI) to Y	—	0.61	—	0.69	—	0.82	ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
C-Cell Propagation Delays								
t_{CC}	Input to carry chain (FCI) to carry chain output (FCO)	—	0.08	—	0.09	—	0.11	ns

2.6.2 Carry-Chain Logic

The Axcelerator dedicated carry-chain logic offers a very compact solution for implementing arithmetic functions without sacrificing performance.

To implement the carry-chain logic, two C-cells in a Cluster are connected together so the FCO (that is, carry out) for the two bits is generated in a carry look-ahead scheme to achieve minimum propagation delay from the FCI (that is, carry in) into the two-bit Cluster. The two-bit carry logic is shown in the following figure.

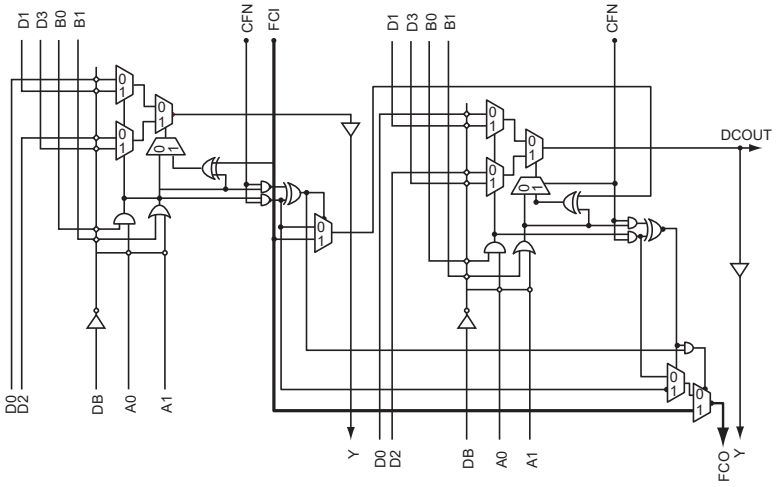
The FCI of one C-cell pair is driven by the FCO of the C-cell pair immediately above it. Similarly, the FCO of one C-cell pair, drives the FCI input of the C-cell pair immediately below it (see Figure 1-4 and Figure 2-31).

The carry-chain logic is selected via the CFN input. When carry logic is not required, this signal is deasserted to save power. Again, this configuration is handled automatically for the user through Microchip's macro library.

The signal propagation delay between two C-cells in the carry-chain sequence is 0.1 ns.

The following figure shows the two-bit carry logic of Axcelerator device.

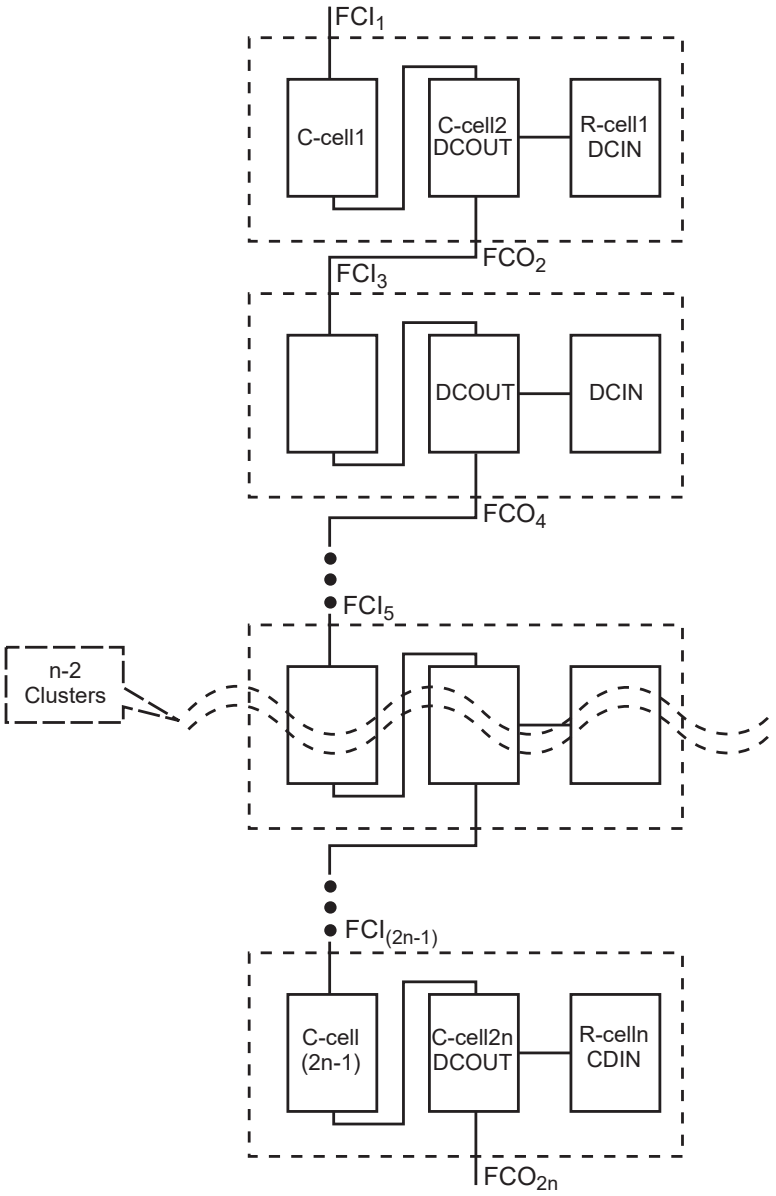
Figure 2-30. Axcelerator's Two-Bit Carry Logic



The following figure shows carry-chain sequencing of C-Cells.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-31. Carry-Chain Sequencing of C-Cells



2.6.2.1 Timing Characteristics

For more information on carry-chain timing characteristics, see Table 2-66.

2.6.3 R-Cell

The R-cell, the sequential logic resource of the Axcelerator devices, is the second logic module type in the AX family architecture. It includes clock inputs for all eight global resources of the Axcelerator architecture as well as global presets and clears (see the following figure).

The main features of the R-cell include the following:

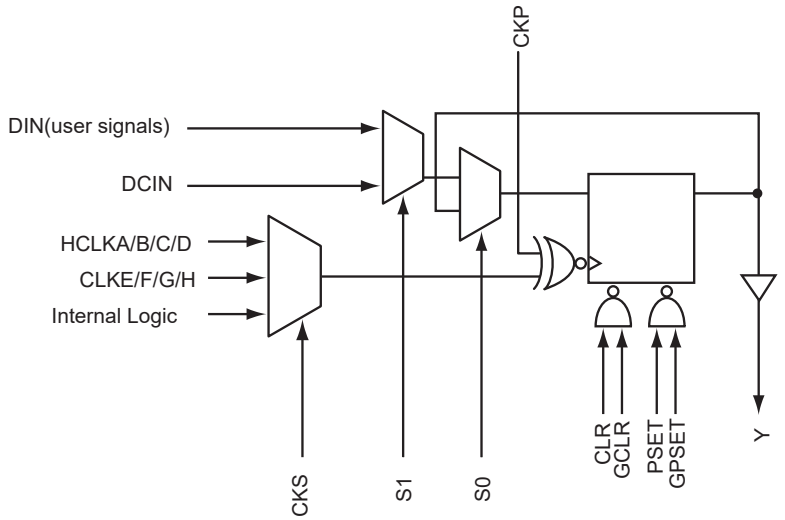
- Direct connection to the adjacent logic module through the hardwired connection DCIN. DCIN is driven by the DCOUT of an adjacent C-cell via the Direct-Connect routing resource, providing a connection with less than 0.1 ns of routing delay.

© 2024 Microchip Technology Inc. and its subsidiaries

- The R-cell can be used as a standalone flip-flop. It can be driven by any C-cell or I/O modules through the regular routing structure (using DIN as a routable data input). This gives the option of using the R-Cell as a 2:1 MUXed flip-flop as well.
- Provision of data enable-input (S0)
- Independent active-low asynchronous clear (CLR)
- Independent active-low asynchronous preset (PSET). If both CLR and PSET are low, CLR has higher priority
- Clock can be driven by any of the following (CKP selects clock polarity).
  - One of the four high performance hardwired fast clocks (HCLKs)
  - One of the four routed clocks (CLKs)
  - User signals
- Global Power-On Clear (GCLR) and Global Power-On Preset (GPSET), which drive each flip-flop on a chip-wide basis.
  - When the Global Set Fuse option in the Designer software is unchecked (by default), GCLR = 0 and GPSET = 1 at device power-up. When the option is checked, GCLR = 1 and GPSET = 0. Both pins are pulled High when the device is in user mode. For information on simulation support, see the "Simulation Support for GCLR/GPSET in Axcelerator" section in the Antifuse Macro Library Guide.
- S0, S1, PSET, and CLR can be driven by routed clocks CLKE/F/G/H or user signals.
- DIN and S1 can be driven by user signals.

As with the C-cell, the configuration of the R-cell to perform various functions is handled automatically for the user through Microchip's extensive macro library (for a complete listing of available AX macros, see the Antifuse Macro Library Guide).

Figure 2-32. R-Cell

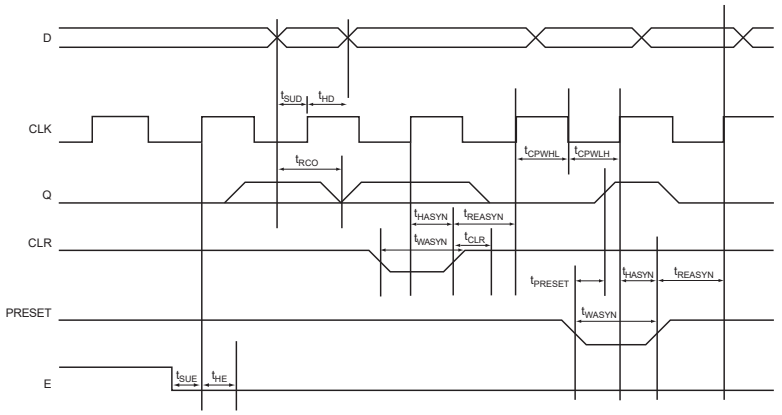


2.6.3.1 Timing Models and Waveforms

The following figure shows R-Cell delays.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-33. R-Cell Delays



2.6.3.2 Timing Characteristics

The following table lists the timing characteristics of R-Cell.

Table 2-67. R-Cell Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
R-Cell Propagation Delays								
t_{RCO}	Sequential Clock-to-Q	—	0.67	—	0.77	—	0.90	ns
t_{CLR}	Asynchronous Clear-to-Q	—	0.67	—	0.77	—	0.90	ns
t_{PRESET}	Asynchronous Preset-to-Q	—	0.36	—	0.36	—	0.36	ns
t_{SUD}	Flip-flop data input set-up	—	0.34	—	0.34	—	0.34	ns
t_{SUE}	Flip-flop enable input set-up	—	0.00	—	0.00	—	0.00	ns
t_{HD}	Flip-flop data input hold	—	0.67	—	0.77	—	0.90	ns
t_{HE}	Flip-flop enable input hold	—	0.67	—	0.77	—	0.90	ns
t_{WASYN}	Asynchronous pulse width	0.48	—	0.48	—	0.48	—	ns
t_{REASYN}	Asynchronous recovery time	—	0.23	—	0.27	—	0.31	ns
t_{HASYN}	Asynchronous removal time	—	0.36	—	0.36	—	0.36	ns
t_{CPWHL}	Clock pulse width high to low	0.36	—	0.36	—	0.36	—	ns
t_{CPWLH}	Clock pulse width low to high	0.36	—	0.36	—	0.36	—	ns

2.6.4 Buffer Module

An additional resource inside each SuperCluster is the Buffer (B) module (see Figure 1-4). When a fanout constraint is applied to a design, the synthesis tool inserts buffers as needed. The buffer module has been added to the AX architecture to avoid logic duplication resulting from the hard fanout constraints. The router utilizes this logic resource to save area and reduce loading and delays on medium to high fanout nets.

2.6.4.1 Timing Models and Waveforms

The following figures show the timing model and waveform of buffer module.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-34. Buffer Module Timing Model

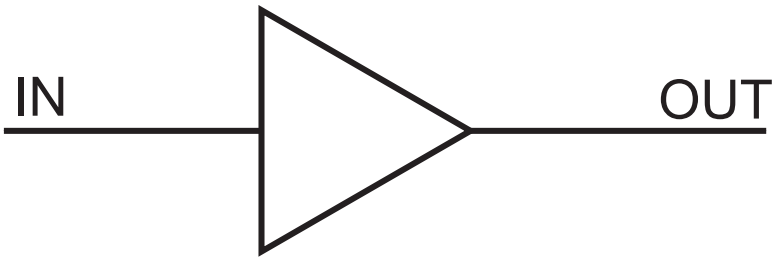
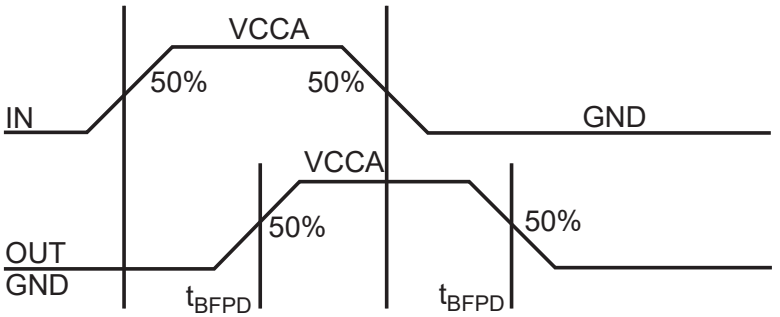


Figure 2-35. Buffer Module Waveform



2.6.4.2 Timing Characteristics

The following table lists the timing characteristics of buffer module.

Table 2-68. Buffer Module Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Buffer Module Propagation Delays								
t_{BFPD}	Any input to output Y	—	0.12	—	0.14	—	0.16	ns

2.7 Routing Specifications

2.7.1 Routing Resources

The routing structure found in Axcelerator devices enables any logic module to be connected to any other logic module while retaining high performance. There are multiple paths and routing resources that can be used to route one logic module to another, both within a SuperCluster and elsewhere on the chip.

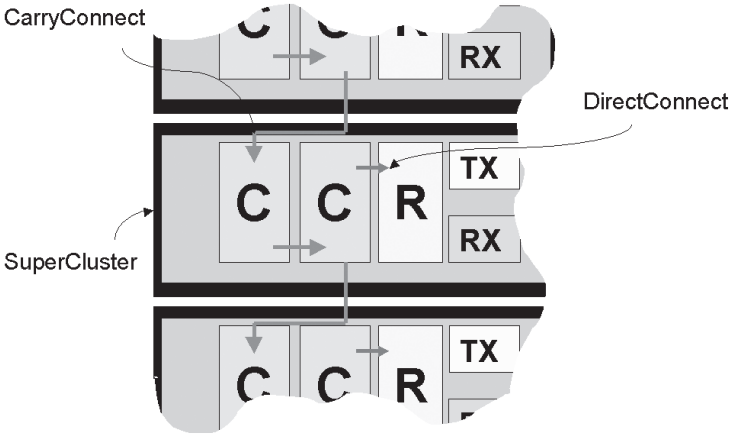
There are four primary types of routing within the AX architecture: DirectConnect, CarryConnect, FastConnect, and Vertical and Horizontal Routing.

2.7.1.1 DirectConnect

DirectConnects provide a high-speed connection between an R-cell and its adjacent C-cell (see the following figure). This connection can be made from DCOUT of the C-cell to DCIN of the R-cell by configuring of the S1 line of the R-cell. This provides a connection that does not require an antifuse and has a delay of less than 0.1 ns.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-36. DirectConnect and CarryConnect



2.7.1.2 CarryConnect

CarryConnects are used to build carry chains for arithmetic functions (see Figure 2-36). The FCO output of the right C-cell of a two C-cell Cluster drives the FCI input of the left C-cell in the two C-cell Cluster immediately below it. This pattern continues down both sides of each SuperCluster column.

Similar to the DirectConnects, CarryConnects can be built without an antifuse connection. This connection has a delay of less than 0.1 ns from the FCO of one two C-cell cluster to the FCI of the two C-cell cluster immediately below it (see Carry-Chain Logic for more information).

2.7.1.3 FastConnect

For high-speed routing of logic signals, FastConnects can be used to build a short distance connection using a single antifuse (see Figure 2-38). FastConnects provide a maximum delay of 0.3 ns. The outputs of each logic module connect directly to the Output Tracks within a SuperCluster. Signals on the Output Tracks can then be routed through a single antifuse connection to drive the inputs of logic modules either within one SuperCluster or in the SuperCluster immediately below it.

2.7.1.4 Vertical and Horizontal Routing

Vertical and Horizontal Tracks provide both local and long distance routing (see the following figure). These tracks are composed of both short-distance, segmented routing, and across-chip routing tracks (segmented at core tile boundaries). The short-distance, segmented routing resources can be concatenated through antifuse connections to build longer routing tracks.

These short-distance routing tracks can be used within and between SuperClusters or between modules of non-adjacent SuperClusters. They can be connected to the Output Tracks and to any logic module input (R-cell, C-cell, Buffer, and TX module).

The across-chip horizontal and vertical routing provides long-distance routing resources. These resources interface with the rest of the routing structures through the RX and TX modules (see the following figure). The RX module is used to drive signals from the across-chip horizontal and vertical routing to the Output Tracks within the SuperCluster. The TX module is used to drive vertical and horizontal across-chip routing from either short-distance horizontal tracks or from Output Tracks. The TX module can also be used to drive signals from vertical across-chip tracks to horizontal across-chip tracks and vice versa.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-37. Horizontal and Vertical Tracks

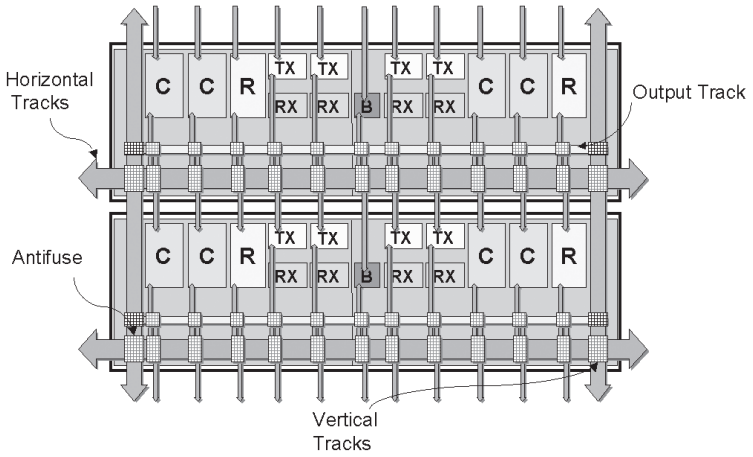
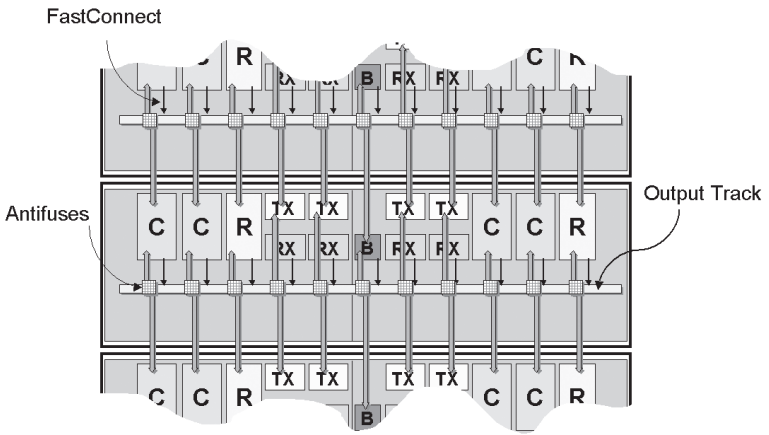


Figure 2-38. FastConnect Routing



2.7.1.5 Timing Characteristics

The following table lists the predicted routing delays of Axcelerator devices.

Table 2-69. AX125 Predicted Routing Delays Worst-Case Commercial Conditions VCCA = 1.425V, T_J = 70 °C

Parameter	Description	–2 Speed	–1 Speed	Std Speed	UnitsUnits
		Typical	Typical	Typical	
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.35	0.40	0.47	ns
t_{RD2}	Routing delay for FO2	0.38	0.43	0.51	ns
t_{RD3}	Routing delay for FO3	0.43	0.48	0.57	ns
t_{RD4}	Routing delay for FO4	0.48	0.55	0.64	ns
t_{RD5}	Routing delay for FO5	0.55	0.62	0.73	ns
t_{RD6}	Routing delay for FO6	0.64	0.72	0.85	ns
t_{RD7}	Routing delay for FO7	0.79	0.89	1.05	ns
t_{RD8}	Routing delay for FO8	0.88	0.99	1.17	ns
t_{RD16}	Routing delay for FO16	1.49	1.69	1.99	ns
t_{RD32}	Routing delay for FO32	2.32	2.63	3.10	ns

© 2024 Microchip Technology Inc. and its subsidiaries

Table 2-70. AX250 Predicted Routing Delays Worst-Case Commercial Conditions VCCA = 1.425V, T_J = 70 °C

Parameter	Description	–2 Speed	–1 Speed	Std Speed	UnitsUnits
		Typical	Typical	Typical	
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.39	0.45	0.53	ns
t_{RD2}	Routing delay for FO2	0.41	0.46	0.54	ns
t_{RD3}	Routing delay for FO3	0.48	0.55	0.64	ns
t_{RD4}	Routing delay for FO4	0.56	0.63	0.75	ns
t_{RD5}	Routing delay for FO5	0.60	0.68	0.80	ns
t_{RD6}	Routing delay for FO6	0.84	0.96	1.13	ns
t_{RD7}	Routing delay for FO7	0.90	1.02	1.20	ns
t_{RD8}	Routing delay for FO8	1.00	1.13	1.33	ns
t_{RD16}	Routing delay for FO16	2.17	2.46	2.89	ns
t_{RD32}	Routing delay for FO32	3.55	4.03	4.74	ns

Table 2-71. AX500 Predicted Routing Delays Worst-Case Commercial Conditions VCCA = 1.425V, T_J = 70 °C

Parameter	Description	–2 Speed	–1 Speed	Std Speed	UnitsUnits
		Typical	Typical	Typical	
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.11	0.12	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.39	0.45	0.53	ns
t_{RD2}	Routing delay for FO2	0.41	0.46	0.54	ns
t_{RD3}	Routing delay for FO3	0.48	0.55	0.64	ns
t_{RD4}	Routing delay for FO4	0.56	0.63	0.75	ns
t_{RD5}	Routing delay for FO5	0.60	0.68	0.80	ns
t_{RD6}	Routing delay for FO6	0.84	0.96	1.13	ns
t_{RD7}	Routing delay for FO7	0.90	1.02	1.20	ns
t_{RD8}	Routing delay for FO8	1.00	1.13	1.33	ns
t_{RD16}	Routing delay for FO16	2.17	2.46	2.89	ns
t_{RD32}	Routing delay for FO32	3.55	4.03	4.74	ns

Table 2-72. AX1000 Predicted Routing Delays Worst-Case Commercial Conditions VCCA = 1.425V, T_J = 70 °C

Parameter	Description	–2 Speed	–1 Speed	Std Speed	UnitsUnits
		Typical	Typical	Typical	
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.12	0.13	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.45	0.51	0.60	ns
t_{RD2}	Routing delay for FO2	0.53	0.60	0.71	ns
t_{RD3}	Routing delay for FO3	0.56	0.63	0.74	ns
t_{RD4}	Routing delay for FO4	0.63	0.71	0.84	ns
t_{RD5}	Routing delay for FO5	0.73	0.82	0.97	ns
t_{RD6}	Routing delay for FO6	0.99	1.13	1.32	ns
t_{RD7}	Routing delay for FO7	1.02	1.15	1.36	ns
t_{RD8}	Routing delay for FO8	1.48	1.68	1.97	ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2 Speed	–1 Speed	Std Speed	UnitsUnits
		Typical	Typical	Typical	
Predicted Routing Delays					
t_{RD16}	Routing delay for FO16	2.57	2.91	3.42	ns
t_{RD32}	Routing delay for FO32	4.24	4.81	5.65	ns

Table 2-73. AX2000 Predicted Routing Delays Worst-Case Commercial Conditions VCCA = 1.425V, T_J = 70 °C

Parameter	Description	–2 Speed	–1 Speed	Std Speed	UnitsUnits
		Typical	Typical	Typical	
Predicted Routing Delays					
t_{DC}	DirectConnect Routing Delay, FO1	0.12	0.13	0.15	ns
t_{FC}	FastConnect Routing Delay, FO1	0.35	0.39	0.46	ns
t_{RD1}	Routing delay for FO1	0.50	0.56	0.66	ns
t_{RD2}	Routing delay for FO2	0.59	0.67	0.79	ns
t_{RD3}	Routing delay for FO3	0.70	0.80	0.94	ns
t_{RD4}	Routing delay for FO4	0.76	0.87	1.02	ns
t_{RD5}	Routing delay for FO5	0.98	1.11	1.31	ns
t_{RD6}	Routing delay for FO6	1.48	1.68	1.97	ns
t_{RD7}	Routing delay for FO7	1.65	1.87	2.20	ns
t_{RD8}	Routing delay for FO8	1.73	1.96	2.31	ns
t_{RD16}	Routing delay for FO16	2.58	2.92	3.44	ns
t_{RD32}	Routing delay for FO32	4.24	4.81	5.65	ns

2.8 Global Resources

One of the most important aspects of any FPGA architecture is its global resources or clocks. The Axcelerator family provides the user with flexible and easy-to-use global resources, without the limitations normally found in other FPGA architectures.

The AX architecture contains two types of global resources, the Hardwired Clock (HCLK) and Routed Clock (CLK). Every Axcelerator device is provided with four HCLKs and four CLKs for a total of eight clocks, regardless of device density.

2.8.1 Hardwired Clocks

The Hardwired Clock (HCLK) is a low-skew network that can directly drive the clock inputs of all sequential modules (R-cells, I/O registers, and embedded RAM/FIFOs) in the device with no antifuse in the path. All four HCLKs are available everywhere on the chip.

Timing Characteristics

The following tables lists the dedicated (hardwired) array clock networks of Axcelerator devices.

Table 2-74. AX125 Dedicated (Hardwired) Array Clock Networks Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input low to high	—	3.02	—	3.44	—	4.05	ns
t_{HCKH}	Input high to low	—	3.03	—	3.46	—	4.06	ns
t_{HPWH}	Minimum pulse width high	0.58	—	0.65	—	0.77	—	ns
t_{HPWL}	Minimum pulse width low	0.52	—	0.59	—	0.69	—	ns
t_{HCKSW}	Maximum skew	—	0.06	—	0.07	—	0.08	ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t_{HP}	Minimum period	1.15	—	1.31	—	1.54	—	ns
t_{HMAX}	maximum frequency	—	870	—	763	—	649	MHz

Table 2-75. AX250 Dedicated (Hardwired) Array Clock Networks Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input low to high	—	2.57	—	2.93	—	3.45	ns
t_{HCKH}	Input high to low	—	2.61	—	2.97	—	3.50	ns
t_{HPWH}	Minimum pulse width high	0.58	—	0.65	—	0.77	—	ns
t_{HPWL}	Minimum pulse width low	0.52	—	0.59	—	0.69	—	ns
t_{HCKSW}	Maximum skew	—	0.06	—	0.07	—	0.08	ns
t_{HP}	Minimum period	1.15	—	1.31	—	1.54	—	ns
t_{HMAX}	maximum frequency	—	870	—	763	—	649	MHz

Table 2-76. AX500 Dedicated (Hardwired) Array Clock Networks Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input low to high	—	2.35	—	2.68	—	3.15	ns
t_{HCKH}	Input high to low	—	2.44	—	2.79	—	3.27	ns
t_{HPWH}	Minimum pulse width high	0.58	—	0.65	—	0.77	—	ns
t_{HPWL}	Minimum pulse width low	0.52	—	0.59	—	0.69	—	ns
t_{HCKSW}	Maximum skew	—	0.06	—	0.07	—	0.08	ns
t_{HP}	Minimum period	1.15	—	1.31	—	1.54	—	ns
t_{HMAX}	maximum frequency	—	870	—	763	—	649	MHz

Table 2-77. AX1000 Dedicated (Hardwired) Array Clock Networks Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input low to high	—	3.02	—	3.44	—	4.05	ns
t_{HCKH}	Input high to low	—	3.03	—	3.46	—	4.06	ns
t_{HPWH}	Minimum pulse width high	0.58	—	0.65	—	0.77	—	ns
t_{HPWL}	Minimum pulse width low	0.52	—	0.59	—	0.69	—	ns
t_{HCKSW}	Maximum skew	—	0.06	—	0.07	—	0.08	ns
t_{HP}	Minimum period	1.15	—	1.31	—	1.54	—	ns
t_{HMAX}	maximum frequency	—	870	—	763	—	649	MHz

© 2024 Microchip Technology Inc. and its subsidiaries

Table 2-78. AX2000 Dedicated (Hardwired) Array Clock Networks Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Dedicated (Hardwired) Array Clock Networks								
t_{HCKL}	Input low to high	—	3.02	—	3.44	—	4.05	ns
t_{HCKH}	Input high to low	—	3.03	—	3.46	—	4.06	ns
t_{HPWH}	Minimum pulse width high	0.58	—	0.65	—	0.77	—	ns
t_{HPWL}	Minimum pulse width low	0.52	—	0.59	—	0.69	—	ns
t_{HCKSW}	Maximum skew	—	0.06	—	0.07	—	0.08	ns
t_{HP}	Minimum period	1.15	—	1.31	—	1.54	—	ns
t_{HMAX}	Maximum frequency	—	870	—	763	—	649	MHz

2.8.2 Routed Clocks

The Routed Clock (CLK) is a low-skew network that can drive the clock inputs of all sequential modules in the device (logically equivalent to the HCLK), but has the added flexibility in that it can drive the S0 (Enable), S1, PSET, and CLR input of a register (R-cells and I/O registers) as well as any of the inputs of any C-cell in the device. This allows CLKs to be used not only as clocks, but also for other global signals or high fanout nets. All four CLKs are available everywhere on the chip.

2.8.2.1 Timing Characteristics

The following tables lists the routed array clock networks of Axcelerator devices.

Table 2-79. AX125 Routed Array Clock Networks Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Routed Array Clock Networks								
t_{RCKL}	Input low to high	—	3.08	—	3.50	—	4.12	ns
t_{RCKH}	Input high to low	—	3.13	—	3.56	—	4.19	ns
t_{RPWH}	Minimum pulse width high	0.57	—	0.64	—	0.75	—	ns
t_{RPWL}	Minimum pulse width low	0.52	—	0.59	—	0.69	—	ns
t_{RCKSW}	Maximum skew	—	0.35	—	0.39	—	0.46	ns
t_{RP}	Minimum period	1.15	—	1.31	—	1.54	—	ns
t_{RMAX}	Maximum frequency	—	870	—	763	—	649	MHz

Table 2-80. AX250 Routed Array Clock Networks Worst-Case Commercial Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 70°C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Routed Array Clock Networks								
t_{RCKL}	Input low to high	—	2.52	—	2.87	—	3.37	ns
t_{RCKH}	Input high to low	—	2.59	—	2.95	—	3.47	ns
t_{RPWH}	Minimum pulse width high	0.57	—	0.64	—	0.75	—	ns
t_{RPWL}	Minimum pulse width low	0.52	—	0.59	—	0.69	—	ns
t_{RCKSW}	Maximum skew	—	0.35	—	0.39	—	0.46	ns
t_{RP}	Minimum period	1.15	—	1.31	—	1.54	—	ns
t_{RMAX}	Maximum frequency	—	870	—	763	—	649	MHz

© 2024 Microchip Technology Inc. and its subsidiaries

Table 2-81. AX500 Routed Array Clock Networks Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Routed Array Clock Networks								
t_{RCKL}	Input low to high	—	2.31	—	2.63	—	3.09	ns
t_{RCKH}	Input high to low	—	2.44	—	2.78	—	3.27	ns
t_{RPWH}	Minimum pulse width high	0.57	—	0.64	—	0.75	—	ns
t_{RPWL}	Minimum pulse width low	0.52	—	0.59	—	0.69	—	ns
t_{RCKSW}	Maximum skew	—	0.35	—	0.39	—	0.46	ns
t_{RP}	Minimum period	1.15	—	1.31	—	1.54	—	ns
t_{RMAX}	Maximum frequency	—	870	—	763	—	649	MHz

Table 2-82. AX1000 Routed Array Clock Networks Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Routed Array Clock Networks								
t_{RCKL}	Input low to high	—	3.08	—	3.50	—	4.12	ns
t_{RCKH}	Input high to low	—	3.13	—	3.56	—	4.19	ns
t_{RPWH}	Minimum pulse width high	0.57	—	0.64	—	0.75	—	ns
t_{RPWL}	Minimum pulse width low	0.52	—	0.59	—	0.69	—	ns
t_{RCKSW}	Maximum skew	—	0.35	—	0.39	—	0.46	ns
t_{RP}	Minimum period	1.15	—	1.31	—	1.54	—	ns
t_{RMAX}	Maximum frequency	—	870	—	763	—	649	MHz

Table 2-83. AX2000 Routed Array Clock Networks Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

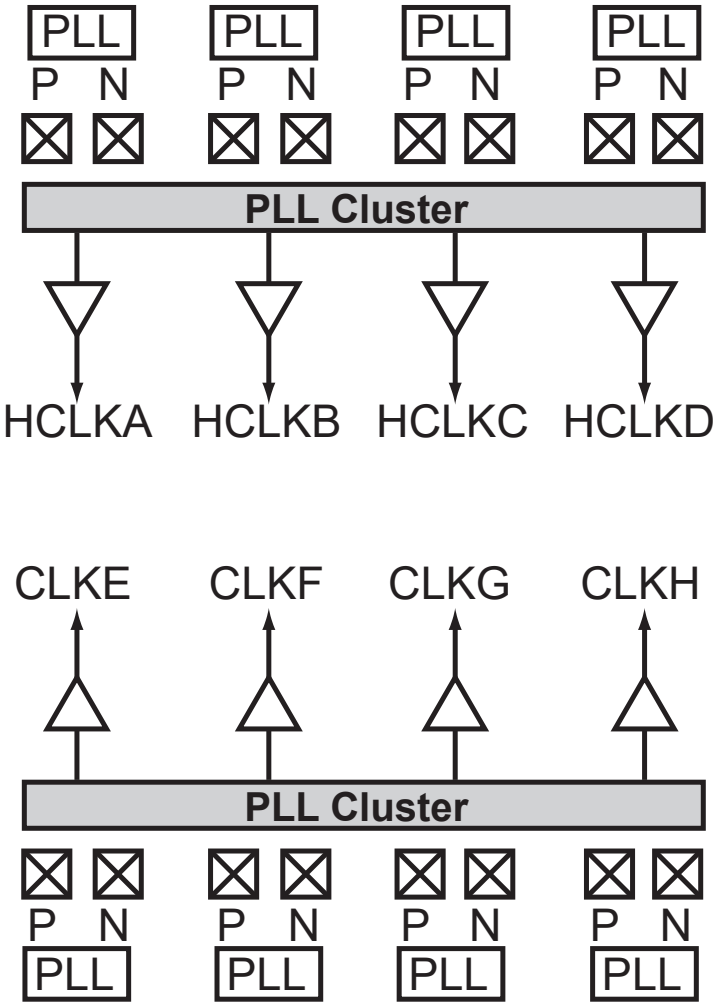
Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Routed Array Clock Networks								
t_{RCKL}	Input low to high	—	3.08	—	3.50	—	4.12	ns
t_{RCKH}	Input high to low	—	3.13	—	3.56	—	4.19	ns
t_{RPWH}	Minimum pulse width high	0.57	—	0.64	—	0.75	—	ns
t_{RPWL}	Minimum pulse width low	0.52	—	0.59	—	0.69	—	ns
t_{RCKSW}	Maximum skew	—	0.35	—	0.39	—	0.46	ns
t_{RP}	Minimum period	1.15	—	1.31	—	1.54	—	ns
t_{RMAX}	Maximum frequency	—	870	—	763	—	649	MHz

2.8.3 Global Resource Distribution

At the root of each global resource is a PLL. There are two groups of four PLLs for every device. One group, located at the center of the north edge (in the I/O ring) of the chip, sources the four HCLKs. The second group, located at the center of the south edge (again in the I/O ring), sources the four CLKs (see the following figure).

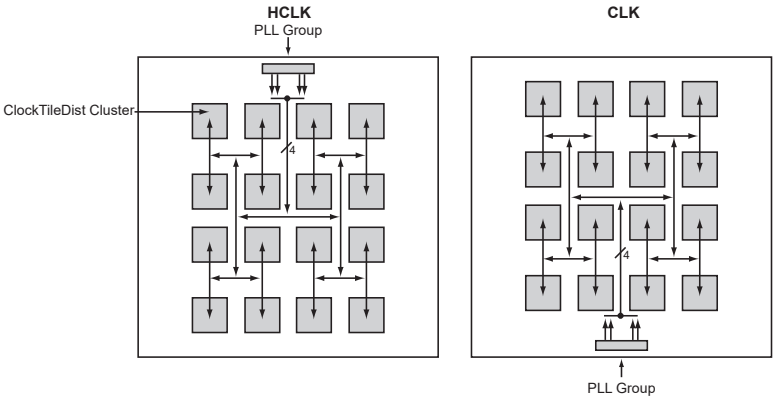
© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-39. PLL Group



Regardless of the type of global resource, HCLK or CLK, each of the eight resources reach the ClockTileDist (CTD) Cluster located at the center of every core tile with zero skew. From the ClockTileDist Cluster, all four HCLKs and four CLKs are distributed through the core tile (see the following figure).

Figure 2-40. Example of HCLK and CLK Distributions on the AX2000



© 2024 Microchip Technology Inc. and its subsidiaries

The ClockTileDist Cluster contains an HCLKMux (HM) module for each of the four HCLK trees and a CLKMux (CM) module for each of the CLK trees. The HCLK branches then propagate horizontally through the middle of the core tile to HCLKColDist (HD) modules in every SuperCluster column. The CLK branches propagate vertically through the center of the core tile to CLKRowDist (RD) modules in every SuperCluster row. Together, the HCLK and CLK branches provide for a low-skew global fanout within the core tile (see the following figures).

Figure 2-41. CTD, CD, and HD Module Layout

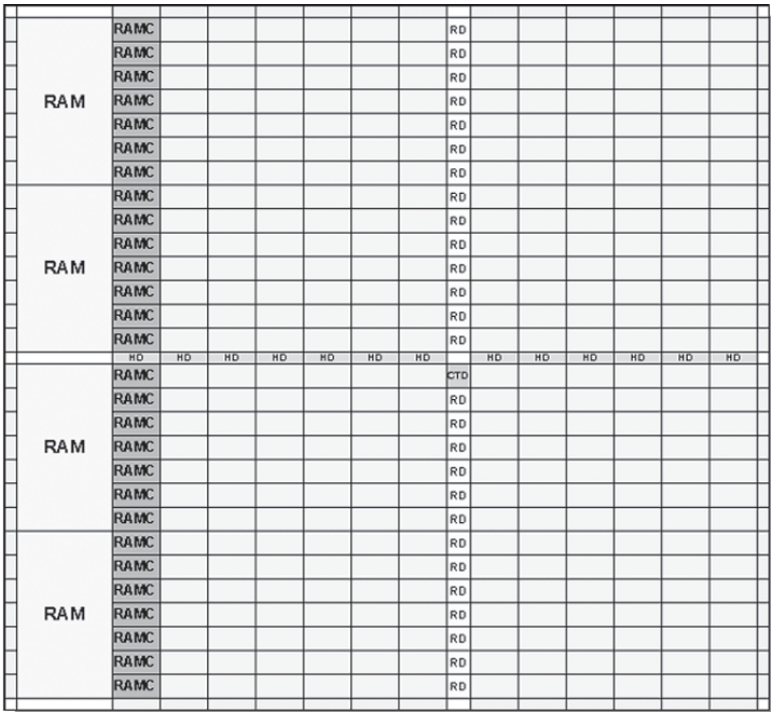
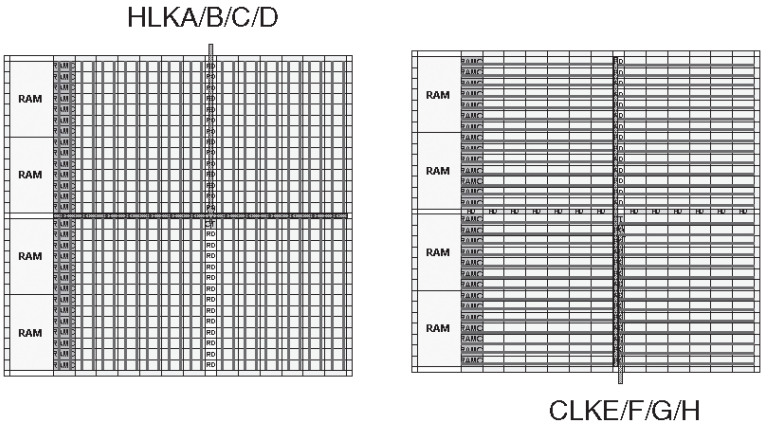


Figure 2-42. HCLK and CLK Distribution within a Core Tile



The HM and CM modules can select between:

- The HCLK or CLK source respectively
- A local signal routed on generic routing resources

This allows each core tile to have eight clocks independent of the other core tiles in the device.

© 2024 Microchip Technology Inc. and its subsidiaries

Both HCLK and CLK are segmentable, meaning that individual branches of the global resource can be used independently.

Like the HM and CM modules, the HD and RD modules can select between:

- The HCLK or CLK source from the HM or CM module respectively
- A local signal routed on generic routing resources

The AX architecture is capable of supporting a large number of local clocks—24 segments per HCLK driving north-south and 28 segments per CLK driving east-west per core tile.

Microchip's Designer software's place-and-route takes advantage of the segmented clock structure found in Axcelerator devices by turning off any unused clock segments. This results in not only better performance but also lower power consumption.

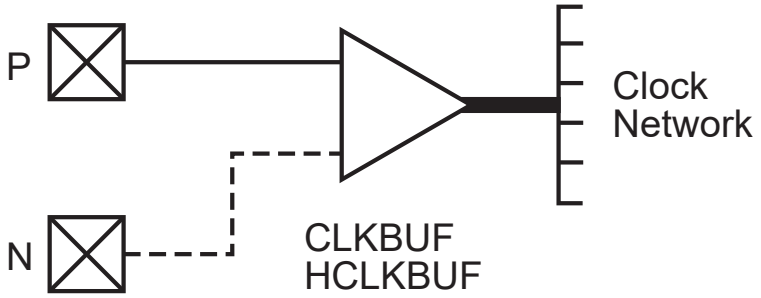
2.8.4 Global Resource Access Macros

Global resources can be driven by one of three sources: external pad(s), an internal net, or the output of a PLL. These connections can be made by using one of three types of macros: CLKBUF, CLKINT, and PLLCLK.

2.8.4.1 CLKBUF and HCLKBUF

CLKBUF (HCLKBUF) is used to drive a CLK (HCLK) from external pads. These macros can be used either generically or with the specific I/O standard desired (for example, CLKBUF_LVCMOS25, HCLKBUF_LVDS, and so on). See the following figure.

Figure 2-43. CLKBUF and HCLKBUF



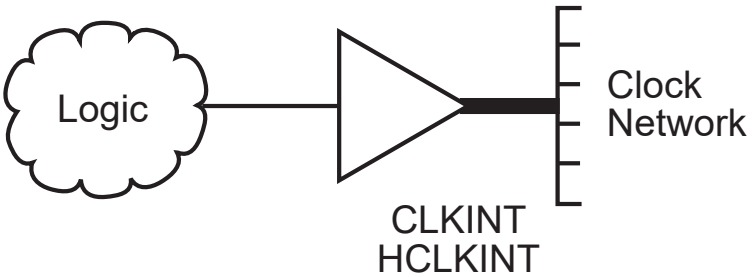
Package pins CLKEP and CLKEN are associated with CLKE, package pins HCLKAP and HCLKAN are associated with HCLKA, and so on.

Note that when CLKBUF (HCLKBUF) is used with a single-ended I/O standard, it must be tied to the P-pad of the CLK (HCLK) package pin. In this case, the CLK (HCLK) N-pad can be used for user signals.

2.8.4.2 CLKINT and HCLKINT

CLKINT (HCLKINT) is used to access the CLK (HCLK) resource internally from the user signals (see the following figure).

Figure 2-44. CLKINT and HCLKINT

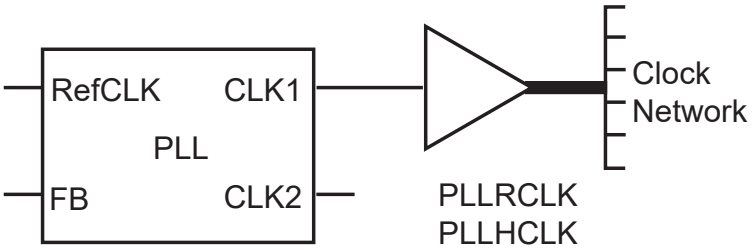


© 2024 Microchip Technology Inc. and its subsidiaries

2.8.4.3 PLLRCLK and PLLHCLK

PLLRCLK (PLLHCLK) is used to drive global resource CLK (HCLK) from a PLL (see the following figure).

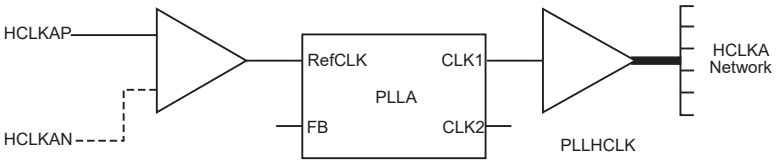
Figure 2-45. PLLRCLK and PLLHCLK



2.8.5 Using Global Resources with PLLs

Each global resource has an associated PLL at its root. For example, PLLA can drive HCLKA, PLLE can drive CLKE, and so on. (see the following figure).

Figure 2-46. Example of HCLKA Driven from a PLL with External Clock Source



In addition, each clock pin of the package can be used to drive either its associated global resource or PLL. For example, package pins CLKEP and CLKEN can drive either the RefCLK input of PLLE or CLKE.

There are two macros required when interfacing the embedded PLLs with the global resources: PLLINT and PLLOUT.

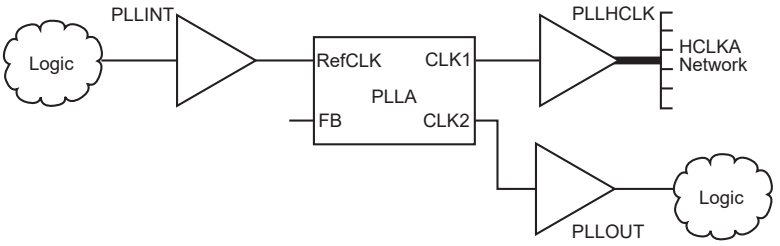
2.8.5.1 PLLINT

This macro is used to drive the RefCLK input of the PLL internally from user signals.

2.8.5.2 PLLOUT

This macro is used to connect either the CLK1 or CLK2 output of a PLL to the regular routing network (see the following figure).

Figure 2-47. Example of PLLINT and PLLOUT Usage

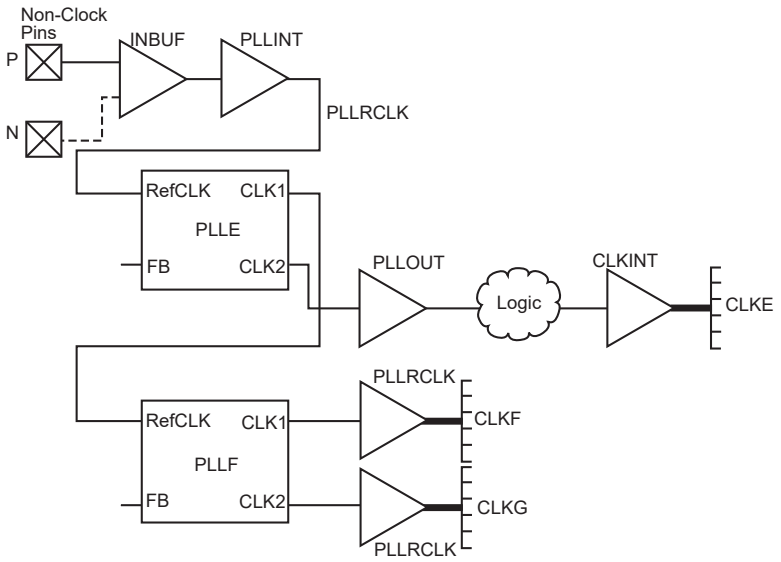


2.8.5.3 Implementation Example

The following figure shows a complex clock distribution example. The reference clock (RefCLK) of PLLE is being sourced from non-clock signal pins (INBUF to PLLINT). The CLK1 output of PLLE is being fed to the RefCLK input of PLLF. The CLK2 output of PLLE is driving logic (via PLLOUT). In turn, this logic is driving the global resource CLKE. PLLF is driving both CLKF and CLKG global resources.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-48. Complex Clock Distribution Example



2.9 Axcelerator Clock Management System

Each member of the Axcelerator family[6] contains eight Phase-Locked Loop (PLL) blocks, which perform the following functions:

- Programmable Delay (32 steps of 250 ps)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range: 14 to 200 MHz
- Output Frequency Range: 20 MHz to 1 GHz
- Output Duty Cycle Range: 45% to 55%
- Maximum Long-Term Jitter: 1% or 100ps (whichever is greater)
- Maximum Short-Term Jitter: 50ps + 1% of Output Frequency
- Maximum Acquisition Time (lock): 20µs

2.9.1 Physical Implementation

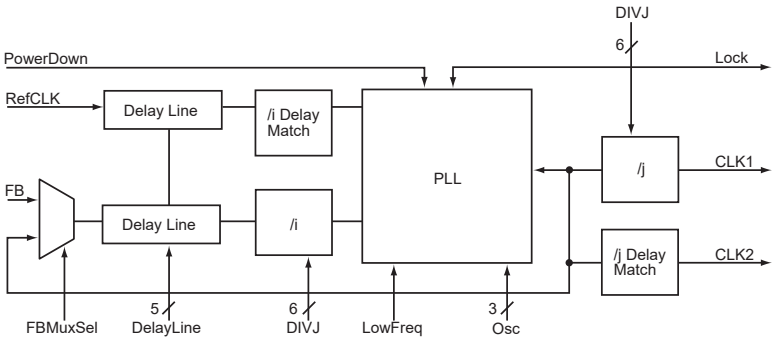
The eight PLL blocks are arranged in two groups of four. One group is located in the center of the northern edge of the chip, while the second group is centered on the southern edge. The northern group is associated with the four HCLK networks (for example, PLLA can drive HCLKA), while the southern group is associated with the four CLK networks (for example, PLLE can drive CLKE).

Each PLL cell is connected to two I/O pads and a PLL Cluster that interfaces with the FPGA core. The following figure illustrates a PLL block. The VCCPLL pin should be connected to a 1.5V power supply through a 250Ω resistor. Furthermore, 0.1 µF and 10 µF decoupling capacitors should be connected across the VCCPLL and VCOMPPLL pins.

[6] AX2000-CQ256 does not support operation of the Phase-Locked Loops. This is in order to support full pin compatibility with RTAX2000S/SL-CQ256.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-49. PLL Block Diagram



The VCOMPPLL pin should never be grounded (see Figure 2-2).

The I/O pads associated with the PLL can also be configured for regular I/O functions, except when it is used as a clock buffer. The I/O pads can be configured in all the modes available to the regular I/O pads in the same I/O bank. In particular, the [H]CLKxP pad can be configured as a differential pair, single-ended, or voltage-referenced standard. The [H]CLKxN pad can only be used as a differential pair with [H]CLKxP.

The block marked "/i Delay Match" is a fixed delay equal to that of the i divider. The "/j Delay Match" block has the same function as its j divider counterpart.

2.9.2 Functional Description

Figure 2-49 illustrates a block diagram of the PLL. The PLL contains two dividers, i and j, that allow frequency scaling of the clock signal:

- The i divider in the feedback path allows multiplication of the input clock by integer factors ranging from 1 to 64, and the resultant frequency is available at the output of the PLL block.
- The j divider divides the PLL output by integer factors ranging from 1 to 64, and the divided clock is available at CLK1.
- The two dividers together can implement any combination of multiplication and division up to a maximum frequency of 1 GHz on CLK1. Both the CLK1 and CLK2 outputs have a fixed 50/50 duty cycle.
- The output frequencies of the two clocks are given by the following formulas (fREF is the reference clock frequency):
  fCLK1 = fREF × (DividerI) / (DividerJ)

  fCLK2 = fREF × (DividerI)
- CLK2 provides the PLL output directly—without division

The input and output frequency ranges are selected by LowFreq and Osc(2:0), respectively. These functions and their possible values are detailed in the following table.

The delay lines shown in Figure 2-49 are programmable. The feedback clock path can be delayed (using the five DelayLine bits) relative to the reference clock (or vice versa) by up to 3.75 ns in increments of 250 ps. The following table describes the usage of these bits. The delay increments are independent of frequency, so this results in phase changes that vary with frequency. The delay value is highly dependent on VCC and the speed grade.

The following figure is a logical diagram of the various control signals to the PLL and shows how the PLL interfaces with the global and routing networks of the FPGA. Note that not all signals are user-accessible. These non-user-accessible signals are used by the place-and-route tool to control the configuration of the PLL. The user gains access to these control signals either based upon the connections built in the user's design or through the special macros (see Table 2-88) inserted into the design. For example, connecting the macro PLLOUT to CLK2 will control the OUTSEL signal.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-50. PLL Logical Interface

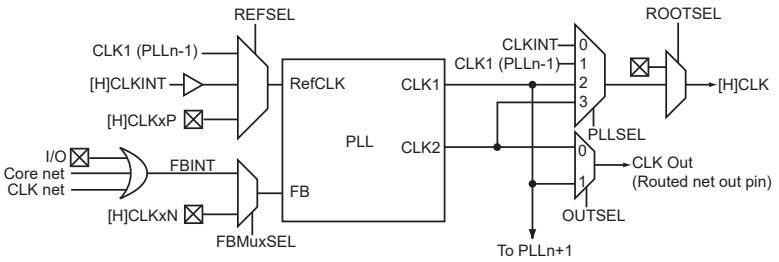


Table 2-84. PLL Interface Signals

Signal Name	Type	User Accessible	Allowable Values	Function
RefCLK	Input	Yes	—	Reference Clock for the PLL
FB	Input	Yes	—	Feedback port for the PLL
PowerDown	Input	Yes	—	PLL power down control
			0	PLL powered down
			1	PLL active
DIVI[5:0]	Input	Yes	1 to 64, in unsigned binary notation offset by -1	Sets value for feedback divider (multiplier)
DIVJ[5:0]	Input	Yes		Sets value for CLK1 divider
LowFreq	Input	Yes	—	Input frequency range selector
			0	50–200 MHz
			1	14–50 MHz
Osc[2:0]	Input	Yes	—	Output frequency range selector
			XX0	400–1000 MHZ
			001	200–400 MHZ
			011	100–200 MHZ
			101	50–100 MHZ
			111	20–50 MHZ
DelayLine[4:0]	Input	Yes	–15 to +15 (increments), in signed-and-magnitude binary representation	Clock Delay (positive/negative) in increments of 250 ps, with maximum value of ± 3.75 ns
FBMuxSel	Input	No	—	Selects the source for the feedback input
REFSEL	Input	No	—	Selects the source for the reference clock
OUTSEL	Input	No	—	Selects the source for the routed net output
PLLSEL	Input	No	—	ROOTSEL and PLLSEL are used to select the source of the global clock network
ROOTSEL	Input	No	—	—
Lock	Output	Yes	—	High value indicates PLL has locked
CLK1	Output	Yes	—	PLL clock output
CLK2	Output	Yes	—	PLL clock output

Note: If the input RefClk is taken outside its operating range, the outputs Lock and CLK1 and CLK2 are indeterminate.

2.9.3 PLL Configurations

The following configurations apply to the different PLL inputs and outputs.

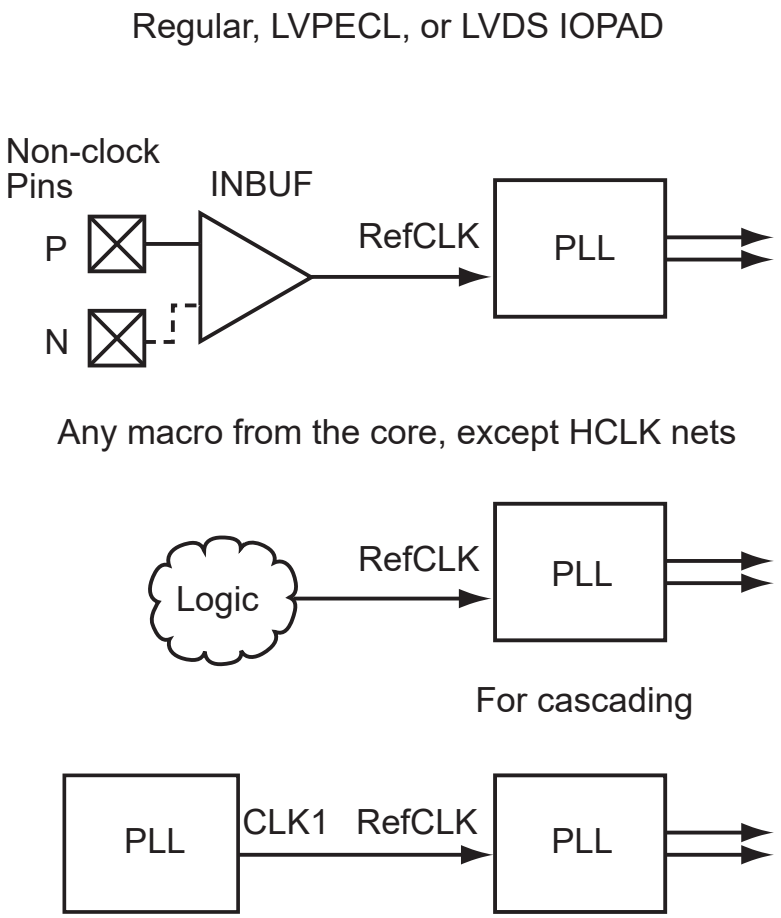
© 2024 Microchip Technology Inc. and its subsidiaries

2.9.3.1 Reference Clock

The RefCLK can be driven by the following:

- Global routed clocks (CLKE/F/G/H) or user-created clock network
- CLK1 output of an adjacent PLL
- [H]CLKxP (single-ended or voltage-referenced)
- [H]CLKxP/[H]CLKxN pair (differential modes like LVPECL or LVDS)

Figure 2-51. Reference Clock Connections



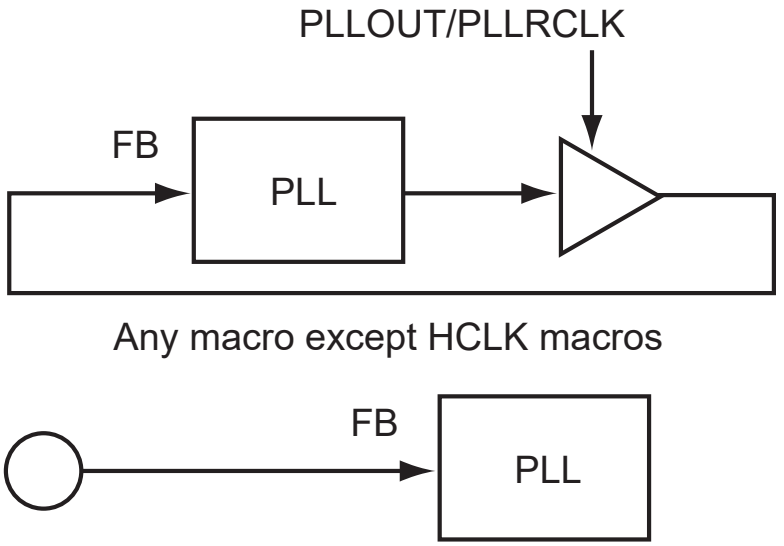
2.9.3.2 Feedback Clock

The feedback clock can be driven by the following:

- Global routed clocks (CLKE/F/G/H) or user-created clock network
- External [H]CLKxP/N I/O pad(s) from the adjacent PLL cell
- An internal signal from the PLL block

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-52. Feedback Clock Connections



2.9.3.3 CLK1 and CLK2

Both PLL outputs, CLK1 and CLK2, can be used to drive a global resource, an adjacent PLL RefCLK input, or a net in the FPGA core. Not all drive combinations are possible (see the following table).

Table 2-85. PLL General Connections Rules

CLK1	CLK2
HCLK	HCLK
CLK	CLK
HCLK	Routed net output
Routed net output	HCLK
HCLK	NONE
NONE	HCLK
CLK	NONE
NONE	CLK

Note: The PLL outputs remain Low when REFCLK is constant (either Low or High).

2.9.3.4 Restrictions on CLK1 and CLK2

- When both are driving global resources, they must be driving the same type of global resource (that is, either HCLK or CLK)
- Only one can drive a routed net at any given time

The following tables specify all the possible CLK1 and CLK2 connections for the north and south PLLs. HCLK1 and HCLK2 are used to denote the different HCLK networks when two are being driven at the same time by a single PLL (the HCLK1 is the primary clock resource associated with the PLL, and HCLK2 is the clock resource associated with the adjacent PLL). Likewise, CLK1 and CLK2 are used to denote the different CLK networks when two are being driven at the same time by a single PLL (see Figure 2-49).

Table 2-86. North PLL Connections

CLK1	CLK2
HCLK1	Routed net
HCLK1	Unused
HCLK2	HCLK1

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CLK1	CLK2
HCLK2	Routed net
HCLK2	Both HCLK1 and routed net
HCLK2	Unused
Unused	HCLK1
Unused	Routed net
Unused	Both HCLK1 and routed net
Unused	Unused
Routed net	HCLK1
Routed net	Unused
Both HCLK1 and HCLK2	Routed net
Both HCLK1 and HCLK2	Unused
Both HCLK1 and routed net	Unusable
Both HCLK2 and routed net	HCLK1
Both HCLK2 and routed net	Unused
HCLK1, HCLK2, and routed net	Unusable

Note: Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (for example, CLK1 driving HCLK1, and HCLK2 is not supported).

Table 2-87. South PLL Connections

CLK1	CLK2
CLK1	Routed net
CLK1	Unused
CLK2	CLK1
CLK2	Routed net
CLK2	Both CLK1 and routed net
CLK2	Unused
Unused	CLK1
Unused	Routed net
Unused	Both CLK1 and routed net
Unused	Unused
Routed net	CLK1
Routed net	Unused
Both CLK1 and CLK2	Routed net
Both CLK1 and CLK2	Unused
Both CLK1 and routed net	Unusable
Both CLK2 and routed net	CLK1
Both CLK2 and routed net	Unused
CLK1, CLK2, and routed net	Unusable

Note: Designer software currently does not support all of these connections. Only exclusive connections where one output connects to a single net are supported at this time (for example, CLK1 driving both CLK1 and CLK2 is not supported).

© 2024 Microchip Technology Inc. and its subsidiaries

2.9.4 Special PLL Macros

The following tables show the macros used to connect the RefCLK input and CLK1 and CLK2 outputs using the different routing resources.

Table 2-88. PLL Special Macros

Macro Name	Usage
PLLINT	Connects RefCLK to a regular routed net or a pad.
PLLRCLK	Connects CLK1 or CLK2 to the CLK network.
PLLHCLK	Connects CLK1 or CLK2 to the HCLK network.
PLLOUT	Connects CLK1 or CLK2 to a regular routed net.

Table 2-89. Electrical Specifications

Parameter	Value	Notes
Frequency Ranges		
Reference frequency (min.)	14 MHz	Lowest input frequency
Reference frequency (max.)	200 MHz	Highest input frequency
OSC frequency (min.)	20 MHz	Lowest output frequency
OSC frequency (max.)	1 GHz	Highest output frequency
Jitter		
Long-term jitter (max.)	1%	Percentage of period, low reference clock frequencies
Long-term jitter (max.)	100ps	High reference clock frequencies
Short-term jitter (max.)	50ps+1%	Percentage of output frequency
Acquisition Time (lock) from Cold Start		
Acquisition time (max.)[1]	400 cycles	Period of low reference clock frequencies
Acquisition time (max.)[1]	1.5 µs	High reference clock frequencies
Power Consumption		
Analog supply current (low freq.)	200 µA	Current at minimum oscillator frequency
Analog supply current (high freq.)	200 µA	Frequency-dependent current
Digital Supply Current (low freq.)	0.5 µA/MHz	Current at maximum oscillator frequency, unloaded
Digital supply current (high freq.)	1 µA/MHz	Frequency-dependent current
Duty Cycle		
Minimum output duty cycle	45%	—
Maximum output duty cycle	55%	—

Note:

1. The lock bit remains Low until RefCLK reaches the minimum input frequency.

2.9.5 User Flow

There are two methods of including a PLL in a design:

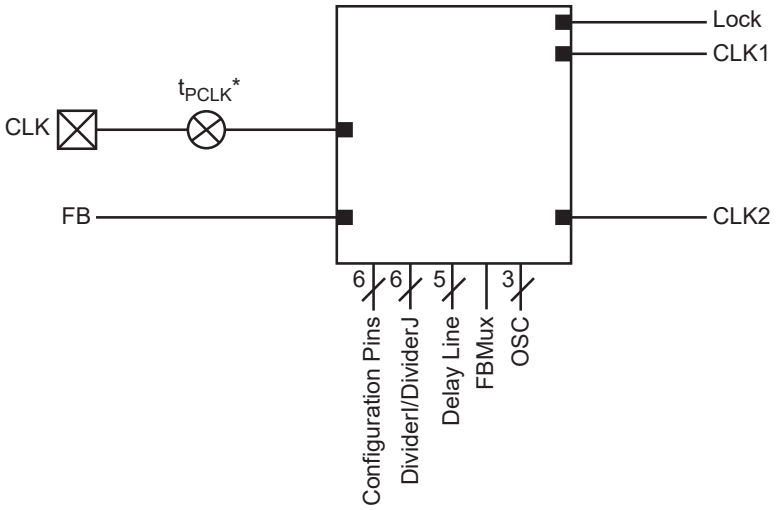
- The recommended method of using a PLL is to create custom PLL blocks using Microchip's macro generator, SmartGen, that can be instantiated in a design.
- The alternative method is to instantiate one of the generic library primitives (PLL or PLLFB) into either a schematic or HDL netlist, using inverters for polarity control and tying all unused address and data bits to ground.

2.9.5.1 Timing Model

The following figure shows the timing model of PLL.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-53. PLL Model

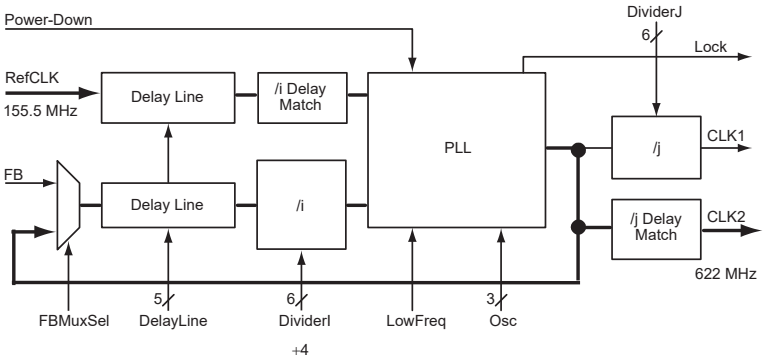


2.9.6 Sample Implementations

2.9.6.1 Frequency Synthesis

The following figure illustrates an example where the PLL is used to multiply a 155.5 MHz external clock up to 622 MHz. Note that the same PLL schematic could use an external 350 MHz clock, which is divided down to 155 MHz by the FPGA internal logic.

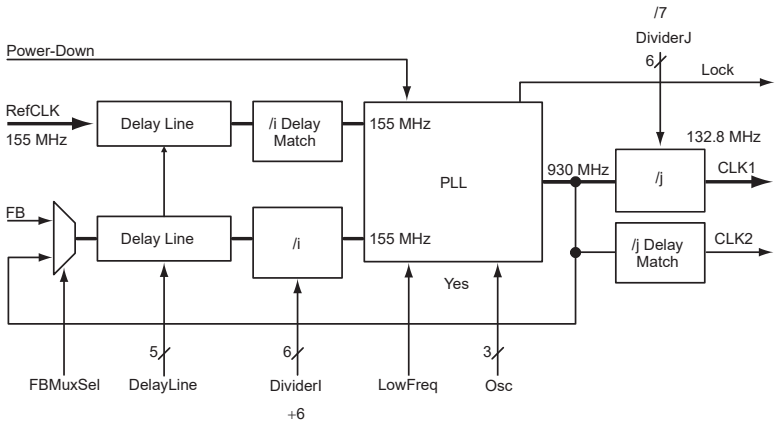
Figure 2-54. Using the PLL 155.5 MHz In and 622 MHz Out



The following figure illustrates the PLL using both dividers to synthesize a 133 MHz output clock from a 155 MHz input reference clock. The input frequency of 155 MHz is multiplied by 6 and divided by 7, giving a CLK1 output frequency of 132.86 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL.

© 2024 Microchip Technology Inc. and its subsidiaries

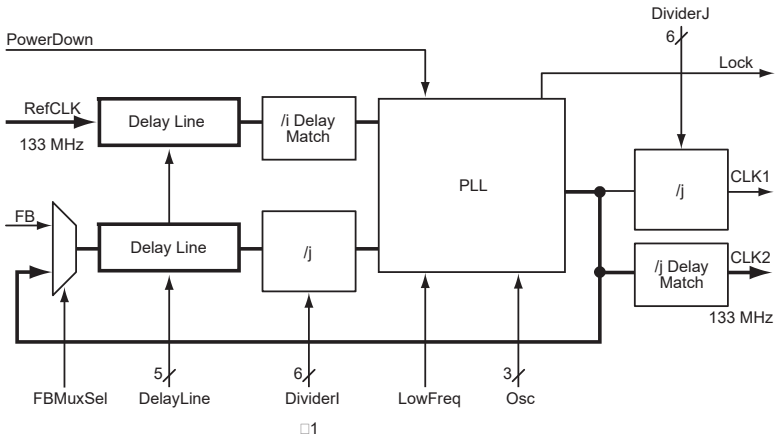
Figure 2-55. Using the PLL 155 MHz In and 133 MHz Out



2.9.6.2 Adjustable Clock Delay

The following figure illustrates using the PLL to delay the reference clock by employing one of the adjustable delay lines. In this case, the output clock is delayed relative to the reference clock. Delaying the reference clock relative to the output clock is accomplished by using the delay line in the feedback path.

Figure 2-56. Using the PLL Delaying the Reference Clock

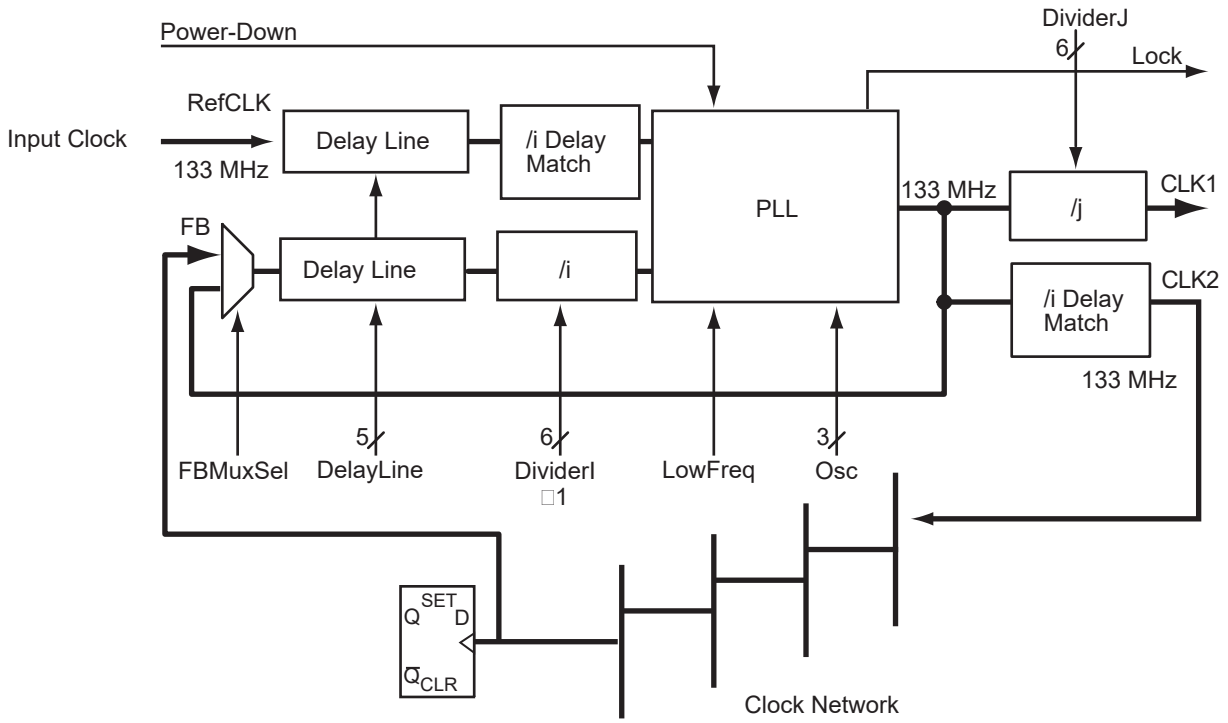


2.9.7 Clock Skew Minimization

The following figure indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the input clock. The input clock is fed to the reference clock input of the PLL. The output clock (CLK2) feeds a routed clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. For more information, see the Axcelerator Family PLL and Clock Management application note.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-57. Using the PLL for Clock Deskewing



2.10 Embedded Memory

The AX architecture provides extensive, high-speed memory resources to the user. Each 4,608 bit block of RAM contains its own embedded FIFO controller, allowing the user to configure each block as either RAM or FIFO.

To meet the needs of high performance designs, the memory blocks operate in synchronous mode for both read and write operations. However, the read and write clocks are completely independent, and each may operate up to and above 500 MHz.

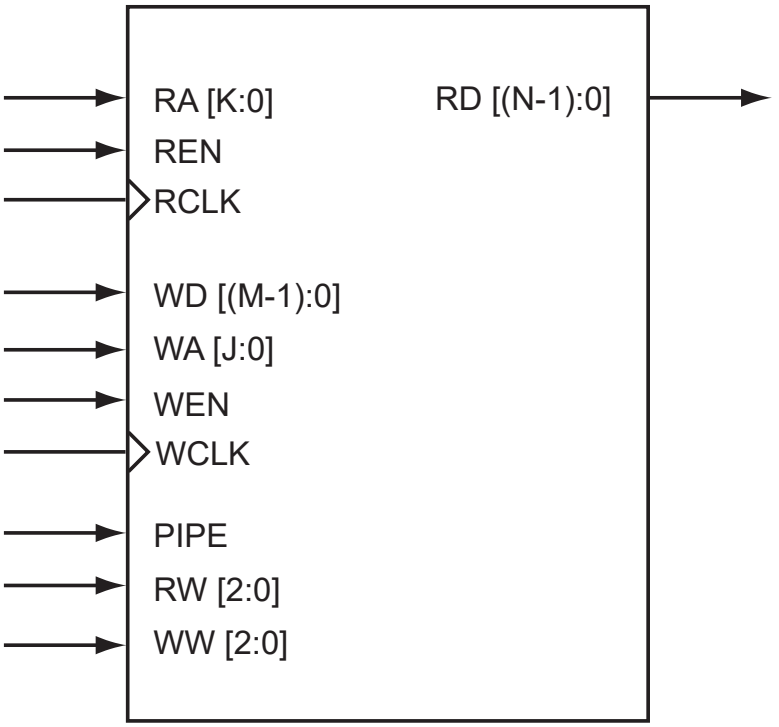
No additional core logic resources are required to cascade the address and data buses when cascading different RAM blocks. Dedicated routing runs along each column of RAM to facilitate cascading.

The AX memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, and AEMPTY). Since read and write operations can occur asynchronously to one another, special control circuitry is included to prevent metastability, overflow, and underflow. A block diagram of the memory module is illustrated in the following figure.

During RAM operation, read (RA) and write (WA) addresses are sourced by user logic and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Enables with programmable polarity are provided to create upper address bits for cascading up to 16 memory blocks. When cascading memory blocks, the bussed signals WA, WD, WEN, RA, RD, and REN are internally linked to eliminate external routing congestion.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-58. Axcelerator Memory Module



2.10.1 RAM

Each memory block consists of 4,608 bits that can be organized as 128x36, 256x18, 512x9, 1kx4, 2kx2, or 4kx1 and are cascadable to create larger memory sizes. This allows built-in bus width conversion (see the following table). Each block has independent read and write ports which enable simultaneous read and write operations.

Table 2-90. Memory Block WxD Options

Data-word (in bits)	Depth	Address Bus	Data Bus
1	4,096	RA/WA[11:0]	RD/WD[0]
2	2,048	RA/WA[10:0]	RD/WD[1:0]
4	1,024	RA/WA[9:0]	RD/WD[3:0]
9	512	RA/WA[8:0]	RD/WD[8:0]
18	256	RA/WA[7:0]	RD/WD[17:0]
36	128	RA/WA[6:0]	RD/WD[35:0]

2.10.2 Clocks

The RCLK and the WCLK have independent source polarity selection and can be sourced by any global or local signal.

2.10.3 RAM Configurations

The AX architecture allows the read side and write side of RAMs to be organized independently, allowing for bus conversion. For example, the write side can be set to 256x18 and the read side to 512x9.

Both the write width and read width for the RAM blocks can be specified independently and changed dynamically with the WW (write width) and RW (read width) pins. The D x W different configurations are: 128 x 36, 256 x 18, 512 x 9, 1k x 4, 2k x 2, and 4k x 1. The allowable RW and WW values are shown in the following table.

© 2024 Microchip Technology Inc. and its subsidiaries

Table 2-91. Allowable RW and WW Values

RW(2:0)	WW(2:0)	D x W
000	000	4k x 1
001	001	2k x 2
010	010	1k x 4
011	011	512 x 9
100	100	256 x 18
101	101	128 x 36
11x	11x	reserved

When widths of one, two, and four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible. Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined.

Note that the RAM blocks employ little-endian byte order for read and write operations.

The following table lists the RAM signals and their descriptions.

Table 2-92. RAM Signal Description

Signal	Direction	Description
WCLK	Input	Write clock (can be active on either edge)
WA[J:0]	Input	Write address bus.The value J is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for J is from 6 to15.
WD[M-1:0]	Input	Write data bus. The value M is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
RCLK	Input	Read clock (can be active on either edge)
RA[K:0]	Input	Read address bus. The value K is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for K is from 6 to 15.
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
REN	Input	Read enable. When this signal is valid on the active edge of the clock, data at location RA will be driven onto RD.
WEN	Input	Write enable. When this signal is valid on the active edge of the clock, WD data will be written at location WA.
RW[2:0]	Input	Width of the read operation dataword
WW[2:0]	Input	Width of the write operation dataword
Pipe	Input	Sets the pipe option to be on or off

2.10.4 Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous—one clock edge)
- Read Pipelined (synchronous—two clock edges)
- Write (synchronous—one clock edge)

In the standard read mode, new data is driven onto the RD bus in the clock cycle immediately following RA and REN valid. The read address is registered on the read-port active-clock edge and data appears at read-data after the RAM access time. Setting the PIPE to OFF enables this mode.

The pipelined mode incurs an additional clock delay from address to data, but enables operation at a much higher frequency. The read-address is registered on the read-port active-clock edge, and the

© 2024 Microchip Technology Inc. and its subsidiaries

read data is registered and appears at RD after the second read clock edge. Setting the PIPE to On enables this mode.

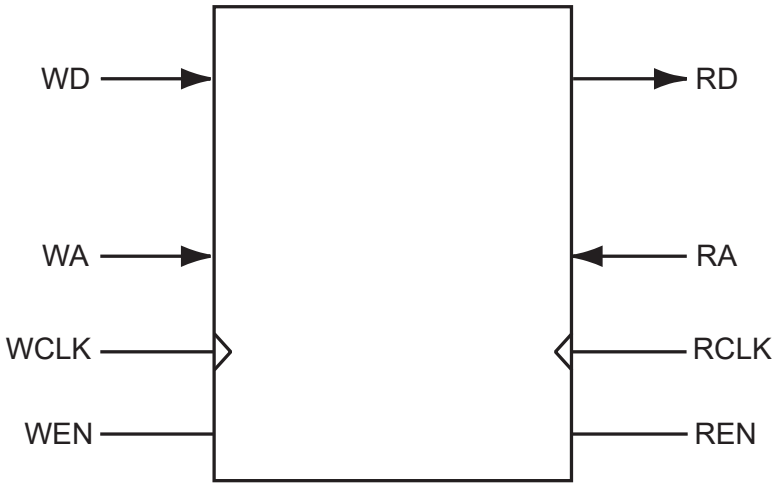
On the write active-clock edge, the write data are written into the SRAM at the write address when Wen is high. The setup time of the write address, write enables, and write data are minimal with respect to the write clock.

Write and read transfers are described with timing requirements beginning in the Timing Characteristics.

2.10.4.1 Timing Characteristics

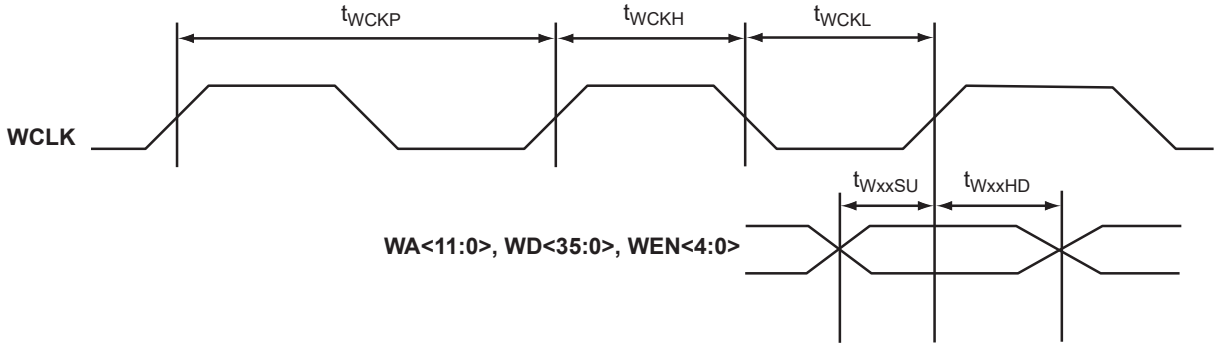
The following figure shows the timing model of SRAM.

Figure 2-59. SRAM Model



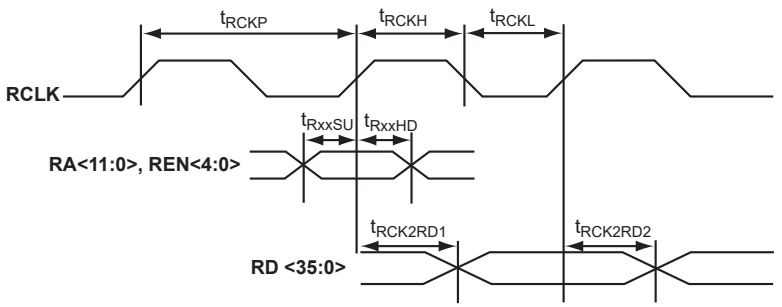
The following figures shows the timing waveforms of RAM write and RAM read.

Figure 2-60. RAM Write Timing Waveforms



© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-61. RAM Read Timing Waveforms



The following tables list the timing characteristics of different RAM blocks.

Table 2-93. One RAM Block Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Mode								
t_{WDASU}	Write data setup vs. WCLK	—	1.08	—	1.23	—	1.45	ns
t_{WDAHD}	Write data hold vs. WCLK	—	0.22	—	0.25	—	0.30	ns
t_{WADSU}	Write address setup vs. WCLK	—	1.08	—	1.23	—	1.45	ns
t_{WADHD}	Write address hold vs. WCLK	—	0.00	—	0.00	—	0.00	ns
t_{WENSU}	Write enable setup vs. WCLK	—	1.08	—	1.23	—	1.45	ns
t_{WENHD}	Write enable hold vs. WCLK	—	0.22	—	0.25	—	0.30	ns
t_{WCKH}	WCLK minimum high pulse width	0.75	—	0.75	—	0.75	—	ns
t_{WCLK}	WCLK minimum low pulse width	0.88	—	0.88	—	0.88	—	ns
t_{WCKP}	WCLK minimum period	1.63	—	1.63	—	1.63	—	ns
Read Mode								
t_{RADSU}	Read address setup vs. RCLK	—	0.81	—	0.92	—	1.08	ns
t_{RADHD}	Read address hold vs. RCLK	—	0.00	—	0.00	—	0.00	ns
t_{RENSU}	Read enable setup vs. RCLK	—	0.81	—	0.92	—	1.08	ns
t_{RENHD}	Read enable hold vs. RCLK	—	0.00	—	0.00	—	0.00	ns
$t_{RCK2RD1}$	RCLK-to-OUT (Pipelined)	—	1.32	—	1.51	—	1.77	ns
$t_{RCK2RD2}$	RCLK-to-OUT (Non-Pipelined)	—	2.16	—	2.46	—	2.90	ns
t_{RCLKH}	RCLK minimum high pulse width	0.77	—	0.77	—	0.77	—	ns
t_{RCLKL}	RCLK minimum low pulse width	0.93	—	0.93	—	0.93	—	ns
t_{RCKP}	RCLK minimum period	1.70	—	1.70	—	1.70	—	ns

Note: Timing data for this single block RAM has a depth of 4,096. For all other combinations, use Microchip's timing software.

Table 2-94. Two RAM Blocks Cascaded Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Units
Write Mode								
t_{WDASU}	Write data setup vs. WCLK	—	1.39	—	1.59	—	1.87	ns
t_{WDAHD}	Write data hold vs. WCLK	—	0.00	—	0.00	—	0.00	ns
t_{WADSU}	Write address setup vs. WCLK	—	1.39	—	1.59	—	1.87	ns
t_{WADHD}	Write address hold vs. WCLK	—	0.00	—	0.00	—	0.00	ns
t_{WENSU}	Write enable setup vs. WCLK	—	1.39	—	1.59	—	1.87	ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2 Speed		–1 Speed		Std Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{WENHD}	Write enable hold vs. WCLK	—	0.00	—	0.00	—	0.00	ns
t_{WCKH}	WCLK minimum high pulse width	0.75	—	0.75	—	0.75	—	ns
t_{WCLK}	WCLK minimum low pulse width	1.76	—	1.76	—	1.76	—	ns
t_{WCKP}	WCLK minimum period	2.51	—	2.51	—	2.51	—	ns
Read Mode								
t_{RADSU}	Read address setup vs. RCLK	—	1.71	—	1.94	—	2.28	ns
t_{RADHD}	Read address hold vs. RCLK	—	0.00	—	0.00	—	0.00	ns
t_{RENSU}	Read enable setup vs. RCLK	—	1.71	—	1.94	—	2.28	ns
t_{RENHD}	Read enable hold vs. RCLK	—	0.00	—	0.00	—	0.00	ns
$t_{RCK2RD1}$	RCLK-to-OUT (Pipelined)	—	1.43	—	1.63	—	1.92	ns
$t_{RCK2RD2}$	RCLK-to-OUT (Non-Pipelined)	—	2.26	—	2.58	—	3.03	ns
t_{RCLKH}	RCLK minimum high pulse width	0.73	—	0.73	—	0.73	—	ns
t_{RCLKL}	RCLK minimum low pulse width	1.89	—	1.89	—	1.89	—	ns
t_{RCKP}	RCLK minimum period	2.62	—	2.62	—	2.62	—	ns

Note: Timing data for these two cascaded RAM blocks uses a depth of 8,192. For all other combinations, use Microchip's timing software.

Table 2-95. Four RAM Blocks Cascaded Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Units
Write Mode								
t_{WDASU}	Write data setup vs. WCLK	—	2.37	—	2.70	—	3.17	ns
t_{WDAHD}	Write data hold vs. WCLK	—	0.00	—	0.00	—	0.00	ns
t_{WADSU}	Write address setup vs. WCLK	—	2.37	—	2.70	—	3.17	ns
t_{WADHD}	Write address hold vs. WCLK	—	0.00	—	0.00	—	0.00	ns
t_{WENSU}	Write enable setup vs. WCLK	—	2.37	—	2.70	—	3.17	ns
t_{WENHD}	Write enable hold vs. WCLK	—	0.00	—	0.00	—	0.00	ns
t_{WCKH}	WCLK minimum high pulse width	0.75	—	0.75	—	0.75	—	ns
t_{WCLK}	WCLK minimum low pulse width	2.51	—	2.51	—	2.51	—	ns
t_{WCKP}	WCLK minimum period	3.26	—	3.26	—	3.26	—	ns
Read Mode								
t_{RADSU}	Read address setup vs. RCLK	—	3.08	—	3.51	—	4.13	ns
t_{RADHD}	Read address hold vs. RCLK	—	0.00	—	0.00	—	0.00	ns
t_{RENSU}	Read enable setup vs. RCLK	—	3.08	—	3.51	—	4.13	ns
t_{RENHD}	Read enable hold vs. RCLK	—	0.00	—	0.00	—	0.00	ns
$t_{RCK2RD1}$	RCLK-to-OUT (Pipelined)	—	2.36	—	2.69	—	3.16	ns
$t_{RCK2RD2}$	RCLK-to-OUT (Non-Pipelined)	—	2.83	—	3.23	—	3.79	ns
t_{RCLKH}	RCLK minimum high pulse width	0.73	—	0.73	—	0.73	—	ns
t_{RCLKL}	RCLK minimum low pulse width	2.96	—	2.96	—	2.96	—	ns
t_{RCKP}	RCLK minimum period	3.69	—	3.69	—	3.69	—	ns

Note: Timing data for these four cascaded RAM blocks uses a depth of 16,384. For all other combinations, use Microchip's timing software.

© 2024 Microchip Technology Inc. and its subsidiaries

Table 2-96. Eight RAM Blocks Cascaded Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Units
Write Mode								
t_{WDASU}	Write data setup vs. WCLK	—	5.78	—	6.58	—	7.74	ns
t_{WDAHD}	Write data hold vs. WCLK	—	0.00	—	0.00	—	0.00	ns
t_{WADSU}	Write address setup vs. WCLK	—	5.78	—	6.58	—	7.74	ns
t_{WADHD}	Write address hold vs. WCLK	—	0.00	—	0.00	—	0.00	ns
t_{WENSU}	Write enable setup vs. WCLK	—	5.78	—	6.58	—	7.74	ns
t_{WENHD}	Write enable hold vs. WCLK	—	0.00	—	0.00	—	0.00	ns
t_{WCKH}	WCLK minimum high pulse width	0.75	—	0.75	—	0.75	—	ns
t_{WCLK}	WCLK minimum low pulse width	5.13	—	5.13	—	5.13	—	ns
t_{WCKP}	WCLK minimum period	5.88	—	5.88	—	5.88	—	ns
Read Mode								
t_{RADSU}	Read address setup vs. RCLK	—	6.75	—	7.69	—	9.04	ns
t_{RADHD}	Read address hold vs. RCLK	—	0.00	—	0.00	—	0.00	ns
t_{RENSU}	Read enable setup vs. RCLK	—	6.75	—	7.69	—	9.04	ns
t_{RENHD}	Read enable hold vs. RCLK	—	0.00	—	0.00	—	0.00	ns
$t_{RCK2RD1}$	RCLK-to-OUT (Pipelined)	—	3.39	—	3.86	—	4.54	ns
$t_{RCK2RD2}$	RCLK-to-OUT (Non-Pipelined)	—	4.93	—	5.62	—	6.61	ns
t_{RCLKH}	RCLK minimum high pulse width	0.73	—	0.73	—	0.73	—	ns
t_{RCLKL}	RCLK minimum low pulse width	5.77	—	5.77	—	5.77	—	ns
t_{RCKP}	RCLK minimum period	6.50	—	6.50	—	6.50	—	ns

Note: Timing data for these eight cascaded RAM blocks uses a depth of 32,768. For all other combinations, use Microchip's timing software.

Table 2-97. Sixteen RAM Blocks Cascaded Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2 Speed		–1 Speed		Std Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Units
Write Mode								
t_{WDASU}	Write data setup vs. WCLK	—	16.54	—	18.84	—	22.15	ns
t_{WDAHD}	Write data hold vs. WCLK	—	0.00	—	0.00	—	0.00	ns
t_{WADSU}	Write address setup vs. WCLK	—	16.54	—	18.84	—	22.15	ns
t_{WADHD}	Write address hold vs. WCLK	—	0.00	—	0.00	—	0.00	ns
t_{WENSU}	Write enable setup vs. WCLK	—	16.54	—	18.84	—	22.15	ns
t_{WENHD}	Write enable hold vs. WCLK	—	0.00	—	0.00	—	0.00	ns
t_{WCKH}	WCLK minimum high pulse width	0.75	—	0.75	—	0.75	—	ns
t_{WCLK}	WCLK minimum low pulse width	13.40	—	13.40	—	13.40	—	ns
t_{WCKP}	WCLK minimum period	14.15	—	14.15	—	14.15	—	ns
Read Mode								
t_{RADSU}	Read address setup vs. RCLK	—	18.13	—	20.65	—	24.27	ns
t_{RADHD}	Read address hold vs. RCLK	—	0.00	—	0.00	—	0.00	ns
t_{RENSU}	Read enable setup vs. RCLK	—	18.13	—	20.65	—	24.27	ns
t_{RENHD}	Read enable hold vs. RCLK	—	0.00	—	0.00	—	0.00	ns
$t_{RCK2RD1}$	RCLK-to-OUT (Pipelined)	—	12.08	—	13.76	—	16.17	ns
$t_{RCK2RD2}$	RCLK-to-OUT (Non-Pipelined)	—	12.83	—	14.62	—	17.18	ns
t_{RCLKH}	RCLK minimum high pulse width	0.73	—	0.73	—	0.73	—	ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2 Speed		–1 Speed		Std Speed		
		Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{RCLKL}	RCLK minimum low pulse width	14.41	—	14.41	—	14.41	—	ns
t_{RCKP}	RCLK minimum period	15.14	—	15.14	—	15.14	—	ns

Note: Timing data for these sixteen cascaded RAM blocks uses a depth of 65,536. For all other combinations, use Microchip's timing software.

2.10.5 FIFO

Every memory block has its own embedded FIFO controller. Each FIFO block has one read port and one write port. This embedded FIFO controller uses no internal FPGA logic and features.

- Glitch-free FIFO Flags
- Gray-code address counters/pointers to prevent metastability problems
- Overflow and underflow control

Both ports are configurable in various sizes from 4k x 1 to 128 x 36, similar to the RAM block size. Each port is fully synchronous.

Read and write operations can be completely independent. Data on the appropriate WD pins are written to the FIFO on every active WCLK edge as long as WEN is high. Data is read from the FIFO and output on the appropriate RD pins on every active RCLK edge as long as REN is asserted.

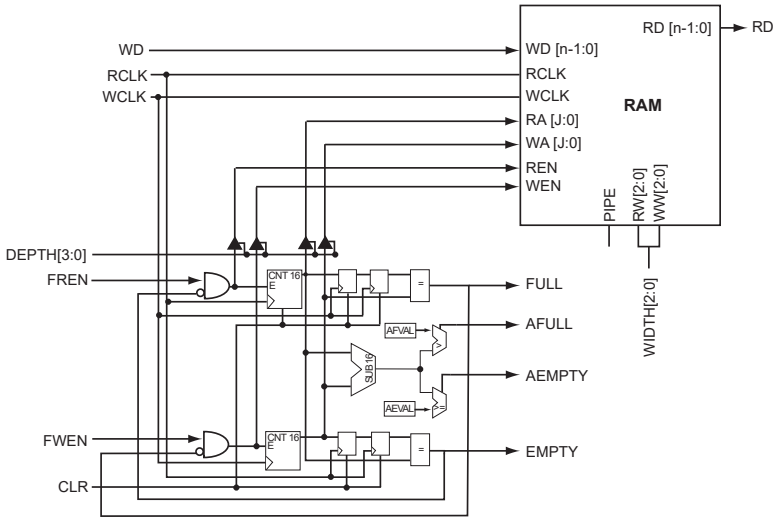
The FIFO block offers programmable almost-empty (AEMPTY) and almost-full (AFULL) flags as well as EMPTY and FULL flags (see the following figure):

- The FULL flag is synchronous to WCLK. It allows the FIFO to inhibit writing when full.
- The EMPTY flag is synchronous to RCLK. It allows the FIFO to inhibit reading at the empty condition.

Gray code counters are used to prevent metastability problems associated with flag logic. The depth of the FIFO is dependent on the data width and the number of memory blocks used to create the FIFO. The write operations to the FIFO are synchronous with respect to the WCLK, and the read operations are synchronous with respect to the RCLK.

The FIFO block may be reset to the empty state.

Figure 2-62. Axcelerator RAM with Embedded FIFO Controller



© 2024 Microchip Technology Inc. and its subsidiaries

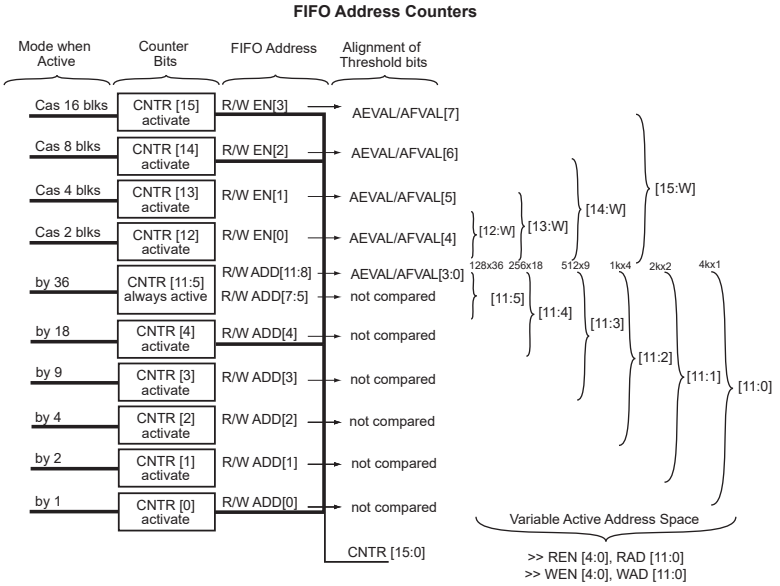
2.10.6 FIFO Flag Logic

The FIFO is user configurable into various DEPTHs and WIDTHs. The following figure shows the FIFO address counter details.

- Bits 11 to 5 are active for all modes
- As the data word size is reduced, more least-significant bits are added to the address
- As the number of cascaded blocks increases, the number of significant bits in the address increases

For example, if four blocks are cascaded as a 1kx16 FIFO with each block having a 1kx4 aspect ratio, bits 11 to 2 of the address will be used to specify locations within each RAM block, whereas bits 13 and 12 will be used to specify the RAM block.

Figure 2-63. FIFO Address Counters



The AFULL and AEMPTY flag threshold values are programmable. The threshold values are AFVAL and AEVAL, respectively. Although the trigger threshold for each flag is defined with eight bits, the effective number of threshold bits in the comparison depends on the configuration. The effective number of threshold bits corresponds to the range of active bits in the FIFO address space (see the following table).

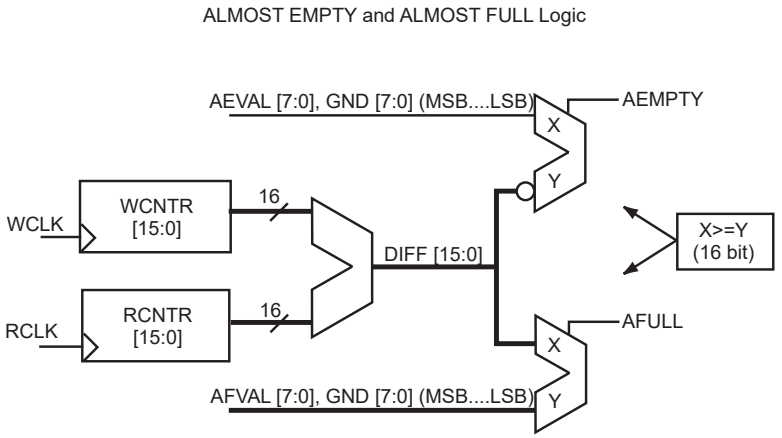
Table 2-98. FIFO Flag Logic

Mode	Inactive AEVAL/AFVAL Bits	Inactive DIFF Bits (set to 0)	DIFF Comparison to AFVAL/AEVAL
Non-cascade	[7:4]	[15:12]	DIFF[11:8] withAE/FVAL[3:0]
Cascade 2 blocks	[7:5]	[15:13]	DIFF[12:8] withAE/FVAL[4:0]
Cascade 4 blocks	[7:6]	[15:14]	DIFF[13:8] withAE/FVAL[5:0]
Cascade 8 blocks	[7]	[15]	DIFF[14:8] withAE/FVAL[6:0]
Cascade 16 blocks	None	None	DIFF[15:8] withAE/FVAL[7:0]

The following figure illustrates flag generation.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-64. ALMOST-EMPTY and ALMOST-FULL Logic



The Verilog codes for the flags are:

```
assign AF = (DIFF[15:0] >={AFVAL[7:0],8'b00000000})?1:0;
assign AE = ({AEVAL[7:0],8'b00000000}>=DIFF[15:0])?1:0;
```

The number of DIFF-bits active depends on the configuration depth and width (see the following table).

Table 2-99. Number of Available Configuration Bits

Number of Blocks	Block DxW	Number of AEVAL/AFVAL Bits
1	1x1	4
2	1x2	4
2	2x1	5
4	1x4	4
4	2x2	5
4	4x1	6
8	1x8	4
8	2x4	5
8	4x2	6
8	8x1	7
16	1x16	4
16	2x8	5
16	4x4	6
16	8x2	7
16	16x1	8

The active-high CLR pin is used to reset the FIFO to the empty state, which sets FULL and AFULL low, and EMPTY and AEMPTY high.

Assuming that the EMPTY flag is not set, new data is read from the FIFO when REN is valid on the active edge of the clock. Write and read transfers are described with timing requirements in Timing Characteristics .

2.10.7 Glitch Elimination

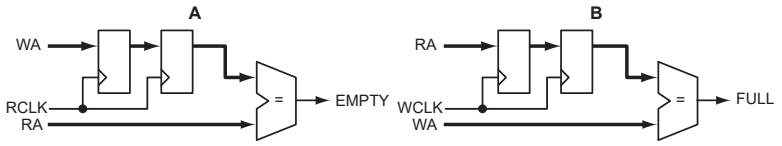
An analog filter is added to each FIFO controller to guarantee glitch-free FIFO-flag logic.

© 2024 Microchip Technology Inc. and its subsidiaries

2.10.8 Overflow and Underflow Control

The counter MSB keeps track of the difference between the read address (RA) and the write address (WA). The EMPTY flag is set when the read and write addresses are equal. To prevent underflow, the write address is double-sampled by the read clock prior to comparison with the read address (part A in following figure). To prevent overflow, the read address is double-sampled by the write clock prior to comparison to the write address (part B in the following figure).

Figure 2-65. Overflow and Underflow Control



2.10.9 FIFO Configurations

Unlike the RAM, the FIFO's write width and read width cannot be specified independently. For the FIFO, the write and read widths must be the same. The WIDTH pins are used to specify one of six allowable word widths, as shown in the following table.

Table 2-100. FIFO Width Configurations

WIDTH (2:0)	W x D
000	1 x 4k
001	2 x 2k
010	4 x 1k
011	9 x 512
100	18 x 256
101	36 x 128
11x	reserved

The DEPTH pins allow RAM cells to be cascaded to create larger FIFOs. The four pins allow depths of 2, 4, 8, and 16 to be specified. Table 2-90 describes the FIFO depth options for various data width and memory blocks.

2.10.10 Cascading FIFO Blocks

FIFO blocks can be cascaded to create deeper FIFO functions. When building larger FIFO blocks, if the word width can be fractured in a multi-bit FIFO, the fractured word configuration is recommended over a cascaded configuration. For example, 256x36 can be configured as two blocks of 256x18. This should be taken into account when, building the FIFO blocks manually. However, when using SmartGen, the user only needs to specify the depth and width of the necessary FIFO blocks. SmartGen automatically configures these blocks to optimize performance.

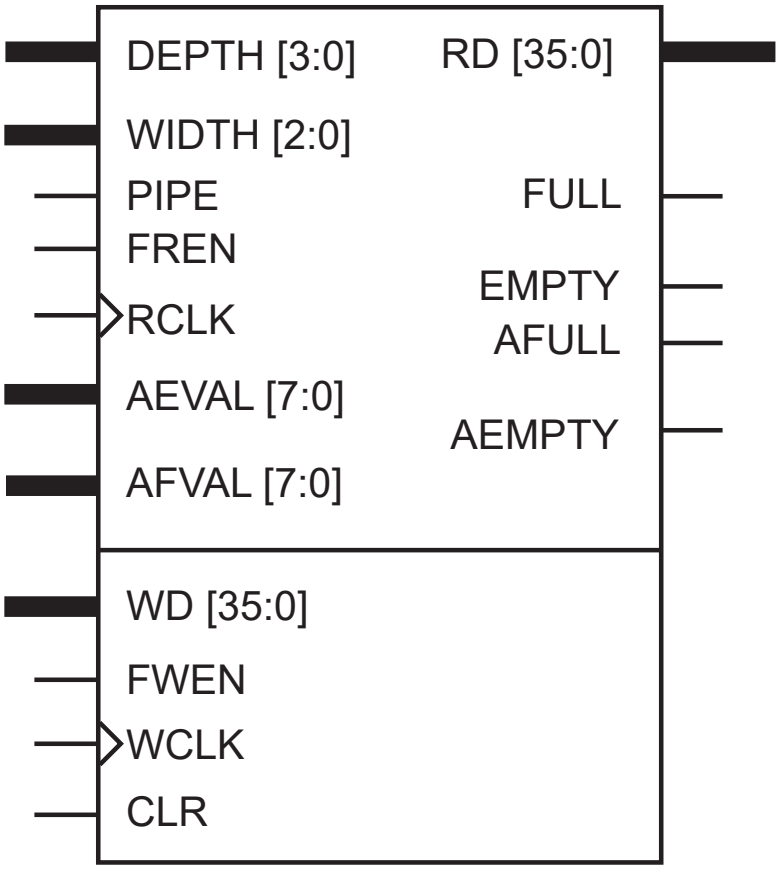
2.10.11 Clock

As with RAM configuration, the RCLK and WCLK pins have independent polarity selection.

The following figure shows a logic block diagram of the Axcelerator FIFO module.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-66. FIFO Block Diagram



The following table lists the FIFO signals and their descriptions.

Table 2-101. FIFO Signal Description

Signal	Direction	Description
WCLK	Input	Write clock (active either edge)
FWEN	Input	FIFO write enable. When this signal is asserted, the WD bus data is latched into the FIFO, and the internal write counters are incremented.
WD[N-1:0]	Input	Write data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
FULL	Output	Active high signal indicating that the FIFO is FULL. When this signal is set, additional write requests are ignored.
AFULL	Output	Active high signal indicating that the FIFO is AFULL
AFVAL	Input	8-bit input defining the AFULL value of the FIFO
RCLK	Input	Read clock (active either edge)
FREN	Input	FIFO read enable
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
EMPTY	Output	Empty flag indicating that the FIFO is EMPTY. When this signal is asserted, attempts to read the FIFO will be ignored.
AEMPTY	Output	Active high signal indicating that the FIFO is AEMPTY
AEVAL	Input	8-bit input defining the almost-empty value of the FIFO
PIPE	Input	Sets the pipe option on or off
CLR	Input	Active high clear input

© 2024 Microchip Technology Inc. and its subsidiaries

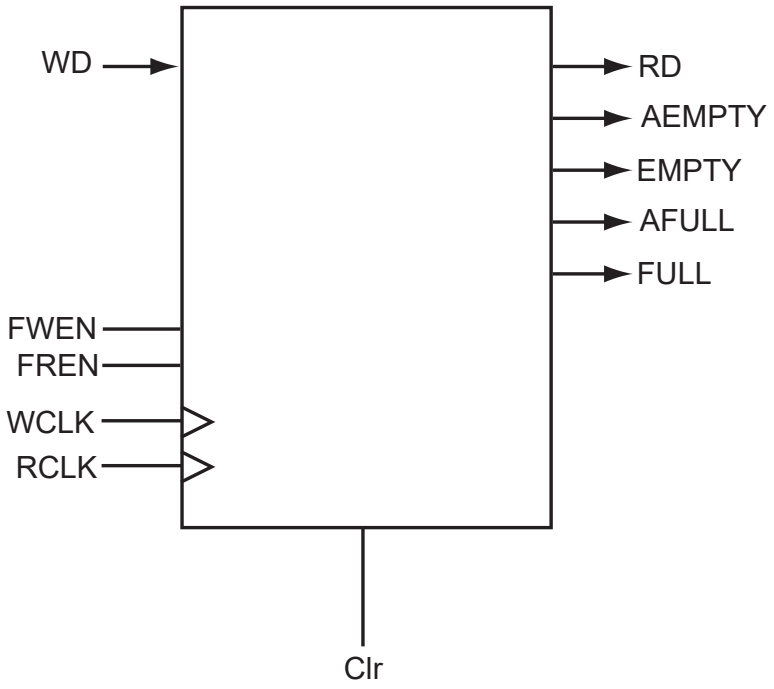
.....continued

Signal	Direction	Description
DEPTH	Input	Determines the depth of the FIFO and the number of FIFOs to be cascaded
WIDTH	Input	Determines the width of the dataword/FIFO, and the number of the FIFOs to be cascaded

2.10.11.1 Timing Characteristics

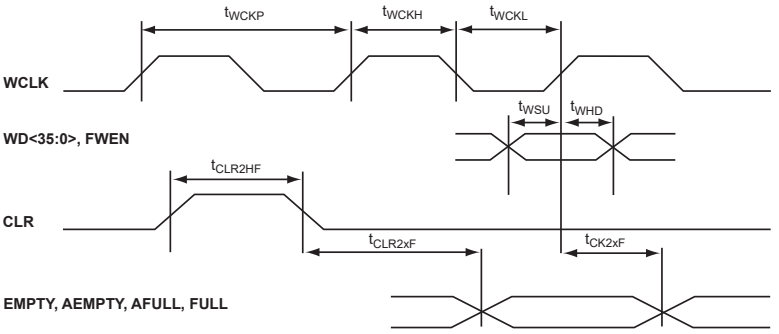
The following figure shows the timing model of FIFO.

Figure 2-67. FIFO Model



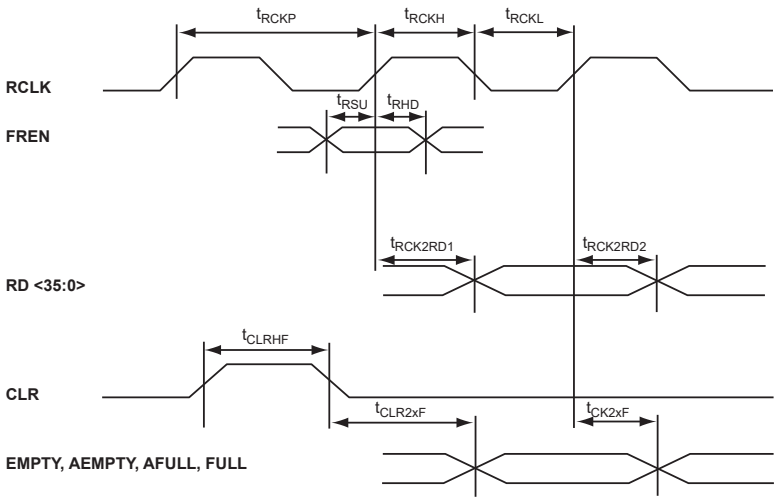
The following figures show the timing waveforms of FIFO write and FIFO read.

Figure 2-68. FIFO Write Timing Waveform



© 2024 Microchip Technology Inc. and its subsidiaries

Figure 2-69. FIFO Read Timing Waveform



The following tables list the timing characteristics of different FIFO blocks.

Table 2-102. One FIFO Block Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2Speed		–1Speed		StdSpeed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
FIFOModule Timing								
t_{WSU}	Write setup	11.40		12.98		15.26		ns
t_{WHD}	Write hold	0.22		0.25		0.30		ns
t_{WCKH}	WCLK high	0.75		0.75		0.75		ns
t_{WCKL}	WCLK low	0.88		0.88		0.88		ns
t_{WCKP}	Minimum WCLK period	1.63		1.63		1.63		ns
t_{RSU}	Read setup	11.63		13.25		15.58		ns
t_{RHD}	Read hold	0.00		0.00		0.00		ns
t_{RCKH}	RCLK high	0.77		0.77		0.77		ns
t_{RCKL}	RCLK low	0.93		0.93		0.93		ns
t_{RCKP}	Minimum RCLK period	1.70		1.70		1.70		ns
t_{CLRHF}	Clear high	0.00		0.00		0.00		ns
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	1.92		2.18		2.57		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	4.39		5.00		5.88		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	2.13		2.42		2.85		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	5.04		5.75		6.75		ns
$t_{RCK2RD1}$	RCLK-to-OUT (Pipelined)	1.32		1.51		1.77		ns
$t_{RCK2RD2}$	RCLK-to-OUT (Non-Pipelined)	2.16		2.46		2.90		ns

Note: Timingdata for this single block FIFO has a depth of 4,096. For all other combinations, use Microchip's timing software.

Table 2-103. Two FIFO Blocks Cascaded Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2Speed		–1Speed		StdSpeed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
FIFOModule Timing								
t_{WSU}	Write setup	13.75		15.66		18.41		ns
t_{WHD}	Write hold	0.00		0.00		0.00		ns

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Parameter	Description	–2Speed		–1Speed		StdSpeed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
FIFOModule Timing								
t_{WCKH}	WCLK high	0.75		0.75		0.75		ns
t_{WCKL}	WCLK low	1.76		1.76		1.76		ns
t_{WCKP}	Minimum WCLK period	2.51		2.51		2.51		ns
t_{RSU}	Read setup	14.33		16.32		19.19		ns
t_{RHD}	Read hold	0.00		0.00		0.00		ns
t_{RCKH}	RCLK high	0.73		0.73		0.73		ns
t_{RCKL}	RCLK low	1.89		1.89		1.89		ns
t_{RCKP}	Minimum RCLK period	2.62		2.62		2.62		ns
t_{CLRHF}	Clear high	0.00		0.00		0.00		ns
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	1.92		2.18		2.57		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	4.39		5.00		5.88		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	2.13		2.42		2.85		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	5.04		5.75		6.75		ns
$t_{RCK2RD1}$	RCLK-to-OUT (Pipelined)	1.43		1.63		1.92		ns
$t_{RCK2RD2}$	RCLK-to-OUT (Non-Pipelined)	2.26		2.58		3.03		ns

Note: Timingdata for these two cascaded FIFO blocks uses a depth of 8,192. For all other combinations, use Microchip's timing software.

Table 2-104. Four FIFO Blocks Cascaded Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2Speed		–1Speed		StdSpeed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
FIFOModule Timing								
t_{WSU}	Write setup	14.60		16.63		19.55		ns
t_{WHD}	Write hold	0.00		0.00		0.00		ns
t_{WCKH}	WCLK high	0.75		0.75		0.75		ns
t_{WCKL}	WCLK low	2.51		2.51		2.51		ns
t_{WCKP}	Minimum WCLK period	3.26		3.26		3.26		ns
t_{RSU}	Read setup	15.27		17.39		20.44		ns
t_{RHD}	Read hold	0.00		0.00		0.00		ns
t_{RCKH}	RCLK high	0.73		0.73		0.73		ns
t_{RCKL}	RCLK low	2.96		2.96		2.96		ns
t_{RCKP}	Minimum RCLK period	3.69		3.69		3.69		ns
t_{CLRHF}	Clear high	0.00		0.00		0.00		ns
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	1.92		2.18		2.57		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	4.39		5.00		5.88		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	2.13		2.42		2.85		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	5.04		5.75		6.75		ns
$t_{RCK2RD1}$	RCLK-to-OUT (Pipelined)	2.36		2.69		3.16		ns
$t_{RCK2RD2}$	RCLK-to-OUT (Non-Pipelined)	2.83		3.23		3.79		ns

Note: Timingdata for these four cascaded FIFO blocks uses a depth of 16,384. For all other combinations, use Microchip's timing software.

© 2024 Microchip Technology Inc. and its subsidiaries

Table 2-105. Eight FIFO Blocks Cascaded Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2Speed		–1Speed		StdSpeed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
FIFOModule Timing								
t_{WSU}	Write setup	15.46		17.61		20.70		ns
t_{WHD}	Write hold	0.00		0.00		0.00		ns
t_{WCKH}	WCLK high	0.75		0.75		0.75		ns
t_{WCKL}	WCLK low	5.13		5.13		5.13		ns
t_{WCKP}	Minimum WCLK period	5.88		5.88		5.88		ns
t_{RSU}	Read setup	16.22		18.47		21.72		ns
t_{RHD}	Read hold	0.00		0.00		0.00		ns
t_{RCKH}	RCLK high	0.73		0.73		0.73		ns
t_{RCKL}	RCLK low	5.77		5.77		5.77		ns
t_{RCKP}	Minimum RCLK period	6.50		6.50		6.50		ns
t_{CLRHF}	Clear high	0.00		0.00		0.00		ns
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	1.92		2.18		2.57		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	4.39		5.00		5.88		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	2.13		2.42		2.85		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	5.04		5.75		6.75		ns
$t_{RCK2RD1}$	RCLK-to-OUT (Pipelined)	3.39		3.86		4.54		ns
$t_{RCK2RD2}$	RCLK-to-OUT (Non-Pipelined)	4.93		5.62		6.61		ns

Note: Timing data for these eight cascaded FIFO blocks uses a depth of 32,768. For all other combinations, useMicrochip's timing software.

Table 2-106. Sixteen FIFO Blocks Cascaded Worst-Case Commercial Conditions VCCA = 1.425V, VCCI = 3.0V, T_J = 70 °C

Parameter	Description	–2Speed		–1Speed		StdSpeed		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
FIFOModule Timing								
t_{WSU}	Write setup	16.32		18.60		21.86		ns
t_{WHD}	Write hold	0.00		0.00		0.00		ns
t_{WCKH}	WCLK high	0.75		0.75		0.75		ns
t_{WCKL}	WCLK low	13.40		13.40		13.40		ns
t_{WCKP}	Minimum WCLK period	14.15		14.15		14.15		ns
t_{RSU}	Read setup	17.16		19.54		22.97		ns
t_{RHD}	Read hold	0.00		0.00		0.00		ns
t_{RCKH}	RCLK high	0.73		0.73		0.73		ns
t_{RCKL}	RCLK low	14.41		14.41		14.41		ns
t_{RCKP}	Minimum RCLK period	15.14		15.14		15.14		ns
t_{CLRHF}	Clear high	0.00		0.00		0.00		ns
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	1.92		2.18		2.57		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	4.39		5.00		5.88		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	2.13		2.42		2.85		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	5.04		5.75		6.75		ns
$t_{RCK2RD1}$	RCLK-to-OUT (Pipelined)	12.08		13.76		16.17		ns
$t_{RCK2RD2}$	RCLK-to-OUT (Non-Pipelined)	12.83		14.62		17.18		ns

© 2024 Microchip Technology Inc. and its subsidiaries

Note: Timing data for these sixteen cascaded FIFO blocks uses a depth of 65,536. For all other combinations, use Microchip's timing software.

2.10.12 Building RAM and FIFO Modules

RAM and FIFO modules can be generated and included in a design in two different ways:

- Using the SmartGen Core Generator where the user defines the depth and width of the FIFO/RAM, and then instantiates this block into the design (for more information, see the SmartGen, FlashROM, Analog System Builder, and Flash Memory System Builder User's Guide).
- The alternative is to instantiate the RAM/FIFO blocks manually, using inverters for polarity control and tying all unused data bits to ground.

2.11 Other Architectural Features

2.11.1 Low Power Mode

Although designed for high performance, the AX architecture also allows the user to place the device into a low power mode. Each I/O bank in an Axcelerator device can be configured individually, when in low power mode, to tristate all outputs, disable inputs, or both. The low power mode is activated by asserting the LP pin, which is grounded in normal operation.

While in the low power mode, the device is still fully functional and all internal logic states are preserved. This allows a user to disable all but a few signals and operate the part in a low-frequency, watchdog mode if desired. If the I/O bank is not disabled, differential I/Os belonging to the I/O bank will still consume normal power, even when operating in the low power mode.

The Axcelerator device will resume normal operation 10 µs after the LP pin is pulled Low.

To further reduce power consumption, the internal charge pump can be bypassed and an external power supply voltage can be used instead. This saves the internal charge-pump operating current, resulting in no DC current draw. The Axcelerator family devices have a dedicated "VPUMP" pin that can be used to access an external charge pump device. In normal chip operation, when using the internal charge pump, VPUMP should be tied to GND. When the voltage level on VPUMP is set to 3.3V, the internal charge pump is turned off, and the VPUMP voltage will be used as the charge pump voltage. Adequate voltage regulation (that is, high drive, low output impedance, and good decoupling) should be used at VPUMP.

In addition, any PLL in use can be powered down to further reduce power consumption. This can be done with the PowerDown pin driven Low. Driving this pin High restarts the PLL with the output clock(s) being stable once lock is restored.

2.11.2 JTAG

Axcelerator offers a JTAG interface that is compliant with the IEEE 1149.1 standard. The user can employ the JTAG interface for probing a design and performing any JTAG Public Instructions as defined in the following table.

Table 2-107. JTAG Instruction Code

Instruction (IR4:IR0)	Binary Code
Extest	00000
Preload/Sample	00001
Intest	00010
USERCODE	00011
IDCODE	00100
HIGHZ	01110
CLAMP	01111
Diagnostic	10000

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued	
Instruction (IR4:IR0)	Binary Code
Reserved	All others
Bypass	11111

2.11.3 Interface

The interface consists of four inputs: Test Mode Select (TMS), Test Data In (TDI), Test Clock (TCK), TAP Controller Reset (TRST), an output, and Test Data Out (TDO). TMS, TDI, and TRST have on-chip pull-up resistors.

2.11.3.1 TRST

Test-Logic Reset (TRST) is an active-low, asynchronous reset signal to the TAP controller. The TRST input can be used to reset the Test Access Port (TAP) Controller to the TRST state. The TAP Controller can be held at this state permanently by grounding the TRST pin. To hold the JTAG TAP controller in the TRST state, it is recommended to connect TRST to ground via a 1 kΩ resistor.

There is an optional internal pull-up resistor available for the TRST input that can be set by the user at programming. Care should be exercised when using this option in combination with an external tie-off to ground.

An on-chip Power-On-Reset (POWRST) circuit is included. POWRST has the same function as TRST, but it only occurs at power-up or during recovery from a VCCA and/or VCCDA voltage drop.

2.11.3.2 TDO

TDO is normally tristated, and it is active only when the TAP controller is in the “Shift_DR” state or “Shift_IR” state. The least significant bit of the selected register (that is, IR or DR) is clocked out to TDO first by the falling edge of TCK.

2.11.3.3 TAP Controller

The TAP Controller is compliant with the IEEE Standard 1149.1. It is a state machine of 16 states that controls the Instruction Register (IR) and the Data Registers (such as BSR, IDCODE, USRCODE, BYPASS, and so on.). The TAP Controller steps into one of the states depending on the sequence of TMS at the rising edges of TCK.

2.11.3.4 Instruction Register (IR)

The IR has five bits (IR4 to IR0). At the TRST state, IR is reset to IDCODE. Each time when IR is selected, it goes through “select IR-Scan,” “Capture-IR,” “Shift-IR,” all the way through “Update-IR.” When there is no test error, the first five data bits coming out of TDO during the “Shift-IR” will be “10111”. If a test error occurs, the last three bits will contain one to three zeroes corresponding to negatively asserted signals: “TDO_ERRORB,” “PROBA_ERRORB,” and “PROBB_ERRORB.” The error(s) will be erased when the TAP is at the “Update-IR” or the TRST state. When in user mode start-up sequence, if the micro-probe has not been used, the “PROBA_ERRORB” is used as a “Power-up done successfully” flag.

2.11.3.5 Data Registers (DRs)

Data registers are distributed throughout the chip. They store testing/programming vectors. The MSB of a data register is connected to TDI, while the LSB is connected to TDO. There are different types of data registers. Descriptions of the main registers are as follow:

IDCODE:

The IDCODE is a 20-bit hard coded JTAG Silicon Signature. It is a hardwired device ID code, which contains the Microchip identity, part number, and version number in a specific JTAG format.

USERCODE:

The USERCODE is a 33-bit programmable register. However, only 20 bits are allocated to use as JTAG Silicon Signature. It is a supplementary identity code for the user to program information

© 2024 Microchip Technology Inc. and its subsidiaries

to distinguish different programmed parts. USERCODE fuses will read out as “zeroes” when not programmed, so only the “1” bits need to be programmed.

Boundary-Scan Register (BSR):

Each I/O contains three Boundary-Scan Cells. Each cell has a shift register bit, a latch, and two MUXes. The boundary-scan cells are used for the Output-enable (E), Output (O), and Input (I) registers. The bit order of the boundary-scan cells for each of them is E-O-I. The boundary-scan cells are then chained serially to form the Boundary-Scan Register (BSR). The length of the BSR is the number of I/Os in the die multiplied by three.

Bypass Register (BYR):

This is the “1-bit” register. It is used to shorten the TDI-TDO serial chain in board-level testing to only one bit per device not being tested. It is also selected for all “reserved” or unused instructions.

2.11.3.6 Probing

Internal activities of the JTAG interface can be observed via the Silicon Explorer II probes: “PRA,” “PRB,” “PRC,” and “PRD.”

2.11.4 Special Fuses

2.11.4.1 Security

Microchip antifuse FPGAs, with FuseLock technology, offer the highest level of design security available in a programmable logic device. Since antifuse FPGAs are live-at power-up, there is no bitstream that can be intercepted, and no bitstream or programming data is ever downloaded to the device during power-up, thus protecting against device cloning. In addition, special security fuses are hidden throughout the fabric of the device and may be programmed by the user to thwart attempts to reverse engineer the device by attempting to exploit either the programming or probing interfaces. Both invasive and noninvasive attacks against an Axcelerator device that access or bypass these security fuses will destroy access to the rest of the device. (see the Design Security in Nonvolatile Flash and Antifuse FPGAs white paper).

Look for the following symbol to ensure your valuable IP is protected with highest level of security in the industry.

Figure 2-70. FuseLock Logo

To ensure maximum security in Axcelerator devices, it is recommended that the user program the device security fuse (SFUS). When programmed, the Silicon Explorer II testing probes are disabled to prevent internal probing, and the programming interface is also disabled. All JTAG public instructions are still accessible by the user.

2.11.4.2 Global Set Fuse

The Global Set Fuse determines if all R-cells and I/O registers (InReg, OutReg, and EnReg) are either cleared or preset by driving the GCLR and GPSET inputs of all R-cells and I/O Registers (see Figure 2-32). Default setting is to clear all registers (GCLR = 0 and GPSET =1) at device power-up. When the GBSETFUS option is checked during FUSE file generation, all registers are preset (GCLR = 1 and GPSET= 0). A local CLR or PRESET will take precedence over this setting. Both pins are pulled High during normal device operation. For use details, see the Libero IDE online help.

2.11.5 Silicon Explorer II Probe Interface

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer tools, allows users to examine any of the internal nets (except I/O registers) of the device

© 2024 Microchip Technology Inc. and its subsidiaries

while it is operating in a prototype or a production system. The user can probe up to four nodes at a time without changing the placement and routing of the design and without using any additional device resources. Highlighted nets in Designer's ChipPlanner can be accessed using Silicon Explorer II in order to observe their real time values.

Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle. In addition, Silicon Explorer II does not require relayout or additional MUXes to bring signals out to external pins, which is necessary when using programmable logic devices from other suppliers. By eliminating multiple place-and-route program cycles, the integrity of the design is maintained throughout the debug process.

Each member of the Axcelerator family has four external pads: PRA, PRB, PRC, and PRD. These can be used to bring out four probe signals from the Axcelerator device (note that the AX125 only has two probe signals that can be observed: PRA and PRB). Each core tile has up to two probe signals. To disallow probing, the SFUS security fuse in the silicon signature has to be programmed (see Special Fuses).

Silicon Explorer II connects to the host PC using a standard serial port connector. Connections to the circuit board are achieved using a nine-pin D-Sub connector (see Figure 1-9). Once the design has been placed-and-routed, and the Axcelerator device has been programmed, Silicon Explorer II can be connected and the Explorer software can be launched.

Silicon Explorer II comes with an additional optional PC hosted tool that emulates an 18-channel logic analyzer. Four channels are used to monitor four internal nodes, and 14 channels are available to probe external signals. The software included with the tool provides the user with an intuitive interface that allows for easy viewing and editing of signal waveforms.

2.12 Programming

Device programming is supported through the Silicon Sculptor II, a single-site, robust and compact device programmer for the PC. Up to four Silicon Sculptor IIs can be daisy-chained and controlled from a single PC host. With standalone software for the PC, Silicon Sculptor II is designed to allow concurrent programming of multiple units from the same PC when daisy-chained.

Silicon Sculptor II programs devices independently to achieve the fastest programming times possible. Each fuse is verified by Silicon Sculptor II to ensure correct programming. Furthermore, at the end of programming, there are integrity tests that are run to ensure that programming was completed properly. Not only does it test programmed and nonprogrammed fuses, Silicon Sculptor II also provides a self-test to test its own hardware extensively.

Programming an Axcelerator device using Silicon Sculptor II is similar to programming any other antifuse device. The procedure is as follows:

Load the *.AFM file.

Select the device to be programmed.

Begin programming.

When the design is ready to go to production, Microchip offers device volume-programming services either through distribution partners or via our In-House Programming Center.

In addition, BP Microsystems offers multi-site programmers that provide qualified support for Axcelerator devices.

For more details on programming the Axcelerator devices, see the Silicon Sculptor II User's Guide.

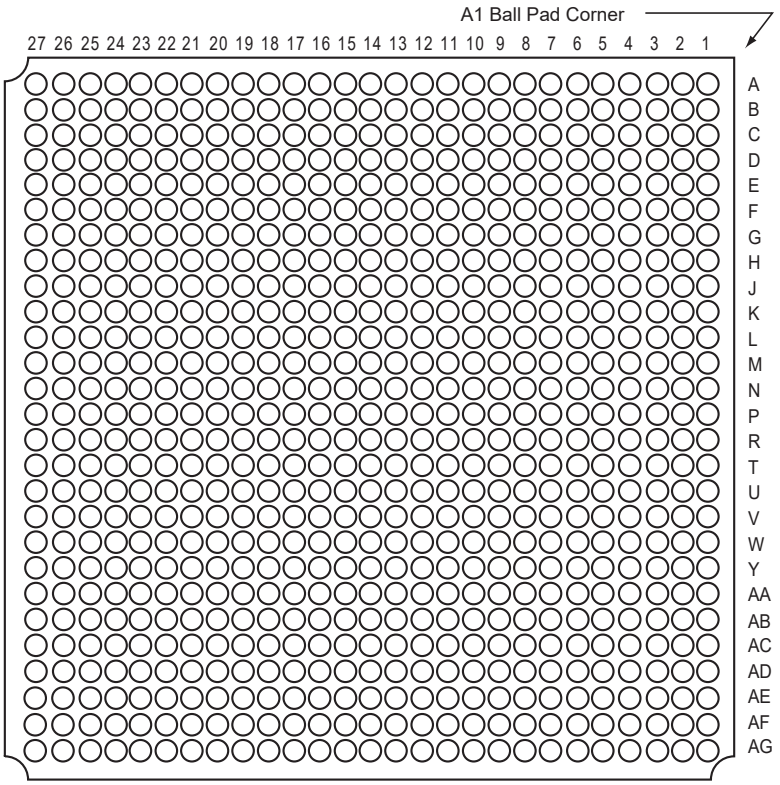
© 2024 Microchip Technology Inc. and its subsidiaries

3. Package Pin Assignments

3.1 BG729

The following figure shows package bottom-view of BG729.

Figure 3-1. Package Bottom-View



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

The following table lists the IOD interface pin placement.

Table 3-1. Packaging Pin Assignment Table (PPAT)

BG729	
AX1000 Function	Pin Number
Bank 0	
IO00NB0F0	E6
IO00PB0F0	F6
IO01NB0F0	G8
IO01PB0F0	G7
IO02NB0F0	D7
IO02PB0F0	E7
IO03NB0F0	D5
IO03PB0F0	E5
IO04NB0F0	G9
IO04PB0F0	H9

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
IO05NB0F0	E8
IO05PB0F0	F8
IO06NB0F0	C6
IO06PB0F0	D6
IO07NB0F0	B5
IO07PB0F0	C5
IO08NB0F0	A6
IO08PB0F0	A5
IO09NB0F0	E9
IO09PB0F0	F9
IO10NB0F0	G10
IO10PB0F0	H10
IO11NB0F0	B7
IO11PB0F0	B6
IO12NB0F1	C8
IO12PB0F1	C7
IO13NB0F1	E10
IO13PB0F1	F10
IO14NB0F1	G11
IO14PB0F1	H11
IO15NB0F1	D9
IO15PB0F1	D8
IO16NB0F1	A8
IO16PB0F1	A7
IO17NB0F1	B9
IO17PB0F1	B8
IO18NB0F1	C10
IO18PB0F1	C9
IO19NB0F1	E11
IO19PB0F1	F11
IO20NB0F1	G12
IO20PB0F1	H12
IO21NB0F1	D11
IO21PB0F1	D10
IO22NB0F2	A10
IO22PB0F2	A9
IO23NB0F2	B11
IO23PB0F2	B10
IO24NB0F2	G13
IO24PB0F2	H13
IO25NB0F2	C12
IO25PB0F2	C11
IO26NB0F2	E12
IO26PB0F2	D12

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
IO27NB0F2	E13
IO27PB0F2	F13
IO28NB0F2	G14
IO28PB0F2	H14
IO29NB0F2	A12
IO29PB0F2	B12
IO30NB0F2/HCLKAN	C13
IO30PB0F2/HCLKAP	D13
IO31NB0F2/HCLKBN	F14
IO31PB0F2/HCLKBP	E14
Bank 1	
IO32NB1F3/HCLKCN	C14
IO32PB1F3/HCLKCP	B14
IO33NB1F3/HCLKDN	D16
IO33PB1F3/HCLKDP	D15
IO34NB1F3	B16
IO34PB1F3	A16
IO35NB1F3	E15
IO35PB1F3	F15
IO36NB1F3	H15
IO36PB1F3	G15
IO37NB1F3	C17
IO37PB1F3	C16
IO38NB1F3	B18
IO38PB1F3	B17
IO39NB1F3	A18
IO39PB1F3	A17
IO40NB1F3	H16
IO40PB1F3	G16
IO41NB1F4	B19
IO41PB1F4	A19
IO42NB1F4	C19
IO42PB1F4	C18
IO43NB1F4	D18
IO43PB1F4	D17
IO44NB1F4	H17
IO44PB1F4	G17
IO45NB1F4	F17
IO45PB1F4	E17
IO46NB1F4	B20
IO46PB1F4	A20
IO47NB1F4	C21
IO47PB1F4	C20
IO48NB1F4	H18

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
IO48PB1F4	G18
IO49NB1F4	F18
IO49PB1F4	E18
IO50NB1F4	D20
IO50PB1F4	D19
IO51NB1F4	A22
IO51PB1F4	A21
IO52NB1F4	B22
IO52PB1F4	B21
IO53NB1F4	F19
IO53PB1F4	E19
IO54NB1F5	F20
IO54PB1F5	E20
IO55NB1F5	E21
IO55PB1F5	D21
IO56NB1F5	H19
IO56PB1F5	G19
IO57NB1F5	D22
IO57PB1F5	C22
IO58NB1F5	B23
IO58PB1F5	A23
IO59NB1F5	D23
IO59PB1F5	C23
IO60NB1F5	G21
IO60PB1F5	G20
IO61NB1F5	E23
IO61PB1F5	E22
IO62NB1F5	F22
IO62PB1F5	F21
IO63NB1F5	H20
IO63PB1F5	J19
Bank 2	
IO64NB2F6	J21
IO64PB2F6	H21
IO65NB2F6	F24
IO65PB2F6	F23
IO66NB2F6	F26
IO66PB2F6	F25
IO67NB2F6	E26
IO67PB2F6	E25
IO68NB2F6	J22
IO68PB2F6	H22
IO69NB2F6	G24
IO69PB2F6	G23

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
IO70NB2F6	K20
IO70PB2F6	J20
IO71NB2F6	G26
IO71PB2F6	G25
IO72NB2F6	J24
IO72PB2F6	J23
IO73NB2F6	H24
IO73PB2F6	H23
IO74NB2F7	L21
IO74PB2F7	K21
IO75NB2F7	G27
IO75PB2F7	F27
IO76NB2F7	K23
IO76PB2F7	K22
IO77NB2F7	H26
IO77PB2F7	H25
IO78NB2F7	K25
IO78PB2F7	K24
IO79NB2F7	J26
IO79PB2F7	J25
IO80NB2F7	M20
IO80PB2F7	L20
IO81NB2F7	J27
IO81PB2F7	H27
IO82NB2F7	L23
IO82PB2F7	L22
IO83NB2F7	L25
IO83PB2F7	L24
IO84NB2F7	N21
IO84PB2F7	M21
IO85NB2F8	K27
IO85PB2F8	K26
IO86NB2F8	M23
IO86PB2F8	M22
IO87NB2F8	M25
IO87PB2F8	M24
IO88NB2F8	L27
IO88PB2F8	L26
IO89NB2F8	M27
IO89PB2F8	M26
IO90NB2F8	N23
IO90PB2F8	N22
IO91NB2F8	N25
IO91PB2F8	N24

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
IO92NB2F8	N27
IO92PB2F8	N26
IO93NB2F8	P26
IO93PB2F8	P27
IO94NB2F8	N19
IO94PB2F8	N20
IO95NB2F8	P23
IO95PB2F8	P22
Bank 3	
IO96NB3F9	P25
IO96PB3F9	P24
IO97NB3F9	R26
IO97PB3F9	R27
IO98NB3F9	P21
IO98PB3F9	P20
IO99NB3F9	R24
IO99PB3F9	R25
IO100NB3F9	T26
IO100PB3F9	T27
IO101NB3F9	T24
IO101PB3F9	T25
IO102NB3F9	R20
IO102PB3F9	R21
IO103NB3F9	R23
IO103PB3F9	R22
IO104NB3F9	U26
IO104PB3F9	U27
IO105NB3F9	U24
IO105PB3F9	U25
IO106NB3F9	R19
IO106PB3F9	P19
IO107NB3F10	V26
IO107PB3F10	V27
IO108NB3F10	T23
IO108PB3F10	T22
IO109NB3F10	V24
IO109PB3F10	V25
IO110NB3F10	T20
IO110PB3F10	T21
IO111NB3F10	W26
IO111PB3F10	W27
IO112NB3F10	U22
IO112PB3F10	U23
IO113NB3F10	Y26

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
IO113PB3F10	Y27
IO114NB3F10	U20
IO114PB3F10	U21
IO115NB3F10	W24
IO115PB3F10	W25
IO116NB3F10	V22
IO116PB3F10	V23
IO117NB3F10	Y24
IO117PB3F10	Y25
IO118NB3F11	V20
IO118PB3F11	V21
IO119NB3F11	AA26
IO119PB3F11	AA27
IO120NB3F11	W22
IO120PB3F11	W23
IO121NB3F11	AA24
IO121PB3F11	AA25
IO122NB3F11	W20
IO122PB3F11	W21
IO123NB3F11	AB26
IO123PB3F11	AB27
IO124NB3F11	Y22
IO124PB3F11	Y23
IO125NB3F11	AB24
IO125PB3F11	AB25
IO126NB3F11	AA22
IO126PB3F11	AA23
IO127NB3F11	AC26
IO127PB3F11	AC27
IO128NB3F11	Y20
IO128PB3F11	W19
Bank 4	
IO129NB4F12	AA20
IO129PB4F12	Y21
IO130NB4F12	AB22
IO130PB4F12	AB23
IO131NB4F12	AC22
IO131PB4F12	AC23
IO132NB4F12	AD23
IO132PB4F12	AD24
IO133NB4F12	AF23
IO133PB4F12	AE23
IO134NB4F12	AC21
IO134PB4F12	AB21

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
IO135NB4F12	AC20
IO135PB4F12	AB20
IO136NB4F12	AD21
IO136PB4F12	AD22
IO137NB4F12	Y19
IO137PB4F12	AA19
IO138NB4F12	AE21
IO138PB4F12	AE22
IO139NB4F13	AF21
IO139PB4F13	AF22
IO140NB4F13	AG22
IO140PB4F13	AG23
IO141NB4F13	Y18
IO141PB4F13	AA18
IO142NB4F13	AE20
IO142PB4F13	AD20
IO143NB4F13	AG20
IO143PB4F13	AG21
IO144NB4F13	AC19
IO144PB4F13	AB19
IO145NB4F13	AD18
IO145PB4F13	AD19
IO146NB4F13	AC18
IO146PB4F13	AB18
IO147NB4F13	Y17
IO147PB4F13	AA17
IO148NB4F13	AF19
IO148PB4F13	AF20
IO149NB4F13	AC17
IO149PB4F13	AB17
IO150NB4F13	AE18
IO150PB4F13	AE19
IO151NB4F13	AA16
IO151PB4F13	Y16
IO152NB4F14	AG18
IO152PB4F14	AG19
IO153NB4F14	AC16
IO153PB4F14	AB16
IO154NB4F14	AF17
IO154PB4F14	AF18
IO155NB4F14	AB15
IO155PB4F14	AC15
IO156NB4F14	AE16
IO156PB4F14	AE17

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
IO157NB4F14	Y15
IO157PB4F14	AA15
IO158NB4F14	AG16
IO158PB4F14	AG17
IO159NB4F14/CLKEN	AF15
IO159PB4F14/CLKEP	AF16
IO160NB4F14/CLKFN	AD14
IO160PB4F14/CLKFP	AD15
Bank 5	
IO161NB5F15/CLKGN	AE14
IO161PB5F15/CLKGP	AE15
IO162NB5F15/CLKHN	AC13
IO162PB5F15/CLKHP	AD13
IO163NB5F15	Y14
IO163PB5F15	AA14
IO164NB5F15	AE13
IO164PB5F15	AF13
IO165NB5F15	AF12
IO165PB5F15	AG12
IO166NB5F15	AD12
IO166PB5F15	AE12
IO167NB5F15	Y13
IO167PB5F15	AA13
IO168NB5F15	AD11
IO168PB5F15	AE11
IO169NB5F15	AG11
IO169PB5F15	AF11
IO170NB5F15	AB11
IO170PB5F15	AC11
IO171NB5F16	AF10
IO171PB5F16	AG10
IO172NB5F16	AD10
IO172PB5F16	AE10
IO173NB5F16	Y12
IO173PB5F16	AA12
IO174NB5F16	AB10
IO174PB5F16	AC10
IO175NB5F16	AF9
IO175PB5F16	AG9
IO176NB5F16	AD9
IO176PB5F16	AE9
IO177NB5F16	Y11
IO177PB5F16	AA11
IO178NB5F16	AF8

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
IO178PB5F16	AG8
IO179NB5F16	AD8
IO179PB5F16	AE8
IO180NB5F16	AB9
IO180PB5F16	AC9
IO181NB5F17	Y10
IO181PB5F17	AA10
IO182NB5F17	AF7
IO182PB5F17	AG7
IO183NB5F17	AD7
IO183PB5F17	AE7
IO184NB5F17	AC7
IO184PB5F17	AC8
IO185NB5F17	AF6
IO185PB5F17	AG6
IO186NB5F17	AB7
IO186PB5F17	AB8
IO187NB5F17	Y9
IO187PB5F17	AA9
IO188NB5F17	AD6
IO188PB5F17	AE6
IO189NB5F17	AB6
IO189PB5F17	AC6
IO190NB5F17	AF5
IO190PB5F17	AG5
IO191NB5F17	AA6
IO191PB5F17	AA7
IO192NB5F17	Y8
IO192PB5F17	AA8
Bank 6	
IO193NB6F18	W8
IO193PB6F18	Y7
IO194NB6F18	AB5
IO194PB6F18	AC5
IO195NB6F18	AC2
IO195PB6F18	AC3
IO196NB6F18	AC4
IO196PB6F18	AD4
IO197NB6F18	Y5
IO197PB6F18	Y6
IO198NB6F18	AB3
IO198PB6F18	AB4
IO199NB6F18	V7
IO199PB6F18	W7

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
IO200NB6F18	AA4
IO200PB6F18	AA5
IO201NB6F18	W5
IO201PB6F18	W6
IO202NB6F18	AB1
IO202PB6F18	AC1
IO203NB6F19	Y3
IO203PB6F19	AA3
IO204NB6F19	AA2
IO204PB6F19	AB2
IO205NB6F19	U8
IO205PB6F19	V8
IO206NB6F19	V5
IO206PB6F19	V6
IO207NB6F19	Y1
IO207PB6F19	AA1
IO208NB6F19	W4
IO208PB6F19	Y4
IO209NB6F19	T7
IO209PB6F19	U7
IO210NB6F19	W2
IO210PB6F19	Y2
IO211NB6F19	U5
IO211PB6F19	U6
IO212NB6F19	V3
IO212PB6F19	W3
IO213NB6F19	R9
IO213PB6F19	T8
IO214NB6F20	U4
IO214PB6F20	V4
IO215NB6F20	T5
IO215PB6F20	T6
IO216NB6F20	V1
IO216PB6F20	W1
IO217NB6F20	R7
IO217PB6F20	R8
IO218NB6F20	U2
IO218PB6F20	V2
IO219NB6F20	T1
IO219PB6F20	U1
IO220NB6F20	R5
IO220PB6F20	R6
IO221NB6F20	T3
IO221PB6F20	T4

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
IO222NB6F20	R2
IO222PB6F20	T2
IO223NB6F20	P8
IO223PB6F20	P9
IO224NB6F20	R3
IO224PB6F20	R4
Bank 7	
IO225NB7F21	P1
IO225PB7F21	R1
IO226NB7F21	P3
IO226PB7F21	P2
IO227NB7F21	N7
IO227PB7F21	P7
IO228NB7F21	P5
IO228PB7F21	P4
IO229NB7F21	N2
IO229PB7F21	N1
IO230NB7F21	N6
IO230PB7F21	P6
IO231NB7F21	N9
IO231PB7F21	N8
IO232NB7F21	N4
IO232PB7F21	N3
IO233NB7F21	M2
IO233PB7F21	M1
IO234NB7F21	M4
IO234PB7F21	M3
IO235NB7F21	M5
IO235PB7F21	N5
IO236NB7F22	L2
IO236PB7F22	L1
IO237NB7F22	L4
IO237PB7F22	L3
IO238NB7F22	L6
IO238PB7F22	M6
IO239NB7F22	M8
IO239PB7F22	M7
IO240NB7F22	K2
IO240PB7F22	K1
IO241NB7F22	K4
IO241PB7F22	K3
IO242NB7F22	K5
IO242PB7F22	L5
IO243NB7F22	J2

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
IO243PB7F22	J1
IO244NB7F22	J4
IO244PB7F22	J3
IO245NB7F22	H2
IO245PB7F22	H1
IO246NB7F22	H4
IO246PB7F22	H3
IO247NB7F23	L8
IO247PB7F23	L7
IO248NB7F23	J6
IO248PB7F23	K6
IO249NB7F23	H5
IO249PB7F23	J5
IO250NB7F23	G2
IO250PB7F23	G1
IO251NB7F23	K8
IO251PB7F23	K7
IO252NB7F23	G4
IO252PB7F23	G3
IO253NB7F23	F2
IO253PB7F23	F1
IO254NB7F23	G6
IO254PB7F23	H6
IO255NB7F23	F5
IO255PB7F23	G5
IO256NB7F23	F3
IO256PB7F23	F4
IO257NB7F23	H7
IO257PB7F23	J7
Dedicated I/O	
GND	A1
GND	A2
GND	A25
GND	A26
GND	A27
GND	A3
GND	AC24
GND	AE1
GND	AE2
GND	AE25
GND	AE26
GND	AE27
GND	AE3
GND	AE5

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
GND	AF1
GND	AF2
GND	AF25
GND	AF26
GND	AF27
GND	AF3
GND	AG1
GND	AG2
GND	AG25
GND	AG26
GND	AG27
GND	AG3
GND	B1
GND	B2
GND	B25
GND	B26
GND	B27
GND	B3
GND	C1
GND	C2
GND	C25
GND	C26
GND	C27
GND	C3
GND	E27
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	L16
GND	L17
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
GND	N16
GND	N17
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND/LP	J8
NC	U3
PRA	J14
PRB	D14
PRC	V14
PRD	AB14
TCK	E4
TDI	D4
TDO	J9
TMS	H8
TRST	E3
VCCA	AA21
VCCA	AD5
VCCA	E1

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
VCCA	G22
VCCA	K10
VCCA	K11
VCCA	K17
VCCA	K18
VCCA	L10
VCCA	L18
VCCA	U10
VCCA	U18
VCCA	V10
VCCA	V11
VCCA	V17
VCCA	V18
VCCPLA	A13
VCCPLB	J13
VCCPLC	B15
VCCPLD	C15
VCCPLE	AG14
VCCPLF	AF14
VCCPLG	AB13
VCCPLH	AG13
VCCDA	A11
VCCDA	AB12
VCCDA	AC12
VCCDA	AC25
VCCDA	AD16
VCCDA	AD17
VCCDA	E16
VCCDA	E2
VCCDA	E24
VCCDA	F12
VCCDA	F16
VCCDA	F7
VCCDA	K14
VCCDA	P10
VCCDA	P18
VCCDA	W14
VCCDA	W9
VCCIB0	A4
VCCIB0	B4
VCCIB0	C4
VCCIB0	J10
VCCIB0	J11
VCCIB0	J12

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

BG729	
AX1000 Function	Pin Number
VCCIB0	K12
VCCIB0	K13
VCCIB1	A24
VCCIB1	B24
VCCIB1	C24
VCCIB1	J16
VCCIB1	J17
VCCIB1	J18
VCCIB1	K15
VCCIB1	K16
VCCIB2	D25
VCCIB2	D26
VCCIB2	D27
VCCIB2	K19
VCCIB2	L19
VCCIB2	M18
VCCIB2	M19
VCCIB2	N18
VCCIB3	AD25
VCCIB3	AD26
VCCIB3	AD27
VCCIB3	R18
VCCIB3	T18
VCCIB3	T19
VCCIB3	U19
VCCIB3	V19
VCCIB4	AE24
VCCIB4	AF24
VCCIB4	AG24
VCCIB4	V15
VCCIB4	V16
VCCIB4	W16
VCCIB4	W17
VCCIB4	W18
VCCIB5	AE4
VCCIB5	AF4
VCCIB5	AG4
VCCIB5	V12
VCCIB5	V13
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB6	AD1
VCCIB6	AD2

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

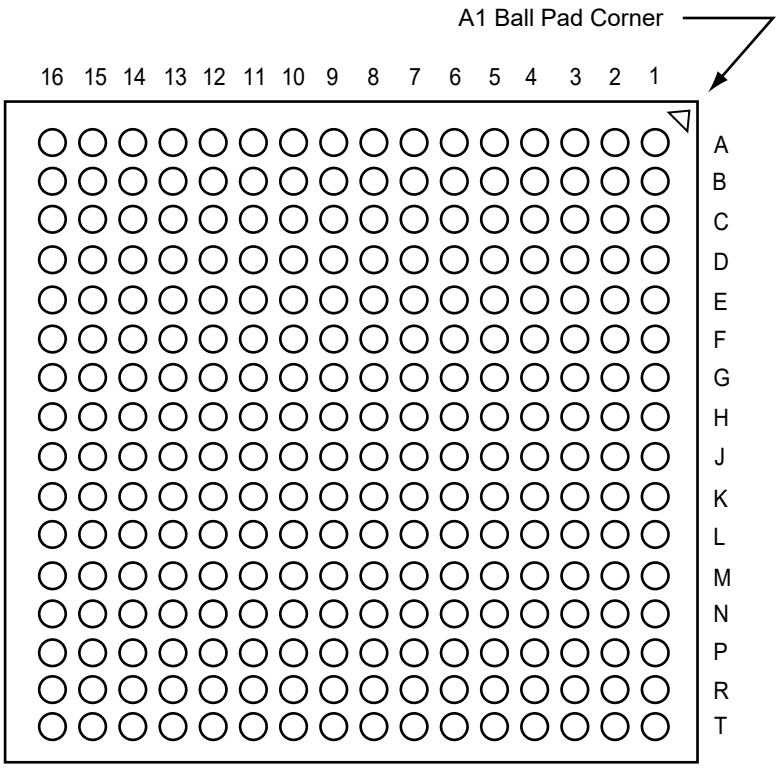
BG729	
AX1000 Function	Pin Number
VCCIB6	AD3
VCCIB6	R10
VCCIB6	T10
VCCIB6	T9
VCCIB6	U9
VCCIB6	V9
VCCIB7	D1
VCCIB7	D2
VCCIB7	D3
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCOMPLA	B13
VCOMPLB	A14
VCOMPLC	A15
VCOMPLD	J15
VCOMPLE	AG15
VCOMPLF	W15
VCOMPLG	AC14
VCOMPLH	W13
VPUMP	D24

3.2 FG256

The following figure shows package bottom-view of FG256.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 3-2. Package Bottom-View



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

The following tables list the IOD interface pin placement.

Table 3-2. Packaging Pin Assignment Table (PPAT)

FG256-Pin FBGA	
AX125 Function	Pin Number
Bank 0	
IO01NB0F0	B4
IO01PB0F0	B3
IO03NB0F0	A4
IO03PB0F0	A3
IO04NB0F0	B6
IO04PB0F0	B5
IO06NB0F0	A6
IO06PB0F0	A5
IO07NB0F0/HCLKAN	B8
IO07PB0F0/HCLKAP	B7
IO08NB0F0/HCLKBN	A9
IO08PB0F0/HCLKBP	A8
Bank 1	
IO09NB1F1/HCLKCN	C10
IO09PB1F1/HCLKCP	C9
IO10NB1F1/HCLKDN	B11
IO10PB1F1/HCLKDP	B10

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG256-Pin FBGA	
AX125 Function	Pin Number
IO12NB1F1	A13
IO12PB1F1	A12
IO13NB1F1	B13
IO13PB1F1	B12
IO14NB1F1	C12
IO14PB1F1	C11
IO15NB1F1	A15
IO15PB1F1	B14
IO16NB1F1	C15
IO16PB1F1	C14
IO17NB1F1	D13
IO17PB1F1	D12
Bank 2	
IO18NB2F2	F13
IO18PB2F2	E13
IO19NB2F2	F14
IO19PB2F2	E14
IO20NB2F2	F15
IO20PB2F2	E15
IO21NB2F2	C16
IO21PB2F2	B16
IO22NB2F2	H13
IO22PB2F2	G13
IO23NB2F2	E16
IO23PB2F2	D16
IO25NB2F2	H15
IO25PB2F2	G15
IO26NB2F2	H14
IO26PB2F2	G14
IO27NB2F2	G16
IO27PB2F2	F16
IO28NB2F2	K15
IO28PB2F2	K16
IO29NB2F2	J16
IO29PB2F2	H16
Bank 3	
IO30NB3F3	K13
IO30PB3F3	J13
IO31NB3F3	K14
IO31PB3F3	J14
IO33NB3F3	L15
IO33PB3F3	L16
IO35NB3F3	P16
IO35PB3F3	N16

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG256-Pin FBGA	
AX125 Function	Pin Number
IO36PB3F3	M16
IO37NB3F3	P15
IO37PB3F3	R16
IO39NB3F3	N15
IO39PB3F3	M15
IO40NB3F3	M13
IO40PB3F3	L13
IO41NB3F3	M14
IO41PB3F3	L14
Bank 4	
IO42NB4F4	N12
IO42PB4F4	N13
IO43NB4F4	T14
IO43PB4F4	R14
IO44PB4F4	T15
IO45NB4F4	R12
IO45PB4F4	R13
IO46NB4F4	P11
IO46PB4F4	P12
IO47PB4F4	T11
IO48NB4F4	T12
IO48PB4F4	T13
IO49NB4F4/CLKEN	R9
IO49PB4F4/CLKEP	R10
IO50NB4F4/CLKFN	T8
IO50PB4F4/CLKFP	T9
Bank 5	
IO51NB5F5/CLKGN	P7
IO51PB5F5/CLKGP	P8
IO52NB5F5/CLKHN	R6
IO52PB5F5/CLKHP	R7
IO54NB5F5	T5
IO54PB5F5	T6
IO55NB5F5	P5
IO55PB5F5	P6
IO56NB5F5	T3
IO56PB5F5	T4
IO57NB5F5	R3
IO57PB5F5	R4
IO58NB5F5	R1
IO58PB5F5	T2
IO59NB5F5	N4
IO59PB5F5	N5
Bank 6	

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG256-Pin FBGA	
AX125 Function	Pin Number
IO60NB6F6	L4
IO60PB6F6	M4
IO61NB6F6	L3
IO61PB6F6	M3
IO63NB6F6	P2
IO63PB6F6	N2
IO64NB6F6	J4
IO64PB6F6	K4
IO65NB6F6	N1
IO65PB6F6	P1
IO67NB6F6	L2
IO67PB6F6	M2
IO69NB6F6	L1
IO69PB6F6	M1
IO70NB6F6	J3
IO70PB6F6	K3
IO71NB6F6	J2
IO71PB6F6	K2
Bank 7	
IO72NB7F7	J1
IO72PB7F7	K1
IO73NB7F7	G2
IO73PB7F7	H2
IO74NB7F7	G3
IO74PB7F7	H3
IO75NB7F7	E1
IO75PB7F7	F1
IO76NB7F7	G1
IO77NB7F7	E2
IO77PB7F7	F2
IO78NB7F7	G4
IO78PB7F7	H4
IO79NB7F7	C1
IO79PB7F7	D1
IO81NB7F7	C2
IO81PB7F7	B1
IO82NB7F7	D2
IO82PB7F7	D3
IO83NB7F7	E3
IO83PB7F7	F3
Dedicated I/O	
VCCDA	E4
GND	A1
GND	A16

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG256-Pin FBGA	
AX125 Function	Pin Number
GND	B15
GND	B2
GND	D15
GND	E12
GND	E5
GND	F11
GND	F6
GND	G10
GND	G7
GND	G8
GND	G9
GND	H10
GND	H7
GND	H8
GND	H9
GND	J10
GND	J7
GND	J8
GND	J9
GND	K10
GND	K7
GND	K8
GND	K9
GND	L11
GND	L6
GND	M12
GND	M5
GND	P13
GND	P3
GND	R15
GND	R2
GND	T1
GND	T16
GND/LP	D4
NC	A11
NC	R11
NC	R5
PRA	D8
PRB	C8
PRC	N9
PRD	P9
TCK	D5
TDI	C6
TDO	C4

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG256-Pin FBGA	
AX125 Function	Pin Number
TMS	C3
TRST	C5
VCCA	D14
VCCA	F10
VCCA	F4
VCCA	F7
VCCA	F8
VCCA	F9
VCCA	G11
VCCA	G6
VCCA	H11
VCCA	H6
VCCA	J11
VCCA	J6
VCCA	K11
VCCA	K6
VCCA	L10
VCCA	L7
VCCA	L8
VCCA	L9
VCCA	N3
VCCA	P14
VCCPLA	C7
VCCPLB	D6
VCCPLC	A10
VCCPLD	D10
VCCPLE	P10
VCCPLF	N11
VCCPLG	T7
VCCPLH	N7
VCCDA	A2
VCCDA	C13
VCCDA	D9
VCCDA	H1
VCCDA	J15
VCCDA	N14
VCCDA	N8
VCCDA	P4
VCCIB0	E6
VCCIB0	E7
VCCIB0	E8
VCCIB1	E10
VCCIB1	E11
VCCIB1	E9

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG256-Pin FBGA	
AX125 Function	Pin Number
VCCIB2	F12
VCCIB2	G12
VCCIB2	H12
VCCIB3	J12
VCCIB3	K12
VCCIB3	L12
VCCIB4	M10
VCCIB4	M11
VCCIB4	M9
VCCIB5	M6
VCCIB5	M7
VCCIB5	M8
VCCIB6	J5
VCCIB6	K5
VCCIB6	L5
VCCIB7	F5
VCCIB7	G5
VCCIB7	H5
VCOMPLA	A7
VCOMPLB	D7
VCOMPLC	B9
VCOMPLD	D11
VCOMPLE	T10
VCOMPLF	N10
VCOMPLG	R8
VCOMPLH	N6
VPUMP	A14

Table 3-3. Packaging Pin Assignment Table (PPAT)

FG256	
AX250 Function	Pin Number
Bank 0	
IO01NB0F0	B4
IO01PB0F0	B3
IO03NB0F0	A4
IO03PB0F0	A3
IO05NB0F0	B6
IO05PB0F0	B5
IO07NB0F0	A6
IO07PB0F0	A5
IO12NB0F0/HCLKAN	B8
IO12PB0F0/HCLKAP	B7
IO13NB0F0/HCLKBN	A9
IO13PB0F0/HCLKBP	A8

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG256	
AX250 Function	Pin Number
Bank 1	
IO14NB1F1/HCLKCN	C10
IO14PB1F1/HCLKCP	C9
IO15NB1F1/HCLKDN	B11
IO15PB1F1/HCLKDP	B10
IO17NB1F1	A13
IO17PB1F1	A12
IO19NB1F1	B13
IO19PB1F1	B12
IO21NB1F1	C12
IO21PB1F1	C11
IO23NB1F1	A15
IO23PB1F1	B14
IO26NB1F1	C15
IO26PB1F1	C14
IO27NB1F1	D13
IO27PB1F1	D12
Bank 2	
IO29NB2F2	F13
IO29PB2F2	E13
IO30NB2F2	F14
IO30PB2F2	E14
IO32NB2F2	C16
IO32PB2F2	B16
IO33NB2F2	F15
IO33PB2F2	E15
IO35NB2F2	H13
IO35PB2F2	G13
IO36NB2F2	E16
IO36PB2F2	D16
IO38NB2F2	H15
IO38PB2F2	G15
IO39NB2F2	H14
IO39PB2F2	G14
IO40NB2F2	G16
IO40PB2F2	F16
IO43NB2F2	K15
IO43PB2F2	K16
IO44NB2F2	J16
IO44PB2F2	H16
Bank 3	
IO45NB3F3	K13
IO45PB3F3	J13
IO46NB3F3	K14

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG256	
AX250 Function	Pin Number
IO46PB3F3	J14
IO52NB3F3	L15
IO52PB3F3	L16
IO54NB3F3	P16
IO54PB3F3	N16
IO55PB3F3	M16
IO56NB3F3	P15
IO56PB3F3	R16
IO58NB3F3	N15
IO58PB3F3	M15
IO59NB3F3	M13
IO59PB3F3	L13
IO61NB3F3	M14
IO61PB3F3	L14
Bank 4	
IO62NB4F4	N12
IO62PB4F4	N13
IO63NB4F4	T14
IO63PB4F4	R14
IO66PB4F4	T15
IO67NB4F4	R12
IO67PB4F4	R13
IO69NB4F4	P11
IO69PB4F4	P12
IO70PB4F4	T11
IO73NB4F4	T12
IO73PB4F4	T13
IO74NB4F4/CLKEN	R9
IO74PB4F4/CLKEP	R10
IO75NB4F4/CLKFN	T8
IO75PB4F4/CLKFP	T9
Bank 5	
IO76NB5F5/CLKGN	P7
IO76PB5F5/CLKGP	P8
IO77NB5F5/CLKHN	R6
IO77PB5F5/CLKHP	R7
IO79NB5F5	T5
IO79PB5F5	T6
IO81NB5F5	P5
IO81PB5F5	P6
IO83NB5F5	T3
IO83PB5F5	T4
IO85NB5F5	R3
IO85PB5F5	R4

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG256	
AX250 Function	Pin Number
IO88NB5F5	R1
IO88PB5F5	T2
IO89NB5F5	N4
IO89PB5F5	N5
Bank 6	
IO91NB6F6	L4
IO91PB6F6	M4
IO92NB6F6	L3
IO92PB6F6	M3
IO94NB6F6	P2
IO94PB6F6	N2
IO97NB6F6	J4
IO97PB6F6	K4
IO98NB6F6	N1
IO98PB6F6	P1
IO100NB6F6	L2
IO100PB6F6	M2
IO102NB6F6	L1
IO102PB6F6	M1
IO103NB6F6	J3
IO103PB6F6	K3
IO104NB6F6	J2
IO104PB6F6	K2
Bank 7	
IO107NB7F7	J1
IO107PB7F7	K1
IO108NB7F7	G2
IO108PB7F7	H2
IO111NB7F7	G3
IO111PB7F7	H3
IO112NB7F7	E1
IO112PB7F7	F1
IO113NB7F7	G1
IO114NB7F7	E2
IO114PB7F7	F2
IO115NB7F7	G4
IO115PB7F7	H4
IO116NB7F7	C1
IO116PB7F7	D1
IO117NB7F7	C2
IO117PB7F7	B1
IO118NB7F7	D2
IO118PB7F7	D3
IO119NB7F7	E3

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG256	
AX250 Function	Pin Number
IO119PB7F7	F3
Dedicated I/O	
VCCDA	E4
GND	A1
GND	A16
GND	B15
GND	B2
GND	D15
GND	E12
GND	E5
GND	F11
GND	F6
GND	G10
GND	G7
GND	G8
GND	G9
GND	H10
GND	H7
GND	H8
GND	H9
GND	J10
GND	J7
GND	J8
GND	J9
GND	K10
GND	K7
GND	K8
GND	K9
GND	L11
GND	L6
GND	M12
GND	M5
GND	P13
GND	P3
GND	R15
GND	R2
GND	T1
GND	T16
GND/LP	D4
PRA	D8
PRB	C8
PRC	N9
PRD	P9
TCK	D5

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG256	
AX250 Function	Pin Number
TDI	C6
TDO	C4
TMS	C3
TRST	C5
VCCA	D14
VCCA	F10
VCCA	F4
VCCA	F7
VCCA	F8
VCCA	F9
VCCA	G11
VCCA	G6
VCCA	H11
VCCA	H6
VCCA	J11
VCCA	J6
VCCA	K11
VCCA	K6
VCCA	L10
VCCA	L7
VCCA	L8
VCCA	L9
VCCA	N3
VCCA	P14
VCCPLA	C7
VCCPLB	D6
VCCPLC	A10
VCCPLD	D10
VCCPLE	P10
VCCPLF	N11
VCCPLG	T7
VCCPLH	N7
VCCDA	A11
VCCDA	A2
VCCDA	C13
VCCDA	D9
VCCDA	H1
VCCDA	J15
VCCDA	N14
VCCDA	N8
VCCDA	P4
VCCDA	R11
VCCDA	R5
VCCIB0	E6

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

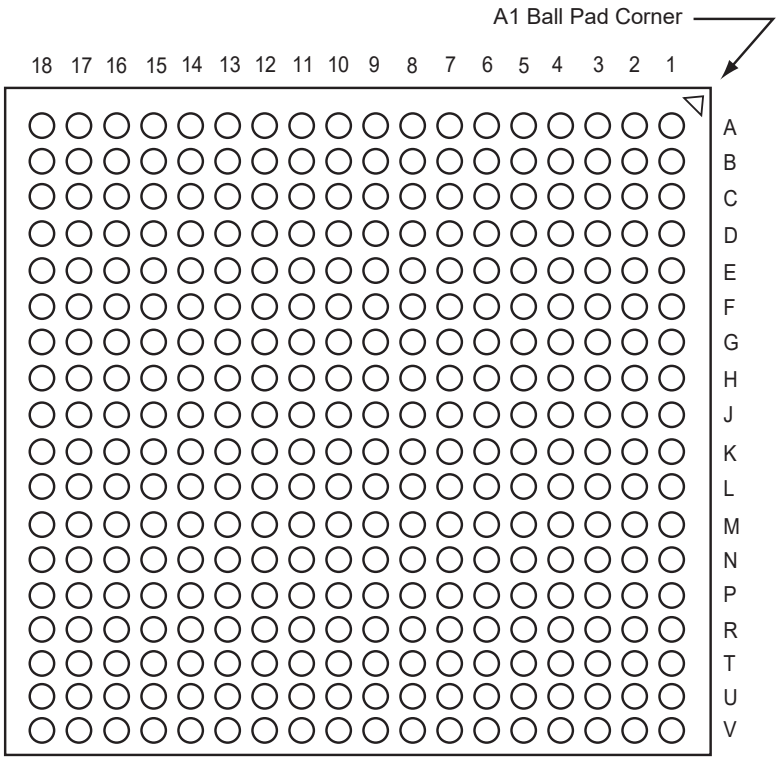
FG256	
AX250 Function	Pin Number
VCCIB0	E7
VCCIB0	E8
VCCIB1	E10
VCCIB1	E11
VCCIB1	E9
VCCIB2	F12
VCCIB2	G12
VCCIB2	H12
VCCIB3	J12
VCCIB3	K12
VCCIB3	L12
VCCIB4	M10
VCCIB4	M11
VCCIB4	M9
VCCIB5	M6
VCCIB5	M7
VCCIB5	M8
VCCIB6	J5
VCCIB6	K5
VCCIB6	L5
VCCIB7	F5
VCCIB7	G5
VCCIB7	H5
VCOMPLA	A7
VCOMPLB	D7
VCOMPLC	B9
VCOMPLD	D11
VCOMPLE	T10
VCOMPLF	N10
VCOMPLG	R8
VCOMPLH	N6
VPUMP	A14

3.3 FG324

The following figure shows package bottom-view of FG324.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 3-3. Package Bottom-View



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

The following table lists the IOD interface pin placement.

Table 3-4. Packaging Pin Assignment Table (PPAT)

FG324	
AX125 Function	Pin Number
Bank 0	
IO00NB0F0	C5
IO00PB0F0	C4
IO01NB0F0	A3
IO01PB0F0	A2
IO02NB0F0	C7
IO02PB0F0	C6
IO03NB0F0	B5
IO03PB0F0	B4
IO04NB0F0	A5
IO04PB0F0	A4
IO05NB0F0	A7
IO05PB0F0	A6
IO06NB0F0	B7
IO06PB0F0	B6
IO07NB0F0/HCLKAN	C9
IO07PB0F0/HCLKAP	C8
IO08NB0F0/HCLKBN	B10

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG324	
AX125 Function	Pin Number
IO08PB0F0/HCLKBP	B9
Bank 1	
IO09NB1F1/HCLKCN	D11
IO09PB1F1/HCLKCP	D10
IO10NB1F1/HCLKDN	C12
IO10PB1F1/HCLKDP	C11
IO11NB1F1	A15
IO11PB1F1	A14
IO12NB1F1	B14
IO12PB1F1	B13
IO13NB1F1	A17
IO13PB1F1	A16
IO14NB1F1	D13
IO14PB1F1	D12
IO15NB1F1	C14
IO15PB1F1	C13
IO16NB1F1	B16
IO16PB1F1	C15
IO17NB1F1	E14
IO17PB1F1	E13
Bank 2	
IO18NB2F2	G14
IO18PB2F2	F14
IO19NB2F2	D16
IO19PB2F2	D15
IO20NB2F2	C18
IO20PB2F2	B18
IO21NB2F2	D17
IO21PB2F2	C17
IO22NB2F2	F17
IO22PB2F2	E17
IO23NB2F2	G16
IO23PB2F2	F16
IO24NB2F2	E18
IO24PB2F2	D18
IO25NB2F2	G18
IO25PB2F2	F18
IO26NB2F2	H17
IO26PB2F2	G17
IO27NB2F2	J16
IO27PB2F2	H16
IO28NB2F2	J18
IO28PB2F2	H18
IO29NB2F2	K17

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG324	
AX125 Function	Pin Number
IO29PB2F2	J17
Bank 3	
IO30NB3F3	N18
IO30PB3F3	M18
IO31NB3F3	L18
IO31PB3F3	K18
IO32NB3F3	L16
IO32PB3F3	L17
IO33NB3F3	R18
IO33PB3F3	P18
IO34NB3F3	N15
IO34PB3F3	M15
IO35NB3F3	M16
IO35PB3F3	M17
IO36NB3F3	P16
IO36PB3F3	N16
IO37NB3F3	R17
IO37PB3F3	P17
IO38NB3F3	N14
IO38PB3F3	M14
IO39NB3F3	U18
IO39PB3F3	T18
IO40NB3F3	R16
IO40PB3F3	T17
IO41NB3F3	P13
IO41PB3F3	P14
Bank 4	
IO42NB4F4	T13
IO42PB4F4	T14
IO43NB4F4	U15
IO43PB4F4	T15
IO44NB4F4	U13
IO44PB4F4	U14
IO45NB4F4	V15
IO45PB4F4	V16
IO46NB4F4	V13
IO46PB4F4	V14
IO47NB4F4	V12
IO47PB4F4	U12
IO48NB4F4	V10
IO48PB4F4	V11
IO49NB4F4/CLKEN	T10
IO49PB4F4/CLKEP	T11
IO50NB4F4/CLKFN	U9

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG324	
AX125 Function	Pin Number
IO50PB4F4/CLKFP	U10
Bank 5	
IO51NB5F5/CLKGN	R8
IO51PB5F5/CLKGP	R9
IO52NB5F5/CLKHN	T7
IO52PB5F5/CLKHP	T8
IO53NB5F5	U6
IO53PB5F5	U7
IO54NB5F5	V8
IO54PB5F5	V9
IO55NB5F5	V6
IO55PB5F5	V7
IO56NB5F5	U4
IO56PB5F5	U5
IO57NB5F5	T4
IO57PB5F5	T5
IO58NB5F5	V4
IO58PB5F5	V5
IO59NB5F5	V2
IO59PB5F5	V3
Bank 6	
IO60NB6F6	P5
IO60PB6F6	P6
IO61NB6F6	T2
IO61PB6F6	U3
IO62NB6F6	T1
IO62PB6F6	U1
IO63NB6F6	P1
IO63PB6F6	R1
IO64NB6F6	R3
IO64PB6F6	P3
IO65NB6F6	P2
IO65PB6F6	R2
IO66NB6F6	M3
IO66PB6F6	N3
IO67NB6F6	M2
IO67PB6F6	N2
IO68NB6F6	M1
IO68PB6F6	N1
IO69NB6F6	K4
IO69PB6F6	L4
IO70NB6F6	K1
IO70PB6F6	L1
IO71NB6F6	K3

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG324	
AX125 Function	Pin Number
IO71PB6F6	L3
Bank 7	
IO72NB7F7	H4
IO72PB7F7	J4
IO73NB7F7	K2
IO73PB7F7	L2
IO74NB7F7	H2
IO74PB7F7	H1
IO75NB7F7	H3
IO75PB7F7	J3
IO76NB7F7	F2
IO76PB7F7	G2
IO77NB7F7	F1
IO77PB7F7	G1
IO78NB7F7	D2
IO78PB7F7	E2
IO79NB7F7	F3
IO79PB7F7	G3
IO80NB7F7	E3
IO80PB7F7	E4
IO81NB7F7	D1
IO81PB7F7	E1
IO82NB7F7	D3
IO82PB7F7	C2
IO83NB7F7	B1
IO83PB7F7	C1
Dedicated I/O	
VCCDA	F5
GND	A1
GND	A18
GND	B17
GND	B2
GND	C16
GND	C3
GND	E16
GND	F13
GND	F6
GND	G12
GND	G7
GND	H10
GND	H11
GND	H8
GND	H9
GND	J10

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG324	
AX125 Function	Pin Number
GND	J11
GND	J8
GND	J9
GND	K10
GND	K11
GND	K8
GND	K9
GND	L10
GND	L11
GND	L8
GND	L9
GND	M12
GND	M7
GND	N13
GND	N6
GND	R14
GND	R4
GND	T16
GND	T3
GND	U17
GND	U2
GND	V1
GND	V18
GND/LP	E5
NC	A10
NC	A11
NC	A12
NC	A13
NC	A8
NC	A9
NC	B12
NC	F15
NC	F4
NC	G15
NC	G4
NC	H14
NC	H15
NC	H5
NC	J1
NC	J14
NC	J15
NC	J5
NC	K14
NC	K15

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG324	
AX125 Function	Pin Number
NC	K5
NC	L14
NC	L15
NC	L5
NC	M4
NC	M5
NC	N17
NC	N4
NC	N5
NC	R12
NC	R13
NC	R6
NC	R7
NC	T12
NC	T6
NC	U16
NC	V17
PRA	E9
PRB	D9
PRC	P10
PRD	R10
TCK	E6
TDI	D7
TDO	D5
TMS	D4
TRST	D6
VCCA	E15
VCCA	G10
VCCA	G11
VCCA	G5
VCCA	G8
VCCA	G9
VCCA	H12
VCCA	H7
VCCA	J12
VCCA	J7
VCCA	K12
VCCA	K7
VCCA	L12
VCCA	L7
VCCA	M10
VCCA	M11
VCCA	M8
VCCA	M9

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG324	
AX125 Function	Pin Number
VCCA	P4
VCCA	R15
VCCPLA	D8
VCCPLB	E7
VCCPLC	B11
VCCPLD	E11
VCCPLE	R11
VCCPLF	P12
VCCPLG	U8
VCCPLH	P8
VCCDA	B3
VCCDA	D14
VCCDA	E10
VCCDA	J2
VCCDA	K16
VCCDA	P15
VCCDA	P9
VCCDA	R5
VCCIB0	F7
VCCIB0	F8
VCCIB0	F9
VCCIB1	F10
VCCIB1	F11
VCCIB1	F12
VCCIB2	G13
VCCIB2	H13
VCCIB2	J13
VCCIB3	K13
VCCIB3	L13
VCCIB3	M13
VCCIB4	N10
VCCIB4	N11
VCCIB4	N12
VCCIB5	N7
VCCIB5	N8
VCCIB5	N9
VCCIB6	K6
VCCIB6	L6
VCCIB6	M6
VCCIB7	G6
VCCIB7	H6
VCCIB7	J6
VCOMPLA	B8
VCOMPLB	E8

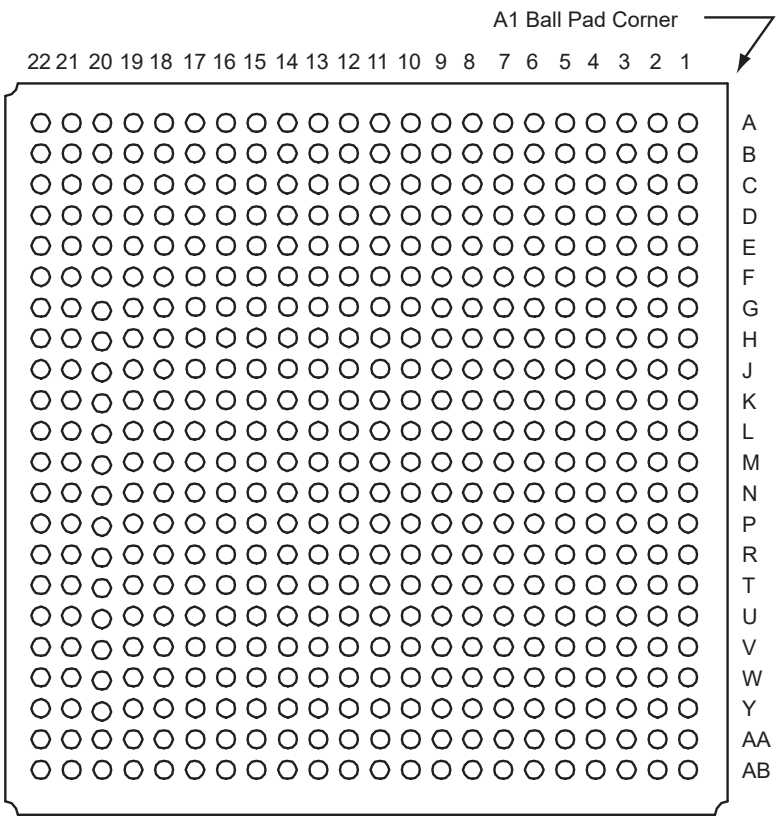
© 2024 Microchip Technology Inc. and its subsidiaries

.....continued	
FG324	
AX125 Function	Pin Number
VCOMPLC	C10
VCOMPLD	E12
VCOMPLE	U11
VCOMPLF	P11
VCOMPLG	T9
VCOMPLH	P7
VPUMP	B15

3.4 FG484

The following figure shows package bottom-view of FG484.

Figure 3-4. Package Bottom-View



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

The following tables list the IOD interface pin placement.

Table 3-5. Packaging Pin Assignment Table (PPAT)

FG484	
AX250 Function	Pin Number
Bank 0	
IO00NB0F0	D7
IO00PB0F0	D6

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX250 Function	Pin Number
IO01NB0F0	E7
IO01PB0F0	E6
IO02NB0F0	C5
IO02PB0F0	C4
IO03NB0F0	C7
IO03PB0F0	C6
IO04NB0F0	E9
IO04PB0F0	E8
IO05NB0F0	D9
IO05PB0F0	D8
IO06NB0F0	B7
IO06PB0F0	B6
IO07NB0F0	C9
IO07PB0F0	C8
IO08NB0F0	A7
IO08PB0F0	A6
IO09NB0F0	B9
IO09PB0F0	B8
IO10NB0F0	A9
IO10PB0F0	A8
IO11NB0F0	B10
IO11PB0F0	A10
IO12NB0F0/HCLKAN	E11
IO12PB0F0/HCLKAP	E10
IO13NB0F0/HCLKBN	D12
IO13PB0F0/HCLKBP	D11
Bank 1	
IO14NB1F1/HCLKCN	F13
IO14PB1F1/HCLKCP	F12
IO15NB1F1/HCLKDN	E14
IO15PB1F1/HCLKDP	E13
IO16NB1F1	C13
IO16PB1F1	C12
IO17NB1F1	B14
IO17PB1F1	B13
IO18NB1F1	A14
IO18PB1F1	A13
IO19NB1F1	A16
IO19PB1F1	A15
IO20NB1F1	B16
IO20PB1F1	B15
IO21NB1F1	C17
IO21PB1F1	C16
IO22NB1F1	F15

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX250 Function	Pin Number
IO22PB1F1	F14
IO23NB1F1	D16
IO23PB1F1	D15
IO24NB1F1	E16
IO24PB1F1	E15
IO25NB1F1	F18
IO25PB1F1	F17
IO26NB1F1	D18
IO26PB1F1	E17
IO27NB1F1	G16
IO27PB1F1	G15
Bank 2	
IO28NB2F2	F19
IO28PB2F2	E19
IO29NB2F2	J16
IO29PB2F2	H16
IO30NB2F2	E20
IO30PB2F2	D20
IO31NB2F2	J17
IO31PB2F2	H17
IO32NB2F2	G20
IO32PB2F2	F20
IO33NB2F2	H19
IO33PB2F2	G19
IO34NB2F2	E22
IO34PB2F2	D22
IO35NB2F2	J18
IO35PB2F2	H18
IO36NB2F2	G21
IO36PB2F2	F21
IO37NB2F2	K19
IO37PB2F2	J19
IO38NB2F2	J20
IO38PB2F2	H20
IO39NB2F2	L16
IO39PB2F2	K16
IO40NB2F2	J21
IO40PB2F2	H21
IO41NB2F2	L17
IO41PB2F2	K17
IO42NB2F2	J22
IO42PB2F2	H22
IO43NB2F2	L18
IO43PB2F2	K18

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX250 Function	Pin Number
IO44NB2F2	L20
IO44PB2F2	K20
Bank 3	
IO45NB3F3	M19
IO45PB3F3	L19
IO46NB3F3	M21
IO46PB3F3	L21
IO47NB3F3	N17
IO47PB3F3	M17
IO48NB3F3	N18
IO48PB3F3	N19
IO49NB3F3	N16
IO49PB3F3	M16
IO50NB3F3	N20
IO50PB3F3	M20
IO51NB3F3	P21
IO51PB3F3	N21
IO52NB3F3	P18
IO52PB3F3	P19
IO53NB3F3	R20
IO53PB3F3	P20
IO54NB3F3	T21
IO54PB3F3	R21
IO55NB3F3	R17
IO55PB3F3	P17
IO56NB3F3	U20
IO56PB3F3	T20
IO57NB3F3	T18
IO57PB3F3	R18
IO58NB3F3	U19
IO58PB3F3	T19
IO59NB3F3	R16
IO59PB3F3	P16
IO60NB3F3	W20
IO60PB3F3	V20
IO61NB3F3	U18
IO61PB3F3	V19
Bank 4	
IO62NB4F4	T15
IO62PB4F4	T16
IO63NB4F4	W17
IO63PB4F4	V17
IO64NB4F4	V15
IO64PB4F4	V16

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX250 Function	Pin Number
IO65NB4F4	Y19
IO65PB4F4	W18
IO66NB4F4	AB18
IO66PB4F4	AB19
IO67NB4F4	W15
IO67PB4F4	W16
IO68NB4F4	U14
IO68PB4F4	U15
IO69NB4F4	AA16
IO69PB4F4	AA17
IO70NB4F4	AB14
IO70PB4F4	AB15
IO71NB4F4	Y14
IO71PB4F4	W14
IO72NB4F4	AA14
IO72PB4F4	AA15
IO73NB4F4	AA13
IO73PB4F4	AB13
IO74NB4F4/CLKEN	V12
IO74PB4F4/CLKEP	V13
IO75NB4F4/CLKFN	W11
IO75PB4F4/CLKFP	W12
Bank 5	
IO76NB5F5/CLKGN	U10
IO76PB5F5/CLKGP	U11
IO77NB5F5/CLKHN	V9
IO77PB5F5/CLKHP	V10
IO78NB5F5	AA9
IO78PB5F5	AA10
IO79NB5F5	AB9
IO79PB5F5	AB10
IO80NB5F5	AA7
IO80PB5F5	AA8
IO81NB5F5	W8
IO81PB5F5	W9
IO82NB5F5	AB5
IO82PB5F5	AB6
IO83NB5F5	AA5
IO83PB5F5	AA6
IO84NB5F5	U8
IO84PB5F5	U9
IO85NB5F5	Y6
IO85PB5F5	Y7
IO86NB5F5	W6

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX250 Function	Pin Number
IO86PB5F5	W7
IO87NB5F5	Y4
IO87PB5F5	Y5
IO88NB5F5	V6
IO88PB5F5	V7
IO89NB5F5	T7
IO89PB5F5	T8
Bank 6	
IO90NB6F6	V4
IO90PB6F6	W5
IO91NB6F6	P7
IO91PB6F6	R7
IO92NB6F6	U5
IO92PB6F6	T5
IO93NB6F6	P6
IO93PB6F6	R6
IO94NB6F6	T4
IO94PB6F6	U4
IO95NB6F6	P5
IO95PB6F6	R5
IO96NB6F6	T3
IO96PB6F6	U3
IO97NB6F6	P3
IO97PB6F6	R3
IO98NB6F6	R2
IO98PB6F6	T2
IO99NB6F6	P4
IO99PB6F6	R4
IO100NB6F6	P1
IO100PB6F6	R1
IO101NB6F6	M7
IO101PB6F6	N7
IO102NB6F6	N2
IO102PB6F6	P2
IO103NB6F6	M6
IO103PB6F6	N6
IO104NB6F6	M4
IO104PB6F6	N4
IO105NB6F6	M5
IO105PB6F6	N5
IO106NB6F6	M3
IO106PB6F6	N3
Bank 7	
IO107NB7F7	M2

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX250 Function	Pin Number
IO107PB7F7	N1
IO108NB7F7	L3
IO108PB7F7	L2
IO109NB7F7	K2
IO109PB7F7	K1
IO110NB7F7	K5
IO110PB7F7	L5
IO111NB7F7	K6
IO111PB7F7	L6
IO112NB7F7	K4
IO112PB7F7	K3
IO113NB7F7	K7
IO113PB7F7	L7
IO114NB7F7	H1
IO114PB7F7	J1
IO115NB7F7	H2
IO115PB7F7	J2
IO116NB7F7	H4
IO116PB7F7	J4
IO117NB7F7	H5
IO117PB7F7	J5
IO118NB7F7	F2
IO118PB7F7	G2
IO119NB7F7	H6
IO119PB7F7	J6
IO120NB7F7	F1
IO120PB7F7	G1
IO121NB7F7	F4
IO121PB7F7	G4
IO122NB7F7	G5
IO122PB7F7	G6
IO123NB7F7	F5
IO123PB7F7	E4
Dedicated I/O	
VCCDA	H7
GND	A1
GND	A11
GND	A12
GND	A2
GND	A21
GND	A22
GND	AA1
GND	AA2
GND	AA21

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX250 Function	Pin Number
GND	AA22
GND	AB1
GND	AB11
GND	AB12
GND	AB2
GND	AB21
GND	AB22
GND	B1
GND	B2
GND	B21
GND	B22
GND	C20
GND	C3
GND	D19
GND	D4
GND	E18
GND	E5
GND	G18
GND	H15
GND	H8
GND	J14
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	L1
GND	L10
GND	L11
GND	L12
GND	L13
GND	L22
GND	M1
GND	M10
GND	M11
GND	M12
GND	M13
GND	M22
GND	N10
GND	N11
GND	N12
GND	N13
GND	P14
GND	P9

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX250 Function	Pin Number
GND	R15
GND	R8
GND	U16
GND	U6
GND	V18
GND	V5
GND	W19
GND	W4
GND	Y20
GND	Y3
GND/LP	G7
NC	A17
NC	A18
NC	A19
NC	A4
NC	A5
NC	AA11
NC	AA12
NC	AA18
NC	AA19
NC	AA4
NC	AB16
NC	AB17
NC	AB4
NC	AB7
NC	AB8
NC	B11
NC	B12
NC	B17
NC	B18
NC	B19
NC	B4
NC	B5
NC	C10
NC	C11
NC	C14
NC	C15
NC	C18
NC	C19
NC	D1
NC	D2
NC	D21
NC	D3
NC	E1

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX250 Function	Pin Number
NC	E2
NC	E21
NC	E3
NC	F22
NC	F3
NC	G22
NC	G3
NC	H3
NC	J3
NC	K21
NC	K22
NC	N22
NC	P22
NC	R19
NC	R22
NC	T1
NC	T22
NC	U1
NC	U2
NC	U21
NC	U22
NC	V1
NC	V2
NC	V21
NC	V22
NC	V3
NC	W1
NC	W2
NC	W21
NC	W22
NC	W3
NC	Y10
NC	Y11
NC	Y12
NC	Y13
NC	Y15
NC	Y16
NC	Y17
NC	Y18
NC	Y8
NC	Y9
PRA	G11
PRB	F11
PRC	T12

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX250 Function	Pin Number
PRD	U12
TCK	G8
TDI	F9
TDO	F7
TMS	F6
TRST	F8
VCCA	G17
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J7
VCCA	K14
VCCA	K9
VCCA	L14
VCCA	L9
VCCA	M14
VCCA	M9
VCCA	N14
VCCA	N9
VCCA	P10
VCCA	P11
VCCA	P12
VCCA	P13
VCCA	T6
VCCA	U17
VCCPLA	F10
VCCPLB	G9
VCCPLC	D13
VCCPLD	G13
VCCPLE	U13
VCCPLF	T14
VCCPLG	W10
VCCPLH	T10
VCCDA	D14
VCCDA	D5
VCCDA	F16
VCCDA	G12
VCCDA	L4
VCCDA	M18
VCCDA	T11
VCCDA	T17
VCCDA	U7
VCCDA	V14

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX250 Function	Pin Number
VCCDA	V8
VCCIB0	A3
VCCIB0	B3
VCCIB0	H10
VCCIB0	H11
VCCIB0	H9
VCCIB1	A20
VCCIB1	B20
VCCIB1	H12
VCCIB1	H13
VCCIB1	H14
VCCIB2	C21
VCCIB2	C22
VCCIB2	J15
VCCIB2	K15
VCCIB2	L15
VCCIB3	M15
VCCIB3	N15
VCCIB3	P15
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA20
VCCIB4	AB20
VCCIB4	R12
VCCIB4	R13
VCCIB4	R14
VCCIB5	AA3
VCCIB5	AB3
VCCIB5	R10
VCCIB5	R11
VCCIB5	R9
VCCIB6	M8
VCCIB6	N8
VCCIB6	P8
VCCIB6	Y1
VCCIB6	Y2
VCCIB7	C1
VCCIB7	C2
VCCIB7	J8
VCCIB7	K8
VCCIB7	L8
VCOMPLA	D10
VCOMPLB	G10
VCOMPLC	E12

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX250 Function	Pin Number
VCOMPLD	G14
VCOMPLE	W13
VCOMPLF	T13
VCOMPLG	V11
VCOMPLH	T9
VPUMP	D17

Table 3-6. Packaging Pin Assignment Table (PPAT)

FG484	
AX500 Function	Pin Number
Bank 0	
IO00NB0F0	E3
IO00PB0F0	D3
IO01NB0F0	E7
IO01PB0F0	E6
IO02NB0F0	C5
IO02PB0F0	C4
IO03NB0F0	D7
IO03PB0F0	D6
IO04NB0F0	B5
IO04PB0F0	B4
IO05NB0F0	C7
IO05PB0F0	C6
IO06NB0F0	A5
IO06PB0F0	A4
IO07NB0F0	A7
IO07PB0F0	A6
IO08NB0F0	B7
IO08PB0F0	B6
IO10NB0F0	B9
IO10PB0F0	B8
IO11NB0F0	E9
IO11PB0F0	E8
IO12NB0F1	D9
IO12PB0F1	D8
IO13NB0F1	C9
IO13PB0F1	C8
IO14NB0F1	A9
IO14PB0F1	A8
IO15NB0F1	B10
IO15PB0F1	A10
IO16NB0F1	B12
IO16PB0F1	B11
IO18NB0F1	C13

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX500 Function	Pin Number
IO18PB0F1	C12
IO19NB0F1/HCLKAN	E11
IO19PB0F1/HCLKAP	E10
IO20NB0F1/HCLKBN	D12
IO20PB0F1/HCLKBP	D11
Bank 1	
IO21NB1F2/HCLKCN	F13
IO21PB1F2/HCLKCP	F12
IO22NB1F2/HCLKDN	E14
IO22PB1F2/HCLKDP	E13
IO24NB1F2	A14
IO24PB1F2	A13
IO25NB1F2	B14
IO25PB1F2	B13
IO26NB1F2	C15
IO27NB1F2	A16
IO27PB1F2	A15
IO28NB1F2	B16
IO28PB1F2	B15
IO29NB1F2	D16
IO29PB1F2	D15
IO30NB1F2	A18
IO30PB1F2	A17
IO31NB1F2	F15
IO31PB1F2	F14
IO32NB1F3	C17
IO32PB1F3	C16
IO33NB1F3	E16
IO33PB1F3	E15
IO34NB1F3	B18
IO34PB1F3	B17
IO35NB1F3	B19
IO35PB1F3	A19
IO36NB1F3	C19
IO36PB1F3	C18
IO37NB1F3	F18
IO37PB1F3	F17
IO38NB1F3	D18
IO38PB1F3	E17
IO39NB1F3	E21
IO39PB1F3	D21
IO40NB1F3	E20
IO40PB1F3	D20
IO41NB1F3	G16

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX500 Function	Pin Number
IO41PB1F3	G15
Bank 2	
IO42NB2F4	F19
IO42PB2F4	E19
IO43NB2F4	J16
IO43PB2F4	H16
IO44NB2F4	E22
IO44PB2F4	D22
IO45NB2F4	H19
IO45PB2F4	G19
IO46NB2F4	G22
IO46PB2F4	F22
IO47NB2F4	J17
IO47PB2F4	H17
IO48NB2F4	G20
IO48PB2F4	F20
IO49NB2F4	J18
IO49PB2F4	H18
IO50NB2F4	G21
IO50PB2F4	F21
IO51NB2F4	K19
IO51PB2F4	J19
IO52NB2F5	J21
IO52PB2F5	H21
IO53NB2F5	J20
IO53PB2F5	H20
IO54NB2F5	J22
IO54PB2F5	H22
IO55NB2F5	L17
IO55PB2F5	K17
IO56NB2F5	K21
IO56PB2F5	K22
IO58NB2F5	L20
IO58PB2F5	K20
IO59NB2F5	L18
IO59PB2F5	K18
IO60NB2F5	M21
IO60PB2F5	L21
IO61NB2F5	L16
IO61PB2F5	K16
IO62NB2F5	M19
IO62PB2F5	L19
Bank 3	
IO63NB3F6	N16

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX500 Function	Pin Number
IO63PB3F6	M16
IO64NB3F6	P22
IO64PB3F6	N22
IO65NB3F6	N20
IO65PB3F6	M20
IO66NB3F6	P21
IO66PB3F6	N21
IO67NB3F6	N18
IO67PB3F6	N19
IO68NB3F6	T22
IO68PB3F6	R22
IO69NB3F6	N17
IO69PB3F6	M17
IO70NB3F6	T21
IO70PB3F6	R21
IO71NB3F6	P18
IO71PB3F6	P19
IO72NB3F6	R20
IO72PB3F6	P20
IO73PB3F6	R19
IO74NB3F7	V21
IO74PB3F7	U21
IO75NB3F7	V22
IO75PB3F7	U22
IO76NB3F7	U20
IO76PB3F7	T20
IO77NB3F7	R17
IO77PB3F7	P17
IO78NB3F7	W21
IO78PB3F7	W22
IO79NB3F7	T18
IO79PB3F7	R18
IO80NB3F7	W20
IO80PB3F7	V20
IO81NB3F7	U19
IO81PB3F7	T19
IO82NB3F7	U18
IO82PB3F7	V19
IO83NB3F7	R16
IO83PB3F7	P16
Bank 4	
IO84NB4F8	AB18
IO84PB4F8	AB19
IO85NB4F8	T15

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX500 Function	Pin Number
IO85PB4F8	T16
IO86NB4F8	AA18
IO86PB4F8	AA19
IO87NB4F8	W17
IO87PB4F8	V17
IO88NB4F8	Y19
IO88PB4F8	W18
IO89NB4F8	U14
IO89PB4F8	U15
IO90NB4F8	Y17
IO90PB4F8	Y18
IO91NB4F8	V15
IO91PB4F8	V16
IO92PB4F8	AB17
IO93NB4F8	Y15
IO93PB4F8	Y16
IO94NB4F9	AA16
IO94PB4F9	AA17
IO95NB4F9	AB14
IO95PB4F9	AB15
IO96NB4F9	W15
IO96PB4F9	W16
IO97NB4F9	AA13
IO97PB4F9	AB13
IO98NB4F9	AA14
IO98PB4F9	AA15
IO100NB4F9	Y14
IO100PB4F9	W14
IO101NB4F9	Y12
IO101PB4F9	Y13
IO102NB4F9	AA11
IO102PB4F9	AA12
IO103NB4F9/CLKEN	V12
IO103PB4F9/CLKEP	V13
IO104NB4F9/CLKFN	W11
IO104PB4F9/CLKFP	W12
Bank 5	
IO105NB5F10/CLKGN	U10
IO105PB5F10/CLKGP	U11
IO106NB5F10/CLKHN	V9
IO106PB5F10/CLKHP	V10
IO107NB5F10	Y10
IO107PB5F10	Y11
IO108NB5F10	AA9

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX500 Function	Pin Number
IO108PB5F10	AA10
IO110NB5F10	AB9
IO110PB5F10	AB10
IO111NB5F10	Y8
IO111PB5F10	Y9
IO112NB5F10	AB7
IO113NB5F10	W8
IO113PB5F10	W9
IO114NB5F11	AA7
IO114PB5F11	AA8
IO115NB5F11	AB5
IO115PB5F11	AB6
IO116NB5F11	Y6
IO116PB5F11	Y7
IO117NB5F11	U8
IO117PB5F11	U9
IO118NB5F11	AA5
IO118PB5F11	AA6
IO119NB5F11	AA4
IO119PB5F11	AB4
IO120NB5F11	Y4
IO120PB5F11	Y5
IO121NB5F11	W6
IO121PB5F11	W7
IO122NB5F11	V3
IO122PB5F11	W3
IO123NB5F11	T7
IO123PB5F11	T8
IO124NB5F11	V4
IO124PB5F11	W5
IO125NB5F11	V6
IO125PB5F11	V7
Bank 6	
IO126NB6F12	V2
IO126PB6F12	W2
IO127NB6F12	P7
IO127PB6F12	R7
IO128NB6F12	V1
IO128PB6F12	W1
IO129NB6F12	U5
IO129PB6F12	T5
IO130NB6F12	T1
IO130PB6F12	U1
IO131NB6F12	P6

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX500 Function	Pin Number
IO131PB6F12	R6
IO132NB6F12	T4
IO132PB6F12	U4
IO133NB6F12	U2
IO134NB6F12	T3
IO134PB6F12	U3
IO135NB6F12	P5
IO135PB6F12	R5
IO136NB6F13	R2
IO136PB6F13	T2
IO138NB6F13	P4
IO138PB6F13	R4
IO139NB6F13	N2
IO139PB6F13	P2
IO140NB6F13	P3
IO140PB6F13	R3
IO141NB6F13	M6
IO141PB6F13	N6
IO142NB6F13	P1
IO142PB6F13	R1
IO143NB6F13	M5
IO143PB6F13	N5
IO144NB6F13	M4
IO144PB6F13	N4
IO145NB6F13	M7
IO145PB6F13	N7
IO146NB6F13	M3
IO146PB6F13	N3
Bank 7	
IO147NB7F14	K7
IO147PB7F14	L7
IO148NB7F14	M2
IO148PB7F14	N1
IO149NB7F14	K5
IO149PB7F14	L5
IO150NB7F14	L3
IO150PB7F14	L2
IO151NB7F14	K6
IO151PB7F14	L6
IO152NB7F14	K2
IO152PB7F14	K1
IO153NB7F14	K4
IO153PB7F14	K3
IO154NB7F14	H3

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX500 Function	Pin Number
IO154PB7F14	J3
IO155NB7F14	H5
IO155PB7F14	J5
IO156NB7F14	H4
IO156PB7F14	J4
IO157NB7F14	H2
IO157PB7F14	J2
IO158NB7F15	H1
IO158PB7F15	J1
IO159NB7F15	F1
IO159PB7F15	G1
IO160NB7F15	F2
IO160PB7F15	G2
IO161NB7F15	H6
IO161PB7F15	J6
IO162NB7F15	F3
IO162PB7F15	G3
IO163NB7F15	G5
IO163PB7F15	G6
IO164NB7F15	D1
IO164PB7F15	E1
IO165NB7F15	F4
IO165PB7F15	G4
IO166NB7F15	D2
IO166PB7F15	E2
IO167NB7F15	F5
IO167PB7F15	E4
Dedicated I/O	
VCCDA	H7
GND	A1
GND	A11
GND	A12
GND	A2
GND	A21
GND	A22
GND	AA1
GND	AA2
GND	AA21
GND	AA22
GND	AB1
GND	AB11
GND	AB12
GND	AB2
GND	AB21

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX500 Function	Pin Number
GND	AB22
GND	B1
GND	B2
GND	B21
GND	B22
GND	C20
GND	C3
GND	D19
GND	D4
GND	E18
GND	E5
GND	G18
GND	H15
GND	H8
GND	J14
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	L1
GND	L10
GND	L11
GND	L12
GND	L13
GND	L22
GND	M1
GND	M10
GND	M11
GND	M12
GND	M13
GND	M22
GND	N10
GND	N11
GND	N12
GND	N13
GND	P14
GND	P9
GND	R15
GND	R8
GND	U16
GND	U6
GND	V18
GND	V5

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX500 Function	Pin Number
GND	W19
GND	W4
GND	Y20
GND	Y3
GND/LP	G7
NC	AB8
NC	AB16
NC	C10
NC	C11
NC	C14
PRA	G11
PRB	F11
PRC	T12
PRD	U12
TCK	G8
TDI	F9
TDO	F7
TMS	F6
TRST	F8
VCCA	G17
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J7
VCCA	K14
VCCA	K9
VCCA	L14
VCCA	L9
VCCA	M14
VCCA	M9
VCCA	N14
VCCA	N9
VCCA	P10
VCCA	P11
VCCA	P12
VCCA	P13
VCCA	T6
VCCA	U17
VCCPLA	F10
VCCPLB	G9
VCCPLC	D13
VCCPLD	G13
VCCPLE	U13

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX500 Function	Pin Number
VCCPLF	T14
VCCPLG	W10
VCCPLH	T10
VCCDA	D14
VCCDA	D5
VCCDA	F16
VCCDA	G12
VCCDA	L4
VCCDA	M18
VCCDA	T11
VCCDA	T17
VCCDA	U7
VCCDA	V14
VCCDA	V8
VCCIB0	A3
VCCIB0	B3
VCCIB0	H10
VCCIB0	H11
VCCIB0	H9
VCCIB1	A20
VCCIB1	B20
VCCIB1	H12
VCCIB1	H13
VCCIB1	H14
VCCIB2	C21
VCCIB2	C22
VCCIB2	J15
VCCIB2	K15
VCCIB2	L15
VCCIB3	M15
VCCIB3	N15
VCCIB3	P15
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA20
VCCIB4	AB20
VCCIB4	R12
VCCIB4	R13
VCCIB4	R14
VCCIB5	AA3
VCCIB5	AB3
VCCIB5	R10
VCCIB5	R11
VCCIB5	R9

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX500 Function	Pin Number
VCCIB6	M8
VCCIB6	N8
VCCIB6	P8
VCCIB6	Y1
VCCIB6	Y2
VCCIB7	C1
VCCIB7	C2
VCCIB7	J8
VCCIB7	K8
VCCIB7	L8
VCOMPLA	D10
VCOMPLB	G10
VCOMPLC	E12
VCOMPLD	G14
VCOMPLE	W13
VCOMPLF	T13
VCOMPLG	V11
VCOMPLH	T9
VPUMP	D17

Table 3-7. Packaging Pin Assignment Table (PPAT)

FG484	
AX1000 Function	Pin Number
Bank 0	
IO01NB0F0	E3
IO01PB0F0	D3
IO02NB0F0	E7
IO02PB0F0	E6
IO05NB0F0	D2
IO05PB0F0	E2
IO06NB0F0	C5
IO06PB0F0	C4
IO12NB0F1	D7
IO12PB0F1	D6
IO13NB0F1	B5
IO13PB0F1	B4
IO14NB0F1	E9
IO14PB0F1	E8
IO15NB0F1	C7
IO15PB0F1	C6
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	B7
IO17PB0F1	B6

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX1000 Function	Pin Number
IO18NB0F1	A7
IO18PB0F1	A6
IO19NB0F1	C9
IO19PB0F1	C8
IO20NB0F1	D9
IO20PB0F1	D8
IO21NB0F1	B9
IO21PB0F1	B8
IO22NB0F2	A9
IO22PB0F2	A8
IO23NB0F2	B10
IO23PB0F2	A10
IO26NB0F2	A14
IO26PB0F2	A13
IO29NB0F2	B12
IO29PB0F2	B11
IO30NB0F2/HCLKAN	E11
IO30PB0F2/HCLKAP	E10
IO31NB0F2/HCLKBN	D12
IO31PB0F2/HCLKBP	D11
Bank 1	
IO32NB1F3/HCLKCN	F13
IO32PB1F3/HCLKCP	F12
IO33NB1F3/HCLKDN	E14
IO33PB1F3/HCLKDP	E13
IO34NB1F3	C13
IO34PB1F3	C12
IO37NB1F3	B14
IO37PB1F3	B13
IO38NB1F3	A16
IO38PB1F3	A15
IO40NB1F3	C15
IO42NB1F4	A18
IO42PB1F4	A17
IO43NB1F4	B16
IO43PB1F4	B15
IO44NB1F4	B18
IO44PB1F4	B17
IO45NB1F4	B19
IO45PB1F4	A19
IO46NB1F4	C19
IO46PB1F4	C18
IO48NB1F4	F15
IO48PB1F4	F14

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX1000 Function	Pin Number
IO49NB1F4	D16
IO49PB1F4	D15
IO50NB1F4	C17
IO50PB1F4	C16
IO51NB1F4	E22
IO51PB1F4	D22
IO52NB1F4	E16
IO52PB1F4	E15
IO57NB1F5	E21
IO57PB1F5	D21
IO60NB1F5	G16
IO60PB1F5	G15
IO61NB1F5	D18
IO61PB1F5	E17
IO63NB1F5	E20
IO63PB1F5	D20
Bank 2	
IO64NB2F6	F18
IO64PB2F6	F17
IO67NB2F6	F19
IO67PB2F6	E19
IO68NB2F6	J16
IO68PB2F6	H16
IO70NB2F6	J17
IO70PB2F6	H17
IO74NB2F7	J18
IO74PB2F7	H18
IO75NB2F7	G20
IO75PB2F7	F20
IO79NB2F7	H19
IO79PB2F7	G19
IO80NB2F7	L16
IO80PB2F7	K16
IO84NB2F7	L17
IO84PB2F7	K17
IO85NB2F8	G21
IO85PB2F8	F21
IO86NB2F8	G22
IO86PB2F8	F22
IO87NB2F8	J20
IO87PB2F8	H20
IO88NB2F8	L18
IO88PB2F8	K18
IO89NB2F8	K19

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX1000 Function	Pin Number
IO89PB2F8	J19
IO90NB2F8	J21
IO90PB2F8	H21
IO91NB2F8	J22
IO91PB2F8	H22
IO93NB2F8	K21
IO93PB2F8	K22
IO94NB2F8	L20
IO94PB2F8	K20
IO95NB2F8	M21
IO95PB2F8	L21
Bank 3	
IO96NB3F9	N16
IO96PB3F9	M16
IO97NB3F9	M19
IO97PB3F9	L19
IO98NB3F9	P22
IO98PB3F9	N22
IO99NB3F9	N20
IO99PB3F9	M20
IO100NB3F9	N17
IO100PB3F9	M17
IO101NB3F9	P21
IO101PB3F9	N21
IO103NB3F9	R20
IO103PB3F9	P20
IO104NB3F9	N18
IO104PB3F9	N19
IO105NB3F9	T22
IO105PB3F9	R22
IO106NB3F9	R17
IO106PB3F9	P17
IO107NB3F10	T21
IO107PB3F10	R21
IO110NB3F10	V22
IO110PB3F10	U22
IO113NB3F10	V21
IO113PB3F10	U21
IO114NB3F10	P18
IO114PB3F10	P19
IO116PB3F10	R19
IO117NB3F10	U20
IO117PB3F10	T20
IO118NB3F11	T18

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX1000 Function	Pin Number
IO118PB3F11	R18
IO121NB3F11	U19
IO121PB3F11	T19
IO124NB3F11	R16
IO124PB3F11	P16
IO127NB3F11	W21
IO127PB3F11	W22
Bank 4	
IO129PB4F12	AB17
IO132NB4F12	Y19
IO132PB4F12	W18
IO133NB4F12	W17
IO133PB4F12	V17
IO135NB4F12	T15
IO135PB4F12	T16
IO138NB4F12	Y17
IO138PB4F12	Y18
IO139NB4F13	V15
IO139PB4F13	V16
IO140NB4F13	U18
IO140PB4F13	V19
IO142NB4F13	W20
IO142PB4F13	V20
IO143NB4F13	W15
IO143PB4F13	W16
IO144NB4F13	AA18
IO144PB4F13	AA19
IO145NB4F13	U14
IO145PB4F13	U15
IO146NB4F13	Y15
IO146PB4F13	Y16
IO147NB4F13	AB18
IO147PB4F13	AB19
IO149NB4F13	Y14
IO149PB4F13	W14
IO150NB4F13	AA16
IO150PB4F13	AA17
IO152NB4F14	AA14
IO152PB4F14	AA15
IO154NB4F14	AB14
IO154PB4F14	AB15
IO155NB4F14	AA13
IO155PB4F14	AB13
IO158NB4F14	Y12

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX1000 Function	Pin Number
IO158PB4F14	Y13
IO159NB4F14/CLKEN	V12
IO159PB4F14/CLKEP	V13
IO160NB4F14/CLKFN	W11
IO160PB4F14/CLKFP	W12
Bank 5	
IO161NB5F15/CLKGN	U10
IO161PB5F15/CLKGP	U11
IO162NB5F15/CLKHN	V9
IO162PB5F15/CLKHP	V10
IO163NB5F15	Y10
IO163PB5F15	Y11
IO167NB5F15	AA11
IO167PB5F15	AA12
IO169NB5F15	AA9
IO169PB5F15	AA10
IO170NB5F15	AB9
IO170PB5F15	AB10
IO171NB5F16	W8
IO171PB5F16	W9
IO172NB5F16	Y8
IO172PB5F16	Y9
IO173NB5F16	U8
IO173PB5F16	U9
IO174NB5F16	AA7
IO174PB5F16	AA8
IO175NB5F16	AB5
IO175PB5F16	AB6
IO176NB5F16	AA5
IO176PB5F16	AA6
IO177NB5F16	AA4
IO177PB5F16	AB4
IO178NB5F16	Y6
IO178PB5F16	Y7
IO179NB5F16	T7
IO179PB5F16	T8
IO180NB5F16	W6
IO180PB5F16	W7
IO181NB5F17	Y4
IO181PB5F17	Y5
IO184NB5F17	AB7
IO187NB5F17	V3
IO187PB5F17	W3
IO188NB5F17	V4

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX1000 Function	Pin Number
IO188PB5F17	W5
IO192NB5F17	V6
IO192PB5F17	V7
Bank 6	
IO194NB6F18	V2
IO194PB6F18	W2
IO195NB6F18	U5
IO195PB6F18	T5
IO200NB6F18	T4
IO200PB6F18	U4
IO201NB6F18	P6
IO201PB6F18	R6
IO203NB6F19	U2
IO204NB6F19	T3
IO204PB6F19	U3
IO205NB6F19	P5
IO205PB6F19	R5
IO208NB6F19	V1
IO208PB6F19	W1
IO209NB6F19	P7
IO209PB6F19	R7
IO212NB6F19	P4
IO212PB6F19	R4
IO214NB6F20	P3
IO214PB6F20	R3
IO215NB6F20	M6
IO215PB6F20	N6
IO216NB6F20	R2
IO216PB6F20	T2
IO217NB6F20	T1
IO217PB6F20	U1
IO219NB6F20	M5
IO219PB6F20	N5
IO220NB6F20	P1
IO220PB6F20	R1
IO221NB6F20	N2
IO221PB6F20	P2
IO222NB6F20	M3
IO222PB6F20	N3
IO223NB6F20	M7
IO223PB6F20	N7
IO224NB6F20	M4
IO224PB6F20	N4
Bank 7	

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX1000 Function	Pin Number
IO225NB7F21	M2
IO225PB7F21	N1
IO226NB7F21	K2
IO226PB7F21	K1
IO228NB7F21	L3
IO228PB7F21	L2
IO229NB7F21	K5
IO229PB7F21	L5
IO230NB7F21	H1
IO230PB7F21	J1
IO231NB7F21	H2
IO231PB7F21	J2
IO232NB7F21	K4
IO232PB7F21	K3
IO233NB7F21	K6
IO233PB7F21	L6
IO234NB7F21	F1
IO234PB7F21	G1
IO235NB7F21	F2
IO235PB7F21	G2
IO236NB7F22	H3
IO236PB7F22	J3
IO237NB7F22	K7
IO237PB7F22	L7
IO241NB7F22	H6
IO241PB7F22	J6
IO242NB7F22	H4
IO242PB7F22	J4
IO243NB7F22	H5
IO243PB7F22	J5
IO246NB7F22	F3
IO246PB7F22	G3
IO250NB7F23	F4
IO250PB7F23	G4
IO253NB7F23	G5
IO253PB7F23	G6
IO254NB7F23	D1
IO254PB7F23	E1
IO257NB7F23	F5
IO257PB7F23	E4
Dedicated I/O	
VCCDA	H7
GND	A1
GND	A11

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX1000 Function	Pin Number
GND	A12
GND	A2
GND	A21
GND	A22
GND	AA1
GND	AA2
GND	AA21
GND	AA22
GND	AB1
GND	AB11
GND	AB12
GND	AB2
GND	AB21
GND	AB22
GND	B1
GND	B2
GND	B21
GND	B22
GND	C20
GND	C3
GND	D19
GND	D4
GND	E18
GND	E5
GND	G18
GND	H15
GND	H8
GND	J14
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	L1
GND	L10
GND	L11
GND	L12
GND	L13
GND	L22
GND	M1
GND	M10
GND	M11
GND	M12
GND	M13

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX1000 Function	Pin Number
GND	M22
GND	N10
GND	N11
GND	N12
GND	N13
GND	P14
GND	P9
GND	R15
GND	R8
GND	U16
GND	U6
GND	V18
GND	V5
GND	W19
GND	W4
GND	Y20
GND	Y3
GND/LP	G7
PRA	G11
PRB	F11
PRC	T12
PRD	U12
TCK	G8
TDI	F9
TDO	F7
TMS	F6
TRST	F8
VCCA	G17
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J7
VCCA	K14
VCCA	K9
VCCA	L14
VCCA	L9
VCCA	M14
VCCA	M9
VCCA	N14
VCCA	N9
VCCA	P10
VCCA	P11
VCCA	P12

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG484	
AX1000 Function	Pin Number
VCCA	P13
VCCA	T6
VCCA	U17
VCCPLA	F10
VCCPLB	G9
VCCPLC	D13
VCCPLD	G13
VCCPLE	U13
VCCPLF	T14
VCCPLG	W10
VCCPLH	T10
VCCDA	AB16
VCCDA	AB8
VCCDA	C10
VCCDA	C11
VCCDA	C14
VCCDA	D14
VCCDA	D5
VCCDA	F16
VCCDA	G12
VCCDA	L4
VCCDA	M18
VCCDA	T11
VCCDA	T17
VCCDA	U7
VCCDA	V14
VCCDA	V8
VCCIB0	A3
VCCIB0	B3
VCCIB0	H10
VCCIB0	H11
VCCIB0	H9
VCCIB1	A20
VCCIB1	B20
VCCIB1	H12
VCCIB1	H13
VCCIB1	H14
VCCIB2	C21
VCCIB2	C22
VCCIB2	J15
VCCIB2	K15
VCCIB2	L15
VCCIB3	M15
VCCIB3	N15

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

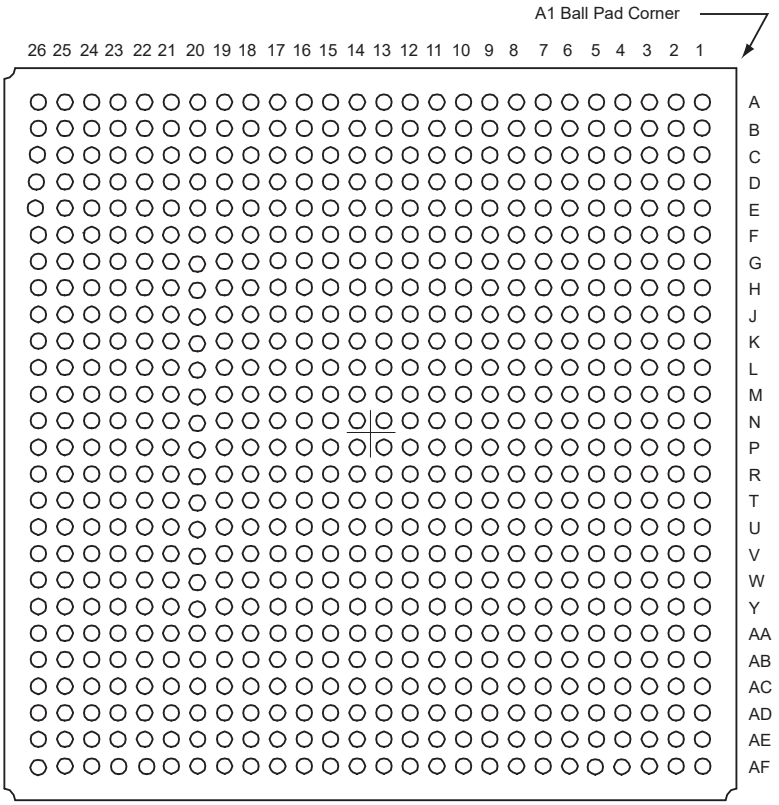
FG484	
AX1000 Function	Pin Number
VCCIB3	P15
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA20
VCCIB4	AB20
VCCIB4	R12
VCCIB4	R13
VCCIB4	R14
VCCIB5	AA3
VCCIB5	AB3
VCCIB5	R10
VCCIB5	R11
VCCIB5	R9
VCCIB6	M8
VCCIB6	N8
VCCIB6	P8
VCCIB6	Y1
VCCIB6	Y2
VCCIB7	C1
VCCIB7	C2
VCCIB7	J8
VCCIB7	K8
VCCIB7	L8
VCOMPLA	D10
VCOMPLB	G10
VCOMPLC	E12
VCOMPLD	G14
VCOMPLE	W13
VCOMPLF	T13
VCOMPLG	V11
VCOMPLH	T9
VPUMP	D17

3.5 FG676

The following figure shows package bottom-view of FG676.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 3-5. Package Bottom-View



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

The following tables list the IOD interface pin placement.

Table 3-8. Packaging Pin Assignment Table (PPAT)

FG676	
AX500 Function	Pin Number
Bank 0	
IO00NB0F0	F8
IO00PB0F0	E8
IO01NB0F0	A5
IO01PB0F0	A4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	B6
IO05PB0F0	C6
IO06NB0F0	C7
IO06PB0F0	D7
IO07NB0F0	A7
IO07PB0F0	A6

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
IO08NB0F0	C8
IO08PB0F0	D8
IO09NB0F0	F10
IO09PB0F0	F9
IO10NB0F0	B8
IO10PB0F0	B7
IO11NB0F0	D10
IO11PB0F0	E10
IO12NB0F1	B9
IO12PB0F1	C9
IO13NB0F1	F11
IO13PB0F1	G11
IO14NB0F1	D11
IO14PB0F1	E11
IO15NB0F1	B10
IO15PB0F1	C10
IO16NB0F1	A10
IO16PB0F1	A9
IO17NB0F1	F12
IO17PB0F1	G12
IO18NB0F1	C12
IO18PB0F1	C11
IO19NB0F1/HCLKAN	A12
IO19PB0F1/HCLKAP	B12
IO20NB0F1/HCLKBN	C13
IO20PB0F1/HCLKBP	B13
Bank 1	
IO21NB1F2/HCLKCN	C15
IO21PB1F2/HCLKCP	C14
IO22NB1F2/HCLKDN	A15
IO22PB1F2/HCLKDP	B15
IO23NB1F2	F15
IO23PB1F2	G15
IO24NB1F2	B16
IO24PB1F2	A16
IO25NB1F2	A18
IO25PB1F2	A17
IO26NB1F2	D16
IO26PB1F2	E16
IO27NB1F2	F16
IO27PB1F2	G16
IO28NB1F2	C18
IO28PB1F2	C17
IO29NB1F2	B19

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
IO29PB1F2	B18
IO30NB1F2	D19
IO30PB1F2	C19
IO31NB1F2	F17
IO31PB1F2	E17
IO32NB1F3	B20
IO32PB1F3	A20
IO33NB1F3	B22
IO33PB1F3	B21
IO34NB1F3	D20
IO34PB1F3	C20
IO35NB1F3	D21
IO35PB1F3	C21
IO36NB1F3	D22
IO36PB1F3	C22
IO37NB1F3	F19
IO37PB1F3	E19
IO38NB1F3	B23
IO38PB1F3	A23
IO39NB1F3	E21
IO39PB1F3	E20
IO40NB1F3	D23
IO40PB1F3	C23
IO41NB1F3	D25
IO41PB1F3	C25
Bank 2	
IO42NB2F4	G24
IO42PB2F4	G23
IO43NB2F4	G26
IO43PB2F4	F26
IO44NB2F4	F25
IO44PB2F4	E25
IO45NB2F4	J21
IO45PB2F4	J22
IO46NB2F4	H25
IO46PB2F4	G25
IO47NB2F4	K23
IO47PB2F4	J23
IO48NB2F4	J24
IO48PB2F4	H24
IO49NB2F4	K21
IO49PB2F4	K22
IO50NB2F4	K25
IO50PB2F4	J25

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
IO51NB2F4	L20
IO51PB2F4	L21
IO52NB2F5	K26
IO52PB2F5	J26
IO53NB2F5	L23
IO53PB2F5	L22
IO54NB2F5	L24
IO54PB2F5	K24
IO55NB2F5	M20
IO55PB2F5	M21
IO56NB2F5	L26
IO56PB2F5	L25
IO57NB2F5	M23
IO57PB2F5	M22
IO58NB2F5	M26
IO58PB2F5	M25
IO59NB2F5	N22
IO59PB2F5	N23
IO60NB2F5	N24
IO60PB2F5	M24
IO61NB2F5	N20
IO61PB2F5	N21
IO62NB2F5	P25
IO62PB2F5	N25
Bank 3	
IO63NB3F6	T26
IO63PB3F6	R26
IO64NB3F6	R24
IO64PB3F6	P24
IO65NB3F6	P20
IO65PB3F6	P21
IO66NB3F6	T25
IO66PB3F6	R25
IO67NB3F6	T23
IO67PB3F6	R23
IO68NB3F6	V26
IO68PB3F6	U26
IO69NB3F6	V25
IO69PB3F6	U25
IO70NB3F6	Y25
IO70PB3F6	W25
IO71NB3F6	W24
IO71PB3F6	V24
IO72NB3F6	V23

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
IO72PB3F6	U23
IO73NB3F6	T21
IO73PB3F6	T20
IO74NB3F7	AA26
IO74PB3F7	Y26
IO75NB3F7	AA24
IO75PB3F7	Y24
IO76NB3F7	Y23
IO76PB3F7	W23
IO77NB3F7	V21
IO77PB3F7	U21
IO78NB3F7	AB25
IO78PB3F7	AA25
IO79NB3F7	AC26
IO79PB3F7	AB26
IO80NB3F7	AC24
IO80PB3F7	AB24
IO81NB3F7	AB23
IO81PB3F7	AA23
IO82NB3F7	AA22
IO82PB3F7	Y22
IO83NB3F7	AE26
IO83PB3F7	AD26
Bank 4	
IO84NB4F8	AB21
IO84PB4F8	AA21
IO85NB4F8	AE23
IO85PB4F8	AE24
IO86NB4F8	AC21
IO86PB4F8	AC22
IO87NB4F8	AF22
IO87PB4F8	AF23
IO88NB4F8	AD22
IO88PB4F8	AD23
IO89NB4F8	AC19
IO89PB4F8	AC20
IO90NB4F8	AE21
IO90PB4F8	AE22
IO91NB4F8	AA17
IO91PB4F8	AA18
IO92NB4F8	AD20
IO92PB4F8	AD21
IO93NB4F8	AF20
IO93PB4F8	AF21

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
IO94NB4F9	AE19
IO94PB4F9	AE20
IO95NB4F9	AC17
IO95PB4F9	AC18
IO96NB4F9	AD18
IO96PB4F9	AD19
IO97NB4F9	AA16
IO97PB4F9	Y16
IO98NB4F9	AE17
IO98PB4F9	AE18
IO99NB4F9	AC16
IO99PB4F9	AB16
IO100NB4F9	AF17
IO100PB4F9	AF18
IO101NB4F9	AA15
IO101PB4F9	Y15
IO102NB4F9	AC15
IO102PB4F9	AB15
IO103NB4F9/CLKEN	AE16
IO103PB4F9/CLKEP	AF16
IO104NB4F9/CLKFN	AE14
IO104PB4F9/CLKFP	AE15
Bank 5	
IO105NB5F10/CLKGN	AE12
IO105PB5F10/CLKGP	AE13
IO106NB5F10/CLKHN	AE11
IO106PB5F10/CLKHP	AF11
IO107NB5F10	Y12
IO107PB5F10	AA13
IO108NB5F10	AC12
IO108PB5F10	AB12
IO109NB5F10	AC10
IO109PB5F10	AC11
IO110NB5F10	AF9
IO110PB5F10	AF10
IO111NB5F10	Y11
IO111PB5F10	AA12
IO112NB5F10	AE9
IO112PB5F10	AE10
IO113NB5F10	AC9
IO113PB5F10	AD9
IO114NB5F11	AF6
IO114PB5F11	AF7
IO115NB5F11	AA10

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
IO115PB5F11	AB10
IO116NB5F11	AE7
IO116PB5F11	AE8
IO117NB5F11	AD7
IO117PB5F11	AD8
IO118NB5F11	AC7
IO118PB5F11	AC8
IO119NB5F11	AD6
IO119PB5F11	AE6
IO120NB5F11	AE5
IO120PB5F11	AF5
IO121NB5F11	AF4
IO121PB5F11	AE4
IO122NB5F11	AC5
IO122PB5F11	AC6
IO123NB5F11	AD4
IO123PB5F11	AD5
IO124NB5F11	AB6
IO124PB5F11	AB7
IO125NB5F11	AE3
IO125PB5F11	AF3
Bank 6	
IO126NB6F12	AB3
IO126PB6F12	AC3
IO127NB6F12	AA2
IO127PB6F12	AB2
IO128NB6F12	AC2
IO128PB6F12	AD2
IO129NB6F12	Y1
IO129PB6F12	AA1
IO130NB6F12	Y3
IO130PB6F12	AA3
IO131NB6F12	U6
IO131PB6F12	V6
IO132NB6F12	W2
IO132PB6F12	Y2
IO133NB6F12	V4
IO133PB6F12	W4
IO134NB6F12	V3
IO134PB6F12	W3
IO135NB6F12	V1
IO135PB6F12	V2
IO136NB6F13	U4
IO136PB6F13	U5

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
IO137NB6F13	T6
IO137PB6F13	T7
IO138NB6F13	T5
IO138PB6F13	T4
IO139NB6F13	R6
IO139PB6F13	R7
IO140NB6F13	T3
IO140PB6F13	U3
IO141NB6F13	U1
IO141PB6F13	U2
IO142NB6F13	R2
IO142PB6F13	T2
IO143NB6F13	P3
IO143PB6F13	R3
IO144NB6F13	P5
IO144PB6F13	P4
IO145NB6F13	P6
IO145PB6F13	P7
IO146NB6F13	R1
IO146PB6F13	T1
Bank 7	
IO147NB7F14	N6
IO147PB7F14	N7
IO148NB7F14	N5
IO148PB7F14	N4
IO149NB7F14	N2
IO149PB7F14	N3
IO150NB7F14	L1
IO150PB7F14	M1
IO151NB7F14	M2
IO151PB7F14	M3
IO152NB7F14	M5
IO152PB7F14	M4
IO153NB7F14	M7
IO153PB7F14	M6
IO154NB7F14	K2
IO154PB7F14	L2
IO155NB7F14	K3
IO155PB7F14	L3
IO156NB7F14	L5
IO156PB7F14	L4
IO157NB7F14	L6
IO157PB7F14	L7
IO158NB7F15	J1

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
IO158PB7F15	K1
IO159NB7F15	J4
IO159PB7F15	K4
IO160NB7F15	H2
IO160PB7F15	J2
IO161NB7F15	K6
IO161PB7F15	K5
IO162NB7F15	H3
IO162PB7F15	J3
IO163NB7F15	G2
IO163PB7F15	G1
IO164NB7F15	G4
IO164PB7F15	H4
IO165NB7F15	F3
IO165PB7F15	G3
IO166NB7F15	E2
IO166PB7F15	F2
IO167NB7F15	F5
IO167PB7F15	G5
Dedicated I/O	
GND	A1
GND	A13
GND	A14
GND	A19
GND	A26
GND	A8
GND	AC23
GND	AC4
GND	AD24
GND	AD3
GND	AE2
GND	AE25
GND	AF1
GND	AF13
GND	AF14
GND	AF19
GND	AF26
GND	AF8
GND	B2
GND	B25
GND	B26
GND	C24
GND	C3
GND	G20

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
GND	G7
GND	H1
GND	H19
GND	H26
GND	H8
GND	J18
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	K14
GND	K15
GND	K16
GND	K17
GND	L10
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	L16
GND	L17
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N1
GND	N10
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N26
GND	P1
GND	P10
GND	P11

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P26
GND	R10
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	V18
GND	V9
GND	W1
GND	W19
GND	W26
GND	W8
GND	Y20
GND	Y7
GND/LP	C2
NC	A11
NC	A21
NC	A22
NC	A24

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
NC	A25
NC	AA11
NC	AA19
NC	AA20
NC	AA4
NC	AA5
NC	AA6
NC	AA7
NC	AA8
NC	AA9
NC	AB1
NC	AB11
NC	AB17
NC	AB18
NC	AB19
NC	AB20
NC	AB8
NC	AB9
NC	AC1
NC	AC13
NC	AC14
NC	AC25
NC	AD1
NC	AD11
NC	AD16
NC	AD25
NC	AE1
NC	AF2
NC	AF25
NC	B11
NC	B24
NC	B4
NC	C16
NC	C4
NC	D1
NC	D13
NC	D14
NC	D17
NC	D18
NC	D2
NC	D26
NC	D3
NC	D9
NC	E1

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
NC	E18
NC	E23
NC	E24
NC	E26
NC	E3
NC	E4
NC	E9
NC	F1
NC	F18
NC	F20
NC	F21
NC	F22
NC	F23
NC	F24
NC	F4
NC	F6
NC	F7
NC	G21
NC	G22
NC	H21
NC	H22
NC	H23
NC	H5
NC	H6
NC	J5
NC	J6
NC	P22
NC	R20
NC	R21
NC	R22
NC	R4
NC	R5
NC	T22
NC	T24
NC	U22
NC	U24
NC	V22
NC	V5
NC	W21
NC	W22
NC	W5
NC	W6
NC	Y21
NC	Y4

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
NC	Y5
NC	Y6
PRA	E13
PRB	B14
PRC	Y14
PRD	AD14
TCK	E5
TDI	B3
TDO	G6
TMS	D4
TRST	A2
VCCA	AB4
VCCA	AF24
VCCA	C1
VCCA	C26
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J14
VCCA	J15
VCCA	J16
VCCA	J17
VCCA	K18
VCCA	K9
VCCA	L18
VCCA	L9
VCCA	M18
VCCA	M9
VCCA	N18
VCCA	N9
VCCA	P18
VCCA	P9
VCCA	R18
VCCA	R9
VCCA	T18
VCCA	T9
VCCA	U18
VCCA	U9
VCCA	V10
VCCA	V11
VCCA	V12
VCCA	V13
VCCA	V14

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
VCCA	V15
VCCA	V16
VCCA	V17
VCCDA	A3
VCCDA	AB22
VCCDA	AB5
VCCDA	AD10
VCCDA	AD13
VCCDA	AD17
VCCDA	B1
VCCDA	B17
VCCDA	D24
VCCDA	E14
VCCDA	P2
VCCDA	P23
VCCIB0	G10
VCCIB0	G8
VCCIB0	G9
VCCIB0	H10
VCCIB0	H11
VCCIB0	H12
VCCIB0	H13
VCCIB0	H9
VCCIB1	G17
VCCIB1	G18
VCCIB1	G19
VCCIB1	H14
VCCIB1	H15
VCCIB1	H16
VCCIB1	H17
VCCIB1	H18
VCCIB2	H20
VCCIB2	J19
VCCIB2	J20
VCCIB2	K19
VCCIB2	K20
VCCIB2	L19
VCCIB2	M19
VCCIB2	N19
VCCIB3	P19
VCCIB3	R19
VCCIB3	T19
VCCIB3	U19
VCCIB3	U20

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
VCCIB3	V19
VCCIB3	V20
VCCIB3	W20
VCCIB4	W14
VCCIB4	W15
VCCIB4	W16
VCCIB4	W17
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCCPLA	E12
VCCPLB	F13
VCCPLC	E15
VCCPLD	G14
VCCPLE	AF15
VCCPLF	AA14
VCCPLG	AF12
VCCPLH	AB13
VCOMPLA	D12

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX500 Function	Pin Number
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12
VCOMPLH	Y13
VPUMP	E22

Table 3-9. Packaging Pin Assignment Table (PPAT)

FG676	
AX1000 Function	Pin Number
Bank 0	
IO00NB0F0	B4
IO00PB0F0	C4
IO02NB0F0	E7
IO02PB0F0	E6
IO03NB0F0	D6
IO03PB0F0	D5
IO04NB0F0	B5
IO04PB0F0	C5
IO05NB0F0	A5
IO05PB0F0	A4
IO06NB0F0	F7
IO06PB0F0	F6
IO07NB0F0	B6
IO07PB0F0	C6
IO08NB0F0	C7
IO08PB0F0	D7
IO10NB0F0	F8
IO10PB0F0	E8
IO11NB0F0	A7
IO11PB0F0	A6
IO12NB0F1	C8
IO12PB0F1	D8
IO13NB0F1	B8
IO13PB0F1	B7
IO14NB0F1	D9
IO14PB0F1	E9
IO16NB0F1	F10
IO16PB0F1	F9
IO18NB0F1	B9
IO18PB0F1	C9
IO19NB0F1	A10

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX1000 Function	Pin Number
IO19PB0F1	A9
IO20NB0F1	D10
IO20PB0F1	E10
IO21NB0F1	B10
IO21PB0F1	C10
IO22NB0F2	F11
IO22PB0F2	G11
IO24NB0F2	D11
IO24PB0F2	E11
IO26NB0F2	C12
IO26PB0F2	C11
IO28NB0F2	F12
IO28PB0F2	G12
IO30NB0F2/HCLKAN	A12
IO30PB0F2/HCLKAP	B12
IO31NB0F2/HCLKBN	C13
IO31PB0F2/HCLKBP	B13
Bank 1	
IO32NB1F3/HCLKCN	C15
IO32PB1F3/HCLKCP	C14
IO33NB1F3/HCLKDN	A15
IO33PB1F3/HCLKDP	B15
IO35NB1F3	B16
IO35PB1F3	A16
IO36NB1F3	F15
IO36PB1F3	G15
IO38NB1F3	F16
IO38PB1F3	G16
IO40NB1F3	A18
IO40PB1F3	A17
IO41NB1F4	C18
IO41PB1F4	C17
IO42NB1F4	D16
IO42PB1F4	E16
IO44NB1F4	D18
IO44PB1F4	D17
IO45NB1F4	B19
IO45PB1F4	B18
IO46NB1F4	B20
IO46PB1F4	A20
IO48NB1F4	F17
IO48PB1F4	E17
IO49NB1F4	A22
IO49PB1F4	A21

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX1000 Function	Pin Number
IO50NB1F4	E18
IO50PB1F4	F18
IO51NB1F4	D19
IO51PB1F4	C19
IO52NB1F4	D20
IO52PB1F4	C20
IO54NB1F5	B22
IO54PB1F5	B21
IO55NB1F5	D21
IO55PB1F5	C21
IO56NB1F5	F19
IO56PB1F5	E19
IO57NB1F5	B23
IO57PB1F5	A23
IO58NB1F5	D22
IO58PB1F5	C22
IO59NB1F5	B24
IO59PB1F5	A24
IO60NB1F5	E21
IO60PB1F5	E20
IO62NB1F5	D23
IO62PB1F5	C23
IO63NB1F5	F21
IO63PB1F5	F20
Bank 2	
IO64NB2F6	H21
IO64PB2F6	G21
IO65NB2F6	G22
IO65PB2F6	F22
IO66NB2F6	F24
IO66PB2F6	F23
IO67NB2F6	E24
IO67PB2F6	E23
IO68NB2F6	H23
IO68PB2F6	H22
IO69NB2F6	D25
IO69PB2F6	C25
IO70NB2F6	G24
IO70PB2F6	G23
IO71NB2F6	F25
IO71PB2F6	E25
IO72NB2F6	G26
IO72PB2F6	F26
IO73NB2F6	E26

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX1000 Function	Pin Number
IO73PB2F6	D26
IO74NB2F7	J21
IO74PB2F7	J22
IO75NB2F7	J24
IO75PB2F7	H24
IO76NB2F7	K23
IO76PB2F7	J23
IO77NB2F7	H25
IO77PB2F7	G25
IO78NB2F7	K25
IO78PB2F7	J25
IO80NB2F7	K21
IO80PB2F7	K22
IO81NB2F7	K26
IO81PB2F7	J26
IO82NB2F7	L24
IO82PB2F7	K24
IO83NB2F7	L23
IO83PB2F7	L22
IO84NB2F7	L20
IO84PB2F7	L21
IO86NB2F8	L26
IO86PB2F8	L25
IO88NB2F8	M23
IO88PB2F8	M22
IO89NB2F8	M26
IO89PB2F8	M25
IO90NB2F8	M20
IO90PB2F8	M21
IO91NB2F8	N24
IO91PB2F8	M24
IO92NB2F8	N22
IO92PB2F8	N23
IO94NB2F8	N20
IO94PB2F8	N21
IO95NB2F8	P25
IO95PB2F8	N25
Bank 3	
IO98NB3F9	P20
IO98PB3F9	P21
IO99NB3F9	R24
IO99PB3F9	P24
IO100NB3F9	R22
IO100PB3F9	P22

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX1000 Function	Pin Number
IO101NB3F9	T26
IO101PB3F9	R26
IO102NB3F9	R21
IO102PB3F9	R20
IO103NB3F9	T25
IO103PB3F9	R25
IO105NB3F9	V26
IO105PB3F9	U26
IO106NB3F9	T23
IO106PB3F9	R23
IO107NB3F10	U24
IO107PB3F10	T24
IO108NB3F10	U22
IO108PB3F10	T22
IO109NB3F10	V25
IO109PB3F10	U25
IO110NB3F10	T21
IO110PB3F10	T20
IO112NB3F10	V23
IO112PB3F10	U23
IO113NB3F10	Y25
IO113PB3F10	W25
IO114NB3F10	V21
IO114PB3F10	U21
IO115NB3F10	W24
IO115PB3F10	V24
IO116NB3F10	AA26
IO116PB3F10	Y26
IO118NB3F11	AC26
IO118PB3F11	AB26
IO119NB3F11	AB25
IO119PB3F11	AA25
IO120NB3F11	W22
IO120PB3F11	V22
IO121NB3F11	Y23
IO121PB3F11	W23
IO122NB3F11	AA24
IO122PB3F11	Y24
IO123NB3F11	AE26
IO123PB3F11	AD26
IO124NB3F11	Y21
IO124PB3F11	W21
IO125NB3F11	AD25
IO125PB3F11	AC25

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX1000 Function	Pin Number
IO126NB3F11	AB23
IO126PB3F11	AA23
IO127NB3F11	AC24
IO127PB3F11	AB24
IO128NB3F11	AA22
IO128PB3F11	Y22
Bank 4	
IO129NB4F12	AB21
IO129PB4F12	AA21
IO131NB4F12	AD22
IO131PB4F12	AD23
IO132NB4F12	AE23
IO132PB4F12	AE24
IO133NB4F12	AB20
IO133PB4F12	AA20
IO134NB4F12	AC21
IO134PB4F12	AC22
IO135NB4F12	AF22
IO135PB4F12	AF23
IO137NB4F12	AB19
IO137PB4F12	AA19
IO139NB4F13	AC19
IO139PB4F13	AC20
IO140NB4F13	AE21
IO140PB4F13	AE22
IO141NB4F13	AD20
IO141PB4F13	AD21
IO143NB4F13	AB17
IO143PB4F13	AB18
IO144NB4F13	AE19
IO144PB4F13	AE20
IO145NB4F13	AC17
IO145PB4F13	AC18
IO146NB4F13	AD18
IO146PB4F13	AD19
IO147NB4F13	AA17
IO147PB4F13	AA18
IO148NB4F13	AF20
IO148PB4F13	AF21
IO149NB4F13	AA16
IO149PB4F13	Y16
IO151NB4F13	AC16
IO151PB4F13	AB16
IO153NB4F14	AE17

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX1000 Function	Pin Number
IO153PB4F14	AE18
IO154NB4F14	AF17
IO154PB4F14	AF18
IO155NB4F14	AA15
IO155PB4F14	Y15
IO157NB4F14	AC15
IO157PB4F14	AB15
IO159NB4F14/CLKEN	AE16
IO159PB4F14/CLKEP	AF16
IO160NB4F14/CLKFN	AE14
IO160PB4F14/CLKFP	AE15
Bank 5	
IO161NB5F15/CLKGN	AE12
IO161PB5F15/CLKGP	AE13
IO162NB5F15/CLKHN	AE11
IO162PB5F15/CLKHP	AF11
IO163NB5F15	AC12
IO163PB5F15	AB12
IO165NB5F15	Y12
IO165PB5F15	AA13
IO167NB5F15	Y11
IO167PB5F15	AA12
IO168NB5F15	AF9
IO168PB5F15	AF10
IO169NB5F15	AB11
IO169PB5F15	AA11
IO171NB5F16	AE9
IO171PB5F16	AE10
IO173NB5F16	AC10
IO173PB5F16	AC11
IO174NB5F16	AE7
IO174PB5F16	AE8
IO175NB5F16	AC9
IO175PB5F16	AD9
IO176NB5F16	AF6
IO176PB5F16	AF7
IO177NB5F16	AA10
IO177PB5F16	AB10
IO179NB5F16	AD7
IO179PB5F16	AD8
IO180NB5F16	AC7
IO180PB5F16	AC8
IO181NB5F17	AA9
IO181PB5F17	AB9

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX1000 Function	Pin Number
IO183NB5F17	AD6
IO183PB5F17	AE6
IO184NB5F17	AE5
IO184PB5F17	AF5
IO185NB5F17	AA8
IO185PB5F17	AB8
IO187NB5F17	AC5
IO187PB5F17	AC6
IO188NB5F17	AD4
IO188PB5F17	AD5
IO189NB5F17	AB6
IO189PB5F17	AB7
IO190NB5F17	AF4
IO190PB5F17	AE4
IO191NB5F17	AE3
IO191PB5F17	AF3
IO192NB5F17	AA6
IO192PB5F17	AA7
Bank 6	
IO193NB6F18	Y5
IO193PB6F18	AA5
IO194NB6F18	AB3
IO194PB6F18	AC3
IO195NB6F18	Y4
IO195PB6F18	AA4
IO196NB6F18	AC2
IO196PB6F18	AD2
IO197NB6F18	W6
IO197PB6F18	Y6
IO198NB6F18	AD1
IO198PB6F18	AE1
IO199NB6F18	AA2
IO199PB6F18	AB2
IO200NB6F18	Y3
IO200PB6F18	AA3
IO201NB6F18	V5
IO201PB6F18	W5
IO202NB6F18	AB1
IO202PB6F18	AC1
IO203NB6F19	V4
IO203PB6F19	W4
IO204NB6F19	V3
IO204PB6F19	W3
IO205NB6F19	U6

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX1000 Function	Pin Number
IO205PB6F19	V6
IO206NB6F19	W2
IO206PB6F19	Y2
IO207NB6F19	U4
IO207PB6F19	U5
IO208NB6F19	Y1
IO208PB6F19	AA1
IO209NB6F19	T6
IO209PB6F19	T7
IO211NB6F19	T3
IO211PB6F19	U3
IO212NB6F19	V1
IO212PB6F19	V2
IO213NB6F19	T5
IO213PB6F19	T4
IO214NB6F20	U1
IO214PB6F20	U2
IO215NB6F20	R6
IO215PB6F20	R7
IO217NB6F20	R5
IO217PB6F20	R4
IO218NB6F20	R2
IO218PB6F20	T2
IO219NB6F20	P3
IO219PB6F20	R3
IO220NB6F20	R1
IO220PB6F20	T1
IO221NB6F20	P6
IO221PB6F20	P7
IO223NB6F20	P5
IO223PB6F20	P4
Bank 7	
IO225NB7F21	N5
IO225PB7F21	N4
IO226NB7F21	N2
IO226PB7F21	N3
IO227NB7F21	N6
IO227PB7F21	N7
IO229NB7F21	M7
IO229PB7F21	M6
IO231NB7F21	M5
IO231PB7F21	M4
IO232NB7F21	L1
IO232PB7F21	M1

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX1000 Function	Pin Number
IO233NB7F21	M2
IO233PB7F21	M3
IO235NB7F21	K2
IO235PB7F21	L2
IO236NB7F22	L5
IO236PB7F22	L4
IO237NB7F22	L6
IO237PB7F22	L7
IO238NB7F22	K3
IO238PB7F22	L3
IO240NB7F22	J1
IO240PB7F22	K1
IO241NB7F22	K6
IO241PB7F22	K5
IO242NB7F22	H2
IO242PB7F22	J2
IO243NB7F22	J4
IO243PB7F22	K4
IO244NB7F22	H3
IO244PB7F22	J3
IO245NB7F22	G2
IO245PB7F22	G1
IO247NB7F23	J6
IO247PB7F23	J5
IO248NB7F23	E1
IO248PB7F23	F1
IO249NB7F23	E2
IO249PB7F23	F2
IO250NB7F23	G4
IO250PB7F23	H4
IO251NB7F23	F3
IO251PB7F23	G3
IO253NB7F23	H6
IO253PB7F23	H5
IO254NB7F23	D2
IO254PB7F23	D1
IO255NB7F23	E4
IO255PB7F23	F4
IO256NB7F23	D3
IO256PB7F23	E3
IO257NB7F23	F5
IO257PB7F23	G5
Dedicated I/O	
GND	A1

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX1000 Function	Pin Number
GND	A13
GND	A14
GND	A19
GND	A26
GND	A8
GND	AC23
GND	AC4
GND	AD24
GND	AD3
GND	AE2
GND	AE25
GND	AF1
GND	AF13
GND	AF14
GND	AF19
GND	AF26
GND	AF8
GND	B2
GND	B25
GND	B26
GND	C24
GND	C3
GND	G20
GND	G7
GND	H1
GND	H19
GND	H26
GND	H8
GND	J18
GND	J9
GND	K10
GND	K11
GND	K12
GND	K13
GND	K14
GND	K15
GND	K16
GND	K17
GND	L10
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX1000 Function	Pin Number
GND	L16
GND	L17
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	N1
GND	N10
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N26
GND	P1
GND	P10
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P26
GND	R10
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	T10
GND	T11
GND	T12
GND	T13
GND	T14
GND	T15

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX1000 Function	Pin Number
GND	T16
GND	T17
GND	U10
GND	U11
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	V18
GND	V9
GND	W1
GND	W19
GND	W26
GND	W8
GND	Y20
GND	Y7
GND/LP	C2
NC	A25
NC	AC13
NC	AC14
NC	AF2
NC	AF25
NC	D13
NC	D14
PRA	E13
PRB	B14
PRC	Y14
PRD	AD14
TCK	E5
TDI	B3
TDO	G6
TMS	D4
TRST	A2
VCCA	AB4
VCCA	AF24
VCCA	C1
VCCA	C26
VCCA	J10
VCCA	J11
VCCA	J12
VCCA	J13
VCCA	J14

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX1000 Function	Pin Number
VCCA	J15
VCCA	J16
VCCA	J17
VCCA	K18
VCCA	K9
VCCA	L18
VCCA	L9
VCCA	M18
VCCA	M9
VCCA	N18
VCCA	N9
VCCA	P18
VCCA	P9
VCCA	R18
VCCA	R9
VCCA	T18
VCCA	T9
VCCA	U18
VCCA	U9
VCCA	V10
VCCA	V11
VCCA	V12
VCCA	V13
VCCA	V14
VCCA	V15
VCCA	V16
VCCA	V17
VCCPLA	E12
VCCPLB	F13
VCCPLC	E15
VCCPLD	G14
VCCPLE	AF15
VCCPLF	AA14
VCCPLG	AF12
VCCPLH	AB13
VCCDA	A11
VCCDA	A3
VCCDA	AB22
VCCDA	AB5
VCCDA	AD10
VCCDA	AD11
VCCDA	AD13
VCCDA	AD16
VCCDA	AD17

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG676	
AX1000 Function	Pin Number
VCCDA	B1
VCCDA	B11
VCCDA	B17
VCCDA	C16
VCCDA	D24
VCCDA	E14
VCCDA	P2
VCCDA	P23
VCCIB0	G10
VCCIB0	G8
VCCIB0	G9
VCCIB0	H10
VCCIB0	H11
VCCIB0	H12
VCCIB0	H13
VCCIB0	H9
VCCIB1	G17
VCCIB1	G18
VCCIB1	G19
VCCIB1	H14
VCCIB1	H15
VCCIB1	H16
VCCIB1	H17
VCCIB1	H18
VCCIB2	H20
VCCIB2	J19
VCCIB2	J20
VCCIB2	K19
VCCIB2	K20
VCCIB2	L19
VCCIB2	M19
VCCIB2	N19
VCCIB3	P19
VCCIB3	R19
VCCIB3	T19
VCCIB3	U19
VCCIB3	U20
VCCIB3	V19
VCCIB3	V20
VCCIB3	W20
VCCIB4	W14
VCCIB4	W15
VCCIB4	W16
VCCIB4	W17

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

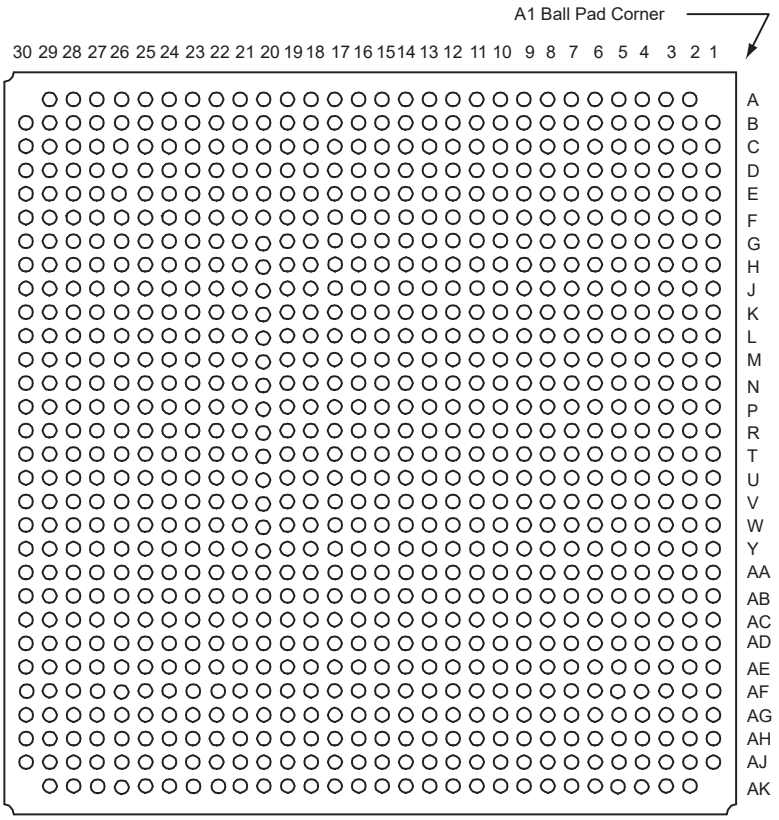
FG676	
AX1000 Function	Pin Number
VCCIB4	W18
VCCIB4	Y17
VCCIB4	Y18
VCCIB4	Y19
VCCIB5	W10
VCCIB5	W11
VCCIB5	W12
VCCIB5	W13
VCCIB5	W9
VCCIB5	Y10
VCCIB5	Y8
VCCIB5	Y9
VCCIB6	P8
VCCIB6	R8
VCCIB6	T8
VCCIB6	U7
VCCIB6	U8
VCCIB6	V7
VCCIB6	V8
VCCIB6	W7
VCCIB7	H7
VCCIB7	J7
VCCIB7	J8
VCCIB7	K7
VCCIB7	K8
VCCIB7	L8
VCCIB7	M8
VCCIB7	N8
VCOMPLA	D12
VCOMPLB	G13
VCOMPLC	D15
VCOMPLD	F14
VCOMPLE	AD15
VCOMPLF	AB14
VCOMPLG	AD12
VCOMPLH	Y13
VPUMP	E22

3.6 FG896

The following figure shows package bottom-view of FG896.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 3-6. Package Bottom-View



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

The following tables list the IOD interface pin placement.

Table 3-10. Packaging Pin Assignment Table (PPAT)

FG896	
AX1000 Function	Pin Number
Bank 0	
IO00NB0F0	D6
IO00PB0F0	E6
IO01NB0F0	A5
IO01PB0F0	B5
IO02NB0F0	G9
IO02PB0F0	G8
IO03NB0F0	F8
IO03PB0F0	F7
IO04NB0F0	D7
IO04PB0F0	E7
IO05NB0F0	C7
IO05PB0F0	C6
IO06NB0F0	H9
IO06PB0F0	H8
IO07NB0F0	D8

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
IO07PB0F0	E8
IO08NB0F0	E9
IO08PB0F0	F9
IO09NB0F0	A7
IO09PB0F0	B7
IO10NB0F0	H10
IO10PB0F0	G10
IO11NB0F0	C9
IO11PB0F0	C8
IO12NB0F1	E10
IO12PB0F1	F10
IO13NB0F1	D10
IO13PB0F1	D9
IO14NB0F1	F11
IO14PB0F1	G11
IO15NB0F1	A10
IO15PB0F1	A9
IO16NB0F1	H12
IO16PB0F1	H11
IO17NB0F1	B11
IO17PB0F1	B10
IO18NB0F1	D11
IO18PB0F1	E11
IO19NB0F1	C12
IO19PB0F1	C11
IO20NB0F1	F12
IO20PB0F1	G12
IO21NB0F1	D12
IO21PB0F1	E12
IO22NB0F2	H13
IO22PB0F2	J13
IO23NB0F2	A12
IO23PB0F2	A11
IO24NB0F2	F13
IO24PB0F2	G13
IO25NB0F2	B13
IO25PB0F2	B12
IO26NB0F2	E14
IO26PB0F2	E13
IO27NB0F2	B14
IO27PB0F2	A14
IO28NB0F2	H14
IO28PB0F2	J14
IO29NB0F2	B15

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
IO29PB0F2	A15
IO30NB0F2/HCLKAN	C14
IO30PB0F2/HCLKAP	D14
IO31NB0F2/HCLKBN	E15
IO31PB0F2/HCLKBP	D15
Bank 1	
IO32NB1F3/HCLKCN	E17
IO32PB1F3/HCLKCP	E16
IO33NB1F3/HCLKDN	C17
IO33PB1F3/HCLKDP	D17
IO34NB1F3	A17
IO34PB1F3	B17
IO35NB1F3	D18
IO35PB1F3	C18
IO36NB1F3	H17
IO36PB1F3	J17
IO37NB1F3	B19
IO37PB1F3	A19
IO38NB1F3	H18
IO38PB1F3	J18
IO39NB1F3	B20
IO39PB1F3	A20
IO40NB1F3	C20
IO40PB1F3	C19
IO41NB1F4	E20
IO41PB1F4	E19
IO42NB1F4	F18
IO42PB1F4	G18
IO43NB1F4	A22
IO43PB1F4	A21
IO44NB1F4	F20
IO44PB1F4	F19
IO45NB1F4	D21
IO45PB1F4	D20
IO46NB1F4	D22
IO46PB1F4	C22
IO47NB1F4	A25
IO47PB1F4	A24
IO48NB1F4	H19
IO48PB1F4	G19
IO49NB1F4	C24
IO49PB1F4	C23
IO50NB1F4	G20
IO50PB1F4	H20

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
IO51NB1F4	F21
IO51PB1F4	E21
IO52NB1F4	F22
IO52PB1F4	E22
IO53NB1F4	B25
IO53PB1F4	B24
IO54NB1F5	D24
IO54PB1F5	D23
IO55NB1F5	F23
IO55PB1F5	E23
IO56NB1F5	H21
IO56PB1F5	G21
IO57NB1F5	D25
IO57PB1F5	C25
IO58NB1F5	F24
IO58PB1F5	E24
IO59NB1F5	D26
IO59PB1F5	C26
IO60NB1F5	G23
IO60PB1F5	G22
IO61NB1F5	B27
IO61PB1F5	A27
IO62NB1F5	F25
IO62PB1F5	E25
IO63NB1F5	H23
IO63PB1F5	H22
Bank 2	
IO64NB2F6	K23
IO64PB2F6	J23
IO65NB2F6	J24
IO65PB2F6	H24
IO66NB2F6	H26
IO66PB2F6	H25
IO67NB2F6	G26
IO67PB2F6	G25
IO68NB2F6	K25
IO68PB2F6	K24
IO69NB2F6	F27
IO69PB2F6	E27
IO70NB2F6	J26
IO70PB2F6	J25
IO71NB2F6	H27
IO71PB2F6	G27
IO72NB2F6	J28

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
IO72PB2F6	H28
IO73NB2F6	G28
IO73PB2F6	F28
IO74NB2F7	L23
IO74PB2F7	L24
IO75NB2F7	L26
IO75PB2F7	K26
IO76NB2F7	M25
IO76PB2F7	L25
IO77NB2F7	K27
IO77PB2F7	J27
IO78NB2F7	M27
IO78PB2F7	L27
IO79NB2F7	K30
IO79PB2F7	K29
IO80NB2F7	M23
IO80PB2F7	M24
IO81NB2F7	M28
IO81PB2F7	L28
IO82NB2F7	N26
IO82PB2F7	M26
IO83NB2F7	N25
IO83PB2F7	N24
IO84NB2F7	N22
IO84PB2F7	N23
IO85NB2F8	M29
IO85PB2F8	L29
IO86NB2F8	N28
IO86PB2F8	N27
IO87NB2F8	P29
IO87PB2F8	P30
IO88NB2F8	P25
IO88PB2F8	P24
IO89NB2F8	P28
IO89PB2F8	P27
IO90NB2F8	P22
IO90PB2F8	P23
IO91NB2F8	R26
IO91PB2F8	P26
IO92NB2F8	R24
IO92PB2F8	R25
IO93NB2F8	R29
IO93PB2F8	R30
IO94NB2F8	R22

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
IO94PB2F8	R23
IO95NB2F8	T27
IO95PB2F8	R27
Bank 3	
IO96NB3F9	T29
IO96PB3F9	T30
IO97NB3F9	U29
IO97PB3F9	U30
IO98NB3F9	T22
IO98PB3F9	T23
IO99NB3F9	U26
IO99PB3F9	T26
IO100NB3F9	U24
IO100PB3F9	T24
IO101NB3F9	V28
IO101PB3F9	U28
IO102NB3F9	U23
IO102PB3F9	U22
IO103NB3F9	V27
IO103PB3F9	U27
IO104NB3F9	W29
IO104PB3F9	V29
IO105NB3F9	Y28
IO105PB3F9	W28
IO106NB3F9	V25
IO106PB3F9	U25
IO107NB3F10	W26
IO107PB3F10	V26
IO108NB3F10	W24
IO108PB3F10	V24
IO109NB3F10	Y27
IO109PB3F10	W27
IO110NB3F10	V23
IO110PB3F10	V22
IO111NB3F10	AA29
IO111PB3F10	Y29
IO112NB3F10	Y25
IO112PB3F10	W25
IO113NB3F10	AB27
IO113PB3F10	AA27
IO114NB3F10	Y23
IO114PB3F10	W23
IO115NB3F10	AA26
IO115PB3F10	Y26

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
IO116NB3F10	AC28
IO116PB3F10	AB28
IO117NB3F10	AE29
IO117PB3F10	AD29
IO118NB3F11	AE28
IO118PB3F11	AD28
IO119NB3F11	AD27
IO119PB3F11	AC27
IO120NB3F11	AA24
IO120PB3F11	Y24
IO121NB3F11	AB25
IO121PB3F11	AA25
IO122NB3F11	AC26
IO122PB3F11	AB26
IO123NB3F11	AG28
IO123PB3F11	AF28
IO124NB3F11	AB23
IO124PB3F11	AA23
IO125NB3F11	AF27
IO125PB3F11	AE27
IO126NB3F11	AD25
IO126PB3F11	AC25
IO127NB3F11	AE26
IO127PB3F11	AD26
IO128NB3F11	AC24
IO128PB3F11	AB24
Bank 4	
IO129NB4F12	AD23
IO129PB4F12	AC23
IO130NB4F12	AK26
IO130PB4F12	AK27
IO131NB4F12	AF24
IO131PB4F12	AF25
IO132NB4F12	AG25
IO132PB4F12	AG26
IO133NB4F12	AD22
IO133PB4F12	AC22
IO134NB4F12	AE23
IO134PB4F12	AE24
IO135NB4F12	AH24
IO135PB4F12	AH25
IO136NB4F12	AJ25
IO136PB4F12	AJ26
IO137NB4F12	AD21

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
IO137PB4F12	AC21
IO138NB4F12	AK24
IO138PB4F12	AK25
IO139NB4F13	AE21
IO139PB4F13	AE22
IO140NB4F13	AG23
IO140PB4F13	AG24
IO141NB4F13	AF22
IO141PB4F13	AF23
IO142NB4F13	AJ23
IO142PB4F13	AJ24
IO143NB4F13	AD19
IO143PB4F13	AD20
IO144NB4F13	AG21
IO144PB4F13	AG22
IO145NB4F13	AE19
IO145PB4F13	AE20
IO146NB4F13	AF20
IO146PB4F13	AF21
IO147NB4F13	AC19
IO147PB4F13	AC20
IO148NB4F13	AH22
IO148PB4F13	AH23
IO149NB4F13	AC18
IO149PB4F13	AB18
IO150NB4F13	AK21
IO150PB4F13	AJ21
IO151NB4F13	AE18
IO151PB4F13	AD18
IO152NB4F14	AJ20
IO152PB4F14	AK20
IO153NB4F14	AG19
IO153PB4F14	AG20
IO154NB4F14	AH19
IO154PB4F14	AH20
IO155NB4F14	AC17
IO155PB4F14	AB17
IO156NB4F14	AK19
IO156PB4F14	AJ19
IO157NB4F14	AE17
IO157PB4F14	AD17
IO158NB4F14	AJ17
IO158PB4F14	AJ18
IO159NB4F14/CLKEN	AG18

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
IO159PB4F14/CLKEP	AH18
IO160NB4F14/CLKFN	AG16
IO160PB4F14/CLKFP	AG17
Bank 5	
IO161NB5F15/CLKGN	AG14
IO161PB5F15/CLKGP	AG15
IO162NB5F15/CLKHN	AG13
IO162PB5F15/CLKHP	AH13
IO163NB5F15	AE14
IO163PB5F15	AD14
IO164NB5F15	AJ12
IO164PB5F15	AJ13
IO165NB5F15	AB14
IO165PB5F15	AC15
IO166NB5F15	AK11
IO166PB5F15	AK12
IO167NB5F15	AB13
IO167PB5F15	AC14
IO168NB5F15	AH11
IO168PB5F15	AH12
IO169NB5F15	AD13
IO169PB5F15	AC13
IO170NB5F15	AJ10
IO170PB5F15	AJ11
IO171NB5F16	AG11
IO171PB5F16	AG12
IO172NB5F16	AK9
IO172PB5F16	AK10
IO173NB5F16	AE12
IO173PB5F16	AE13
IO174NB5F16	AG9
IO174PB5F16	AG10
IO175NB5F16	AE11
IO175PB5F16	AF11
IO176NB5F16	AH8
IO176PB5F16	AH9
IO177NB5F16	AC12
IO177PB5F16	AD12
IO178NB5F16	AJ7
IO178PB5F16	AJ8
IO179NB5F16	AF9
IO179PB5F16	AF10
IO180NB5F16	AE9
IO180PB5F16	AE10

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
IO181NB5F17	AC11
IO181PB5F17	AD11
IO182NB5F17	AK6
IO182PB5F17	AK7
IO183NB5F17	AF8
IO183PB5F17	AG8
IO184NB5F17	AG7
IO184PB5F17	AH7
IO185NB5F17	AC10
IO185PB5F17	AD10
IO186NB5F17	AJ5
IO186PB5F17	AJ6
IO187NB5F17	AE7
IO187PB5F17	AE8
IO188NB5F17	AF6
IO188PB5F17	AF7
IO189NB5F17	AD8
IO189PB5F17	AD9
IO190NB5F17	AH6
IO190PB5F17	AG6
IO191NB5F17	AG5
IO191PB5F17	AH5
IO192NB5F17	AC8
IO192PB5F17	AC9
Bank 6	
IO193NB6F18	AB7
IO193PB6F18	AC7
IO194NB6F18	AD5
IO194PB6F18	AE5
IO195NB6F18	AB6
IO195PB6F18	AC6
IO196NB6F18	AE4
IO196PB6F18	AF4
IO197NB6F18	AA8
IO197PB6F18	AB8
IO198NB6F18	AF3
IO198PB6F18	AG3
IO199NB6F18	AC4
IO199PB6F18	AD4
IO200NB6F18	AB5
IO200PB6F18	AC5
IO201NB6F18	Y7
IO201PB6F18	AA7
IO202NB6F18	AD3

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
IO202PB6F18	AE3
IO203NB6F19	Y6
IO203PB6F19	AA6
IO204NB6F19	Y5
IO204PB6F19	AA5
IO205NB6F19	W8
IO205PB6F19	Y8
IO206NB6F19	AA4
IO206PB6F19	AB4
IO207NB6F19	W6
IO207PB6F19	W7
IO208NB6F19	AB3
IO208PB6F19	AC3
IO209NB6F19	V8
IO209PB6F19	V9
IO210NB6F19	AA2
IO210PB6F19	AA1
IO211NB6F19	V5
IO211PB6F19	W5
IO212NB6F19	Y3
IO212PB6F19	Y4
IO213NB6F19	V7
IO213PB6F19	V6
IO214NB6F20	W3
IO214PB6F20	W4
IO215NB6F20	U8
IO215PB6F20	U9
IO216NB6F20	W1
IO216PB6F20	W2
IO217NB6F20	U7
IO217PB6F20	U6
IO218NB6F20	U4
IO218PB6F20	V4
IO219NB6F20	T5
IO219PB6F20	U5
IO220NB6F20	U3
IO220PB6F20	V3
IO221NB6F20	T8
IO221PB6F20	T9
IO222NB6F20	U2
IO222PB6F20	V2
IO223NB6F20	T7
IO223PB6F20	T6
IO224NB6F20	R2

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
IO224PB6F20	T2
Bank 7	
IO225NB7F21	R7
IO225PB7F21	R6
IO226NB7F21	R4
IO226PB7F21	R5
IO227NB7F21	R8
IO227PB7F21	R9
IO228NB7F21	P1
IO228PB7F21	R1
IO229NB7F21	P9
IO229PB7F21	P8
IO230NB7F21	N2
IO230PB7F21	P2
IO231NB7F21	P7
IO231PB7F21	P6
IO232NB7F21	N3
IO232PB7F21	P3
IO233NB7F21	P4
IO233PB7F21	P5
IO234NB7F21	L1
IO234PB7F21	M1
IO235NB7F21	M4
IO235PB7F21	N4
IO236NB7F22	N7
IO236PB7F22	N6
IO237NB7F22	N8
IO237PB7F22	N9
IO238NB7F22	M5
IO238PB7F22	N5
IO239NB7F22	L2
IO239PB7F22	M2
IO240NB7F22	L3
IO240PB7F22	M3
IO241NB7F22	M8
IO241PB7F22	M7
IO242NB7F22	K4
IO242PB7F22	L4
IO243NB7F22	L6
IO243PB7F22	M6
IO244NB7F22	K5
IO244PB7F22	L5
IO245NB7F22	J4
IO245PB7F22	J3

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
IO246NB7F22	G2
IO246PB7F22	H2
IO247NB7F23	L8
IO247PB7F23	L7
IO248NB7F23	G3
IO248PB7F23	H3
IO249NB7F23	G4
IO249PB7F23	H4
IO250NB7F23	J6
IO250PB7F23	K6
IO251NB7F23	H5
IO251PB7F23	J5
IO252NB7F23	F2
IO252PB7F23	F1
IO253NB7F23	K8
IO253PB7F23	K7
IO254NB7F23	F4
IO254PB7F23	F3
IO255NB7F23	G6
IO255PB7F23	H6
IO256NB7F23	F5
IO256PB7F23	G5
IO257NB7F23	H7
IO257PB7F23	J7
Dedicated I/O	
GND	A13
GND	A18
GND	A2
GND	A23
GND	A29
GND	A8
GND	AA10
GND	AA21
GND	AA28
GND	AA3
GND	AB2
GND	AB22
GND	AB29
GND	AB9
GND	AC1
GND	AC30
GND	AE25
GND	AE6
GND	AF26

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
GND	AF5
GND	AG27
GND	AG4
GND	AH10
GND	AH15
GND	AH16
GND	AH21
GND	AH28
GND	AH3
GND	AJ1
GND	AJ2
GND	AJ22
GND	AJ29
GND	AJ30
GND	AJ9
GND	AK13
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	R12
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3
GND	T12
GND	T13

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T28
GND	T3
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	V1
GND	V12
GND	V13
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18
GND	V19
GND	V30
GND	W12
GND	W13
GND	W14
GND	W15
GND	W16
GND	W17
GND	W18
GND	W19
GND	Y11
GND	Y20
GND/LP	E4
NC	A16
NC	A26
NC	A4
NC	A6
NC	AA30
NC	AB1
NC	AB30

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
NC	AC2
NC	AC29
NC	AD1
NC	AD2
NC	AD30
NC	AE1
NC	AE15
NC	AE16
NC	AE2
NC	AE30
NC	AF1
NC	AF2
NC	AF29
NC	AF30
NC	AG1
NC	AG2
NC	AG29
NC	AG30
NC	AH27
NC	AH4
NC	AJ14
NC	AJ15
NC	AJ16
NC	AJ27
NC	AJ4
NC	AK14
NC	AK15
NC	AK16
NC	AK17
NC	AK22
NC	AK4
NC	AK5
NC	B16
NC	B18
NC	B21
NC	B23
NC	B26
NC	B4
NC	B6
NC	B8
NC	C27
NC	D1
NC	D2
NC	D29

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
NC	D30
NC	E1
NC	E2
NC	E29
NC	E30
NC	F15
NC	F16
NC	F29
NC	F30
NC	G1
NC	G29
NC	G30
NC	H29
NC	J1
NC	J30
NC	K1
NC	K2
NC	L30
NC	M30
NC	N29
NC	T1
NC	U1
NC	W30
NC	Y1
NC	Y2
NC	Y30
PRA	G15
PRB	D16
PRC	AB16
PRD	AF16
TCK	G7
TDI	D5
TDO	J8
TMS	F6
TRST	C4
VCCA	AD6
VCCA	AH26
VCCA	E28
VCCA	E3
VCCA	L12
VCCA	L13
VCCA	L14
VCCA	L15
VCCA	L16

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
VCCA	L17
VCCA	L18
VCCA	L19
VCCA	M11
VCCA	M20
VCCA	N11
VCCA	N20
VCCA	P11
VCCA	P20
VCCA	R11
VCCA	R20
VCCA	T11
VCCA	T20
VCCA	U11
VCCA	U20
VCCA	V11
VCCA	V20
VCCA	W11
VCCA	W20
VCCA	Y12
VCCA	Y13
VCCA	Y14
VCCA	Y15
VCCA	Y16
VCCA	Y17
VCCA	Y18
VCCA	Y19
VCCPLA	G14
VCCPLB	H15
VCCPLC	G17
VCCPLD	J16
VCCPLE	AH17
VCCPLF	AC16
VCCPLG	AH14
VCCPLH	AD15
VCCDA	AD24
VCCDA	AD7
VCCDA	AF12
VCCDA	AF13
VCCDA	AF15
VCCDA	AF18
VCCDA	AF19
VCCDA	C13
VCCDA	C5

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
VCCDA	D13
VCCDA	D19
VCCDA	D3
VCCDA	E18
VCCDA	F26
VCCDA	G16
VCCDA	T25
VCCDA	T4
VCCIB0	A3
VCCIB0	B3
VCCIB0	J10
VCCIB0	J11
VCCIB0	J12
VCCIB0	K11
VCCIB0	K12
VCCIB0	K13
VCCIB0	K14
VCCIB0	K15
VCCIB1	A28
VCCIB1	B28
VCCIB1	J19
VCCIB1	J20
VCCIB1	J21
VCCIB1	K16
VCCIB1	K17
VCCIB1	K18
VCCIB1	K19
VCCIB1	K20
VCCIB2	C29
VCCIB2	C30
VCCIB2	K22
VCCIB2	L21
VCCIB2	L22
VCCIB2	M21
VCCIB2	M22
VCCIB2	N21
VCCIB2	P21
VCCIB2	R21
VCCIB3	AA22
VCCIB3	AH29
VCCIB3	AH30
VCCIB3	T21
VCCIB3	U21
VCCIB3	V21

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
VCCIB3	W21
VCCIB3	W22
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA16
VCCIB4	AA17
VCCIB4	AA18
VCCIB4	AA19
VCCIB4	AA20
VCCIB4	AB19
VCCIB4	AB20
VCCIB4	AB21
VCCIB4	AJ28
VCCIB4	AK28
VCCIB5	AA11
VCCIB5	AA12
VCCIB5	AA13
VCCIB5	AA14
VCCIB5	AA15
VCCIB5	AB10
VCCIB5	AB11
VCCIB5	AB12
VCCIB5	AJ3
VCCIB5	AK3
VCCIB6	AA9
VCCIB6	AH1
VCCIB6	AH2
VCCIB6	T10
VCCIB6	U10
VCCIB6	V10
VCCIB6	W10
VCCIB6	W9
VCCIB6	Y10
VCCIB6	Y9
VCCIB7	C1
VCCIB7	C2
VCCIB7	K9
VCCIB7	L10
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCCIB7	P10
VCCIB7	R10

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX1000 Function	Pin Number
VCOMPLA	F14
VCOMPLB	J15
VCOMPLC	F17
VCOMPLD	H16
VCOMPLE	AF17
VCOMPLF	AD16
VCOMPLG	AF14
VCOMPLH	AB15
VPUMP	G24

Table 3-11. Packaging Pin Assignment Table (PPAT)

FG896	
AX2000 Function	Pin Number
Bank 0	
IO00NB0F0	B4
IO00PB0F0	A4
IO01NB0F0	F8
IO01PB0F0	F7
IO02NB0F0	D6
IO02PB0F0	E6
IO04NB0F0	A5
IO04PB0F0	B5
IO05NB0F0	H8
IO05PB0F0	G8
IO06NB0F0	D7
IO06PB0F0	E7
IO07NB0F0	D8
IO07PB0F0	E8
IO08NB0F0	C7
IO08PB0F0	C6
IO09NB0F0	G9
IO09PB0F0	H9
IO10NB0F0	A6
IO10PB0F0	B6
IO11NB0F0	H10
IO11PB0F0	G10
IO12NB0F1	E9
IO12PB0F1	F9
IO13NB0F1	E10
IO13PB0F1	F10
IO15NB0F1	F11
IO15PB0F1	G11
IO16NB0F1	A7
IO16PB0F1	B7

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	C9
IO18PB0F1	C8
IO19NB0F1	D11
IO19PB0F1	E11
IO20PB0F1	B8
IO21NB0F1	H12
IO21PB0F1	H11
IO23NB0F2	A10
IO23PB0F2	A9
IO25NB0F2	F12
IO25PB0F2	G12
IO26NB0F2	B11
IO26PB0F2	B10
IO27NB0F2	D12
IO27PB0F2	E12
IO28NB0F2	C12
IO28PB0F2	C11
IO30NB0F2	A12
IO30PB0F2	A11
IO31NB0F2	F13
IO31PB0F2	G13
IO33NB0F2	H13
IO33PB0F2	J13
IO34NB0F3	B13
IO34PB0F3	B12
IO37NB0F3	E14
IO37PB0F3	E13
IO38NB0F3	B14
IO38PB0F3	A14
IO39NB0F3	H14
IO39PB0F3	J14
IO40NB0F3	B15
IO40PB0F3	A15
IO41NB0F3/HCLKAN	C14
IO41PB0F3/HCLKAP	D14
IO42NB0F3/HCLKBN	E15
IO42PB0F3/HCLKBP	D15
Bank 1	
IO43NB1F4/HCLKCN	E17
IO43PB1F4/HCLKCP	E16
IO44NB1F4/HCLKDN	C17
IO44PB1F4/HCLKDP	D17

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
IO45NB1F4	A16
IO45PB1F4	B16
IO47NB1F4	H17
IO47PB1F4	J17
IO48NB1F4	A17
IO48PB1F4	B17
IO49NB1F4	H18
IO49PB1F4	J18
IO51NB1F4	F18
IO51PB1F4	G18
IO52NB1F4	B18
IO53NB1F4	D18
IO53PB1F4	C18
IO55NB1F5	H19
IO55PB1F5	G19
IO56NB1F5	B19
IO56PB1F5	A19
IO57NB1F5	E20
IO57PB1F5	E19
IO58NB1F5	C20
IO58PB1F5	C19
IO59NB1F5	B20
IO59PB1F5	A20
IO61NB1F5	F20
IO61PB1F5	F19
IO62NB1F5	A22
IO62PB1F5	A21
IO63NB1F5	D21
IO63PB1F5	D20
IO65NB1F6	G20
IO65PB1F6	H20
IO66NB1F6	B23
IO66PB1F6	B21
IO67NB1F6	H21
IO67PB1F6	G21
IO68NB1F6	D22
IO68PB1F6	C22
IO69NB1F6	A25
IO69PB1F6	A24
IO70NB1F6	F22
IO70PB1F6	E22
IO71NB1F6	F21
IO71PB1F6	E21
IO73NB1F6	C24

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
IO73PB1F6	C23
IO74NB1F6	D24
IO74PB1F6	D23
IO75NB1F6	H23
IO75PB1F6	H22
IO76NB1F7	B25
IO76PB1F7	B24
IO78NB1F7	B26
IO78PB1F7	A26
IO79NB1F7	F23
IO79PB1F7	E23
IO80NB1F7	D25
IO80PB1F7	C25
IO81NB1F7	G23
IO81PB1F7	G22
IO82NB1F7	B27
IO82PB1F7	A27
IO83NB1F7	F24
IO83PB1F7	E24
IO84NB1F7	D26
IO84PB1F7	C26
IO85NB1F7	F25
IO85PB1F7	E25
Bank 2	
IO86NB2F8	G26
IO86PB2F8	G25
IO87NB2F8	K23
IO87PB2F8	J23
IO88NB2F8	J24
IO88PB2F8	H24
IO89NB2F8	E29
IO89PB2F8	D29
IO90NB2F8	F27
IO90PB2F8	E27
IO91NB2F8	H26
IO91PB2F8	H25
IO92NB2F8	G28
IO92PB2F8	F28
IO93NB2F8	J26
IO93PB2F8	J25
IO94NB2F8	H27
IO94PB2F8	G27
IO95NB2F8	H29
IO95PB2F8	G29

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
IO96NB2F9	G30
IO96PB2F9	F30
IO97NB2F9	K25
IO97PB2F9	K24
IO98NB2F9	J28
IO98PB2F9	H28
IO99NB2F9	L23
IO99PB2F9	L24
IO100NB2F9	K27
IO100PB2F9	J27
IO101PB2F9	J30
IO102NB2F9	E30
IO102PB2F9	D30
IO103NB2F9	L26
IO103PB2F9	K26
IO104NB2F9	F29
IO105NB2F9	M25
IO105PB2F9	L25
IO106NB2F9	K30
IO106PB2F9	K29
IO107NB2F10	M23
IO107PB2F10	M24
IO109NB2F10	M27
IO109PB2F10	L27
IO110NB2F10	M28
IO110PB2F10	L28
IO111NB2F10	N22
IO111PB2F10	N23
IO112NB2F10	M29
IO112PB2F10	L29
IO113NB2F10	N26
IO113PB2F10	M26
IO114NB2F10	M30
IO114PB2F10	L30
IO115NB2F10	N28
IO115PB2F10	N27
IO117NB2F10	N25
IO117PB2F10	N24
IO118NB2F11	N29
IO119NB2F11	P22
IO119PB2F11	P23
IO121NB2F11	P25
IO121PB2F11	P24
IO122NB2F11	P28

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
IO122PB2F11	P27
IO123NB2F11	R26
IO123PB2F11	P26
IO124NB2F11	P29
IO124PB2F11	P30
IO125NB2F11	R22
IO125PB2F11	R23
IO127NB2F11	R24
IO127PB2F11	R25
IO128NB2F11	R29
IO128PB2F11	R30
Bank 3	
IO129NB3F12	T27
IO129PB3F12	R27
IO130NB3F12	T29
IO130PB3F12	T30
IO131NB3F12	T22
IO131PB3F12	T23
IO132NB3F12	U26
IO132PB3F12	T26
IO133NB3F12	U24
IO133PB3F12	T24
IO135NB3F12	U23
IO135PB3F12	U22
IO136NB3F12	U29
IO136PB3F12	U30
IO137NB3F12	V28
IO137PB3F12	U28
IO138NB3F12	V27
IO138PB3F12	U27
IO139NB3F13	V25
IO139PB3F13	U25
IO141NB3F13	V23
IO141PB3F13	V22
IO142NB3F13	W29
IO142PB3F13	V29
IO143NB3F13	W26
IO143PB3F13	V26
IO145NB3F13	W24
IO145PB3F13	V24
IO146NB3F13	W27
IO146PB3F13	W28
IO147NB3F13	Y28
IO147PB3F13	Y27

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
IO148NB3F13	Y30
IO148PB3F13	W30
IO149NB3F13	Y25
IO149PB3F13	W25
IO150NB3F14	AA29
IO150PB3F14	Y29
IO151NB3F14	AC29
IO152NB3F14	AA26
IO152PB3F14	Y26
IO153NB3F14	Y23
IO153PB3F14	W23
IO154NB3F14	AB30
IO154PB3F14	AA30
IO155NB3F14	AB27
IO155PB3F14	AA27
IO156NB3F14	AC28
IO156PB3F14	AB28
IO157NB3F14	AA24
IO157PB3F14	Y24
IO158NB3F14	AF29
IO158PB3F14	AF30
IO159NB3F14	AB25
IO159PB3F14	AA25
IO160NB3F14	AE30
IO160PB3F14	AD30
IO161NB3F15	AE29
IO161PB3F15	AD29
IO162NB3F15	AD27
IO162PB3F15	AC27
IO163NB3F15	AC26
IO163PB3F15	AB26
IO164NB3F15	AE28
IO164PB3F15	AD28
IO165NB3F15	AC24
IO165PB3F15	AB24
IO166NB3F15	AG28
IO166PB3F15	AF28
IO167NB3F15	AE26
IO167PB3F15	AD26
IO168NB3F15	AD25
IO168PB3F15	AC25
IO169NB3F15	AF27
IO169PB3F15	AE27
IO170NB3F15	AB23

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
IO170PB3F15	AA23
Bank 4	
IO171NB4F16	AG29
IO171PB4F16	AG30
IO172NB4F16	AF24
IO172PB4F16	AF25
IO173NB4F16	AG25
IO173PB4F16	AG26
IO174NB4F16	AJ25
IO174PB4F16	AJ26
IO175NB4F16	AK26
IO175PB4F16	AK27
IO176NB4F16	AE23
IO176PB4F16	AE24
IO177NB4F16	AH24
IO177PB4F16	AH25
IO178NB4F16	AD23
IO178PB4F16	AC23
IO179PB4F16	AJ27
IO180NB4F16	AG23
IO180PB4F16	AG24
IO181NB4F17	AK24
IO181PB4F17	AK25
IO182NB4F17	AD22
IO182PB4F17	AC22
IO183NB4F17	AF22
IO183PB4F17	AF23
IO184NB4F17	AE21
IO184PB4F17	AE22
IO185NB4F17	AJ23
IO185PB4F17	AJ24
IO187NB4F17	AH22
IO187PB4F17	AH23
IO188NB4F17	AD21
IO188PB4F17	AC21
IO189PB4F17	AK22
IO190NB4F17	AF20
IO190PB4F17	AF21
IO191NB4F17	AG21
IO191PB4F17	AG22
IO192NB4F17	AE19
IO192PB4F17	AE20
IO195NB4F18	AK21
IO195PB4F18	AJ21

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
IO196NB4F18	AD19
IO196PB4F18	AD20
IO197NB4F18	AJ20
IO197PB4F18	AK20
IO198NB4F18	AC19
IO198PB4F18	AC20
IO199NB4F18	AG19
IO199PB4F18	AG20
IO200NB4F18	AH19
IO200PB4F18	AH20
IO201NB4F18	AK19
IO201PB4F18	AJ19
IO202NB4F18	AC18
IO202PB4F18	AB18
IO206NB4F19	AE18
IO206PB4F19	AD18
IO207NB4F19	AJ17
IO207PB4F19	AJ18
IO208NB4F19	AE17
IO208PB4F19	AD17
IO209NB4F19	AK17
IO210NB4F19	AC17
IO210PB4F19	AB17
IO211NB4F19	AJ16
IO211PB4F19	AK16
IO212NB4F19/CLKEN	AG18
IO212PB4F19/CLKEP	AH18
IO213NB4F19/CLKFN	AG16
IO213PB4F19/CLKFP	AG17
Bank 5	
IO214NB5F20/CLKGN	AG14
IO214PB5F20/CLKGP	AG15
IO215NB5F20/CLKHN	AG13
IO215PB5F20/CLKHP	AH13
IO216NB5F20	AB14
IO216PB5F20	AC15
IO217NB5F20	AK15
IO217PB5F20	AJ15
IO218NB5F20	AE14
IO218PB5F20	AD14
IO219NB5F20	AK14
IO219PB5F20	AJ14
IO222NB5F20	AB13
IO222PB5F20	AC14

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
IO223NB5F21	AJ12
IO223PB5F21	AJ13
IO225NB5F21	AH11
IO225PB5F21	AH12
IO226NB5F21	AC13
IO226PB5F21	AD13
IO227NB5F21	AE12
IO227PB5F21	AE13
IO228NB5F21	AG11
IO228PB5F21	AG12
IO229NB5F21	AK11
IO229PB5F21	AK12
IO230NB5F21	AC12
IO230PB5F21	AD12
IO232NB5F21	AE11
IO232PB5F21	AF11
IO233NB5F21	AJ10
IO233PB5F21	AJ11
IO234NB5F21	AC11
IO234PB5F21	AD11
IO236NB5F22	AK9
IO236PB5F22	AK10
IO237NB5F22	AG9
IO237PB5F22	AG10
IO238NB5F22	AF9
IO238PB5F22	AF10
IO239NB5F22	AH8
IO239PB5F22	AH9
IO240NB5F22	AC10
IO240PB5F22	AD10
IO242NB5F22	AE9
IO242PB5F22	AE10
IO243NB5F22	AJ7
IO243PB5F22	AJ8
IO244NB5F22	AK6
IO244PB5F22	AK7
IO245NB5F23	AF8
IO245PB5F23	AG8
IO246NB5F23	AD8
IO246PB5F23	AD9
IO247NB5F23	AG7
IO247PB5F23	AH7
IO248NB5F23	AK5
IO249NB5F23	AJ5

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
IO249PB5F23	AJ6
IO250NB5F23	AC8
IO250PB5F23	AC9
IO251NB5F23	AH6
IO251PB5F23	AG6
IO252NB5F23	AF6
IO252PB5F23	AF7
IO253NB5F23	AG2
IO253PB5F23	AG1
IO254NB5F23	AE7
IO254PB5F23	AE8
IO255NB5F23	AG5
IO255PB5F23	AH5
IO256NB5F23	AJ4
IO256PB5F23	AK4
Bank 6	
IO257NB6F24	AE4
IO257PB6F24	AF4
IO258NB6F24	AB7
IO258PB6F24	AC7
IO259NB6F24	AD5
IO259PB6F24	AE5
IO260NB6F24	AF1
IO260PB6F24	AF2
IO261NB6F24	AF3
IO261PB6F24	AG3
IO262NB6F24	AC4
IO262PB6F24	AD4
IO263NB6F24	AD3
IO263PB6F24	AE3
IO264NB6F24	AB6
IO264PB6F24	AC6
IO265NB6F24	AD1
IO265PB6F24	AE1
IO266NB6F24	AA8
IO266PB6F24	AB8
IO267NB6F25	AB5
IO267PB6F25	AC5
IO268NB6F25	AB3
IO268PB6F25	AC3
IO269NB6F25	AC2
IO269PB6F25	AD2
IO270NB6F25	Y7
IO270PB6F25	AA7

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
IO271NB6F25	AA4
IO271PB6F25	AB4
IO272NB6F25	Y6
IO272PB6F25	AA6
IO273NB6F25	AB1[1]
IO273PB6F25	AE2[1]
IO274NB6F25	W8
IO274PB6F25	Y8
IO275NB6F25	Y5
IO275PB6F25	AA5
IO277NB6F25	AA2
IO277PB6F25	AA1
IO278NB6F26	W6
IO278PB6F26	W7
IO279NB6F26	Y3
IO279PB6F26	Y4
IO280NB6F26	V8
IO280PB6F26	V9
IO281NB6F26	Y1
IO281PB6F26	Y2
IO282NB6F26	V5
IO282PB6F26	W5
IO284NB6F26	V7
IO284PB6F26	V6
IO285NB6F26	W3
IO285PB6F26	W4
IO286NB6F26	U8
IO286PB6F26	U9
IO287NB6F26	W1
IO287PB6F26	W2
IO288NB6F26	U7
IO288PB6F26	U6
IO290NB6F27	U4
IO290PB6F27	V4
IO291NB6F27	U3
IO291PB6F27	V3
IO292NB6F27	T5
IO292PB6F27	U5
IO293NB6F27	U2
IO293PB6F27	V2
IO294NB6F27	T8
IO294PB6F27	T9
IO296NB6F27	T1
IO296PB6F27	U1

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
IO298NB6F27	T7
IO298PB6F27	T6
IO299NB6F27	R2
IO299PB6F27	T2
Bank 7	
IO300NB7F28	R8
IO300PB7F28	R9
IO302NB7F28	R4
IO302PB7F28	R5
IO303NB7F28	P1
IO303PB7F28	R1
IO304NB7F28	R7
IO304PB7F28	R6
IO306NB7F28	N2
IO306PB7F28	P2
IO307NB7F28	N3
IO307PB7F28	P3
IO308NB7F28	P9
IO308PB7F28	P8
IO309NB7F28	P4
IO309PB7F28	P5
IO310NB7F29	P7
IO310PB7F29	P6
IO311NB7F29	L1
IO311PB7F29	M1
IO312NB7F29	M5
IO312PB7F29	N5
IO313NB7F29	M4
IO313PB7F29	N4
IO315NB7F29	L2
IO315PB7F29	M2
IO316NB7F29	N7
IO316PB7F29	N6
IO317NB7F29	L3
IO317PB7F29	M3
IO318NB7F29	N8
IO318PB7F29	N9
IO320NB7F29	L6
IO320PB7F29	M6
IO321NB7F30	K4
IO321PB7F30	L4
IO322NB7F30	M8
IO322PB7F30	M7
IO323NB7F30	J1

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
IO323PB7F30	K1
IO324NB7F30	K5
IO324PB7F30	L5
IO326NB7F30	G1[1]
IO326PB7F30	K2[1]
IO327NB7F30	J4
IO327PB7F30	J3
IO328NB7F30	L8
IO328PB7F30	L7
IO329NB7F30	G2
IO329PB7F30	H2
IO330NB7F30	G3
IO330PB7F30	H3
IO331NB7F30	K8
IO331PB7F30	K7
IO332NB7F31	J6
IO332PB7F31	K6
IO333NB7F31	D1
IO333PB7F31	D2
IO334NB7F31	G4
IO334PB7F31	H4
IO335NB7F31	F2
IO335PB7F31	F1
IO336NB7F31	H5
IO336PB7F31	J5
IO337NB7F31	E2
IO337PB7F31	E1
IO338NB7F31	H7
IO338PB7F31	J7
IO339NB7F31	F4
IO339PB7F31	F3
IO340NB7F31	F5
IO340PB7F31	G5
IO341NB7F31	G6
IO341PB7F31	H6
Dedicated I/O	
GND	A13
GND	A18
GND	A2
GND	A23
GND	A29
GND	A8
GND	AA10
GND	AA21

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
GND	AA28
GND	AA3
GND	AB2
GND	AB22
GND	AB29
GND	AB9
GND	AC1
GND	AC30
GND	AE25
GND	AE6
GND	AF26
GND	AF5
GND	AG27
GND	AG4
GND	AH10
GND	AH15
GND	AH16
GND	AH21
GND	AH28
GND	AH3
GND	AJ1
GND	AJ2
GND	AJ22
GND	AJ29
GND	AJ30
GND	AJ9
GND	AK13
GND	AK18
GND	AK2
GND	AK23
GND	AK29
GND	AK8
GND	B1
GND	B2
GND	B22
GND	B29
GND	B30
GND	B9
GND	C10
GND	C15
GND	C16
GND	C21
GND	C28
GND	C3

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
GND	D27
GND	D28
GND	D4
GND	E26
GND	E5
GND	H1
GND	H30
GND	J2
GND	J22
GND	J29
GND	J9
GND	K10
GND	K21
GND	K28
GND	K3
GND	L11
GND	L20
GND	M12
GND	M13
GND	M14
GND	M15
GND	M16
GND	M17
GND	M18
GND	M19
GND	N1
GND	N12
GND	N13
GND	N14
GND	N15
GND	N16
GND	N17
GND	N18
GND	N19
GND	N30
GND	P12
GND	P13
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	R12

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
GND	R13
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R28
GND	R3
GND	T12
GND	T13
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T28
GND	T3
GND	U12
GND	U13
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	V1
GND	V12
GND	V13
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18
GND	V19
GND	V30
GND	W12
GND	W13
GND	W14
GND	W15
GND	W16
GND	W17
GND	W18

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
GND	W19
GND	Y11
GND	Y20
GND/LP	E4
PRA	G15
PRB	D16
PRC	AB16
PRD	AF16
TCK	G7
TDI	D5
TDO	J8
TMS	F6
TRST	C4
VCCA	AD6
VCCA	AH26
VCCA	E28
VCCA	E3
VCCA	L12
VCCA	L13
VCCA	L14
VCCA	L15
VCCA	L16
VCCA	L17
VCCA	L18
VCCA	L19
VCCA	M11
VCCA	M20
VCCA	N11
VCCA	N20
VCCA	P11
VCCA	P20
VCCA	R11
VCCA	R20
VCCA	T11
VCCA	T20
VCCA	U11
VCCA	U20
VCCA	V11
VCCA	V20
VCCA	W11
VCCA	W20
VCCA	Y12
VCCA	Y13
VCCA	Y14

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
VCCA	Y15
VCCA	Y16
VCCA	Y17
VCCA	Y18
VCCA	Y19
VCCDA	AD24
VCCDA	AD7
VCCDA	AE15
VCCDA	AE16
VCCDA	AF12
VCCDA	AF13
VCCDA	AF15
VCCDA	AF18
VCCDA	AF19
VCCDA	AH27
VCCDA	AH4
VCCDA	C13
VCCDA	C27
VCCDA	C5
VCCDA	D13
VCCDA	D19
VCCDA	D3
VCCDA	E18
VCCDA	F15
VCCDA	F16
VCCDA	F26
VCCDA	G16
VCCDA	T25
VCCDA	T4
VCCIB0	A3
VCCIB0	B3
VCCIB0	J10
VCCIB0	J11
VCCIB0	J12
VCCIB0	K11
VCCIB0	K12
VCCIB0	K13
VCCIB0	K14
VCCIB0	K15
VCCIB1	A28
VCCIB1	B28
VCCIB1	J19
VCCIB1	J20
VCCIB1	J21

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
VCCIB1	K16
VCCIB1	K17
VCCIB1	K18
VCCIB1	K19
VCCIB1	K20
VCCIB2	C29
VCCIB2	C30
VCCIB2	K22
VCCIB2	L21
VCCIB2	L22
VCCIB2	M21
VCCIB2	M22
VCCIB2	N21
VCCIB2	P21
VCCIB2	R21
VCCIB3	AA22
VCCIB3	AH29
VCCIB3	AH30
VCCIB3	T21
VCCIB3	U21
VCCIB3	V21
VCCIB3	W21
VCCIB3	W22
VCCIB3	Y21
VCCIB3	Y22
VCCIB4	AA16
VCCIB4	AA17
VCCIB4	AA18
VCCIB4	AA19
VCCIB4	AA20
VCCIB4	AB19
VCCIB4	AB20
VCCIB4	AB21
VCCIB4	AJ28
VCCIB4	AK28
VCCIB5	AA11
VCCIB5	AA12
VCCIB5	AA13
VCCIB5	AA14
VCCIB5	AA15
VCCIB5	AB10
VCCIB5	AB11
VCCIB5	AB12
VCCIB5	AJ3

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG896	
AX2000 Function	Pin Number
VCCIB5	AK3
VCCIB6	AA9
VCCIB6	AH1
VCCIB6	AH2
VCCIB6	T10
VCCIB6	U10
VCCIB6	V10
VCCIB6	W10
VCCIB6	W9
VCCIB6	Y10
VCCIB6	Y9
VCCIB7	C1
VCCIB7	C2
VCCIB7	K9
VCCIB7	L10
VCCIB7	L9
VCCIB7	M10
VCCIB7	M9
VCCIB7	N10
VCCIB7	P10
VCCIB7	R10
VCCPLA	G14
VCCPLB	H15
VCCPLC	G17
VCCPLD	J16
VCCPLE	AH17
VCCPLF	AC16
VCCPLG	AH14
VCCPLH	AD15
VCOMPLA	F14
VCOMPLB	J15
VCOMPLC	F17
VCOMPLD	H16
VCOMPLE	AF17
VCOMPLF	AD16
VCOMPLG	AF14
VCOMPLH	AB15
VPUMP	G24

Note:

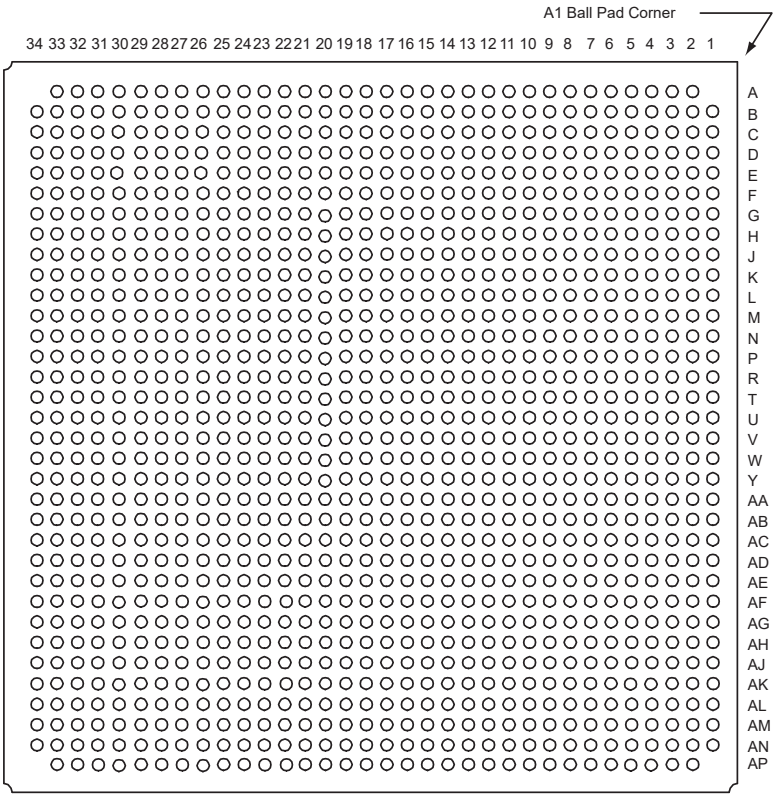
1. Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

3.7 FG1152

The following figure shows package bottom-view of FG1152.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 3-7. Package Bottom-View



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

The following table lists the IOD interface pin placement.

Table 3-12. Packaging Pin Assignment Table (PPAT)

FG1152	
AX2000 Function	Pin Number
Bank 0	
IO00NB0F0	D6
IO00PB0F0	C6
IO01NB0F0	H10
IO01PB0F0	H9
IO02NB0F0	F8
IO02PB0F0	G8
IO03NB0F0	A6
IO03PB0F0	B6
IO04NB0F0	C7
IO04PB0F0	D7
IO05NB0F0	K10
IO05PB0F0	J10
IO06NB0F0	F9
IO06PB0F0	G9
IO07NB0F0	F10
IO07PB0F0	G10

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO08NB0F0	E9
IO08PB0F0	E8
IO09NB0F0	J11
IO09PB0F0	K11
IO10NB0F0	C8
IO10PB0F0	D8
IO11NB0F0	K12
IO11PB0F0	J12
IO12NB0F1	G11
IO12PB0F1	H11
IO13NB0F1	G12
IO13PB0F1	H12
IO14NB0F1	A7
IO14PB0F1	B7
IO15NB0F1	H13
IO15PB0F1	J13
IO16NB0F1	C9
IO16PB0F1	D9
IO17NB0F1	F12
IO17PB0F1	F11
IO18NB0F1	E11
IO18PB0F1	E10
IO19NB0F1	F13
IO19PB0F1	G13
IO20NB0F1	A10
IO20PB0F1	A9
IO21NB0F1	K14
IO21PB0F1	K13
IO22NB0F2	B11
IO22PB0F2	B10
IO23NB0F2	C12
IO23PB0F2	C11
IO24NB0F2	A12
IO24PB0F2	A11
IO25NB0F2	H14
IO25PB0F2	J14
IO26NB0F2	D13
IO26PB0F2	D12
IO27NB0F2	F14
IO27PB0F2	G14
IO28NB0F2	E14
IO28PB0F2	E13
IO29NB0F2	B13
IO29PB0F2	B12

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO30NB0F2	C14
IO30PB0F2	C13
IO31NB0F2	H15
IO31PB0F2	J15
IO32NB0F2	A14
IO32PB0F2	B14
IO33NB0F2	K15
IO33PB0F2	L15
IO34NB0F3	D15
IO34PB0F3	D14
IO35NB0F3	A15
IO35PB0F3	B15
IO36NB0F3	B16
IO36PB0F3	A16
IO37NB0F3	G16
IO37PB0F3	G15
IO38NB0F3	D16
IO38PB0F3	C16
IO39NB0F3	K16
IO39PB0F3	L16
IO40NB0F3	D17
IO40PB0F3	C17
IO41NB0F3/HCLKAN	E16
IO41PB0F3/HCLKAP	F16
IO42NB0F3/HCLKBN	G17
IO42PB0F3/HCLKBP	F17
Bank 1	
IO43NB1F4/HCLKCN	G19
IO43PB1F4/HCLKCP	G18
IO44NB1F4/HCLKDN	E19
IO44PB1F4/HCLKDP	F19
IO45NB1F4	C18
IO45PB1F4	D18
IO46NB1F4	A18
IO46PB1F4	B18
IO47NB1F4	K19
IO47PB1F4	L19
IO48NB1F4	C19
IO48PB1F4	D19
IO49NB1F4	K20
IO49PB1F4	L20
IO50NB1F4	A19
IO50PB1F4	B19
IO51NB1F4	H20

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO51PB1F4	J20
IO52NB1F4	B20
IO52PB1F4	A20
IO53NB1F4	F20
IO53PB1F4	E20
IO54NB1F5	B21
IO54PB1F5	A21
IO55NB1F5	K21
IO55PB1F5	J21
IO56NB1F5	D21
IO56PB1F5	C21
IO57NB1F5	G22
IO57PB1F5	G21
IO58NB1F5	E22
IO58PB1F5	E21
IO59NB1F5	D22
IO59PB1F5	C22
IO60NB1F5	B23
IO60PB1F5	A23
IO61NB1F5	H22
IO61PB1F5	H21
IO62NB1F5	C24
IO62PB1F5	C23
IO63NB1F5	F23
IO63PB1F5	F22
IO64NB1F6	B24
IO64PB1F6	A24
IO65NB1F6	J22
IO65PB1F6	K22
IO66NB1F6	B25
IO66PB1F6	A25
IO67NB1F6	K23
IO67PB1F6	J23
IO68NB1F6	F24
IO68PB1F6	E24
IO69NB1F6	C27
IO69PB1F6	C26
IO70NB1F6	H24
IO70PB1F6	G24
IO71NB1F6	H23
IO71PB1F6	G23
IO72NB1F6	B28
IO72PB1F6	A28
IO73NB1F6	E26

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO73PB1F6	E25
IO74NB1F6	F26
IO74PB1F6	F25
IO75NB1F6	K25
IO75PB1F6	K24
IO76NB1F7	D27
IO76PB1F7	D26
IO77NB1F7	B29
IO77PB1F7	A29
IO78NB1F7	D28
IO78PB1F7	C28
IO79NB1F7	H25
IO79PB1F7	G25
IO80NB1F7	F27
IO80PB1F7	E27
IO81NB1F7	J25
IO81PB1F7	J24
IO82NB1F7	D29
IO82PB1F7	C29
IO83NB1F7	H26
IO83PB1F7	G26
IO84NB1F7	F28
IO84PB1F7	E28
IO85NB1F7	H27
IO85PB1F7	G27
Bank 2	
IO86NB2F8	J28
IO86PB2F8	J27
IO87NB2F8	M25
IO87PB2F8	L25
IO88NB2F8	L26
IO88PB2F8	K26
IO89NB2F8	G31
IO89PB2F8	F31
IO90NB2F8	H29
IO90PB2F8	G29
IO91NB2F8	K28
IO91PB2F8	K27
IO92NB2F8	J30
IO92PB2F8	H30
IO93NB2F8	L28
IO93PB2F8	L27
IO94NB2F8	K29
IO94PB2F8	J29

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO95NB2F8	K31
IO95PB2F8	J31
IO96NB2F9	J32
IO96PB2F9	H32
IO97NB2F9	M27
IO97PB2F9	M26
IO98NB2F9	L30
IO98PB2F9	K30
IO99NB2F9	N25
IO99PB2F9	N26
IO100NB2F9	M29
IO100PB2F9	L29
IO101NB2F9	L33
IO101PB2F9	L32
IO102NB2F9	K34
IO102PB2F9	K33
IO103NB2F9	N28
IO103PB2F9	M28
IO104NB2F9	M34
IO104PB2F9	L34
IO105NB2F9	P27
IO105PB2F9	N27
IO106NB2F9	M32
IO106PB2F9	M31
IO107NB2F10	P25
IO107PB2F10	P26
IO108NB2F10	N33
IO108PB2F10	M33
IO109NB2F10	P29
IO109PB2F10	N29
IO110NB2F10	P30
IO110PB2F10	N30
IO111NB2F10	R24
IO111PB2F10	R25
IO112NB2F10	P31
IO112PB2F10	N31
IO113NB2F10	R28
IO113PB2F10	P28
IO114NB2F10	P32
IO114PB2F10	N32
IO115NB2F10	R30
IO115PB2F10	R29
IO116NB2F10	P34
IO116PB2F10	P33

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO117NB2F10	R27
IO117PB2F10	R26
IO118NB2F11	R34
IO118PB2F11	R33
IO119NB2F11	T24
IO119PB2F11	T25
IO120NB2F11	T33
IO120PB2F11	T34
IO121NB2F11	T27
IO121PB2F11	T26
IO122NB2F11	T30
IO122PB2F11	T29
IO123NB2F11	U28
IO123PB2F11	T28
IO124NB2F11	T31
IO124PB2F11	T32
IO125NB2F11	U24
IO125PB2F11	U25
IO126NB2F11	U33
IO126PB2F11	U34
IO127NB2F11	U26
IO127PB2F11	U27
IO128NB2F11	U31
IO128PB2F11	U32
Bank 3	
IO129NB3F12	V29
IO129PB3F12	U29
IO130NB3F12	V31
IO130PB3F12	V32
IO131NB3F12	V24
IO131PB3F12	V25
IO132NB3F12	W28
IO132PB3F12	V28
IO133NB3F12	W26
IO133PB3F12	V26
IO134NB3F12	W33
IO134PB3F12	V33
IO135NB3F12	W25
IO135PB3F12	W24
IO136NB3F12	W31
IO136PB3F12	W32
IO137NB3F12	Y30
IO137PB3F12	W30
IO138NB3F12	Y29

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO138PB3F12	W29
IO139NB3F13	Y27
IO139PB3F13	W27
IO140NB3F13	AA33
IO140PB3F13	Y33
IO141NB3F13	Y25
IO141PB3F13	Y24
IO142NB3F13	AA31
IO142PB3F13	Y31
IO143NB3F13	AA28
IO143PB3F13	Y28
IO144NB3F13	AA34
IO144PB3F13	Y34
IO145NB3F13	AA26
IO145PB3F13	Y26
IO146NB3F13	AA29
IO146PB3F13	AA30
IO147NB3F13	AB30
IO147PB3F13	AB29
IO148NB3F13	AB32
IO148PB3F13	AA32
IO149NB3F13	AB27
IO149PB3F13	AA27
IO150NB3F14	AC31
IO150PB3F14	AB31
IO151NB3F14	AD33
IO151PB3F14	AC33
IO152NB3F14	AC28
IO152PB3F14	AB28
IO153NB3F14	AB25
IO153PB3F14	AA25
IO154NB3F14	AD32
IO154PB3F14	AC32
IO155NB3F14	AD29
IO155PB3F14	AC29
IO156NB3F14	AE30
IO156PB3F14	AD30
IO157NB3F14	AC26
IO157PB3F14	AB26
IO158NB3F14	AH33
IO158PB3F14	AG33
IO159NB3F14	AD27
IO159PB3F14	AC27
IO160NB3F14	AG32

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO160PB3F14	AF32
IO161NB3F15	AG31
IO161PB3F15	AF31
IO162NB3F15	AF29
IO162PB3F15	AE29
IO163NB3F15	AE28
IO163PB3F15	AD28
IO164NB3F15	AG30
IO164PB3F15	AF30
IO165NB3F15	AE26
IO165PB3F15	AD26
IO166NB3F15	AJ30
IO166PB3F15	AH30
IO167NB3F15	AG28
IO167PB3F15	AF28
IO168NB3F15	AF27
IO168PB3F15	AE27
IO169NB3F15	AH29
IO169PB3F15	AG29
IO170NB3F15	AD25
IO170PB3F15	AC25
Bank 4	
IO171NB4F16	AP29
IO171PB4F16	AN29
IO172NB4F16	AH26
IO172PB4F16	AH27
IO173NB4F16	AJ27
IO173PB4F16	AJ28
IO174NB4F16	AL27
IO174PB4F16	AL28
IO175NB4F16	AM28
IO175PB4F16	AM29
IO176NB4F16	AG25
IO176PB4F16	AG26
IO177NB4F16	AK26
IO177PB4F16	AK27
IO178NB4F16	AF25
IO178PB4F16	AE25
IO179NB4F16	AP28
IO179PB4F16	AN28
IO180NB4F16	AJ25
IO180PB4F16	AJ26
IO181NB4F17	AM26
IO181PB4F17	AM27

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO182NB4F17	AF24
IO182PB4F17	AE24
IO183NB4F17	AH24
IO183PB4F17	AH25
IO184NB4F17	AG23
IO184PB4F17	AG24
IO185NB4F17	AL25
IO185PB4F17	AL26
IO186NB4F17	AP25
IO186PB4F17	AP26
IO187NB4F17	AK24
IO187PB4F17	AK25
IO188NB4F17	AF23
IO188PB4F17	AE23
IO189NB4F17	AN24
IO189PB4F17	AM24
IO190NB4F17	AH22
IO190PB4F17	AH23
IO191NB4F17	AJ23
IO191PB4F17	AJ24
IO192NB4F17	AG21
IO192PB4F17	AG22
IO193NB4F18	AP23
IO193PB4F18	AP24
IO194NB4F18	AN22
IO194PB4F18	AN23
IO195NB4F18	AM23
IO195PB4F18	AL23
IO196NB4F18	AF21
IO196PB4F18	AF22
IO197NB4F18	AL22
IO197PB4F18	AM22
IO198NB4F18	AE21
IO198PB4F18	AE22
IO199NB4F18	AJ21
IO199PB4F18	AJ22
IO200NB4F18	AK21
IO200PB4F18	AK22
IO201NB4F18	AM21
IO201PB4F18	AL21
IO202NB4F18	AE20
IO202PB4F18	AD20
IO203NB4F19	AN21
IO203PB4F19	AP21

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO204NB4F19	AP20
IO204PB4F19	AN20
IO205NB4F19	AN19
IO205PB4F19	AP19
IO206NB4F19	AG20
IO206PB4F19	AF20
IO207NB4F19	AL19
IO207PB4F19	AL20
IO208NB4F19	AG19
IO208PB4F19	AF19
IO209NB4F19	AN18
IO209PB4F19	AP18
IO210NB4F19	AE19
IO210PB4F19	AD19
IO211NB4F19	AL18
IO211PB4F19	AM18
IO212NB4F19/CLKEN	AJ20
IO212PB4F19/CLKEP	AK20
IO213NB4F19/CLKFN	AJ18
IO213PB4F19/CLKFP	AJ19
Bank 5	
IO214NB5F20/CLKGN	AJ16
IO214PB5F20/CLKGP	AJ17
IO215NB5F20/CLKHN	AJ15
IO215PB5F20/CLKHP	AK15
IO216NB5F20	AD16
IO216PB5F20	AE17
IO217NB5F20	AM17
IO217PB5F20	AL17
IO218NB5F20	AG16
IO218PB5F20	AF16
IO219NB5F20	AM16
IO219PB5F20	AL16
IO220NB5F20	AP16
IO220PB5F20	AN16
IO221NB5F20	AN15
IO221PB5F20	AP15
IO222NB5F20	AD15
IO222PB5F20	AE16
IO223NB5F21	AL14
IO223PB5F21	AL15
IO224NB5F21	AN14
IO224PB5F21	AP14
IO225NB5F21	AK13

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO225PB5F21	AK14
IO226NB5F21	AE15
IO226PB5F21	AF15
IO227NB5F21	AG14
IO227PB5F21	AG15
IO228NB5F21	AJ13
IO228PB5F21	AJ14
IO229NB5F21	AM13
IO229PB5F21	AM14
IO230NB5F21	AE14
IO230PB5F21	AF14
IO231NB5F21	AN12
IO231PB5F21	AP12
IO232NB5F21	AG13
IO232PB5F21	AH13
IO233NB5F21	AL12
IO233PB5F21	AL13
IO234NB5F21	AE13
IO234PB5F21	AF13
IO235NB5F22	AN11
IO235PB5F22	AP11
IO236NB5F22	AM11
IO236PB5F22	AM12
IO237NB5F22	AJ11
IO237PB5F22	AJ12
IO238NB5F22	AH11
IO238PB5F22	AH12
IO239NB5F22	AK10
IO239PB5F22	AK11
IO240NB5F22	AE12
IO240PB5F22	AF12
IO241NB5F22	AN10
IO241PB5F22	AP10
IO242NB5F22	AG11
IO242PB5F22	AG12
IO243NB5F22	AL9
IO243PB5F22	AL10
IO244NB5F22	AM8
IO244PB5F22	AM9
IO245NB5F23	AH10
IO245PB5F23	AJ10
IO246NB5F23	AF10
IO246PB5F23	AF11
IO247NB5F23	AJ9

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO247PB5F23	AK9
IO248NB5F23	AN7
IO248PB5F23	AP7
IO249NB5F23	AL7
IO249PB5F23	AL8
IO250NB5F23	AE10
IO250PB5F23	AE11
IO251NB5F23	AK8
IO251PB5F23	AJ8
IO252NB5F23	AH8
IO252PB5F23	AH9
IO253NB5F23	AN6
IO253PB5F23	AP6
IO254NB5F23	AG9
IO254PB5F23	AG10
IO255NB5F23	AJ7
IO255PB5F23	AK7
IO256NB5F23	AL6
IO256PB5F23	AM6
Bank 6	
IO257NB6F24	AG6
IO257PB6F24	AH6
IO258NB6F24	AD9
IO258PB6F24	AE9
IO259NB6F24	AF7
IO259PB6F24	AG7
IO260NB6F24	AH3
IO260PB6F24	AH4
IO261NB6F24	AH5
IO261PB6F24	AJ5
IO262NB6F24	AE6
IO262PB6F24	AF6
IO263NB6F24	AF5
IO263PB6F24	AG5
IO264NB6F24	AD8
IO264PB6F24	AE8
IO265NB6F24	AF3
IO265PB6F24	AG3
IO266NB6F24	AC10
IO266PB6F24	AD10
IO267NB6F25	AD7
IO267PB6F25	AE7
IO268NB6F25	AD5
IO268PB6F25	AE5

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO269NB6F25	AE4
IO269PB6F25	AF4
IO270NB6F25	AB9
IO270PB6F25	AC9
IO271NB6F25	AC6
IO271PB6F25	AD6
IO272NB6F25	AB8
IO272PB6F25	AC8
IO273NB6F25	AE1
IO273PB6F25	AE2
IO274NB6F25	AA10
IO274PB6F25	AB10
IO275NB6F25	AB7
IO275PB6F25	AC7
IO276NB6F25	AD1
IO276PB6F25	AD2
IO277NB6F25	AC4
IO277PB6F25	AC3
IO278NB6F26	AA8
IO278PB6F26	AA9
IO279NB6F26	AB5
IO279PB6F26	AB6
IO280NB6F26	Y10
IO280PB6F26	Y11
IO281NB6F26	AB3
IO281PB6F26	AB4
IO282NB6F26	Y7
IO282PB6F26	AA7
IO283NB6F26	AC2
IO283PB6F26	AC1
IO284NB6F26	Y9
IO284PB6F26	Y8
IO285NB6F26	AA5
IO285PB6F26	AA6
IO286NB6F26	W10
IO286PB6F26	W11
IO287NB6F26	AA3
IO287PB6F26	AA4
IO288NB6F26	W9
IO288PB6F26	W8
IO289NB6F27	AA1
IO289PB6F27	AA2
IO290NB6F27	W6
IO290PB6F27	Y6

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO291NB6F27	W5
IO291PB6F27	Y5
IO292NB6F27	V7
IO292PB6F27	W7
IO293NB6F27	W4
IO293PB6F27	Y4
IO294NB6F27	V10
IO294PB6F27	V11
IO295NB6F27	Y1
IO295PB6F27	Y2
IO296NB6F27	W1
IO296PB6F27	W2
IO297NB6F27	V1
IO297PB6F27	V2
IO298NB6F27	V9
IO298PB6F27	V8
IO299NB6F27	U4
IO299PB6F27	V4
Bank 7	
IO300NB7F28	U10
IO300PB7F28	U11
IO301NB7F28	U2
IO301PB7F28	U1
IO302NB7F28	U6
IO302PB7F28	U7
IO303NB7F28	T3
IO303PB7F28	U3
IO304NB7F28	U9
IO304PB7F28	U8
IO305NB7F28	R2
IO305PB7F28	R1
IO306NB7F28	R4
IO306PB7F28	T4
IO307NB7F28	R5
IO307PB7F28	T5
IO308NB7F28	T11
IO308PB7F28	T10
IO309NB7F28	T6
IO309PB7F28	T7
IO310NB7F29	T9
IO310PB7F29	T8
IO311NB7F29	N3
IO311PB7F29	P3
IO312NB7F29	P7

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO312PB7F29	R7
IO313NB7F29	P6
IO313PB7F29	R6
IO314NB7F29	M2
IO314PB7F29	N2
IO315NB7F29	N4
IO315PB7F29	P4
IO316NB7F29	R9
IO316PB7F29	R8
IO317NB7F29	N5
IO317PB7F29	P5
IO318NB7F29	R10
IO318PB7F29	R11
IO319NB7F29	L2
IO319PB7F29	L1
IO320NB7F29	N8
IO320PB7F29	P8
IO321NB7F30	M6
IO321PB7F30	N6
IO322NB7F30	P10
IO322PB7F30	P9
IO323NB7F30	L3
IO323PB7F30	M3
IO324NB7F30	M7
IO324PB7F30	N7
IO325NB7F30	K2
IO325PB7F30	K1
IO326NB7F30	G2
IO326PB7F30	H2
IO327NB7F30	L6
IO327PB7F30	L5
IO328NB7F30	N10
IO328PB7F30	N9
IO329NB7F30	J4
IO329PB7F30	K4
IO330NB7F30	J5
IO330PB7F30	K5
IO331NB7F30	M10
IO331PB7F30	M9
IO332NB7F31	L8
IO332PB7F31	M8
IO333NB7F31	F2
IO333PB7F31	F1
IO334NB7F31	J6

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
IO334PB7F31	K6
IO335NB7F31	H4
IO335PB7F31	H3
IO336NB7F31	K7
IO336PB7F31	L7
IO337NB7F31	G4
IO337PB7F31	G3
IO338NB7F31	K9
IO338PB7F31	L9
IO339NB7F31	H6
IO339PB7F31	H5
IO340NB7F31	H7
IO340PB7F31	J7
IO341NB7F31	J8
IO341PB7F31	K8
Dedicated I/O	
GND	A13
GND	A2
GND	A22
GND	A27
GND	A3
GND	A31
GND	A32
GND	A33
GND	A4
GND	A8
GND	AA14
GND	AA15
GND	AA16
GND	AA17
GND	AA18
GND	AA19
GND	AA20
GND	AA21
GND	AB1
GND	AB13
GND	AB22
GND	AB34
GND	AC12
GND	AC23
GND	AC30
GND	AC5
GND	AD11
GND	AD24

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
GND	AD31
GND	AD4
GND	AE3
GND	AE32
GND	AF2
GND	AF33
GND	AG1
GND	AG27
GND	AG34
GND	AG8
GND	AH28
GND	AH7
GND	AJ29
GND	AJ6
GND	AK12
GND	AK17
GND	AK18
GND	AK23
GND	AK30
GND	AK5
GND	AL1
GND	AL11
GND	AL2
GND	AL24
GND	AL3
GND	AL31
GND	AL32
GND	AL33
GND	AL34
GND	AL4
GND	AM1
GND	AM10
GND	AM15
GND	AM2
GND	AM20
GND	AM25
GND	AM3
GND	AM31
GND	AM32
GND	AM33
GND	AM34
GND	AM4
GND	AN1
GND	AN2

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
GND	AN26
GND	AN3
GND	AN31
GND	AN32
GND	AN33
GND	AN34
GND	AN4
GND	AN9
GND	AP13
GND	AP2
GND	AP22
GND	AP27
GND	AP3
GND	AP31
GND	AP32
GND	AP33
GND	AP4
GND	AP8
GND	B1
GND	B2
GND	B26
GND	B3
GND	B31
GND	B32
GND	B33
GND	B34
GND	B4
GND	B9
GND	C1
GND	C10
GND	C15
GND	C2
GND	C20
GND	C25
GND	C3
GND	C31
GND	C32
GND	C33
GND	C34
GND	C4
GND	D1
GND	D11
GND	D2
GND	D24

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
GND	D3
GND	D31
GND	D32
GND	D33
GND	D34
GND	D4
GND	E12
GND	E17
GND	E18
GND	E23
GND	E30
GND	E5
GND	F29
GND	F30
GND	F6
GND	G28
GND	G7
GND	H1
GND	H34
GND	J2
GND	J33
GND	K3
GND	K32
GND	L11
GND	L24
GND	L31
GND	L4
GND	M12
GND	M23
GND	M30
GND	M5
GND	N1
GND	N13
GND	N22
GND	N34
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19
GND	P20
GND	P21
GND	R14

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R20
GND	R21
GND	R3
GND	R32
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T20
GND	T21
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	U20
GND	U21
GND	U30
GND	U5
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18
GND	V19
GND	V20
GND	V21
GND	V30
GND	V5
GND	W14
GND	W15
GND	W16
GND	W17
GND	W18
GND	W19
GND	W20

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
GND	W21
GND	Y14
GND	Y15
GND	Y16
GND	Y17
GND	Y18
GND	Y19
GND	Y20
GND	Y21
GND	Y3
GND	Y32
GND/LP	G6
NC	A17
NC	A26
NC	AB2
NC	AB33
NC	AC34
NC	AD3
NC	AD34
NC	AE31
NC	AE33
NC	AE34
NC	AF1
NC	AF34
NC	AG2
NC	AG4
NC	AH1
NC	AH2
NC	AH31
NC	AH32
NC	AH34
NC	AJ1
NC	AJ2
NC	AJ3
NC	AJ31
NC	AJ32
NC	AJ33
NC	AJ34
NC	AJ4
NC	AL29
NC	AM19
NC	AM7
NC	AN13
NC	AN17

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
NC	AN25
NC	AN27
NC	AN8
NC	AP17
NC	AP9
NC	B17
NC	B22
NC	B27
NC	B8
NC	D10
NC	D20
NC	D23
NC	D25
NC	F3
NC	F32
NC	F33
NC	F34
NC	F4
NC	G1
NC	G32
NC	G33
NC	G34
NC	H31
NC	H33
NC	J1
NC	J3
NC	J34
NC	M1
NC	M4
NC	P1
NC	P2
NC	R31
NC	T1
NC	T2
NC	V3
NC	V34
NC	W3
NC	W34
PRA	J17
PRB	F18
PRC	AD18
PRD	AH18
TCK	J9
TDI	F7

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
TDO	L10
TMS	H8
TRST	E6
VCCA	AA13
VCCA	AA22
VCCA	AB14
VCCA	AB15
VCCA	AB16
VCCA	AB17
VCCA	AB18
VCCA	AB19
VCCA	AB20
VCCA	AB21
VCCA	AF8
VCCA	AK28
VCCA	G30
VCCA	G5
VCCA	N14
VCCA	N15
VCCA	N16
VCCA	N17
VCCA	N18
VCCA	N19
VCCA	N20
VCCA	N21
VCCA	P13
VCCA	P22
VCCA	R13
VCCA	R22
VCCA	T13
VCCA	T22
VCCA	U13
VCCA	U22
VCCA	V13
VCCA	V22
VCCA	W13
VCCA	W22
VCCA	Y13
VCCA	Y22
VCCDA	AF26
VCCDA	AF9
VCCDA	AG17
VCCDA	AG18
VCCDA	AH14

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
VCCDA	AH15
VCCDA	AH17
VCCDA	AH20
VCCDA	AH21
VCCDA	AK29
VCCDA	AK6
VCCDA	E15
VCCDA	E29
VCCDA	E7
VCCDA	F15
VCCDA	F21
VCCDA	F5
VCCDA	G20
VCCDA	H17
VCCDA	H18
VCCDA	H28
VCCDA	J18
VCCDA	V27
VCCDA	V6
VCCIB0	A5
VCCIB0	B5
VCCIB0	C5
VCCIB0	D5
VCCIB0	L12
VCCIB0	L13
VCCIB0	L14
VCCIB0	M13
VCCIB0	M14
VCCIB0	M15
VCCIB0	M16
VCCIB0	M17
VCCIB1	A30
VCCIB1	B30
VCCIB1	C30
VCCIB1	D30
VCCIB1	L21
VCCIB1	L22
VCCIB1	L23
VCCIB1	M18
VCCIB1	M19
VCCIB1	M20
VCCIB1	M21
VCCIB1	M22
VCCIB2	E31

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

FG1152	
AX2000 Function	Pin Number
VCCIB2	E32
VCCIB2	E33
VCCIB2	E34
VCCIB2	M24
VCCIB2	N23
VCCIB2	N24
VCCIB2	P23
VCCIB2	P24
VCCIB2	R23
VCCIB2	T23
VCCIB2	U23
VCCIB3	AA23
VCCIB3	AA24
VCCIB3	AB23
VCCIB3	AB24
VCCIB3	AC24
VCCIB3	AK31
VCCIB3	AK32
VCCIB3	AK33
VCCIB3	AK34
VCCIB3	V23
VCCIB3	W23
VCCIB3	Y23
VCCIB4	AC18
VCCIB4	AC19
VCCIB4	AC20
VCCIB4	AC21
VCCIB4	AC22
VCCIB4	AD21
VCCIB4	AD22
VCCIB4	AD23
VCCIB4	AL30
VCCIB4	AM30
VCCIB4	AN30
VCCIB4	AP30
VCCIB5	AC13
VCCIB5	AC14
VCCIB5	AC15
VCCIB5	AC16
VCCIB5	AC17
VCCIB5	AD12
VCCIB5	AD13
VCCIB5	AD14
VCCIB5	AL5

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

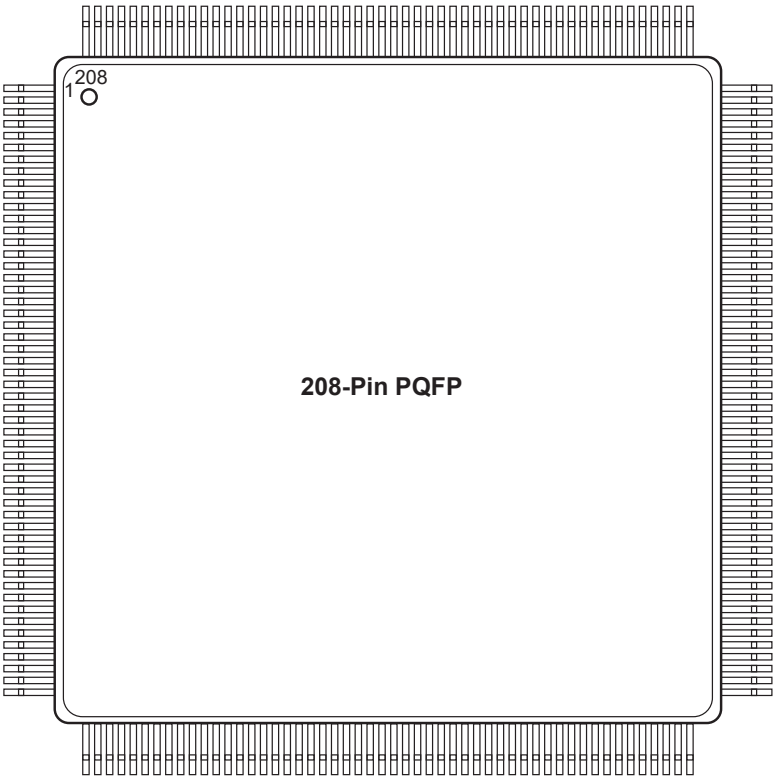
FG1152	
AX2000 Function	Pin Number
VCCIB5	AM5
VCCIB5	AN5
VCCIB5	AP5
VCCIB6	AA11
VCCIB6	AA12
VCCIB6	AB11
VCCIB6	AB12
VCCIB6	AC11
VCCIB6	AK1
VCCIB6	AK2
VCCIB6	AK3
VCCIB6	AK4
VCCIB6	V12
VCCIB6	W12
VCCIB6	Y12
VCCIB7	E1
VCCIB7	E2
VCCIB7	E3
VCCIB7	E4
VCCIB7	M11
VCCIB7	N11
VCCIB7	N12
VCCIB7	P11
VCCIB7	P12
VCCIB7	R12
VCCIB7	T12
VCCIB7	U12
VCCPLA	J16
VCCPLB	K17
VCCPLC	J19
VCCPLD	L18
VCCPLE	AK19
VCCPLF	AE18
VCCPLG	AK16
VCCPLH	AF17
VCOMPLA	H16
VCOMPLB	L17
VCOMPLC	H19
VCOMPLD	K18
VCOMPLE	AH19
VCOMPLF	AF18
VCOMPLG	AH16
VCOMPLH	AD17
VPUMP	J26

© 2024 Microchip Technology Inc. and its subsidiaries

3.8 PQ208

The following figure shows package bottom-view of PQ208.

Figure 3-8. Package Bottom-View



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

The following tables list the IOD interface pin placement.

Table 3-13. Packaging Pin Assignment Table (PPAT)

PQ208	
AX250 Function	Pin Number
Bank 0	
IO02NB0F0	197
IO03NB0F0	198
IO03PB0F0	199
IO12NB0F0/HCLKAN	191
IO12PB0F0/HCLKAP	192
IO13NB0F0/HCLKBN	185
IO13PB0F0/HCLKBP	186
Bank 1	
IO14NB1F1/HCLKCN	180
IO14PB1F1/HCLKCP	181
IO15NB1F1/HCLKDN	174
IO15PB1F1/HCLKDP	175
IO16NB1F1	170

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

PQ208	
AX250 Function	Pin Number
IO16PB1F1	171
IO24NB1F1	165
IO24PB1F1	166
IO26NB1F1	161
IO26PB1F1	162
IO27NB1F1	159
IO27PB1F1	160
Bank 2	
IO29NB2F2	151
IO29PB2F2	153
IO30NB2F2	152
IO30PB2F2	154
IO31PB2F2	148
IO32NB2F2	146
IO32PB2F2	147
IO34NB2F2	144
IO34PB2F2	145
IO39NB2F2	139
IO39PB2F2	140
IO40PB2F2	141
IO41NB2F2	137
IO41PB2F2	138
IO43NB2F2	132
IO43PB2F2	134
IO44NB2F2	131
IO44PB2F2	133
Bank 3	
IO45NB3F3	127
IO45PB3F3	129
IO46NB3F3	126
IO46PB3F3	128
IO48NB3F3	122
IO48PB3F3	123
IO50NB3F3	120
IO50PB3F3	121
IO55NB3F3	116
IO55PB3F3	117
IO57NB3F3	114
IO57PB3F3	115
IO59NB3F3	110
IO59PB3F3	111
IO60NB3F3	108
IO60PB3F3	109
IO61NB3F3	106

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

PQ208	
AX250 Function	Pin Number
IO61PB3F3	107
Bank 4	
IO62NB4F4	100
IO62PB4F4	103
IO63NB4F4	101
IO63PB4F4	102
IO64NB4F4	96
IO64PB4F4	97
IO72NB4F4	91
IO72PB4F4	92
IO74NB4F4/CLKEN	87
IO74PB4F4/CLKEP	88
IO75NB4F4/CLKFN	81
IO75PB4F4/CLKFP	82
Bank 5	
IO76NB5F5/CLKGN	76
IO76PB5F5/CLKGP	77
IO77NB5F5/CLKHN	70
IO77PB5F5/CLKHP	71
IO78NB5F5	66
IO78PB5F5	67
IO86NB5F5	62
IO87NB5F5	60
IO87PB5F5	61
IO88NB5F5	56
IO88PB5F5	57
IO89NB5F5	54
IO89PB5F5	55
Bank 6	
IO91NB6F6	47
IO91PB6F6	49
IO92NB6F6	48
IO92PB6F6	50
IO93NB6F6	42
IO93PB6F6	43
IO94PB6F6	44
IO96NB6F6	40
IO96PB6F6	41
IO101NB6F6	35
IO101PB6F6	36
IO102PB6F6	37
IO103NB6F6	33
IO103PB6F6	34
IO105NB6F6	28

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

PQ208	
AX250 Function	Pin Number
IO105PB6F6	30
IO106NB6F6	27
IO106PB6F6	29
Bank 7	
IO107NB7F7	23
IO107PB7F7	25
IO108NB7F7	22
IO108PB7F7	24
IO110NB7F7	18
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

PQ208	
AX250 Function	Pin Number
GND	69
GND	90
GND	94
GND	99
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	52
VCCA	156
VCCA	14
VCCA	38
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	168
VCCA	195
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

PQ208	
AX250 Function	Pin Number
VCCPLG	74
VCCPLH	72
VCCIB0	193
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

Table 3-14. Packaging Pin Assignment Table (PPAT)

PQ208	
AX500 Function	Pin Number
Bank 0	
IO03NB0F0	198
IO03PB0F0	199
IO04NB0F0	197
IO19NB0F1/HCLKAN	191
IO19PB0F1/HCLKAP	192
IO20NB0F1/HCLKBN	185
IO20PB0F1/HCLKBP	186
Bank 1	
IO21NB1F2/HCLKCN	180
IO21PB1F2/HCLKCP	181
IO22NB1F2/HCLKDN	174
IO22PB1F2/HCLKDP	175

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

PQ208	
AX500 Function	Pin Number
IO23NB1F2	170
IO23PB1F2	171
IO37NB1F3	165
IO37PB1F3	166
IO39NB1F3	161
IO39PB1F3	162
IO41NB1F3	159
IO41PB1F3	160
Bank 2	
IO43NB2F4	151
IO43PB2F4	153
IO44NB2F4	152
IO44PB2F4	154
IO45PB2F4	148
IO46NB2F4	146
IO46PB2F4	147
IO48NB2F4	144
IO48PB2F4	145
IO57NB2F5	139
IO57PB2F5	140
IO58PB2F5	141
IO59NB2F5	137
IO59PB2F5	138
IO61NB2F5	132
IO61PB2F5	134
IO62NB2F5	131
IO62PB2F5	133
Bank 3	
IO63NB3F6	127
IO63PB3F6	129
IO64NB3F6	126
IO64PB3F6	128
IO66NB3F6	122
IO66PB3F6	123
IO68NB3F6	120
IO68PB3F6	121
IO77NB3F7	116
IO77PB3F7	117
IO79NB3F7	114
IO79PB3F7	115
IO81NB3F7	110
IO81PB3F7	111
IO82NB3F7	108
IO82PB3F7	109

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

PQ208	
AX500 Function	Pin Number
IO83NB3F7	106
IO83PB3F7	107
Bank 4	
IO84PB4F8	103
IO85NB4F8	100
IO86NB4F8	101
IO86PB4F8	102
IO87NB4F8	96
IO87PB4F8	97
IO101NB4F9	91
IO101PB4F9	92
IO103NB4F9/CLKEN	87
IO103PB4F9/CLKEP	88
IO104NB4F9/CLKFN	81
IO104PB4F9/CLKFP	82
Bank 5	
IO105NB5F10/CLKGN	76
IO105PB5F10/CLKGP	77
IO106NB5F10/CLKHN	70
IO106PB5F10/CLKHP	71
IO107NB5F10	66
IO107PB5F10	67
IO119NB5F11	62
IO121NB5F11	60
IO121PB5F11	61
IO123NB5F11	56
IO123PB5F11	57
IO125NB5F11	54
IO125PB5F11	55
Bank 6	
IO127NB6F12	47
IO127PB6F12	49
IO128NB6F12	48
IO128PB6F12	50
IO129NB6F12	42
IO129PB6F12	43
IO130PB6F12	44
IO132NB6F12	40
IO132PB6F12	41
IO141NB6F13	35
IO141PB6F13	36
IO142PB6F13	37
IO143NB6F13	33
IO143PB6F13	34

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

PQ208	
AX500 Function	Pin Number
IO145NB6F13	28
IO145PB6F13	30
IO146NB6F13	27
IO146PB6F13	29
Bank 7	
IO147NB7F14	23
IO147PB7F14	25
IO148NB7F14	22
IO148PB7F14	24
IO150NB7F14	18
IO150PB7F14	19
IO152NB7F14	16
IO152PB7F14	17
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165PB7F15	7
IO166NB7F15	5
IO166PB7F15	6
IO167NB7F15	3
IO167PB7F15	4
Dedicated I/O	
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
GND	104
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

PQ208	
AX500 Function	Pin Number
GND	65
GND	69
GND	90
GND	94
GND	99
GND	113
GND	119
GND	125
GND	143
GND	136
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

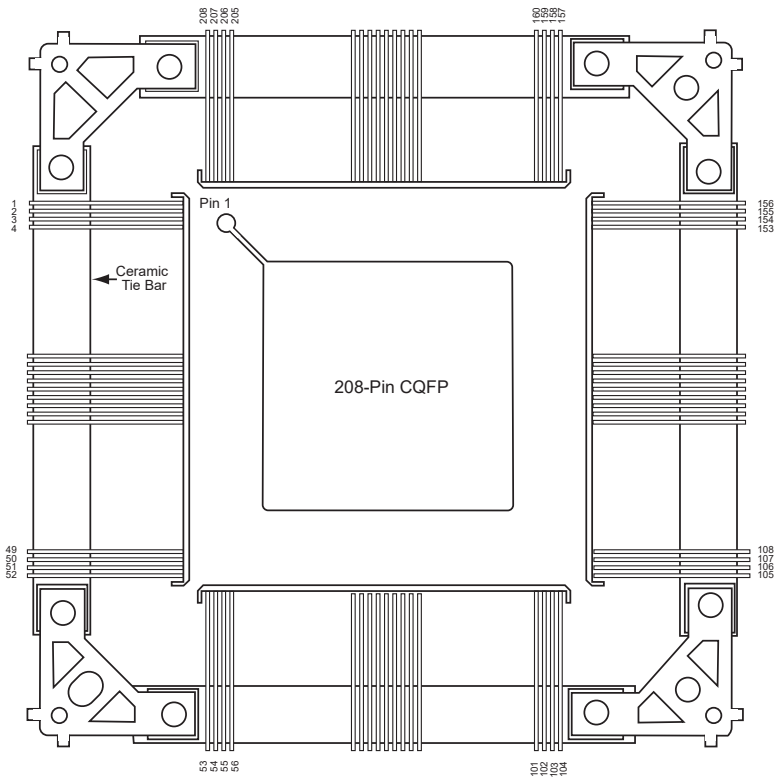
PQ208	
AX500 Function	Pin Number
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCCIB0	200
VCCIB0	193
VCCIB1	172
VCCIB1	163
VCCIB2	149
VCCIB2	135
VCCIB3	124
VCCIB3	112
VCCIB4	98
VCCIB4	89
VCCIB5	68
VCCIB5	58
VCCIB6	45
VCCIB6	31
VCCIB7	20
VCCIB7	8
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

3.9 CQ208

The following figure shows package bottom-view of CQ208.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 3-9. Package Bottom-View



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

The following tables list the IOD interface pin placement.

Table 3-15. Packaging Pin Assignment Table (PPAT)

CQ208	
AX250 Function	Pin Number
Bank 0	
IO02NB0F0	197
IO03NB0F0	198
IO03PB0F0	199
IO12NB0F0/HCLKAN	191
IO12PB0F0/HCLKAP	192
IO13NB0F0/HCLKBN	185
IO13PB0F0/HCLKBP	186
Bank 1	
IO14NB1F1/HCLKCN	180
IO14PB1F1/HCLKCP	181
IO15NB1F1/HCLKDN	174
IO15PB1F1/HCLKDP	175
IO16NB1F1	170
IO16PB1F1	171
IO24NB1F1	165
IO24PB1F1	166

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ208	
AX250 Function	Pin Number
IO26NB1F1	161
IO26PB1F1	162
IO27NB1F1	159
IO27PB1F1	160
Bank 2	
IO29NB2F2	151
IO29PB2F2	153
IO30NB2F2	152
IO30PB2F2	154
IO31PB2F2	148
IO32NB2F2	146
IO32PB2F2	147
IO34NB2F2	144
IO34PB2F2	145
IO39NB2F2	139
IO39PB2F2	140
IO40PB2F2	141
IO41NB2F2	137
IO41PB2F2	138
IO43NB2F2	132
IO43PB2F2	134
IO44NB2F2	131
IO44PB2F2	133
Bank 3	
IO45NB3F3	127
IO45PB3F3	129
IO46NB3F3	126
IO46PB3F3	128
IO48NB3F3	122
IO48PB3F3	123
IO50NB3F3	120
IO50PB3F3	121
IO55NB3F3	116
IO55PB3F3	117
IO57NB3F3	114
IO57PB3F3	115
IO59NB3F3	110
IO59PB3F3	111
IO60NB3F3	108
IO60PB3F3	109
IO61NB3F3	106
IO61PB3F3	107
Bank 4	
IO62NB4F4	100

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ208	
AX250 Function	Pin Number
IO62PB4F4	103
IO63NB4F4	101
IO63PB4F4	102
IO64NB4F4	96
IO64PB4F4	97
IO72NB4F4	91
IO72PB4F4	92
IO74NB4F4/CLKEN	87
IO74PB4F4/CLKEP	88
IO75NB4F4/CLKFN	81
IO75PB4F4/CLKFP	82
Bank 5	
IO76NB5F5/CLKGN	76
IO76PB5F5/CLKGP	77
IO77NB5F5/CLKHN	70
IO77PB5F5/CLKHP	71
IO78NB5F5	66
IO78PB5F5	67
IO86NB5F5	62
IO87NB5F5	60
IO87PB5F5	61
IO88NB5F5	56
IO88PB5F5	57
IO89NB5F5	54
IO89PB5F5	55
Bank 6	
IO91NB6F6	47
IO91PB6F6	49
IO92NB6F6	48
IO92PB6F6	50
IO93NB6F6	42
IO93PB6F6	43
IO94PB6F6	44
IO96NB6F6	40
IO96PB6F6	41
IO101NB6F6	35
IO101PB6F6	36
IO102PB6F6	37
IO103NB6F6	33
IO103PB6F6	34
IO105NB6F6	28
IO105PB6F6	30
IO106NB6F6	27
IO106PB6F6	29

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ208	
AX250 Function	Pin Number
Bank 7	
IO107NB7F7	23
IO107PB7F7	25
IO108NB7F7	22
IO108PB7F7	24
IO110NB7F7	18
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173
GND	194

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ208	
AX250 Function	Pin Number
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	1
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124
VCCIB4	89

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ208	
AX250 Function	Pin Number
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

Table 3-16. Packaging Pin Assignment Table (PPAT)

CQ208	
AX500 Function	Pin Number
Bank 0	
IO03NB0F0	198
IO03PB0F0	199
IO04NB0F0	197
IO19NB0F1/HCLKAN	191
IO19PB0F1/HCLKAP	192
IO20NB0F1/HCLKBN	185
IO20PB0F1/HCLKBP	186
Bank 1	
IO21NB1F2/HCLKCN	180
IO21PB1F2/HCLKCP	181
IO22NB1F2/HCLKDN	174
IO22PB1F2/HCLKDP	175
IO23NB1F2	170
IO23PB1F2	171
IO37NB1F3	165

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ208	
AX500 Function	Pin Number
IO37PB1F3	166
IO39NB1F3	161
IO39PB1F3	162
IO41NB1F3	159
IO41PB1F3	160
Bank 2	
IO43NB2F4	151
IO43PB2F4	153
IO44NB2F4	152
IO44PB2F4	154
IO45PB2F4	148
IO46NB2F4	146
IO46PB2F4	147
IO48NB2F4	144
IO48PB2F4	145
IO57NB2F5	139
IO57PB2F5	140
IO58PB2F5	141
IO59NB2F5	137
IO59PB2F5	138
IO61NB2F5	132
IO61PB2F5	134
IO62NB2F5	131
IO62PB2F5	133
Bank 3	
IO63NB3F6	127
IO63PB3F6	129
IO64NB3F6	126
IO64PB3F6	128
IO66NB3F6	122
IO66PB3F6	123
IO68NB3F6	120
IO68PB3F6	121
IO77NB3F7	116
IO77PB3F7	117
IO79NB3F7	114
IO79PB3F7	115
IO81NB3F7	110
IO81PB3F7	111
IO82NB3F7	108
IO82PB3F7	109
IO83NB3F7	106
IO83PB3F7	107
Bank 4	

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ208	
AX500 Function	Pin Number
IO84PB4F8	103
IO85NB4F8	100
IO86NB4F8	101
IO86PB4F8	102
IO87NB4F8	96
IO87PB4F8	97
IO101NB4F9	91
IO101PB4F9	92
IO103NB4F9/CLKEN	87
IO103PB4F9/CLKEP	88
IO104NB4F9/CLKFN	81
IO104PB4F9/CLKFP	82
Bank 5	
IO105NB5F10/CLKGN	76
IO105PB5F10/CLKGP	77
IO106NB5F10/CLKHN	70
IO106PB5F10/CLKHP	71
IO107NB5F10	66
IO107PB5F10	67
IO119NB5F11	62
IO121NB5F11	60
IO121PB5F11	61
IO123NB5F11	56
IO123PB5F11	57
IO125NB5F11	54
IO125PB5F11	55
Bank 6	
IO127NB6F12	47
IO127PB6F12	49
IO128NB6F12	48
IO128PB6F12	50
IO129NB6F12	42
IO129PB6F12	43
IO130PB6F12	44
IO132NB6F12	40
IO132PB6F12	41
IO141NB6F13	35
IO141PB6F13	36
IO142PB6F13	37
IO143NB6F13	33
IO143PB6F13	34
IO145NB6F13	28
IO145PB6F13	30
IO146NB6F13	27

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ208	
AX500 Function	Pin Number
IO146PB6F13	29
Bank 7	
IO147NB7F14	23
IO147PB7F14	25
IO148NB7F14	22
IO148PB7F14	24
IO150NB7F14	18
IO150PB7F14	19
IO152NB7F14	16
IO152PB7F14	17
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165PB7F15	7
IO166NB7F15	5
IO166PB7F15	6
IO167NB7F15	3
IO167PB7F15	4
Dedicated I/O	
VCCDA	1
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ208	
AX500 Function	Pin Number
GND	173
GND	194
GND	196
GND	201
GND/LP	208
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
VCCA	2
VCCA	14
VCCA	38
VCCA	52
VCCA	64
VCCA	93
VCCA	118
VCCA	142
VCCA	156
VCCA	168
VCCA	195
VCCDA	26
VCCDA	53
VCCDA	63
VCCDA	78
VCCDA	95
VCCDA	105
VCCDA	130
VCCDA	157
VCCDA	167
VCCDA	182
VCCDA	202
VCCIB0	193
VCCIB0	200
VCCIB1	163
VCCIB1	172
VCCIB2	135
VCCIB2	149
VCCIB3	112
VCCIB3	124

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

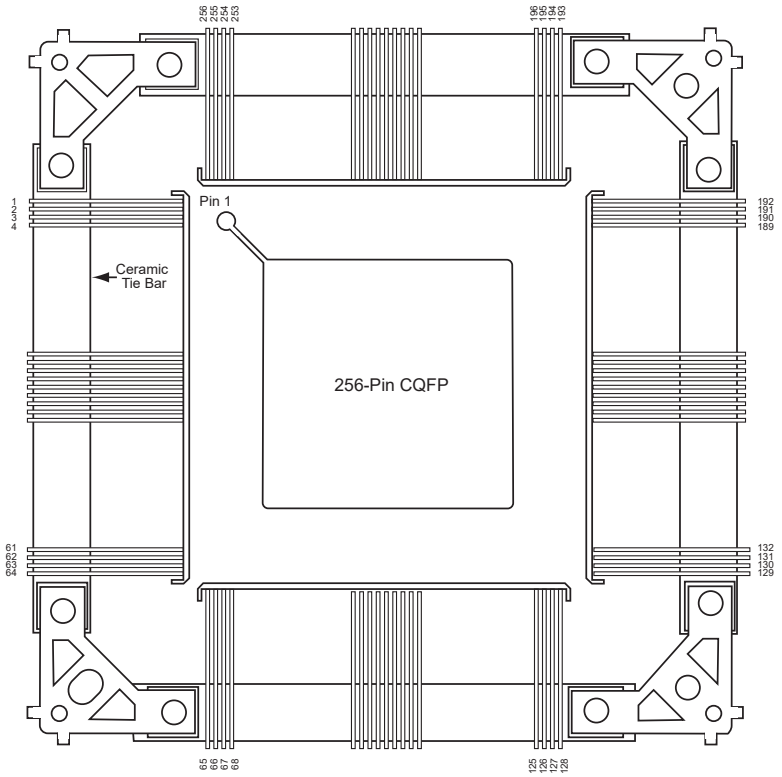
CQ208	
AX500 Function	Pin Number
VCCIB4	89
VCCIB4	98
VCCIB5	58
VCCIB5	68
VCCIB6	31
VCCIB6	45
VCCIB7	8
VCCIB7	20
VCCPLA	189
VCCPLB	187
VCCPLC	178
VCCPLD	176
VCCPLE	85
VCCPLF	83
VCCPLG	74
VCCPLH	72
VCOMPLA	190
VCOMPLB	188
VCOMPLC	179
VCOMPLD	177
VCOMPLE	86
VCOMPLF	84
VCOMPLG	75
VCOMPLH	73
VPUMP	158

3.10 CQ256

The following figure shows package bottom-view of CQ256.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 3-10. Package Bottom-View



Note: For Package Manufacturing and Environmental information, visit the Resource center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

The following table lists the IOD interface pin placement.

Table 3-17. Packaging Pin Assignment Table (PPAT)

CQ256	
AX2000 Function	Pin Number
Bank 0	
IO01NB0F0	248
IO01PB0F0	249
IO04NB0F0	246
IO04PB0F0	247
IO05NB0F0	242
IO05PB0F0	243
IO08NB0F0	240
IO08PB0F0	241
IO37NB0F3	234
IO37PB0F3	235
IO41NB0F3/HCLKAN	232
IO41PB0F3/HCLKAP	233
IO42NB0F3/HCLKBN	228
IO42PB0F3/HCLKBP	229
Bank 1	
IO43NB1F4/HCLKCN	220

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ256	
AX2000 Function	Pin Number
IO43PB1F4/HCLKCP	221
IO44NB1F4/HCLKDN	216
IO44PB1F4/HCLKDP	217
IO65NB1F6	210
IO65PB1F6	211
IO69NB1F6	208
IO69PB1F6	209
IO70NB1F6	199
IO71NB1F6	204
IO71PB1F6	205
IO73NB1F6	202
IO73PB1F6	203
IO74NB1F6	197
IO74PB1F6	198
Bank 2	
IO87NB2F8	187
IO87PB2F8	188
IO89PB2F8	186
IO107NB2F10	184
IO107PB2F10	185
IO110NB2F10	180
IO110PB2F10	181
IO111NB2F10	178
IO111PB2F10	179
IO112NB2F10	174
IO112PB2F10	175
IO113NB2F10	172
IO113PB2F10	173
IO114NB2F10	168
IO114PB2F10	169
IO115NB2F10	166
IO115PB2F10	167
IO117NB2F10	162
IO117PB2F10	163
Bank 3	
IO139NB3F13	158
IO139PB3F13	159
IO141NB3F13	154
IO141PB3F13	155
IO142NB3F13	152
IO142PB3F13	153
IO145NB3F13	148
IO145PB3F13	149
IO146NB3F13	146

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ256	
AX2000 Function	Pin Number
IO146PB3F13	147
IO147NB3F13	140
IO147PB3F13	141
IO148NB3F13	142
IO148PB3F13	143
IO149NB3F13	136
IO149PB3F13	137
IO165NB3F15	135
IO167NB3F15	133
IO167PB3F15	134
Bank 4	
IO181NB4F17	124
IO181PB4F17	125
IO182NB4F17	122
IO182PB4F17	123
IO183NB4F17	118
IO183PB4F17	119
IO184NB4F17	116
IO184PB4F17	117
IO190NB4F17	112
IO190PB4F17	113
IO192NB4F17	110
IO192PB4F17	111
IO212NB4F19/CLKEN	104
IO212PB4F19/CLKEP	105
IO213NB4F19/CLKFN	100
IO213PB4F19/CLKFP	101
Bank 5	
IO214NB5F20/CLKGN	92
IO214PB5F20/CLKGP	93
IO215NB5F20/CLKHN	88
IO215PB5F20/CLKHP	89
IO236NB5F22	82
IO236PB5F22	83
IO238NB5F22	80
IO238PB5F22	81
IO240NB5F22	76
IO240PB5F22	77
IO242NB5F22	74
IO242PB5F22	75
IO243NB5F22	70
IO243PB5F22	71
IO244NB5F22	68
IO244PB5F22	69

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ256	
AX2000 Function	Pin Number
Bank 6	
IO257PB6F24	60
IO258NB6F24	58
IO258PB6F24	59
IO279NB6F26	56
IO279PB6F26	57
IO280NB6F26	52
IO280PB6F26	53
IO281NB6F26	50
IO281PB6F26	51
IO282NB6F26	46
IO282PB6F26	47
IO284NB6F26	44
IO284PB6F26	45
IO285NB6F26	40
IO285PB6F26	41
IO286NB6F26	38
IO286PB6F26	39
IO287NB6F26	34
IO287PB6F26	35
Bank 7	
IO310NB7F29	30
IO310PB7F29	31
IO311NB7F29	26
IO311PB7F29	27
IO312NB7F29	24
IO312PB7F29	25
IO315NB7F29	20
IO315PB7F29	21
IO316NB7F29	18
IO316PB7F29	19
IO317NB7F29	14
IO317PB7F29	15
IO318NB7F29	12
IO318PB7F29	13
IO320NB7F29	8
IO320PB7F29	9
IO341NB7F31	6
IO341PB7F31	7
Dedicated I/O	
GND	1
GND	5
GND	11
GND	17

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ256	
AX2000 Function	Pin Number
GND	23
GND	29
GND	33
GND	37
GND	43
GND	49
GND	55
GND	62
GND	64
GND	65
GND	73
GND	79
GND	85
GND	91
GND	97
GND	103
GND	109
GND	115
GND	121
GND	128
GND	129
GND	132
GND	139
GND	145
GND	151
GND	157
GND	161
GND	165
GND	171
GND	177
GND	183
GND	190
GND	192
GND	193
GND	201
GND	207
GND	213
GND	219
GND	225
GND	231
GND	239
GND	245
GND	256
PRA	227

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ256	
AX2000 Function	Pin Number
PRB	226
PRC	99
PRD	98
TCK	253
TDI	252
TDO	250
TMS	254
TRST	255
VCCA	3
VCCA	4
VCCA	22
VCCA	42
VCCA	61
VCCA	63
VCCA	84
VCCA	108
VCCA	127
VCCA	131
VCCA	150
VCCA	170
VCCA	189
VCCA	191
VCCA	212
VCCA	238
VCCDA	2
VCCDA	32
VCCDA	66
VCCDA	67
VCCDA	86
VCCDA	87
VCCDA	94
VCCDA	95
VCCDA	96
VCCDA	106
VCCDA	107
VCCDA	126
VCCDA	130
VCCDA	160
VCCDA	194
VCCDA	196
VCCDA	214
VCCDA	215
VCCDA	222
VCCDA	223

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

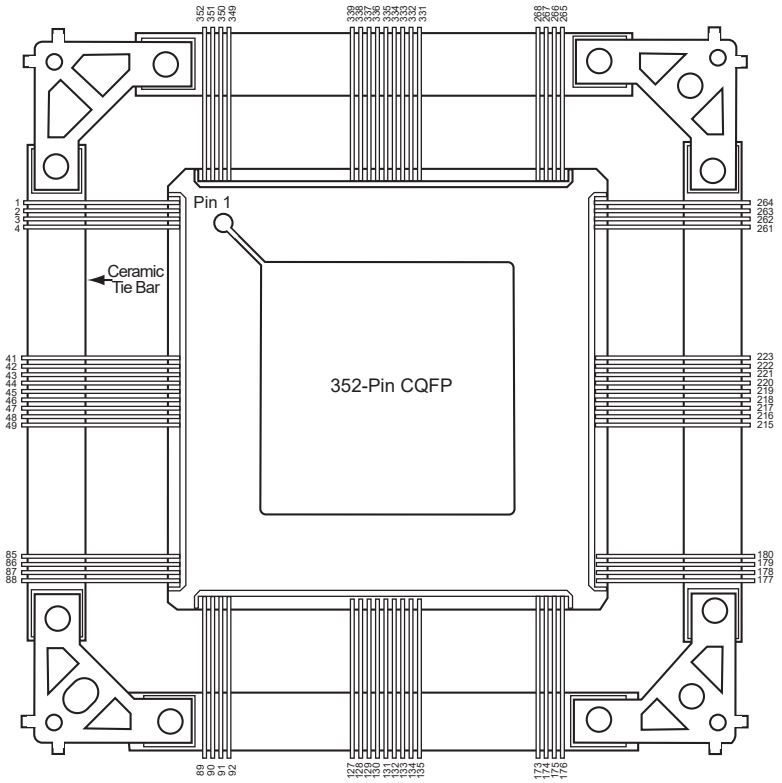
CQ256	
AX2000 Function	Pin Number
VCCDA	224
VCCDA	236
VCCDA	237
VCCDA	251
VCCIB0	230
VCCIB0	244
VCCIB1	200
VCCIB1	206
VCCIB1	218
VCCIB2	164
VCCIB2	176
VCCIB2	182
VCCIB3	138
VCCIB3	144
VCCIB3	156
VCCIB4	102
VCCIB4	114
VCCIB4	120
VCCIB5	72
VCCIB5	78
VCCIB5	90
VCCIB6	36
VCCIB6	48
VCCIB6	54
VCCIB7	10
VCCIB7	16
VCCIB7	28
VPUMP	195

3.11 CQ352

The following figure shows package bottom-view of CQ352.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 3-11. Package Bottom-View



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

The following tables list the IOD interface pin placement.

Table 3-18. Packaging Pin Assignment Table (PPAT)

CQ352	
AX250 Function	Pin Number
Bank 0	
IO00NB0F0	341
IO00PB0F0	342
IO01NB0F0	343
IO02NB0F0	337
IO02PB0F0	338
IO04NB0F0	335
IO04PB0F0	336
IO06NB0F0	331
IO06PB0F0	332
IO08NB0F0	325
IO08PB0F0	326
IO10NB0F0	323
IO10PB0F0	324
IO12NB0F0/HCLKAN	319
IO12PB0F0/HCLKAP	320
IO13NB0F0/HCLKBN	313

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX250 Function	Pin Number
IO13PB0F0/HCLKBP	314
Bank 1	
IO14NB1F1/HCLKCN	305
IO14PB1F1/HCLKCP	306
IO15NB1F1/HCLKDN	299
IO15PB1F1/HCLKDP	300
IO16NB1F1	289
IO16PB1F1	290
IO17NB1F1	295
IO17PB1F1	296
IO18NB1F1	287
IO18PB1F1	288
IO20NB1F1	283
IO20PB1F1	284
IO22NB1F1	277
IO22PB1F1	278
IO23NB1F1	281
IO23PB1F1	282
IO24NB1F1	275
IO24PB1F1	276
IO25NB1F1	271
IO25PB1F1	272
IO27NB1F1	269
IO27PB1F1	270
Bank 2	
IO29NB2F2	261
IO29PB2F2	262
IO30NB2F2	259
IO30PB2F2	260
IO31NB2F2	255
IO31PB2F2	256
IO33NB2F2	249
IO33PB2F2	250
IO34NB2F2	253
IO34PB2F2	254
IO35NB2F2	247
IO35PB2F2	248
IO36NB2F2	243
IO36PB2F2	244
IO37NB2F2	241
IO37PB2F2	242
IO38NB2F2	237
IO38PB2F2	238
IO39NB2F2	235

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX250 Function	Pin Number
IO39PB2F2	236
IO41NB2F2	231
IO41PB2F2	232
IO42NB2F2	229
IO42PB2F2	230
IO43NB2F2	225
IO43PB2F2	226
IO44NB2F2	223
IO44PB2F2	224
Bank 3	
IO45NB3F3	217
IO45PB3F3	218
IO46NB3F3	219
IO46PB3F3	220
IO47NB3F3	213
IO47PB3F3	214
IO48NB3F3	211
IO48PB3F3	212
IO49NB3F3	207
IO49PB3F3	208
IO51NB3F3	205
IO51PB3F3	206
IO52NB3F3	201
IO52PB3F3	202
IO53NB3F3	199
IO53PB3F3	200
IO54NB3F3	195
IO54PB3F3	196
IO55NB3F3	193
IO55PB3F3	194
IO56NB3F3	187
IO56PB3F3	188
IO57NB3F3	189
IO57PB3F3	190
IO59NB3F3	183
IO59PB3F3	184
IO60NB3F3	181
IO60PB3F3	182
IO61NB3F3	179
IO61PB3F3	180
Bank 4	
IO62NB4F4	172
IO62PB4F4	173
IO64NB4F4	166

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX250 Function	Pin Number
IO64PB4F4	167
IO65NB4F4	170
IO65PB4F4	171
IO66NB4F4	164
IO66PB4F4	165
IO67NB4F4	160
IO67PB4F4	161
IO68NB4F4	158
IO68PB4F4	159
IO70NB4F4	154
IO70PB4F4	155
IO72NB4F4	152
IO72PB4F4	153
IO73NB4F4	146
IO73PB4F4	147
IO74NB4F4/CLKEN	142
IO74PB4F4/CLKEP	143
IO75NB4F4/CLKFN	136
IO75PB4F4/CLKFP	137
Bank 5	
IO76NB5F5/CLKGN	128
IO76PB5F5/CLKGP	129
IO77NB5F5/CLKHN	122
IO77PB5F5/CLKHP	123
IO78NB5F5	112
IO78PB5F5	113
IO79NB5F5	118
IO79PB5F5	119
IO80NB5F5	110
IO80PB5F5	111
IO82NB5F5	106
IO82PB5F5	107
IO84NB5F5	100
IO84PB5F5	101
IO85NB5F5	104
IO85PB5F5	105
IO86NB5F5	98
IO86PB5F5	99
IO87NB5F5	94
IO87PB5F5	95
IO89NB5F5	92
IO89PB5F5	93
Bank 6	
IO90PB6F6	86

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX250 Function	Pin Number
IO91NB6F6	84
IO91PB6F6	85
IO92NB6F6	78
IO92PB6F6	79
IO93NB6F6	82
IO93PB6F6	83
IO95NB6F6	76
IO95PB6F6	77
IO96NB6F6	72
IO96PB6F6	73
IO97NB6F6	70
IO97PB6F6	71
IO98NB6F6	66
IO98PB6F6	67
IO99NB6F6	64
IO99PB6F6	65
IO100NB6F6	60
IO100PB6F6	61
IO101NB6F6	58
IO101PB6F6	59
IO103NB6F6	54
IO103PB6F6	55
IO104NB6F6	52
IO104PB6F6	53
IO105NB6F6	48
IO105PB6F6	49
IO106NB6F6	46
IO106PB6F6	47
Bank 7	
IO107NB7F7	40
IO107PB7F7	41
IO108NB7F7	42
IO108PB7F7	43
IO109NB7F7	36
IO109PB7F7	37
IO110NB7F7	34
IO110PB7F7	35
IO111NB7F7	30
IO111PB7F7	31
IO113NB7F7	28
IO113PB7F7	29
IO114NB7F7	24
IO114PB7F7	25
IO115NB7F7	22

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX250 Function	Pin Number
IO115PB7F7	23
IO116NB7F7	18
IO116PB7F7	19
IO117NB7F7	16
IO117PB7F7	17
IO118NB7F7	12
IO118PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121NB7F7	6
IO121PB7F7	7
IO123NB7F7	4
IO123PB7F7	5
Dedicated I/O	
GND	1
GND	9
GND	15
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX250 Function	Pin Number
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330
GND	334
GND	340
GND	345
GND	352
NC	91
NC	117
NC	130
NC	131
NC	148
NC	174
NC	268
NC	294
NC	307
NC	308
NC	327
NC	328
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349
TDI	348

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX250 Function	Pin Number
TDO	347
TMS	350
TRST	351
VCCA	3
VCCA	14
VCCA	32
VCCA	56
VCCA	74
VCCA	87
VCCA	102
VCCA	114
VCCA	150
VCCA	162
VCCA	175
VCCA	191
VCCA	209
VCCA	233
VCCA	251
VCCA	263
VCCA	279
VCCA	291
VCCA	329
VCCA	339
VCCDA	2
VCCDA	44
VCCDA	90
VCCDA	116
VCCDA	132
VCCDA	149
VCCDA	178
VCCDA	221
VCCDA	266
VCCDA	293
VCCDA	309
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX250 Function	Pin Number
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

Table 3-19. Packaging Pin Assignment Table (PPAT)

CQ352	
AX500 Function	Pin Number
Bank 0	
IO00PB0F0	343
IO03NB0F0	341

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX500 Function	Pin Number
IO03PB0F0	342
IO05NB0F0	337
IO05PB0F0	338
IO07NB0F0	335
IO07PB0F0	336
IO09NB0F0	331
IO09PB0F0	332
IO15NB0F1	325
IO15PB0F1	326
IO17NB0F1	323
IO17PB0F1	324
IO19NB0F1/HCLKAN	319
IO19PB0F1/HCLKAP	320
IO20NB0F1/HCLKBN	313
IO20PB0F1/HCLKBP	314
Bank 1	
IO21NB1F2/HCLKCN	305
IO21PB1F2/HCLKCP	306
IO22NB1F2/HCLKDN	299
IO22PB1F2/HCLKDP	300
IO23NB1F2	289
IO23PB1F2	290
IO24NB1F2	295
IO24PB1F2	296
IO25NB1F2	287
IO25PB1F2	288
IO27NB1F2	283
IO27PB1F2	284
IO29NB1F2	281
IO29PB1F2	282
IO31NB1F2	277
IO31PB1F2	278
IO35NB1F3	275
IO35PB1F3	276
IO37NB1F3	271
IO37PB1F3	272
IO41NB1F3	269
IO41PB1F3	270
Bank 2	
IO43NB2F4	261
IO43PB2F4	262
IO45NB2F4	259
IO45PB2F4	260
IO47NB2F4	255

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX500 Function	Pin Number
IO47PB2F4	256
IO49NB2F4	253
IO49PB2F4	254
IO50NB2F4	247
IO50PB2F4	248
IO51NB2F4	249
IO51PB2F4	250
IO53NB2F5	243
IO53PB2F5	244
IO54NB2F5	241
IO54PB2F5	242
IO55NB2F5	237
IO55PB2F5	238
IO57NB2F5	235
IO57PB2F5	236
IO58NB2F5	231
IO58PB2F5	232
IO59NB2F5	229
IO59PB2F5	230
IO61NB2F5	225
IO61PB2F5	226
IO62NB2F5	223
IO62PB2F5	224
Bank 3	
IO63NB3F6	217
IO63PB3F6	218
IO64NB3F6	219
IO64PB3F6	220
IO65NB3F6	213
IO65PB3F6	214
IO67NB3F6	207
IO67PB3F6	208
IO68NB3F6	211
IO68PB3F6	212
IO69NB3F6	205
IO69PB3F6	206
IO71NB3F6	201
IO71PB3F6	202
IO73NB3F6	199
IO73PB3F6	200
IO75NB3F7	193
IO75PB3F7	194
IO76NB3F7	195
IO76PB3F7	196

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX500 Function	Pin Number
IO77NB3F7	189
IO77PB3F7	190
IO79NB3F7	187
IO79PB3F7	188
IO80NB3F7	183
IO80PB3F7	184
IO81NB3F7	181
IO81PB3F7	182
IO83NB3F7	179
IO83PB3F7	180
Bank 4	
IO85NB4F8	172
IO85PB4F8	173
IO87NB4F8	170
IO87PB4F8	171
IO89NB4F8	166
IO89PB4F8	167
IO94NB4F9	164
IO94PB4F9	165
IO95NB4F9	160
IO95PB4F9	161
IO97NB4F9	158
IO97PB4F9	159
IO99NB4F9	154
IO99PB4F9	155
IO100NB4F9	146
IO100PB4F9	147
IO101NB4F9	152
IO101PB4F9	153
IO103NB4F9/CLKEN	142
IO103PB4F9/CLKEP	143
IO104NB4F9/CLKFN	136
IO104PB4F9/CLKFP	137
Bank 5	
IO105NB5F10/CLKGN	128
IO105PB5F10/CLKGP	129
IO106NB5F10/CLKHN	122
IO106PB5F10/CLKHP	123
IO107NB5F10	118
IO107PB5F10	119
IO114NB5F11	112
IO114PB5F11	113
IO115NB5F11	110
IO115PB5F11	111

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX500 Function	Pin Number
IO116NB5F11	106
IO116PB5F11	107
IO117NB5F11	104
IO117PB5F11	105
IO119NB5F11	100
IO119PB5F11	101
IO121NB5F11	98
IO121PB5F11	99
IO123NB5F11	94
IO123PB5F11	95
IO125NB5F11	92
IO125PB5F11	93
Bank 6	
IO126PB6F12	86
IO127NB6F12	84
IO127PB6F12	85
IO129NB6F12	82
IO129PB6F12	83
IO131NB6F12	78
IO131PB6F12	79
IO133NB6F12	76
IO133PB6F12	77
IO134NB6F12	72
IO134PB6F12	73
IO135NB6F12	70
IO135PB6F12	71
IO137NB6F13	66
IO137PB6F13	67
IO138NB6F13	64
IO138PB6F13	65
IO139NB6F13	60
IO139PB6F13	61
IO141NB6F13	54
IO141PB6F13	55
IO142NB6F13	58
IO142PB6F13	59
IO143NB6F13	52
IO143PB6F13	53
IO145NB6F13	48
IO145PB6F13	49
IO146NB6F13	46
IO146PB6F13	47
Bank 7	
IO147NB7F14	40

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX500 Function	Pin Number
IO147PB7F14	41
IO148NB7F14	42
IO148PB7F14	43
IO149NB7F14	36
IO149PB7F14	37
IO151NB7F14	30
IO151PB7F14	31
IO152NB7F14	34
IO152PB7F14	35
IO153NB7F14	28
IO153PB7F14	29
IO155NB7F14	24
IO155PB7F14	25
IO157NB7F14	22
IO157PB7F14	23
IO159NB7F15	16
IO159PB7F15	17
IO160NB7F15	18
IO160PB7F15	19
IO161NB7F15	12
IO161PB7F15	13
IO163NB7F15	10
IO163PB7F15	11
IO165NB7F15	6
IO165PB7F15	7
IO167NB7F15	4
IO167PB7F15	5
Dedicated I/O	
GND	1
GND	9
GND	15
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88
GND	89

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX500 Function	Pin Number
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330
GND	334
GND	340
GND	345
GND/LP	352
NC	91
NC	117
NC	130
NC	131

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX500 Function	Pin Number
NC	148
NC	174
NC	268
NC	294
NC	307
NC	308
NC	327
NC	328
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349
TDI	348
TDO	347
TMS	350
TRST	351
VCCA	3
VCCA	14
VCCA	32
VCCA	56
VCCA	74
VCCA	87
VCCA	102
VCCA	114
VCCA	150
VCCA	162
VCCA	175
VCCA	191
VCCA	209
VCCA	233
VCCA	251
VCCA	263
VCCA	279
VCCA	291
VCCA	329
VCCA	339
VCCDA	2
VCCDA	44
VCCDA	90
VCCDA	116
VCCDA	132
VCCDA	149
VCCDA	178

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX500 Function	Pin Number
VCCDA	221
VCCDA	266
VCCDA	293
VCCDA	309
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued	
CQ352	
AX500 Function	Pin Number
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

Table 3-20. Packaging Pin Assignment Table (PPAT)

CQ352	
AX1000 Function	Pin Number
Bank 0	
IO02NB0F0	341
IO02PB0F0	342
IO03PB0F0	343
IO04NB0F0	337
IO04PB0F0	338
IO08NB0F0	331
IO08PB0F0	332
IO09NB0F0	335
IO09PB0F0	336
IO24NB0F2	325
IO24PB0F2	326
IO25NB0F2	323
IO25PB0F2	324
IO30NB0F2/HCLKAN	319
IO30PB0F2/HCLKAP	320
IO31NB0F2/HCLKBN	313
IO31PB0F2/HCLKBP	314
Bank 1	
IO32NB1F3/HCLKCN	305
IO32PB1F3/HCLKCP	306
IO33NB1F3/HCLKDN	299
IO33PB1F3/HCLKDP	300
IO38NB1F3	295
IO38PB1F3	296
IO54NB1F5	287
IO54PB1F5	288
IO55NB1F5	289
IO55PB1F5	290
IO56NB1F5	281
IO56PB1F5	282
IO57NB1F5	283
IO57PB1F5	284

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX1000 Function	Pin Number
IO59NB1F5	277
IO59PB1F5	278
IO60NB1F5	275
IO60PB1F5	276
IO61NB1F5	271
IO61PB1F5	272
IO63NB1F5	269
IO63PB1F5	270
Bank 2	
IO64NB2F6	259
IO64PB2F6	260
IO67NB2F6	261
IO67PB2F6	262
IO68NB2F6	255
IO68PB2F6	256
IO69NB2F6	253
IO69PB2F6	254
IO74NB2F7	249
IO74PB2F7	250
IO75NB2F7	247
IO75PB2F7	248
IO76NB2F7	243
IO76PB2F7	244
IO77NB2F7	241
IO77PB2F7	242
IO78NB2F7	237
IO78PB2F7	238
IO79NB2F7	235
IO79PB2F7	236
IO82NB2F7	231
IO82PB2F7	232
IO83NB2F7	229
IO83PB2F7	230
IO94NB2F8	225
IO94PB2F8	226
IO95NB2F8	223
IO95PB2F8	224
Bank 3	
IO96NB3F9	217
IO96PB3F9	218
IO97NB3F9	219
IO97PB3F9	220
IO99NB3F9	213
IO99PB3F9	214

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX1000 Function	Pin Number
IO108NB3F10	211
IO108PB3F10	212
IO109NB3F10	207
IO109PB3F10	208
IO111NB3F10	205
IO111PB3F10	206
IO112NB3F10	199
IO112PB3F10	200
IO113NB3F10	201
IO113PB3F10	202
IO115NB3F10	195
IO115PB3F10	196
IO116NB3F10	193
IO116PB3F10	194
IO117NB3F10	189
IO117PB3F10	190
IO124NB3F11	183
IO124PB3F11	184
IO125NB3F11	187
IO125PB3F11	188
IO127NB3F11	181
IO127PB3F11	182
IO128NB3F11	179
IO128PB3F11	180
Bank 4	
IO130NB4F12	172
IO130PB4F12	173
IO131NB4F12	170
IO131PB4F12	171
IO132NB4F12	166
IO132PB4F12	167
IO133NB4F12	164
IO133PB4F12	165
IO134NB4F12	160
IO134PB4F12	161
IO136NB4F12	158
IO136PB4F12	159
IO137NB4F12	154
IO137PB4F12	155
IO138NB4F12	152
IO138PB4F12	153
IO153NB4F14	146
IO153PB4F14	147
IO159NB4F14/CLKEN	142

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX1000 Function	Pin Number
IO159PB4F14/CLKEP	143
IO160NB4F14/CLKFN	136
IO160PB4F14/CLKFP	137
Bank 5	
IO161NB5F15/CLKGN	128
IO161PB5F15/CLKGP	129
IO162NB5F15/CLKHN	122
IO162PB5F15/CLKHP	123
IO167NB5F15	118
IO167PB5F15	119
IO183NB5F17	110
IO183PB5F17	111
IO184NB5F17	112
IO184PB5F17	113
IO185NB5F17	104
IO185PB5F17	105
IO186NB5F17	106
IO186PB5F17	107
IO187NB5F17	98
IO187PB5F17	99
IO188NB5F17	100
IO188PB5F17	101
IO190NB5F17	94
IO190PB5F17	95
IO192NB5F17	92
IO192PB5F17	93
Bank 6	
IO193PB6F18	86
IO194NB6F18	84
IO194PB6F18	85
IO196NB6F18	78
IO196PB6F18	79
IO197NB6F18	82
IO197PB6F18	83
IO198NB6F18	76
IO198PB6F18	77
IO203NB6F19	72
IO203PB6F19	73
IO204NB6F19	70
IO204PB6F19	71
IO205NB6F19	66
IO205PB6F19	67
IO206NB6F19	64
IO206PB6F19	65

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX1000 Function	Pin Number
IO207NB6F19	60
IO207PB6F19	61
IO208NB6F19	58
IO208PB6F19	59
IO211NB6F19	54
IO211PB6F19	55
IO212NB6F19	52
IO212PB6F19	53
IO223NB6F20	48
IO223PB6F20	49
IO224NB6F20	46
IO224PB6F20	47
Bank 7	
IO225NB7F21	40
IO225PB7F21	41
IO226NB7F21	42
IO226PB7F21	43
IO237NB7F22	34
IO237PB7F22	35
IO238NB7F22	36
IO238PB7F22	37
IO240NB7F22	30
IO240PB7F22	31
IO241NB7F22	28
IO241PB7F22	29
IO242NB7F22	24
IO242PB7F22	25
IO244NB7F22	22
IO244PB7F22	23
IO245NB7F22	18
IO245PB7F22	19
IO246NB7F22	16
IO246PB7F22	17
IO249NB7F23	12
IO249PB7F23	13
IO250NB7F23	10
IO250PB7F23	11
IO256NB7F23	4
IO256PB7F23	5
IO257NB7F23	6
IO257PB7F23	7
Dedicated I/O	
GND	1
GND	9

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX1000 Function	Pin Number
GND	15
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX1000 Function	Pin Number
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330
GND	334
GND	340
GND	345
GND	352
NC	91
NC	130
NC	131
NC	174
NC	268
NC	307
NC	308
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349
TDI	348
TDO	347
TMS	350
TRST	351
VCCA	3
VCCA	14
VCCA	32
VCCA	56
VCCA	74
VCCA	87
VCCA	102
VCCA	114
VCCA	150
VCCA	162
VCCA	175
VCCA	191
VCCA	209
VCCA	233
VCCA	251
VCCA	263
VCCA	279
VCCA	291

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX1000 Function	Pin Number
VCCA	329
VCCA	339
VCCDA	2
VCCDA	44
VCCDA	90
VCCDA	116
VCCDA	117
VCCDA	132
VCCDA	148
VCCDA	149
VCCDA	178
VCCDA	221
VCCDA	266
VCCDA	293
VCCDA	294
VCCDA	309
VCCDA	327
VCCDA	328
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX1000 Function	Pin Number
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

Table 3-21. Packaging Pin Assignment Table (PPAT)

CQ352	
AX2000 Function	Pin Number
Bank 0	
IO01NB0F0	341
IO01PB0F0	342
IO02PB0F0	343
IO04NB0F0	337
IO04PB0F0	338
IO05NB0F0	335
IO05PB0F0	336
IO08NB0F0	331
IO08PB0F0	332
IO37NB0F3	325
IO37PB0F3	326
IO38NB0F3	323
IO38PB0F3	324
IO41NB0F3/HCLKAN	319
IO41PB0F3/HCLKAP	320
IO42NB0F3/HCLKBN	313
IO42PB0F3/HCLKBP	314
Bank 1	
IO43NB1F4/HCLKCN	305

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX2000 Function	Pin Number
IO43PB1F4/HCLKCP	306
IO44NB1F4/HCLKDN	299
IO44PB1F4/HCLKDP	300
IO48NB1F4	295
IO48PB1F4	296
IO65NB1F6	283
IO65PB1F6	284
IO66NB1F6	289
IO66PB1F6	290
IO68NB1F6	287
IO68PB1F6	288
IO69NB1F6	275
IO69PB1F6	276
IO70NB1F6	281
IO70PB1F6	282
IO71NB1F6	277
IO71PB1F6	278
IO73NB1F6	269
IO73PB1F6	270
IO74NB1F6	271
IO74PB1F6	272
Bank 2	
IO87NB2F8	261
IO87PB2F8	262
IO88NB2F8	255
IO88PB2F8	256
IO89NB2F8	259
IO89PB2F8	260
IO91NB2F8	253
IO91PB2F8	254
IO99NB2F9	249
IO99PB2F9	250
IO100NB2F9	247
IO100PB2F9	248
IO107NB2F10	243
IO107PB2F10	244
IO110NB2F10	241
IO110PB2F10	242
IO111NB2F10	237
IO111PB2F10	238
IO112NB2F10	235
IO112PB2F10	236
IO113NB2F10	231
IO113PB2F10	232

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX2000 Function	Pin Number
IO114NB2F10	229
IO114PB2F10	230
IO115NB2F10	225
IO115PB2F10	226
IO117NB2F10	223
IO117PB2F10	224
Bank 3	
IO129NB3F12	219
IO129PB3F12	220
IO132NB3F12	217
IO132PB3F12	218
IO137NB3F12	213
IO137PB3F12	214
IO139NB3F13	211
IO139PB3F13	212
IO141NB3F13	205
IO141PB3F13	206
IO142NB3F13	207
IO142PB3F13	208
IO145NB3F13	199
IO145PB3F13	200
IO146NB3F13	201
IO146PB3F13	202
IO147NB3F13	193
IO147PB3F13	194
IO148NB3F13	195
IO148PB3F13	196
IO149NB3F13	189
IO149PB3F13	190
IO161NB3F15	183
IO161PB3F15	184
IO163NB3F15	187
IO163PB3F15	188
IO165NB3F15	181
IO165PB3F15	182
IO167NB3F15	179
IO167PB3F15	180
Bank 4	
IO181NB4F17	172
IO181PB4F17	173
IO182NB4F17	170
IO182PB4F17	171
IO183NB4F17	166
IO183PB4F17	167

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX2000 Function	Pin Number
IO184NB4F17	164
IO184PB4F17	165
IO185NB4F17	160
IO185PB4F17	161
IO190NB4F17	158
IO190PB4F17	159
IO191NB4F17	154
IO191PB4F17	155
IO192NB4F17	152
IO192PB4F17	153
IO207NB4F19	146
IO207PB4F19	147
IO212NB4F19/CLKEN	142
IO212PB4F19/CLKEP	143
IO213NB4F19/CLKFN	136
IO213PB4F19/CLKFP	137
Bank 5	
IO214NB5F20/CLKGN	128
IO214PB5F20/CLKGP	129
IO215NB5F20/CLKHN	122
IO215PB5F20/CLKHP	123
IO217NB5F20	118
IO217PB5F20	119
IO236NB5F22	110
IO236PB5F22	111
IO237NB5F22	112
IO237PB5F22	113
IO238NB5F22	104
IO238PB5F22	105
IO239NB5F22	106
IO239PB5F22	107
IO240NB5F22	100
IO240PB5F22	101
IO242NB5F22	94
IO242PB5F22	95
IO243NB5F22	98
IO243PB5F22	99
IO244NB5F22	92
IO244PB5F22	93
Bank 6	
IO257PB6F24	86
IO258NB6F24	84
IO258PB6F24	85
IO261NB6F24	82

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX2000 Function	Pin Number
IO261PB6F24	83
IO262NB6F24	78
IO262PB6F24	79
IO265NB6F24	76
IO265PB6F24	77
IO279NB6F26	72
IO279PB6F26	73
IO280NB6F26	70
IO280PB6F26	71
IO281NB6F26	66
IO281PB6F26	67
IO282NB6F26	64
IO282PB6F26	65
IO284NB6F26	60
IO284PB6F26	61
IO285NB6F26	58
IO285PB6F26	59
IO286NB6F26	54
IO286PB6F26	55
IO287NB6F26	52
IO287PB6F26	53
IO294NB6F27	48
IO294PB6F27	49
IO296NB6F27	46
IO296PB6F27	47
Bank 7	
IO300NB7F28	42
IO300PB7F28	43
IO303NB7F28	40
IO303PB7F28	41
IO310NB7F29	34
IO310PB7F29	35
IO311NB7F29	36
IO311PB7F29	37
IO312NB7F29	28
IO312PB7F29	29
IO315NB7F29	30
IO315PB7F29	31
IO316NB7F29	22
IO316PB7F29	23
IO317NB7F29	24
IO317PB7F29	25
IO318NB7F29	18
IO318PB7F29	19

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX2000 Function	Pin Number
IO320NB7F29	16
IO320PB7F29	17
IO334NB7F31	10
IO334PB7F31	11
IO335NB7F31	12
IO335PB7F31	13
IO338NB7F31	6
IO338PB7F31	7
IO341NB7F31	4
IO341PB7F31	5
Dedicated I/O	
GND	1
GND	9
GND	15
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX2000 Function	Pin Number
GND	210
GND	216
GND	222
GND	228
GND	234
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330
GND	334
GND	340
GND	345
GND	352
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349
TDI	348
TDO	347
TMS	350
TRST	351
VCCA	3
VCCA	14
VCCA	32
VCCA	56
VCCA	74
VCCA	87
VCCA	102
VCCA	114
VCCA	150
VCCA	162
VCCA	175
VCCA	191

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CQ352	
AX2000 Function	Pin Number
VCCA	209
VCCA	233
VCCA	251
VCCA	263
VCCA	279
VCCA	291
VCCA	329
VCCA	339
VCCDA	2
VCCDA	44
VCCDA	90
VCCDA	91
VCCDA	116
VCCDA	117
VCCDA	130
VCCDA	131
VCCDA	132
VCCDA	148
VCCDA	149
VCCDA	174
VCCDA	178
VCCDA	221
VCCDA	266
VCCDA	268
VCCDA	293
VCCDA	294
VCCDA	307
VCCDA	308
VCCDA	309
VCCDA	327
VCCDA	328
VCCDA	346
VCCIB0	321
VCCIB0	333
VCCIB0	344
VCCIB1	273
VCCIB1	285
VCCIB1	297
VCCIB2	227
VCCIB2	239
VCCIB2	245
VCCIB2	257
VCCIB3	185
VCCIB3	197

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

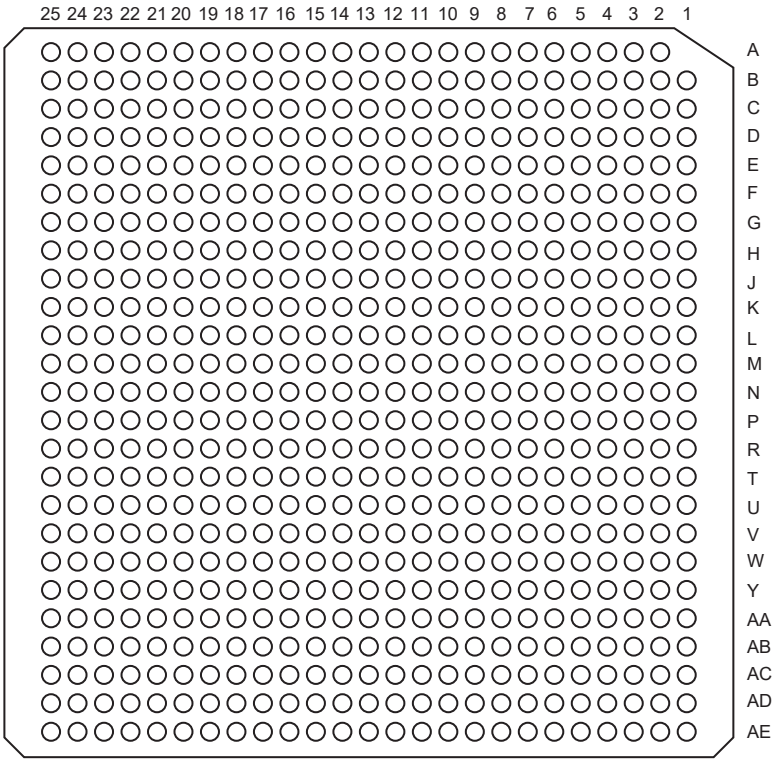
CQ352	
AX2000 Function	Pin Number
VCCIB3	203
VCCIB3	215
VCCIB4	144
VCCIB4	156
VCCIB4	168
VCCIB5	96
VCCIB5	108
VCCIB5	120
VCCIB6	50
VCCIB6	62
VCCIB6	68
VCCIB6	80
VCCIB7	8
VCCIB7	20
VCCIB7	26
VCCIB7	38
VCCPLA	317
VCCPLB	315
VCCPLC	303
VCCPLD	301
VCCPLE	140
VCCPLF	138
VCCPLG	126
VCCPLH	124
VCOMPLA	318
VCOMPLB	316
VCOMPLC	304
VCOMPLD	302
VCOMPLE	141
VCOMPLF	139
VCOMPLG	127
VCOMPLH	125
VPUMP	267

3.12 CG624

The following figure shows package bottom-view of CG624.

© 2024 Microchip Technology Inc. and its subsidiaries

Figure 3-12. Package Bottom-View



Note: For Package Manufacturing and Environmental information, visit Resource center at www.microchip.com/en-us/support/package-drawings/fpga-packaging.

The following tables list the IOD interface pin placement.

Table 3-22. Packaging Pin Assignment Table (PPAT)

CG624	
AX1000 Function	Pin Number
Bank 0	
IO00NB0F0	F8
IO00PB0F0	F7
IO02NB0F0	G7
IO02PB0F0	G6
IO04NB0F0	E9
IO04PB0F0	D8
IO06NB0F0	G9
IO06PB0F0	G8
IO07PB0F0	B6
IO08NB0F0	F10
IO08PB0F0	F9
IO09PB0F0	C7
IO10NB0F0	H8
IO10PB0F0	H7
IO11NB0F0	D10
IO11PB0F0	D9
IO12NB0F1	B5

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX1000 Function	Pin Number
IO12PB0F1	B4
IO13NB0F1	A7
IO13PB0F1	A6
IO14NB0F1	C9
IO14PB0F1	C8
IO15PB0F1	B7
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	A9
IO17PB0F1	B9
IO18NB0F1	D12
IO18PB0F1	D11
IO20NB0F1	B11
IO20PB0F1	B10
IO21NB0F1	A11
IO21PB0F1	A10
IO22NB0F2	H10
IO22PB0F2	H9
IO23NB0F2	E11
IO23PB0F2	F11
IO24NB0F2	D7
IO24PB0F2	E7
IO25PB0F2	B12
IO26NB0F2	H11
IO26PB0F2	G11
IO27NB0F2	C11
IO27PB0F2	B8
IO28NB0F2	J13
IO28PB0F2	K13
IO29NB0F2	J8
IO29PB0F2	J7
IO30NB0F2/HCLKAN	G13
IO30PB0F2/HCLKAP	G12
IO31NB0F2/HCLKBN	C13
IO31PB0F2/HCLKBP	C12
Bank 1	
IO32NB1F3/HCLKCN	G15
IO32PB1F3/HCLKCP	G14
IO33NB1F3/HCLKDN	B14
IO33PB1F3/HCLKDP	B13
IO34NB1F3	G16
IO34PB1F3	H16
IO35NB1F3	C17
IO35PB1F3	B18

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX1000 Function	Pin Number
IO36NB1F3	H18
IO36PB1F3	H15
IO37NB1F3	H13
IO38NB1F3	E15
IO38PB1F3	F15
IO39NB1F3	D14
IO39PB1F3	C14
IO40NB1F3	D16
IO40PB1F3	D15
IO41NB1F4	F16
IO42NB1F4	G21
IO42PB1F4	G20
IO43NB1F4	A16
IO43PB1F4	A15
IO44NB1F4	A20
IO44PB1F4	A19
IO45NB1F4	B17
IO45PB1F4	B16
IO46NB1F4	G17
IO46PB1F4	H17
IO47NB1F4	A17
IO48NB1F4	C19
IO48PB1F4	C18
IO49NB1F4	B20
IO49PB1F4	B19
IO50NB1F4	H20
IO50PB1F4	H19
IO51NB1F4	A22
IO51PB1F4	A21
IO52NB1F4	C21
IO52PB1F4	C20
IO53NB1F4	B22
IO53PB1F4	B21
IO54NB1F5	J18
IO54PB1F5	J19
IO55NB1F5	D18
IO55PB1F5	D17
IO56NB1F5	F20
IO56PB1F5	F19
IO58NB1F5	E17
IO58PB1F5	F17
IO60NB1F5	D20
IO60PB1F5	D19
IO62NB1F5	E18

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX1000 Function	Pin Number
IO62PB1F5	F18
IO63NB1F5	G19
IO63PB1F5	G18
Bank 2	
IO64NB2F6	M17
IO64PB2F6	G22
IO65NB2F6	J21
IO65PB2F6	J20
IO66NB2F6	L23
IO66PB2F6	K20
IO67NB2F6	F23
IO67PB2F6	E23
IO68NB2F6	L18
IO68PB2F6	K18
IO70NB2F6	E24
IO70PB2F6	D24
IO71NB2F6	H23
IO71PB2F6	G23
IO72NB2F6	L19
IO72PB2F6	K19
IO74NB2F7	J22
IO74PB2F7	H22
IO75NB2F7	N23
IO75PB2F7	M23
IO76NB2F7	N17
IO76PB2F7	N16
IO77NB2F7	L22
IO77PB2F7	K22
IO78NB2F7	M19
IO78PB2F7	M18
IO79NB2F7	N19
IO79PB2F7	N18
IO80NB2F7	L21
IO80PB2F7	L20
IO82NB2F7	P18
IO82PB2F7	P17
IO83NB2F7	N22
IO83PB2F7	M22
IO84NB2F7	M20
IO84PB2F7	M21
IO86NB2F8	E25
IO86PB2F8	D25
IO87NB2F8	L24
IO87PB2F8	K24

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX1000 Function	Pin Number
IO88NB2F8	G24
IO88PB2F8	F24
IO89NB2F8	J25
IO90NB2F8	G25
IO90PB2F8	F25
IO91NB2F8	L25
IO91PB2F8	K25
IO92NB2F8	J24
IO92PB2F8	H24
IO93PB2F8	J23
IO94NB2F8	N24
IO94PB2F8	M24
IO95NB2F8	N25
IO95PB2F8	M25
Bank 3	
IO96NB3F9	T18
IO96PB3F9	R18
IO97NB3F9	N20
IO97PB3F9	P24
IO98NB3F9	P20
IO98PB3F9	P19
IO99NB3F9	P21
IO100NB3F9	T22
IO100PB3F9	W24
IO101NB3F9	R22
IO101PB3F9	P22
IO102NB3F9	U19
IO102PB3F9	T19
IO104NB3F9	V20
IO104PB3F9	U20
IO105NB3F9	R23
IO105PB3F9	P23
IO106NB3F9	R19
IO106PB3F9	R20
IO107NB3F10	AB24
IO108NB3F10	R25
IO108PB3F10	P25
IO109NB3F10	U25
IO109PB3F10	T25
IO110NB3F10	U24
IO110PB3F10	U23
IO112NB3F10	T24
IO112PB3F10	R24
IO113NB3F10	Y25

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX1000 Function	Pin Number
IO113PB3F10	W25
IO114NB3F10	V23
IO114PB3F10	V24
IO116NB3F10	AA24
IO116PB3F10	Y24
IO117NB3F10	AB25
IO117PB3F10	AA25
IO118NB3F11	T20
IO118PB3F11	R21
IO120NB3F11	W22
IO120PB3F11	W23
IO122NB3F11	V22
IO122PB3F11	U22
IO124NB3F11	Y23
IO124PB3F11	AA23
IO126NB3F11	V21
IO126PB3F11	U21
IO128NB3F11	Y22
IO128PB3F11	Y21
Bank 4	
IO129NB4F12	W20
IO129PB4F12	Y20
IO131NB4F12	V19
IO131PB4F12	W19
IO133NB4F12	Y18
IO133PB4F12	Y19
IO135NB4F12	W18
IO135PB4F12	V18
IO137NB4F12	Y17
IO137PB4F12	AA17
IO138NB4F12	AB19
IO138PB4F12	AB18
IO139NB4F13	AA19
IO139PB4F13	U18
IO140NB4F13	AC20
IO140PB4F13	AC21
IO141NB4F13	AD17
IO141PB4F13	AD18
IO142NB4F13	AD21
IO142PB4F13	AD22
IO143NB4F13	AB17
IO143PB4F13	AC17
IO144PB4F13	AE22
IO145NB4F13	AE15

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX1000 Function	Pin Number
IO145PB4F13	AE16
IO146NB4F13	AD19
IO146PB4F13	AD20
IO147NB4F13	AD15
IO147PB4F13	AD16
IO148PB4F13	AE21
IO149NB4F13	AD14
IO149PB4F13	AC14
IO150NB4F13	AE19
IO150PB4F13	AE20
IO151NB4F13	V17
IO151PB4F13	W17
IO152NB4F14	AB16
IO152PB4F14	W16
IO153NB4F14	Y15
IO153PB4F14	Y16
IO155NB4F14	V15
IO155PB4F14	V16
IO156NB4F14	AB14
IO156PB4F14	AB15
IO157NB4F14	AE14
IO157PB4F14	AC18
IO158NB4F14	AC15
IO158PB4F14	AC19
IO159NB4F14/CLKEN	W14
IO159PB4F14/CLKEP	W15
IO160NB4F14/CLKFN	AC13
IO160PB4F14/CLKFP	AD13
Bank 5	
IO161NB5F15/CLKGN	W13
IO161PB5F15/CLKGP	Y13
IO162NB5F15/CLKHN	AC12
IO162PB5F15/CLKHP	AD12
IO163NB5F15	V9
IO163PB5F15	V10
IO164NB5F15	V11
IO164PB5F15	T13
IO165NB5F15	U13
IO165PB5F15	V13
IO167NB5F15	W11
IO167PB5F15	W12
IO168NB5F15	AB6
IO168PB5F15	AA6
IO169NB5F15	V8

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX1000 Function	Pin Number
IO169PB5F15	V7
IO171NB5F16	W8
IO171PB5F16	W9
IO172NB5F16	AB8
IO172PB5F16	AC8
IO173NB5F16	AA11
IO173PB5F16	Y11
IO174NB5F16	AB10
IO174PB5F16	AB11
IO175NB5F16	AC9
IO175PB5F16	AE9
IO177NB5F16	AA8
IO177PB5F16	Y8
IO178NB5F16	Y6
IO178PB5F16	W6
IO179NB5F16	Y10
IO179PB5F16	W10
IO180NB5F16	Y7
IO180PB5F16	W7
IO181NB5F17	AD9
IO181PB5F17	AD10
IO182NB5F17	AE10
IO182PB5F17	AE11
IO183NB5F17	AD7
IO183PB5F17	AD8
IO184NB5F17	AB9
IO185NB5F17	AE6
IO185PB5F17	AE7
IO186NB5F17	AE4
IO186PB5F17	AE5
IO187NB5F17	AA9
IO187PB5F17	Y9
IO188NB5F17	U8
IO189NB5F17	AD5
IO189PB5F17	AD6
IO191NB5F17	AC5
IO191PB5F17	AC6
IO192NB5F17	AB7
IO192PB5F17	AC7
Bank 6	
IO193NB6F18	U6
IO193PB6F18	U5
IO194NB6F18	Y3
IO194PB6F18	AA3

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX1000 Function	Pin Number
IO195NB6F18	V6
IO195PB6F18	W4
IO197NB6F18	R5
IO197PB6F18	U3
IO198NB6F18	P6
IO199NB6F18	Y5
IO199PB6F18	W5
IO200NB6F18	V3
IO200PB6F18	W3
IO201NB6F18	T7
IO201PB6F18	U7
IO202NB6F18	V2
IO203NB6F19	W2
IO203PB6F19	Y2
IO204NB6F19	AA1
IO204PB6F19	AB1
IO205NB6F19	R6
IO205PB6F19	T6
IO206NB6F19	W1
IO206PB6F19	Y1
IO207NB6F19	T2
IO207PB6F19	U2
IO208NB6F19	T1
IO208PB6F19	U1
IO209NB6F19	AA2
IO209PB6F19	AB2
IO210NB6F19	P5
IO211NB6F19	M1
IO211PB6F19	N1
IO212NB6F19	P1
IO212PB6F19	R1
IO213NB6F19	R8
IO213PB6F19	T8
IO215NB6F20	U4
IO215PB6F20	V4
IO216NB6F20	P8
IO216PB6F20	R3
IO217NB6F20	P7
IO217PB6F20	R7
IO219NB6F20	R4
IO219PB6F20	T4
IO220NB6F20	P2
IO220PB6F20	R2
IO221NB6F20	N4

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX1000 Function	Pin Number
IO221PB6F20	P4
IO223NB6F20	M2
IO223PB6F20	N2
IO224NB6F20	N3
IO224PB6F20	P3
Bank 7	
IO225NB7F21	J2
IO225PB7F21	J1
IO226PB7F21	G2
IO227NB7F21	H3
IO227PB7F21	H2
IO229NB7F21	K2
IO229PB7F21	L2
IO230NB7F21	K1
IO230PB7F21	L1
IO231NB7F21	E2
IO231PB7F21	F2
IO232NB7F21	F1
IO232PB7F21	G1
IO233NB7F21	L3
IO233PB7F21	M3
IO234NB7F21	D1
IO234PB7F21	E1
IO235NB7F21	K4
IO235PB7F21	L4
IO236NB7F22	M6
IO237NB7F22	N8
IO237PB7F22	N7
IO238NB7F22	M5
IO239NB7F22	L6
IO239PB7F22	L5
IO240NB7F22	M4
IO241NB7F22	L7
IO241PB7F22	M7
IO242NB7F22	J3
IO243NB7F22	M9
IO243PB7F22	M8
IO244NB7F22	P9
IO244PB7F22	N6
IO245NB7F22	K8
IO245PB7F22	L8
IO246NB7F22	F3
IO246PB7F22	E3
IO247NB7F23	K7

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX1000 Function	Pin Number
IO247PB7F23	K6
IO248NB7F23	D2
IO249NB7F23	G4
IO249PB7F23	G3
IO251NB7F23	N10
IO251PB7F23	N9
IO253NB7F23	H4
IO253PB7F23	J4
IO255NB7F23	J6
IO255PB7F23	J5
IO257NB7F23	H5
IO257PB7F23	H6
Dedicated I/O	
GND	K5
GND	A18
GND	A2
GND	A24
GND	A25
GND	A8
GND	AA10
GND	AA16
GND	AA18
GND	AA21
GND	AA5
GND	AB22
GND	AB4
GND	AC10
GND	AC16
GND	AC23
GND	AC3
GND	AD1
GND	AD2
GND	AD24
GND	AD25
GND	AE1
GND	AE18
GND	AE2
GND	AE24
GND	AE25
GND	AE8
GND	B1
GND	B2
GND	B24
GND	B25

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX1000 Function	Pin Number
GND	C10
GND	C16
GND	C23
GND	C3
GND	D22
GND	D4
GND	E10
GND	E16
GND	E21
GND	E5
GND/LP	E8
GND	H1
GND	H21
GND	H25
GND	K21
GND	K23
GND	K3
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	T21
GND	T23

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX1000 Function	Pin Number
GND	T3
GND	T5
GND	V1
GND	V25
GND	V5
NC	A14
NC	AA20
NC	AB13
NC	AD4
NC	AE12
NC	F21
NC	G10
PRA	F13
PRB	A13
PRC	AB12
PRD	AE13
TCK	F5
TDI	C5
TDO	F6
TMS	D6
TRST	E6
VCCA	AB20
VCCA	F22
VCCA	F4
VCCA	J17
VCCA	J9
VCCA	K10
VCCA	K11
VCCA	K15
VCCA	K16
VCCA	L10
VCCA	L16
VCCA	R10
VCCA	R16
VCCA	T10
VCCA	T11
VCCA	T15
VCCA	T16
VCCA	U17
VCCA	U9
VCCA	Y4
VCCDA	A12
VCCDA	AA13
VCCDA	AA15

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX1000 Function	Pin Number
VCCDA	AA7
VCCDA	AC11
VCCDA	AD11
VCCDA	AE17
VCCDA	B15
VCCDA	C15
VCCDA	C6
VCCDA	D13
VCCDA	E13
VCCDA	E19
VCCDA	G5
VCCDA	N21
VCCDA	N5
VCCDA	W21
VCCIB0	A3
VCCIB0	B3
VCCIB0	C4
VCCIB0	D5
VCCIB0	J10
VCCIB0	J11
VCCIB0	K12
VCCIB1	A23
VCCIB1	B23
VCCIB1	C22
VCCIB1	D21
VCCIB1	J15
VCCIB1	J16
VCCIB1	K14
VCCIB2	C24
VCCIB2	C25
VCCIB2	D23
VCCIB2	E22
VCCIB2	K17
VCCIB2	L17
VCCIB2	M16
VCCIB3	AA22
VCCIB3	AB23
VCCIB3	AC24
VCCIB3	AC25
VCCIB3	P16
VCCIB3	R17
VCCIB3	T17
VCCIB4	AB21
VCCIB4	AC22

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX1000 Function	Pin Number
VCCIB4	AD23
VCCIB4	AE23
VCCIB4	T14
VCCIB4	U15
VCCIB4	U16
VCCIB5	AB5
VCCIB5	AC4
VCCIB5	AD3
VCCIB5	AE3
VCCIB5	T12
VCCIB5	U10
VCCIB5	U11
VCCIB6	AA4
VCCIB6	AB3
VCCIB6	AC1
VCCIB6	AC2
VCCIB6	P10
VCCIB6	R9
VCCIB6	T9
VCCIB7	C1
VCCIB7	C2
VCCIB7	D3
VCCIB7	E4
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10
VCCPLA	E12
VCCPLB	J12
VCCPLC	E14
VCCPLD	H14
VCCPLE	Y14
VCCPLF	U14
VCCPLG	Y12
VCCPLH	U12
VCOMPLA	F12
VCOMPLB	H12
VCOMPLC	F14
VCOMPLD	J14
VCOMPLE	AA14
VCOMPLF	V14
VCOMPLG	AA12
VCOMPLH	V12
VPUMP	E20

© 2024 Microchip Technology Inc. and its subsidiaries

Table 3-23. Packaging Pin Assignment Table (PPAT)

CG624	
AX2000 Function	Pin Number
Bank 0	
IO00NB0F0	D7[1]
IO00PB0F0	E7[1]
IO01NB0F0	G7
IO01PB0F0	G6
IO02NB0F0	B5
IO02PB0F0	B4
IO04PB0F0	C7
IO05NB0F0	F8
IO05PB0F0	F7
IO06NB0F0	H8
IO06PB0F0	H7
IO11NB0F0	J8
IO11PB0F0	J7
IO12PB0F1	B6
IO13NB0F1	E9[1]
IO13PB0F1	D8[1]
IO15NB0F1	C9
IO15PB0F1	C8
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	A7
IO18PB0F1	A6
IO19NB0F1	G9
IO19PB0F1	G8
IO20PB0F1	B7
IO23NB0F2	F10
IO23PB0F2	F9
IO26NB0F2	C11[1]
IO26PB0F2	B8[1]
IO27NB0F2	H10
IO27PB0F2	H9
IO28NB0F2	A9
IO28PB0F2	B9
IO30NB0F2	B11
IO30PB0F2	B10
IO31NB0F2	E11
IO31PB0F2	F11
IO33NB0F2	D12
IO33PB0F2	D11
IO34NB0F3	A11
IO34PB0F3	A10

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX2000 Function	Pin Number
IO37NB0F3	J13
IO37PB0F3	K13
IO38NB0F3	H11
IO38PB0F3	G11
IO40PB0F3	B12
IO41NB0F3/HCLKAN	G13
IO41PB0F3/HCLKAP	G12
IO42NB0F3/HCLKBN	C13
IO42PB0F3/HCLKBP	C12
Bank 1	
IO43NB1F4/HCLKCN	G15
IO43PB1F4/HCLKCP	G14
IO44NB1F4/HCLKDN	B14
IO44PB1F4/HCLKDP	B13
IO45NB1F4	H13
IO47NB1F4	D14
IO47PB1F4	C14
IO48NB1F4	A16
IO48PB1F4	A15
IO49PB1F4	H15
IO51NB1F4	E15
IO51PB1F4	F15
IO52NB1F4	A17
IO55NB1F5	G16
IO55PB1F5	H16
IO56NB1F5	A20
IO56PB1F5	A19
IO57NB1F5	D16
IO57PB1F5	D15
IO58NB1F5	A22
IO58PB1F5	A21
IO59NB1F5	F16
IO61NB1F5	G17
IO61PB1F5	H17
IO62NB1F5	B17
IO62PB1F5	B16
IO63NB1F5	H18
IO65NB1F6	C17
IO66PB1F6	B18
IO67NB1F6	J18
IO67PB1F6	J19
IO68NB1F6	B20
IO68PB1F6	B19
IO69NB1F6	E17

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX2000 Function	Pin Number
IO69PB1F6	F17
IO70NB1F6	B22
IO70PB1F6	B21
IO71PB1F6	G18
IO73NB1F6	G19
IO74NB1F6	C19
IO74PB1F6	C18
IO75NB1F6	D18
IO75PB1F6	D17
IO76NB1F7	C21
IO76PB1F7	C20
IO79NB1F7	H20
IO79PB1F7	H19
IO80NB1F7	E18
IO80PB1F7	F18
IO81NB1F7	G21
IO81PB1F7	G20
IO82NB1F7	F20
IO82PB1F7	F19
IO85NB1F7	D20[1]
IO85PB1F7	D19[1]
Bank 2	
IO86NB2F8	F23
IO86PB2F8	E23
IO87NB2F8	H23
IO87PB2F8	G23
IO88NB2F8	E24
IO88PB2F8	D24
IO89NB2F8	M17[1]
IO89PB2F8	G22[1]
IO91NB2F8	J22
IO91PB2F8	H22
IO92NB2F8	L18
IO92PB2F8	K18
IO96NB2F9	G24
IO96PB2F9	F24
IO97NB2F9	J21
IO97PB2F9	J20
IO98PB2F9	J23
IO99NB2F9	L19
IO99PB2F9	K19
IO100NB2F9	E25
IO100PB2F9	D25
IO103PB2F9	K20

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX2000 Function	Pin Number
IO105NB2F9	M19
IO105PB2F9	M18
IO106NB2F9	J24
IO106PB2F9	H24
IO107NB2F10	L23[1]
IO107PB2F10	N16[1]
IO109NB2F10	L22
IO109PB2F10	K22
IO110NB2F10	G25
IO110PB2F10	F25
IO111NB2F10	L21
IO111PB2F10	L20
IO112NB2F10	L24
IO112PB2F10	K24
IO113NB2F10	N17
IO115NB2F10	M20
IO115PB2F10	M21
IO117NB2F10	N19
IO117PB2F10	N18
IO118NB2F11	J25
IO121NB2F11	N24
IO121PB2F11	M24
IO122NB2F11	L25
IO122PB2F11	K25
IO123NB2F11	N22
IO123PB2F11	M22
IO124NB2F11	N23
IO124PB2F11	M23
IO127NB2F11	P18
IO127PB2F11	P17
IO128NB2F11	N25
IO128PB2F11	M25
Bank 3	
IO129NB3F12	N20
IO130PB3F12	P24
IO131NB3F12	P21
IO133NB3F12	P20
IO133PB3F12	P19
IO138NB3F12	R23
IO138PB3F12	P23
IO139NB3F13	R22
IO139PB3F13	P22
IO141NB3F13	R19
IO142NB3F13	R25

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX2000 Function	Pin Number
IO142PB3F13	P25
IO143PB3F13	R21
IO145NB3F13	T18
IO145PB3F13	R18
IO146NB3F13	T24
IO146PB3F13	R24
IO147NB3F13	T20
IO147PB3F13	R20
IO148NB3F13	U25
IO148PB3F13	T25
IO149NB3F13	T22
IO153NB3F14	U19
IO153PB3F14	T19
IO154NB3F14	Y25
IO154PB3F14	W25
IO157NB3F14	V20
IO157PB3F14	U20
IO158NB3F14	AB25
IO158PB3F14	AA25
IO160PB3F14	W24
IO161NB3F15	U24
IO161PB3F15	U23
IO162NB3F15	AA24
IO162PB3F15	Y24
IO163NB3F15	V22
IO163PB3F15	U22
IO164NB3F15	V23
IO164PB3F15	V24
IO166NB3F15	AB24
IO167NB3F15	V21
IO167PB3F15	U21
IO168NB3F15	Y23
IO168PB3F15	AA23
IO169NB3F15	W22[1]
IO169PB3F15	W23[1]
IO170NB3F15	Y22
IO170PB3F15	Y21
Bank 4	
IO171NB4F16	AC20[1]
IO171PB4F16	AC21[1]
IO172NB4F16	W20
IO172PB4F16	Y20
IO173NB4F16	AD21
IO173PB4F16	AD22

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX2000 Function	Pin Number
IO174NB4F16	AA19
IO176NB4F16	Y18
IO176PB4F16	Y19
IO177NB4F16	AB19
IO177PB4F16	AB18
IO182NB4F17	V19
IO182PB4F17	W19
IO183PB4F17	AC19
IO184NB4F17	AB17
IO184PB4F17	AC17
IO185NB4F17	AD19
IO185PB4F17	AD20
IO187PB4F17	AC18
IO188NB4F17	Y17
IO188PB4F17	AA17
IO189PB4F17	AE22
IO191NB4F17	W18
IO191PB4F17	V18
IO192PB4F17	U18
IO195PB4F18	AE21
IO196NB4F18	AB16
IO197NB4F18	AD17
IO197PB4F18	AD18
IO198NB4F18	V17
IO198PB4F18	W17
IO199NB4F18	AE19
IO199PB4F18	AE20
IO200NB4F18	AC15
IO201NB4F18	AD15
IO201PB4F18	AD16
IO202NB4F18	Y15
IO202PB4F18	Y16
IO206NB4F19	AB14
IO206PB4F19	AB15
IO207NB4F19	AE15
IO207PB4F19	AE16
IO208PB4F19	W16
IO209NB4F19	AE14
IO210NB4F19	V15
IO210PB4F19	V16
IO211NB4F19	AD14
IO211PB4F19	AC14
IO212NB4F19/CLKEN	W14
IO212PB4F19/CLKEP	W15

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX2000 Function	Pin Number
IO213NB4F19/CLKFN	AC13
IO213PB4F19/CLKFP	AD13
Bank 5	
IO214NB5F20/CLKGN	W13
IO214PB5F20/CLKGP	Y13
IO215NB5F20/CLKHN	AC12
IO215PB5F20/CLKHP	AD12
IO216NB5F20	U13
IO216PB5F20	V13
IO217NB5F20	AE10
IO217PB5F20	AE11
IO218NB5F20	W11
IO218PB5F20	W12
IO222NB5F20	AA11
IO222PB5F20	Y11
IO223PB5F21	AE9
IO225NB5F21	AE6
IO225PB5F21	AE7
IO226NB5F21	Y10
IO226PB5F21	W10
IO227PB5F21	T13
IO228NB5F21	AB10
IO228PB5F21	AB11
IO229NB5F21	AD9
IO229PB5F21	AD10
IO230NB5F21	V11
IO233NB5F21	AD7
IO233PB5F21	AD8
IO234NB5F21	V9
IO234PB5F21	V10
IO236NB5F22	AC9
IO238NB5F22	W8
IO238PB5F22	W9
IO239NB5F22	AE4
IO239PB5F22	AE5
IO240NB5F22	AB9
IO242NB5F22	AA9
IO242PB5F22	Y9
IO243NB5F22	AD5
IO243PB5F22	AD6
IO244NB5F22	U8
IO246NB5F23	AB8
IO246PB5F23	AC8
IO247NB5F23	AB7

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX2000 Function	Pin Number
IO247PB5F23	AC7
IO250NB5F23	AA8
IO250PB5F23	Y8
IO251NB5F23	V8
IO251PB5F23	V7
IO252NB5F23	Y7
IO252PB5F23	W7
IO253NB5F23	AC5
IO253PB5F23	AC6
IO254NB5F23	Y6
IO254PB5F23	W6
IO256NB5F23	AB6[1]
IO256PB5F23	AA6[1]
Bank 6	
IO257NB6F24	Y3
IO257PB6F24	AA3
IO258NB6F24	V3
IO258PB6F24	W3
IO259NB6F24	AA2
IO259PB6F24	AB2
IO260NB6F24	V6[1]
IO260PB6F24	W4[1]
IO262NB6F24	U4
IO262PB6F24	V4
IO263NB6F24	Y5
IO263PB6F24	W5
IO268NB6F25	U6
IO268PB6F25	U5
IO269PB6F25	U3
IO272NB6F25	T2
IO272PB6F25	U2
IO273NB6F25	W2
IO273PB6F25	Y2
IO274NB6F25	R6
IO274PB6F25	T6
IO275NB6F25	T7
IO275PB6F25	U7
IO277NB6F25	V2
IO278NB6F26	R4
IO278PB6F26	T4
IO279PB6F26	R3
IO280NB6F26	R5
IO281NB6F26	AA1
IO281PB6F26	AB1

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX2000 Function	Pin Number
IO284NB6F26	R8
IO284PB6F26	T8
IO285NB6F26	W1
IO285PB6F26	Y1
IO286NB6F26	P2
IO286PB6F26	R2
IO287NB6F26	T1
IO287PB6F26	U1
IO288NB6F26	P5
IO290NB6F27	P6
IO291NB6F27	P1
IO291PB6F27	R1
IO292NB6F27	P7
IO292PB6F27	R7
IO293NB6F27	M1
IO293PB6F27	N1
IO294NB6F27	P8
IO296NB6F27	N3
IO296PB6F27	P3
IO298NB6F27	N4
IO298PB6F27	P4
IO299NB6F27	M2
IO299PB6F27	N2
Bank 7	
IO300NB7F28	P9[1]
IO300PB7F28	N6[1]
IO302NB7F28	M6
IO304NB7F28	N8
IO304PB7F28	N7
IO308NB7F28	M4
IO309NB7F28	L3
IO309PB7F28	M3
IO310NB7F29	N10
IO310PB7F29	N9
IO311NB7F29	K1
IO311PB7F29	L1
IO313NB7F29	M5
IO316NB7F29	L6
IO316PB7F29	L5
IO317NB7F29	K2
IO317PB7F29	L2
IO318NB7F29	K4
IO318PB7F29	L4
IO320NB7F29	J3

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX2000 Function	Pin Number
IO321NB7F30	J2
IO321PB7F30	J1
IO323NB7F30	L7
IO323PB7F30	M7
IO324NB7F30	M9
IO324PB7F30	M8
IO327NB7F30	F1
IO327PB7F30	G1
IO328NB7F30	K7
IO328PB7F30	K6
IO329NB7F30	D1
IO329PB7F30	E1
IO331PB7F30	G2
IO332NB7F31	H3
IO332PB7F31	H2
IO333NB7F31	E2
IO333PB7F31	F2
IO334NB7F31	H4
IO334PB7F31	J4
IO335NB7F31	H5
IO335PB7F31	H6
IO337NB7F31	D2
IO338NB7F31	J6
IO338PB7F31	J5
IO339NB7F31	F3
IO339PB7F31	E3
IO340NB7F31	G4[1]
IO340PB7F31	G3[1]
IO341NB7F31	K8
IO341PB7F31	L8
Dedicated I/O	
GND	K5
GND	A18
GND	A2
GND	A24
GND	A25
GND	A8
GND	AA10
GND	AA16
GND	AA18
GND	AA21
GND	AA5
GND	AB22
GND	AB4

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX2000 Function	Pin Number
GND	AC10
GND	AC16
GND	AC23
GND	AC3
GND	AD1
GND	AD2
GND	AD24
GND	AD25
GND	AE1
GND	AE18
GND	AE2
GND	AE24
GND	AE25
GND	AE8
GND	B1
GND	B2
GND	B24
GND	B25
GND	C10
GND	C16
GND	C23
GND	C3
GND	D22
GND	D4
GND	E10
GND	E16
GND	E21
GND	E5
GND/LP	E8
GND	H1
GND	H21
GND	H25
GND	K21
GND	K23
GND	K3
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	M11
GND	M12
GND	M13
GND	M14

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX2000 Function	Pin Number
GND	M15
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	T21
GND	T23
GND	T3
GND	T5
GND	V1
GND	V25
GND	V5
PRA	F13
PRB	A13
PRC	AB12
PRD	AE13
TCK	F5
TDI	C5
TDO	F6
TMS	D6
TRST	E6
VCCA	AB20
VCCA	F22
VCCA	F4
VCCA	J17
VCCA	J9
VCCA	K10
VCCA	K11
VCCA	K15
VCCA	K16
VCCA	L10
VCCA	L16
VCCA	R10

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX2000 Function	Pin Number
VCCA	R16
VCCA	T10
VCCA	T11
VCCA	T15
VCCA	T16
VCCA	U17
VCCA	U9
VCCA	Y4
VCCDA	A12
VCCDA	A14
VCCDA	AA13
VCCDA	AA15
VCCDA	AA20
VCCDA	AA7
VCCDA	AB13
VCCDA	AC11
VCCDA	AD11
VCCDA	AD4
VCCDA	AE12
VCCDA	AE17
VCCDA	B15
VCCDA	C15
VCCDA	C6
VCCDA	D13
VCCDA	E13
VCCDA	E19
VCCDA	F21
VCCDA	G10
VCCDA	G5
VCCDA	N21
VCCDA	N5
VCCDA	W21
VCCIB0	A3
VCCIB0	B3
VCCIB0	C4
VCCIB0	D5
VCCIB0	J10
VCCIB0	J11
VCCIB0	K12
VCCIB1	A23
VCCIB1	B23
VCCIB1	C22
VCCIB1	D21
VCCIB1	J15

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX2000 Function	Pin Number
VCCIB1	J16
VCCIB1	K14
VCCIB2	C24
VCCIB2	C25
VCCIB2	D23
VCCIB2	E22
VCCIB2	K17
VCCIB2	L17
VCCIB2	M16
VCCIB3	AA22
VCCIB3	AB23
VCCIB3	AC24
VCCIB3	AC25
VCCIB3	P16
VCCIB3	R17
VCCIB3	T17
VCCIB4	AB21
VCCIB4	AC22
VCCIB4	AD23
VCCIB4	AE23
VCCIB4	T14
VCCIB4	U15
VCCIB4	U16
VCCIB5	AB5
VCCIB5	AC4
VCCIB5	AD3
VCCIB5	AE3
VCCIB5	T12
VCCIB5	U10
VCCIB5	U11
VCCIB6	AA4
VCCIB6	AB3
VCCIB6	AC1
VCCIB6	AC2
VCCIB6	P10
VCCIB6	R9
VCCIB6	T9
VCCIB7	C1
VCCIB7	C2
VCCIB7	D3
VCCIB7	E4
VCCIB7	K9
VCCIB7	L9
VCCIB7	M10

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

CG624	
AX2000 Function	Pin Number
VCCPLA	E12
VCCPLB	J12
VCCPLC	E14
VCCPLD	H14
VCCPLE	Y14
VCCPLF	U14
VCCPLG	Y12
VCCPLH	U12
VCOMPLA	F12
VCOMPLB	H12
VCOMPLC	F14
VCOMPLD	J14
VCOMPLE	AA14
VCOMPLF	V14
VCOMPLG	AA12
VCOMPLH	V12
VPUMP	E20

Note:

1. Not routed on the same package layer and to adjacent LGA pads as its differential pair complement. Recommended to be used as a single-ended I/O.

© 2024 Microchip Technology Inc. and its subsidiaries

4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
A	10/2024	The following is the list of changes in revision A of the document: • Migrated this document into Microchip template and updated the Microsemi links with Microchip links. • Updated document number to DS50003755A from 5172160. • Device AX125 has been discontinued in Table 1, Table 2, Table 3, and Table 4. • Package FG676 and CQ352 has been discontinued for device AX500 Table 1, Table 2, and Table 4. • Package FG896 and CG624 has been discontinued for device AX1000 Table 1, Table 2, and Table 4. • Package FG1152 has been discontinued for device AX2000 Table 1, Table 2, and Table 4. • In Table 2-2, under Parameter Range, Ambient temperature is changed to Junction temperature. • In Package Pin Assignments, for AX2000 device in CG624 package pin, E8 function has been updated from GND to GND/LP.
18	03/2012	The following is the list of changes in revision 18 of the document: • Updated Table 2-1 to correct the maximum DC core supply voltage (VCCA) from 1.6 V to 1.7 V (SAR 36786). The maximum input voltage (VI) was corrected from 3.75 V to 4.1 V (SAR 35419). • Added values for tristate leakage current IOZ, and IIH and IIL in table Table 2-3 (SARs 35774, 32021). • Figure 2-2 was updated to correct the units for the resistance from "W" to Ω (SAR 36415). • In User I/Os2 section, the following sentence was added to clarify the slew rate setting (SAR 34943): The slew rate setting is effective for both rising and falling edges. • Figure 2-3 was revised to show the VCCI and GND clamp diodes. The explanatory text above the figure was revised as well (SAR 34942). • Equation for 5 V tolerance was corrected to change Vdiode from 0.6 V to 0.7 V (SAR 36786). • Additional information was added to the Using the Weak Pull-Up and Pull-Down Circuits section to clarify how the weak pull-up and pull-down resistors are physically implemented (SAR 34945). • The description for the CINCLK parameter in Table 2-23 was changed from "Input capacitance on clock pin" to "Input capacitance on HCLK and RCLK pin" (SAR 34944). • Table 2-24 is new (SAR 34942). • The minimum VIL for 1.5 V LVCMOS and PCI was corrected from –0.5 to –0.3 in Table 2-34 and Table 2-37 (SAR 34358). • Support for simulating the GCLR/ GPSET feature in the Axcelerator Family was added in Libero software v9.0 SPI1. Reference to the section explaining this in the Antifuse Macro Library Guide was added to the R-Cell (SAR 26413). • The enable signal in Figure 2-33 was corrected to show it is active low rather than active high (SAR 34946).

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Revision	Date	Description
17	09/2011	The following is the list of changes in revision 17 of the document: • The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The Axcelerator Family Device Status table indicates the status for each device in the device family. • The Features section, Programmable Interconnect Element section, and Security section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 32865). • The C180 package was removed from product tables and the Package Pin Assignments section (PDN 0909). • Package names used in the Table 1 and Package Pin Assignments section were revised to match standards given in Package Mechanical Drawings (SAR 27395). • The section User I/Os2 was updated as follows: "The user does not need to assign VREF pins for OUTBUF and TRIBUF. VREF pins are needed only for input and bidirectional I/Os" (SARs 24181, 24309). • Power values in Table 2-4 were updated to reflect those of SmartPower (SAR 33945). • Two parameter names were corrected in Figure 2-10. One occurrence of tENLZ was changed to tENZL and one occurrence of tENHZ was changed to tENZH (SAR 33890). • The Timing Model section was updated with new timing values. Timing tables in the I/O Specifications section were updated to include enable paths. Values in the timing tables in the Voltage-Referenced I/O Standards section and Differential Standards section were updated. • Table 2-67 was updated (SAR 33945). • Figure 2-11 was replaced (SAR 33043). • The timing tables for RAM and FIFO were updated (SAR 33945). • "Data Registers (DRs)" values were modified for IDCODE and USERCODE (Data Registers (DRs) SARs 18257, 26406). • The package diagram for the CQ208 package was incorrect and has been replaced with the correct diagram (SARs 23865, 26345).
16	10/2010	The following is the list of changes in revision 16 of the document: • The datasheet was updated to include AX2000-CQ2526 information. • MIL-STD-883 Class B is no longer supported by Axcelerator FPGAs and as a result was removed. • A footnote was added to the Axcelerator Clock Management System section.
15	11/2008	The following is the list of changes in revision 15 of the document: • RoHS-compliant information was added to the Ordering Information. • ACTgen was changed to SmartGen because ACTgen is obsolete.
14	—	The following is the list of changes in revision 14 of the document: • In Table 2-4, the units for the PLOAD, P10, and PI/O were updated from mW/MHz to mW/MHz. • In the Pin Descriptions section, the HCLK and CLK descriptions were updated to include tie-off information. • The Global Resource Distribution section was updated. • The CG624 table was updated.
13	—	The following is the list of changes in revision 13 of the document: • A note was added to Table 2-2. • In the Package Thermal Characteristics, the temperature was changed from 150°C to 125°C.
12	—	The following is the list of changes in revision 12 of the document: • Revised Ordering Information and timing data to reflect phase out of –3 speed grade options. • Table 2-3 was updated.

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Revision	Date	Description
11	—	The following is the list of changes in revision 11 of the document: • The Packaging Data section is new. • Table 2-2 was updated. • Table 2-8 was updated. • Table 2-11 was updated. • The User I/Os2 was updated.
10	—	The following is the list of changes in revision 10 of the document: • Figure 1-3 was updated. • Table 2-2 was updated. • The Power-Up/Down Sequence section was updated. • Table 2-4 was updated. • Table 2-5 was updated. • The Timing Characteristics section was added. • Table 2-7 was updated. • Figure 2-1 was updated. • The External Setup and Clock-to-Out (Pad-to-Pad) equations in the Hardwired Clock—Using LVTTL 24 mA High Slew Clock I/O section were updated. • The External Setup and Clock-to-Out (Pad-to-Pad) in the Routed Clock—Using LVTTL 24 mA High Slew Clock I/O section were updated. • The Global Pins section was updated. • The User I/Os2 section was updated. • Table 2-22 was updated. • Figure 2-8 was updated. • Figure 2-13 and Figure 2-14 were updated. • The following timing parameters were renamed in I/O timing characteristic tables from Table 2-27 to Table 2-64: tIOCLKQ > tICLKQ tIOCLKY > tOCLKQ • Timing numbers were updated from Table 2-27 to Table 2-82. • The R-Cell section was updated. • Figure 2-60 was updated. • Figure 2-61 was updated. • Figure Figure 2-68 was updated. • Figure 2-69 was updated. • Table 2-93 to Table 2-97 were updated. • Table 2-102 to Table 2-106 were updated. • The TRST section was updated. • The Global Set Fuse section was added. • A footnote was added to FG896 for the AX2000 regarding pins AB1, AE2, G1, and K2. • Pinouts for the AX250, AX500, and AX1000 were added for CQ352. • Pinout for the AX1000 was added for CG624.
9.0	—	The following is the list of changes in revision 9.0 of the document: • Table 2-83 was updated. • The Low Power Mode section was updated.

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Revision	Date	Description
8.0	—	The following is the list of changes in revision 8.0 of the document: • Table 1 has been updated. • The Ordering Information section has been updated. • The Device Resources section has been updated. • The Temperature Grade Offerings section is new. • The Speed Grade and Temperature Grade Matrix section has been updated. • Table 2-14 has been updated. • Table Table 2-15 has been updated. • Table 2-1 has been updated. • Table 2-2 has been updated. • Table 2-3 has been updated. • Table 2-4 has been updated. • Table 2-5 has been updated. • The Power Estimation Example section has been updated. • The Thermal Characteristics section has been updated. • The Package Thermal Characteristics section has been updated. • The Timing Characteristics section has been updated. • The Pin Descriptions section has been updated. • Timing numbers have been updated from the 3.3V LVTTL section to the Timing Characteristics section. Many AC Loads were updated as well. • Timing characteristics for the Hardwired Clocks and Routed Clocks sections were updated. • Table 2-93 to Table 2-96 and Table 2-102 to Table 2-99 were updated. • The following sections were updated: Low Power Mode, Interface, Data Registers (DRs), Security, Silicon Explorer II Probe Interface, and Programming. • In the PQ208 (AX500) section, pins 2, 52, and 156 changed from VCCDA to VCCA. For pins 170 and 171, the I/O names refer to pair 23 instead of 24. • The following changes were made in the FG676 (AX500) section: AE2, AE25 Change from NC to GND. AF2, AF25 Changed from GND to NC AB4, AF24, C1, C26 Changed from VCCDA to VCCA AD15 Change from VCCDA to VCOMPLE AD17 Changed from VCOMPLE to VCCDA • In the FG896 (AX2000) section, the AK28 changed from VCCIB5 to VCCIB4. • The CQ352 and CG624 sections are new.
7.0	—	The following is the list of changes in revision 7.0 of the document: • All I/O FIFO capability was removed. • Table 1 was updated. • Figure 1-9 was updated. • Figure 2-5 was updated. • The Using an I/O Register section was updated. • The AX250 and AX1000 descriptions were added to the FG484 section.
6.0	—	The following is the list of changes in revision 6.0 of the document: • Table 2-3 was updated. • Figure 2-1 was updated. • Figure 2-49 was updated. • Figure 2-53 was updated.

© 2024 Microchip Technology Inc. and its subsidiaries

.....continued

Revision	Date	Description
5.0	—	The following is the list of changes in revision 5.0 of the document: • In the PQ208 table, pin 196 was missing, but it has been added in this version with a function of GND. • The following pins in the FG484 table for AX500 were changed: Pin G7 is GND/LP Pins AB8, C10, C11, C14, AB16 are NC. • The FG676 table was updated.
4.0	—	The following is the list of changes in revision 4.0 of the document: • The Device Resources section was updated for the CS180. • The Programmable Interconnect Element and Figure 1-2 are new. • The "CS180" table is new. • The PQ208 tables for the AX500 were updated. The following pins were not defined in the previous version: GND 21 IO106PB5F10/CLKHP 71 GND 136
3.0	—	The following is the list of changes in revision 3.0 of the document: • Table 1, Ordering Information, Device Resources, and the Product Plan table were updated. • The following figures and tables were updated: – Figure 1-3 – Figure 1-8 – Table 2-3 – Table 2-13 – Figure 2-2 – Figure 2-11 • The Design Environment section was updated. • The Package Thermal Characteristics was updated. • The timing characteristics tables fromTable 2-27 to Table 2-68 were updated. • The Global Resources section was updated. • The timing characteristics tables from Table 2-102 and Table 2-103 were updated. • The PQ208, FG256, and FG324 tables are new.

© 2024 Microchip Technology Inc. and its subsidiaries

Microchip Information

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable". Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure

© 2024 Microchip Technology Inc. and its subsidiaries

that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, TimeCesium, TimeHub, TimePictra, TimeProvider, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, EyeOpen, GridTime, IdealBridge, IGaT, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, MarginLink, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mSiC, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, Power MOS IV, Power MOS 7, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, Turing, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

© 2024 Microchip Technology Inc. and its subsidiaries

All other trademarks mentioned herein are property of their respective companies.

© 2024, Microchip Technology Incorporated and its subsidiaries. All Rights Reserved.

ISBN: 978-1-6683-0312-2

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4485-5910 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-72400 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Hod Hasharon** Tel: 972-9-775-5100 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-72884388 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820

© 2024 Microchip Technology Inc. and its subsidiaries

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View AX250-PQ208M on WIN SOURCE
- Microchip Technology Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management