PE426462

Document category: Product Specification

UltraCMOS® SP6T RF Switch, 10 MHz–8 GHz

Features

- High isolation: 35 dB @ 6 GHz
- Low insertion loss: 1.1 dB @ 6 GHz
- RF T_{RISE}/T_{FALL} time: 100 ns
- Power handling: 31 dBm CW
- Logic Select (LS) pin provides maximum control logic flexibility
- Terminated all-off state mode
- Operating temperature: –55 °C to +125 °C
- Packaging: 24-lead 4 × 4 × 0.85 mm QFN

Applications

- Harsh industrial applications up to 8 GHz
- Applications that require extended temperature support in the –55 °C to +125 °C range
- Filter bank switching
- RF signal routing

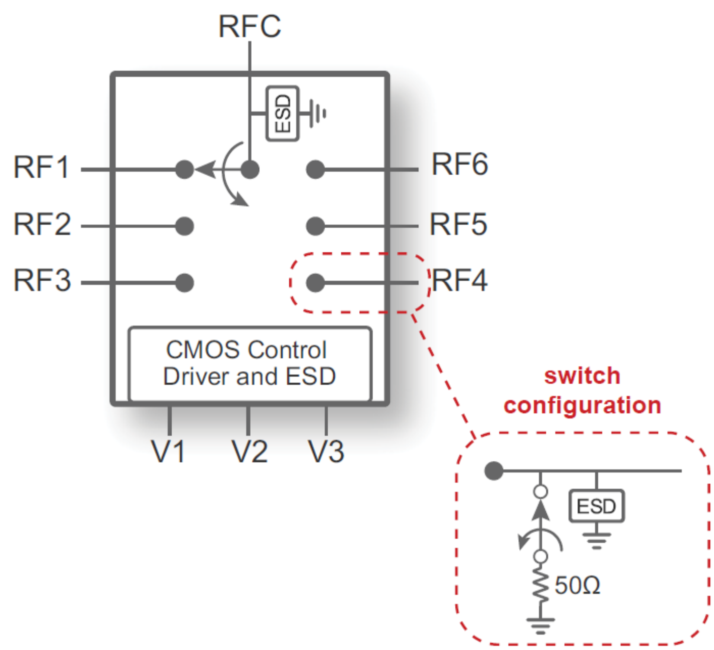


Figure 1. PE426462 functional diagram

Product description

The PE426462 is a HaRP™ technology-enhanced absorptive SP6T RF switch that supports the 10 MHz to 8 GHz frequency range. It delivers low insertion loss, fast RF T_{RISE}/T_{FALL} time, and high isolation in the operating temperature range from –55 °C to +125 °C. It is ideal for harsh industrial applications that require extended support in this temperature range. No blocking capacitors are required if DC voltage is not present on the RF ports.

The PE426462 is manufactured on pSemi's UltraCMOS® process, a patented advanced form of silicon-on-insulator (SOI) technology.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. Absolute maximum ratings

Parameter or condition	Min	Max	Unit
Supply voltage, VDD	–0.3	5.5	V
Digital input voltage (V1, V2, V3, LS)	–0.3	3.6	V
RF input power (RFC–RFx, 50Ω)	–	See Figure 2	dBm
RF input power into terminated ports, CW (RFx, 50Ω)(1)	–	See Figure 2	dBm
Maximum junction temperature	–	+150	°C
Storage temperature range	–65	+150	°C
ESD voltage HBM, all pins(2)	–	1000	V
ESD voltage CDM, all pins(3)	–	1000	V

Notes:
1. 100% duty cycle, all bands, 50Ω
2. Human body model (MIL-STD 883 Method 3015)
3. Charged device model (JEDEC JESD22-C101)

Recommended operating conditions

Table 2 lists the PE426462 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. Operating conditions

Parameter	Min	Typ	Max	Unit
Supply voltage, V_{DD}	2.3	3.3	5.5	V
Supply current, I_{DD}	–	120	200	µA
Digital input high (V1, V2, V3, LS)	1.17	–	3.6	V
Digital input low (V1, V2, V3, LS)	–0.3	–	0.6	V
Digital input current (V1, V2, V3)	–	–	5	µA
Digital input current (LS)	–	–	10	µA
RF input power, CW (RFC–RFx)(1)	–	–	See Figure 2	dBm
RF input power, pulsed (RFC–RFx)(2)	–	–	See Figure 2	dBm
RF input power into terminated ports, CW (RFx)(1)	–	–	See Figure 2	dBm
Operating temperature range	–55	+25	+125	°C

Notes:

- 100% duty cycle, all bands, 50Ω
- Pulsed, 5% duty cycle of 4620-µs period, 50Ω

Electrical specifications

Table 3 lists the PE426462 key electrical specifications at +25 °C T_{CASE} and V_{DD} = 3.3V (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3. Electrical specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	10 MHz	–	8 GHz	As shown
Insertion loss[1]	RFC–RF1/6	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	–	0.7 0.8 0.9 0.9 1.1 1.6	0.9 1.0 1.2 1.5 1.9 2.8	dB
	RFC–RF2/5	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	–	0.8 0.9 0.9 1.0 1.3 1.3	1.0 1.1 1.3 1.6 2.3 2.4	dB
	RFC–RF3/4	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	–	0.8 0.9 1.0 1.1 1.2 1.3	1.0 1.1 1.3 1.7 2.2 2.2	dB
Isolation[1]	RFC–RF1/6	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	61 45 40 34 29 27	65 47 42 36 32 30	–	dB
	RFC–RF2/5	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	64 52 47 42 30 29	68 55 51 44 34 34	–	dB
	RFC–RF3/4	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	64 51 46 38 33 29	68 53 48 40 35 31	–	dB
Return loss (active port)	RFC–RF1/6	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	–	25 24 24 21 26 13	–	dB

Parameter	Path	Condition	Min	Typ	Max	Unit
	RFC–RF2/5	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	–	24 23 20 18 15 16	–	dB
	RFC–RF3/4	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	–	24 23 18 15 12 12	–	dB
Return loss (RFC port)	RFC–RF1/6	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	–	25 23 24 23 24 12	–	dB
	RFC–RF2/5	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	–	24 23 21 19 20 18	–	dB
	RFC–RF3/4	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	–	24 23 19 16 13 13	–	dB
Return loss (terminated port)	RFC–RF1/6	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	–	16 15 15 15 18 21	–	dB
	RFC–RF2/5	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	–	16 15 15 15 18 19	–	dB
	RFC–RF3/4	10–100 MHz 100 MHz–1 GHz 1–2 GHz 2–4 GHz 4–6 GHz 6–8 GHz	–	16 15 15 15 16 19	–	dB

Parameter	Path	Condition	Min	Typ	Max	Unit
Relative insertion phase(2)	RF2–RF1 (RF5–RF6)	1 GHz 2 GHz 4 GHz 6 GHz 8 GHz	–2.6 –4.7 –7.5 –9.4 –1.4	–1.3 –2.4 –3.4 –2.8 4.4	0 –0.1 0.8 3.8 10.1	deg
	RF3–RF1 (RF4–RF6)	1 GHz 2 GHz 4 GHz 6 GHz 8 GHz	–3.0 –5.8 –9.3 –11.2 –10.2	–2.1 –4.0 –5.6 –5.7 –1.0	–1.3 –2.1 –1.9 –0.3 8.2	deg
Input 1-dB compression point(3)	RFC–RFx	–	–	See Figure 2	–	dBm
Input 0.1-dB compression point(3)	RFC–RFx	–	–	See Figure 2	–	dBm
Input IP2	RFC–RFx	100 MHz–8 GHz	–	105	–	dBm
Input IP3	RFC–RFx	100 MHz–8 GHz	–	60	–	dBm
RF T_{RISE}/T_{FALL}	–	10%/90% RF	–	100	130	ns
Settling time	–	50% CTRL to 0.05 dB final value	–	560	920	ns
Switching time	–	50% CTRL to 90% or 10% of RF	–	210	270	ns

Notes:
1. Insertion loss and isolation performance can be improved by a good RF ground on LS (pin 1).
2. Defined with S-parameters, relative insertion phase (RFx–RF1) = ∠S(x+1)1 – ∠S21, where incident Port-1 is RFC, response Port-2 = RF1, and response Port-(x+1) = RFx.
3. The input 1-dB and 0.1-dB compression points are linearity figures of merit. For the RF input power (50Ω), see Table 2.

Switching frequency

The PE426462 has a maximum 25 kHz switching frequency. The switching frequency describes the time duration between switching events. The switching time is the time duration between the point that the control signal reached 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

Spurious performance

The PE426462 spur fundamental occurs around 5 MHz. Its typical performance is –162 dBm/Hz, with 30 kHz bandwidth.

Hot-switching capability

The PE426462 maximum hot switching capability is 18 dBm above 100 MHz. Hot switching occurs when RF power is applied while switching between RF ports.

Thermal data

The junction top-of-package, Psi-JT (Ψ_{JT}), is a thermal metric to estimate the junction temperature of the device in an application PCB, per JEDEC JESD51-2:

$$\Psi_{JT} = (T_J - T_T)/P$$

where:

- Ψ_{JT} = Junction-to-top of package characterization parameter in °C/W
- T_J = Die junction temperature in °C
- T_T = Package temperature (top surface, in the center) in °C
- P = Power dissipated by the device in Watts

Table 4. Thermal data

Parameter	Typ	Unit
Junction top-of-package, Ψ_{JT}	23	°C/W
Junction-to-ambient thermal resistance, Θ_{JA}	63	°C/W

Control logic

Table 5 lists the PE426462 control logic truth table.

Table 5. Truth table

LS(1)	V3	V2	V1	RFC–RF1	RFC–RF2	RFC–RF3	RFC–RF4	RFC–RF5	RFC–RF6
0	0	0	0	ON	OFF	OFF	OFF	OFF	OFF
0	1	0	0	OFF	ON	OFF	OFF	OFF	OFF
0	0	1	0	OFF	OFF	ON	OFF	OFF	OFF
0	1	1	0	OFF	OFF	OFF	ON	OFF	OFF
0	0	0	1	OFF	OFF	OFF	OFF	ON	OFF
0	1	0	1	OFF	OFF	OFF	OFF	OFF	ON
1	1	0	1	ON	OFF	OFF	OFF	OFF	OFF
1	0	0	1	OFF	ON	OFF	OFF	OFF	OFF
1	1	1	0	OFF	OFF	ON	OFF	OFF	OFF
1	0	1	0	OFF	OFF	OFF	ON	OFF	OFF
1	1	0	0	OFF	OFF	OFF	OFF	ON	OFF
1	0	0	0	OFF	OFF	OFF	OFF	OFF	ON
X(2)	0	1	1	OFF	OFF	OFF	OFF	OFF	OFF

Notes:
1. LS has an internal 1 MΩ pull-up resistor to logic high. To generate a logic 0, connect LS to GND externally. Leaving LS floating generates a logic 1.
2. LS = don't care, V3 = 0, V2 = V1 = 1, all ports are terminated to provide an all-isolated state.

Power derating curve

The power derating curve in Figure 2 shows the P1-dB compression, P0.1-dB compression, maximum RF input power (pulsed), maximum RF input power (CW), absolute maximum RF terminated power (CW), and the maximum RF terminated power (CW).

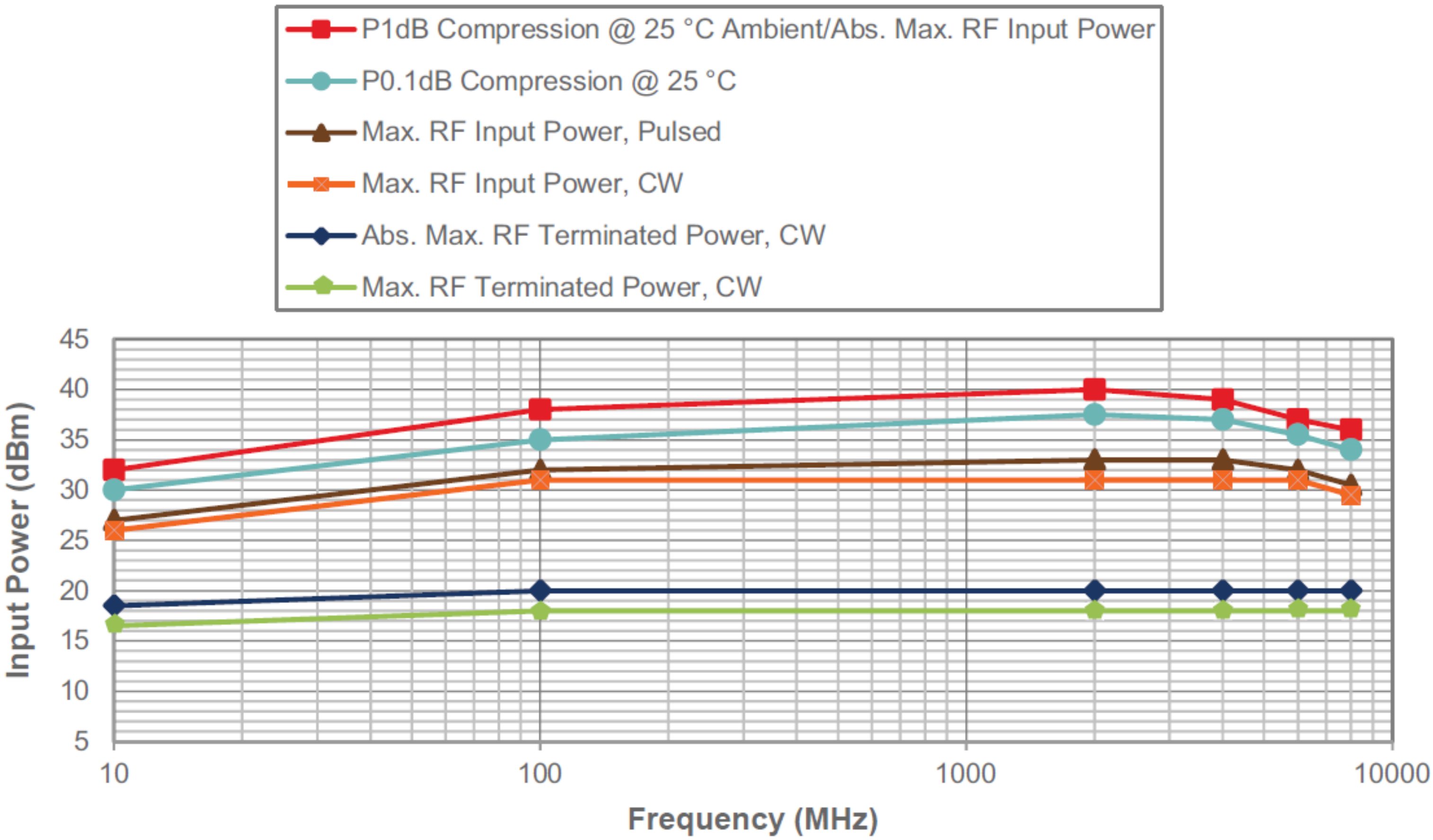


Figure 2. Power derating curve, 10 MHz–8 GHz, –55 °C to +125 °C ambient, 50Ω

Isolation matrix

Table 6 lists the RFC-to-port isolation and Table 7 lists the port-to-port isolation at +25 °C and V_{DD} = 3.3V (ZS = ZL = 50Ω).

Table 6. RFC-to-port isolation

ON port	Frequency	Isolation (dB)					
		RF1	RF2	RF3	RF4	RF5	RF6
RF1	10–100 MHz	–	69	68	88	87	79
	100 MHz–1 GHz		62	53	66	64	57
	1–2 GHz		57	48	60	58	51
	2–4 GHz		48	40	54	52	45
	4–6 GHz		37	35	50	46	42
	6–8 GHz		34	31	47	45	38
RF2	10–100 MHz	67	–	69	88	86	77
	100 MHz–1 GHz	52		60	66	64	56
	1–2 GHz	46		57	60	57	50
	2–4 GHz	39		49	53	52	45
	4–6 GHz	32		43	50	46	42
	6–8 GHz	30		37	47	46	40
RF3	10–100 MHz	65	68	–	88	85	77
	100 MHz–1 GHz	47	55		66	63	55
	1–2 GHz	42	51		60	57	50
	2–4 GHz	36	44		53	52	45
	4–6 GHz	33	40		49	47	42
	6–8 GHz	31	36		46	47	40
RF4	10–100 MHz	73	84	88	–	68	66
	100 MHz–1 GHz	51	62	65		56	50
	1–2 GHz	45	56	59		51	45
	2–4 GHz	40	49	53		46	39
	4–6 GHz	37	46	49		38	35
	6–8 GHz	34	44	45		37	33
RF5	10–100 MHz	73	84	89	69	–	68
	100 MHz–1 GHz	51	62	65	60		57
	1–2 GHz	45	56	59	57		52
	2–4 GHz	40	49	53	50		44
	4–6 GHz	37	45	49	41		33
	6–8 GHz	34	43	46	38		33
RF6	10–100 MHz	74	84	87	68	69	–
	100 MHz–1 GHz	52	62	66	54	65	
	1–2 GHz	46	57	60	48	60	
	2–4 GHz	40	49	53	41	51	
	4–6 GHz	37	46	49	35	34	
	6–8 GHz	33	42	46	31	35	

Table 7. Port-to-port isolation

ON port	Frequency	Isolation (dB)					
		RF1	RF2	RF3	RF4	RF5	RF6
RF1	10–100 MHz	–	65	67	89	89	88
	100 MHz–1 GHz		47	51	69	71	64
	1–2 GHz		41	45	63	65	60
	2–4 GHz		35	39	57	60	53
	4–6 GHz		31	34	52	47	45
	6–8 GHz		29	30	49	47	43
RF2	10–100 MHz	65	–	64	91	92	89
	100 MHz–1 GHz	46		45	70	75	74
	1–2 GHz	41		39	64	69	72
	2–4 GHz	35		34	58	64	63
	4–6 GHz	32		30	53	50	51
	6–8 GHz	29		27	50	50	51
RF3	10–100 MHz	67	65	–	90	92	91
	100 MHz–1 GHz	51	47		70	78	80
	1–2 GHz	46	41		64	72	79
	2–4 GHz	40	36		58	66	68
	4–6 GHz	37	33		53	51	54
	6–8 GHz	33	30		50	51	54
RF4	10–100 MHz	90	92	89	–	65	67
	100 MHz–1 GHz	77	82	70		47	51
	1–2 GHz	65	75	65		42	45
	2–4 GHz	56	66	58		36	39
	4–6 GHz	49	52	53		32	35
	6–8 GHz	46	53	50		31	32
RF5	10–100 MHz	92	92	89	64	–	64
	100 MHz–1 GHz	85	77	70	45		45
	1–2 GHz	70	72	64	39		40
	2–4 GHz	57	64	58	34		35
	4–6 GHz	48	52	53	30		29
	6–8 GHz	46	51	50	27		30
RF6	10–100 MHz	87	91	88	67	65	–
	100 MHz–1 GHz	69	73	69	51	47	
	1–2 GHz	67	67	63	45	41	
	2–4 GHz	56	61	57	39	35	
	4–6 GHz	46	49	52	34	29	
	6–8 GHz	42	49	49	30	29	

Typical performance data

Figure 3–Figure 20 show the typical performance data at +25 °C and V_{DD} = 3.3V (Z_S = Z_L = 50Ω), unless otherwise specified.

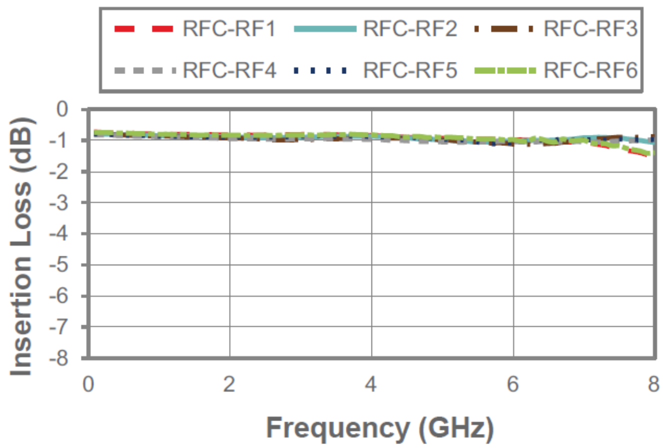


Figure 3. Insertion loss vs. frequency (RFC–RFx)

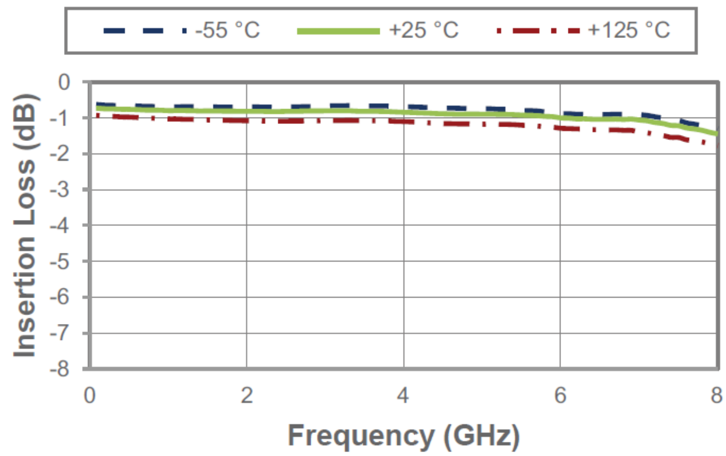


Figure 4. Insertion loss vs. frequency over temperature (RFC–RF1)

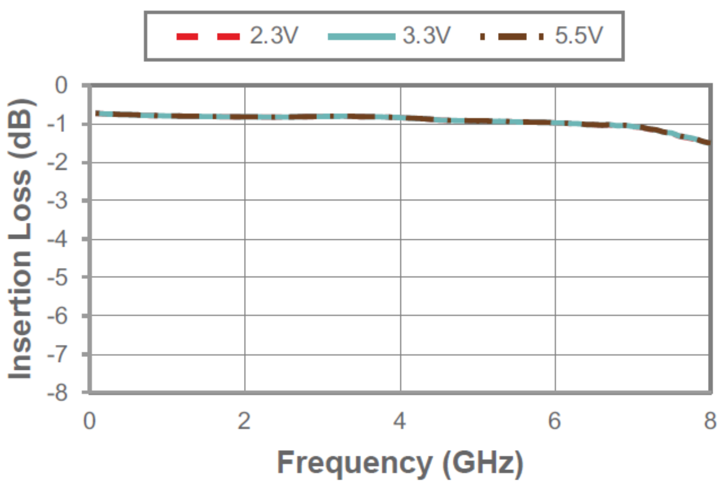


Figure 5. Insertion loss vs. frequency over V_{DD} (RFC–RF1)

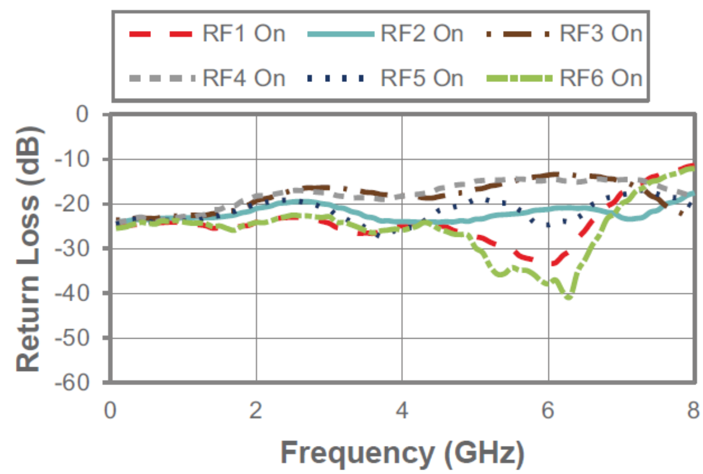


Figure 6. RFC port return loss vs. frequency

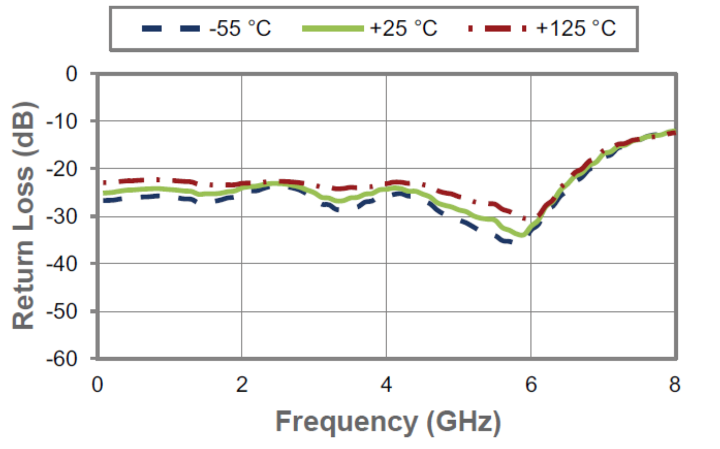


Figure 7. RFC port return loss vs. frequency over temperature (RF1 on)

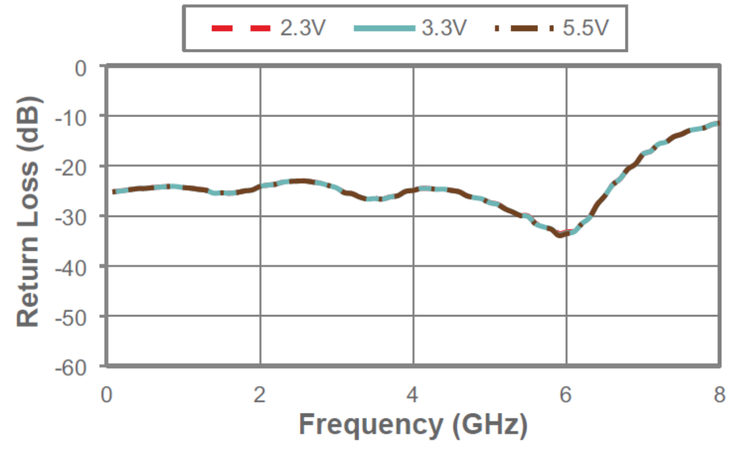


Figure 8. RFC port return loss vs. frequency over V_{DD} (RF1 on)

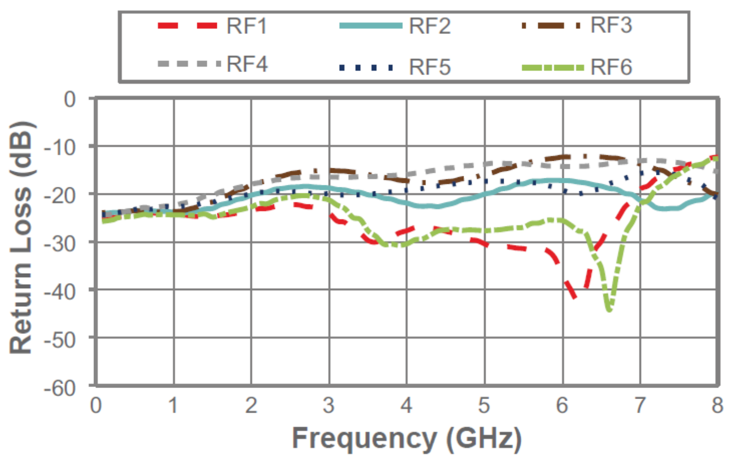


Figure 9. Active port return loss vs. frequency

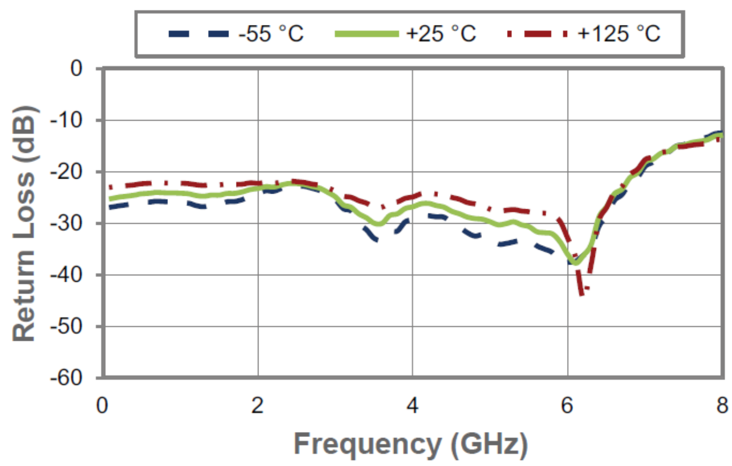


Figure 10. RF1 active port return loss vs. frequency over temperature

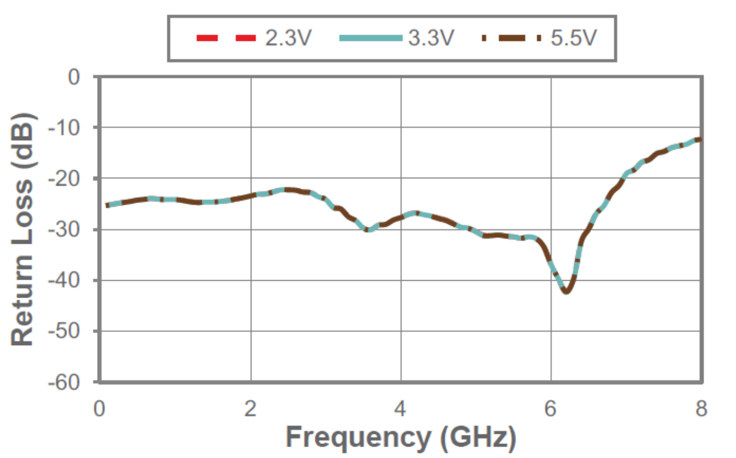


Figure 11. RF1 active port return loss vs. frequency over V_{DD}

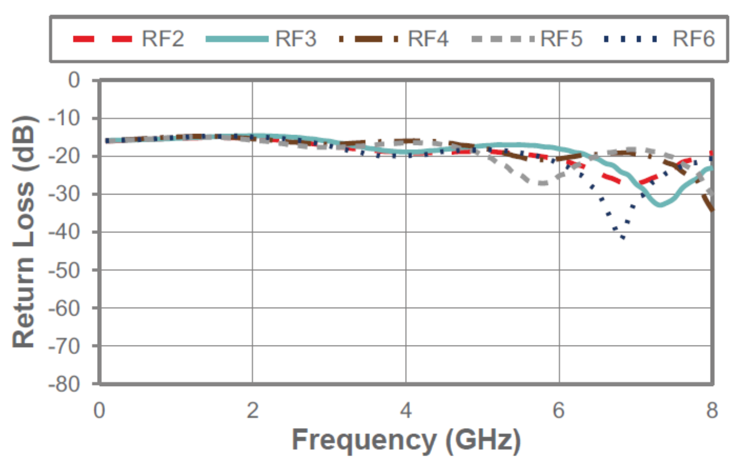


Figure 12. Terminated port return loss vs. frequency (RF1 on)

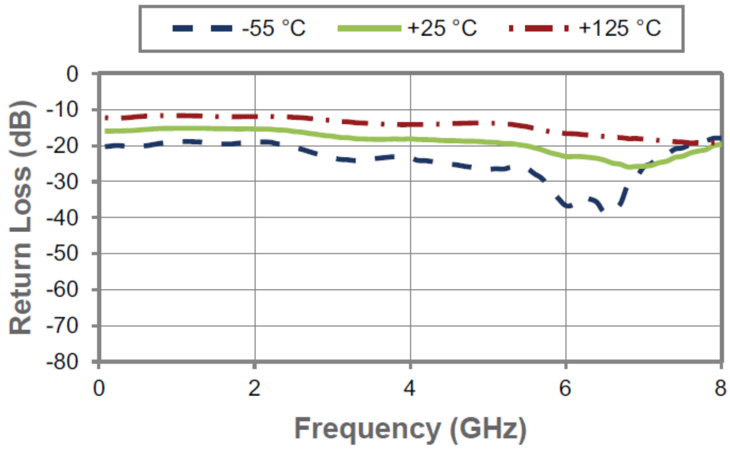


Figure 13. RF2 terminated port return loss vs. frequency over temperature (RF1 on)

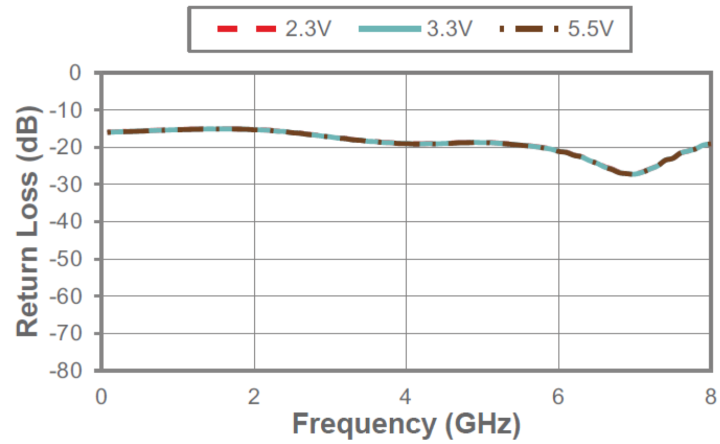


Figure 14. RF2 terminated port return loss vs. frequency over V_{DD} (RF1 on)

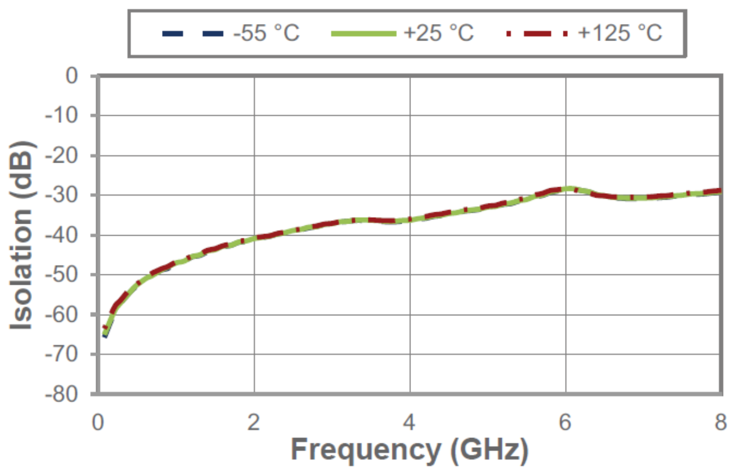


Figure 15. Isolation vs. frequency over temperature (RF1–RF2, RF1 on)

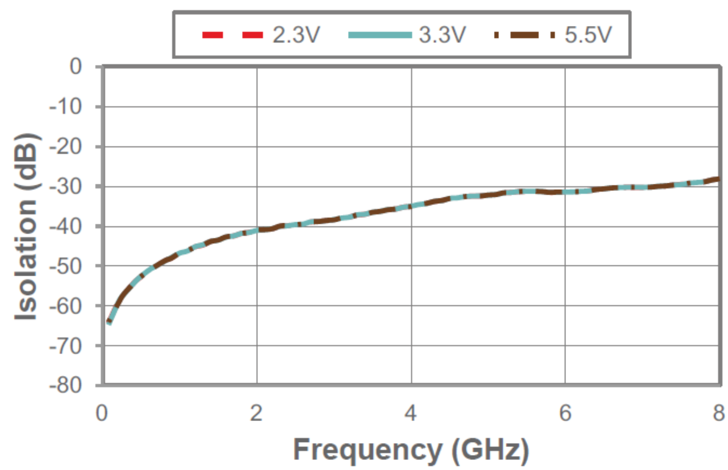


Figure 16. Isolation vs. frequency over V_{DD} (RF1–RF2, RF1 on)

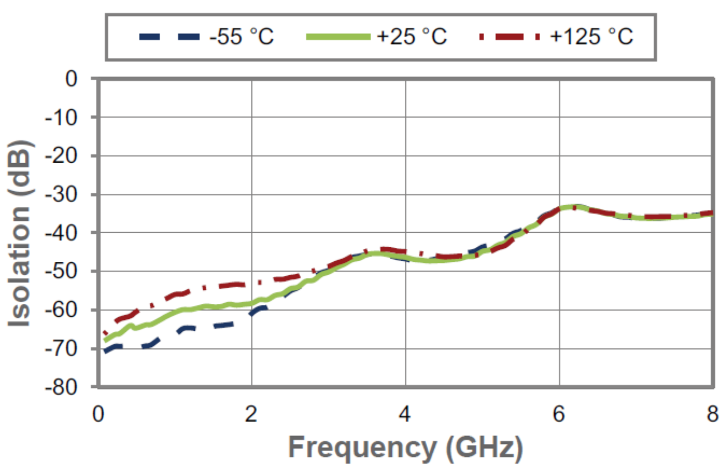


Figure 17. Isolation vs. frequency over temperature (RFC–RF2, RF1 on)

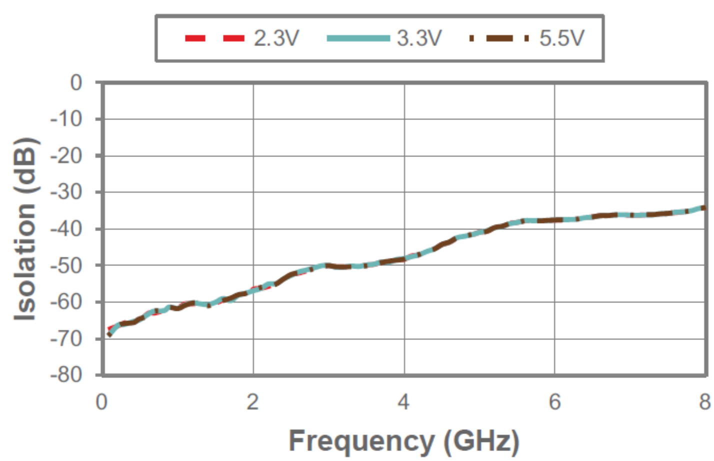


Figure 18. Isolation vs. frequency over V_{DD} (RFC–RF2, RF1 on)

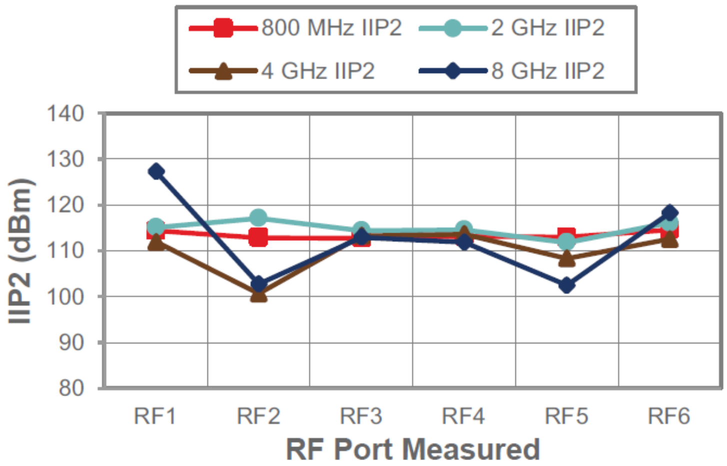


Figure 19. IIP2 vs. RF port measured

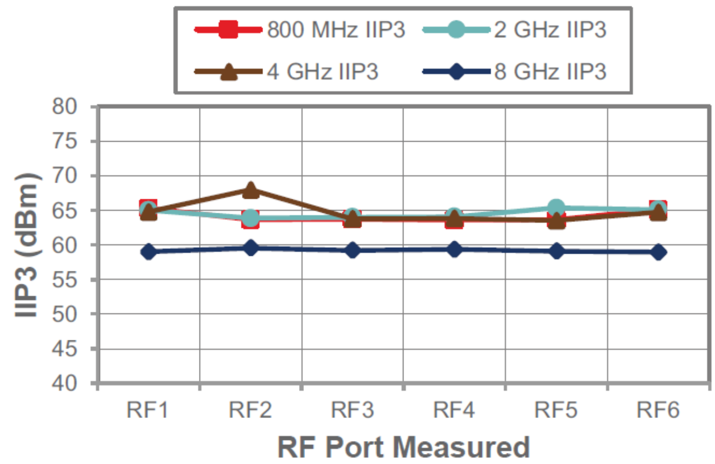


Figure 20. IIP3 vs. RF port measured

Evaluation kit

The high-throw count RF switch evaluation kit (EVK) includes hardware required to control and evaluate the functionality of the high-throw count switches. You can download the high-throw count RF switch evaluation software at http://www.psemi.com. The software requires a PC running the Windows® operating system to control the USB interface board. For more information, see the *Multi-throw Count RF Switch Evaluation Kit (EVK) User's Manual*.

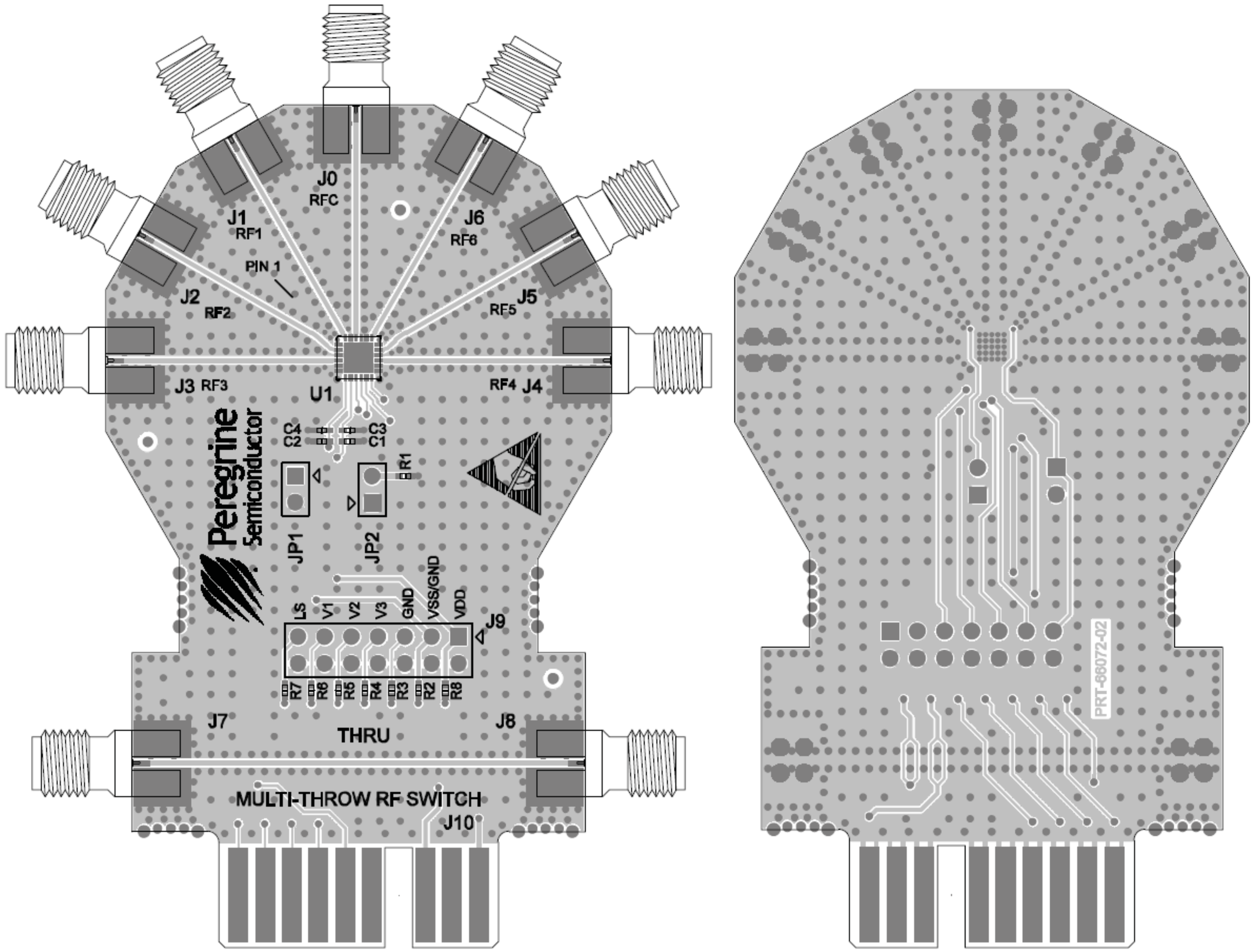


Figure 21. PE426462 evaluation board layout

Pin configuration

Figure 22 shows the PE426462 pin configuration for the 24-lead 4 × 4 × 0.85 mm QFN package, and Table 8 lists the description for each pin.

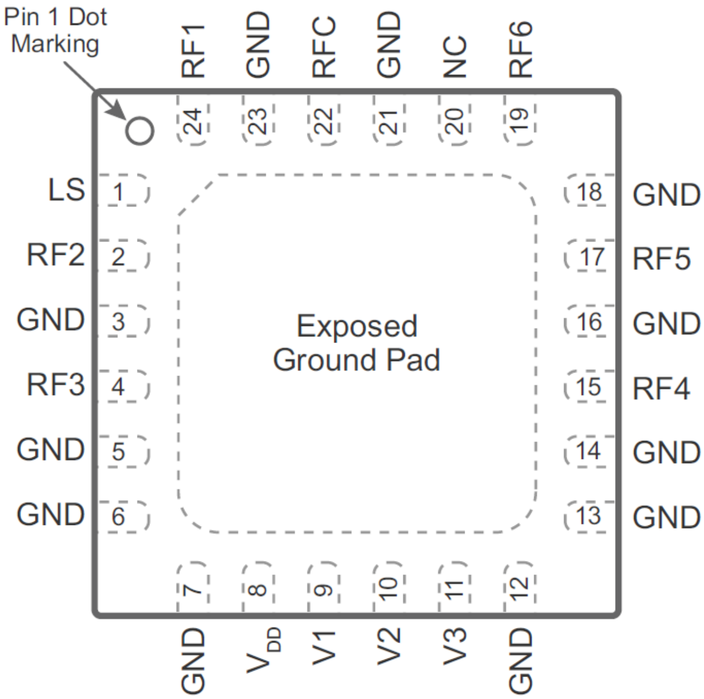


Figure 22. Pin configuration, top view

Table 8. Pin descriptions

Pin no.	Pin name	Description
1	LS	Logic Select. Determines the definition for the V1, V2, and V3 pins.
2[(1)]	RF2	RF port 2
3, 5–7, 12–14, 16, 18, 21, 23	GND	Ground
4[(1)]	RF3	RF port 3
8	V_{DD}	Nominal 3.3V supply voltage
9	V1	Digital control logic input 1
10	V2	Digital control logic input 2
11	V3	Digital control logic input
15[(1)]	RF4	RF port 4
17[(1)]	RF5	RF port 5
19[(1)]	RF6	RF port 6
20[(2)]	NC	No connect
22[(1)]	RFC	RF common port
24[(1)]	RF1	RF port 1
Pad	GND	Exposed pad. Ground for proper operation.

Notes:
1. RF pins 2, 4, 15, 17, 19, 22, and 24 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Pin 20 (NC) can be connected to GND or left not connected externally

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE426462 moisture sensitivity level rating for the 24-lead 4 × 4 × 0.85 mm QFN package is MSL1.

Package drawing

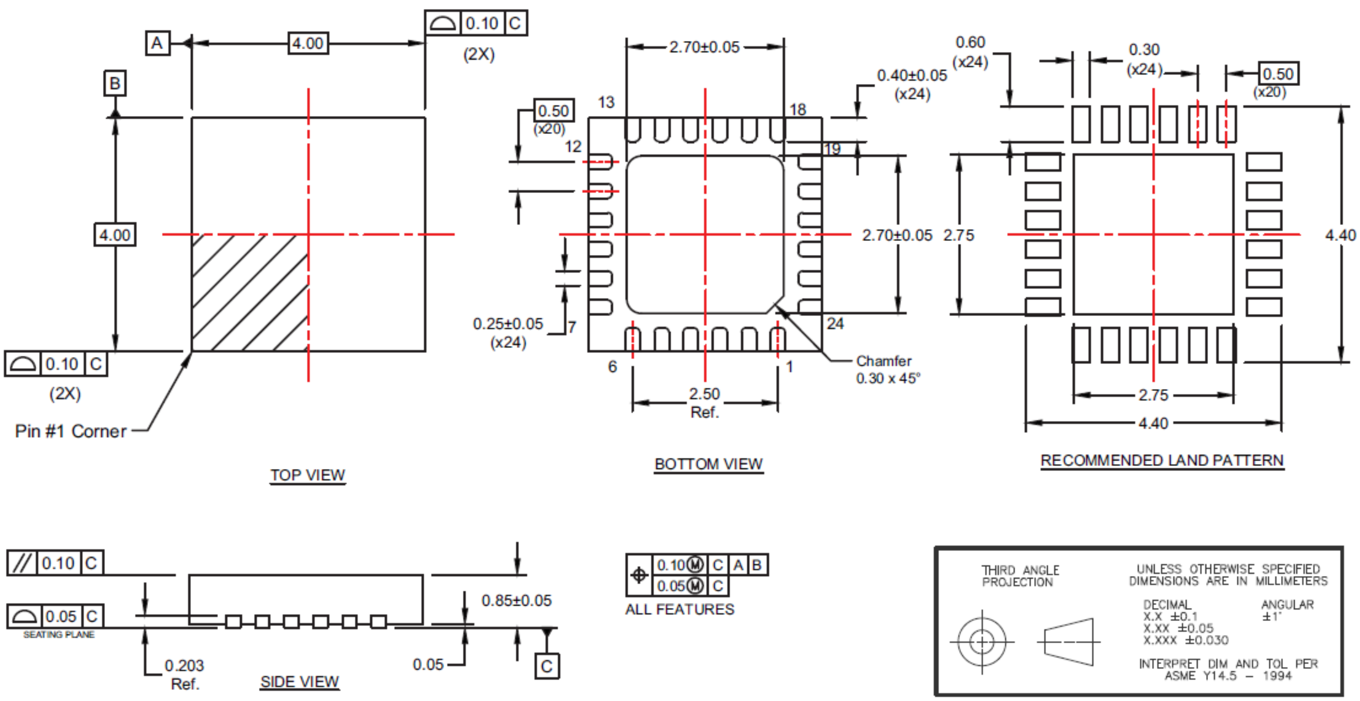
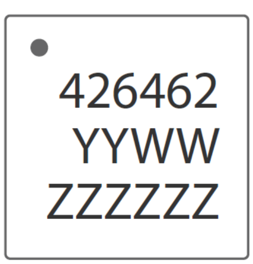


Figure 23. Package mechanical drawing for the 24-lead 4 × 4 × 0.85 mm QFN package

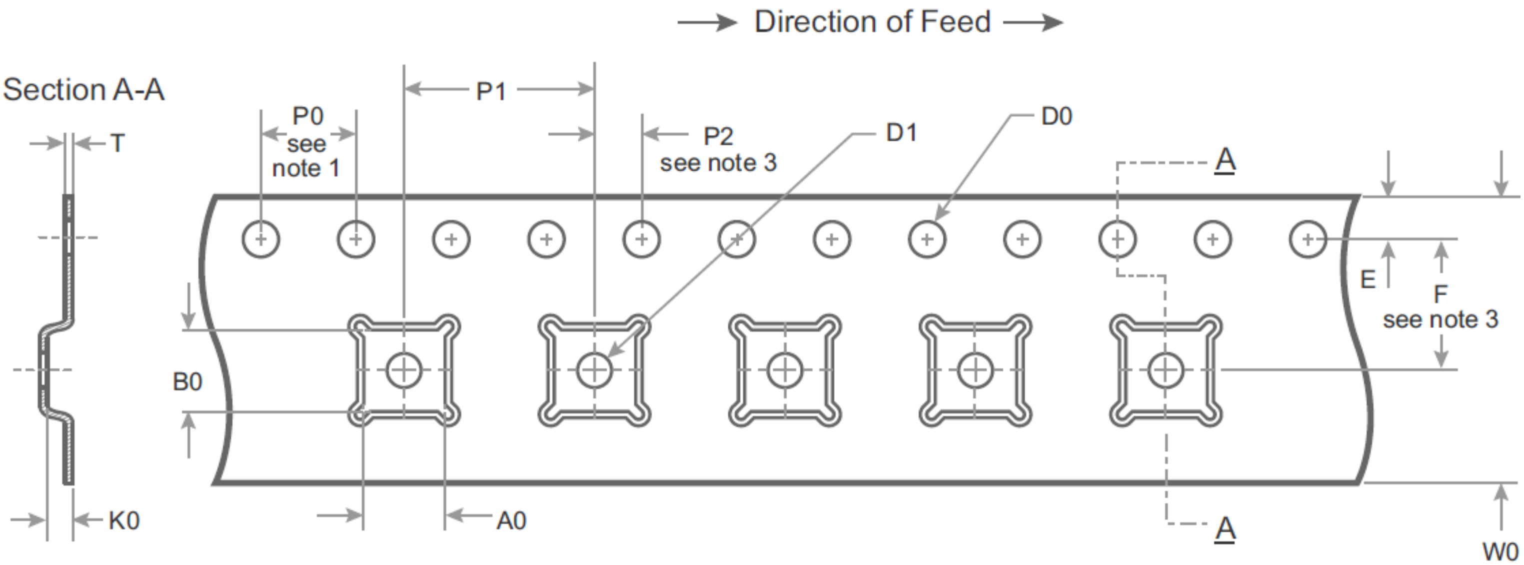
Top-marking specification



● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZ = Assembly lot code

Figure 24. Package marking specification

Tape and reel specification

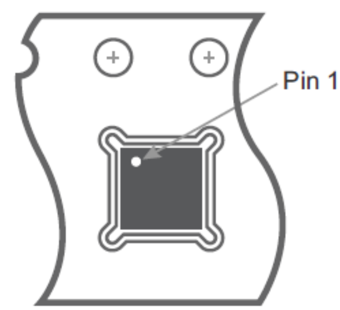


A0	4.35
B0	4.35
K0	1.10
D0	1.50 + 0.10/ -0.00
D1	1.50 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	12.00 ± 0.30

Notes:

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions are in millimeters unless otherwise specified



Device Orientation in Tape

Figure 25. Tape and reel specification for the 24-lead 4 × 4 × 0.85 mm QFN package

Ordering information

Order code	Description	Packaging	Shipping method
PE426462A-X	PE426462 SP6T RF switch	Green 24-lead 4 × 4 × 0.85 mm QFN	500 units/T&R
EK426462-02	PE426462 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
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