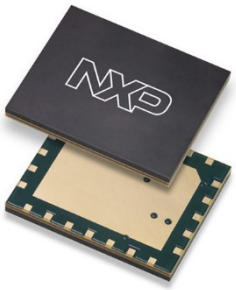
A5M20TG042

Airfast Power Amplifier Module

Rev. 1 — 20 May 2024 **Product data sheet**



1 General description

The A5M20TG042 is a Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells and low power remote radio heads. The field-proven LDMOS and GaN integrated power amplifiers are designed for TDD and FDD 32T mMIMO systems.

2 Features and benefits

- 3-stage module solution that includes a 2-stage LDMOS integrated circuit as a driver and a GaN final stage amplifier
- Advanced high performance in-package Doherty
- Fully matched (50 ohm input/output, DC blocked)
- Reduced memory effects for improved linearized error vector magnitude
- Simultaneous dual band operation (B3–B1/B66)

3 Typical performance

Table 1. 1805–2200 MHz — Typical LTE performance

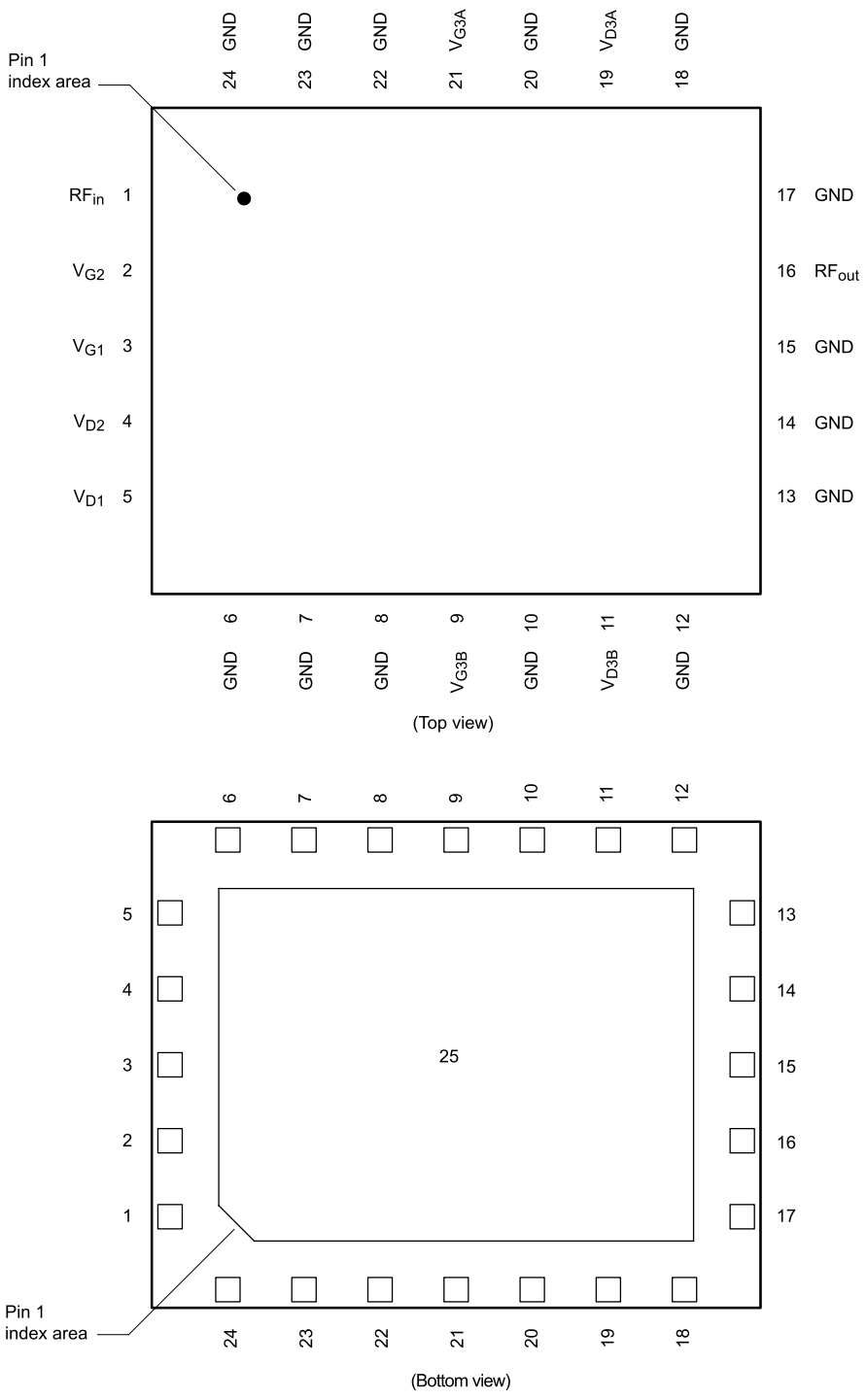
P_{out} = 16 W Avg., V_{D1} + V_{D2} = 28 Vdc, V_{D3A} = V_{D3B} = 45 Vdc, 1 × 20 MHz LTE, input signal PAR = 8 dB @ 0.01% probability on CCDF. [1]

Carrier center frequency	Gain (dB)	ACPR (dBc)	PAE (%)
1815 MHz	47.7	–27.1	43.5
2000 MHz	49.1	–31.8	43.5
2190 MHz	48.3	–33.4	42.7

[1] All data measured with device soldered to NXP reference circuit.

4 Pinning information

4.1 Pinning



Note: Exposed backside of the package is DC and RF ground.

Figure 1. Pin configuration

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4.2 Functional pin description

Table 2. Functional pin description

Pin number	Pin function	Pin description
1	RF_{in}	RF input
2	V_{G2}	Gate voltage, stage 2
3	V_{G1}	Gate voltage, stage 1
4	V_{D2}	Drain voltage, stage 2
5	V_{D1}	Drain voltage, stage 1
6, 7, 8, 10, 12, 13, 14, 15, 17, 18, 20, 22, 23, 24, 25	GND	Ground
9	V_{G3B}	Peaking gate voltage, stage 3
11	V_{D3B}	Peaking drain voltage, stage 3
16	RF_{out}	RF output
19	V_{D3A}	Carrier drain supply, stage 3
21	V_{G3A}	Carrier gate supply, stage 3

5 Functional electrical routing diagram

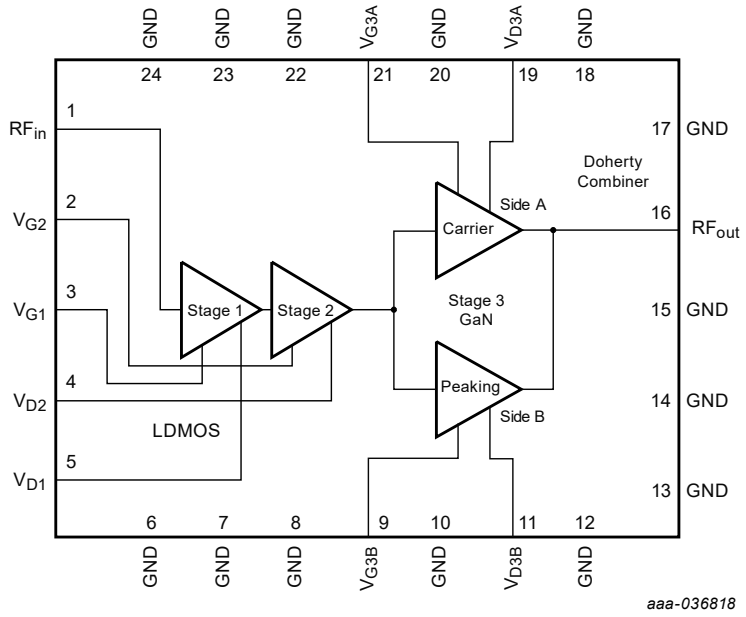

Figure 2. Functional electrical routing diagram

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6 Ordering information

Table 3. Ordering information

Device	Tape and reel information	Package
A5M20TG042T1	T1 suffix = 1,000 units, 32 mm tape width, 13-inch reel	20 mm × 16 mm Module

7 Product marking

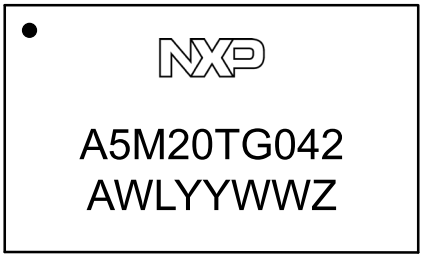

Figure 3. Product marking

Table 4. Product marking trace code

Identifier	Description
A	Assembly location
WL	Wafer lot indicator
YYWW	Date code
Z	Assembly lot

8 Limiting values

Table 5. Limiting values

Rating	Symbol	Value	Unit
Stage 1 and stage 2 gate-bias voltage range	V_{G1}, V_{G2}	–0.5 to +5	Vdc
Stage 1 and stage 2 operating voltage range	V_{D1}, V_{D2}	24 to 32	Vdc
Stage 3 gate-bias voltage range	V_{G3A}, V_{G3B}	–8 to 0	Vdc
Stage 3 operating voltage range	V_{D3A}, V_{D3B}	44 to 52	Vdc
Maximum forward gate current, $I_{G(A+B)}$, @ T_C = 25°C	I_{GMAX}	17.0	mA
Storage temperature range	T_{stg}	–65 to +150	°C
Case operating temperature	T_C	125	°C
Peak input power (2000 MHz, pulsed CW, 10 μsec(on), 10% duty cycle)	P_{in}	11.0	dBm

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9 Lifetime

Table 6. Lifetime

Characteristic	Symbol	Value	Unit
Mean time to failure (Case temperature 125°C, 16 W Avg., V_{D1} + V_{D2} = 28 Vdc, V_{D3A} = V_{D3B} = 45 Vdc)	MTTF	> 10	Years

10 Thermal characteristics

Table 7. Thermal characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance by infrared measurement, active die surface-to-case (Case temperature 115°C, P_D = 22.7 W)	$R_{\theta SC}$ (IR)	1.9[1]	°C/W
Thermal resistance by finite element analysis, channel-to-case (Case temperature 125°C, P_D = 22.7 W)	$R_{\theta CHC}$ (FEA)	3.4[2]	°C/W

[1] Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to https://www.nxp.com/RF and search for AN1955. High conductivity thermal interface used.

[2] $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where T is the channel temperature in degrees Celsius, A = –11.6 and B = 9129.

11 ESD protection characteristics

Table 8. ESD protection characteristics

Test methodology	Class
Human Body Model (per JS-001-2023)	1B
Charge Device Model (per JS-002-2022)	C2a

12 Moisture sensitivity level

Table 9. Moisture sensitivity level

Test methodology	Rating	Package peak temperature	Unit
Per JESD22−A113, IPC/JEDEC J-STD-020	3	250	°C

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13 Electrical characteristics

13.1 DC characteristics — off characteristics

Table 10. DC characteristics — off characteristics

(T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
GaN stage 3 carrier — off characteristics					
Off-state drain leakage (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc)	$I_{D(BR)}$	—	—	4.0	mAdc
Off-state gate leakage (V_{DS} = 48 Vdc, V_{GS} = –8 Vdc)	I_{GLK}	–4.0	—	—	mAdc
GaN stage 3 peaking — off characteristics					
Off-state drain leakage (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc)	$I_{D(BR)}$	—	—	5.5	mAdc
Off-state gate leakage (V_{DS} = 48 Vdc, V_{GS} = –8 Vdc)	I_{GLK}	–5.5	—	—	mAdc

13.2 DC characteristics — on characteristics

Table 11. DC characteristics — on characteristics

(T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Typ	Range	Unit
LDMOS stage 1 — on characteristics				
Gate threshold voltage (V_{DS1} = 10 Vdc, I_{D1} = 2.4 μAdc)	$V_{GS1(th)}$	1.3	±0.4	Vdc
Gate quiescent voltage (V_{DS1} = 28 Vdc, I_{DQ1} = 25 mAdc, measured in production test fixture)	$V_{GS1(Q)}$	2.0	±0.4	Vdc
LDMOS stage 2 — on characteristics				
Gate threshold voltage (V_{GS2} = 10 Vdc, I_{D2} = 12.8 μAdc)	$V_{GS2(th)}$	1.3	±0.4	Vdc
Gate quiescent voltage (V_{DS2} = 28 Vdc, I_{DQ2} = 65 mAdc, measured in production test fixture)	$V_{GS2(Q)}$	1.9	±0.4	Vdc
GaN stage 3 carrier — on characteristics				
Gate threshold voltage (V_{GS3A} = 10 Vdc, I_{D3A} = 10 mAdc)	$V_{GS3A(th)}$	–2.8	±1.0	Vdc
Gate quiescent voltage (V_{DS3A} = 45 Vdc, I_{DQ3A} = 75 mAdc, measured in production test fixture)	$V_{GS3A(Q)}$	–2.6	±1.0	Vdc
GaN stage 3 peaking — on characteristics				
Gate threshold voltage (V_{GS3B} = 10 Vdc, I_{D3B} = 10 mAdc)	$V_{GS3B(th)}$	–2.8	±1.0	Vdc
Gate quiescent voltage (V_{DS3B} = 45 Vdc, I_{DQ3B} = 0 mAdc, measured in production test fixture)	$V_{GS3B(Q)}$	–2.7	±1.0	Vdc

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13.3 Functional tests

Table 12. Functional tests — 1805 MHz

(In NXP production test fixture, T_A = 25°C unless otherwise noted)[1] V_{D1} + V_{D2} = 28 Vdc, V_{D3A} = V_{D3B} = 45 Vdc, I_{DQ1} = 25 mA, I_{DQ2} = 65 mA, I_{DQ3A} = 75 mA, V_{G3B} = (V_{BIAS} – 2.05)[2] Vdc, P_{out} = 16 W Avg., 1-tone CW, f = 1805 MHz.

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G	45.0	48.1	—	dB
Power added efficiency	PAE	34.0	40.9	—	%
Saturated power[3] (Pulsed CW, 5% duty cycle)	P_{sat}	49.0	51.0	—	dBm

[1] Part input and output matched to 50 ohms.
[2] Increase V_{G3B} (peaking side) until I_{DQ3B} = 50 mA current is attained, and then subtract 2.05 V for final V_{G3B} bias voltage.
[3] P_{sat} is defined at P3dB compression point.

Table 13. Functional tests — 2200 MHz

(In NXP production test fixture, T_A = 25°C unless otherwise noted)[1] V_{D1} + V_{D2} = 28 Vdc, V_{D3A} = V_{D3B} = 45 Vdc, I_{DQ1} = 25 mA, I_{DQ2} = 65 mA, I_{DQ3A} = 75 mA, V_{G3B} = (V_{BIAS} – 2.05)[2] Vdc, P_{out} = 16 W Avg., 1-tone CW, f = 2200 MHz.

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G	44.5	48.1	—	dB
Power added efficiency	PAE	34.0	41.6	—	%
Saturated power[3] (Pulsed CW, 5% duty cycle)	P_{sat}	48.0	50.0	—	dBm

[1] Part input and output matched to 50 ohms.
[2] Increase V_{G3B} (peaking side) until I_{DQ3B} = 50 mA current is attained, and then subtract 2.05 V for final V_{G3B} bias voltage.
[3] P_{sat} is defined at P3dB compression point.

13.4 Wideband ruggedness

Table 14. Wideband ruggedness

(In NXP reference circuit, T_A = 25°C unless otherwise noted)[1] I_{DQ1} = 25 mA, I_{DQ2} = 65 mA, I_{DQ3A} = 75 mA, V_{G3B} = (V_{BIAS} – 2.05)[2] Vdc, f = 2000 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR.

Characteristic	Test results
ISBW of 400 MHz at V_{DD3A} = V_{DD3B} = 55 Vdc, 3 dB input overdrive from 16 W Avg. modulated output power	No device degradation

[1] All data measured with device soldered to NXP reference circuit.
[2] Increase V_{G3B} (peaking side) until I_{DQ3B} = 50 mA current is attained, and then subtract 2.05 V for final V_{G3B} bias voltage.

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13.5 Typical performance

Table 15. Typical performance

(In NXP reference circuit, T_A = 25°C unless otherwise noted)[1] V_{D1} + V_{D2} = 28 Vdc, V_{D3A} = V_{D3B} = 45 Vdc, I_{DQ1} = 25 mA, I_{DQ2} = 65 mA, I_{DQ3A} = 75 mA, V_{G3B} = (V_{BIAS} – 2.05)[2] Vdc, P_{out} = 16 W Avg., 1 × 20 MHz LTE, f = 2000 MHz.

Characteristic	Symbol	Min	Typ	Max	Unit
VBW resonance point, 2-tone, 1 MHz tone spacing (IMD third order intermodulation inflection point)	VBW_{res}	—	460	—	MHz
Quiescent current accuracy over temperature[3] with 2.2 kΩ gate feed resistors (–40 to 105°C) Stage 1 with 2.2 kΩ gate feed resistors (–40 to 105°C) Stage 2	ΔI_{QT}	— —	2.4 1.0	— —	%
1-carrier 20 MHz LTE, 8 dB input signal PAR					
Gain	G	—	49.1	—	dB
Power added efficiency	PAE	—	43.5	—	%
Adjacent channel power ratio	ACPR	—	–31.8	—	dBc
Adjacent channel power ratio	ALT1	—	–47.2	—	dBc
Adjacent channel power ratio	ALT2	—	–50.1	—	dBc
Gain flatness[4]	G_F	—	1.7	—	dB
Pulsed CW, 10% duty cycle					
Saturated power[5]	P_{sat}	—	50.9	—	dBm
AM/PM @ saturated power[5]	Φ	—	–15.0	—	°
Gain variation @ Avg. power over temperature (–40°C to +105°C)	ΔG	—	0.038	—	dB/°C
Output power variation @ saturated power over temperature[5] (–40°C to +105°C)	ΔP_{sat}	—	0.005	—	dB/°C

[1] All data measured with device soldered to NXP reference circuit.
[2] Increase V_{G3B} (peaking side) until I_{DQ3B} = 50 mA current is attained, and then subtract 2.05 V for final V_{G3B} bias voltage.
[3] Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to https://www.nxp.com/RF and search for AN1977 or AN1987.
[4] Gain flatness = Max(G(f_{Low} to f_{High})) – Min(G(f_{Low} to f_{High})).
[5] P_{sat} is defined at P3dB compression point.

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Correct biasing sequence

Turn ON:

Bias ON the GaN final stage first (stage 3)

1. Set gate voltage V_{G3A} and V_{G3B} to –8 V.
2. Set drain voltage V_{D3A} and V_{D3B} to nominal supply voltage (+45 V).
3. Increase V_{G3B} (peaking side) until I_{DQ3B} = 50 mA current is attained, and then subtract 2.05 V for final V_{G3B} bias voltage.
4. Increase V_{G3A} (carrier side) until I_{DQ3A} current is attained.

Bias ON the LDMOS drivers second (stages 1 and 2)

5. Set drain voltage V_{D1} and V_{D2} to nominal supply voltage (+28 V), in no particular order.
6. Increase gate voltage V_{G2} until I_{DQ2} current is attained.
7. Increase gate voltage V_{G1} until I_{DQ1} current is attained.
8. Apply RF input power to desired level.

Turn OFF:

Bias OFF the GaN final stage first (stage 3)

1. Disable RF input power.
2. Adjust gate voltage V_{G3A} and V_{G3B} to –8 V.
3. Adjust drain voltage V_{D3A} and V_{D3B} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Disable V_{G3A} and V_{G3B}.

Bias OFF the LDMOS drivers second (stages 1 and 2)

5. Adjust gate voltage V_{G1} and V_{G2} to 0 V.
6. Adjust drain voltage V_{D1} and V_{D2} to 0 V.

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14 Component layout and parts list

14.1 Component layout

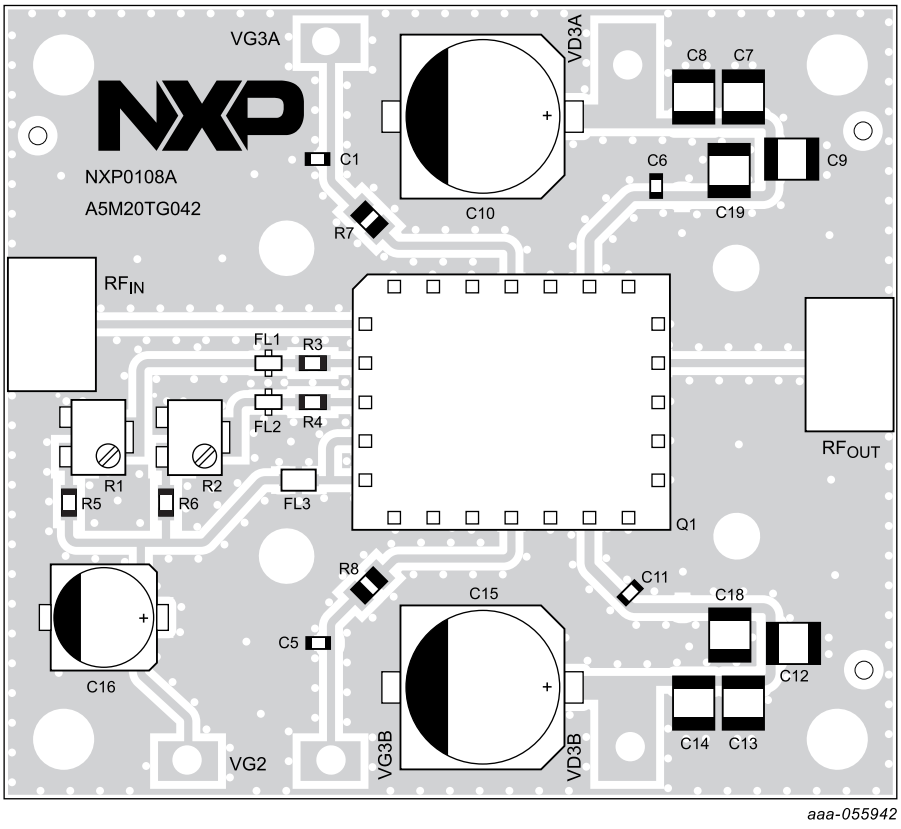

Figure 4. A5M20TG042 reference circuit component layout

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14.2 Component designations and values

Table 16. A5M20TG042 reference circuit component designations and values

Part	Description	Part number	Manufacturer
C1, C5	1 μF chip capacitor	GRT188R61H105KE13D	Murata
C6, C11	15 pF chip capacitor	GQM1875C2E150JB12	Murata
C7, C8, C9, C12, C13, C14, C18, C19	4.7 μF chip capacitor	C3225X7S2A475M200AE	TDK
C10, C15	120 μF, 63 V electrolytic capacitor	EEEFN1J121UV	Panasonic
C16	47 μF, 50 V electrolytic capacitor	EEEFN1H470XP	Panasonic
FL1, FL2	2.2 μF feed through capacitor	NFM18PC225B0J3D	Murata
FL3	22 nF feed through capacitor	NFM21HC223R1H3	Murata
Q1	Power amplifier module	A5M20TG042	NXP
R1, R2	5 kΩ, 1/4 W surface mount potentiometer	3224W-001-502E	Bourns
R3, R4	10 Ω, 1/10 W chip resistor	CRCW060310R0FKEA	Vishay
R5, R6	10 kΩ, 1/10 W chip resistor	RC0603FR-0710KP	Yageo
R7, R8	5.6 Ω, 1/8 W chip resistor	RC0805FR-075R6L	Yageo
PCB	RO4350B, 0.010″, ε_r = 3.66	NXP0108A	Multek

Note: Component numbers C2, C3, C4 and C17 are intentionally omitted.

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15 Package information

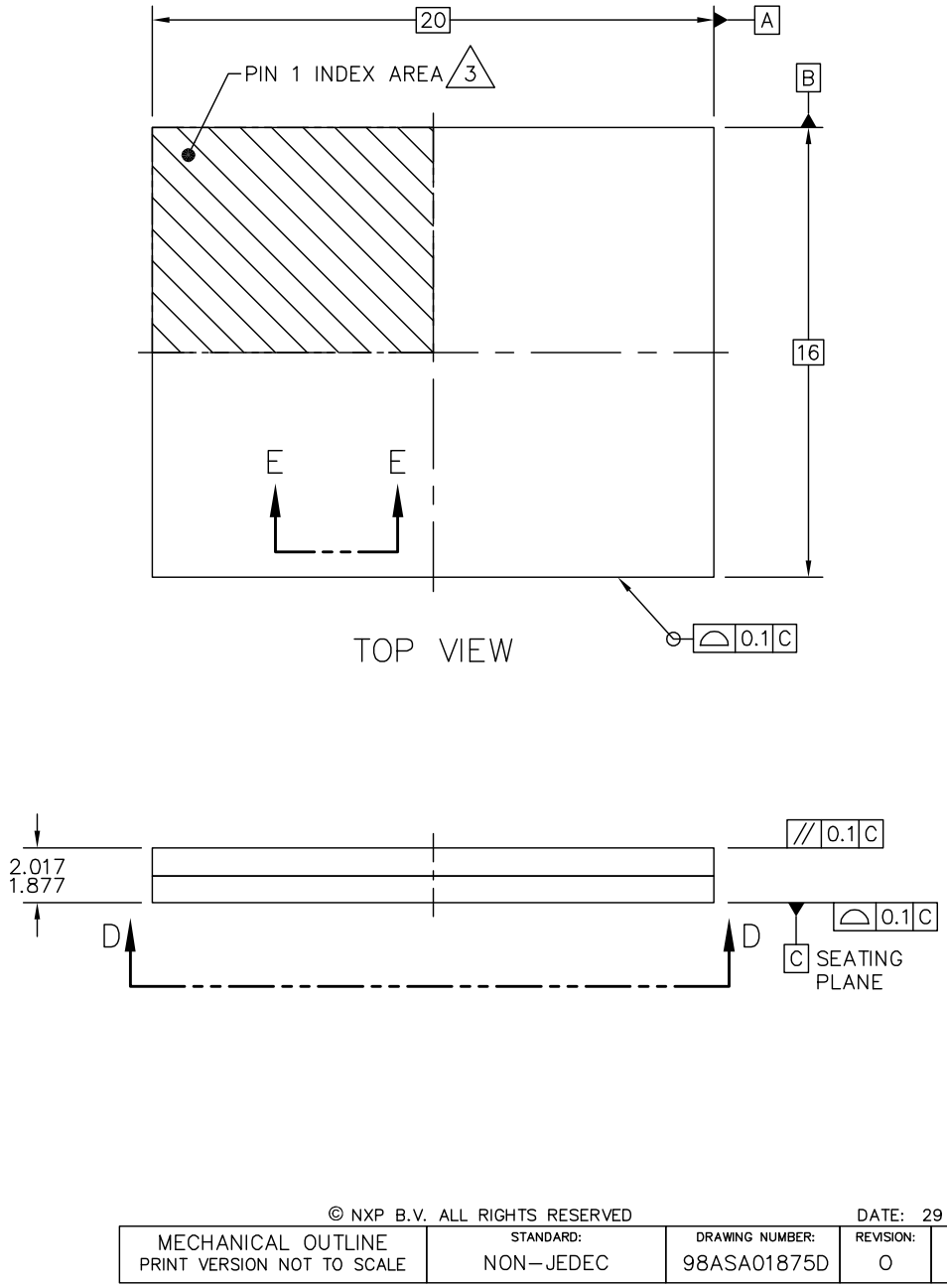

Figure 5. Package outline (20 mm × 16 mm Module) — top view

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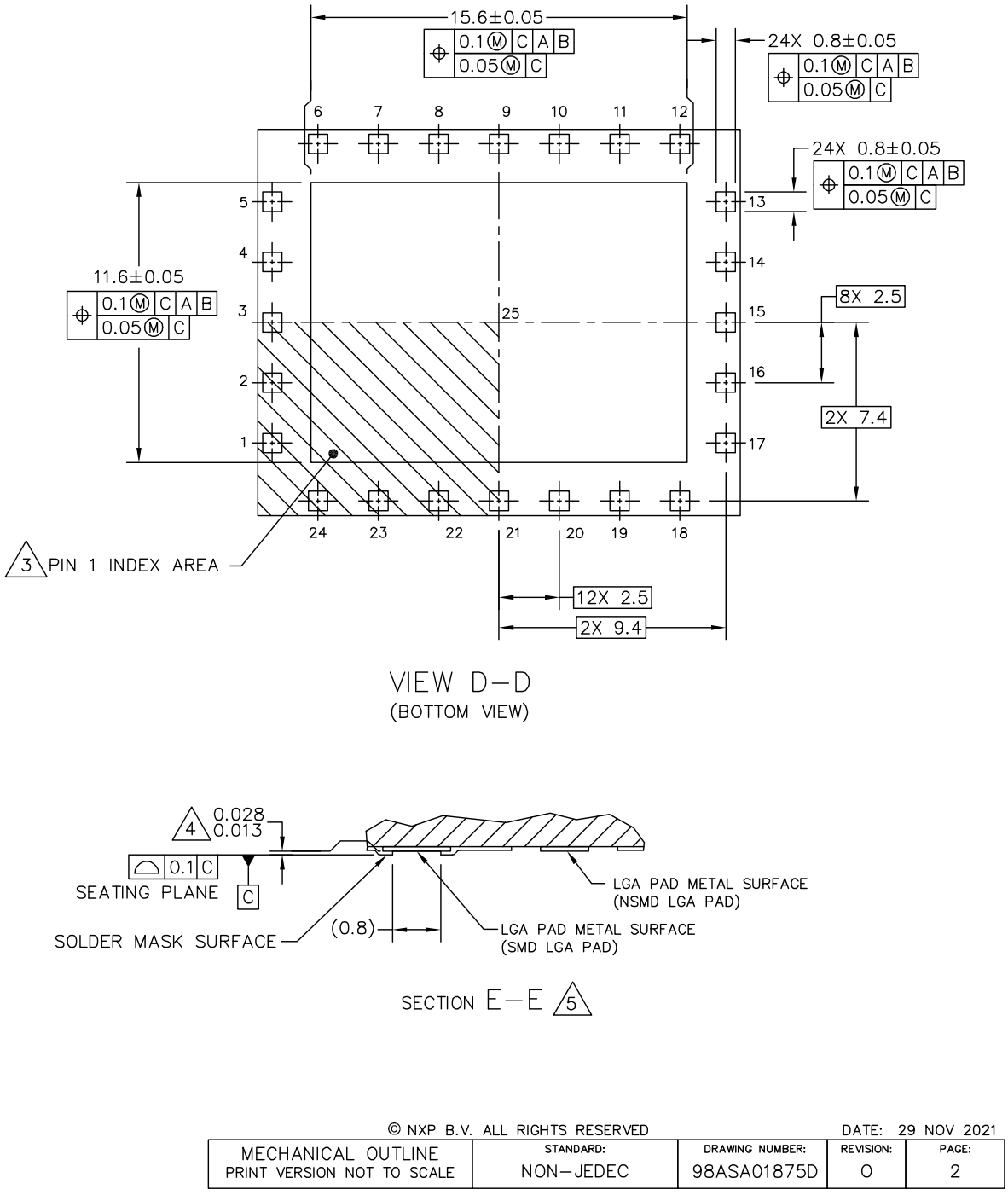

Figure 6. Package outline (20 mm × 16 mm) — bottom view

Note: Vias on the bottom of the package are part of the substrate design and do not impact attachment of the package to the printed circuit board.

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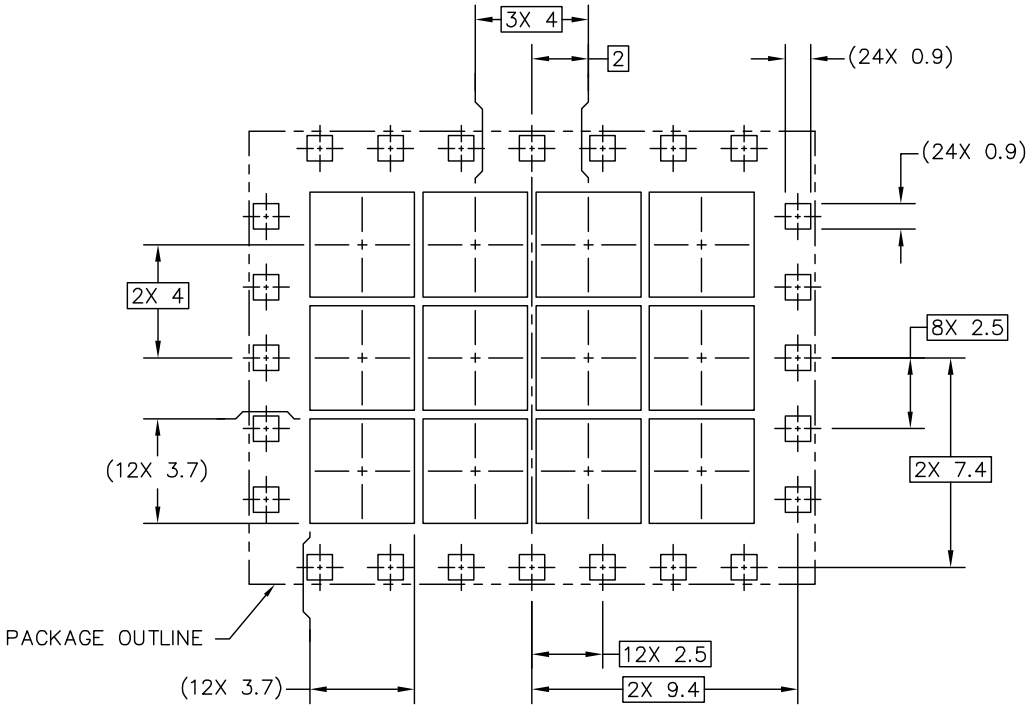
H–PLGA–25 I/O
20 X 16 X 1.947 PKG, 2.5 PITCH

SOT2171–1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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Figure 7. Package outline (20 mm × 16 mm Module) — PCB design guidelines: solder mask opening pattern

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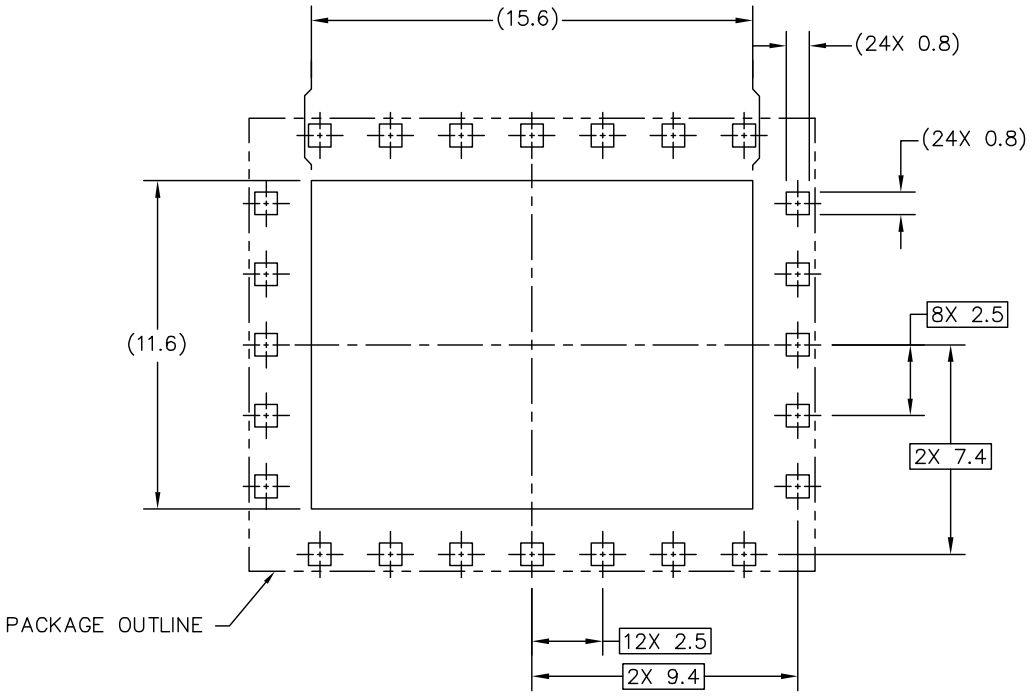
H–PLGA–25 I/O
20 X 16 X 1.947 PKG, 2.5 PITCH

SOT2171–1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREAS

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Figure 8. Package outline (20 mm × 16 mm Module) — PCB design guidelines: I/O pads and solderable areas

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H–PLGA–25 I/O
20 X 16 X 1.947 PKG, 2.5 PITCH

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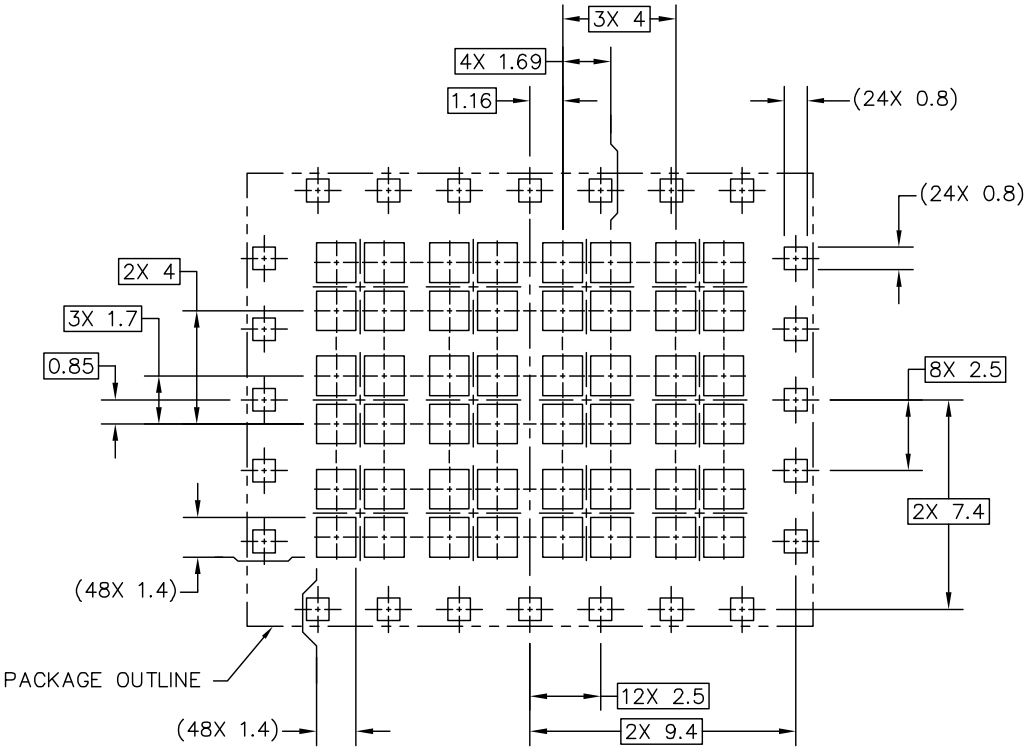

RECOMMENDED STENCIL THICKNESS 0.125 OR 0.15

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 9. Package outline (20 mm × 16 mm Module) — PCB design guidelines: solder paste stencil

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H–PLGA–25 I/O
20 X 16 X 1.947 PKG, 2.5 PITCH

SOT2171–1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. DIMENSION APPLIES TO ALL LEADS.
5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PINS 25) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON–SOLDERMASK DEFINED (NSMD).

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Figure 10. Package outline (20 mm × 16 mm Module) — notes

16 Product documentation and tools

Refer to the following resources to aid your design process.

Application notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Development tools

- Printed circuit boards

17 Failure analysis

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

18 Revision history

The following table summarizes revisions to this document.

Table 17. Revision history

Document ID	Release date	Description
A5M20TG042 Rev. 1	20 May 2024	• Initial release of product data sheet

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Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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Contents

1	**General description**	**1**
2	**Features and benefits**	**1**
3	**Typical performance**	**1**
4	**Pinning information**	**2**
4.1	Pinning	2
4.2	Functional pin description	3
5	**Functional electrical routing diagram**	**3**
6	**Ordering information**	**4**
7	**Product marking**	**4**
8	**Limiting values**	**4**
9	**Lifetime**	**5**
10	**Thermal characteristics**	**5**
11	**ESD protection characteristics**	**5**
12	**Moisture sensitivity level**	**5**
13	**Electrical characteristics**	**6**
13.1	DC characteristics — off characteristics	6
13.2	DC characteristics — on characteristics	6
13.3	Functional tests	7
13.4	Wideband ruggedness	7
13.5	Typical performance	8
14	**Component layout and parts list**	**10**
14.1	Component layout	10
14.2	Component designations and values	11
15	**Package information**	**12**
16	**Product documentation and tools**	**18**
17	**Failure analysis**	**18**
18	**Revision history**	**18**
	Legal information	**19**

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Date of release: 20 May 2024
Document identifier: A5M20TG042

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