

# Zynq UltraScale+ Device Packaging and Pinouts

## *Product Specification User Guide*

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# Packaging Overview

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## Introduction to the UltraScale Architecture

The AMD UltraScale™ architecture is the first ASIC-class architecture to enable multi-hundred gigabit-per-second levels of system performance with smart processing, while efficiently routing and processing data on-chip. UltraScale architecture-based devices address a vast spectrum of high-bandwidth, high-utilization system requirements by using industry-leading technical innovations, including next-generation routing, ASIC-like clocking, 3D-on-3D ICs, multiprocessor SoC (MPSoC) technologies, and new power reduction features. The devices share many building blocks, providing scalability across process nodes and product families to leverage system-level investment across platforms.

Artix™ UltraScale+™ devices provide high serial bandwidth and signal compute density in a cost-optimized device for critical networking applications, vision and video processing, and secured connectivity. Coupled with the innovative InFO packaging, which provides excellent thermal and power distribution, Artix UltraScale+ FPGAs are perfectly suited to applications requiring high compute density in a small footprint.

Virtex™ UltraScale+ devices provide the highest performance and integration capabilities in a FinFET node, including both the highest serial I/O and signal processing bandwidth, as well as the highest on-chip memory density. As the industry's most capable FPGA family, the Virtex UltraScale+ devices are ideal for applications including 1+Tb/s networking and data center and fully integrated radar/early-warning systems.

Kintex™ UltraScale+ devices provide the best price/performance/watt balance in a FinFET node, delivering the most cost-effective solution for high-end capabilities, including transceiver and memory interface line rates as well as 100G connectivity cores. Our newest mid-range family is ideal for both packet processing and DSP-intensive functions and is well suited for applications including wireless MIMO technology, Nx100G networking, and data center.

Zynq™ UltraScale+ MPSoC devices provide 64-bit processor scalability while combining real-time control with soft and hard engines for graphics, video, waveform, and packet processing. Integrating an Arm®-based system for advanced analytics and on-chip programmable logic for task acceleration creates unlimited possibilities for applications including 5G Wireless, next generation ADAS, and Industrial Internet-of-Things.

Zynq UltraScale+ RFSoc integrate the key subsystems required to implement a complete software-defined radio including direct RF sampling data converters, enabling CPRI and

gigabit Ethernet-to-RF on a single, highly programmable SoC. Each device offers multiple RF-sampling analog-to-digital (RF-ADC) and RF-sampling digital-to-analog (RF-DAC) data converters. The data converters are high-precision, high-speed and power efficient.

For the latest Zynq UltraScale+ device descriptions, specifications, data sheets, and user guides are available at [docs.amd.com](https://docs.amd.com).

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## Zynq UltraScale+ Device Packaging and Pinouts

This section describes the packages and pinouts for the in various organic flip-chip 0.5 mm, 0.8 mm, and 1.0 mm pitch BGA packages.



**IMPORTANT:** All standard packages are lead-free (signified by an additional V in the package name). All devices supported in a particular package are footprint compatible. Each device is split into I/O banks to allow for flexibility in the choice of I/O standards. See the *UltraScale Architecture SelectIO Resources User Guide (UG571)*.

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The flip-chip assembly materials for the Zynq UltraScale+ devices are manufactured using ultra-low alpha (ULA) materials defined as  $<0.002$  cph/cm<sup>2</sup> or materials that emit less than 0.002 alpha-particles per square centimeter per hour.



**IMPORTANT:** All non-InFO packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC or XA, and the Pb-free signifier in the package name is Q.

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## Differences from Previous Generations

The packaging and pinout specifications for Zynq UltraScale+ devices differ from past generations, including the Zynq-7000 SoCs. These details are outlined in this section.

- All package and die components, including flip-chip solder bumps, are lead-free.
- Package names contain a single-character alphabetic designator followed by the exact number of pins found on the package.
- VCCAUX\_IO pins are not divided into bank groups. VCCAUX\_IO must be connected to VCCAUX at the board level.
- Internal logic is separated from I/O logic by the addition of the VCCINT\_IO power pins. VCCINT\_IO must be connected to VCCBRAM (depending on the device speed grade and voltage settings) at the board level.
- Groups of gigabit serial transceiver (GT) power pins are separated by column for each column of GT Quads.

- Standard HP I/O banks each have a total of 52 SelectIO™ pins, optionally configurable as (up to) 24 differential pairs.
- Standard HD I/O banks each have a total of 24 SelectIO pins, optionally configurable as (up to) 12 differential pairs.
- Each bank has one dedicated VREF pin. These pins cannot be used as user I/Os.
- Four differential clock pin pairs per bank consist of a single type of global clock (GC or HDGC) input.
- Four memory byte groups per HP I/O bank are each separated into an upper and a lower memory byte group.
- Multiple PL configuration pins are removed.
- A POR\_OVERRIDE pin is used to override the default power-on-reset delay. See [Table 1-4](#).

## Device/Package Combinations

[Table 1-1](#) shows the size and BGA pitch of the Zynq UltraScale+ device packages. All non-InFO packages are available with eutectic BGA balls. For these packages, the Pb-free signifier in the package name is a Q.

**Table 1-1: Package Specifications**

| Packages | Description                                    | Package Specifications |            |           |
|----------|------------------------------------------------|------------------------|------------|-----------|
|          |                                                | Package Type           | Pitch (mm) | Size (mm) |
| UBVA494  | Flip-chip, integrated fan out (InFO), bare-die | BGA                    | 0.5        | 15 x 9.5  |
| UBVA530  | Flip-chip, integrated fan out (InFO), bare-die |                        |            | 16 x 9.5  |
| SBVA484  | Flip-chip, super-fine-pitch, bare-die          |                        | 0.8        | 19 x 19   |
| SFRA484  | Ruggedized flip-chip, super-fine-pitch         |                        |            | 19 x 19   |
| SBVA625  | Flip-chip, super-fine-pitch, bare-die          |                        |            | 21 x 21   |
| SFVA625  | Flip-chip, super-fine-pitch                    |                        |            |           |
| SFVC784  | Flip-chip, super-fine-pitch                    |                        |            | 23 x 23   |
| SFRC784  | Ruggedized flip-chip, super-fine-pitch         |                        |            |           |
| SFVD784  | Flip-chip, super-fine-pitch                    |                        |            |           |
| SFVE784  | Flip-chip, super-fine-pitch                    |                        |            |           |
| FBVB900  | Flip-chip, fine-pitch, bare-die                |                        | 1.0        | 31 x 31   |
| FFRB900  | Ruggedized flip-chip, fine-pitch               |                        |            |           |
| FFVC900  | Flip-chip, fine-pitch                          |                        |            |           |
| FFRC900  | Ruggedized flip-chip, fine-pitch               |                        |            |           |

Table 1-1: Package Specifications (Cont'd)

| Packages | Description                                                   | Package Specifications |            |             |
|----------|---------------------------------------------------------------|------------------------|------------|-------------|
|          |                                                               | Package Type           | Pitch (mm) | Size (mm)   |
| FFVB1156 | Flip-chip, fine-pitch                                         | BGA                    | 1.0        | 35 x 35     |
| FFRB1156 | Ruggedized flip-chip, fine-pitch                              |                        |            |             |
| FFVC1156 | Flip-chip, fine-pitch                                         |                        |            |             |
| FFRC1156 | Ruggedized flip-chip, fine-pitch                              |                        |            |             |
| FFVD1156 | Flip-chip, fine-pitch                                         |                        |            |             |
| FFRD1156 | Ruggedized flip-chip, fine-pitch                              |                        |            |             |
| FFVE1156 | Flip-chip, fine-pitch                                         |                        |            | 40 x 40     |
| FFRE1156 | Ruggedized flip-chip, fine-pitch                              |                        |            |             |
| FFVB1517 | Flip-chip, fine-pitch                                         |                        |            |             |
| FFRB1517 | Ruggedized flip-chip, fine-pitch                              |                        |            |             |
| FFVF1517 | Flip-chip, fine-pitch                                         |                        |            |             |
| FFVG1517 | Flip-chip, fine-pitch                                         |                        |            | 42.5 x 42.5 |
| FFRG1517 | Ruggedized flip-chip, fine-pitch                              |                        |            |             |
| FFVC1760 | Flip-chip, fine-pitch                                         |                        |            |             |
| FFRC1760 | Ruggedized flip-chip, fine-pitch                              |                        |            |             |
| FFVD1760 | Flip-chip, fine-pitch                                         |                        |            |             |
| FFVF1760 | Flip-chip, fine-pitch                                         |                        |            |             |
| FFVH1760 | Flip-chip, fine-pitch                                         |                        |            |             |
| FFRF1760 | Ruggedized flip-chip, fine-pitch                              |                        |            | 45 x 45     |
| FFVE1924 | Flip-chip, fine-pitch                                         |                        |            |             |
| FSVE1156 | Flip-chip, fine-pitch, lidless with stiffener ring            |                        |            | 35 x 35     |
| FSVG1517 |                                                               |                        |            | 40 x 40     |
| FSVF1760 |                                                               |                        |            | 42.5 x 42.5 |
| FSVH1760 |                                                               |                        |            | 40 x 40     |
| FSRG1517 | Ruggedized flip-chip, fine-pitch, lidless with stiffener ring |                        |            |             |
| FSRF1760 |                                                               |                        |            | 42.5 x 42.5 |

# Gigabit Transceiver Channels by Device/Package

Table 1-2 lists the quantity of gigabit transceiver channels for the Zynq UltraScale+ devices. In all devices, a PS-GTR, GTH, or GTY channel is one set of MGTRXP, MGTRXN, MGTTXP, and MGTTXN pins. All non-InFO packages are available with eutectic BGA balls. For these packages, the device type is XQ and the Pb-free signifier in the package name is a Q.

**Table 1-2: Serial Transceiver Channels (PS-GTR, GTH, and GTY) by Device/Package**

| Device  | Package | PS-GTR Channels | GTH Channels | GTY Channels |
|---------|---------|-----------------|--------------|--------------|
| XCZU1CG | SBVA484 | 4               | 0            | 0            |
| XCZU1EG |         | 4               | 0            | 0            |
| XCZU2CG |         | 4               | 0            | 0            |
| XCZU2EG |         | 4               | 0            | 0            |
| XCZU3CG |         | 4               | 0            | 0            |
| XCZU3EG |         | 4               | 0            | 0            |
| XAZU1EG |         | 4               | 0            | 0            |
| XAZU2EG |         | 4               | 0            | 0            |
| XAZU3EG |         | 4               | 0            | 0            |
| XQZU3EG | SFRA484 | 4               | 0            | 0            |
| XCZU1CG | UBVA494 | 4               | 0            | 0            |
| XCZU1EG |         | 4               | 0            | 0            |
| XCZU2CG | UBVA530 | 4               | 0            | 0            |
| XCZU2EG |         | 4               | 0            | 0            |
| XCZU3CG |         | 4               | 0            | 0            |
| XCZU3EG |         | 4               | 0            | 0            |
| XCZU1CG | SFVA625 | 4               | 0            | 0            |
| XCZU1EG |         | 4               | 0            | 0            |
| XCZU2CG |         | 4               | 0            | 0            |
| XCZU2EG |         | 4               | 0            | 0            |
| XCZU3CG |         | 4               | 0            | 0            |
| XCZU3EG |         | 4               | 0            | 0            |
| XAZU1EG |         | 4               | 0            | 0            |
| XAZU2EG |         | 4               | 0            | 0            |
| XAZU3EG |         | 4               | 0            | 0            |

Table 1-2: Serial Transceiver Channels (PS-GTR, GTH, and GTY) by Device/Package (Cont'd)

| Device   | Package | PS-GTR Channels | GTH Channels | GTY Channels |
|----------|---------|-----------------|--------------|--------------|
| XCZU1CG  | SFVC784 | 4               | 0            | 0            |
| XCZU1EG  |         | 4               | 0            | 0            |
| XCZU2CG  |         | 4               | 0            | 0            |
| XCZU2EG  |         | 4               | 0            | 0            |
| XCZU3CG  |         | 4               | 0            | 0            |
| XCZU3EG  |         | 4               | 0            | 0            |
| XCZU3TCG |         | 4               | 4            | 0            |
| XCZU3TEG |         | 4               | 4            | 0            |
| XCZU4CG  |         | 4               | 4            | 0            |
| XCZU4EG  |         | 4               | 4            | 0            |
| XCZU4EV  |         | 4               | 4            | 0            |
| XCZU5CG  |         | 4               | 4            | 0            |
| XCZU5EG  |         | 4               | 4            | 0            |
| XCZU5EV  |         | 4               | 4            | 0            |
| XAZU1EG  |         | 4               | 0            | 0            |
| XAZU2EG  |         | 4               | 0            | 0            |
| XAZU3EG  |         | 4               | 0            | 0            |
| XAZU4EV  |         | 4               | 4            | 0            |
| XAZU5EV  |         | 4               | 4            | 0            |
| XQZU21DR | SFRC784 | 4               | 0            | 0            |
| XQZU5EV  |         | 4               | 4            | 0            |
| XCZU3TCG | SFVD784 | 4               | 8            | 0            |
| XCZU3TEG |         | 4               | 8            | 0            |
| XCZU4CG  | SFVE784 | 4               | 8            | 0            |
| XCZU4EG  |         | 4               | 8            | 0            |
| XCZU4EV  |         | 4               | 8            | 0            |
| XCZU5CG  |         | 4               | 8            | 0            |
| XCZU5EG  |         | 4               | 8            | 0            |
| XCZU5EV  |         | 4               | 8            | 0            |



Table 1-2: Serial Transceiver Channels (PS-GTR, GTH, and GTY) by Device/Package (Cont'd)

| Device   | Package  | PS-GTR Channels | GTH Channels | GTY Channels |
|----------|----------|-----------------|--------------|--------------|
| XCZU4CG  | FBVB900  | 4               | 16           | 0            |
| XCZU4EG  |          | 4               | 16           | 0            |
| XCZU4EV  |          | 4               | 16           | 0            |
| XCZU5CG  |          | 4               | 16           | 0            |
| XCZU5EG  |          | 4               | 16           | 0            |
| XCZU5EV  |          | 4               | 16           | 0            |
| XCZU7CG  |          | 4               | 16           | 0            |
| XCZU7EG  |          | 4               | 16           | 0            |
| XCZU7EV  |          | 4               | 16           | 0            |
| XAZU7EV  |          | 4               | 16           | 0            |
| XQZU5EV  | FFRB900  | 4               | 16           | 0            |
| XQZU7EV  |          | 4               | 16           | 0            |
| XCZU6CG  | FFVC900  | 4               | 16           | 0            |
| XCZU6EG  |          | 4               | 16           | 0            |
| XCZU9CG  |          | 4               | 16           | 0            |
| XCZU9EG  |          | 4               | 16           | 0            |
| XCZU15EG |          | 4               | 16           | 0            |
| XQZU9EG  | FFRC900  | 4               | 16           | 0            |
| XQZU15EG |          | 4               | 16           | 0            |
| XCZU6CG  | FFVB1156 | 4               | 24           | 0            |
| XCZU6EG  |          | 4               | 24           | 0            |
| XCZU9CG  |          | 4               | 24           | 0            |
| XCZU9EG  |          | 4               | 24           | 0            |
| XCZU15EG |          | 4               | 24           | 0            |
| XQZU9EG  | FFRB1156 | 4               | 24           | 0            |
| XQZU15EG |          | 4               | 24           | 0            |
| XCZU7CG  | FFVC1156 | 4               | 20           | 0            |
| XCZU7EG  |          | 4               | 20           | 0            |
| XCZU7EV  |          | 4               | 20           | 0            |
| XCZU11EG |          | 4               | 20           | 0            |
| XQZU7EV  | FFRC1156 | 4               | 20           | 0            |
| XQZU11EG |          | 4               | 20           | 0            |
| XCZU21DR | FFVD1156 | 4               | 0            | 16           |
| XQZU21DR | FFRD1156 | 4               | 0            | 16           |

Table 1-2: Serial Transceiver Channels (PS-GTR, GTH, and GTY) by Device/Package (Cont'd)

| Device   | Package  | PS-GTR Channels | GTH Channels | GTY Channels |
|----------|----------|-----------------|--------------|--------------|
| XCZU25DR | FFVE1156 | 4               | 0            | 8            |
| XCZU27DR |          | 4               | 0            | 8            |
| XCZU28DR |          | 4               | 0            | 8            |
| XCZU42DR |          | 4               | 0            | 8            |
| XCZU43DR |          | 4               | 0            | 8            |
| XCZU47DR |          | 4               | 0            | 8            |
| XCZU48DR |          | 4               | 0            | 8            |
| XCZU63DR |          | 4               | 0            | 8            |
| XCZU64DR |          | 4               | 0            | 8            |
| XCZU65DR |          | 4               | 0            | 8            |
| XCZU67DR |          | 4               | 0            | 8            |
| XQZU28DR | FFRE1156 | 4               | 0            | 8            |
| XQZU48DR |          | 4               | 0            | 8            |
| XCZU25DR | FSVE1156 | 4               | 0            | 8            |
| XCZU27DR |          | 4               | 0            | 8            |
| XCZU28DR |          | 4               | 0            | 8            |
| XCZU42DR |          | 4               | 0            | 8            |
| XCZU43DR |          | 4               | 0            | 8            |
| XCZU47DR |          | 4               | 0            | 8            |
| XCZU48DR |          | 4               | 0            | 8            |
| XCZU63DR |          | 4               | 0            | 4            |
| XCZU64DR |          | 4               | 0            | 8            |
| XCZU65DR |          | 4               | 0            | 8            |
| XCZU67DR |          | 4               | 0            | 8            |
| XCZU11EG | FFVB1517 | 4               | 16           | 0            |
| XCZU17EG |          | 4               | 16           | 0            |
| XCZU19EG |          | 4               | 16           | 0            |
| XQZU19EG | FFRB1517 | 4               | 16           | 0            |
| XCZU7CG  | FFVF1517 | 4               | 24           | 0            |
| XCZU7EG  |          | 4               | 24           | 0            |
| XCZU7EV  |          | 4               | 24           | 0            |
| XCZU11EG |          | 4               | 32           | 0            |
| XAZU11EG |          | 4               | 32           | 0            |

Table 1-2: Serial Transceiver Channels (PS-GTR, GTH, and GTY) by Device/Package (Cont'd)

| Device   | Package  | PS-GTR Channels | GTH Channels | GTY Channels |
|----------|----------|-----------------|--------------|--------------|
| XCZU25DR | FFVG1517 | 4               | 0            | 8            |
| XCZU27DR |          | 4               | 0            | 16           |
| XCZU28DR |          | 4               | 0            | 16           |
| XCZU43DR |          | 4               | 0            | 16           |
| XCZU47DR |          | 4               | 0            | 16           |
| XCZU48DR |          | 4               | 0            | 16           |
| XQZU28DR | FFRG1517 | 4               | 0            | 16           |
| XCZU25DR | FSVG1517 | 4               | 0            | 8            |
| XCZU27DR |          | 4               | 0            | 16           |
| XCZU28DR |          | 4               | 0            | 16           |
| XCZU43DR |          | 4               | 0            | 16           |
| XCZU47DR |          | 4               | 0            | 16           |
| XCZU48DR |          | 4               | 0            | 16           |
| XQZU48DR | FSRG1517 | 4               | 0            | 16           |
| XCZU11EG | FFVC1760 | 4               | 32           | 16           |
| XCZU17EG |          | 4               | 32           | 16           |
| XCZU19EG |          | 4               | 32           | 16           |
| XQZU11EG | FFRC1760 | 4               | 32           | 16           |
| XQZU19EG |          | 4               | 32           | 16           |
| XCZU17EG | FFVD1760 | 4               | 44           | 28           |
| XCZU19EG |          | 4               | 44           | 28           |
| XCZU29DR | FFVF1760 | 4               | 0            | 16           |
| XCZU39DR |          | 4               | 0            | 16           |
| XCZU49DR |          | 4               | 0            | 16           |
| XCZU46DR | FFVH1760 | 4               | 0            | 16           |
| XQZU29DR | FFRF1760 | 4               | 0            | 16           |
| XCZU29DR | FSVF1760 | 4               | 0            | 16           |
| XCZU39DR |          | 4               | 0            | 16           |
| XCZU49DR |          | 4               | 0            | 16           |
| XQZU49DR | FSRF1760 | 4               | 0            | 16           |
| XCZU46DR | FSVH1760 | 4               | 0            | 16           |
| XCZU17EG | FFVE1924 | 4               | 44           | 0            |
| XCZU19EG |          | 4               | 44           | 0            |

## User I/O Pins by Device/Package

Table 1-3 lists the number of available PS I/Os, 3.3V-capable high-density (HD), and 1.8V-capable high-performance (HP) I/Os and the number of HD or HP differential I/O for each device/package combination. All non-InFO packages are available with eutectic BGA balls. For these packages, the device type is XQ and the Pb-free signifier in the package name is a Q.

Table 1-3: Available I/O Pins by Device/Package

| Device  | Package | PS I/Os | Total User I/O    |                   | Differential I/O |     |
|---------|---------|---------|-------------------|-------------------|------------------|-----|
|         |         |         | HD <sup>(1)</sup> | HP <sup>(1)</sup> | HD               | HP  |
| XCZU1CG | SBVA484 | 170     | 24                | 58                | 24               | 52  |
| XCZU1EG |         | 170     | 24                | 58                | 24               | 52  |
| XCZU2CG |         | 170     | 24                | 58                | 24               | 52  |
| XCZU2EG |         | 170     | 24                | 58                | 24               | 52  |
| XCZU3CG |         | 170     | 24                | 58                | 24               | 52  |
| XCZU3EG |         | 170     | 24                | 58                | 24               | 52  |
| XAZU1EG |         | 170     | 24                | 58                | 24               | 52  |
| XAZU2EG |         | 170     | 24                | 58                | 24               | 52  |
| XAZU3EG |         | 170     | 24                | 58                | 24               | 52  |
| XQZU3EG | SFRA484 | 170     | 24                | 58                | 24               | 52  |
| XCZU1CG | UBVA494 | 170     | 24                | 58                | 24               | 52  |
| XCZU1EG |         | 170     | 24                | 58                | 24               | 52  |
| XCZU2CG | UBVA530 | 170     | 24                | 58                | 24               | 52  |
| XCZU2EG |         | 170     | 24                | 58                | 24               | 52  |
| XCZU3CG |         | 170     | 24                | 58                | 24               | 52  |
| XCZU3EG |         | 170     | 24                | 58                | 24               | 52  |
| XCZU1CG | SFVA625 | 170     | 24                | 156               | 24               | 144 |
| XCZU1EG |         | 170     | 24                | 156               | 24               | 144 |
| XCZU2CG |         | 170     | 24                | 156               | 24               | 144 |
| XCZU2EG |         | 170     | 24                | 156               | 24               | 144 |
| XCZU3CG |         | 170     | 24                | 156               | 24               | 144 |
| XCZU3EG |         | 170     | 24                | 156               | 24               | 144 |
| XAZU1EG |         | 170     | 24                | 156               | 24               | 144 |
| XAZU2EG |         | 170     | 24                | 156               | 24               | 144 |
| XAZU3EG |         | 170     | 24                | 156               | 24               | 144 |

Table 1-3: Available I/O Pins by Device/Package (Cont'd)

| Device   | Package | PS I/Os | Total User I/O    |                   | Differential I/O |     |
|----------|---------|---------|-------------------|-------------------|------------------|-----|
|          |         |         | HD <sup>(1)</sup> | HP <sup>(1)</sup> | HD               | HP  |
| XCZU1CG  | SFVC784 | 214     | 24                | 156               | 24               | 144 |
| XCZU1EG  |         | 214     | 24                | 156               | 24               | 144 |
| XCZU2CG  |         | 214     | 96                | 156               | 96               | 144 |
| XCZU2EG  |         | 214     | 96                | 156               | 96               | 144 |
| XCZU3CG  |         | 214     | 96                | 156               | 96               | 144 |
| XCZU3EG  |         | 214     | 96                | 156               | 96               | 144 |
| XCZU3TCG |         | 214     | 72                | 52                | 72               | 48  |
| XCZU3TEG |         | 214     | 72                | 52                | 72               | 48  |
| XCZU4CG  |         | 214     | 96                | 156               | 96               | 144 |
| XCZU4EG  |         | 214     | 96                | 156               | 96               | 144 |
| XCZU4EV  |         | 214     | 96                | 156               | 96               | 144 |
| XCZU5CG  |         | 214     | 96                | 156               | 96               | 144 |
| XCZU5EG  |         | 214     | 96                | 156               | 96               | 144 |
| XCZU5EV  |         | 214     | 96                | 156               | 96               | 144 |
| XAZU1EG  |         | 170     | 24                | 156               | 24               | 144 |
| XAZU2EG  |         | 214     | 96                | 156               | 96               | 144 |
| XAZU3EG  |         | 214     | 96                | 156               | 96               | 144 |
| XAZU4EV  |         | 214     | 96                | 156               | 96               | 144 |
| XAZU5EV  |         | 214     | 96                | 156               | 96               | 144 |
| XQZU3EG  | SFRC784 | 214     | 96                | 156               | 96               | 144 |
| XQZU5EV  |         | 214     | 96                | 156               | 96               | 114 |
| XCZU3TCG | SFVD784 | 214     | 72                | 52                | 72               | 48  |
| XCZU3TEG |         | 214     | 72                | 52                | 72               | 48  |
| XCZU4CG  | SFVE784 | 214     | 72                | 58                | 72               | 52  |
| XCZU4EG  |         | 214     | 72                | 58                | 72               | 52  |
| XCZU4EV  |         | 214     | 72                | 58                | 72               | 52  |
| XCZU5CG  |         | 214     | 72                | 58                | 72               | 52  |
| XCZU5EG  |         | 214     | 72                | 58                | 72               | 52  |
| XCZU5EV  |         | 214     | 72                | 58                | 72               | 52  |

Table 1-3: Available I/O Pins by Device/Package (Cont'd)

| Device   | Package  | PS I/Os | Total User I/O    |                   | Differential I/O |     |
|----------|----------|---------|-------------------|-------------------|------------------|-----|
|          |          |         | HD <sup>(1)</sup> | HP <sup>(1)</sup> | HD               | HP  |
| XCZU4CG  | FBVB900  | 214     | 48                | 156               | 48               | 144 |
| XCZU4EG  |          | 214     | 48                | 156               | 48               | 144 |
| XCZU4EV  |          | 214     | 48                | 156               | 48               | 144 |
| XCZU5CG  |          | 214     | 48                | 156               | 48               | 144 |
| XCZU5EG  |          | 214     | 48                | 156               | 48               | 144 |
| XCZU5EV  |          | 214     | 48                | 156               | 48               | 144 |
| XCZU7CG  |          | 214     | 48                | 156               | 48               | 144 |
| XCZU7EG  |          | 214     | 48                | 156               | 48               | 144 |
| XCZU7EV  |          | 214     | 48                | 156               | 48               | 144 |
| XAZU7EV  |          | 214     | 48                | 156               | 48               | 144 |
| XQZU5EV  | FFRB900  | 214     | 48                | 156               | 48               | 144 |
| XQZU7EV  |          | 214     | 48                | 156               | 48               | 144 |
| XCZU6CG  | FFVC900  | 214     | 48                | 156               | 48               | 144 |
| XCZU6EG  |          | 214     | 48                | 156               | 48               | 144 |
| XCZU9CG  |          | 214     | 48                | 156               | 48               | 144 |
| XCZU9EG  |          | 214     | 48                | 156               | 48               | 144 |
| XCZU15EG |          | 214     | 48                | 156               | 48               | 144 |
| XQZU9EG  | FFRC900  | 214     | 48                | 156               | 48               | 144 |
| XQZU15EG |          | 214     | 48                | 156               | 48               | 144 |
| XCZU6CG  | FFVB1156 | 214     | 120               | 208               | 120              | 192 |
| XCZU6EG  |          | 214     | 120               | 208               | 120              | 192 |
| XCZU9CG  |          | 214     | 120               | 208               | 120              | 192 |
| XCZU9EG  |          | 214     | 120               | 208               | 120              | 192 |
| XCZU15EG |          | 214     | 120               | 208               | 120              | 192 |
| XQZU9EG  | FFRB1156 | 214     | 120               | 208               | 120              | 192 |
| XQZU15EG |          | 214     | 120               | 208               | 120              | 192 |
| XCZU7CG  | FFVC1156 | 214     | 48                | 312               | 48               | 288 |
| XCZU7EG  |          | 214     | 48                | 312               | 48               | 288 |
| XCZU7EV  |          | 214     | 48                | 312               | 48               | 288 |
| XCZU11EG |          | 214     | 48                | 312               | 48               | 288 |
| XQZU7EV  | FFRC1156 | 214     | 48                | 312               | 48               | 288 |
| XQZU11EG |          | 214     | 48                | 312               | 48               | 288 |
| XCZU21DR | FFVD1156 | 214     | 72                | 208               | 72               | 192 |
| XQZU21DR | FFRD1156 | 214     | 72                | 208               | 72               | 192 |

Table 1-3: Available I/O Pins by Device/Package (Cont'd)

| Device   | Package  | PS I/Os | Total User I/O    |                   | Differential I/O |     |
|----------|----------|---------|-------------------|-------------------|------------------|-----|
|          |          |         | HD <sup>(1)</sup> | HP <sup>(1)</sup> | HD               | HP  |
| XCZU25DR | FFVE1156 | 214     | 48                | 104               | 48               | 96  |
| XCZU27DR |          | 214     | 48                | 104               | 48               | 96  |
| XCZU28DR |          | 214     | 48                | 104               | 48               | 96  |
| XCZU42DR |          | 214     | 24                | 130               | 24               | 120 |
| XCZU43DR |          | 214     | 48                | 104               | 48               | 96  |
| XCZU47DR |          | 214     | 48                | 104               | 48               | 96  |
| XCZU48DR |          | 214     | 48                | 104               | 48               | 96  |
| XCZU63DR |          | 214     | 24                | 130               | 24               | 120 |
| XCZU64DR |          | 214     | 24                | 130               | 24               | 120 |
| XCZU65DR |          | 214     | 24                | 130               | 24               | 120 |
| XCZU67DR |          | 214     | 24                | 130               | 24               | 120 |
| XQZU28DR | FFRE1156 | 214     | 48                | 104               | 48               | 96  |
| XQZU48DR |          | 214     | 48                | 104               | 48               | 96  |
| XCZU25DR | FSVE1156 | 214     | 48                | 104               | 48               | 96  |
| XCZU27DR |          | 214     | 48                | 104               | 48               | 96  |
| XCZU28DR |          | 214     | 48                | 104               | 48               | 96  |
| XCZU42DR |          | 214     | 24                | 130               | 24               | 120 |
| XCZU43DR |          | 214     | 48                | 104               | 48               | 96  |
| XCZU47DR |          | 214     | 48                | 104               | 48               | 96  |
| XCZU48DR |          | 214     | 48                | 104               | 48               | 96  |
| XCZU63DR |          | 214     | 24                | 130               | 24               | 120 |
| XCZU64DR |          | 214     | 24                | 130               | 24               | 120 |
| XCZU65DR |          | 214     | 24                | 130               | 24               | 120 |
| XCZU65DR |          | 214     | 24                | 130               | 24               | 120 |
| XCZU11EG | FFVB1517 | 214     | 72                | 416               | 72               | 384 |
| XCZU17EG |          | 214     | 72                | 572               | 72               | 528 |
| XCZU19EG |          | 214     | 72                | 572               | 72               | 528 |
| XQZU19EG | FFRB1517 | 214     | 72                | 572               | 72               | 528 |
| XCZU7CG  | FFVF1517 | 214     | 48                | 416               | 48               | 384 |
| XCZU7EG  |          | 214     | 48                | 416               | 48               | 384 |
| XCZU7EV  |          | 214     | 48                | 416               | 48               | 384 |
| XCZU11EG |          | 214     | 48                | 416               | 48               | 384 |
| XAZU11EG |          | 214     | 48                | 416               | 48               | 384 |

Table 1-3: Available I/O Pins by Device/Package (Cont'd)

| Device   | Package  | PS I/Os | Total User I/O    |                   | Differential I/O |     |
|----------|----------|---------|-------------------|-------------------|------------------|-----|
|          |          |         | HD <sup>(1)</sup> | HP <sup>(1)</sup> | HD               | HP  |
| XCZU25DR | FFVG1517 | 214     | 48                | 299               | 48               | 276 |
| XCZU27DR |          | 214     | 48                | 299               | 48               | 276 |
| XCZU28DR |          | 214     | 48                | 299               | 48               | 276 |
| XCZU43DR |          | 214     | 48                | 299               | 48               | 276 |
| XCZU47DR |          | 214     | 48                | 299               | 48               | 276 |
| XCZU48DR |          | 214     | 48                | 299               | 48               | 276 |
| XQZU28DR | FFRG1517 | 214     | 48                | 299               | 48               | 276 |
| XCZU25DR | FSVG1517 | 214     | 48                | 299               | 48               | 276 |
| XCZU27DR |          | 214     | 48                | 299               | 48               | 276 |
| XCZU28DR |          | 214     | 48                | 299               | 48               | 276 |
| XCZU43DR |          | 214     | 48                | 299               | 48               | 276 |
| XCZU47DR |          | 214     | 48                | 299               | 48               | 276 |
| XCZU48DR |          | 214     | 48                | 299               | 48               | 276 |
| XQZU48DR | FSRG1517 | 214     | 48                | 299               | 48               | 276 |
| XCZU11EG | FFVC1760 | 214     | 96                | 416               | 96               | 384 |
| XCZU17EG |          | 214     | 96                | 416               | 96               | 384 |
| XCZU19EG |          | 214     | 96                | 416               | 96               | 384 |
| XQZU11EG | FFRC1760 | 214     | 96                | 416               | 96               | 384 |
| XQZU19EG |          | 214     | 96                | 416               | 96               | 384 |
| XCZU17EG | FFVD1760 | 214     | 48                | 260               | 48               | 240 |
| XCZU19EG |          | 214     | 48                | 260               | 48               | 240 |
| XCZU29DR | FFVF1760 | 214     | 96                | 312               | 96               | 288 |
| XCZU39DR |          | 214     | 96                | 312               | 96               | 288 |
| XCZU49DR |          | 214     | 96                | 312               | 96               | 288 |
| XQZU49DR | FSRF1760 | 214     | 96                | 312               | 96               | 288 |
| XCZU46DR | FFVH1760 | 214     | 48                | 312               | 48               | 288 |
| XQZU29DR | FFRF1760 | 214     | 96                | 312               | 96               | 288 |
| XCZU29DR | FSVF1760 | 214     | 96                | 312               | 96               | 288 |
| XCZU39DR |          | 214     | 96                | 312               | 96               | 288 |
| XCZU46DR | FSVH1760 | 214     | 48                | 312               | 48               | 288 |



Table 1-3: Available I/O Pins by Device/Package (Cont'd)

| Device   | Package  | PS I/Os | Total User I/O    |                   | Differential I/O |     |
|----------|----------|---------|-------------------|-------------------|------------------|-----|
|          |          |         | HD <sup>(1)</sup> | HP <sup>(1)</sup> | HD               | HP  |
| XCZU17EG | FFVE1924 | 214     | 96                | 572               | 96               | 528 |
| XCZU19EG |          | 214     | 96                | 572               | 96               | 528 |

**Notes:**

1. The maximum user I/O numbers do not include the GT serial transceiver pins or the PUDC\_B and POR\_OVERRIDE pins used for configuration.

# Pin Definitions

Table 1-4 lists the pin definitions.

Table 1-4: Pin Definitions

| Pin Name                                                                                                                                                 | Type           | Direction        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>User I/O Pins</b>                                                                                                                                     |                |                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| IO_L[1 to 24][P or N]_T[0 to 3] [U or L]_N[0 to 12]_ [multi-function]_[bank number] or<br>IO_T[0 to 3][U or L]_N[0 to 12]_[multi-function]_[bank number] |                |                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                                                                                                                                                          | Dedicated      | Input/<br>Output | <p>Most user I/O pins are capable of differential signaling and can be implemented as pairs. Each user I/O pin name consists of several indicator labels, where:</p> <ul style="list-style-type: none"> <li>IO indicates a user I/O pin.</li> <li>L[1 to 24] indicates a unique differential pair with P (positive) and N (negative) sides. User I/O pins without the L indicator are single-ended.</li> <li>T[0 to 3][U or L] indicates the assigned byte group and nibble location (upper or lower portion) within that group for the pin.</li> <li>N[0 to 12] the number of the I/O within its byte group.</li> <li>[multi-function] indicates any other functions that the pin can provide. If not used for this function, the pin can be a user I/O.</li> <li>[bank number] indicates the assigned bank for the user I/O pin.</li> </ul> |
| <b>User I/O Multi-Function Pins</b>                                                                                                                      |                |                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| GC or HDGC                                                                                                                                               | Multi-function | Input            | <p>Four global clock (GC or HDGC) pin pairs are in each bank. HDGC pins have direct access to the global clock buffers. GC pins have direct access to the global clock buffers and the MMCMs and PLLs that are in the clock management tile (CMT) adjacent to the same I/O bank. GC and HDGC inputs provide dedicated, high-speed access to the internal global and regional clock resources. GC and HDGC inputs use dedicated routing and must be used for clock inputs where the timing of various clocking features is imperative.</p> <p>Up-to-date information about designing with the GC (or HDGC) pin is available in the <i>UltraScale Architecture Clocking Resources User Guide</i> (<a href="#">UG572</a>).</p>                                                                                                                   |
| VRP <sup>(1)</sup>                                                                                                                                       | Multi-function | N/A              | <p>This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with a reference resistor).</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

Table 1-4: Pin Definitions (Cont'd)

| Pin Name                                                                                                                                                                                                                                | Type           | Direction    | Description                                                                                                                                                                                                                                                                                                |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DBC<br>QBC                                                                                                                                                                                                                              | Multi-function | Input        | Byte lane clock (DBC and QBC) input pin pairs are clock inputs directly driving source synchronous clocks to the bit slices in the I/O banks. In memory applications, these are also known as DQS. For more information, consult the <i>UltraScale Architecture SelectIO Resources User Guide</i> (UG571). |
| PERSTN[0 to 1]                                                                                                                                                                                                                          | Multi-function | Input        | Default reset pin locations for the integrated block for PCI Express.                                                                                                                                                                                                                                      |
| <b>Configuration Pins</b>                                                                                                                                                                                                               |                |              |                                                                                                                                                                                                                                                                                                            |
| For more information on configuration and recommended external pull-up/pull-down resistors, see the <i>Zynq UltraScale+ Device Technical Reference Manual</i> (UG1085) and the <i>UltraScale Architecture PCB Design Guide</i> (UG583). |                |              |                                                                                                                                                                                                                                                                                                            |
| PUDC_B                                                                                                                                                                                                                                  | Dedicated      | Input        | Active-Low input enables internal pull-ups during configuration on all SelectIO pins:<br>0 = Weak preconfiguration I/O pull-up resistors enabled.<br>1 = Weak preconfiguration I/O pull-up resistors disabled.<br>PUDC_B is powered by V <sub>CCAUX</sub> .                                                |
| POR_OVERRIDE                                                                                                                                                                                                                            | Dedicated      | Input        | Power-on reset delay override.<br>0 = Standard PL power-on delay time (recommended default).<br>1 = Faster PL power-on delay time.<br><br><b>CAUTION!</b> Do not allow this pin to float before and during configuration. This pin must be tied to V <sub>CCINT</sub> or GND.                              |
| PS_DONE                                                                                                                                                                                                                                 | Dedicated      | Output       | PS DONE signal. Requires an external pull-up resistor.                                                                                                                                                                                                                                                     |
| PS_ERROR_OUT                                                                                                                                                                                                                            | Dedicated      | Output       | PS error indication.                                                                                                                                                                                                                                                                                       |
| PS_ERROR_STATUS                                                                                                                                                                                                                         | Dedicated      | Output       | PS error status.                                                                                                                                                                                                                                                                                           |
| PS_INIT_B                                                                                                                                                                                                                               | Dedicated      | Input/Output | Initialization completion indicator after POR. High voltage indicates completion of initialization (PL). Requires an external pull-up resistor.                                                                                                                                                            |
| PS_JTAG_TCK                                                                                                                                                                                                                             | Dedicated      | Input        | JTAG data clock.                                                                                                                                                                                                                                                                                           |
| PS_JTAG_TDI                                                                                                                                                                                                                             | Dedicated      | Input        | JTAG data input.                                                                                                                                                                                                                                                                                           |
| PS_JTAG_TDO                                                                                                                                                                                                                             | Dedicated      | Output       | JTAG data output.                                                                                                                                                                                                                                                                                          |
| PS_JTAG_TMS                                                                                                                                                                                                                             | Dedicated      | Input        | JTAG mode select.                                                                                                                                                                                                                                                                                          |
| PS_MODE                                                                                                                                                                                                                                 | Dedicated      | Input/Output | PS MIO mode selection pins.                                                                                                                                                                                                                                                                                |
| PS_PADI                                                                                                                                                                                                                                 | Dedicated      | Input        | Crystal pad input. Real-time clock (RTC).                                                                                                                                                                                                                                                                  |
| PS_PADO                                                                                                                                                                                                                                 | Dedicated      | Output       | Crystal pad output. Real-time clock (RTC).                                                                                                                                                                                                                                                                 |

Table 1-4: Pin Definitions (Cont'd)

| Pin Name                                                                                                                                                                                                                                    | Type      | Direction | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PS_POR_B                                                                                                                                                                                                                                    | Dedicated | Input     | Power on reset. PS_POR_B must be held at 0 until all PS power supplies meet voltage requirements and the PS_CLK reference is within specification. When deasserted the PS begins the boot process.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| PS_PROG_B                                                                                                                                                                                                                                   | Dedicated | Input     | PROG_B signal to reset configuration block. Requires an external pull-up resistor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| PS_REF_CLK                                                                                                                                                                                                                                  | Dedicated | Input     | System reference clock. PS_CLK must be between 27 MHz and 60 MHz.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| PS_SRST_B                                                                                                                                                                                                                                   | Dedicated | Input     | System reset. For use when debugging. When 0, forces the PS to enter the system reset sequence.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| <b>Power/Ground Pins</b>                                                                                                                                                                                                                    |           |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| For more information on voltage specifications see the <i>Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics (DS925)</i> or the <i>Zynq UltraScale+ RFSoc Data Sheet: DC and AC Switching Characteristics (DS926)</i> . |           |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| GND                                                                                                                                                                                                                                         | Dedicated | N/A       | Ground.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| RSVDGND                                                                                                                                                                                                                                     | Dedicated | N/A       | Reserved pins that must be tied to GND.<br><b>Note:</b> These pins are labeled differently depending upon the device. They can serve a different purpose between footprint compatible devices. To migrate to a footprint compatible device, account for any variation in pin functionality.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| RSVD                                                                                                                                                                                                                                        | Dedicated | N/A       | Reserved pin. Leave floating.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| VCCINT                                                                                                                                                                                                                                      | Dedicated | N/A       | Power-supply pins for the PL internal logic.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| VCCINT_IO                                                                                                                                                                                                                                   | Dedicated | N/A       | Power-supply pins for the I/O banks. VCCINT_IO must be connected to VCCBRAM on the board.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| VCCINT_VCU                                                                                                                                                                                                                                  | Dedicated | N/A       | Power-supply pins for the video codec unit (EV devices only).<br><b>Note:</b> If the video codec unit is not used, then connect the VCCINT_VCU pins to GND to reduce power. In the CG and EG devices, the EV device VCCINT_VCU pins appear as RSVDGND pins.<br><b>Note:</b> When migrating from an EV device to a CG or EG device in the same package, AMD recommends connecting the VCCINT_VCU pins to GND to reduce power. Further VCCINT_VCU migration guidelines are available in <i>UltraScale Architecture PCB Design Guide (UG583)</i> .<br><br><br><b>IMPORTANT:</b> $V_{CCINT\_VCU}$ requires its own dedicated power supply. Do not combine with other power rails on the PCB. |
| VCCAUX                                                                                                                                                                                                                                      | Dedicated | N/A       | Power-supply pins for auxiliary circuits.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

Table 1-4: Pin Definitions (Cont'd)

| Pin Name                          | Type           | Direction    | Description                                                                                                                                                                                                                                                                                            |
|-----------------------------------|----------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VCCAUX_IO                         | Dedicated      | N/A          | Auxiliary power-supply pins for the I/O banks. VCCAUX_IO must be connected to VCCAUX on the board.<br><br><b>Note:</b> Package files for XQ ruggedized devices (for example: FFRC784) have unique pin names for VCCAUX_HPIO and VCCAUX_HDIO. These pins can be connected to a common VCCAUX_IO supply. |
| VCCBRAM                           | Dedicated      | N/A          | Power-supply pins for PL block RAM logic.                                                                                                                                                                                                                                                              |
| VCCO_[bank number] <sup>(2)</sup> | Dedicated      | N/A          | Power-supply pins for the output drivers (per bank).                                                                                                                                                                                                                                                   |
| VREF_[bank number]                | Dedicated      | N/A          | Voltage reference for input pins (per bank).                                                                                                                                                                                                                                                           |
| VCCADC                            | Dedicated      | N/A          | System Monitor analog supply voltage.                                                                                                                                                                                                                                                                  |
| GNDADC                            | Dedicated      | N/A          | System Monitor analog ground.                                                                                                                                                                                                                                                                          |
| VCC_PSADC                         | Dedicated      | N/A          | PS ADC supply voltage.                                                                                                                                                                                                                                                                                 |
| GND_PSADC                         | Dedicated      | N/A          | PS ADC analog ground.                                                                                                                                                                                                                                                                                  |
| VCC_PSAUX                         | Dedicated      | N/A          | PS auxiliary circuits supply voltage.                                                                                                                                                                                                                                                                  |
| VCC_PSBATT                        | Dedicated      | N/A          | PS RTC battery supply voltage. When not used, tie to GND.                                                                                                                                                                                                                                              |
| VCC_PSDDR_PLL                     | Dedicated      | N/A          | PS DDR PLL supply voltage.                                                                                                                                                                                                                                                                             |
| VCC_PSPLL                         | Dedicated      | N/A          | PS PLL (DPLL, RPLL, APLL, VPLL, IOPLL) supply voltage.                                                                                                                                                                                                                                                 |
| VCC_PSINTFP                       | Dedicated      | N/A          | PS full-power domain supply voltage.                                                                                                                                                                                                                                                                   |
| VCC_PSINTFP_DDR                   | Dedicated      | N/A          | PS DDR full-power domain supply voltage.                                                                                                                                                                                                                                                               |
| VCC_PSINTLP                       | Dedicated      | N/A          | PS low-power domain supply voltage.                                                                                                                                                                                                                                                                    |
| VCCO_PSIO[0:3]_[500:503]          | Dedicated      | N/A          | PS I/O supply voltage.                                                                                                                                                                                                                                                                                 |
| VCCO_PSDDR                        | Dedicated      | N/A          | PS DDR controller I/O supply voltage.                                                                                                                                                                                                                                                                  |
| <b>PS MIO Pins</b>                |                |              |                                                                                                                                                                                                                                                                                                        |
| PS_MIO                            | Multi-function | Input/Output | Multiplexed I/O can be configured to support multiple I/O interfaces. These interfaces include SPI and Quad-SPI flash, NAND, USB, Ethernet, SDIO, UART, SPI, and GPIO interfaces.                                                                                                                      |
| <b>PS DDR Pins</b>                |                |              |                                                                                                                                                                                                                                                                                                        |
| PS_DDR_DQ                         | Dedicated      | Input/Output | DRAM data.                                                                                                                                                                                                                                                                                             |
| PS_DDR_DQS_P                      | Dedicated      | Input/Output | DRAM differential data strobe positive.                                                                                                                                                                                                                                                                |
| PS_DDR_DQS_N                      | Dedicated      | Input/Output | DRAM differential data strobe negative.                                                                                                                                                                                                                                                                |
| PS_DDR_ALERT_N                    | Dedicated      | Input        | DRAM alert signal.                                                                                                                                                                                                                                                                                     |
| PS_DDR_ACT_N                      | Dedicated      | Output       | DRAM activation command.                                                                                                                                                                                                                                                                               |

Table 1-4: Pin Definitions (Cont'd)

| Pin Name                                 | Type           | Direction     | Description                                                                                                                                                                                                                                                                                                                                                         |
|------------------------------------------|----------------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PS_DDR_A                                 | Dedicated      | Output        | DRAM row and column address.                                                                                                                                                                                                                                                                                                                                        |
| PS_DDR_BA                                | Dedicated      | Output        | DRAM bank address.                                                                                                                                                                                                                                                                                                                                                  |
| PS_DDR_BG                                | Dedicated      | Output        | DRAM bank group.                                                                                                                                                                                                                                                                                                                                                    |
| PS_DDR_CK_N                              | Dedicated      | Output        | DRAM differential clock negative.                                                                                                                                                                                                                                                                                                                                   |
| PS_DDR_CK                                | Dedicated      | Output        | DRAM differential clock positive.                                                                                                                                                                                                                                                                                                                                   |
| PS_DDR_CKE                               | Dedicated      | Output        | DRAM clock enable.                                                                                                                                                                                                                                                                                                                                                  |
| PS_DDR_CS                                | Dedicated      | Output        | DRAM chip select.                                                                                                                                                                                                                                                                                                                                                   |
| PS_DDR_DM                                | Dedicated      | Output        | DRAM data mask.                                                                                                                                                                                                                                                                                                                                                     |
| PS_DDR_ODT                               | Dedicated      | Output        | DRAM termination control.                                                                                                                                                                                                                                                                                                                                           |
| PS_DDR_PARITY                            | Dedicated      | Output        | DRAM parity signal                                                                                                                                                                                                                                                                                                                                                  |
| PS_DDR_RAM_RST_N                         | Dedicated      | Output        | DRAM reset signal, active low.                                                                                                                                                                                                                                                                                                                                      |
| PS_DDR_ZQ                                | Dedicated      | Input/Output  | ZQ calibration signal.                                                                                                                                                                                                                                                                                                                                              |
| <b>System Monitor Pins<sup>(3)</sup></b> |                |               |                                                                                                                                                                                                                                                                                                                                                                     |
| AD[0 to 15][P or N]                      | Multi-function | Input         | System Monitor differential auxiliary analog inputs 0–15.                                                                                                                                                                                                                                                                                                           |
| VREFP                                    | Dedicated      | N/A           | Voltage reference input.                                                                                                                                                                                                                                                                                                                                            |
| VREFN                                    | Dedicated      | N/A           | Voltage reference GND.                                                                                                                                                                                                                                                                                                                                              |
| VP                                       | Dedicated      | Input         | System Monitor dedicated differential analog input (positive side).                                                                                                                                                                                                                                                                                                 |
| VN                                       | Dedicated      | Input         | System Monitor dedicated differential analog input (negative side).                                                                                                                                                                                                                                                                                                 |
| I2C_SCLK                                 | Multi-function | Bidirectional | <p>I2C serial clock. Directly connected to the System Monitor DRP interface for I2C operation configuration.</p> <p> <b>IMPORTANT:</b> Because the SYSMON I2C interface is active after power-on, this pin should only be used for I2C access until after configuration.</p>     |
| I2C_SDA                                  | Multi-function | Bidirectional | <p>I2C serial data line. Directly connected to the System Monitor DRP interface for I2C operation configuration.</p> <p> <b>IMPORTANT:</b> Because the SYSMON I2C interface is active after power-on, this pin should only be used for I2C access until after configuration.</p> |

Table 1-4: Pin Definitions (Cont'd)

| Pin Name                                                                                                                                                                                                                                                                                                                           | Type           | Direction     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SMBALERT                                                                                                                                                                                                                                                                                                                           | Multi-function | Bidirectional | <p>Optional PMBus alert, interrupt signal. When Low, indicates a system fault that must be cleared using PMBus commands. Connect to SMBALERT_TS.</p> <p>For more information, see the <i>UltraScale Architecture System Monitor User Guide</i> (UG580).</p> <p></p> <p><b>IMPORTANT:</b> By default, the PMBus is active prior to configuration. Only use as a multi-functional I/O pin in designs that can tolerate this pin being driven prior to configuration.</p> <p>This pin is present on Kintex UltraScale+ and Virtex UltraScale+ devices.</p> |
| <b>Multi-gigabit Serial Transceiver Pins (GTHE4, GTYE4, and PS-GTR)</b>                                                                                                                                                                                                                                                            |                |               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| For more information on the GTH and GTY transceivers, see the <i>UltraScale Architecture GTH Transceiver User Guide</i> (UG576) or <i>UltraScale Architecture GTY Transceiver User Guide</i> (UG578). For more information on the PS-GTR transceivers, see the <i>Zynq UltraScale+ Device Technical Reference Manual</i> (UG1085). |                |               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| MGTHRXP or N][0 to 3]_<br>_GT quad number]                                                                                                                                                                                                                                                                                         | Dedicated      | Input         | RXP and RXN are the differential input pairs for each of the receivers in the GTH Quad.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| MGHTXP or N][0 to 3]_<br>_GT quad number]                                                                                                                                                                                                                                                                                          | Dedicated      | Output        | TXP and TXN are the differential output pairs for each of the transmitters in the GTH Quad.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| MGTYPXP or N][0 to 3]_<br>_GT quad number]                                                                                                                                                                                                                                                                                         | Dedicated      | Input         | RXP and RXN are the differential input pairs for each of the receivers in the GTY Quad.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| MGTYPXP or N][0 to 3]_<br>_GT quad number]                                                                                                                                                                                                                                                                                         | Dedicated      | Output        | TXP and TXN are the differential output pairs for each of the transmitters in the GTY Quad.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| PS_MGTRRX[P or N][0 to 3]_<br>_GT quad number]                                                                                                                                                                                                                                                                                     | Dedicated      | Input         | RXP and RXN are the differential input pairs for each of the receivers in the PS-GTR Quad.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| PS_MGTRTX[P or N][0 to 3]_<br>_GT quad number]                                                                                                                                                                                                                                                                                     | Dedicated      | Output        | TXP and TXN are the differential output pairs for each of the transmitters in the PS-GTR Quad.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| MGTAVCC_[L or R]<br>[N or S] <sup>(4)</sup>                                                                                                                                                                                                                                                                                        | Dedicated      | Input         | Analog power-supply pin for the receiver and transmitter internal circuits for the GTH or GTY transceivers.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| PS_MGTRAVCC                                                                                                                                                                                                                                                                                                                        | Dedicated      | N/A           | Analog power-supply pin for the receiver and transmitter internal circuits for the PS-GTR transceivers.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| MGTAVTT_[L or R]<br>[N or S] <sup>(4)</sup>                                                                                                                                                                                                                                                                                        | Dedicated      | Input         | Analog power-supply pin for the transmitter and receiver termination circuits for the GTH or GTY transceivers.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| MGTVCCAUX_[L or R]<br>[N or S] <sup>(4)</sup>                                                                                                                                                                                                                                                                                      | Dedicated      | Input         | Auxiliary analog Quad PLL (QPLL) voltage supply for the transceivers.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

Table 1-4: Pin Definitions (Cont'd)

| Pin Name                                         | Type      | Direction    | Description                                                                                                           |
|--------------------------------------------------|-----------|--------------|-----------------------------------------------------------------------------------------------------------------------|
| PS_MGTRAVTT                                      | Dedicated | N/A          | Analog power-supply pin for the transmitter and receiver termination circuits for the PS-GTR transceivers.            |
| MGTREFCLK[0 or 1]<br>[P or N]                    | Dedicated | Input/Output | Configured as either reference clock input pins or as RX recovered clock output pins for the GTH or GTY transceivers. |
| PS_MGTREFCLK[0 to 3]<br>[P or N]                 | Dedicated | Input        | Differential reference clock for the PS-GTR transceivers.                                                             |
| MGTAVTTTRCAL_[L or R]<br>[N or S] <sup>(4)</sup> | Dedicated | N/A          | Bias current supply for the termination resistor calibration circuit.                                                 |
| MGTRREF_[L or R]<br>[N or S] <sup>(4)</sup>      | Dedicated | Input        | Calibration resistor pin for the termination resistor calibration circuit for the GTH or GTY transceivers.            |
| PS_MGTRREF                                       | Dedicated | Input        | Calibration resistor pin for the termination resistor calibration circuit for the PS-GTR transceivers.                |
| <b>Zynq UltraScale+ RFSoc Dedicated Pins</b>     |           |              |                                                                                                                       |
| VCCSDFEC                                         | Dedicated | N/A          | Power supply for the FEC blocks.                                                                                      |
| VCCINT_AMS                                       | Dedicated | N/A          | Digital power supply for the DDC.                                                                                     |
| ADC_AVCC                                         | Dedicated | N/A          | Core ADC and PLL power supply.                                                                                        |
| ADC_AVCCAUX                                      | Dedicated | N/A          | Input buffer and PLL power supply.                                                                                    |
| ADC_GND                                          | Dedicated | N/A          | Analog ground for the ADC.                                                                                            |
| ADC_SUB_GND                                      | Dedicated | N/A          | Digital ground for the ADC.                                                                                           |
| ADC_CLK_[P or N]                                 | Dedicated | Input        | External reference clock for PLL or ADC direct sampling clock input.                                                  |
| VCM01/VCM23                                      | Dedicated | N/A          | ADC common mode voltage.                                                                                              |
| ADC_VIN_[0 to 3 or _I01<br>and _I23]_[P or N]    | Dedicated | Input        | Analog input signal to the ADC.                                                                                       |
| ADC_REXT                                         | Dedicated | N/A          | ADC external resistor.                                                                                                |
| DAC_AVCC                                         | Dedicated | N/A          | Core DAC and PLL power supply.                                                                                        |
| DAC_AVCCAUX                                      | Dedicated | N/A          | DAC and PLL power supply.                                                                                             |
| DAC_AVTT                                         | Dedicated | N/A          | Termination voltage for on-die 50Ω termination resistors.                                                             |
| DAC_GND                                          | Dedicated | N/A          | Analog ground for the DAC.                                                                                            |
| DAC_SUB_GND                                      | Dedicated | N/A          | Digital ground for the DAC.                                                                                           |
| DAC_CLK_[P or N]                                 | Dedicated | Input        | External reference clock for PLL or DAC direct sampling clock input.                                                  |
| SYSREF_[P or N]                                  | Dedicated | Input        | External reference clock/trigger for synchronizing timing of the data converters.                                     |
| DAC_VOUT[0 to 3]_[P or N]                        | Dedicated | Output       | Analog output signals from the DAC.                                                                                   |
| DAC_REXT                                         | Dedicated | Input        | DAC external resistor.                                                                                                |



Table 1-4: Pin Definitions (Cont'd)

| Pin Name                    | Type      | Direction | Description                                                                                                                                                       |
|-----------------------------|-----------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Other Dedicated Pins</b> |           |           |                                                                                                                                                                   |
| DXN                         | Dedicated | N/A       | Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). The thermal diode is accessed by using the DXP and DXN pins. When not used, tie to GND.                |
| DXP                         |           |           | To use the thermal diode an appropriate external thermal monitoring IC must be added. Consult the external thermal monitoring IC data sheet for usage guidelines. |

**Notes:**

1. See the DCI sections in *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)) for more information on the VRP pins.
2.  $V_{CCO}$  pins in unbonded banks must be connected to the  $V_{CCO}$  for that bank (for package migration). Do NOT connect unbonded  $V_{CCO}$  pins to different supplies. Without a package migration requirement,  $V_{CCO}$  pins in unbonded banks can be tied to a common supply ( $V_{CCO}$  or GND).
3. See the *UltraScale Architecture System Monitor User Guide* ([UG580](#)) for the default connections required to support on-chip monitoring.
4. L (left), R (right), N (north), and S (south) signify the GT transceiver quad power supply groups.

## Footprint Compatibility between Packages

Zynq UltraScale+ devices are footprint compatible only with other Zynq UltraScale+ devices with the same number of package pins and the same preceding alphabetic designator. For example, XCZU9EG-FFVB1156 is compatible with the XCZU15EG-FFVB1156, but not with the XCZU9EG-FFVC900. Pins that are available in one device but are not available in another device are labeled as *No Connects* in the other device's package file.



**IMPORTANT:** Footprint compatibility does not necessarily imply that all pins will function in the same manner for different devices in a package. For limitations and guidelines on designing for footprint compatible packages, refer to the *Migration Between the Zynq UltraScale+ Devices and Packages* section of *UltraScale Architecture PCB Design Guide* ([UG583](#)).

[Table 1-5](#) shows the footprint compatible devices available for each package. See the *Zynq UltraScale+ MPSoC Overview* ([DS891](#)) for specific package letter code options. All non-InFO packages are available with eutectic BGA balls. For these packages, the device type is XQ and the Pb-free signifier in the package name is a Q.

**Table 1-5: Footprint Compatibility**

| Packages               | Footprint Compatible Devices    |                                 |                                             |                       |                                             |                                                         |
|------------------------|---------------------------------|---------------------------------|---------------------------------------------|-----------------------|---------------------------------------------|---------------------------------------------------------|
| SBVA484<br>SFRA484     | XCZU1CG,<br>XCZU1EG,<br>XAZU1EG | XCZU2CG,<br>XCZU2EG,<br>XAZU2EG | XCZU3CG,<br>XCZU3EG,<br>XAZU3EG,<br>XQZU3EG |                       |                                             |                                                         |
| UBVA494                | XCZU1CG,<br>XCZU1EG             |                                 |                                             |                       |                                             |                                                         |
| UBVA530                | XCZU2CG,<br>XCZU2EG,            | XCZU3CG,<br>XCZU3EG,            |                                             |                       |                                             |                                                         |
| SFVA625                | XCZU1CG,<br>XCZU1EG,<br>XAZU1EG | XCZU2CG,<br>XCZU2EG,<br>XAZU2EG | XCZU3CG,<br>XCZU3EG,<br>XAZU3EG             |                       |                                             |                                                         |
| SFVC784<br>SFRC784     | XCZU1CG,<br>XCZU1EG,<br>XAZU1EG | XCZU2CG,<br>XCZU2EG,<br>XAZU2EG | XCZU3CG,<br>XCZU3EG,<br>XAZU3EG,<br>XQZU3EG | XCZU3TCG,<br>XCZU3TEG | XCZU4CG,<br>XCZU4EG,<br>XCZU4EV,<br>XAZU4EV | XCZU5CG,<br>XCZU5EG,<br>XCZU5EV,<br>XAZU5EV,<br>XQZU5EV |
| SFVD784 <sup>(3)</sup> | XCZU3TCG,<br>XCZU3TEG           |                                 |                                             |                       |                                             |                                                         |
| SFVE784 <sup>(3)</sup> | XCZU4CG,<br>XCZU4EG,<br>XCZU4EV | XCZU5CG,<br>XCZU5EG,<br>XCZU5EV |                                             |                       |                                             |                                                         |

Table 1-5: Footprint Compatibility (Cont'd)

| Packages                                     | Footprint Compatible Devices                                                              |                                                                                                                             |                                                                                                                                                            |  |                                                      |  |
|----------------------------------------------|-------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|--|------------------------------------------------------|--|
| FBVB900<br>FFRB900                           | XCZU4CG,<br>XCZU4EG,<br>XCZU4EV                                                           | XCZU5CG,<br>XCZU5EG,<br>XCZU5EV,<br>XQZU5EV                                                                                 | XCZU7CG,<br>XCZU7EG,<br>XCZU7EV,<br>XAZU7EV,<br>XQZU7EV                                                                                                    |  |                                                      |  |
| FFVC900<br>FFRC900                           | XCZU6CG,<br>XCZU6EG                                                                       | XCZU9CG,<br>XCZU9EG,<br>XQZU9EG                                                                                             | XCZU15EG,<br>XQZU15EG                                                                                                                                      |  |                                                      |  |
| FFVB1156<br>FFRB1156                         | XCZU6CG,<br>XCZU6EG                                                                       | XCZU9CG,<br>XCZU9EG,<br>XQZU9EG                                                                                             | XCZU15EG,<br>XQZU15EG                                                                                                                                      |  |                                                      |  |
| FFVC1156<br>FFRC1156                         | XCZU7CG,<br>XCZU7EG,<br>XCZU7EV,<br>XQZU7EV                                               | XCZU11EG,<br>XQZU11EG                                                                                                       |                                                                                                                                                            |  |                                                      |  |
| FFVD1156                                     | XCZU21DR,<br>XQZU21DR                                                                     |                                                                                                                             |                                                                                                                                                            |  |                                                      |  |
| FFVE1156<br>FSVE1156<br>FFRE1156             | XCZU25DR                                                                                  | XCZU27DR,<br>XCZU43DR <sup>(1)</sup> ,<br>XCZU47DR <sup>(1)</sup> ,<br>XCZU48DR <sup>(1)</sup> ,<br>XQZU48DR <sup>(1)</sup> | XCZU42DR <sup>(1)(2)</sup> ,<br>XCZU63DR <sup>(1)(2)</sup> ,<br>XCZU64DR <sup>(1)(2)</sup> ,<br>XCZU65DR <sup>(1)(2)</sup> ,<br>XCZU67DR <sup>(1)(2)</sup> |  | XCZU28DR,<br>XQZU28DR                                |  |
| FFVB1517                                     | XCZU11EG                                                                                  | XCZU17EG                                                                                                                    | XCZU19EG,<br>XQZU19EG                                                                                                                                      |  |                                                      |  |
| FFVF1517                                     | XCZU7CG,<br>XCZU7EG,<br>XCZU7EV                                                           | XCZU11EG,<br>XAZU11EG                                                                                                       |                                                                                                                                                            |  |                                                      |  |
| FFVG1517<br>FSVG1517<br>FSRG1517             | XCZU25DR                                                                                  | XCZU27DR,<br>XCZU43DR <sup>(1)</sup> ,<br>XCZU47DR <sup>(1)</sup> ,<br>XCZU49DR <sup>(1)</sup>                              | XCZU28DR,<br>XQZU28DR                                                                                                                                      |  | XCZU48DR <sup>(1)</sup> ,<br>XQZU48DR <sup>(1)</sup> |  |
| FFVC1760<br>FFRC1760                         | XCZU11EG,<br>XQZU11EG                                                                     | XCZU17EG                                                                                                                    | XCZU19EG,<br>XQZU19EG                                                                                                                                      |  |                                                      |  |
| FFVD1760                                     | XCZU17EG                                                                                  | XCZU19EG                                                                                                                    |                                                                                                                                                            |  |                                                      |  |
| FFVF1760<br>FSVF1760<br>FFRF1760<br>FSRF1760 | XCZU29DR,<br>XCZU39DR,<br>XCZU49DR <sup>(1)</sup><br>XQZU29DR,<br>XQZU49DR <sup>(1)</sup> |                                                                                                                             |                                                                                                                                                            |  |                                                      |  |
| FFVH1760                                     | XCZU46DR                                                                                  |                                                                                                                             |                                                                                                                                                            |  |                                                      |  |
| FSVH1760                                     | XCZU46DR                                                                                  |                                                                                                                             |                                                                                                                                                            |  |                                                      |  |

Table 1-5: Footprint Compatibility (Cont'd)

| Packages                                     | Footprint Compatible Devices                                                              |                                                                                                                             |                                                                                                                                                            |  |                                                      |  |
|----------------------------------------------|-------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|--|------------------------------------------------------|--|
| FBVB900<br>FFRB900                           | XCZU4CG,<br>XCZU4EG,<br>XCZU4EV                                                           | XCZU5CG,<br>XCZU5EG,<br>XCZU5EV,<br>XQZU5EV                                                                                 | XCZU7CG,<br>XCZU7EG,<br>XCZU7EV,<br>XAZU7EV,<br>XQZU7EV                                                                                                    |  |                                                      |  |
| FFVC900<br>FFRC900                           | XCZU6CG,<br>XCZU6EG                                                                       | XCZU9CG,<br>XCZU9EG,<br>XQZU9EG                                                                                             | XCZU15EG,<br>XQZU15EG                                                                                                                                      |  |                                                      |  |
| FFVB1156<br>FFRB1156                         | XCZU6CG,<br>XCZU6EG                                                                       | XCZU9CG,<br>XCZU9EG,<br>XQZU9EG                                                                                             | XCZU15EG,<br>XQZU15EG                                                                                                                                      |  |                                                      |  |
| FFVC1156<br>FFRC1156                         | XCZU7CG,<br>XCZU7EG,<br>XCZU7EV,<br>XQZU7EV                                               | XCZU11EG,<br>XQZU11EG                                                                                                       |                                                                                                                                                            |  |                                                      |  |
| FFVD1156                                     | XCZU21DR,<br>XQZU21DR                                                                     |                                                                                                                             |                                                                                                                                                            |  |                                                      |  |
| FFVE1156<br>FSVE1156<br>FFRE1156             | XCZU25DR                                                                                  | XCZU27DR,<br>XCZU43DR <sup>(1)</sup> ,<br>XCZU47DR <sup>(1)</sup> ,<br>XCZU48DR <sup>(1)</sup> ,<br>XQZU48DR <sup>(1)</sup> | XCZU42DR <sup>(1)(2)</sup> ,<br>XCZU63DR <sup>(1)(2)</sup> ,<br>XCZU64DR <sup>(1)(2)</sup> ,<br>XCZU65DR <sup>(1)(2)</sup> ,<br>XCZU67DR <sup>(1)(2)</sup> |  | XCZU28DR,<br>XQZU28DR                                |  |
| FFVB1517                                     | XCZU11EG                                                                                  | XCZU17EG                                                                                                                    | XCZU19EG,<br>XQZU19EG                                                                                                                                      |  |                                                      |  |
| FFVF1517                                     | XCZU7CG,<br>XCZU7EG,<br>XCZU7EV                                                           | XCZU11EG,<br>XAZU11EG                                                                                                       |                                                                                                                                                            |  |                                                      |  |
| FFVG1517<br>FSVG1517<br>FSRG1517             | XCZU25DR                                                                                  | XCZU27DR,<br>XCZU43DR <sup>(1)</sup> ,<br>XCZU47DR <sup>(1)</sup> ,<br>XCZU49DR <sup>(1)</sup>                              | XCZU28DR,<br>XQZU28DR                                                                                                                                      |  | XCZU48DR <sup>(1)</sup> ,<br>XQZU48DR <sup>(1)</sup> |  |
| FFVC1760<br>FFRC1760                         | XCZU11EG,<br>XQZU11EG                                                                     | XCZU17EG                                                                                                                    | XCZU19EG,<br>XQZU19EG                                                                                                                                      |  |                                                      |  |
| FFVD1760                                     | XCZU17EG                                                                                  | XCZU19EG                                                                                                                    |                                                                                                                                                            |  |                                                      |  |
| FFVF1760<br>FSVF1760<br>FFRF1760<br>FSRF1760 | XCZU29DR,<br>XCZU39DR,<br>XCZU49DR <sup>(1)</sup><br>XQZU29DR,<br>XQZU49DR <sup>(1)</sup> |                                                                                                                             |                                                                                                                                                            |  |                                                      |  |
| FFVH1760                                     | XCZU46DR                                                                                  |                                                                                                                             |                                                                                                                                                            |  |                                                      |  |
| FSVH1760                                     | XCZU46DR                                                                                  |                                                                                                                             |                                                                                                                                                            |  |                                                      |  |

Table 1-5: Footprint Compatibility (Cont’d)

| Packages | Footprint Compatible Devices |          |  |
|----------|------------------------------|----------|--|
| FFVE1924 | XCZU17EG                     | XCZU19EG |  |

Notes:

- 1. The ZU4xDR and ZU6xDR devices are footprint compatible devices. However, they have a different set of ADC and DAC power sequencing requirements from the ZU2xDR devices. Refer to [Zynq UltraScale+ RFSoc Data Sheet: DC and AC Switching Characteristics \(DS926\)](#) for specific power sequencing differences.
- 2. The XCZU42DR, XCZU63DR, XCZU64DR, XCZU65DR, and XCZU67DR are only partially compatible with other devices in the FFVE1156 and FSVE1156 packages due to key differences in the ADC and DAC architecture. When planning migration between devices, differences that must be addressed include ADC and DAC bank/pin locations and power rail voltage specifications.
- 3. Migration between the SFVD784 and SFVE784 is possible by following the guidelines in the [Migration Between SFVD784 and SFVE784 Packages](#) section.

Many Zynq UltraScale+ devices that are footprint compatible in a package have different I/O bank and transceiver quad numbers connected to the same package pins. Due to these differences, when migrating between devices in a specific package, the type of bank (HD vs. HP) or quad (PS-GTR, GTH, or GTY), whether a bank is connected or NC at the package pins, and where the bank or quad is located on the die must be taken into consideration. [Table 1-7](#) and [Table 1-8](#) show how the banks and transceiver quads are numbered between devices in each package.

For all grouped-together footprint-compatible packages, the bank and quad numbers in the same column (indicated by the letters A through Z) for each device are connected to the same package pins. For example, in the FFVB1517 packages, bank 88 for the XCZU11 is connected to the same pins as bank 90 for the XCZU17 and XCZU19.

A limited number of HP I/O banks have fewer than 52 SelectIO pins. For a visual representation of all of this information, see the [Die Level Bank Numbering Overview](#) section.

## Migration Between SFVD784 and SFVE784 Packages

The SFVD784 and SFVE784 packages support footprint compatibility provided the following differences are addressed during the design process:

- The transition between seven GND pins in the SFVD784 and six HP I/O pins plus one VREF pin from Bank 66 in the SFVE784. Pins M6, M8, L9, L11, L13, L15, and J15 as shown in the following figure.

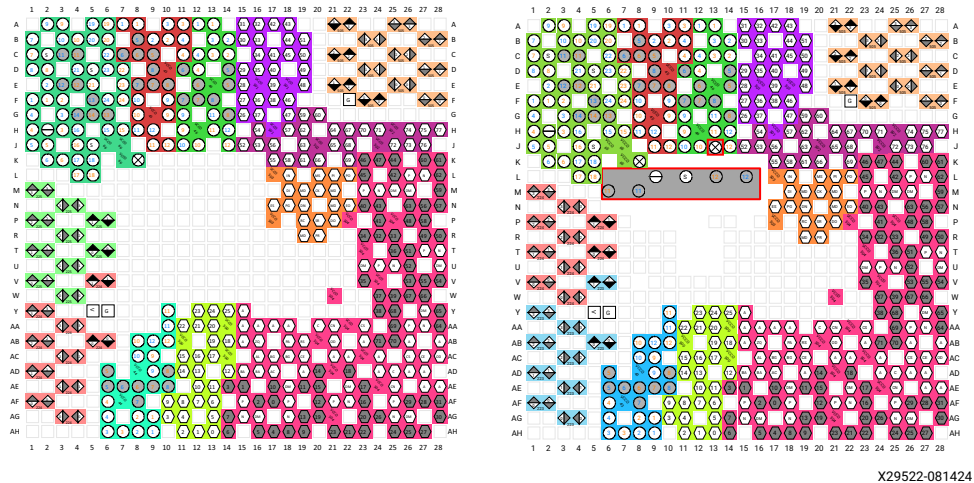


Figure 1-1: SFVD784 I/O Pin Map (Left) vs. SFVE784 I/O Pin Map (Right)

- The transition between four VCCINT pins in the SFVD784 and four VCCINT\_VCU pins for EV devices, or RSVDGND pins for CG and EG devices in the SFVE784. Pins W14, R16, U16, and W16 as shown in the following figure.

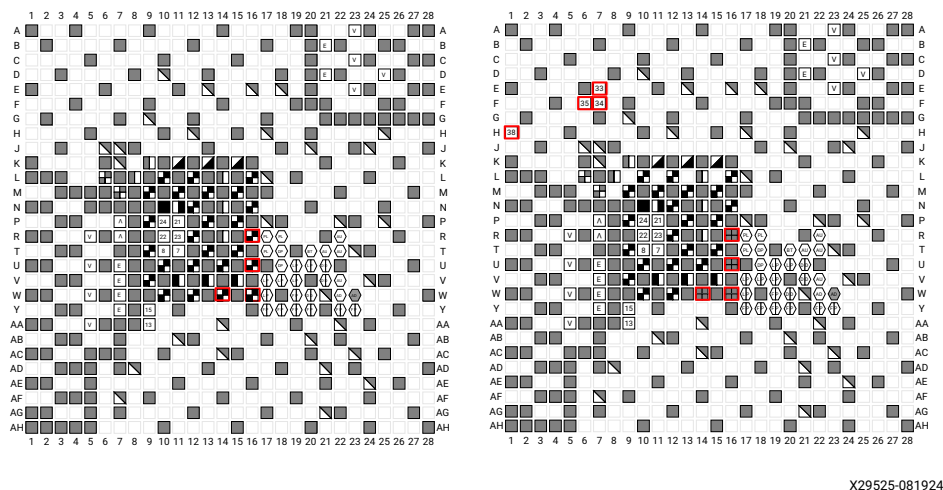


Figure 1-2: SFVD784 Configuration and Power Pin Map (Left) vs. SFVE784 Configuration and Power Pin Map (Right)

- The differences between the System Monitor analog input pin assignments in bank 44 for the SFVD784 and SFVE784.
  - For example: AD8N on pin AB9 for SFVD784 vs. AD0N on pin AB9 for SFVE784.
  - Refer to the [ASCII Pinout Files](#) for a full list of analog input pin assignments.
- The addition of PERSTN0, PERSTN1\_I2C\_SDA, I2C\_SCLK, and SMBALERT functionality on pins F6, F7, and F8 for SFVE784.

See the *I/O Bank Migration* and *Transceiver Quad Migration* sections for differences in bank numbering between SFVD784 and SFVE784 devices. The following table lists the changed pin functions between migrated devices.

Table 1-6: Pin Functionality Differences Between SFVD784 and SFVE784 Packages

| Pin | ZU3T<br>SFVD784 Pin Name  | ZU4CG, ZU4EG, ZU5CG, ZU5EG<br>SFVE784 Pin Names | ZU4EV, ZU5EV<br>SFVE784 Pin Name   |
|-----|---------------------------|-------------------------------------------------|------------------------------------|
| J13 | GND                       | VREF_66                                         | VREF_66                            |
| L11 | GND                       | IO_T3U_N12_66                                   | IO_T3U_N12_66                      |
| L13 | GND                       | IO_L12P_T1U_N10_GC_66                           | IO_L12P_T1U_N10_GC_66              |
| L15 | GND                       | IO_L12N_T1U_N11_GC_66                           | IO_L12N_T1U_N11_GC_66              |
| L9  | GND                       | IO_T0U_N12_VRP_66                               | IO_T0U_N12_VRP_66                  |
| M6  | GND                       | IO_L11P_T1U_N8_GC_66                            | IO_L11P_T1U_N8_GC_66               |
| M8  | GND                       | IO_L11N_T1U_N9_GC_66                            | IO_L11N_T1U_N9_GC_66               |
| R16 | VCCINT                    | RSVDGND                                         | VCCINT_VCU                         |
| U16 | VCCINT                    | RSVDGND                                         | VCCINT_VCU                         |
| W14 | VCCINT                    | RSVDGND                                         | VCCINT_VCU                         |
| W16 | VCCINT                    | RSVDGND                                         | VCCINT_VCU                         |
| E7  | IO_L23P_T3U_N8_66         | IO_L23P_T3U_N8_I2C_SCLK_65                      | IO_L23P_T3U_N8_I2C_SCLK_65         |
| F6  | IO_L24N_T3U_N11_66        | IO_L24N_T3U_N11_PERSTN0_65                      | IO_L24N_T3U_N11_PERSTN0_65         |
| F7  | IO_L24P_T3U_N10_66        | IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65              | IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65 |
| H1  | IO_L4P_T0U_N6_DBC_AD7P_66 | IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65              | IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65 |

I/O Bank Migration

For differences in bank numbering, refer to [Table 1-7](#) and [Table 1-8](#). All other general migration guidelines and *UltraScale Architecture PCB Design Guide* ([UG583](#)) apply to the SFVD784 and SFVE784 as well.

Table 1-7: I/O Bank Migration (HD Banks are Shaded)

| Package | Device         | Package to Device I/O Mapping <sup>(1)</sup> |    |                   |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | Un          |
|---------|----------------|----------------------------------------------|----|-------------------|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------|
|         |                | A                                            | B  | C                 | D  | E | F | G | H | I | J | K | L | M | N | O | P | Q | R | S | T | U | V | W | X | Y | Z |             |
| SBVA484 | XCZU1<br>XAZU1 | 44                                           | 65 | 66                |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 64          |
|         | XCZU2<br>XAZU2 | 26                                           | 65 | 66 <sup>(2)</sup> |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 25, 24, 44, |
|         | XCZU3<br>XAZU3 | 26                                           | 65 | 66 <sup>(2)</sup> |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 25, 24, 44, |
|         | XQZU3          | 26                                           | 65 | 66 <sup>(2)</sup> |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 25, 24, 44, |
| UBVA494 | XCZU1          | 44                                           | 65 | 66                |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 64          |
| UBVA530 | XCZU2          | 26                                           | 65 | 66 <sup>(2)</sup> |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 25, 24, 44, |
|         | XCZU3          | 26                                           | 65 | 66 <sup>(2)</sup> |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 25, 24, 44, |
| SFVA625 | XCZU1<br>XAZU1 | 64                                           | 65 | 66                | 44 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 25, 24, 44, |
|         | XCZU2<br>XAZU2 | 64                                           | 65 | 66                | 26 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 25, 24, 44  |
|         | XCZU3<br>XAZU3 | 64                                           | 65 | 66                | 26 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 25, 24, 44  |



Table 1-7: I/O Bank Migration (HD Banks are Shaded) (Cont'd)

| Package                | Device         | Package to Device I/O Mapping <sup>(1)</sup> |    |                   |    |    |    |   |   |   |   |   |   |   |    |    |   |   |   |   |   |   |   |   |   |   |   | Un          |
|------------------------|----------------|----------------------------------------------|----|-------------------|----|----|----|---|---|---|---|---|---|---|----|----|---|---|---|---|---|---|---|---|---|---|---|-------------|
|                        |                | A                                            | B  | C                 | D  | E  | F  | G | H | I | J | K | L | M | N  | O  | P | Q | R | S | T | U | V | W | X | Y | Z |             |
| SFVC784                | XCZU1<br>XAZU1 | 64                                           | 65 | 66                |    |    |    |   |   |   |   |   |   |   |    | 44 |   |   |   |   |   |   |   |   |   |   |   |             |
|                        | XCZU2<br>XAZU2 | 64                                           | 65 | 66                | 66 | 25 | 26 |   |   |   |   |   |   |   | 24 | 44 |   |   |   |   |   |   |   |   |   |   |   |             |
|                        | XCZU3<br>XAZU3 | 64                                           | 65 | 66                | 66 | 25 | 26 |   |   |   |   |   |   |   | 24 | 44 |   |   |   |   |   |   |   |   |   |   |   |             |
|                        | XCZU3T         |                                              |    |                   | 66 | 45 | 46 |   |   |   |   |   |   |   | 44 |    |   |   |   |   |   |   |   |   |   |   |   |             |
|                        | XCZU4<br>XAZU4 |                                              | 64 | 65                | 66 | 45 | 46 |   |   |   |   |   |   |   | 44 | 43 |   |   |   |   |   |   |   |   |   |   |   | 63          |
|                        | XCZU5<br>XAZU5 |                                              | 64 | 65                | 66 | 45 | 46 |   |   |   |   |   |   |   | 44 | 43 |   |   |   |   |   |   |   |   |   |   |   | 63          |
|                        | XQZU3          |                                              | 64 | 65                | 66 | 25 | 26 |   |   |   |   |   |   |   | 24 | 44 |   |   |   |   |   |   |   |   |   |   |   |             |
|                        | XQZU5          |                                              | 64 | 65                | 66 | 45 | 46 |   |   |   |   |   |   |   | 44 | 43 |   |   |   |   |   |   |   |   |   |   |   | 63          |
| SFVD784 <sup>(3)</sup> | XCZU3T         |                                              |    |                   | 66 | 45 | 46 |   |   |   |   |   |   |   | 44 |    |   |   |   |   |   |   |   |   |   |   |   |             |
| SFVE784 <sup>(3)</sup> | XCZU4          |                                              | 66 | 65 <sup>(2)</sup> | 45 | 46 |    |   |   |   |   |   |   |   | 43 |    |   |   |   |   |   |   |   |   |   |   |   | 64, 63, 44  |
|                        | XCZU5          |                                              | 66 | 65 <sup>(2)</sup> | 45 | 46 |    |   |   |   |   |   |   |   | 43 |    |   |   |   |   |   |   |   |   |   |   |   | 64, 63, 44  |
| FBVB900                | XCZU4          |                                              | 64 | 65                | 66 |    |    |   |   |   |   |   |   |   | 46 | 45 |   |   |   |   |   |   |   |   |   |   |   | 44, 43, 63  |
|                        | XCZU5          |                                              | 64 | 65                | 66 |    |    |   |   |   |   |   |   |   | 46 | 45 |   |   |   |   |   |   |   |   |   |   |   | 44, 43, 63  |
|                        | XCZU7          |                                              | 64 | 65                | 66 |    |    |   |   |   |   |   |   |   | 47 | 48 |   |   |   |   |   |   |   |   |   |   |   | 28, 27, 68, |
|                        | XAZU7          |                                              | 64 | 65                | 66 |    |    |   |   |   |   |   |   |   | 47 | 48 |   |   |   |   |   |   |   |   |   |   |   | 28, 27, 68, |
| FFRB900                | XQZU5          |                                              | 64 | 65                | 66 |    |    |   |   |   |   |   |   |   | 46 | 45 |   |   |   |   |   |   |   |   |   |   |   | 44, 43, 63  |
|                        | XQZU7          |                                              | 64 | 65                | 66 |    |    |   |   |   |   |   |   |   | 47 | 48 |   |   |   |   |   |   |   |   |   |   |   | 28, 27, 68, |

Table 1-7: I/O Bank Migration (HD Banks are Shaded) (Cont'd)

| Package  | Device | Package to Device I/O Mapping <sup>(1)</sup> |    |    |    |    |    |   |   |   |   |   |   |   |    |    |    |    |    |   |   |   |   |   |   | Un |             |             |
|----------|--------|----------------------------------------------|----|----|----|----|----|---|---|---|---|---|---|---|----|----|----|----|----|---|---|---|---|---|---|----|-------------|-------------|
|          |        | A                                            | B  | C  | D  | E  | F  | G | H | I | J | K | L | M | N  | O  | P  | Q  | R  | S | T | U | V | W | X |    | Y           | Z           |
| FFVC900  | XCZU6  |                                              | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 48 | 47 |    |    |    |   |   |   |   |   |   |    |             | 50, 49, 44, |
|          | XCZU9  |                                              | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 48 | 47 |    |    |    |   |   |   |   |   |   |    | 50, 49, 44, |             |
|          | XCZU15 |                                              | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 48 | 47 |    |    |    |   |   |   |   |   |   |    | 50, 49, 44, |             |
| FFRC900  | XQZU9  |                                              | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 48 | 47 |    |    |    |   |   |   |   |   |   |    | 50, 49, 44, |             |
|          | XQZU15 |                                              | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 48 | 47 |    |    |    |   |   |   |   |   |   |    | 50, 49, 44, |             |
| FFVB1156 | XCZU6  | 44                                           | 64 | 65 | 66 | 67 |    |   |   |   |   |   |   |   | 47 | 48 | 49 | 50 |    |   |   |   |   |   |   |    |             |             |
|          | XCZU9  | 44                                           | 64 | 65 | 66 | 67 |    |   |   |   |   |   |   |   | 47 | 48 | 49 | 50 |    |   |   |   |   |   |   |    |             |             |
|          | XCZU15 | 44                                           | 64 | 65 | 66 | 67 |    |   |   |   |   |   |   |   | 47 | 48 | 49 | 50 |    |   |   |   |   |   |   |    |             |             |
| FFRB1156 | XQZU9  | 44                                           | 64 | 65 | 66 | 67 |    |   |   |   |   |   |   |   | 47 | 48 | 49 | 50 |    |   |   |   |   |   |   |    |             |             |
|          | XQZU15 | 44                                           | 64 | 65 | 66 | 67 |    |   |   |   |   |   |   |   | 47 | 48 | 49 | 50 |    |   |   |   |   |   |   |    |             |             |
| FFVC1156 | XCZU7  |                                              | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 | 88 | 68 | 67 | 28 |   |   |   |   |   |   |    | 27, 48, 47, |             |
|          | XCZU11 |                                              | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 88 | 89 | 69 | 68 | 67 |   |   |   |   |   |   |    | 71, 70, 91, |             |
| FFRC1156 | XQZU7  |                                              | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 | 88 | 68 | 67 | 28 |   |   |   |   |   |   |    | 27, 48, 47, |             |
|          | XQZU11 |                                              | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 88 | 89 | 69 | 68 | 67 |   |   |   |   |   |   |    | 71, 70, 91, |             |
| FFVD1156 | XCZU21 |                                              |    | 65 | 66 | 67 | 68 |   |   |   |   |   |   |   | 87 | 88 | 89 |    |    |   |   |   |   |   |   |    | 71, 70, 69, |             |
| FFRD1156 | XQZU21 |                                              |    | 65 | 66 | 67 | 68 |   |   |   |   |   |   |   | 87 | 88 | 89 |    |    |   |   |   |   |   |   |    | 71, 70, 69, |             |

Table 1-7: I/O Bank Migration (HD Banks are Shaded) (Cont'd)

| Package              | Device | Package to Device I/O Mapping <sup>(1)</sup> |    |    |    |    |    |   |   |   |   |   |   |                   |                   |    |    |    |    |    |    |    |    |    |    | Un |        |             |
|----------------------|--------|----------------------------------------------|----|----|----|----|----|---|---|---|---|---|---|-------------------|-------------------|----|----|----|----|----|----|----|----|----|----|----|--------|-------------|
|                      |        | A                                            | B  | C  | D  | E  | F  | G | H | I | J | K | L | M                 | N                 | O  | P  | Q  | R  | S  | T  | U  | V  | W  | X  |    | Y      | Z           |
| FFVE1156<br>FSVE1156 | XCZU25 |                                              |    | 65 | 66 |    |    |   |   |   |   |   |   |                   | 88                | 89 |    |    |    |    |    |    |    |    |    |    |        | 69, 68, 67, |
|                      | XCZU27 |                                              |    | 65 | 66 |    |    |   |   |   |   |   |   |                   | 88                | 89 |    |    |    |    |    |    |    |    |    |    |        | 71, 70, 69, |
|                      | XCZU28 |                                              |    | 65 | 66 |    |    |   |   |   |   |   |   |                   | 88                | 89 |    |    |    |    |    |    |    |    |    |    |        | 71, 70, 69, |
|                      | XCZU42 |                                              |    | 65 | 66 |    |    |   |   |   |   |   |   |                   | 67 <sup>(2)</sup> | 88 |    |    |    |    |    |    |    |    |    |    |        | 68, 64      |
|                      | XCZU43 |                                              |    | 65 | 66 |    |    |   |   |   |   |   |   |                   | 88                | 89 |    |    |    |    |    |    |    |    |    |    |        | 71, 70, 69, |
|                      | XCZU47 |                                              |    | 65 | 66 |    |    |   |   |   |   |   |   |                   | 88                | 89 |    |    |    |    |    |    |    |    |    |    |        | 71, 70, 69, |
|                      | XCZU48 |                                              |    | 65 | 66 |    |    |   |   |   |   |   |   |                   | 88                | 89 |    |    |    |    |    |    |    |    |    |    |        | 71, 70, 69, |
|                      | XCZU63 |                                              |    | 65 | 66 |    |    |   |   |   |   |   |   |                   | 67 <sup>(2)</sup> | 88 |    |    |    |    |    |    |    |    |    |    |        | 68, 64      |
|                      | XCZU64 |                                              |    | 65 | 66 |    |    |   |   |   |   |   |   |                   | 67 <sup>(2)</sup> | 88 |    |    |    |    |    |    |    |    |    |    |        | 68, 64      |
|                      | XCZU65 |                                              |    | 65 | 66 |    |    |   |   |   |   |   |   |                   | 67 <sup>(2)</sup> | 88 |    |    |    |    |    |    |    |    |    |    |        | 68, 64      |
| XCZU67               |        |                                              | 65 | 66 |    |    |    |   |   |   |   |   |   | 67 <sup>(2)</sup> | 88                |    |    |    |    |    |    |    |    |    |    |    | 68, 64 |             |
| FFRE1156             | XQZU28 |                                              |    | 65 | 66 |    |    |   |   |   |   |   |   |                   | 88                | 89 |    |    |    |    |    |    |    |    |    |    |        | 71, 70, 69, |
|                      | XQZU48 |                                              |    | 65 | 66 |    |    |   |   |   |   |   |   |                   | 88                | 89 |    |    |    |    |    |    |    |    |    |    |        | 71, 70, 69, |
| FFVB1517             | XCZU11 |                                              |    | 65 | 64 | 66 |    |   |   |   |   |   |   |                   | 88                | 89 | 90 |    |    |    | 71 | 70 | 69 | 68 | 67 |    |        | 91          |
|                      | XCZU17 |                                              |    | 65 | 64 | 66 |    |   |   |   |   |   |   |                   | 90                | 91 | 93 | 74 | 73 | 72 | 71 | 70 | 69 | 68 | 67 |    |        | 94          |
|                      | XCZU19 |                                              |    | 65 | 64 | 66 |    |   |   |   |   |   |   |                   | 90                | 91 | 93 | 74 | 73 | 72 | 71 | 70 | 69 | 68 | 67 |    |        | 94          |
|                      | XQZU19 |                                              |    | 65 | 64 | 66 |    |   |   |   |   |   |   |                   | 90                | 91 | 93 | 74 | 73 | 72 | 71 | 70 | 69 | 68 | 67 |    |        | 94          |
| FFVF1517             | XCZU7  |                                              |    | 65 | 66 | 64 | 63 |   |   |   |   |   |   |                   | 87                | 88 | 67 | 68 | 28 | 27 |    |    |    |    |    |    |        | 48, 47      |
|                      | XCZU11 |                                              |    | 65 | 66 | 67 | 64 |   |   |   |   |   |   |                   | 88                | 89 | 70 | 71 | 69 | 68 |    |    |    |    |    |    |        | 91, 90      |
|                      | XAZU11 |                                              |    | 65 | 66 | 67 | 64 |   |   |   |   |   |   |                   | 88                | 89 | 70 | 71 | 69 | 68 |    |    |    |    |    |    |        | 91, 90      |

Table 1-7: I/O Bank Migration (HD Banks are Shaded) (Cont'd)

| Package  | Device                | Package to Device I/O Mapping <sup>(1)</sup> |    |    |    |    |    |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |   |   |   | Un |   |             |             |
|----------|-----------------------|----------------------------------------------|----|----|----|----|----|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|---|---|---|----|---|-------------|-------------|
|          |                       | A                                            | B  | C  | D  | E  | F  | G | H | I | J | K | L | M | N  | O  | P  | Q  | R  | S  | T  | U  | V | W | X |    | Y | Z           |             |
| FFVG1517 | XCZU25                | 84                                           | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 |    |    | 67 | 68 | 69 |    |    |   |   |   |    |   | 89, 88      |             |
|          | XCZU27                | 84                                           | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 |    |    | 67 | 68 | 69 |    |    |   |   |   |    |   | 71, 70, 91, |             |
|          | XCZU28                | 84                                           | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 |    |    | 67 | 68 | 69 |    |    |   |   |   |    |   | 71, 70, 91, |             |
|          | XCZU43                | 84                                           | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 |    |    | 67 | 68 | 69 |    |    |   |   |   |    |   | 71, 70, 91, |             |
| FSVG1517 | XCZU47                | 84                                           | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 |    |    | 67 | 68 | 69 |    |    |   |   |   |    |   | 71, 70, 91, |             |
|          | XCZU48                | 84                                           | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 |    |    | 67 | 68 | 69 |    |    |   |   |   |    |   | 71, 70, 91, |             |
| FFRG1517 | XQZU28                | 84                                           | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 |    |    | 67 | 68 | 69 |    |    |   |   |   |    |   | 71, 70, 91, |             |
| FSRG1517 | XQZU48                | 84                                           | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 |    |    | 67 | 68 | 69 |    |    |   |   |   |    |   | 71, 70, 91, |             |
| FFVC1760 | XCZU11                |                                              |    | 65 | 64 | 66 | 67 |   |   |   |   |   |   |   | 88 | 89 | 90 | 91 | 71 | 70 | 69 | 68 |   |   |   |    |   |             |             |
|          | XCZU17                |                                              |    | 65 | 64 | 66 | 67 |   |   |   |   |   |   |   | 90 | 91 | 93 | 94 | 71 | 70 | 69 | 68 |   |   |   |    |   | 74, 73, 72  |             |
|          | XCZU19                |                                              |    | 65 | 64 | 66 | 67 |   |   |   |   |   |   |   | 90 | 91 | 93 | 94 | 71 | 70 | 69 | 68 |   |   |   |    |   | 74, 73, 72  |             |
| FFRC1760 | XQZU11                |                                              |    | 65 | 64 | 66 | 67 |   |   |   |   |   |   |   | 88 | 89 | 90 | 91 | 71 | 70 | 69 | 68 |   |   |   |    |   |             |             |
|          | XQZU19                |                                              |    | 65 | 64 | 66 | 67 |   |   |   |   |   |   |   | 90 | 91 | 93 | 94 | 71 | 70 | 69 | 68 |   |   |   |    |   | 74, 73, 72  |             |
| FFVD1760 | XCZU17                |                                              |    | 65 | 66 |    |    |   |   |   |   |   |   |   | 90 | 91 | 71 | 70 | 69 |    |    |    |   |   |   |    |   |             | 74, 73, 72, |
|          | XCZU19                |                                              |    | 65 | 66 |    |    |   |   |   |   |   |   |   | 90 | 91 | 71 | 70 | 69 |    |    |    |   |   |   |    |   | 74, 73, 72, |             |
| FFVF1760 | XCZU29                | 84                                           | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 | 88 | 89 |    | 67 | 68 | 69 |    |   |   |   |    |   |             | 71, 70, 91, |
|          | XCZU39                | 84                                           | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 | 88 | 89 |    | 67 | 68 | 69 |    |   |   |   |    |   | 71, 70, 91, |             |
|          | XCZU49 <sup>(1)</sup> | 84                                           | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 | 88 | 89 |    | 67 | 68 | 69 |    |   |   |   |    |   | 71, 70, 91, |             |
| FFRF1760 | XQZU29                | 84                                           | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 | 88 | 89 |    | 67 | 68 | 69 |    |   |   |   |    |   | 71, 70, 91, |             |
| FSRF1760 | XQZU49                | 84                                           | 64 | 65 | 66 |    |    |   |   |   |   |   |   |   | 87 | 88 | 89 |    | 67 | 68 | 69 |    |   |   |   |    |   | 71, 70, 91, |             |
| FFVH1760 | XCZU46                |                                              |    | 64 | 65 | 66 |    |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |   |   |   |    |   |             | 67, 68, 84, |
| FSVH1760 |                       |                                              |    |    |    |    |    |   |   |   |   |   |   |   |    |    | 90 | 91 |    | 69 | 71 | 70 |   |   |   |    |   |             |             |

Table 1-7: I/O Bank Migration (HD Banks are Shaded) (Cont'd)

| Package  | Device | Package to Device I/O Mapping <sup>(1)</sup> |    |    |    |    |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |   |   | Un |
|----------|--------|----------------------------------------------|----|----|----|----|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|---|---|----|
|          |        | A                                            | B  | C  | D  | E  | F | G | H | I | J | K | L | M | N  | O  | P  | Q  | R  | S  | T  | U  | V  | W  | X  | Y | Z |    |
| FFVE1924 | XCZU17 |                                              | 65 | 64 | 66 | 67 |   |   |   |   |   |   |   |   | 90 | 91 | 93 | 94 | 74 | 73 | 72 | 71 | 70 | 69 | 68 |   |   |    |
|          | XCZU19 |                                              | 65 | 64 | 66 | 67 |   |   |   |   |   |   |   |   | 90 | 91 | 93 | 94 | 74 | 73 | 72 | 71 | 70 | 69 | 68 |   |   |    |

Notes:

1. An alphabetical designator, A through Z, is assigned to every bank in a package. I/Os from banks with the same designator are bonded out in the same package. For example, in the FFVF1517 package, the E designator is assigned to bank 67 for the XCZU11 and bank 64 for the XCZU7. These pins, regardless of where they appear on the XCZU11 and XCZU7 device.
2. Bank 66 is partially bonded out in the SBVA484 package (see [Figure 1-10](#)). Bank 67 is partially bonded out in the FFVE1156 and FSVE1156 packages (see [Figure 1-55](#), [Figure 1-74](#), and [Figure 1-76](#)).
3. Migration between the SFVD784 and SFVE784 is possible by following the guidelines in the [Migration Between SFVD784 and SFVE784 Package](#).

For each grouped set of footprint compatible packages listed in [Table 1-8](#), there is a row detailing the each Quad. These groups are labeled according to the regions for the transceiver power supply pins, [Pinout Files](#) linked from [Chapter 3, Package Files](#). For a visual representation of all of this information [Numbering Overview](#) section.

## Package to Die Transceiver Mapping<sup>(1)</sup>

## Unborn

Table 1-8: Transceiver Quad Migration (GTY Quads are in Shaded) (Cont'd)

| Package                | Device             | Package to Die Transceiver Mapping <sup>(1)</sup> |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   | Unbonded |               |               |     |               |
|------------------------|--------------------|---------------------------------------------------|-----|-----|-----|---|---|---|---|---|---|---|---|---|---|---|---|----------|---------------|---------------|-----|---------------|
|                        |                    | A                                                 | B   | C   | D   | E | F | G | H | I | J | K | L | M | N | O | P |          | Q             | R             | S-Z | AA-AF         |
| Power Supply Group     |                    | R                                                 |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
| SFVC784                | XCZU1              |                                                   |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
|                        | XAZU1              |                                                   |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
|                        | XCZU2              |                                                   |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
|                        | XAZU2              |                                                   |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
|                        | XCZU3              |                                                   |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
|                        | XAZU3              |                                                   |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
|                        | XCZU3T             | 224                                               |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
|                        | XCZU4              |                                                   |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
| XAZU4                  | 224                |                                                   |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
| XCZU5                  |                    |                                                   |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
| XAZU5                  | 224                |                                                   |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
| SFRC784                | XQZU3              |                                                   |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   | 225      |               |               |     |               |
|                        | XQZU5              |                                                   |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   | 224      | 226, 225, 223 |               |     |               |
| SFVD784                | XCZU3T             | 224                                               | 225 |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               | 226, 225, 223 |     |               |
| Power Supply Group     |                    | R                                                 |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
| SFVE784 <sup>(2)</sup> | XCZU4              | 223                                               | 224 |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               | 226, 225      |     |               |
|                        | XCZU5              | 223                                               | 224 |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               | 226, 225      |     |               |
| Power Supply Group     |                    | R                                                 |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
| FBVB900                | XCZU4              | 223                                               | 224 | 225 | 226 |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
|                        | XCZU5              | 223                                               | 224 | 225 | 226 |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
|                        | XCZU7              | 224                                               | 225 | 226 | 227 |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     | 228, 223      |
|                        | XAZU7              | 224                                               | 225 | 226 | 227 |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     | 228, 223      |
| FFRB900                | XQZU5              | 223                                               | 224 | 225 | 226 |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
|                        | XQZU7              | 224                                               | 225 | 226 | 227 |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     | 228, 223      |
|                        | Power Supply Group |                                                   | R   |     |     |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     |               |
| FFVC900                | XCZU6              | 228                                               | 229 | 230 | 128 |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     | 130, 129, 127 |
|                        | XCZU9              | 228                                               | 229 | 230 | 128 |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     | 130, 129, 127 |
|                        | XCZU15             | 228                                               | 229 | 230 | 128 |   |   |   |   |   |   |   |   |   |   |   |   |          |               |               |     | 130, 129, 127 |

Table 1-8: Transceiver Quad Migration (GTY Quads are in Shaded) (Cont'd)

| Package            | Device | Package to Die Transceiver Mapping <sup>(1)</sup> |     |     |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |     | Unbonded                     |       |
|--------------------|--------|---------------------------------------------------|-----|-----|-----|-----|-----|---|---|---|---|---|---|---|---|---|---|---|---|-----|------------------------------|-------|
|                    |        | A                                                 | B   | C   | D   | E   | F   | G | H | I | J | K | L | M | N | O | P | Q | R | S-Z |                              | AA-AF |
| FFRC900            | XQZU9  | 228                                               | 229 | 230 | 128 |     |     |   |   |   |   |   |   |   |   |   |   |   |   |     | 130, 129, 127                |       |
|                    | XQZU15 | 228                                               | 229 | 230 | 128 |     |     |   |   |   |   |   |   |   |   |   |   |   |   |     | 130, 129, 127                |       |
| Power Supply Group |        | R                                                 |     |     |     | L   |     |   |   |   |   |   |   |   |   |   |   |   |   |     |                              |       |
| FFVB1156           | XCZU6  | 228                                               | 229 | 230 | 128 | 129 | 130 |   |   |   |   |   |   |   |   |   |   |   |   |     |                              | 127   |
|                    | XCZU9  | 228                                               | 229 | 230 | 128 | 129 | 130 |   |   |   |   |   |   |   |   |   |   |   |   |     |                              | 127   |
|                    | XCZU15 | 228                                               | 229 | 230 | 128 | 129 | 130 |   |   |   |   |   |   |   |   |   |   |   |   |     |                              | 127   |
| FFRB1156           | XQZU9  | 228                                               | 229 | 230 | 128 | 129 | 130 |   |   |   |   |   |   |   |   |   |   |   |   |     |                              | 127   |
|                    | XQZU15 | 228                                               | 229 | 230 | 128 | 129 | 130 |   |   |   |   |   |   |   |   |   |   |   |   |     |                              | 127   |
| Power Supply Group |        | R                                                 |     |     |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |     |                              |       |
| FFVC1156           | XCZU7  | 223                                               | 224 | 225 | 226 | 227 |     |   |   |   |   |   |   |   |   |   |   |   |   |     | 228                          |       |
|                    | XCZU11 | 224                                               | 225 | 226 | 227 | 228 |     |   |   |   |   |   |   |   |   |   |   |   |   |     | 131, 130, 129, 128, 127, 228 |       |
| FFRC1156           | XQZU7  | 223                                               | 224 | 225 | 226 | 227 |     |   |   |   |   |   |   |   |   |   |   |   |   |     | 228                          |       |
|                    | XQZU11 | 224                                               | 225 | 226 | 227 | 228 |     |   |   |   |   |   |   |   |   |   |   |   |   |     | 131, 130, 129, 128, 127, 228 |       |
| Power Supply Group |        | L                                                 |     |     |     |     |     |   |   |   |   |   |   |   |   |   |   |   |   |     |                              |       |
| FFVD1156           | XCZU21 | 128                                               | 129 | 130 | 131 |     |     |   |   |   |   |   |   |   |   |   |   |   |   | 127 |                              |       |
| FFRD1156           | XQZU21 | 128                                               | 129 | 130 | 131 |     |     |   |   |   |   |   |   |   |   |   |   |   |   | 127 |                              |       |





Table 1-8: Transceiver Quad Migration (GTY Quads are in Shaded) (Cont’d)

| Package              | Device | Package to Die Transceiver Mapping <sup>(1)</sup> |     |     |     |     |     |   |   |   |   |   |   |   |   |   |   | Unbonded |   |               |     |                                             |     |
|----------------------|--------|---------------------------------------------------|-----|-----|-----|-----|-----|---|---|---|---|---|---|---|---|---|---|----------|---|---------------|-----|---------------------------------------------|-----|
|                      |        | A                                                 | B   | C   | D   | E   | F   | G | H | I | J | K | L | M | N | O | P |          | Q | R             | S-Z | AA-AF                                       |     |
| Power Supply Group   |        | L                                                 |     |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   |               |     |                                             |     |
| FFVE1156<br>FSVE1156 | XCZU25 | 128                                               | 129 |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   | 127           |     |                                             |     |
|                      | XCZU27 | 128                                               | 129 |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   | 131, 130, 127 |     |                                             |     |
|                      | XCZU28 | 128                                               | 129 |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   | 131, 130, 127 |     |                                             |     |
|                      | XCZU42 | 127                                               | 128 |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   |               |     |                                             |     |
|                      | XCZU43 | 128                                               | 129 |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   | 131, 130, 127 |     |                                             |     |
|                      | XCZU47 | 128                                               | 129 |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   | 131, 130, 127 |     |                                             |     |
|                      | XCZU48 | 128                                               | 129 |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   | 131, 130, 127 |     |                                             |     |
|                      | XCZU63 | 127                                               |     |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   | 128           |     |                                             |     |
|                      | XCZU64 | 127                                               | 128 |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   |               |     |                                             |     |
|                      | XCZU65 | 127                                               | 128 |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   |               |     |                                             |     |
| FFRE1156             | XCZU67 | 127                                               | 128 |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   |               |     |                                             |     |
|                      | XQZU28 | 128                                               | 129 |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   | 131, 130, 127 |     |                                             |     |
|                      | XQZU48 | 128                                               | 129 |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   | 131, 130, 127 |     |                                             |     |
| Power Supply Group   |        | R                                                 |     |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   |               |     |                                             |     |
| FFVB1517             | XCZU11 | 224                                               | 225 | 226 | 227 |     |     |   |   |   |   |   |   |   |   |   |   |          |   |               |     | 131, 130, 129, 128, 127, 230, 229, 228      |     |
|                      | XCZU17 | 224                                               | 225 | 226 | 227 |     |     |   |   |   |   |   |   |   |   |   |   |          |   |               |     | 134, 133, 132, 131, 130, 129, 230, 229, 228 |     |
|                      | XCZU19 | 224                                               | 225 | 226 | 227 |     |     |   |   |   |   |   |   |   |   |   |   |          |   |               |     | 134, 133, 132, 131, 130, 129, 230, 229, 228 |     |
|                      | XAZU11 | 224                                               | 225 | 226 | 227 |     |     |   |   |   |   |   |   |   |   |   |   |          |   |               |     | 131, 130, 129, 128, 127, 230, 229, 228      |     |
| FFRB1517             | XQZU19 | 224                                               | 225 | 226 | 227 |     |     |   |   |   |   |   |   |   |   |   |   |          |   |               |     | 134, 133, 132, 131, 130, 129, 230, 229, 228 |     |
| Power Supply Group   |        | RS                                                |     |     |     |     |     |   |   |   |   |   |   |   |   |   |   |          |   |               |     | RN                                          |     |
| FFVF1517             | XCZU7  | 223                                               | 224 | 225 | 226 | 227 | 228 |   |   |   |   |   |   |   |   |   |   |          |   |               |     |                                             |     |
|                      | XCZU11 | 224                                               | 225 | 226 | 227 | 228 | 229 |   |   |   |   |   |   |   |   |   |   |          |   |               |     |                                             | 230 |

Table 1-8: Transceiver Quad Migration (GTY Quads are in Shaded) (Cont’d)

| Package              | Device | Package to Die Transceiver Mapping <sup>(1)</sup> |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | Unbonded                     |
|----------------------|--------|---------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|--|------------------------------|
| Power Supply Group   |        | L                                                 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  |                              |
| FFVG1517<br>FSVG1517 | XCZU25 | 128                                               | 129 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | 127                          |
|                      | XCZU27 | 128                                               | 129 | 130 | 131 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | 127                          |
|                      | XCZU28 | 128                                               | 129 | 130 | 131 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | 127                          |
|                      | XCZU43 | 128                                               | 129 | 130 | 131 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | 127                          |
| FFRG1517<br>FSRG1517 | XCZU47 | 128                                               | 129 | 130 | 131 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | 127                          |
|                      | XCZU48 | 128                                               | 129 | 130 | 131 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | 127                          |
|                      | XQZU28 | 128                                               | 129 | 130 | 131 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | 127                          |
|                      | XQZU48 | 128                                               | 129 | 130 | 131 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | 127                          |
| Power Supply Group   |        | RS                                                |     |     |     | RN  |     |     |     | L   |     |     |     |     |     |     |     |     |     |  |                              |
| FFVC1760             | XCZU11 | 224                                               | 225 | 226 | 227 | 228 | 229 | 230 | 231 | 128 | 129 | 130 | 131 |     |     |     |     |     |     |  | 127                          |
|                      | XCZU17 | 224                                               | 225 | 226 | 227 | 228 | 229 | 230 | 231 | 128 | 129 | 130 | 131 |     |     |     |     |     |     |  | 127                          |
|                      | XCZU19 | 224                                               | 225 | 226 | 227 | 228 | 229 | 230 | 231 | 128 | 129 | 130 | 131 |     |     |     |     |     |     |  | 134, 133, 132, 127, 234, 233 |
| FFRC1760             | XQZU11 | 224                                               | 225 | 226 | 227 | 228 | 229 | 230 | 231 | 128 | 129 | 130 | 131 |     |     |     |     |     |     |  | 127                          |
|                      | XQZU19 | 224                                               | 225 | 226 | 227 | 228 | 229 | 230 | 231 | 128 | 129 | 130 | 131 |     |     |     |     |     |     |  | 134, 133, 132, 127, 234, 233 |
| Power Supply Group   |        | RS                                                |     |     |     | RN  |     |     |     | L   |     |     |     |     |     |     |     |     |     |  |                              |
| FFVD1760             | XCZU17 | 224                                               | 225 | 226 | 227 | 228 | 229 | 230 | 231 | 232 | 233 | 234 | 128 | 129 | 130 | 131 | 132 | 133 | 134 |  | 127                          |
|                      | XCZU19 | 224                                               | 225 | 226 | 227 | 228 | 229 | 230 | 231 | 232 | 233 | 234 | 128 | 129 | 130 | 131 | 132 | 133 | 134 |  | 127                          |
| Power Supply Group   |        | L                                                 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  |                              |
| FFVF1760<br>FSVF1760 | XCZU29 | 128                                               | 129 | 130 | 131 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | 127                          |
|                      | XCZU39 | 128                                               | 129 | 130 | 131 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | 127                          |
|                      | XCZU49 | 128                                               | 129 | 130 | 131 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | 127                          |
| FFVH1760<br>FSVH1760 | XCZU46 | 128                                               | 129 | 130 | 131 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | 127                          |
|                      | XQZU29 | 128                                               | 129 | 130 | 131 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | 127                          |
| FFRF1760<br>FSRF1760 | XQZU49 | 128                                               | 129 | 130 | 131 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |  | 127                          |

Table 1-8: Transceiver Quad Migration (GTY Quads are in Shaded) (Cont'd)

| Package            | Device | Package to Die Transceiver Mapping <sup>(1)</sup> |     |     |     |     |     |     |     |     |     |     |   |   |   |   |   |   |   |     |                              | Unbonded |
|--------------------|--------|---------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|---|---|---|---|---|---|-----|------------------------------|----------|
|                    |        | A                                                 | B   | C   | D   | E   | F   | G   | H   | I   | J   | K   | L | M | N | O | P | Q | R | S-Z | AA-AF                        |          |
| Power Supply Group |        | RS                                                |     |     |     |     |     | RN  |     |     |     |     |   |   |   |   |   |   |   |     |                              |          |
| FFVE1924           | XCZU17 | 224                                               | 225 | 226 | 227 | 228 | 229 | 230 | 231 | 232 | 233 | 234 |   |   |   |   |   |   |   |     | 134, 133, 132, 131, 130, 129 |          |
|                    | XCZU19 | 224                                               | 225 | 226 | 227 | 228 | 229 | 230 | 231 | 232 | 233 | 234 |   |   |   |   |   |   |   |     | 134, 133, 132, 131, 130, 129 |          |

Notes:

- 1. An alphabetical designator, A through Z, is assigned to every Quad in a package. Transceivers from Quads with the same designator are bonded to the same pins in that package. For example, in the FFVF1517 package, the E designator is assigned to Quad 228 for the XCZU11 and Quad 227 for the XCZU7 device. The same pins, regardless of where they appear on the XCZU11 and XCZU7 device.
- 2. Migration between the SFVD784 and SFVE784 is possible by following the guidelines in the [Migration Between SFVD784 and SFVE784 Package](#).

# Die Level Bank Numbering Overview

## *Banking and Clocking Summary*

- For each device, not all banks are bonded out in every package.

## *GTH/GTY Columns*

- One GT Quad = Four transceivers = Four GTHE4 or GTYE4 primitives.
- Not all GT Quads are bonded out in every package.
- Also shown are quads labeled with RCAL. This specifies the location of the RCAL masters for each device. With respect to the package, the RCAL masters are located on the same package pin for each package, regardless of the device.
- The XY coordinates shown in each quad correspond to the transceiver channel number found in the pin names for that quad, as shown in [Figure 1-9](#).
- An alphabetic designator is shown in each quad. Each letter corresponds to the columns in [Table 1-7](#) and [Table 1-8](#).
- The power supply group is shown in brackets [ ] for each quad.

## *I/O Banks*

- Each user HP I/O bank has a total of 52 I/Os where 48 can be used as differential (24 differential pairs) or single-ended I/Os. The remaining four function only as single-ended I/Os. All 52 pads of a bank are not always bonded out to pins.
- A limited number of HP I/O banks have fewer than 52 SelectIO pins. These banks are labeled as partial.
- Each user HD I/O bank has a total of 24 I/Os that can be used as differential (12 differential pairs) or single-ended I/Os.
- Adjacent to each bank is a physical layer (PHY) containing a CMT and other clock resources.
- Adjacent to each bank and PHY is a tile of logic resources that makes up a clock region.
- Banks are arranged in columns and separated into rows which are pitch-matched with adjacent PHY, clock regions, and GT blocks.
- An alphabetic designator is shown in each bank. Each letter corresponds to the columns in [Table 1-7](#) and [Table 1-8](#).

### ***Clocking***

- Each bank has four pairs of global clock (GC or HDGC) inputs for four differential or four single-ended clock inputs. Single-ended clock inputs should be connected to the P-side of the differential pair.
- Clock signals are distributed through global buffers driving routing and distribution networks to reach any clock region, I/O, or GT.
- Global clock inputs can connect to an MMCM and two PLLs within the horizontally adjacent CMT.

### ***Bank Locations of Dedicated and Multi-Function Pins***

- All dedicated configuration I/Os and HD I/Os are 3.3V capable.

### ***Processor (PS) Blocks***

- MIO pins are shared between banks 500, 501, and 502.
- Configuration pins are in bank 503.
- DDR memory pins are in bank 504.
- Transceiver pins are in the PS-GTR quad 505.

### ***SYSMON, Configuration, PCIe, Interlaken, and 100GE Integrated Blocks***

- Configuration: Configuration block.
- SYSMON/Configuration: Block shared between the SYSMONE4 and configuration.
- PCIe: Integrated block for PCIe.  
**Note:** PCIe blocks with an additional (Tandem) label support tandem configuration.
- ILKN: Interlaken block.
- CMAC: 100G Ethernet block.

Device Diagrams

Figure 1-3 shows an example diagram with a brief explanation for each component.

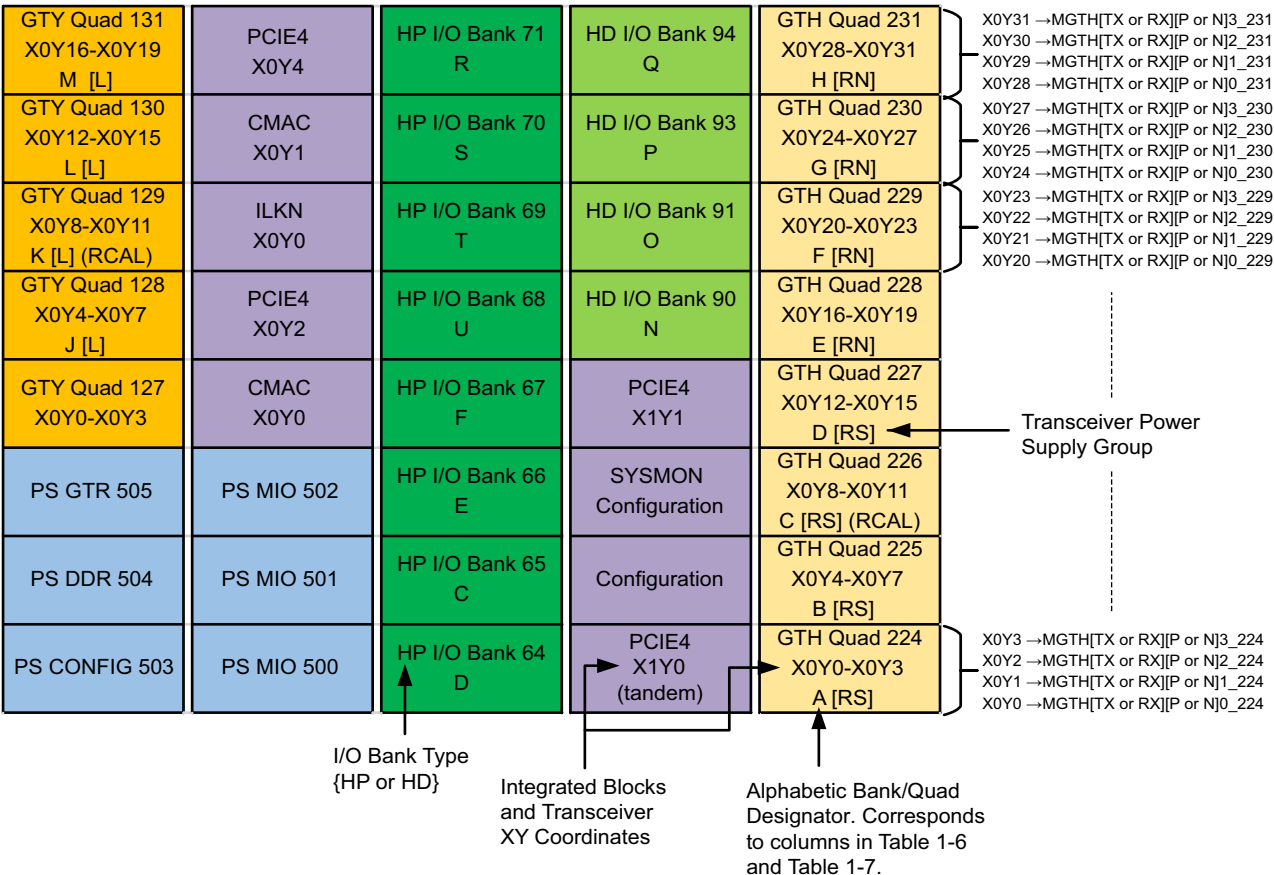


Figure 1-3: Example Device Diagram

Figure 1-4 through Figure 1-76 show a die view of each device followed by a view with respect to each available package. The available resources by device and package are detailed in the Zynq UltraScale+ MPSoC Overview (DS891) or Zynq UltraScale+ RFSoc Overview (DS889).

## XCZU1 Bank Diagram Overview

|               |            |                      |                |
|---------------|------------|----------------------|----------------|
| PS GTR 505    | PS MIO 502 | SYSMON Configuration | HP I/O Bank 66 |
| PS DDR 504    | PS MIO 501 | Configuration        | HP I/O Bank 65 |
| PS CONFIG 503 | PS MIO 500 | HD I/O Bank 44       | HP I/O Bank 64 |

X26100-121921

Figure 1-4: XCZU1 Banks

### Bank Diagram by Package for XCZU1

|                      |            |                      |                            |
|----------------------|------------|----------------------|----------------------------|
| PS GTR 505           | PS MIO 502 | SYSMON Configuration | HP I/O Bank 66 D (Partial) |
| PS DDR 504 (Partial) | PS MIO 501 | Configuration        | HP I/O Bank 65 C           |
| PS CONFIG 503        | PS MIO 500 | HD I/O Bank 44 E     | HP I/O Bank 64             |

X26102-121921

Figure 1-5: XCZU1 Banks in SBVA484 Package

|                      |            |                      |                            |
|----------------------|------------|----------------------|----------------------------|
| PS GTR 505           | PS MIO 502 | SYSMON Configuration | HP I/O Bank 66 D (Partial) |
| PS DDR 504 (Partial) | PS MIO 501 | Configuration        | HP I/O Bank 65 C           |
| PS CONFIG 503        | PS MIO 500 | HD I/O Bank 44       | HP I/O Bank 64             |

X26101-121921

Figure 1-6: XCZU1 Banks in UBVA494 Package



**IMPORTANT:** For the devices in the UBVA494 package shown in [Figure 1-6](#), the HP I/Os in bank 66 are powered by VCCO\_65.

|                      |            |                      |                  |
|----------------------|------------|----------------------|------------------|
| PS GTR 505           | PS MIO 502 | SYSMON Configuration | HP I/O Bank 66 D |
| PS DDR 504 (Partial) | PS MIO 501 | Configuration        | HP I/O Bank 65 C |
| PS CONFIG 503        | PS MIO 500 | HD I/O Bank 44 E     | HP I/O Bank 64 B |

X26103-121921

Figure 1-7: XCZU1 Banks in SBVA625 Package

|               |            |                      |                  |
|---------------|------------|----------------------|------------------|
| PS GTR 505    | PS MIO 502 | SYSMON Configuration | HP I/O Bank 66 D |
| PS DDR 504    | PS MIO 501 | Configuration        | HP I/O Bank 65 C |
| PS CONFIG 503 | PS MIO 500 | HD I/O Bank 44 O     | HP I/O Bank 64 B |

X26104-121921

Figure 1-8: XCZU1 Banks in SFVC784 Package



## XCZU2, XAZU2, XCZU3, XAZU3, and XQZU3 Bank Diagram Overview

|               |            |                |                      |                |
|---------------|------------|----------------|----------------------|----------------|
| PS GTR 505    | PS MIO 502 | HD I/O Bank 26 | SYSMON Configuration | HP I/O Bank 66 |
| PS DDR 504    | PS MIO 501 | HD I/O Bank 25 | Configuration        | HP I/O Bank 65 |
| PS CONFIG 503 | PS MIO 500 | HD I/O Bank 24 | HD I/O Bank 44       | HP I/O Bank 64 |

X15118-060720

Figure 1-9: XCZU2, XAZU2, XCZU3, XAZU3, and XQZU3 Banks

### Bank Diagram by Package for XCZU2, XAZU2, XCZU3, XAZU3, and XQZU3

|                      |            |                  |                      |                                    |
|----------------------|------------|------------------|----------------------|------------------------------------|
| PS GTR 505           | PS MIO 502 | HD I/O Bank 26 B | SYSMON Configuration | HP I/O Bank 66 D (Partial) VCCO_65 |
| PS DDR 504 (Partial) | PS MIO 501 | HD I/O Bank 25   | Configuration        | HP I/O Bank 65 C                   |
| PS CONFIG 503        | PS MIO 500 | HD I/O Bank 24   | HD I/O Bank 44       | HP I/O Bank 64                     |

X15119-082224

Figure 1-10: XCZU2, XAZU2, XCZU3, and XAZU3 Banks in SBVA484 Package



**IMPORTANT:** For the devices in the SBVA484 package shown in [Figure 1-10](#), the HP I/Os in bank 66 are powered by VCCO\_65.

|                         |            |                     |                         |                                          |
|-------------------------|------------|---------------------|-------------------------|------------------------------------------|
| PS GTR 505              | PS MIO 502 | HD I/O Bank 26<br>B | SYSMON<br>Configuration | HP I/O Bank 66<br>D (Partial)<br>VCCO_65 |
| PS DDR 504<br>(Partial) | PS MIO 501 | HD I/O Bank 25      | Configuration           | HP I/O Bank 65<br>C                      |
| PS CONFIG 503           | PS MIO 500 | HD I/O Bank 24      | HD I/O Bank 44          | HP I/O Bank 64                           |

X25451-082224

Figure 1-11: XCZU2 and XCZU3 Banks in UBVA530 Package



**IMPORTANT:** For the devices in the UBVA530 package shown in Figure 1-11, the HP I/Os in bank 66 are powered by VCCO\_65.

|                         |            |                     |                         |                     |
|-------------------------|------------|---------------------|-------------------------|---------------------|
| PS GTR 505              | PS MIO 502 | HD I/O Bank 26<br>E | SYSMON<br>Configuration | HP I/O Bank 66<br>D |
| PS DDR 504<br>(Partial) | PS MIO 501 | HD I/O Bank 25      | Configuration           | HP I/O Bank 65<br>C |
| PS CONFIG 503           | PS MIO 500 | HD I/O Bank 24      | HD I/O Bank 44          | HP I/O Bank 64<br>B |

X15120-060720

Figure 1-12: XCZU2, XAZU2, XCZU3, and XAZU3 Banks in SFVA625 Package

|               |            |                     |                         |                     |
|---------------|------------|---------------------|-------------------------|---------------------|
| PS GTR 505    | PS MIO 502 | HD I/O Bank 26<br>F | SYSMON<br>Configuration | HP I/O Bank 66<br>D |
| PS DDR 504    | PS MIO 501 | HD I/O Bank 25<br>E | Configuration           | HP I/O Bank 65<br>C |
| PS CONFIG 503 | PS MIO 500 | HD I/O Bank 24<br>N | HD I/O Bank 44<br>O     | HP I/O Bank 64<br>B |

X15121-060720

Figure 1-13: XCZU2, XAZU2, XCZU3, XAZU3, and XQZU3 Banks in SFVC784 Package

## XCZU3T Bank Diagram Overview

|               |            |                |                      |                               |
|---------------|------------|----------------|----------------------|-------------------------------|
| PS GTR 505    | PS MIO 502 | HD I/O Bank 46 | SYSMON Configuration | HP I/O Bank 66                |
| PS DDR 504    | PS MIO 501 | HD I/O Bank 45 | Configuration        | GTH Quad 225 X0Y4-X0Y7        |
| PS CONFIG 503 | PS MIO 500 | HD I/O Bank 44 | PCIE4 X0Y0           | GTH Quad 224 X0Y0-X0Y3 (RCAL) |

X27739-020723

Figure 1-14: XCZU3T Banks

### Bank Diagram by Package for XCZU3T

|               |            |                  |                      |                                     |
|---------------|------------|------------------|----------------------|-------------------------------------|
| PS GTR 505    | PS MIO 502 | HD I/O Bank 46 F | SYSMON Configuration | HP I/O Bank 66 D                    |
| PS DDR 504    | PS MIO 501 | HD I/O Bank 45 E | Configuration        | GTH Quad 225 X0Y4-X0Y7              |
| PS CONFIG 503 | PS MIO 500 | HD I/O Bank 44 N | PCIE4 X0Y0           | GTH Quad 224 X0Y0-X0Y3 A [R] (RCAL) |

X27740-020723

Figure 1-15: XCZU3T Banks in SFVC784 Package

|               |            |                  |                      |                                     |
|---------------|------------|------------------|----------------------|-------------------------------------|
| PS GTR 505    | PS MIO 502 | HD I/O Bank 46 F | SYSMON Configuration | HP I/O Bank 66 D                    |
| PS DDR 504    | PS MIO 501 | HD I/O Bank 45 E | Configuration        | GTH Quad 225 X0Y4-X0Y7 B [R]        |
| PS CONFIG 503 | PS MIO 500 | HD I/O Bank 44 N | PCIE4 X0Y0           | GTH Quad 224 X0Y0-X0Y3 A [R] (RCAL) |

X27741-020723

Figure 1-16: XCZU3T Banks in SFVD784 Package

**Note:** Migration between the SFVD784 and SFVE784 is possible by following the guidelines in [Migration Between SFVD784 and SFVE784 Packages, page 34](#).

## XCZU4, XAZU4, XCZU5, XAZU5, and XQZU5 Bank Diagram Overview

|               |            |                |                |                      |                               |
|---------------|------------|----------------|----------------|----------------------|-------------------------------|
| PS GTR 505    | PS MIO 502 | HD I/O Bank 46 | HP I/O Bank 66 | SYSMON Configuration | GTH Quad 226 X0Y12-X0Y15      |
| PS DDR 504    | PS MIO 501 | HD I/O Bank 45 | HP I/O Bank 65 | Configuration        | GTH Quad 225 X0Y8-X0Y11       |
| PS CONFIG 503 | PS MIO 500 | HD I/O Bank 44 | HP I/O Bank 64 | PCIE4 X0Y1 (tandem)  | GTH Quad 224 X0Y4-X0Y7 (RCAL) |
|               |            | HD I/O Bank 43 | HP I/O Bank 63 | PCIE4 X0Y0           | GTH Quad 223 X0Y0-X0Y3        |

X15122-060720

Figure 1-17: XCZU4, XAZU4, XCZU5, XAZU5, and XQZU5 Banks

### Bank Diagram by Package for XCZU4, XAZU4EV, XCZU5, XAZU5EV, and XQZU5

|               |            |                  |                  |                      |                                     |
|---------------|------------|------------------|------------------|----------------------|-------------------------------------|
| PS GTR 505    | PS MIO 502 | HD I/O Bank 46 F | HP I/O Bank 66 D | SYSMON Configuration | GTH Quad 226 X0Y12-X0Y15            |
| PS DDR 504    | PS MIO 501 | HD I/O Bank 45 E | HP I/O Bank 65 C | Configuration        | GTH Quad 225 X0Y8-X0Y11             |
| PS CONFIG 503 | PS MIO 500 | HD I/O Bank 44 N | HP I/O Bank 64 B | PCIE4 X0Y1 (tandem)  | GTH Quad 224 X0Y4-X0Y7 A [R] (RCAL) |
|               |            | HD I/O Bank 43 O | HP I/O Bank 63   | PCIE4 X0Y0           | GTH Quad 223 X0Y0-X0Y3              |

X15124-111316

Figure 1-18: XCZU4, XAZU4EV, XCZU5, and XAZU5EV Banks in SFVC784 Package and XQZU5 Banks in SFRC784 Package

**Note:** Migration between the SFVD784 and SFVE784 is possible by following the guidelines in [Migration Between SFVD784 and SFVE784 Packages, page 34](#).

|               |            |                     |                                          |                         |                                           |
|---------------|------------|---------------------|------------------------------------------|-------------------------|-------------------------------------------|
| PS GTR 505    | PS MIO 502 | HD I/O Bank 46<br>F | HP I/O Bank 66<br>C (Partial)<br>VCCO_65 | SYSMON<br>Configuration | GTH Quad 226<br>X0Y12-X0Y15               |
| PS DDR 504    | PS MIO 501 | HD I/O Bank 45<br>E | HP I/O Bank 65<br>D                      | Configuration           | GTH Quad 225<br>X0Y8-X0Y11                |
| PS CONFIG 503 | PS MIO 500 | HD I/O Bank 44      | HP I/O Bank 64                           | PCIE4_CFG_424<br>X0Y1   | GTH Quad 224<br>X0Y4-X0Y7<br>B [R] (RCAL) |
|               |            | HD I/O Bank 43<br>N | HP I/O Bank 63                           | PCIE4_423<br>X0Y0       | GTH Quad 223<br>X0Y0-X0Y3<br>A [R]        |

X29471-082224

Figure 1-19: XCZU4, XAZU4EV, XCZU5, and XAZU5EV Banks in SFVE784 Package

Migration between the SFVD784 and SFVE784 is possible by following the guidelines in the [Migration Between SFVD784 and SFVE784 Packages](#) section.

|               |            |                     |                     |                         |                                           |
|---------------|------------|---------------------|---------------------|-------------------------|-------------------------------------------|
| PS GTR 505    | PS MIO 502 | HD I/O Bank 46<br>N | HP I/O Bank 66<br>D | SYSMON<br>Configuration | GTH Quad 226<br>X0Y12-X0Y15<br>D [R]      |
| PS DDR 504    | PS MIO 501 | HD I/O Bank 45<br>O | HP I/O Bank 65<br>C | Configuration           | GTH Quad 225<br>X0Y8-X0Y11<br>C [R]       |
| PS CONFIG 503 | PS MIO 500 | HD I/O Bank 44      | HP I/O Bank 64<br>B | PCIE4<br>X0Y1           | GTH Quad 224<br>X0Y4-X0Y7<br>B [R] (RCAL) |
|               |            | HD I/O Bank 43      | HP I/O Bank 63      | PCIE4<br>X0Y0           | GTH Quad 223<br>X0Y0-X0Y3<br>A [R]        |

X15123-112916

Figure 1-20: XCZU4 and XCZU5 Banks in FBVB900 Package and XQZU5 Banks in FFRB900 Package

## XCZU7, XAZU7, and XQZU7 Bank Diagram Overview

|                |                |                |                           |                                     |
|----------------|----------------|----------------|---------------------------|-------------------------------------|
| HP I/O Bank 28 | HD I/O Bank 48 | HP I/O Bank 68 | HD I/O Bank 88            | GTH Quad 228<br>X0Y20-X0Y23         |
| HP I/O Bank 27 | HD I/O Bank 47 | HP I/O Bank 67 | HD I/O Bank 87            | GTH Quad 227<br>X0Y16-X0Y19         |
| PS GTR 505     | PS MIO 502     | HP I/O Bank 66 | SYSMON<br>Configuration   | GTH Quad 226<br>X0Y12-X0Y15         |
| PS DDR 504     | PS MIO 501     | HP I/O Bank 65 | Configuration             | GTH Quad 225<br>X0Y8-X0Y11          |
| PS CONFIG 503  | PS MIO 500     | HP I/O Bank 64 | PCIE4<br>X0Y1<br>(tandem) | GTH Quad 224<br>X0Y4-X0Y7<br>(RCAL) |
|                |                | HP I/O Bank 63 | PCIE4<br>X0Y0             | GTH Quad 223<br>X0Y0-X0Y3           |

X15125-111316

Figure 1-21: XCZU7, XAZU7, and XQZU7 Banks

### Bank Diagram by Package for XCZU7, XAZU7, and XQZU7

|                |                     |                     |                         |                                           |
|----------------|---------------------|---------------------|-------------------------|-------------------------------------------|
| HP I/O Bank 28 | HD I/O Bank 48<br>O | HP I/O Bank 68      | HD I/O Bank 88          | GTH Quad 228<br>X0Y20-X0Y23               |
| HP I/O Bank 27 | HD I/O Bank 47<br>N | HP I/O Bank 67      | HD I/O Bank 87          | GTH Quad 227<br>X0Y16-X0Y19<br>D [R]      |
| PS GTR 505     | PS MIO 502          | HP I/O Bank 66<br>D | SYSMON<br>Configuration | GTH Quad 226<br>X0Y12-X0Y15<br>C [R]      |
| PS DDR 504     | PS MIO 501          | HP I/O Bank 65<br>C | Configuration           | GTH Quad 225<br>X0Y8-X0Y11<br>B [R]       |
| PS CONFIG 503  | PS MIO 500          | HP I/O Bank 64<br>B | PCIE4<br>X0Y1           | GTH Quad 224<br>X0Y4-X0Y7<br>A [R] (RCAL) |
|                |                     | HP I/O Bank 63      | PCIE4<br>X0Y0           | GTH Quad 223<br>X0Y0-X0Y3                 |

X15126-112916

Figure 1-22: XCZU7 and XAZU7 Banks in FBVB900 Package and XQZU7 Banks in FFRB900 Package

|                     |                |                     |                           |                                           |
|---------------------|----------------|---------------------|---------------------------|-------------------------------------------|
| HP I/O Bank 28<br>R | HD I/O Bank 48 | HP I/O Bank 68<br>P | HD I/O Bank 88<br>O       | GTH Quad 228<br>X0Y20-X0Y23               |
| HP I/O Bank 27      | HD I/O Bank 47 | HP I/O Bank 67<br>Q | HD I/O Bank 87<br>N       | GTH Quad 227<br>X0Y16-X0Y19<br>E [R]      |
| PS GTR 505          | PS MIO 502     | HP I/O Bank 66<br>D | SYSMON<br>Configuration   | GTH Quad 226<br>X0Y12-X0Y15<br>D [R]      |
| PS DDR 504          | PS MIO 501     | HP I/O Bank 65<br>C | Configuration             | GTH Quad 225<br>X0Y8-X0Y11<br>C [R]       |
| PS CONFIG 503       | PS MIO 500     | HP I/O Bank 64<br>B | PCIE4<br>X0Y1<br>(tandem) | GTH Quad 224<br>X0Y4-X0Y7<br>B [R] (RCAL) |
|                     |                | HP I/O Bank 63      | PCIE4<br>X0Y0             | GTH Quad 223<br>X0Y0-X0Y3<br>A [R]        |

X15127-111316

Figure 1-23: **XCZU7 Banks in FFVC1156 Package and XQZU7 Banks in FFRC1156 Package**

|                     |                |                     |                           |                                            |
|---------------------|----------------|---------------------|---------------------------|--------------------------------------------|
| HP I/O Bank 28<br>R | HD I/O Bank 48 | HP I/O Bank 68<br>Q | HD I/O Bank 88<br>O       | GTH Quad 228<br>X0Y20-X0Y23<br>F [RN]      |
| HP I/O Bank 27<br>S | HD I/O Bank 47 | HP I/O Bank 67<br>P | HD I/O Bank 87<br>N       | GTH Quad 227<br>X0Y16-X0Y19<br>E [RN]      |
| PS GTR 505          | PS MIO 502     | HP I/O Bank 66<br>D | SYSMON<br>Configuration   | GTH Quad 226<br>X0Y12-X0Y15<br>D [RS]      |
| PS DDR 504          | PS MIO 501     | HP I/O Bank 65<br>C | Configuration             | GTH Quad 225<br>X0Y8-X0Y11<br>C [RS]       |
| PS CONFIG 503       | PS MIO 500     | HP I/O Bank 64<br>E | PCIE4<br>X0Y1<br>(tandem) | GTH Quad 224<br>X0Y4-X0Y7<br>B [RS] (RCAL) |
|                     |                | HP I/O Bank 63<br>F | PCIE4<br>X0Y0             | GTH Quad 223<br>X0Y0-X0Y3<br>A [RS]        |

X15128-111316

Figure 1-24: **XCZU7 Banks in FFVF1517 Package**

## XCZU6, XCZU9, and XQZU9 Bank Diagram Overview

|                                     |            |                         |                                     |
|-------------------------------------|------------|-------------------------|-------------------------------------|
| GTH Quad 130<br>X0Y12-X0Y15         |            | HD I/O Bank 50          | GTH Quad 230<br>X1Y12-X1Y15         |
| GTH Quad 129<br>X0Y8-X0Y11          |            | HD I/O Bank 49          | GTH Quad 229<br>X1Y8-X1Y11          |
| GTH Quad 128<br>X0Y4-X0Y7<br>(RCAL) |            | HD I/O Bank 48          | GTH Quad 228<br>X1Y4-X1Y7<br>(RCAL) |
| GTH Quad 127<br>X0Y0-X0Y3           |            | HD I/O Bank 47          | HP I/O Bank 67                      |
| PS GTR 505                          | PS MIO 502 | SYSMON<br>Configuration | HP I/O Bank 66                      |
| PS DDR 504                          | PS MIO 501 | Configuration           | HP I/O Bank 65                      |
| PS CONFIG 503                       | PS MIO 500 | HD I/O Bank 44          | HP I/O Bank 64                      |

X15129-061420

Figure 1-25: XCZU6, XCZU9, and XQZU9 Banks



### Bank Diagram by Package for XCZU6, XCZU9, and XQZU9

|                                           |            |                         |                                           |
|-------------------------------------------|------------|-------------------------|-------------------------------------------|
| GTH Quad 130<br>X0Y12-X0Y15               |            | HD I/O Bank 50          | GTH Quad 230<br>X1Y12-X1Y15<br>C [R]      |
| GTH Quad 129<br>X0Y8-X0Y11                |            | HD I/O Bank 49          | GTH Quad 229<br>X1Y8-X1Y11<br>B [R]       |
| GTH Quad 128<br>X0Y4-X0Y7<br>D [L] (RCAL) |            | HD I/O Bank 48<br>N     | GTH Quad 228<br>X1Y4-X1Y7<br>A [R] (RCAL) |
| GTH Quad 127<br>X0Y0-X0Y3                 |            | HD I/O Bank 47<br>O     | HP I/O Bank 67                            |
| PS GTR 505                                | PS MIO 502 | SYSMON<br>Configuration | HP I/O Bank 66<br>D                       |
| PS DDR 504                                | PS MIO 501 | Configuration           | HP I/O Bank 65<br>C                       |
| PS CONFIG 503                             | PS MIO 500 | HD I/O Bank 44          | HP I/O Bank 64<br>B                       |

X15130-061420

Figure 1-26: XCZU6 and XCZU9 Banks in FFVC900 Package and XQZU9 in FFRC900 Package

|                                           |            |                         |                                           |
|-------------------------------------------|------------|-------------------------|-------------------------------------------|
| GTH Quad 130<br>X0Y12-X0Y15<br>F [L]      |            | HD I/O Bank 50<br>Q     | GTH Quad 230<br>X1Y12-X1Y15<br>C [R]      |
| GTH Quad 129<br>X0Y8-X0Y11<br>E [L]       |            | HD I/O Bank 49<br>P     | GTH Quad 229<br>X1Y8-X1Y11<br>B [R]       |
| GTH Quad 128<br>X0Y4-X0Y7<br>D [L] (RCAL) |            | HD I/O Bank 48<br>O     | GTH Quad 228<br>X1Y4-X1Y7<br>A [R] (RCAL) |
| GTH Quad 127<br>X0Y0-X0Y3                 |            | HD I/O Bank 47<br>N     | HP I/O Bank 67<br>E                       |
| PS GTR 505                                | PS MIO 502 | SYSMON<br>Configuration | HP I/O Bank 66<br>D                       |
| PS DDR 504                                | PS MIO 501 | Configuration           | HP I/O Bank 65<br>C                       |
| PS CONFIG 503                             | PS MIO 500 | HD I/O Bank 44<br>A     | HP I/O Bank 64<br>B                       |

X15131-061420

Figure 1-27: XCZU6 and XCZU9 Banks in FFVB1156 Package and XQZU9 in FFRB1156 Package

## XCZU11, XAZU11, and XQZU11 Bank Diagram Overview

|                                      |               |                |                           |                                      |
|--------------------------------------|---------------|----------------|---------------------------|--------------------------------------|
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y3 | HP I/O Bank 71 | HD I/O Bank 91            | GTH Quad 231<br>X0Y28-X0Y31          |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | HP I/O Bank 70 | HD I/O Bank 90            | GTH Quad 230<br>X0Y24-X0Y27          |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69 | HD I/O Bank 89            | GTH Quad 229<br>X0Y20-X0Y23          |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y2 | HP I/O Bank 68 | HD I/O Bank 88            | GTH Quad 228<br>X0Y16-X0Y19          |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | HP I/O Bank 67 | PCIE4<br>X1Y1             | GTH Quad 227<br>X0Y12-X0Y15          |
| PS GTR 505                           | PS MIO 502    | HP I/O Bank 66 | SYSMON<br>Configuration   | GTH Quad 226<br>X0Y8-X0Y11<br>(RCAL) |
| PS DDR 504                           | PS MIO 501    | HP I/O Bank 65 | Configuration             | GTH Quad 225<br>X0Y4-X0Y7            |
| PS CONFIG 503                        | PS MIO 500    | HP I/O Bank 64 | PCIE4<br>X1Y0<br>(tandem) | GTH Quad 224<br>X0Y0-X0Y3            |

X15132-121517

Figure 1-28: XCZU11, XAZU11, and XQZU11 Banks

### Bank Diagram by Package for XCZU11, XAZU11, and XQZU11

|                                      |               |                     |                           |                                            |
|--------------------------------------|---------------|---------------------|---------------------------|--------------------------------------------|
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y3 | HP I/O Bank 71      | HD I/O Bank 91            | GTH Quad 231<br>X0Y28-X0Y31                |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | HP I/O Bank 70      | HD I/O Bank 90            | GTH Quad 230<br>X0Y24-X0Y27                |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69<br>P | HD I/O Bank 89<br>O       | GTH Quad 229<br>X0Y20-X0Y23                |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y2 | HP I/O Bank 68<br>Q | HD I/O Bank 88<br>N       | GTH Quad 228<br>X0Y16-X0Y19<br>E [R]       |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | HP I/O Bank 67<br>R | PCIE4<br>X1Y1             | GTH Quad 227<br>X0Y12-X0Y15<br>D [R]       |
| PS GTR 505                           | PS MIO 502    | HP I/O Bank 66<br>D | SYSMON<br>Configuration   | GTH Quad 226<br>X0Y8-X0Y11<br>C [R] (RCAL) |
| PS DDR 504                           | PS MIO 501    | HP I/O Bank 65<br>C | Configuration             | GTH Quad 225<br>X0Y4-X0Y7<br>B [R]         |
| PS CONFIG 503                        | PS MIO 500    | HP I/O Bank 64<br>B | PCIE4<br>X1Y0<br>(tandem) | GTH Quad 224<br>X0Y0-X0Y3<br>A [R]         |

X15133-121517

Figure 1-29: XCZU11 Banks in FFVC1156 Package and XQZU11 Banks in FFRC1156 Package

|                                      |               |                     |                           |                                            |
|--------------------------------------|---------------|---------------------|---------------------------|--------------------------------------------|
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y3 | HP I/O Bank 71<br>T | HD I/O Bank 91            | GTH Quad 231<br>X0Y28-X0Y31                |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | HP I/O Bank 70<br>U | HD I/O Bank 90<br>P       | GTH Quad 230<br>X0Y24-X0Y27                |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69<br>V | HD I/O Bank 89<br>O       | GTH Quad 229<br>X0Y20-X0Y23                |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y2 | HP I/O Bank 68<br>W | HD I/O Bank 88<br>N       | GTH Quad 228<br>X0Y16-X0Y19                |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | HP I/O Bank 67<br>X | PCIE4<br>X1Y1             | GTH Quad 227<br>X0Y12-X0Y15<br>D [R]       |
| PS GTR 505                           | PS MIO 502    | HP I/O Bank 66<br>E | SYSMON<br>Configuration   | GTH Quad 226<br>X0Y8-X0Y11<br>C [R] (RCAL) |
| PS DDR 504                           | PS MIO 501    | HP I/O Bank 65<br>C | Configuration             | GTH Quad 225<br>X0Y4-X0Y7<br>B [R]         |
| PS CONFIG 503                        | PS MIO 500    | HP I/O Bank 64<br>D | PCIE4<br>X1Y0<br>(tandem) | GTH Quad 224<br>X0Y0-X0Y3<br>A [R]         |

X15134-121517

Figure 1-30: XCZU11 Banks in FFVB1517 Package

|                                      |               |                     |                           |                                             |
|--------------------------------------|---------------|---------------------|---------------------------|---------------------------------------------|
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y3 | HP I/O Bank 71<br>Q | HD I/O Bank 91            | GTH Quad 231<br>X0Y28-X0Y31<br>H [RN]       |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | HP I/O Bank 70<br>P | HD I/O Bank 90            | GTH Quad 230<br>X0Y24-X0Y27<br>G [RN]       |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69<br>R | HD I/O Bank 89<br>O       | GTH Quad 229<br>X0Y20-X0Y23<br>F [RN]       |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y2 | HP I/O Bank 68<br>S | HD I/O Bank 88<br>N       | GTH Quad 228<br>X0Y16-X0Y19<br>E [RN]       |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | HP I/O Bank 67<br>E | PCIE4<br>X1Y1             | GTH Quad 227<br>X0Y12-X0Y15<br>D [RS]       |
| PS GTR 505                           | PS MIO 502    | HP I/O Bank 66<br>D | SYSMON<br>Configuration   | GTH Quad 226<br>X0Y8-X0Y11<br>C [RS] (RCAL) |
| PS DDR 504                           | PS MIO 501    | HP I/O Bank 65<br>C | Configuration             | GTH Quad 225<br>X0Y4-X0Y7<br>B [RS]         |
| PS CONFIG 503                        | PS MIO 500    | HP I/O Bank 64<br>F | PCIE4<br>X1Y0<br>(tandem) | GTH Quad 224<br>X0Y0-X0Y3<br>A [RS]         |

X15135-121517

Figure 1-31: XCZU11 and XAZU11 Banks in FVF1517 Package

|                                            |               |                     |                           |                                             |
|--------------------------------------------|---------------|---------------------|---------------------------|---------------------------------------------|
| GTY Quad 131<br>X0Y16-X0Y19<br>M [L]       | PCIE4<br>X0Y3 | HP I/O Bank 71<br>R | HD I/O Bank 91<br>Q       | GTH Quad 231<br>X0Y28-X0Y31<br>H [RN]       |
| GTY Quad 130<br>X0Y12-X0Y15<br>L [L]       | CMAC<br>X0Y1  | HP I/O Bank 70<br>S | HD I/O Bank 90<br>P       | GTH Quad 230<br>X0Y24-X0Y27<br>G [RN]       |
| GTY Quad 129<br>X0Y8-X0Y11<br>K [L] (RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69<br>T | HD I/O Bank 89<br>O       | GTH Quad 229<br>X0Y20-X0Y23<br>F [RN]       |
| GTY Quad 128<br>X0Y4-X0Y7<br>J [L]         | PCIE4<br>X0Y2 | HP I/O Bank 68<br>U | HD I/O Bank 88<br>N       | GTH Quad 228<br>X0Y16-X0Y19<br>E [RN]       |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | HP I/O Bank 67<br>F | PCIE4<br>X1Y1             | GTH Quad 227<br>X0Y12-X0Y15<br>D [RS]       |
| PS GTR 505                                 | PS MIO 502    | HP I/O Bank 66<br>E | SYSMON<br>Configuration   | GTH Quad 226<br>X0Y8-X0Y11<br>C [RS] (RCAL) |
| PS DDR 504                                 | PS MIO 501    | HP I/O Bank 65<br>C | Configuration             | GTH Quad 225<br>X0Y4-X0Y7<br>B [RS]         |
| PS CONFIG 503                              | PS MIO 500    | HP I/O Bank 64<br>D | PCIE4<br>X1Y0<br>(tandem) | GTH Quad 224<br>X0Y0-X0Y3<br>A [RS]         |

X15136-121517

Figure 1-32: XCZU11 Banks in FFVC1760 Package and XQZU11 Banks in FFRC1760 Package

## XCZU15 and XQZU15 Bank Diagrams

|                                     |            |                         |                                     |
|-------------------------------------|------------|-------------------------|-------------------------------------|
| GTH Quad 130<br>X0Y12-X0Y15         |            | HD I/O Bank 50          | GTH Quad 230<br>X1Y12-X1Y15         |
| GTH Quad 129<br>X0Y8-X0Y11          |            | HD I/O Bank 49          | GTH Quad 229<br>X1Y8-X1Y11          |
| GTH Quad 128<br>X0Y4-X0Y7<br>(RCAL) |            | HD I/O Bank 48          | GTH Quad 228<br>X1Y4-X1Y7<br>(RCAL) |
| GTH Quad 127<br>X0Y0-X0Y3           |            | HD I/O Bank 47          | HP I/O Bank 67                      |
| PS GTR 505                          | PS MIO 502 | SYSMON<br>Configuration | HP I/O Bank 66                      |
| PS DDR 504                          | PS MIO 501 | Configuration           | HP I/O Bank 65                      |
| PS CONFIG 503                       | PS MIO 500 | HD I/O Bank 44          | HP I/O Bank 64                      |

X15137-061420

Figure 1-33: XCZU15 and XQZU15 Banks



### Bank Diagram by Package for XCZU15 and XQZU15

|                                           |            |                         |                                           |
|-------------------------------------------|------------|-------------------------|-------------------------------------------|
| GTH Quad 130<br>X0Y12-X0Y15               |            | HD I/O Bank 50          | GTH Quad 230<br>X1Y12-X1Y15<br>C [R]      |
| GTH Quad 129<br>X0Y8-X0Y11                |            | HD I/O Bank 49          | GTH Quad 229<br>X1Y8-X1Y11<br>B [R]       |
| GTH Quad 128<br>X0Y4-X0Y7<br>D [L] (RCAL) |            | HD I/O Bank 48<br>N     | GTH Quad 228<br>X1Y4-X1Y7<br>A [R] (RCAL) |
| GTH Quad 127<br>X0Y0-X0Y3                 |            | HD I/O Bank 47<br>O     | HP I/O Bank 67                            |
| PS GTR 505                                | PS MIO 502 | SYSMON<br>Configuration | HP I/O Bank 66<br>D                       |
| PS DDR 504                                | PS MIO 501 | Configuration           | HP I/O Bank 65<br>C                       |
| PS CONFIG 503                             | PS MIO 500 | HD I/O Bank 44          | HP I/O Bank 64<br>B                       |

X15138-061420

Figure 1-34: XCZU15 Banks in FFVC900 Package and XQZU15 Banks in FFRC900 Package

|                                           |            |                         |                                           |
|-------------------------------------------|------------|-------------------------|-------------------------------------------|
| GTH Quad 130<br>X0Y12-X0Y15<br>F [L]      |            | HD I/O Bank 50<br>Q     | GTH Quad 230<br>X1Y12-X1Y15<br>C [R]      |
| GTH Quad 129<br>X0Y8-X0Y11<br>E [L]       |            | HD I/O Bank 49<br>P     | GTH Quad 229<br>X1Y8-X1Y11<br>B [R]       |
| GTH Quad 128<br>X0Y4-X0Y7<br>D [L] (RCAL) |            | HD I/O Bank 48<br>O     | GTH Quad 228<br>X1Y4-X1Y7<br>A [R] (RCAL) |
| GTH Quad 127<br>X0Y0-X0Y3                 |            | HD I/O Bank 47<br>N     | HP I/O Bank 67<br>E                       |
| PS GTR 505                                | PS MIO 502 | SYSMON<br>Configuration | HP I/O Bank 66<br>D                       |
| PS DDR 504                                | PS MIO 501 | Configuration           | HP I/O Bank 65<br>C                       |
| PS CONFIG 503                             | PS MIO 500 | HD I/O Bank 44<br>A     | HP I/O Bank 64<br>B                       |

X15139-061420

Figure 1-35: XCZU15 Banks in FFVB1156 Package and XQZU15 Banks in FFRB1156 Package

## XCZU17, XCZU19, and XQZU19 Bank Diagram Overview

|                                      |               |                |                           |                                      |
|--------------------------------------|---------------|----------------|---------------------------|--------------------------------------|
| GTY Quad 134<br>X0Y28-X0Y31          | CMAC<br>X0Y3  | HP I/O Bank 74 | HD I/O Bank 94            | GTH Quad 234<br>X0Y40-X0Y43          |
| GTY Quad 133<br>X0Y24-X0Y27          | ILKN<br>X0Y2  | HP I/O Bank 73 | HD I/O Bank 93            | GTH Quad 233<br>X0Y36-X0Y39          |
| GTY Quad 132<br>X0Y20-X0Y23          | CMAC<br>X0Y2  | HP I/O Bank 72 | ILKN<br>X1Y1              | GTH Quad 232<br>X0Y32-X0Y35          |
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y3 | HP I/O Bank 71 | HD I/O Bank 91            | GTH Quad 231<br>X0Y28-X0Y31          |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | HP I/O Bank 70 | HD I/O Bank 90            | GTH Quad 230<br>X0Y24-X0Y27          |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69 | ILKN<br>X1Y0              | GTH Quad 229<br>X0Y20-X0Y23          |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y2 | HP I/O Bank 68 | PCIE4<br>X1Y2             | GTH Quad 228<br>X0Y16-X0Y19          |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | HP I/O Bank 67 | PCIE4<br>X1Y1             | GTH Quad 227<br>X0Y12-X0Y15          |
| PS GTR 505                           | PS MIO 502    | HP I/O Bank 66 | SYSMON<br>Configuration   | GTH Quad 226<br>X0Y8-X0Y11<br>(RCAL) |
| PS DDR 504                           | PS MIO 501    | HP I/O Bank 65 | Configuration             | GTH Quad 225<br>X0Y4-X0Y7            |
| PS CONFIG 503                        | PS MIO 500    | HP I/O Bank 64 | PCIE4<br>X1Y0<br>(tandem) | GTH Quad 224<br>X0Y0-X0Y3            |

X15140-071417

Figure 1-36: XCZU17, XCZU19, and XQZU19 Banks

### Bank Diagram by Package for XCZU17, XCZU19, and XQZU19

|                                      |               |                     |                           |                                            |
|--------------------------------------|---------------|---------------------|---------------------------|--------------------------------------------|
| GTY Quad 134<br>X0Y28-X0Y31          | CMAC<br>X0Y3  | HP I/O Bank 74<br>Q | HD I/O Bank 94            | GTH Quad 234<br>X0Y40-X0Y43                |
| GTY Quad 133<br>X0Y24-X0Y27          | ILKN<br>X0Y2  | HP I/O Bank 73<br>R | HD I/O Bank 93<br>P       | GTH Quad 233<br>X0Y36-X0Y39                |
| GTY Quad 132<br>X0Y20-X0Y23          | CMAC<br>X0Y2  | HP I/O Bank 72<br>S | ILKN<br>X1Y1              | GTH Quad 232<br>X0Y32-X0Y35                |
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y3 | HP I/O Bank 71<br>T | HD I/O Bank 91<br>O       | GTH Quad 231<br>X0Y28-X0Y31                |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | HP I/O Bank 70<br>U | HD I/O Bank 90<br>N       | GTH Quad 230<br>X0Y24-X0Y27                |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69<br>V | ILKN<br>X1Y0              | GTH Quad 229<br>X0Y20-X0Y23                |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y2 | HP I/O Bank 68<br>W | PCIE4<br>X1Y2             | GTH Quad 228<br>X0Y16-X0Y19                |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | HP I/O Bank 67<br>X | PCIE4<br>X1Y1             | GTH Quad 227<br>X0Y12-X0Y15<br>D [R]       |
| PS GTR 505                           | PS MIO 502    | HP I/O Bank 66<br>E | SYSMON<br>Configuration   | GTH Quad 226<br>X0Y8-X0Y11<br>C [R] (RCAL) |
| PS DDR 504                           | PS MIO 501    | HP I/O Bank 65<br>C | Configuration             | GTH Quad 225<br>X0Y4-X0Y7<br>B [R]         |
| PS CONFIG 503                        | PS MIO 500    | HP I/O Bank 64<br>D | PCIE4<br>X1Y0<br>(tandem) | GTH Quad 224<br>X0Y0-X0Y3<br>A [R]         |

X15141-071417

Figure 1-37: XCZU17 and XCZU19 Banks in FFVB1517 Package and XQZU19 Banks in FFRB1517 Package

|                                            |               |                     |                           |                                             |
|--------------------------------------------|---------------|---------------------|---------------------------|---------------------------------------------|
| GTY Quad 134<br>X0Y28-X0Y31                | CMAC<br>X0Y3  | HP I/O Bank 74      | HD I/O Bank 94<br>Q       | GTH Quad 234<br>X0Y40-X0Y43                 |
| GTY Quad 133<br>X0Y24-X0Y27                | ILKN<br>X0Y2  | HP I/O Bank 73      | HD I/O Bank 93<br>P       | GTH Quad 233<br>X0Y36-X0Y39                 |
| GTY Quad 132<br>X0Y20-X0Y23                | CMAC<br>X0Y2  | HP I/O Bank 72      | ILKN<br>X1Y1              | GTH Quad 232<br>X0Y32-X0Y35                 |
| GTY Quad 131<br>X0Y16-X0Y19<br>M [L]       | PCIE4<br>X0Y3 | HP I/O Bank 71<br>R | HD I/O Bank 91<br>O       | GTH Quad 231<br>X0Y28-X0Y31<br>H [RN]       |
| GTY Quad 130<br>X0Y12-X0Y15<br>L [L]       | CMAC<br>X0Y1  | HP I/O Bank 70<br>S | HD I/O Bank 90<br>N       | GTH Quad 230<br>X0Y24-X0Y27<br>G [RN]       |
| GTY Quad 129<br>X0Y8-X0Y11<br>K [L] (RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69<br>T | ILKN<br>X1Y0              | GTH Quad 229<br>X0Y20-X0Y23<br>F [RN]       |
| GTY Quad 128<br>X0Y4-X0Y7<br>J [L]         | PCIE4<br>X0Y2 | HP I/O Bank 68<br>U | PCIE4<br>X1Y2             | GTH Quad 228<br>X0Y16-X0Y19<br>E [RN]       |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | HP I/O Bank 67<br>F | PCIE4<br>X1Y1             | GTH Quad 227<br>X0Y12-X0Y15<br>D [RS]       |
| PS GTR 505                                 | PS MIO 502    | HP I/O Bank 66<br>E | SYSMON<br>Configuration   | GTH Quad 226<br>X0Y8-X0Y11<br>C [RS] (RCAL) |
| PS DDR 504                                 | PS MIO 501    | HP I/O Bank 65<br>C | Configuration             | GTH Quad 225<br>X0Y4-X0Y7<br>B [RS]         |
| PS CONFIG 503                              | PS MIO 500    | HP I/O Bank 64<br>D | PCIE4<br>X1Y0<br>(tandem) | GTH Quad 224<br>X0Y0-X0Y3<br>A [RS]         |

X15142-071417

Figure 1-38: XCZU17 and XCZU19 Banks in FFVC1760 Package and XQZU19 Banks in FFRC1760 Package

|                                            |               |                     |                           |                                             |
|--------------------------------------------|---------------|---------------------|---------------------------|---------------------------------------------|
| GTY Quad 134<br>X0Y28-X0Y31<br>R [L]       | CMAC<br>X0Y3  | HP I/O Bank 74      | HD I/O Bank 94            | GTH Quad 234<br>X0Y40-X0Y43<br>K [RN]       |
| GTY Quad 133<br>X0Y24-X0Y27<br>Q [L]       | ILKN<br>X0Y2  | HP I/O Bank 73      | HD I/O Bank 93            | GTH Quad 233<br>X0Y36-X0Y39<br>J [RN]       |
| GTY Quad 132<br>X0Y20-X0Y23<br>P [L]       | CMAC<br>X0Y2  | HP I/O Bank 72      | ILKN<br>X1Y1              | GTH Quad 232<br>X0Y32-X0Y35<br>I [RN]       |
| GTY Quad 131<br>X0Y16-X0Y19<br>O [L]       | PCIE4<br>X0Y3 | HP I/O Bank 71<br>P | HD I/O Bank 91<br>O       | GTH Quad 231<br>X0Y28-X0Y31<br>H [RN]       |
| GTY Quad 130<br>X0Y12-X0Y15<br>N [L]       | CMAC<br>X0Y1  | HP I/O Bank 70<br>Q | HD I/O Bank 90<br>N       | GTH Quad 230<br>X0Y24-X0Y27<br>G [RN]       |
| GTY Quad 129<br>X0Y8-X0Y11<br>M [L] (RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69<br>R | ILKN<br>X1Y0              | GTH Quad 229<br>X0Y20-X0Y23<br>F [RS]       |
| GTY Quad 128<br>X0Y4-X0Y7<br>L [L]         | PCIE4<br>X0Y2 | HP I/O Bank 68      | PCIE4<br>X1Y2             | GTH Quad 228<br>X0Y16-X0Y19<br>E [RS]       |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | HP I/O Bank 67      | PCIE4<br>X1Y1             | GTH Quad 227<br>X0Y12-X0Y15<br>D [RS]       |
| PS GTR 505                                 | PS MIO 502    | HP I/O Bank 66<br>D | SYSMON<br>Configuration   | GTH Quad 226<br>X0Y8-X0Y11<br>C [RS] (RCAL) |
| PS DDR 504                                 | PS MIO 501    | HP I/O Bank 65<br>C | Configuration             | GTH Quad 225<br>X0Y4-X0Y7<br>B [RS]         |
| PS CONFIG 503                              | PS MIO 500    | HP I/O Bank 64      | PCIE4<br>X1Y0<br>(tandem) | GTH Quad 224<br>X0Y0-X0Y3<br>A [RS]         |

X15143-071417

Figure 1-39: XCZU17 and XCZU19 Banks in FFVD1760 Package

|                                      |               |                     |                           |                                             |
|--------------------------------------|---------------|---------------------|---------------------------|---------------------------------------------|
| GTY Quad 134<br>X0Y28-X0Y31          | CMAC<br>X0Y3  | HP I/O Bank 74<br>R | HD I/O Bank 94<br>Q       | GTH Quad 234<br>X0Y40-X0Y43<br>K [RN]       |
| GTY Quad 133<br>X0Y24-X0Y27          | ILKN<br>X0Y2  | HP I/O Bank 73<br>S | HD I/O Bank 93<br>P       | GTH Quad 233<br>X0Y36-X0Y39<br>J [RN]       |
| GTY Quad 132<br>X0Y20-X0Y23          | CMAC<br>X0Y2  | HP I/O Bank 72<br>T | ILKN<br>X1Y1              | GTH Quad 232<br>X0Y32-X0Y35<br>I [RN]       |
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y3 | HP I/O Bank 71<br>U | HD I/O Bank 91<br>O       | GTH Quad 231<br>X0Y28-X0Y31<br>H [RN]       |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | HP I/O Bank 70<br>V | HD I/O Bank 90<br>N       | GTH Quad 230<br>X0Y24-X0Y27<br>G [RN]       |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69<br>W | ILKN<br>X1Y0              | GTH Quad 229<br>X0Y20-X0Y23<br>F [RS]       |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y2 | HP I/O Bank 68<br>X | PCIE4<br>X1Y2             | GTH Quad 228<br>X0Y16-X0Y19<br>E [RS]       |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | HP I/O Bank 67<br>F | PCIE4<br>X1Y1             | GTH Quad 227<br>X0Y12-X0Y15<br>D [RS]       |
| PS GTR 505                           | PS MIO 502    | HP I/O Bank 66<br>E | SYSMON<br>Configuration   | GTH Quad 226<br>X0Y8-X0Y11<br>C [RS] (RCAL) |
| PS DDR 504                           | PS MIO 501    | HP I/O Bank 65<br>C | Configuration             | GTH Quad 225<br>X0Y4-X0Y7<br>B [RS]         |
| PS CONFIG 503                        | PS MIO 500    | HP I/O Bank 64<br>D | PCIE4<br>X1Y0<br>(tandem) | GTH Quad 224<br>X0Y0-X0Y3<br>A [RS]         |

X15144-071417

Figure 1-40: XCZU17 and XCZU19 Banks in FFVE1924 Package

## XCZU21DR and XQZU21DR Bank Diagram Overview

|                                      |               |        |                |                         |
|--------------------------------------|---------------|--------|----------------|-------------------------|
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y1 | SD-FEC | HP I/O Bank 71 | HD I/O Bank 91          |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | SD-FEC | HP I/O Bank 70 | HD I/O Bank 90          |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | SD-FEC | HP I/O Bank 69 | HD I/O Bank 89          |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y0 | SD-FEC | HP I/O Bank 68 | HD I/O Bank 88          |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | SD-FEC | HP I/O Bank 67 | HD I/O Bank 87          |
| PS GTR 505                           | PS MIO 502    | SD-FEC | HP I/O Bank 66 | SYSMON<br>Configuration |
| PS DDR 504                           | PS MIO 501    | SD-FEC | HP I/O Bank 65 | Configuration           |
| PS CONFIG 503                        | PS MIO 500    | SD-FEC | HP I/O Bank 64 | HD I/O Bank 84          |

X19543-101518

Figure 1-41: XCZU21DR and XQZU21DR Banks



### Bank Diagram by Package for XCZU21DR and XQZU21DR

|                                            |               |        |                     |                         |
|--------------------------------------------|---------------|--------|---------------------|-------------------------|
| GTY Quad 131<br>X0Y16-X0Y19<br>D [L]       | PCIE4<br>X0Y1 | SD-FEC | HP I/O Bank 71      | HD I/O Bank 91          |
| GTY Quad 130<br>X0Y12-X0Y15<br>C [L]       | CMAC<br>X0Y1  | SD-FEC | HP I/O Bank 70      | HD I/O Bank 90          |
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | SD-FEC | HP I/O Bank 69      | HD I/O Bank 89<br>P     |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | SD-FEC | HP I/O Bank 68<br>F | HD I/O Bank 88<br>O     |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | SD-FEC | HP I/O Bank 67<br>E | HD I/O Bank 87<br>N     |
| PS GTR 505                                 | PS MIO 502    | SD-FEC | HP I/O Bank 66<br>D | SYSMON<br>Configuration |
| PS DDR 504                                 | PS MIO 501    | SD-FEC | HP I/O Bank 65<br>C | Configuration           |
| PS CONFIG 503                              | PS MIO 500    | SD-FEC | HP I/O Bank 64      | HD I/O Bank 84          |

X19535-081621

Figure 1-42: XCZU21DR Banks in FFVD1156 Package and XQZU21DR Banks in FFRD1156 Package

## XCZU25DR Bank Diagram Overview

|                                      |               |                |                         |              |
|--------------------------------------|---------------|----------------|-------------------------|--------------|
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69 | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y0 | HP I/O Bank 68 | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | HP I/O Bank 67 | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                           | PS MIO 502    | HP I/O Bank 66 | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                           | PS MIO 501    | HP I/O Bank 65 | Configuration           | ADC Bank 225 |
| PS CONFIG 503                        | PS MIO 500    | HP I/O Bank 64 | HD I/O Bank 84          | ADC Bank 224 |

X19546-042720

Figure 1-43: XCZU25DR Banks

### Bank Diagram by Package for XCZU25DR

|                                            |               |                     |                         |              |
|--------------------------------------------|---------------|---------------------|-------------------------|--------------|
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69      | HD I/O Bank 89<br>O     | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | HP I/O Bank 68      | HD I/O Bank 88<br>N     | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | HP I/O Bank 67      | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | HP I/O Bank 66<br>D | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | HP I/O Bank 65<br>C | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | HP I/O Bank 64      | HD I/O Bank 84          | ADC Bank 224 |

X19547-042720

Figure 1-44: XCZU25DR Banks in FFVE1156 and FSVE1156 Packages

|                                            |               |                               |                         |              |
|--------------------------------------------|---------------|-------------------------------|-------------------------|--------------|
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69<br>S           | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | HP I/O Bank 68<br>R           | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | HP I/O Bank 67<br>Q           | HD I/O Bank 87<br>N     | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | HP I/O Bank 66<br>D           | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | HP I/O Bank 65<br>C           | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | HP I/O Bank 64<br>B (Partial) | HD I/O Bank 84<br>A     | ADC Bank 224 |

X19548-040720

Figure 1-45: XCZU25DR Banks in FFVG1517 and FSVG1517 Packages

## XCZU27DR Bank Diagram Overview

|                                      |               |                |                         |              |
|--------------------------------------|---------------|----------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y1 | HP I/O Bank 71 | HD I/O Bank 91          |              |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | HP I/O Bank 70 | HD I/O Bank 90          |              |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69 | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y0 | HP I/O Bank 68 | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | HP I/O Bank 67 | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                           | PS MIO 502    | HP I/O Bank 66 | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                           | PS MIO 501    | HP I/O Bank 65 | Configuration           | ADC Bank 225 |
| PS CONFIG 503                        | PS MIO 500    | HP I/O Bank 64 | HD I/O Bank 84          | ADC Bank 224 |

X19549-040320

Figure 1-46: XCZU27DR Banks

### Bank Diagram by Package for XCZU27DR

|                                            |               |                     |                         |              |
|--------------------------------------------|---------------|---------------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19                | PCIE4<br>X0Y1 | HP I/O Bank 71      | HD I/O Bank 91          |              |
| GTY Quad 130<br>X0Y12-X0Y15                | CMAC<br>X0Y1  | HP I/O Bank 70      | HD I/O Bank 90          |              |
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69      | HD I/O Bank 89<br>O     | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | HP I/O Bank 68      | HD I/O Bank 88<br>N     | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | HP I/O Bank 67      | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | HP I/O Bank 66<br>D | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | HP I/O Bank 65<br>C | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | HP I/O Bank 64      | HD I/O Bank 84          | ADC Bank 224 |

X19550-040320

Figure 1-47: XCZU27DR Banks in FFVE1156 and FSVE1156 Packages

|                                            |               |                               |                         |              |
|--------------------------------------------|---------------|-------------------------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19<br>D [L]       | PCIE4<br>X0Y1 | HP I/O Bank 71                | HD I/O Bank 91          |              |
| GTY Quad 130<br>X0Y12-X0Y15<br>C [L]       | CMAC<br>X0Y1  | HP I/O Bank 70                | HD I/O Bank 90          |              |
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69<br>S           | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | HP I/O Bank 68<br>R           | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | HP I/O Bank 67<br>Q           | HD I/O Bank 87<br>N     | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | HP I/O Bank 66<br>D           | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | HP I/O Bank 65<br>C           | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | HP I/O Bank 64<br>B (Partial) | HD I/O Bank 84<br>A     | ADC Bank 224 |

X19551-040320

Figure 1-48: XCZU27DR Banks in FFVG1517 and FSVG1517 Packages

## XCZU28DR and XQZU28DR Bank Diagram Overview

|                                      |               |        |                |                         |              |
|--------------------------------------|---------------|--------|----------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y1 | SD-FEC | HP I/O Bank 71 | HD I/O Bank 91          |              |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | SD-FEC | HP I/O Bank 70 | HD I/O Bank 90          |              |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | SD-FEC | HP I/O Bank 69 | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y0 | SD-FEC | HP I/O Bank 68 | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | SD-FEC | HP I/O Bank 67 | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                           | PS MIO 502    | SD-FEC | HP I/O Bank 66 | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                           | PS MIO 501    | SD-FEC | HP I/O Bank 65 | Configuration           | ADC Bank 225 |
| PS CONFIG 503                        | PS MIO 500    | SD-FEC | HP I/O Bank 64 | HD I/O Bank 84          | ADC Bank 224 |

X19552-040320

Figure 1-49: XCZU28DR and XQZU28DR Banks

### Bank Diagram by Package for XCZU28DR and XQZU28DR

|                                            |               |        |                     |                         |              |
|--------------------------------------------|---------------|--------|---------------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19                | PCIE4<br>X0Y1 | SD-FEC | HP I/O Bank 71      | HD I/O Bank 91          |              |
| GTY Quad 130<br>X0Y12-X0Y15                | CMAC<br>X0Y1  | SD-FEC | HP I/O Bank 70      | HD I/O Bank 90          |              |
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | SD-FEC | HP I/O Bank 69      | HD I/O Bank 89<br>O     | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | SD-FEC | HP I/O Bank 68      | HD I/O Bank 88<br>N     | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | SD-FEC | HP I/O Bank 67      | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | SD-FEC | HP I/O Bank 66<br>D | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | SD-FEC | HP I/O Bank 65<br>C | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | SD-FEC | HP I/O Bank 64      | HD I/O Bank 84          | ADC Bank 224 |

X19553-042720

Figure 1-50: XCZU28DR Banks in FFVE1156 and FSVE1156 Packages and XQZU28DR in FFRE1156 Package



|                                            |               |        |                               |                         |              |
|--------------------------------------------|---------------|--------|-------------------------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19<br>D [L]       | PCIE4<br>X0Y1 | SD-FEC | HP I/O Bank 71                | HD I/O Bank 91          |              |
| GTY Quad 130<br>X0Y12-X0Y15<br>C [L]       | CMAC<br>X0Y1  | SD-FEC | HP I/O Bank 70                | HD I/O Bank 90          |              |
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | SD-FEC | HP I/O Bank 69<br>S           | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | SD-FEC | HP I/O Bank 68<br>R           | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | SD-FEC | HP I/O Bank 67<br>Q           | HD I/O Bank 87<br>N     | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | SD-FEC | HP I/O Bank 66<br>D           | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | SD-FEC | HP I/O Bank 65<br>C           | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | SD-FEC | HP I/O Bank 64<br>B (Partial) | HD I/O Bank 84<br>A     | ADC Bank 224 |

X19554-042720

**Figure 1-51: XCZU28DR Banks in FFVG1517 and FSVG1517 Packages and XQZU28DR in FFRG1517 Package**

## XCZU29DR, XQZU29DR, and XCZU39DR Bank Diagram Overview

|                                      |               |                |                         |              |
|--------------------------------------|---------------|----------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y1 | HP I/O Bank 71 | HD I/O Bank 91          | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | HP I/O Bank 70 | HD I/O Bank 90          | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69 | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y0 | HP I/O Bank 68 | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | HP I/O Bank 67 | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                           | PS MIO 502    | HP I/O Bank 66 | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                           | PS MIO 501    | HP I/O Bank 65 | Configuration           | ADC Bank 225 |
| PS CONFIG 503                        | PS MIO 500    | HP I/O Bank 64 | HD I/O Bank 84          | ADC Bank 224 |

X19555-040620

Figure 1-52: XCZU29DR, XQZU29DR, and XCZU39DR Banks

### Bank Diagram by Package for XCZU29DR, XQZU29DR, and XCZU39DR

|                                            |               |                     |                         |              |
|--------------------------------------------|---------------|---------------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19<br>D [L]       | PCIE4<br>X0Y1 | HP I/O Bank 71      | HD I/O Bank 91          | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15<br>C [L]       | CMAC<br>X0Y1  | HP I/O Bank 70      | HD I/O Bank 90          | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69<br>T | HD I/O Bank 89<br>P     | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | HP I/O Bank 68<br>S | HD I/O Bank 88<br>O     | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | HP I/O Bank 67<br>R | HD I/O Bank 87<br>N     | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | HP I/O Bank 66<br>D | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | HP I/O Bank 65<br>C | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | HP I/O Bank 64<br>B | HD I/O Bank 84<br>A     | ADC Bank 224 |

X19556-042620

Figure 1-53: XCZU29DR and XCZU39DR Banks in FFVF1760 and FSVF1760 Packages and XQZU29DR Banks in FFRF1760 Package

## XCZU42DR Bank Diagram Overview

|                                     |              |                |                         |              |
|-------------------------------------|--------------|----------------|-------------------------|--------------|
| GTY Quad 128<br>X0Y4-X0Y7<br>(RCAL) |              | HP I/O Bank 68 | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3           | CMAC<br>X0Y0 | HP I/O Bank 67 |                         | DAC Bank 227 |
| PS GTR 505                          | PS MIO 502   | HP I/O Bank 66 | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                          | PS MIO 501   | HP I/O Bank 65 | Configuration           | ADC Bank 225 |
| PS CONFIG 503                       | PS MIO 500   | HP I/O Bank 64 |                         | ADC Bank 224 |

X25704-090221

Figure 1-54: XCZU42DR Banks

### Bank Diagram by Package for XCZU42DR

|                                           |              |                               |                         |              |
|-------------------------------------------|--------------|-------------------------------|-------------------------|--------------|
| GTY Quad 128<br>X0Y4-X0Y7<br>B [L] (RCAL) |              | HP I/O Bank 68                | HD I/O Bank 88<br>O     | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3<br>A [L]        | CMAC<br>X0Y0 | HP I/O Bank 67<br>N (Partial) |                         | DAC Bank 227 |
| PS GTR 505                                | PS MIO 502   | HP I/O Bank 66<br>D           | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                | PS MIO 501   | HP I/O Bank 65<br>C           | Configuration           | ADC Bank 225 |
| PS CONFIG 503                             | PS MIO 500   | HP I/O Bank 64                |                         | ADC Bank 224 |

X25705-011422

Figure 1-55: XCZU42DR Banks in FFVE1156 and FSVE1156 Packages

## XCZU43DR Bank Diagram Overview

|                                      |               |                |                         |              |
|--------------------------------------|---------------|----------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y1 | HP I/O Bank 71 | HD I/O Bank 91          | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | HP I/O Bank 70 | HD I/O Bank 90          | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69 | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y0 | HP I/O Bank 68 | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | HP I/O Bank 67 | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                           | PS MIO 502    | HP I/O Bank 66 | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                           | PS MIO 501    | HP I/O Bank 65 | Configuration           | ADC Bank 225 |
| PS CONFIG 503                        | PS MIO 500    | HP I/O Bank 64 | HD I/O Bank 84          | ADC Bank 224 |

X23814-042620

Figure 1-56: XCZU43DR Banks

### Bank Diagram by Package for XCZU43DR

|                                            |               |                     |                         |              |
|--------------------------------------------|---------------|---------------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19                | PCIE4<br>X0Y1 | HP I/O Bank 71      | HD I/O Bank 91          | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15                | CMAC<br>X0Y1  | HP I/O Bank 70      | HD I/O Bank 90          | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69      | HD I/O Bank 89<br>O     | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | HP I/O Bank 68      | HD I/O Bank 88<br>N     | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | HP I/O Bank 67      | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | HP I/O Bank 66<br>D | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | HP I/O Bank 65<br>C | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | HP I/O Bank 64      | HD I/O Bank 84          | ADC Bank 224 |

XZ3816-122021

Figure 1-57: XCZU43DR Banks in FFVE1156 and FSVE1156 Packages

|                                            |               |                               |                         |              |
|--------------------------------------------|---------------|-------------------------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19<br>D [L]       | PCIE4<br>X0Y1 | HP I/O Bank 71                | HD I/O Bank 91          | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15<br>C [L]       | CMAC<br>X0Y1  | HP I/O Bank 70                | HD I/O Bank 90          | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69<br>S           | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | HP I/O Bank 68<br>R           | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | HP I/O Bank 67<br>Q           | HD I/O Bank 87<br>N     | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | HP I/O Bank 66<br>D           | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | HP I/O Bank 65<br>C           | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | HP I/O Bank 64<br>B (Partial) | HD I/O Bank 84<br>A     | ADC Bank 224 |

X23817-042720

Figure 1-58: XCZU43DR Banks in FFVG1517 and FSVG1517 Packages

## XCZU46DR Bank Diagram Overview

|                                      |               |        |                |                         |              |
|--------------------------------------|---------------|--------|----------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y1 | SD-FEC | HP I/O Bank 71 | HD I/O Bank 91          | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | SD-FEC | HP I/O Bank 70 | HD I/O Bank 90          | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | SD-FEC | HP I/O Bank 69 | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y0 | SD-FEC | HP I/O Bank 68 | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | SD-FEC | HP I/O Bank 67 | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                           | PS MIO 502    | SD-FEC | HP I/O Bank 66 | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                           | PS MIO 501    | SD-FEC | HP I/O Bank 65 | Configuration           | ADC Bank 225 |
| PS CONFIG 503                        | PS MIO 500    | SD-FEC | HP I/O Bank 64 | HD I/O Bank 84          | ADC Bank 224 |

X23818-042720

Figure 1-59: XCZU46DR Banks



### Bank Diagram by Package for XCZU46DR

|                                            |               |        |                     |                         |              |
|--------------------------------------------|---------------|--------|---------------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19<br>D [L]       | PCIE4<br>X0Y1 | SD-FEC | HP I/O Bank 71<br>S | HD I/O Bank 91<br>P     | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15<br>C [L]       | CMAC<br>X0Y1  | SD-FEC | HP I/O Bank 70<br>T | HD I/O Bank 90<br>O     | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | SD-FEC | HP I/O Bank 69<br>R | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | SD-FEC | HP I/O Bank 68      | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | SD-FEC | HP I/O Bank 67      | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | SD-FEC | HP I/O Bank 66<br>D | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | SD-FEC | HP I/O Bank 65<br>C | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | SD-FEC | HP I/O Bank 64<br>B | HD I/O Bank 84          | ADC Bank 224 |

X23819-081621

Figure 1-60: XCZU46DR Banks in FFVH1760 and FSVH1760 Packages

## XCZU47DR Bank Diagram Overview

|                                      |               |                |                         |              |
|--------------------------------------|---------------|----------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y1 | HP I/O Bank 71 | HD I/O Bank 91          | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | HP I/O Bank 70 | HD I/O Bank 90          | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69 | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y0 | HP I/O Bank 68 | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | HP I/O Bank 67 | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                           | PS MIO 502    | HP I/O Bank 66 | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                           | PS MIO 501    | HP I/O Bank 65 | Configuration           | ADC Bank 225 |
| PS CONFIG 503                        | PS MIO 500    | HP I/O Bank 64 | HD I/O Bank 84          | ADC Bank 224 |

X23820-042720

Figure 1-61: XCZU47DR Banks

### Bank Diagram by Package for XCZU47DR

|                                            |               |                     |                         |              |
|--------------------------------------------|---------------|---------------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19                | PCIE4<br>X0Y1 | HP I/O Bank 71      | HD I/O Bank 91          | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15                | CMAC<br>X0Y1  | HP I/O Bank 70      | HD I/O Bank 90          | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69      | HD I/O Bank 89<br>O     | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | HP I/O Bank 68      | HD I/O Bank 88<br>N     | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | HP I/O Bank 67      | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | HP I/O Bank 66<br>D | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | HP I/O Bank 65<br>C | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | HP I/O Bank 64      | HD I/O Bank 84          | ADC Bank 224 |

X23821-042720

Figure 1-62: XCZU47DR Banks in FFVE1156 and FSVE1156 Packages

|                                            |               |                               |                         |              |
|--------------------------------------------|---------------|-------------------------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19<br>D [L]       | PCIE4<br>X0Y1 | HP I/O Bank 71                | HD I/O Bank 91          | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15<br>C [L]       | CMAC<br>X0Y1  | HP I/O Bank 70                | HD I/O Bank 90          | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69<br>S           | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | HP I/O Bank 68<br>R           | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | HP I/O Bank 67<br>Q           | HD I/O Bank 87<br>N     | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | HP I/O Bank 66<br>D           | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | HP I/O Bank 65<br>C           | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | HP I/O Bank 64<br>B (Partial) | HD I/O Bank 84<br>A     | ADC Bank 224 |

X23822-042720

Figure 1-63: XCZU47DR Banks in FFVG1517 and FSVG1517 Packages

## XCZU48DR Bank Diagram Overview

|                                      |               |        |                |                         |              |
|--------------------------------------|---------------|--------|----------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y1 | SD-FEC | HP I/O Bank 71 | HD I/O Bank 91          | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | SD-FEC | HP I/O Bank 70 | HD I/O Bank 90          | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | SD-FEC | HP I/O Bank 69 | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y0 | SD-FEC | HP I/O Bank 68 | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | SD-FEC | HP I/O Bank 67 | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                           | PS MIO 502    | SD-FEC | HP I/O Bank 66 | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                           | PS MIO 501    | SD-FEC | HP I/O Bank 65 | Configuration           | ADC Bank 225 |
| PS CONFIG 503                        | PS MIO 500    | SD-FEC | HP I/O Bank 64 | HD I/O Bank 84          | ADC Bank 224 |

X23823-042720

Figure 1-64: XCZU48DR Banks

### Bank Diagram by Package for XCZU48DR

|                                            |               |     |                     |                         |              |
|--------------------------------------------|---------------|-----|---------------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19                | PCIE4<br>X0Y1 | FEC | HP I/O Bank 71      | HD I/O Bank 91          | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15                | CMAC<br>X0Y1  | FEC | HP I/O Bank 70      | HD I/O Bank 90          | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | FEC | HP I/O Bank 69      | HD I/O Bank 89<br>O     | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | FEC | HP I/O Bank 68      | HD I/O Bank 88<br>N     | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | FEC | HP I/O Bank 67      | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | FEC | HP I/O Bank 66<br>D | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | FEC | HP I/O Bank 65<br>C | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | FEC | HP I/O Bank 64      | HD I/O Bank 84          | ADC Bank 224 |

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Figure 1-65: XCZU48DR Banks in FFVE1156 and FSVE1156 Packages

|                                            |               |        |                               |                         |              |
|--------------------------------------------|---------------|--------|-------------------------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19<br>D [L]       | PCIE4<br>X0Y1 | SD-FEC | HP I/O Bank 71                | HD I/O Bank 91          | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15<br>C [L]       | CMAC<br>X0Y1  | SD-FEC | HP I/O Bank 70                | HD I/O Bank 90          | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | SD-FEC | HP I/O Bank 69<br>S           | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | SD-FEC | HP I/O Bank 68<br>R           | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | SD-FEC | HP I/O Bank 67<br>Q           | HD I/O Bank 87<br>N     | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | SD-FEC | HP I/O Bank 66<br>D           | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | SD-FEC | HP I/O Bank 65<br>C           | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | SD-FEC | HP I/O Bank 64<br>B (Partial) | HD I/O Bank 84<br>A     | ADC Bank 224 |

X23825-042720

Figure 1-66: XCZU48DR Banks in FFVG1517 and FSVG1517, and XQZU48DR Banks in FSRG1517 Packages

## XCZU49DR Bank Diagram Overview

|                                      |               |                |                         |              |
|--------------------------------------|---------------|----------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19          | PCIE4<br>X0Y1 | HP I/O Bank 71 | HD I/O Bank 91          | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15          | CMAC<br>X0Y1  | HP I/O Bank 70 | HD I/O Bank 90          | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>(RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69 | HD I/O Bank 89          | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7            | PCIE4<br>X0Y0 | HP I/O Bank 68 | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3            | CMAC<br>X0Y0  | HP I/O Bank 67 | HD I/O Bank 87          | ADC Bank 227 |
| PS GTR 505                           | PS MIO 502    | HP I/O Bank 66 | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                           | PS MIO 501    | HP I/O Bank 65 | Configuration           | ADC Bank 225 |
| PS CONFIG 503                        | PS MIO 500    | HP I/O Bank 64 | HD I/O Bank 84          | ADC Bank 224 |

X23826-042720

Figure 1-67: XCZU49DR Banks

### Bank Diagram by Package for XCZU49DR

|                                            |               |                     |                         |              |
|--------------------------------------------|---------------|---------------------|-------------------------|--------------|
| GTY Quad 131<br>X0Y16-X0Y19<br>D [L]       | PCIE4<br>X0Y1 | HP I/O Bank 71      | HD I/O Bank 91          | DAC Bank 231 |
| GTY Quad 130<br>X0Y12-X0Y15<br>C [L]       | CMAC<br>X0Y1  | HP I/O Bank 70      | HD I/O Bank 90          | DAC Bank 230 |
| GTY Quad 129<br>X0Y8-X0Y11<br>B [L] (RCAL) | ILKN<br>X0Y0  | HP I/O Bank 69<br>T | HD I/O Bank 89<br>P     | DAC Bank 229 |
| GTY Quad 128<br>X0Y4-X0Y7<br>A [L]         | PCIE4<br>X0Y0 | HP I/O Bank 68<br>S | HD I/O Bank 88<br>O     | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3                  | CMAC<br>X0Y0  | HP I/O Bank 67<br>R | HD I/O Bank 87<br>N     | ADC Bank 227 |
| PS GTR 505                                 | PS MIO 502    | HP I/O Bank 66<br>D | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                 | PS MIO 501    | HP I/O Bank 65<br>C | Configuration           | ADC Bank 225 |
| PS CONFIG 503                              | PS MIO 500    | HP I/O Bank 64<br>B | HD I/O Bank 84<br>A     | ADC Bank 224 |

X23815-042720

Figure 1-68: XCZU49DR Banks in FFVF1760 and FSVF1760, and XQZU49DR Banks in FSRF1760 Packages



## XCZU63DR Bank Diagram Overview

|                                     |              |                |                         |              |
|-------------------------------------|--------------|----------------|-------------------------|--------------|
| GTY Quad 128<br>X0Y4-X0Y7<br>(RCAL) |              | HP I/O Bank 68 | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3           | CMAC<br>X0Y0 | HP I/O Bank 67 |                         | DAC Bank 227 |
| PS GTR 505                          | PS MIO 502   | HP I/O Bank 66 | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                          | PS MIO 501   | HP I/O Bank 65 | Configuration           | ADC Bank 225 |
| PS CONFIG 503                       | PS MIO 500   | HP I/O Bank 64 |                         | ADC Bank 224 |

X28948-010524

Figure 1-69: XCZU63DR Banks

### Bank Diagram by Package for XCZU63DR

|                                     |              |                               |                         |                           |
|-------------------------------------|--------------|-------------------------------|-------------------------|---------------------------|
| GTY Quad 128<br>X0Y4-X0Y7<br>(RCAL) |              | HP I/O Bank 68                | HD I/O Bank 88<br>O     | DAC Bank 228              |
| GTY Quad 127<br>X0Y0-X0Y3<br>A [L]  | CMAC<br>X0Y0 | HP I/O Bank 67<br>N (Partial) |                         | DAC Bank 227              |
| PS GTR 505                          | PS MIO 502   | HP I/O Bank 66<br>D           | SYSMON<br>Configuration | ADC Bank 226<br>(Partial) |
| PS DDR 504                          | PS MIO 501   | HP I/O Bank 65<br>C           | Configuration           | ADC Bank 225              |
| PS CONFIG 503                       | PS MIO 500   | HP I/O Bank 64                |                         | ADC Bank 224              |

X28949-010524

Figure 1-70: XCZU63DR Banks in FFVE1156 and FSVE1156 Packages

## XCZU64DR Bank Diagram Overview

|                                     |              |                |                         |              |
|-------------------------------------|--------------|----------------|-------------------------|--------------|
| GTY Quad 128<br>X0Y4-X0Y7<br>(RCAL) |              | HP I/O Bank 68 | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3           | CMAC<br>X0Y0 | HP I/O Bank 67 |                         | DAC Bank 227 |
| PS GTR 505                          | PS MIO 502   | HP I/O Bank 66 | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                          | PS MIO 501   | HP I/O Bank 65 | Configuration           | ADC Bank 225 |
| PS CONFIG 503                       | PS MIO 500   | HP I/O Bank 64 |                         | ADC Bank 224 |

X28951-010524

Figure 1-71: XCZU64DR Banks

### Bank Diagram by Package for XCZU64DR

|                                           |              |                               |                         |                           |
|-------------------------------------------|--------------|-------------------------------|-------------------------|---------------------------|
| GTY Quad 128<br>X0Y4-X0Y7<br>B [L] (RCAL) |              | HP I/O Bank 68                | HD I/O Bank 88<br>O     | DAC Bank 228              |
| GTY Quad 127<br>X0Y0-X0Y3<br>A [L]        | CMAC<br>X0Y0 | HP I/O Bank 67<br>N (Partial) |                         | DAC Bank 227              |
| PS GTR 505                                | PS MIO 502   | HP I/O Bank 66<br>D           | SYSMON<br>Configuration | ADC Bank 226<br>(Partial) |
| PS DDR 504                                | PS MIO 501   | HP I/O Bank 65<br>C           | Configuration           | ADC Bank 225              |
| PS CONFIG 503                             | PS MIO 500   | HP I/O Bank 64                |                         | ADC Bank 224              |

X28950-010524

Figure 1-72: XCZU64DR Banks in FFVE1156 and FSVE1156 Packages

## XCZU65DR Bank Diagram Overview

|                                     |              |                |                         |              |
|-------------------------------------|--------------|----------------|-------------------------|--------------|
| GTY Quad 128<br>X0Y4-X0Y7<br>(RCAL) |              | HP I/O Bank 68 | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3           | CMAC<br>X0Y0 | HP I/O Bank 67 |                         | DAC Bank 227 |
| PS GTR 505                          | PS MIO 502   | HP I/O Bank 66 | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                          | PS MIO 501   | HP I/O Bank 65 | Configuration           | ADC Bank 225 |
| PS CONFIG 503                       | PS MIO 500   | HP I/O Bank 64 |                         | ADC Bank 224 |

X25706-090221

Figure 1-73: XCZU65DR Banks

### Bank Diagram by Package for XCZU65DR

|                                           |              |                               |                         |              |
|-------------------------------------------|--------------|-------------------------------|-------------------------|--------------|
| GTY Quad 128<br>X0Y4-X0Y7<br>B [L] (RCAL) |              | HP I/O Bank 68                | HD I/O Bank 88<br>O     | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3<br>A [L]        | CMAC<br>X0Y0 | HP I/O Bank 67<br>N (Partial) |                         | DAC Bank 227 |
| PS GTR 505                                | PS MIO 502   | HP I/O Bank 66<br>D           | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                | PS MIO 501   | HP I/O Bank 65<br>C           | Configuration           | ADC Bank 225 |
| PS CONFIG 503                             | PS MIO 500   | HP I/O Bank 64                |                         | ADC Bank 224 |

X25707-011322

Figure 1-74: XCZU65DR Banks in FFVE1156 and FSVE1156 Packages

## XCZU67DR Bank Diagram Overview

|                                     |              |                |                         |              |
|-------------------------------------|--------------|----------------|-------------------------|--------------|
| GTY Quad 128<br>X0Y4-X0Y7<br>(RCAL) |              | HP I/O Bank 68 | HD I/O Bank 88          | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3           | CMAC<br>X0Y0 | HP I/O Bank 67 |                         | DAC Bank 227 |
| PS GTR 505                          | PS MIO 502   | HP I/O Bank 66 | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                          | PS MIO 501   | HP I/O Bank 65 | Configuration           | ADC Bank 225 |
| PS CONFIG 503                       | PS MIO 500   | HP I/O Bank 64 |                         | ADC Bank 224 |

X25708-090221

Figure 1-75: XCZU67DR Banks

### Bank Diagram by Package for XCZU67DR

|                                           |              |                               |                         |              |
|-------------------------------------------|--------------|-------------------------------|-------------------------|--------------|
| GTY Quad 128<br>X0Y4-X0Y7<br>B [L] (RCAL) |              | HP I/O Bank 68                | HD I/O Bank 88<br>O     | DAC Bank 228 |
| GTY Quad 127<br>X0Y0-X0Y3<br>A [L]        | CMAC<br>X0Y0 | HP I/O Bank 67<br>N (Partial) |                         | DAC Bank 227 |
| PS GTR 505                                | PS MIO 502   | HP I/O Bank 66<br>D           | SYSMON<br>Configuration | ADC Bank 226 |
| PS DDR 504                                | PS MIO 501   | HP I/O Bank 65<br>C           | Configuration           | ADC Bank 225 |
| PS CONFIG 503                             | PS MIO 500   | HP I/O Bank 64                |                         | ADC Bank 224 |

X25709-011322

Figure 1-76: XCZU67DR Banks in FFVE1156 and FSVE1156 Packages

# PS Memory Interface Pin Guidelines

## Introduction to PS Memory Interface Pins

This chapter shows what is needed to support the broad requirements of various memory interfaces using the Zynq™ UltraScale+™ device DDR subsystem. It covers DDR3/3L, DDR4, LPDDR4, and LPDDR3.



**IMPORTANT:** SBVA484 and SFVA625 packages only support 32-bit data buses for the PS DDR controller. The Zynq UltraScale+ device DDR subsystem can only be configured for 32-bit or 32-bit plus ECC DDR3/DDR4/LPDDR3 designs when using these packages.



**IMPORTANT:** For the devices in the SBVA484, UBVA454, and UBVA530 packages, the HP I/Os in bank 66 are powered by VCCO\_65.

## DDR3/3L Guidelines

### DDR3/3L Pin Rules

The DDR3/3L pin rules are for single and dual-rank memory interfaces.

- All unused DDR pins can be left unconnected. For example, in a 64-bit interface without ECC, the PS\_DDR\_DQ64 to PS\_DDR\_DQ71, PS\_DDR\_DQS\_P8/N8, and PS\_DDR\_DM8 pins can be left unconnected.
- Connect the PS\_DDR\_ZQ pin to GND using a 240Ω resistor. There should be separate 240Ω resistors at the MPSoC or RFSoc and at the DRAM.

### DDR3/3L Pin Swapping Restrictions

- Address/command/control bits cannot be swapped.
- DQ byte lane swapping is allowed. A byte lane includes any signals associated with the aligned 8-bits of DQ, such as DM, DQS, DQS\_N, and DQ signals.
- DQ bits swapping within a byte lane is allowed.

## DDR3/3L Pinout Example for Supported Configurations

Table 2-1 shows a pinout example for the DDR3/3L supported configurations. For termination details, see the *UltraScale Architecture PCB Design Guide (UG583)*. When not being used for a memory interface, all pins should be left unconnected with the exception of VCCO\_PSDDR and VCC\_PSDDR\_PLL, which should be tied to GND.



**IMPORTANT:** *VCC\_PSINTFP must be tied to VCC\_PSINTFP\_DDR. This requirement is in Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics (DS925) and Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics (DS926), where both VCC\_PSINTFP and VCC\_PSINTFP\_DDR must be connected to the same supply and thus both must be powered to avoid MBIST failure.*

Table 2-1: DDR3/3L Supported Pinout Configurations

| Pin Name                  | DDR3/3L 64-bit 1Rank                                 | DDR3/3L 64-bit 2Rank                                 | DDR3/3L 32-bit 1Rank                                 | DDR3/3L 32-bit 2Rank                                 |
|---------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|
| VCCO_PSDDR <sup>(1)</sup> | Set to 1.5V (1.35V for DDR3L)                        | Set to 1.5V (1.35V for DDR3L)                        | Set to 1.5V (1.35V for DDR3L)                        | Set to 1.5V (1.35V for DDR3L)                        |
| PS_DDR_A0 to PS_DDR_A15   | Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on. | Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on. | Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on. | Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on. |
| PS_DDR_A16                | WE#                                                  | WE#                                                  | WE#                                                  | WE#                                                  |
| PS_DDR_A17                | CAS#                                                 | CAS#                                                 | CAS#                                                 | CAS#                                                 |
| PS_DDR_ACT_N              | RAS#                                                 | RAS#                                                 | RAS#                                                 | RAS#                                                 |
| PS_DDR_ALERT_N            | Can be left unconnected.                             | Can be left unconnected.                             | Can be left unconnected.                             | Can be left unconnected.                             |
| PS_DDR_BA0                | BA[0]                                                | BA[0]                                                | BA[0]                                                | BA[0]                                                |
| PS_DDR_BA1                | BA[1]                                                | BA[1]                                                | BA[1]                                                | BA[1]                                                |
| PS_DDR_BG0                | BA[2]                                                | BA[2]                                                | BA[2]                                                | BA[2]                                                |
| PS_DDR_BG1                | Can be left unconnected.                             | Can be left unconnected.                             | Can be left unconnected.                             | Can be left unconnected.                             |
| PS_DDR_CK_N0              | CK#                                                  | CK#[0]                                               | CK#                                                  | CK#[0]                                               |
| PS_DDR_CK_N1              | Can be left unconnected.                             | CK#[1]                                               | Can be left unconnected.                             | CK#[1]                                               |
| PS_DDR_CK0                | CK.                                                  | CK[0]                                                | CK.                                                  | CK[0]                                                |
| PS_DDR_CK1                | Can be left unconnected.                             | CK[1]                                                | Can be left unconnected.                             | CK[1]                                                |
| PS_DDR_CKE0               | CKE                                                  | CKE[0]                                               | CKE                                                  | CKE[0]                                               |
| PS_DDR_CKE1               | Can be left unconnected.                             | CKE[1]                                               | Can be left unconnected.                             | CKE[1]                                               |
| PS_DDR_CS_N0              | CS#                                                  | CS#[0]                                               | CS#                                                  | CS#[0]                                               |

Table 2-1: DDR3/3L Supported Pinout Configurations (Cont'd)

| Pin Name                   | DDR3/3L 64-bit 1Rank                                         | DDR3/3L 64-bit 2Rank                                         | DDR3/3L 32-bit 1Rank                                     | DDR3/3L 32-bit 2Rank                                     |
|----------------------------|--------------------------------------------------------------|--------------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------|
| PS_DDR_CS_N1               | Can be left unconnected.                                     | CS#[1]                                                       | Can be left unconnected.                                 | CS#[1]                                                   |
| PS_DDR_DM0 to PS_DDR_DM3   | Connect DM0 to PS_DDR_DM0, DM1 to PS_DDR_DM1, and so on.     | Connect DM0 to PS_DDR_DM0, DM1 to PS_DDR_DM1, and so on.     | Connect DM0 to PS_DDR_DM0, DM1 to PS_DDR_DM1, and so on. | Connect DM0 to PS_DDR_DM0, DM1 to PS_DDR_DM1, and so on. |
| PS_DDR_DM4 to PS_DDR_DM7   | Connect DM4 to PS_DDR_DM4, DM5 to PS_DDR_DM5, and so on.     | Connect DM4 to PS_DDR_DM4, DM5 to PS_DDR_DM5, and so on.     | Can be left unconnected.                                 | Can be left unconnected.                                 |
| PS_DDR_DM8                 | DM8, can be left unconnected without ECC.                    | DM8, can be left unconnected without ECC.                    | DM4, can be left unconnected without ECC.                | DM4, can be left unconnected without ECC.                |
| PS_DDR_DQ0 to PS_DDR_DQ31  | Connect DQ0 to PS_DDR_DQ0, DQ1 to PS_DDR_DQ1, and so on.     | Connect DQ0 to PS_DDR_DQ0, DQ1 to PS_DDR_DQ1, and so on.     | Connect DQ0 to PS_DDR_DQ0, DQ1 to PS_DDR_DQ1, and so on. | Connect DQ0 to PS_DDR_DQ0, DQ1 to PS_DDR_DQ1, and so on. |
| PS_DDR_DQ32 to PS_DDR_DQ63 | Connect DQ32 to PS_DDR_DQ32, DQ33 to PS_DDR_DQ33, and so on. | Connect DQ32 to PS_DDR_DQ32, DQ33 to PS_DDR_DQ33, and so on. | Can be left unconnected.                                 | Can be left unconnected.                                 |
| PS_DDR_DQ64                | ECC_bit[0], can be left unconnected without ECC.             | ECC_bit[0], can be left unconnected without ECC.             | ECC_bit[0], can be left unconnected without ECC.         | ECC_bit[0], can be left unconnected without ECC.         |
| PS_DDR_DQ65                | ECC_bit[1], can be left unconnected without ECC.             | ECC_bit[1], can be left unconnected without ECC.             | ECC_bit[1], can be left unconnected without ECC.         | ECC_bit[1], can be left unconnected without ECC.         |
| PS_DDR_DQ66                | ECC_bit[2], can be left unconnected without ECC.             | ECC_bit[2], can be left unconnected without ECC.             | ECC_bit[2], can be left unconnected without ECC.         | ECC_bit[2], can be left unconnected without ECC.         |
| PS_DDR_DQ67                | ECC_bit[3], can be left unconnected without ECC.             | ECC_bit[3], can be left unconnected without ECC.             | ECC_bit[3], can be left unconnected without ECC.         | ECC_bit[3], can be left unconnected without ECC.         |
| PS_DDR_DQ68                | ECC_bit[4], can be left unconnected without ECC.             | ECC_bit[4], can be left unconnected without ECC.             | ECC_bit[4], can be left unconnected without ECC.         | ECC_bit[4], can be left unconnected without ECC.         |
| PS_DDR_DQ69                | ECC_bit[5], can be left unconnected without ECC.             | ECC_bit[5], can be left unconnected without ECC.             | ECC_bit[5], can be left unconnected without ECC.         | ECC_bit[5], can be left unconnected without ECC.         |
| PS_DDR_DQ70                | ECC_bit[6], can be left unconnected without ECC.             | ECC_bit[6], can be left unconnected without ECC.             | ECC_bit[6], can be left unconnected without ECC.         | ECC_bit[6], can be left unconnected without ECC.         |

Table 2-1: DDR3/3L Supported Pinout Configurations (Cont'd)

| Pin Name                       | DDR3/3L 64-bit 1Rank                                                  | DDR3/3L 64-bit 2Rank                                                  | DDR3/3L 32-bit 1Rank                                                  | DDR3/3L 32-bit 2Rank                                                  |
|--------------------------------|-----------------------------------------------------------------------|-----------------------------------------------------------------------|-----------------------------------------------------------------------|-----------------------------------------------------------------------|
| PS_DDR_DQ71                    | ECC_bit[7], can be left unconnected without ECC.                      | ECC_bit[7], can be left unconnected without ECC.                      | ECC_bit[7], can be left unconnected without ECC.                      | ECC_bit[7], can be left unconnected without ECC.                      |
| PS_DDR_DQS_N0 to PS_DDR_DQS_N3 | Connect DQS#0 to PS_DDR_DQS_N0, DQS#1 to PS_DDR_DQS_N1, and so on.    | Connect DQS#0 to PS_DDR_DQS_N0, DQS#1 to PS_DDR_DQS_N1, and so on.    | Connect DQS#0 to PS_DDR_DQS_N0, DQS#1 to PS_DDR_DQS_N1, and so on.    | Connect DQS#0 to PS_DDR_DQS_N0, DQS#1 to PS_DDR_DQS_N1, and so on.    |
| PS_DDR_DQS_N4 to PS_DDR_DQS_N7 | Connect DQS#4 to PS_DDR_DQS_N4, DQS#5 to PS_DDR_DQS_N5, and so on.    | Connect DQS#4 to PS_DDR_DQS_N4, DQS#5 to PS_DDR_DQS_N5, and so on.    | Can be left unconnected.                                              | Can be left unconnected.                                              |
| PS_DDR_DQS_N8                  | DQS#8, can be left unconnected without ECC.                           | DQS#8, can be left unconnected without ECC.                           | DQS#4, can be left unconnected without ECC.                           | DQS#4, can be left unconnected without ECC.                           |
| PS_DDR_DQS_P0 to PS_DDR_DQS_P3 | Connect DQS0 to PS_DDR_DQS_P0, DQS1 to PS_DDR_DQS_P1, and so on.      | Connect DQS0 to PS_DDR_DQS_P0, DQS1 to PS_DDR_DQS_P1, and so on.      | Connect DQS0 to PS_DDR_DQS_P0, DQS1 to PS_DDR_DQS_P1, and so on.      | Connect DQS0 to PS_DDR_DQS_P0, DQS1 to PS_DDR_DQS_P1, and so on.      |
| PS_DDR_DQS_P4 to PS_DDR_DQS_P7 | Connect DQS4 to PS_DDR_DQS_P4, DQS5 to PS_DDR_DQS_P5, and so on.      | Connect DQS4 to PS_DDR_DQS_P4, DQS5 to PS_DDR_DQS_P5, and so on.      | Can be left unconnected.                                              | Can be left unconnected.                                              |
| PS_DDR_DQS_P8                  | DQS8, can be left unconnected without ECC.                            | DQS8, can be left unconnected without ECC.                            | DQS4, can be left unconnected without ECC.                            | DQS4, can be left unconnected without ECC.                            |
| PS_DDR_ODT0                    | ODT                                                                   | ODT[0]                                                                | ODT                                                                   | ODT[0]                                                                |
| PS_DDR_ODT1                    | Can be left unconnected.                                              | ODT[1]                                                                | Can be left unconnected.                                              | ODT[1]                                                                |
| PS_DDR_PARITY                  | Par_In for RDIMMs. Can be left unconnected for components and UDIMMs. | Par_In for RDIMMs. Can be left unconnected for components and UDIMMs. | Par_In for RDIMMs. Can be left unconnected for components and UDIMMs. | Par_In for RDIMMs. Can be left unconnected for components and UDIMMs. |
| PS_DDR_RAM_RST_N               | RESET#                                                                | RESET#                                                                | RESET#                                                                | RESET#                                                                |
| PS_DDR_ZQ                      | Connect a 240Ω resistor to GND. <sup>(2)</sup>                        | Connect a 240Ω resistor to GND. <sup>(2)</sup>                        | Connect a 240Ω resistor to GND. <sup>(2)</sup>                        | Connect a 240Ω resistor to GND. <sup>(2)</sup>                        |

**Notes:**

- For VCCO\_PSDDR decoupling guidelines, see the *UltraScale Architecture PCB Design Guide* (UG583).
- There should be separate 240Ω resistors at the FPGA and at the DRAM.



---

## DDR4 Guidelines

### ***DDR4 Pin Rules***

The DDR4 pin rules are for single and dual-rank memory interfaces.

- All unused DDR pins can be left unconnected. For example, in a 64-bit interface without ECC, the PS\_DDR\_DQ64 to PS\_DDR\_DQ71, PS\_DDR\_DQS\_P8/N8, and PS\_DDR\_DM8 pins can be left unconnected.
- The PS\_DDR\_ALERT\_N can be left floating at the DRAM. For component interfaces, connect the PS\_DDR\_ALERT\_N pin to the ALERT\_N pins of the DDR4 devices in fly-by routing, and terminate to  $V_{DD}$  with a  $50\Omega$  pull-up resistor. For DIMM designs, connect the PS\_DDR\_ALERT\_N pin to the ALERT\_N pin of the connector.
- Connect the PS\_DDR\_ZQ pin to GND using a  $240\Omega$  resistor. There should be separate  $240\Omega$  resistors at the FPGA and at the DRAM.
- Component interfaces with the same component for all components in the interface. The x16 components have a different number of bank groups than the x8 components. For example, create a 72-bit wide component interface by using nine x8 components or five x16 components, where half of one component is not used. Creating four x16 components and one x8 component is not permissible.

### ***DDR4 Pin Swapping Restrictions***

- Address/command/control bits cannot be swapped.
- DQ byte lane swapping is allowed. A byte lane includes any signals associated with the aligned 8-bits of DQ, such as DM, DQS, DQS\_N, and DQ signals.
- DQ bits swapping within a byte lane is allowed.

DDR4 Pinout Example for Supported Configurations

Table 2-2 shows a pinout example for the DDR4 supported configurations. For termination details, see details, see the *UltraScale Architecture PCB Design Guide* ([UG583](#)). When not being used for a memory be left unconnected with the exception of VCCO\_PSDDR and VCC\_PSDDR\_PLL, which should be tied to



**IMPORTANT:** *VCC\_PSINTFP must be tied to VCC\_PSINTFP\_DDR. This requirement is in his requirement is in Zynq Sheet: DC and AC Switching Characteristics ([DS925](#)) and Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching where both VCC\_PSINTFP and VCC\_PSINTFP\_DDR must be connected to the same supply and thus both must be p failure.*

Table 2-2: DDR4 Supported Pinout Configurations

| Pin Name                  | DDR4 64-bit 1Rank                                                                                                                                                         | DDR4 64-bit 2Rank                                                                                                                                                         | DDR4 32-bit 1Rank                                                                                                                                                         | DDR4 32-bit 2Rank                                                                                                                                                         | DDR4 16-bit 1Rank                                                                                                                                                         |
|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VCCO_PSDDR <sup>(1)</sup> | Set to 1.2V.                                                                                                                                                              | Set to 1.2V.                                                                                                                                                              | Set to 1.2V.                                                                                                                                                              | Set to 1.2V.                                                                                                                                                              | Set to 1.2V.                                                                                                                                                              |
| PS_DDR_A0 to PS_DDR_A16   | Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on.<br>WE_N can be shared with PS_DDR_A14, CAS_N can be shared with PS_DDR_A15, and RAS_N can be shared with PS_DDR_A16. | Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on.<br>WE_N can be shared with PS_DDR_A14, CAS_N can be shared with PS_DDR_A15, and RAS_N can be shared with PS_DDR_A16. | Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on.<br>WE_N can be shared with PS_DDR_A14, CAS_N can be shared with PS_DDR_A15, and RAS_N can be shared with PS_DDR_A16. | Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on.<br>WE_N can be shared with PS_DDR_A14, CAS_N can be shared with PS_DDR_A15, and RAS_N can be shared with PS_DDR_A16. | Connect A0 to PS_DDR_A0, A1 to PS_DDR_A1, and so on.<br>WE_N can be shared with PS_DDR_A14, CAS_N can be shared with PS_DDR_A15, and RAS_N can be shared with PS_DDR_A16. |
| PS_DDR_A17                | Can be left unconnected                                                                                                                                                   | Can be left unconnected                                                                                                                                                   | Can be left unconnected                                                                                                                                                   | Can be left unconnected                                                                                                                                                   | Can be left unconnected                                                                                                                                                   |
| PS_DDR_ACT_N              | ACT_n                                                                                                                                                                     | ACT_n                                                                                                                                                                     | ACT_n                                                                                                                                                                     | ACT_n                                                                                                                                                                     | ACT_n                                                                                                                                                                     |
| PS_DDR_ALERT_N            | ALERT_n                                                                                                                                                                   | ALERT_n                                                                                                                                                                   | ALERT_n                                                                                                                                                                   | ALERT_n                                                                                                                                                                   | ALERT_n                                                                                                                                                                   |
| PS_DDR_BA0                | BA[0]                                                                                                                                                                     | BA[0]                                                                                                                                                                     | BA[0]                                                                                                                                                                     | BA[0]                                                                                                                                                                     | BA[0]                                                                                                                                                                     |
| PS_DDR_BA1                | BA[1]                                                                                                                                                                     | BA[1]                                                                                                                                                                     | BA[1]                                                                                                                                                                     | BA[1]                                                                                                                                                                     | BA[1]                                                                                                                                                                     |

Table 2-2: DDR4 Supported Pinout Configurations (Cont'd)

| Pin Name                    | DDR4 64-bit<br>1Rank                                                                              | DDR4 64-bit<br>2Rank                                                                              | DDR4 32-bit<br>1Rank                                                                              | DDR4 32-bit<br>2Rank                                                                              | DDR4 16-bit<br>1Rank                                                                              |
|-----------------------------|---------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------|
| PS_DDR_BG0                  | BG[0]                                                                                             | BG[0]                                                                                             | BG[0]                                                                                             | BG[0]                                                                                             | BG[0]                                                                                             |
| PS_DDR_BG1 <sup>(2)</sup>   | BG[1]                                                                                             | BG[1]                                                                                             | BG[1]                                                                                             | BG[1]                                                                                             | BG[1]                                                                                             |
| PS_DDR_CK_N0                | CK_c[0]                                                                                           | CK_c[0]                                                                                           | CK_c[0]                                                                                           | CK_c[0]                                                                                           | CK_c[0]                                                                                           |
| PS_DDR_CK_N1                | Can be left<br>unconnected.                                                                       | CK_c[1]                                                                                           | Can be left<br>unconnected.                                                                       | CK_c[1]                                                                                           | Can be left<br>unconnected.                                                                       |
| PS_DDR_CK0                  | CK_t[0]                                                                                           | CK_t[0]                                                                                           | CK_t[0]                                                                                           | CK_t[0]                                                                                           | CK_t[0]                                                                                           |
| PS_DDR_CK1                  | Can be left<br>unconnected.                                                                       | CK_t[1]                                                                                           | Can be left<br>unconnected.                                                                       | CK_t[1]                                                                                           | Can be left<br>unconnected.                                                                       |
| PS_DDR_CKE0                 | CKE                                                                                               | CKE[0]                                                                                            | CKE                                                                                               | CKE[0]                                                                                            | CKE                                                                                               |
| PS_DDR_CKE1                 | Can be left<br>unconnected.                                                                       | CKE[1]                                                                                            | Can be left<br>unconnected.                                                                       | CKE[1]                                                                                            | Can be left<br>unconnected.                                                                       |
| PS_DDR_CS_N0                | CS_n                                                                                              | CS_n[0]                                                                                           | CS_n                                                                                              | CS_n[0]                                                                                           | CS_n                                                                                              |
| PS_DDR_CS_N1                | Can be left<br>unconnected.                                                                       | CS_n[1]                                                                                           | Can be left<br>unconnected.                                                                       | CS_n[1]                                                                                           | Can be left<br>unconnected.                                                                       |
| PS_DDR_DM0 to<br>PS_DDR_DM1 | Connect<br>DM_n[0]/DBI_n[0]<br>to PS_DDR_DM0,<br>DM_n[1]/DBI_n[1]<br>to PS_DDR_DM1,<br>and so on. | Connect<br>DM_n[0]/DBI_n[0]<br>to PS_DDR_DM0,<br>DM_n[1]/DBI_n[1]<br>to PS_DDR_DM1,<br>and so on. | Connect<br>DM_n[0]/DBI_n[0]<br>to PS_DDR_DM0,<br>DM_n[1]/DBI_n[1]<br>to PS_DDR_DM1,<br>and so on. | Connect<br>DM_n[0]/DBI_n[0]<br>to PS_DDR_DM0,<br>DM_n[1]/DBI_n[1]<br>to PS_DDR_DM1,<br>and so on. | Connect<br>DM_n[0]/DBI_n[0]<br>to PS_DDR_DM0,<br>DM_n[1]/DBI_n[1]<br>to PS_DDR_DM1,<br>and so on. |
| PS_DDR_DM2 to<br>PS_DDR_DM3 | Connect<br>DM_n[2]/DBI_n[2]<br>to PS_DDR_DM2,<br>DM_n[3]/DBI_n[3]<br>to PS_DDR_DM3,<br>and so on. | Connect<br>DM_n[2]/DBI_n[2]<br>to PS_DDR_DM2,<br>DM_n[3]/DBI_n[3]<br>to PS_DDR_DM3,<br>and so on. | Connect<br>DM_n[2]/DBI_n[2]<br>to PS_DDR_DM2,<br>DM_n[3]/DBI_n[3]<br>to PS_DDR_DM3,<br>and so on. | Connect<br>DM_n[2]/DBI_n[2]<br>to PS_DDR_DM2,<br>DM_n[3]/DBI_n[3]<br>to PS_DDR_DM3,<br>and so on. | Can be left<br>unconnected.                                                                       |

Table 2-2: DDR4 Supported Pinout Configurations (Cont'd)

| Pin Name                      | DDR4 64-bit<br>1Rank                                                                              | DDR4 64-bit<br>2Rank                                                                              | DDR4 32-bit<br>1Rank                                                             | DDR4 32-bit<br>2Rank                                                             | DDR4 16-bit<br>1Rank                                                            |
|-------------------------------|---------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|----------------------------------------------------------------------------------|---------------------------------------------------------------------------------|
| PS_DDR_DM4 to<br>PS_DDR_DM7   | Connect<br>DM_n[4]/DBI_n[4]<br>to PS_DDR_DM4,<br>DM_n[5]/DBI_n[5]<br>to PS_DDR_DM5,<br>and so on. | Connect<br>DM_n[4]/DBI_n[4]<br>to PS_DDR_DM4,<br>DM_n[5]/DBI_n[5]<br>to PS_DDR_DM5,<br>and so on. | Can be left<br>unconnected.                                                      | Can be left<br>unconnected.                                                      | Can be left<br>unconnected.                                                     |
| PS_DDR_DM8                    | DM_n[8]/DBI_n[8],<br>can be left<br>unconnected<br>without ECC.                                   | DM_n[8]/DBI_n[8],<br>can be left<br>unconnected<br>without ECC.                                   | DM_n[4]/DBI_n[4],<br>can be left<br>unconnected<br>without ECC.                  | DM_n[4]/DBI_n[4],<br>can be left<br>unconnected<br>without ECC.                  | DM_n[2]/DBI_n[2]<br>can be left<br>unconnected<br>without ECC.                  |
| PS_DDR_DQ0 to<br>PS_DDR_DQ15  | Connect DQ0 to<br>PS_DDR_DQ0, DQ1<br>to PS_DDR_DQ1,<br>and so on.                                 | Connect DQ0 to<br>PS_DDR_DQ0, DQ1<br>to PS_DDR_DQ1,<br>and so on.                                 | Connect DQ0 to<br>PS_DDR_DQ0, DQ1<br>to PS_DDR_DQ1,<br>and so on.                | Connect DQ0 to<br>PS_DDR_DQ0, DQ1<br>to PS_DDR_DQ1,<br>and so on.                | Connect DQ0 to<br>PS_DDR_DQ0,<br>to PS_DDR_DQ1<br>and so on.                    |
| PS_DDR_DQ16 to<br>PS_DDR_DQ31 | Connect DQ16 to<br>PS_DDR_DQ16,<br>DQ17 to<br>PS_DDR_DQ17, and<br>so on.                          | Connect DQ16 to<br>PS_DDR_DQ16,<br>DQ17 to<br>PS_DDR_DQ17, and<br>so on.                          | Connect DQ16 to<br>PS_DDR_DQ16,<br>DQ17 to<br>PS_DDR_DQ17, and<br>so on.         | Connect DQ16 to<br>PS_DDR_DQ16,<br>DQ17 to<br>PS_DDR_DQ17, and<br>so on.         | Can be left<br>unconnected. Do<br>not swap with<br>PS_DDR_DQ0 to<br>PS_DDR_DQ15 |
| PS_DDR_DQ32 to<br>PS_DDR_DQ63 | Connect DQ32 to<br>PS_DDR_DQ32,<br>DQ33 to<br>PS_DDR_DQ33, and<br>so on.                          | Connect DQ32 to<br>PS_DDR_DQ32,<br>DQ33 to<br>PS_DDR_DQ33, and<br>so on.                          | Can be left<br>unconnected. Do<br>not swap with<br>PS_DDR_DQ0 to<br>PS_DDR_DQ31. | Can be left<br>unconnected. Do<br>not swap with<br>PS_DDR_DQ0 to<br>PS_DDR_DQ31. | Can be left<br>unconnected. Do<br>not swap with<br>PS_DDR_DQ0 to<br>PS_DDR_DQ31 |
| PS_DDR_DQ64                   | ECC_bit[0], can be<br>left unconnected<br>without ECC.                                            | ECC_bit[0], can be<br>left unconnected<br>without ECC.                                            | ECC_bit[0], can be<br>left unconnected<br>without ECC.                           | ECC_bit[0], can be<br>left unconnected<br>without ECC.                           | ECC_bit[0], can<br>left unconnect<br>without ECC.                               |
| PS_DDR_DQ65                   | ECC_bit[1], can be<br>left unconnected<br>without ECC.                                            | ECC_bit[1], can be<br>left unconnected<br>without ECC.                                            | ECC_bit[1], can be<br>left unconnected<br>without ECC.                           | ECC_bit[1], can be<br>left unconnected<br>without ECC.                           | ECC_bit[1], can<br>left unconnect<br>without ECC.                               |

Table 2-2: DDR4 Supported Pinout Configurations (Cont'd)

| Pin Name                       | DDR4 64-bit<br>1Rank                                                 | DDR4 64-bit<br>2Rank                                                 | DDR4 32-bit<br>1Rank                                                 | DDR4 32-bit<br>2Rank                                                 | DDR4 16-bit<br>1Rank                                                 |
|--------------------------------|----------------------------------------------------------------------|----------------------------------------------------------------------|----------------------------------------------------------------------|----------------------------------------------------------------------|----------------------------------------------------------------------|
| PS_DDR_DQ66                    | ECC_bit[2], can be left unconnected without ECC.                     | ECC_bit[2], can be left unconnected without ECC.                     | ECC_bit[2], can be left unconnected without ECC.                     | ECC_bit[2], can be left unconnected without ECC.                     | ECC_bit[2], can be left unconnected without ECC.                     |
| PS_DDR_DQ67                    | ECC_bit[3], can be left unconnected without ECC.                     | ECC_bit[3], can be left unconnected without ECC.                     | ECC_bit[3], can be left unconnected without ECC.                     | ECC_bit[3], can be left unconnected without ECC.                     | ECC_bit[3], can be left unconnected without ECC.                     |
| PS_DDR_DQ68                    | ECC_bit[4], can be left unconnected without ECC.                     | ECC_bit[4], can be left unconnected without ECC.                     | ECC_bit[4], can be left unconnected without ECC.                     | ECC_bit[4], can be left unconnected without ECC.                     | ECC_bit[4], can be left unconnected without ECC.                     |
| PS_DDR_DQ69                    | ECC_bit[5], can be left unconnected without ECC.                     | ECC_bit[5], can be left unconnected without ECC.                     | ECC_bit[5], can be left unconnected without ECC.                     | ECC_bit[5], can be left unconnected without ECC.                     | ECC_bit[5], can be left unconnected without ECC.                     |
| PS_DDR_DQ70                    | ECC_bit[6], can be left unconnected without ECC.                     | ECC_bit[6], can be left unconnected without ECC.                     | ECC_bit[6], can be left unconnected without ECC.                     | ECC_bit[6], can be left unconnected without ECC.                     | ECC_bit[6], can be left unconnected without ECC.                     |
| PS_DDR_DQ71                    | ECC_bit[7], can be left unconnected without ECC.                     | ECC_bit[7], can be left unconnected without ECC.                     | ECC_bit[7], can be left unconnected without ECC.                     | ECC_bit[7], can be left unconnected without ECC.                     | ECC_bit[7], can be left unconnected without ECC.                     |
| PS_DDR_DQS_N0 to PS_DDR_DQS_N1 | Connect DQS_c0 to PS_DDR_DQS_N0, DQS_c1 to PS_DDR_DQS_N1, and so on. | Connect DQS_c0 to PS_DDR_DQS_N0, DQS_c1 to PS_DDR_DQS_N1, and so on. | Connect DQS_c0 to PS_DDR_DQS_N0, DQS_c1 to PS_DDR_DQS_N1, and so on. | Connect DQS_c0 to PS_DDR_DQS_N0, DQS_c1 to PS_DDR_DQS_N1, and so on. | Connect DQS_c0 to PS_DDR_DQS_N0, DQS_c1 to PS_DDR_DQS_N1, and so on. |
| PS_DDR_DQS_N2 to PS_DDR_DQS_N3 | Connect DQS_c2 to PS_DDR_DQS_N2, DQS_c3 to PS_DDR_DQS_N3, and so on. | Connect DQS_c2 to PS_DDR_DQS_N2, DQS_c3 to PS_DDR_DQS_N3, and so on. | Connect DQS_c2 to PS_DDR_DQS_N2, DQS_c3 to PS_DDR_DQS_N3, and so on. | Connect DQS_c2 to PS_DDR_DQS_N2, DQS_c3 to PS_DDR_DQS_N3, and so on. | Can be left unconnected.                                             |



Table 2-2: DDR4 Supported Pinout Configurations (Cont'd)

| Pin Name                          | DDR4 64-bit<br>1Rank                                                             | DDR4 64-bit<br>2Rank                                                             | DDR4 32-bit<br>1Rank                                                             | DDR4 32-bit<br>2Rank                                                             | DDR4 16-bit<br>1Rank                                                             |
|-----------------------------------|----------------------------------------------------------------------------------|----------------------------------------------------------------------------------|----------------------------------------------------------------------------------|----------------------------------------------------------------------------------|----------------------------------------------------------------------------------|
| PS_DDR_DQS_N4 to<br>PS_DDR_DQS_N7 | Connect DQS_c4 to<br>PS_DDR_DQS_N4,<br>DQS_c5 to<br>PS_DDR_DQS_N5,<br>and so on. | Connect DQS_c4 to<br>PS_DDR_DQS_N4,<br>DQS_c5 to<br>PS_DDR_DQS_N5,<br>and so on. | Can be left<br>unconnected.                                                      | Can be left<br>unconnected.                                                      | Can be left<br>unconnected.                                                      |
| PS_DDR_DQS_N8                     | DQS_c8, can be left<br>unconnected<br>without ECC.                               | DQS_c8, can be left<br>unconnected<br>without ECC.                               | DQS_c4, can be left<br>unconnected<br>without ECC.                               | DQS_c4, can be left<br>unconnected<br>without ECC.                               | DQS_c2, can be<br>unconnected<br>without ECC.                                    |
| PS_DDR_DQS_P0 to<br>PS_DDR_DQS_P1 | Connect DQS_t0 to<br>PS_DDR_DQS_P0,<br>DQS_t1 to<br>PS_DDR_DQS_P1,<br>and so on. | Connect DQS_t0 to<br>PS_DDR_DQS_P0,<br>DQS_t1 to<br>PS_DDR_DQS_P1,<br>and so on. | Connect DQS_t0 to<br>PS_DDR_DQS_P0,<br>DQS_t1 to<br>PS_DDR_DQS_P1,<br>and so on. | Connect DQS_t0 to<br>PS_DDR_DQS_P0,<br>DQS_t1 to<br>PS_DDR_DQS_P1,<br>and so on. | Connect DQS_t0 to<br>PS_DDR_DQS_P0,<br>DQS_t1 to<br>PS_DDR_DQS_P1,<br>and so on. |
| PS_DDR_DQS_P2 to<br>PS_DDR_DQS_P3 | Connect DQS_t2 to<br>PS_DDR_DQS_P2,<br>DQS_t3 to<br>PS_DDR_DQS_P3,<br>and so on. | Connect DQS_t2 to<br>PS_DDR_DQS_P2,<br>DQS_t3 to<br>PS_DDR_DQS_P3,<br>and so on. | Connect DQS_t2 to<br>PS_DDR_DQS_P2,<br>DQS_t3 to<br>PS_DDR_DQS_P3,<br>and so on. | Connect DQS_t2 to<br>PS_DDR_DQS_P2,<br>DQS_t3 to<br>PS_DDR_DQS_P3,<br>and so on. | Can be left<br>unconnected.                                                      |
| PS_DDR_DQS_P4 to<br>PS_DDR_DQS_P7 | Connect DQS_t4 to<br>PS_DDR_DQS_P4,<br>DQS_t5 to<br>PS_DDR_DQS_P5,<br>and so on. | Connect DQS_t4 to<br>PS_DDR_DQS_P4,<br>DQS_t5 to<br>PS_DDR_DQS_P5,<br>and so on. | Can be left<br>unconnected.                                                      | Can be left<br>unconnected.                                                      | Can be left<br>unconnected.                                                      |
| PS_DDR_DQS_P8                     | DQS_t8, can be left<br>unconnected<br>without ECC.                               | DQS_t8, can be left<br>unconnected<br>without ECC.                               | DQS_t4, can be left<br>unconnected<br>without ECC.                               | DQS_t4, can be left<br>unconnected<br>without ECC.                               | DQS_t2, can be<br>unconnected<br>without ECC.                                    |
| PS_DDR_ODT0                       | ODT                                                                              | ODT[0]                                                                           | ODT                                                                              | ODT[0]                                                                           | ODT                                                                              |
| PS_DDR_ODT1                       | Can be left<br>unconnected.                                                      | ODT[1]                                                                           | Can be left<br>unconnected.                                                      | ODT[1]                                                                           | Can be left<br>unconnected.                                                      |
| PS_DDR_PARITY                     | PAR                                                                              | PAR                                                                              | PAR                                                                              | PAR                                                                              | PAR                                                                              |
| PS_DDR_RAM_RST_N                  | RESET_n                                                                          | RESET_n                                                                          | RESET_n                                                                          | RESET_n                                                                          | RESET_n                                                                          |

Table 2-2: DDR4 Supported Pinout Configurations (Cont'd)

| Pin Name  | DDR4 64-bit<br>1Rank                                                                          | DDR4 64-bit<br>2Rank                                                                          | DDR4 32-bit<br>1Rank                                                                          | DDR4 32-bit<br>2Rank                                                                          | DDR4 16-bit<br>1Rank                                                                          |
|-----------|-----------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|
| PS_DDR_ZQ | Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VSSQ through a 240Ω resistor. | Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VSSQ through a 240Ω resistor. | Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VSSQ through a 240Ω resistor. | Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VSSQ through a 240Ω resistor. | Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VSSQ through a 240Ω resistor. |

Notes:

1. For VCCQ\_PSDDR decoupling guidelines, see the *UltraScale Architecture PCB Design Guide* ([UG583](#)).
2. The PS\_DDR\_BG1 pin can be left unconnected when targeting x16 component interfaces without a BG1 pin, but it should always be connected.

## LPDDR4 Guidelines

### LPDDR4 Pin Rules

The LPDDR4 pin rules are for single and dual-rank memory interfaces.

- All unused DDR pins can be left unconnected. For example, in an 64-bit interface without ECC, the PS\_DDR\_DQ64 to PS\_DDR\_DQ71, PS\_DDR\_DQS\_P8/N8, and PS\_DDR\_DM8 pins can be left unconnected.
- Connect the PS\_DDR\_ZQ pin to GND using a 240Ω resistor. There should be separate 240Ω resistors at the FPGA and at the DRAM.
- To achieve maximum performance, address copy mode is suggested.

### LPDDR4 Pin Swapping Restrictions

- Command/address bits cannot be swapped.
- To support write DQS to DQ training, DQ byte lane swapping is not allowed.
- To support write DQS to DQ training, DQ bits with bytes 0, 2, and 8 are not allowed to be swapped.
- Bits within bytes 1 and 3 can be swapped.

### LPDDR4 Pinout Example for Supported Configurations

Table 2-3 shows a pinout example for the LPDDR4 supported configurations. For termination details, see the *UltraScale Architecture PCB Design Guide* (UG583). When not being used for a memory interface, all pins should be left unconnected with the exception of VCCO\_PSDDR and VCC\_PSDDR\_PLL, which should be tied to GND.



**IMPORTANT:** VCC\_PSINTFP must be tied to VCC\_PSINTFP\_DDR. This requirement is in Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics (DS925) and Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics (DS926), where both VCC\_PSINTFP and VCC\_PSINTFP\_DDR must be connected to the same supply and thus both must be powered to avoid MBIST failure.

Table 2-3: LPDDR4 Supported Pinout Configurations

| Pin Name                  | LPDDR4 32-bit 1Rank | LPDDR4 32-bit 1Rank ECC | LPDDR4 32-bit 2Rank | LPDDR4 32-bit 2Rank ECC |
|---------------------------|---------------------|-------------------------|---------------------|-------------------------|
| VCCO_PSDDR <sup>(1)</sup> | Set to 1.1V         | Set to 1.1V             | Set to 1.1V         | Set to 1.1V             |
| PS_DDR_A0                 | CA0_A               | CA0_A                   | CA0_A               | CA0_A                   |
| PS_DDR_A1                 | CA1_A               | CA1_A                   | CA1_A               | CA1_A                   |
| PS_DDR_A2                 | CA2_A               | CA2_A                   | CA2_A               | CA2_A                   |



Table 2-3: LPDDR4 Supported Pinout Configurations (Cont'd)

| Pin Name               | LPDDR4 32-bit 1Rank      | LPDDR4 32-bit 1Rank ECC  | LPDDR4 32-bit 2Rank      | LPDDR4 32-bit 2Rank ECC  |
|------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| PS_DDR_A3              | CA3_A                    | CA3_A                    | CA3_A                    | CA3_A                    |
| PS_DDR_A4              | CA4_A                    | CA4_A                    | CA4_A                    | CA4_A                    |
| PS_DDR_A5              | CA5_A                    | CA5_A                    | CA5_A                    | CA5_A                    |
| PS_DDR_A6 to PS_DDR_A9 | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. |
| PS_DDR_A10             | CA0_B                    | CA0_B                    | CA0_B                    | CA0_B                    |
| PS_DDR_A11             | CA1_B                    | CA1_B                    | CA1_B                    | CA1_B                    |
| PS_DDR_A12             | CA2_B                    | CA2_B                    | CA2_B                    | CA2_B                    |
| PS_DDR_A13             | CA3_B                    | CA3_B                    | CA3_B                    | CA3_B                    |
| PS_DDR_A14             | CA4_B                    | CA4_B                    | CA4_B                    | CA4_B                    |
| PS_DDR_A15             | CA5_B                    | CA5_B                    | CA5_B                    | CA5_B                    |
| PS_DDR_A16             | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. |
| PS_DDR_A17             | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. |
| PS_DDR_ACT_N           | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. |
| PS_DDR_ALERT_N         | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. |
| PS_DDR_BA0             | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. |
| PS_DDR_BA1             | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. |
| PS_DDR_BG0             | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. |
| PS_DDR_BG1             | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. | Can be left unconnected. |
| PS_DDR_CK_N0           | CK_c_A                   | CK_c_A                   | CK_c_A                   | CK_c_A                   |
| PS_DDR_CK_N1           | CK_c_B                   | CK_c_B                   | CK_c_B                   | CK_c_B                   |
| PS_DDR_CK0             | CK_t_A                   | CK_t_A                   | CK_t_A                   | CK_t_A                   |
| PS_DDR_CK1             | CK_t_B                   | CK_t_B                   | CK_t_B                   | CK_t_B                   |
| PS_DDR_CKE0            | CKE_A and CKE_B          | CKE_A                    | CKE0_A and CKE0_B        | CKE0_A                   |
| PS_DDR_CKE1            | Can be left unconnected. | Can be left unconnected. | CKE1_A and CKE1_B        | CKE1_A                   |
| PS_DDR_CS_N0           | CS_A and CS_B            | CS_A                     | CS0_A and CS0_B          | CS0_A                    |
| PS_DDR_CS_N1           | Can be left unconnected. | Can be left unconnected. | CS1_A and CS1_B          | CS1_A                    |
| PS_DDR_DM0             | DMI0_A                   | DMI0_A                   | DMI0_A                   | DMI0_A                   |

Table 2-3: LPDDR4 Supported Pinout Configurations (Cont'd)

| Pin Name                       | LPDDR4 32-bit 1Rank                                            | LPDDR4 32-bit 1Rank ECC                                        | LPDDR4 32-bit 2Rank                                            | LPDDR4 32-bit 2Rank ECC                                        |
|--------------------------------|----------------------------------------------------------------|----------------------------------------------------------------|----------------------------------------------------------------|----------------------------------------------------------------|
| PS_DDR_DM1                     | DMI1_A                                                         | DMI1_A                                                         | DMI1_A                                                         | DMI1_A                                                         |
| PS_DDR_DM2                     | DMI0_B                                                         | DMI0_B                                                         | DMI0_B                                                         | DMI0_B                                                         |
| PS_DDR_DM3                     | DMI1_B                                                         | DMI1_B                                                         | DMI1_B                                                         | DMI1_B                                                         |
| PS_DDR_DM4 to PS_DDR_DM7       | Can be left unconnected.                                       | Can be left unconnected.                                       | Can be left unconnected.                                       | Can be left unconnected.                                       |
| PS_DDR_DM8                     | Can be left unconnected.                                       | DMI_ECC                                                        | Can be left unconnected.                                       | DMI_ECC                                                        |
| PS_DDR_DQ0 to PS_DDR_DQ15      | Connect DQ0_A to PS_DDR_DQ0, DQ1_A to PS_DDR_DQ1, and so on.   | Connect DQ0_A to PS_DDR_DQ0, DQ1_A to PS_DDR_DQ1, and so on.   | Connect DQ0_A to PS_DDR_DQ0, DQ1_A to PS_DDR_DQ1, and so on.   | Connect DQ0_A to PS_DDR_DQ0, DQ1_A to PS_DDR_DQ1, and so on.   |
| PS_DDR_DQ16 to PS_DDR_DQ31     | Connect DQ0_B to PS_DDR_DQ16, DQ1_B to PS_DDR_DQ17, and so on. | Connect DQ0_B to PS_DDR_DQ16, DQ1_B to PS_DDR_DQ17, and so on. | Connect DQ0_B to PS_DDR_DQ16, DQ1_B to PS_DDR_DQ17, and so on. | Connect DQ0_B to PS_DDR_DQ16, DQ1_B to PS_DDR_DQ17, and so on. |
| PS_DDR_DQ32 to PS_DDR_DQ63     | Can be left unconnected.                                       | Can be left unconnected.                                       | Can be left unconnected.                                       | Can be left unconnected.                                       |
| PS_DDR_DQ64                    | Can be left unconnected.                                       | DQ_ECC0 (ECC_bit[0])                                           | Can be left unconnected.                                       | DQ_ECC0 (ECC_bit[0])                                           |
| PS_DDR_DQ65                    | Can be left unconnected.                                       | DQ_ECC1 (ECC_bit[1])                                           | Can be left unconnected.                                       | DQ_ECC1 (ECC_bit[1])                                           |
| PS_DDR_DQ66                    | Can be left unconnected.                                       | DQ_ECC2 (ECC_bit[2])                                           | Can be left unconnected.                                       | DQ_ECC2 (ECC_bit[2])                                           |
| PS_DDR_DQ67                    | Can be left unconnected.                                       | DQ_ECC3 (ECC_bit[3])                                           | Can be left unconnected.                                       | DQ_ECC3 (ECC_bit[3])                                           |
| PS_DDR_DQ68                    | Can be left unconnected.                                       | DQ_ECC4 (ECC_bit[4])                                           | Can be left unconnected.                                       | DQ_ECC4 (ECC_bit[4])                                           |
| PS_DDR_DQ69                    | Can be left unconnected.                                       | DQ_ECC5 (ECC_bit[5])                                           | Can be left unconnected.                                       | DQ_ECC5 (ECC_bit[5])                                           |
| PS_DDR_DQ70                    | Can be left unconnected.                                       | DQ_ECC6 (ECC_bit[6])                                           | Can be left unconnected.                                       | DQ_ECC6 (ECC_bit[6])                                           |
| PS_DDR_DQ71                    | Can be left unconnected.                                       | DQ_ECC7 (ECC_bit[7])                                           | Can be left unconnected.                                       | DQ_ECC7 (ECC_bit[7])                                           |
| PS_DDR_DQS_N0                  | DQS0_c_A                                                       | DQS0_c_A                                                       | DQS0_c_A                                                       | DQS0_c_A                                                       |
| PS_DDR_DQS_N1                  | DQS1_c_A                                                       | DQS1_c_A                                                       | DQS1_c_A                                                       | DQS1_c_A                                                       |
| PS_DDR_DQS_N2                  | DQS0_c_B                                                       | DQS0_c_B                                                       | DQS0_c_B                                                       | DQS0_c_B                                                       |
| PS_DDR_DQS_N3                  | DQS1_c_B                                                       | DQS1_c_B                                                       | DQS1_c_B                                                       | DQS1_c_B                                                       |
| PS_DDR_DQS_N4 to PS_DDR_DQS_N7 | Can be left unconnected.                                       | Can be left unconnected.                                       | Can be left unconnected.                                       | Can be left unconnected.                                       |

Table 2-3: LPDDR4 Supported Pinout Configurations (Cont'd)

| Pin Name                       | LPDDR4 32-bit 1Rank                                                                           | LPDDR4 32-bit 1Rank ECC                                                                       | LPDDR4 32-bit 2Rank                                                                           | LPDDR4 32-bit 2Rank ECC                                                                       |
|--------------------------------|-----------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------|
| PS_DDR_DQS_N8                  | Can be left unconnected.                                                                      | DQS_c_ECC                                                                                     | Can be left unconnected.                                                                      | DQS_c_ECC                                                                                     |
| PS_DDR_DQS_P0                  | DQS0_t_A                                                                                      | DQS0_t_A                                                                                      | DQS0_t_A                                                                                      | DQS0_t_A                                                                                      |
| PS_DDR_DQS_P1                  | DQS1_t_A                                                                                      | DQS1_t_A                                                                                      | DQS1_t_A                                                                                      | DQS1_t_A                                                                                      |
| PS_DDR_DQS_P2                  | DQS0_t_B                                                                                      | DQS0_t_B                                                                                      | DQS0_t_B                                                                                      | DQS0_t_B                                                                                      |
| PS_DDR_DQS_P3                  | DQS1_t_B                                                                                      | DQS1_t_B                                                                                      | DQS1_t_B                                                                                      | DQS1_t_B                                                                                      |
| PS_DDR_DQS_P4 to PS_DDR_DQS_P7 | Can be left unconnected.                                                                      | Can be left unconnected.                                                                      | Can be left unconnected.                                                                      | Can be left unconnected.                                                                      |
| PS_DDR_DQS_P8                  | Can be left unconnected.                                                                      | DQS_t_ECC                                                                                     | Can be left unconnected.                                                                      | DQS_t_ECC                                                                                     |
| PS_DDR_ODT0                    | Unconnected at FPGA.                                                                          | Unconnected at FPGA.                                                                          | Unconnected at FPGA.                                                                          | Unconnected at FPGA.                                                                          |
| PS_DDR_ODT1                    | Can be left unconnected.                                                                      | Can be left unconnected.                                                                      | Can be left unconnected.                                                                      | Can be left unconnected.                                                                      |
| PS_DDR_PARITY                  | Can be left unconnected.                                                                      | Can be left unconnected.                                                                      | Can be left unconnected.                                                                      | Can be left unconnected.                                                                      |
| PS_DDR_RAM_RST_N               | RESET_n                                                                                       | RESET_n                                                                                       | RESET_n                                                                                       | RESET_n                                                                                       |
| PS_DDR_ZQ                      | Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VDDQ through a 240Ω resistor. | Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VDDQ through a 240Ω resistor. | Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VDDQ through a 240Ω resistor. | Connect to GND through a 240Ω resistor. Connect DRAM ZQ pins to VDDQ through a 240Ω resistor. |

**Notes:**

- For VCCO\_PSDDR decoupling guidelines, see the *UltraScale Architecture PCB Design Guide* ([UG583](#)).

# LPDDR3 Guidelines

## LPDDR3 Pin Rules

The LPDDR3 pin rules are for single and dual-rank memory interfaces.

- All unused DDR pins can be left unconnected. For example, in an 64-bit interface without ECC, the PS\_DDR\_DQ64 to PS\_DDR\_DQ71, PS\_DDR\_DQS\_P8/N8, and PS\_DDR\_DM8 pins can be left unconnected.
- Connect the PS\_DDR\_ZQ pin to GND using a 240Ω resistor. There should be separate 240Ω resistors at the FPGA and at the DRAM.
- To achieve maximum performance, address copy mode is suggested.

## LPDDR3 Pin Swapping Restrictions

- Command/address bits cannot be swapped.
- To support command/address training, DQ byte lane swapping is not allowed.
- To support command/address training, DQ bits swapping within a byte lane is not allowed.

## LPDDR3 Pinout Example for Supported Configurations

Table 2-4 shows a pinout example for the LPDDR3 supported configurations. For termination details, see the *UltraScale Architecture PCB Design Guide* (UG583). When not being used for a memory interface, all pins should be left unconnected with the exception of VCCO\_PSDDR and VCC\_PSDDR\_PLL, which should be tied to GND.



**IMPORTANT:** VCC\_PSINTFP must be tied to VCC\_PSINTFP\_DDR. This requirement is in Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics (DS925) and Zynq UltraScale+ RFSoc Data Sheet: DC and AC Switching Characteristics (DS926), where both VCC\_PSINTFP and VCC\_PSINTFP\_DDR must be connected to the same supply and thus both must be powered to avoid MBIST failure.

Table 2-4: LPDDR3 Supported Pinout Configurations

| Pin Name                  | LPDDR3 64-bit | LPDDR3 64-bit (Dual Rank) | LPDDR3 32-bit (Dual Rank) |
|---------------------------|---------------|---------------------------|---------------------------|
| VCCO_PSDDR <sup>(1)</sup> | Set to 1.2V   | Set to 1.2V               | Set to 1.2V               |
| PS_DDR_A0                 | CA0_A         | CA0_A                     | CA0                       |
| PS_DDR_A1                 | CA1_A         | CA1_A                     | CA1                       |
| PS_DDR_A2                 | CA2_A         | CA2_A                     | CA2                       |
| PS_DDR_A3                 | CA3_A         | CA3_A                     | CA3                       |

Table 2-4: LPDDR3 Supported Pinout Configurations (Cont'd)

| Pin Name       | LPDDR3 64-bit            | LPDDR3 64-bit<br>(Dual Rank) | LPDDR3 32-bit<br>(Dual Rank) |
|----------------|--------------------------|------------------------------|------------------------------|
| PS_DDR_A4      | CA4_A                    | CA4_A                        | CA4                          |
| PS_DDR_A5      | CA5_A                    | CA5_A                        | CA5                          |
| PS_DDR_A6      | CA6_A                    | CA6_A                        | CA6                          |
| PS_DDR_A7      | CA7_A                    | CA7_A                        | CA7                          |
| PS_DDR_A8      | CA8_A                    | CA8_A                        | CA8                          |
| PS_DDR_A9      | CA9_A                    | CA9_A                        | CA9                          |
| PS_DDR_A10     | CA0_B                    | CA0_B                        | Can be left unconnected.     |
| PS_DDR_A11     | CA1_B                    | CA1_B                        | Can be left unconnected.     |
| PS_DDR_A12     | CA2_B                    | CA2_B                        | Can be left unconnected.     |
| PS_DDR_A13     | CA3_B                    | CA3_B                        | Can be left unconnected.     |
| PS_DDR_A14     | CA4_B                    | CA4_B                        | Can be left unconnected.     |
| PS_DDR_A15     | CA5_B                    | CA5_B                        | Can be left unconnected.     |
| PS_DDR_A16     | Can be left unconnected. | Can be left unconnected.     | Can be left unconnected.     |
| PS_DDR_A17     | Can be left unconnected. | Can be left unconnected.     | Can be left unconnected.     |
| PS_DDR_ACT_N   | CA9_B                    | CA9_B                        | Can be left unconnected.     |
| PS_DDR_ALERT_N | Can be left unconnected. | Can be left unconnected.     | Can be left unconnected.     |
| PS_DDR_BA0     | CA6_B                    | CA6_B                        | Can be left unconnected.     |
| PS_DDR_BA1     | CA7_B                    | CA7_B                        | Can be left unconnected.     |
| PS_DDR_BG0     | CA8_B                    | CA8_B                        | Can be left unconnected.     |
| PS_DDR_BG1     | Can be left unconnected. | Can be left unconnected.     | Can be left unconnected.     |
| PS_DDR_CK_N0   | CK_c_A                   | CK_c_A                       | CK_c                         |
| PS_DDR_CK_N1   | CK_c_B                   | CK_c_B                       | Can be left unconnected.     |
| PS_DDR_CK0     | CK_t_A                   | CK_t_A                       | CK_t                         |
| PS_DDR_CK1     | CK_t_B                   | CK_t_B                       | Can be left unconnected.     |
| PS_DDR_CKE0    | CKE_A and CKE_B          | CKE0_A and CKE0_B            | CKE0                         |
| PS_DDR_CKE1    | Can be left unconnected. | CKE1_A and CKE1_B            | CKE1                         |
| PS_DDR_CS_N0   | CS_n_A and CS_n_B        | CS0_n_A and CS0_n_B          | CS0_n                        |
| PS_DDR_CS_N1   | Can be left unconnected. | CS1_n_A and CS1_n_B          | CS1_n                        |
| PS_DDR_DM0     | DM0_A                    | DM0_A                        | DM0                          |
| PS_DDR_DM1     | DM1_A                    | DM1_A                        | DM1                          |
| PS_DDR_DM2     | DM2_A                    | DM2_A                        | DM2                          |
| PS_DDR_DM3     | DM3_A                    | DM3_A                        | DM3                          |
| PS_DDR_DM4     | DM0_B                    | DM0_B                        | Can be left unconnected.     |
| PS_DDR_DM5     | DM1_B                    | DM1_B                        | Can be left unconnected.     |

Table 2-4: LPDDR3 Supported Pinout Configurations (Cont'd)

| Pin Name    | LPDDR3 64-bit                                | LPDDR3 64-bit<br>(Dual Rank)                 | LPDDR3 32-bit<br>(Dual Rank)                 |
|-------------|----------------------------------------------|----------------------------------------------|----------------------------------------------|
| PS_DDR_DM6  | DM2_B                                        | DM2_B                                        | Can be left unconnected.                     |
| PS_DDR_DM7  | DM3_B                                        | DM3_B                                        | Can be left unconnected.                     |
| PS_DDR_DM8  | DM_ECC, can be left unconnected without ECC. | DM_ECC, can be left unconnected without ECC. | DM_ECC, can be left unconnected without ECC. |
| PS_DDR_DQ0  | DQ0_A                                        | DQ0_A                                        | DQ0                                          |
| PS_DDR_DQ1  | DQ1_A                                        | DQ1_A                                        | DQ1                                          |
| PS_DDR_DQ2  | DQ2_A                                        | DQ2_A                                        | DQ2                                          |
| PS_DDR_DQ3  | DQ3_A                                        | DQ3_A                                        | DQ3                                          |
| PS_DDR_DQ4  | DQ4_A                                        | DQ4_A                                        | DQ4                                          |
| PS_DDR_DQ5  | DQ5_A                                        | DQ5_A                                        | DQ5                                          |
| PS_DDR_DQ6  | DQ6_A                                        | DQ6_A                                        | DQ6                                          |
| PS_DDR_DQ7  | DQ7_A                                        | DQ7_A                                        | DQ7                                          |
| PS_DDR_DQ8  | DQ8_A                                        | DQ8_A                                        | DQ8                                          |
| PS_DDR_DQ9  | DQ9_A                                        | DQ9_A                                        | DQ9                                          |
| PS_DDR_DQ10 | DQ10_A                                       | DQ10_A                                       | DQ10                                         |
| PS_DDR_DQ11 | DQ11_A                                       | DQ11_A                                       | DQ11                                         |
| PS_DDR_DQ12 | DQ12_A                                       | DQ12_A                                       | DQ12                                         |
| PS_DDR_DQ13 | DQ13_A                                       | DQ13_A                                       | DQ13                                         |
| PS_DDR_DQ14 | DQ14_A                                       | DQ14_A                                       | DQ14                                         |
| PS_DDR_DQ15 | DQ15_A                                       | DQ15_A                                       | DQ15                                         |
| PS_DDR_DQ16 | DQ16_A                                       | DQ16_A                                       | DQ16                                         |
| PS_DDR_DQ17 | DQ17_A                                       | DQ17_A                                       | DQ17                                         |
| PS_DDR_DQ18 | DQ18_A                                       | DQ18_A                                       | DQ18                                         |
| PS_DDR_DQ19 | DQ19_A                                       | DQ19_A                                       | DQ19                                         |
| PS_DDR_DQ20 | DQ20_A                                       | DQ20_A                                       | DQ20                                         |
| PS_DDR_DQ21 | DQ21_A                                       | DQ21_A                                       | DQ21                                         |
| PS_DDR_DQ22 | DQ22_A                                       | DQ22_A                                       | DQ22                                         |
| PS_DDR_DQ23 | DQ23_A                                       | DQ23_A                                       | DQ23                                         |
| PS_DDR_DQ24 | DQ24_A                                       | DQ24_A                                       | DQ24                                         |
| PS_DDR_DQ25 | DQ25_A                                       | DQ25_A                                       | DQ25                                         |
| PS_DDR_DQ26 | DQ26_A                                       | DQ26_A                                       | DQ26                                         |
| PS_DDR_DQ27 | DQ27_A                                       | DQ27_A                                       | DQ27                                         |
| PS_DDR_DQ28 | DQ28_A                                       | DQ28_A                                       | DQ28                                         |
| PS_DDR_DQ29 | DQ29_A                                       | DQ29_A                                       | DQ29                                         |

Table 2-4: LPDDR3 Supported Pinout Configurations (Cont'd)

| Pin Name    | LPDDR3 64-bit | LPDDR3 64-bit<br>(Dual Rank) | LPDDR3 32-bit<br>(Dual Rank) |
|-------------|---------------|------------------------------|------------------------------|
| PS_DDR_DQ30 | DQ30_A        | DQ30_A                       | DQ30                         |
| PS_DDR_DQ31 | DQ31_A        | DQ31_A                       | DQ31                         |
| PS_DDR_DQ32 | DQ0_B         | DQ0_B                        | Can be left unconnected.     |
| PS_DDR_DQ33 | DQ1_B         | DQ1_B                        | Can be left unconnected.     |
| PS_DDR_DQ34 | DQ2_B         | DQ2_B                        | Can be left unconnected.     |
| PS_DDR_DQ35 | DQ3_B         | DQ3_B                        | Can be left unconnected.     |
| PS_DDR_DQ36 | DQ4_B         | DQ4_B                        | Can be left unconnected.     |
| PS_DDR_DQ37 | DQ5_B         | DQ5_B                        | Can be left unconnected.     |
| PS_DDR_DQ38 | DQ6_B         | DQ6_B                        | Can be left unconnected.     |
| PS_DDR_DQ39 | DQ7_B         | DQ7_B                        | Can be left unconnected.     |
| PS_DDR_DQ40 | DQ8_B         | DQ8_B                        | Can be left unconnected.     |
| PS_DDR_DQ41 | DQ9_B         | DQ9_B                        | Can be left unconnected.     |
| PS_DDR_DQ42 | DQ10_B        | DQ10_B                       | Can be left unconnected.     |
| PS_DDR_DQ43 | DQ11_B        | DQ11_B                       | Can be left unconnected.     |
| PS_DDR_DQ44 | DQ12_B        | DQ12_B                       | Can be left unconnected.     |
| PS_DDR_DQ45 | DQ13_B        | DQ13_B                       | Can be left unconnected.     |
| PS_DDR_DQ46 | DQ14_B        | DQ14_B                       | Can be left unconnected.     |
| PS_DDR_DQ47 | DQ15_B        | DQ15_B                       | Can be left unconnected.     |
| PS_DDR_DQ48 | DQ16_B        | DQ16_B                       | Can be left unconnected.     |
| PS_DDR_DQ49 | DQ17_B        | DQ17_B                       | Can be left unconnected.     |
| PS_DDR_DQ50 | DQ18_B        | DQ18_B                       | Can be left unconnected.     |
| PS_DDR_DQ51 | DQ19_B        | DQ19_B                       | Can be left unconnected.     |
| PS_DDR_DQ52 | DQ20_B        | DQ20_B                       | Can be left unconnected.     |
| PS_DDR_DQ53 | DQ21_B        | DQ21_B                       | Can be left unconnected.     |
| PS_DDR_DQ54 | DQ22_B        | DQ22_B                       | Can be left unconnected.     |
| PS_DDR_DQ55 | DQ23_B        | DQ23_B                       | Can be left unconnected.     |
| PS_DDR_DQ56 | DQ24_B        | DQ24_B                       | Can be left unconnected.     |
| PS_DDR_DQ57 | DQ25_B        | DQ25_B                       | Can be left unconnected.     |
| PS_DDR_DQ58 | DQ26_B        | DQ26_B                       | Can be left unconnected.     |
| PS_DDR_DQ59 | DQ27_B        | DQ27_B                       | Can be left unconnected.     |
| PS_DDR_DQ60 | DQ28_B        | DQ28_B                       | Can be left unconnected.     |
| PS_DDR_DQ61 | DQ29_B        | DQ29_B                       | Can be left unconnected.     |
| PS_DDR_DQ62 | DQ30_B        | DQ30_B                       | Can be left unconnected.     |
| PS_DDR_DQ63 | DQ31_B        | DQ31_B                       | Can be left unconnected.     |

Table 2-4: LPDDR3 Supported Pinout Configurations (Cont'd)

| Pin Name      | LPDDR3 64-bit                                              | LPDDR3 64-bit<br>(Dual Rank)                               | LPDDR3 32-bit<br>(Dual Rank)                               |
|---------------|------------------------------------------------------------|------------------------------------------------------------|------------------------------------------------------------|
| PS_DDR_DQ64   | DQ_ECC0 (ECC_bit[0]), can be left unconnected without ECC. | DQ_ECC0 (ECC_bit[0]), can be left unconnected without ECC. | DQ_ECC0 (ECC_bit[0]), can be left unconnected without ECC. |
| PS_DDR_DQ65   | DQ_ECC1 (ECC_bit[1]), can be left unconnected without ECC. | DQ_ECC1 (ECC_bit[1]), can be left unconnected without ECC. | DQ_ECC1 (ECC_bit[1]), can be left unconnected without ECC. |
| PS_DDR_DQ66   | DQ_ECC2 (ECC_bit[2]), can be left unconnected without ECC. | DQ_ECC2 (ECC_bit[2]), can be left unconnected without ECC. | DQ_ECC2 (ECC_bit[2]), can be left unconnected without ECC. |
| PS_DDR_DQ67   | DQ_ECC3 (ECC_bit[3]), can be left unconnected without ECC. | DQ_ECC3 (ECC_bit[3]), can be left unconnected without ECC. | DQ_ECC3 (ECC_bit[3]), can be left unconnected without ECC. |
| PS_DDR_DQ68   | DQ_ECC4 (ECC_bit[4]), can be left unconnected without ECC. | DQ_ECC4 (ECC_bit[4]), can be left unconnected without ECC. | DQ_ECC4 (ECC_bit[4]), can be left unconnected without ECC. |
| PS_DDR_DQ69   | DQ_ECC5 (ECC_bit[5]), can be left unconnected without ECC. | DQ_ECC5 (ECC_bit[5]), can be left unconnected without ECC. | DQ_ECC5 (ECC_bit[5]), can be left unconnected without ECC. |
| PS_DDR_DQ70   | DQ_ECC6 (ECC_bit[6]), can be left unconnected without ECC. | DQ_ECC6 (ECC_bit[6]), can be left unconnected without ECC. | DQ_ECC6 (ECC_bit[6]), can be left unconnected without ECC. |
| PS_DDR_DQ71   | DQ_ECC7 (ECC_bit[7]), can be left unconnected without ECC. | DQ_ECC7 (ECC_bit[7]), can be left unconnected without ECC. | DQ_ECC7 (ECC_bit[7]), can be left unconnected without ECC. |
| PS_DDR_DQS_N0 | DQS0_c_A                                                   | DQS0_c_A                                                   | DQS0_c                                                     |
| PS_DDR_DQS_N1 | DQS1_c_A                                                   | DQS1_c_A                                                   | DQS1_c                                                     |
| PS_DDR_DQS_N2 | DQS2_c_A                                                   | DQS2_c_A                                                   | DQS2_c                                                     |
| PS_DDR_DQS_N3 | DQS3_c_A                                                   | DQS3_c_A                                                   | DQS3_c                                                     |
| PS_DDR_DQS_N4 | DQS0_c_B                                                   | DQS0_c_B                                                   | Can be left unconnected.                                   |
| PS_DDR_DQS_N5 | DQS1_c_B                                                   | DQS1_c_B                                                   | Can be left unconnected.                                   |
| PS_DDR_DQS_N6 | DQS2_c_B                                                   | DQS2_c_B                                                   | Can be left unconnected.                                   |
| PS_DDR_DQS_N7 | DQS3_c_B                                                   | DQS3_c_B                                                   | Can be left unconnected.                                   |
| PS_DDR_DQS_N8 | DQS_c_ECC, can be left unconnected without ECC.            | DQS_c_ECC, can be left unconnected without ECC.            | DQS_c_ECC, can be left unconnected without ECC.            |
| PS_DDR_DQS_P0 | DQS0_t_A                                                   | DQS0_t_A                                                   | DQS0_t                                                     |
| PS_DDR_DQS_P1 | DQS1_t_A                                                   | DQS1_t_A                                                   | DQS1_t                                                     |
| PS_DDR_DQS_P2 | DQS2_t_A                                                   | DQS2_t_A                                                   | DQS2_t                                                     |
| PS_DDR_DQS_P3 | DQS3_t_A                                                   | DQS3_t_A                                                   | DQS3_t                                                     |
| PS_DDR_DQS_P4 | DQS0_t_B                                                   | DQS0_t_B                                                   | Can be left unconnected.                                   |
| PS_DDR_DQS_P5 | DQS1_t_B                                                   | DQS1_t_B                                                   | Can be left unconnected.                                   |



Table 2-4: LPDDR3 Supported Pinout Configurations (Cont'd)

| Pin Name         | LPDDR3 64-bit                                   | LPDDR3 64-bit<br>(Dual Rank)                    | LPDDR3 32-bit<br>(Dual Rank)                    |
|------------------|-------------------------------------------------|-------------------------------------------------|-------------------------------------------------|
| PS_DDR_DQS_P6    | DQS2_t_B                                        | DQS2_t_B                                        | Can be left unconnected.                        |
| PS_DDR_DQS_P7    | DQS3_t_B                                        | DQS3_t_B                                        | Can be left unconnected.                        |
| PS_DDR_DQS_P8    | DQS_t_ECC, can be left unconnected without ECC. | DQS_t_ECC, can be left unconnected without ECC. | DQS_t_ECC, can be left unconnected without ECC. |
| PS_DDR_ODT0      | ODT_A and ODT_B                                 | ODT_A and ODT_B                                 | ODT                                             |
| PS_DDR_ODT1      | Can be left unconnected.                        | Can be left unconnected.                        | Can be left unconnected.                        |
| PS_DDR_PARITY    | Can be left unconnected.                        | Can be left unconnected.                        | Can be left unconnected.                        |
| PS_DDR_RAM_RST_N | Can be left unconnected.                        | Can be left unconnected.                        | Can be left unconnected.                        |
| PS_DDR_ZQ        | Connect a 240Ω resistor to GND. <sup>(2)</sup>  | Connect a 240Ω resistor to GND. <sup>(2)</sup>  | Connect a 240Ω resistor to GND. <sup>(2)</sup>  |

**Notes:**

1. For VCCO\_PSDDR decoupling guidelines, see the *UltraScale Architecture PCB Design Guide* ([UG583](#)).
2. There should be separate 240Ω resistors at the FPGA and at the DRAM.

# Package Files

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## About ASCII Package Files

The ASCII package files for each Zynq™ UltraScale+™ device include a comma-separated-values (CSV) version and a text version optimized for a browser or text editor in fixed-width fonts. The information in each of the files includes:

- Device/Package name (*family-device-package*), with date and time of creation
- Six columns containing data for each pin:
  - Pin—Pin location on the package.
  - Pin Name—The name of the assigned pin.
  - Memory Byte Group—Memory byte group between 0 and 3 split into upper (U) and lower (L) halves. For more information on the memory byte group, see the *UltraScale Architecture-Based Memory Interface Solutions Product Guide* ([PG150](#)).
  - Bank—Bank number.
  - I/O Type—CONFIG, HD, HP, GTH, GTY, PS-GTR, PSMIO, PSDDR, or PSCONFIG depends on the I/O type. For more information on the I/O type, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).
  - Super Logic Region—Number corresponding to the super logic region (SLR) in the devices implemented with stacked silicon interconnect (SSI) technology.
- Total number of pins in the package.

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## Package Specifications Designations

Package specifications are designated as evaluation only, engineering sample, or production. Each designation is defined as follows.

### Evaluation Only

These package specifications are based on initial device specifications, package routability analysis and mechanical package construction. Package specifications with this designation are not stable and package pinouts are likely to change and these specifications should only be used for initial system level design feasibility.

### Engineering Sample

These package specifications are based on a released package design and validated with ES engineering sample (ES) devices. Package specifications with this designation are considered stable, however some pinout and mechanical specifications might change prior to the production release of the particular device. Package pinouts with this designation are to be used for PCB and Vivado™ designs using ES devices.

### Production

These package specifications are released coincident with production release of a particular device. Customers receive formal notification of any subsequent changes.

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## ASCII Pinout Files

Links to the ASCII pinout information device/package combinations are listed in [Table 3-1](#).

Download all available package/device/pinout files at:

[www.xilinx.com/support/package-pinout-files/zynq-ultrascale-plus-pkgs.html](http://www.xilinx.com/support/package-pinout-files/zynq-ultrascale-plus-pkgs.html)

**Note:** All package files are ASCII files in TXT and CSV file format. Only the available files listed in [Table 3-1](#) are linked and consolidated in this ZIP file:

[www.xilinx.com/support/packagefiles/zuppackages/zupall.zip](http://www.xilinx.com/support/packagefiles/zuppackages/zupall.zip)



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**IMPORTANT:** All non-InFO packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC or XA, and the Pb-free signifier in the package name is Q.

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Table 3-1: Package/Device Pinout Files for CG, EG, and EV Devices

| Packages               | Footprint Compatible Devices                  |                       |            |                       |                       |                       |
|------------------------|-----------------------------------------------|-----------------------|------------|-----------------------|-----------------------|-----------------------|
| SBVA484                | XCZU1CG                                       | XCZU2CG               | XCZU3CG    |                       |                       |                       |
|                        | XCZU1EG                                       | XCZU2EG               | XCZU3EG    |                       |                       |                       |
|                        | XAZU1EG                                       | XAZU2EG               | XAZU3EG    |                       |                       |                       |
|                        | Production                                    | Production            | Production |                       |                       |                       |
| SFRA484                | XQZU3EG<br>Production                         |                       |            |                       |                       |                       |
| UBVA494                | XCZU1CG                                       |                       |            |                       |                       |                       |
|                        | XCZU1EG<br>Production                         |                       |            |                       |                       |                       |
| UBVA530                | XCZU2CG                                       | XCZU3CG               |            |                       |                       |                       |
|                        | XCZU2EG<br>Production                         | XCZU3EG<br>Production |            |                       |                       |                       |
| SFVA625                | XCZU1CG                                       | XCZU2CG               | XCZU3CG    |                       |                       |                       |
|                        | XCZU1EG                                       | XCZU2EG               | XCZU3EG    |                       |                       |                       |
|                        | XAZU1EG                                       | XAZU2EG               | XAZU3EG    |                       |                       |                       |
|                        | Production                                    | Production            | Production |                       |                       |                       |
| SFVC784                | XCZU1CG                                       | XCZU2CG               | XCZU3CG    | XCZU3TCG              | XCZU4CG               | XCZU5CG               |
|                        | XCZU1EG                                       | XCZU2EG               | XCZU3EG    | XCZU3TEG              | XCZU4EG               | XCZU5EG               |
|                        | XAZU1EG                                       | XAZU2EG               | XAZU3EG    | Engineering<br>Sample | XAZU4EV               | XCZU5EV               |
|                        | Production                                    | Production            | Production |                       | XAZU4EV<br>Production | XAZU5EV<br>Production |
| SFRC784                | XQZU3EG<br>Production                         | XQZU5EV<br>Production |            |                       |                       |                       |
| SFVD784                | XCZU3TCG<br>XCZU3TEG<br>Engineering<br>Sample |                       |            |                       |                       |                       |
| SFVE784 <sup>(3)</sup> | XCZU4CG                                       | XCZU5CG               |            |                       |                       |                       |
|                        | XCZU4EG                                       | XCZU5EG               |            |                       |                       |                       |
|                        | XCZU4EV                                       | XCZU5EV               |            |                       |                       |                       |
|                        | Production                                    | Production            |            |                       |                       |                       |
| FBVB900                | XCZU4CG                                       | XCZU5CG               | XCZU7CG    | XAZU7EV<br>Production |                       |                       |
|                        | XCZU4EG                                       | XCZU5EG               | XCZU7EG    |                       |                       |                       |
|                        | XCZU4EV                                       | XCZU5EV               | XCZU7EV    |                       |                       |                       |
|                        | Production                                    | Production            | Production |                       |                       |                       |
| FFRB900                | XQZU5EV<br>Production                         | XQZU7EV<br>Production |            |                       |                       |                       |

Table 3-1: Package/Device Pinout Files for CG, EG, and EV Devices (Cont'd)

| Packages | Footprint Compatible Devices                |                                  |                        |  |
|----------|---------------------------------------------|----------------------------------|------------------------|--|
| FFVC900  | XCZU6CG<br>XCZU6EG<br>Production            | XCZU9CG<br>XCZU9EG<br>Production | XCZU15EG<br>Production |  |
| FFRC900  | XQZU9EG<br>Production                       | XQZU15EG<br>Production           |                        |  |
| FFVB1156 | XCZU6CG<br>XCZU6EG<br>Production            | XCZU9CG<br>XCZU9EG<br>Production | XCZU15EG<br>Production |  |
| FFRB1156 | XQZU9EG<br>Production                       | XQZU15EG<br>Production           |                        |  |
| FFVC1156 | XCZU7CG<br>XCZU7EG<br>XCZU7EV<br>Production | XCZU11EG<br>Production           |                        |  |
| FFRC1156 | XQZU7EV<br>Production                       | XQZU11EG<br>Production           |                        |  |
| FFVB1517 | XCZU11EG<br>Production                      | XCZU17EG<br>Production           | XCZU19EG<br>Production |  |
| FFRB1517 | XCZU19EG<br>Production                      |                                  |                        |  |
| FFVF1517 | XCZU7CG<br>XCZU7EG<br>XCZU7EV<br>Production | XCZU11EG<br>Production           | XAZU11EG<br>Production |  |
| FFVC1760 | XCZU11EG<br>Production                      | XCZU17EG<br>Production           | XCZU19EG<br>Production |  |
| FFRC1760 | XQZU11EG<br>Production                      | XQZU19EG<br>Production           |                        |  |
| FFVD1760 | XCZU17EG<br>Production                      | XCZU19EG<br>Production           |                        |  |
| FFVE1924 | XCZU17EG<br>Production                      | XCZU19EG<br>Production           |                        |  |



Table 3-2: Package/Device Pinout Files for Zynq UltraScale+ RFSocS

| Package  | Footprint Compatible Devices                         |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |  |
|----------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|--|
| FFVD1156 | <a href="#">XCZU21DR</a><br>Production               |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |  |
| FFRD1156 | <a href="#">XQZU21DR</a><br>Production               |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |  |
| FFVE1156 | <a href="#">XCZU25DR</a><br>Production               | <a href="#">XCZU27DR</a><br>Production               | <a href="#">XCZU28DR</a><br>Production               | <a href="#">XCZU42DR<sup>(2)</sup></a><br>Production | <a href="#">XCZU43DR<sup>(1)</sup></a><br>Production | <a href="#">XCZU47DR<sup>(1)</sup></a><br>Production | <a href="#">XCZU48DR<sup>(1)</sup></a><br>Production | <a href="#">XCZU63DR<sup>(2)</sup></a><br>Production | <a href="#">XCZU64DR<sup>(2)</sup></a><br>Production |  |
| FFRE1156 | <a href="#">XQZU28DR</a><br>Production               | <a href="#">XQZU48DR<sup>(1)</sup></a><br>Production |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |  |
| FSVE1156 | <a href="#">XCZU25DR</a><br>Production               | <a href="#">XCZU27DR</a><br>Production               | <a href="#">XCZU28DR</a><br>Production               | <a href="#">XCZU42DR<sup>(2)</sup></a><br>Production | <a href="#">XCZU43DR<sup>(1)</sup></a><br>Production | <a href="#">XCZU47DR<sup>(1)</sup></a><br>Production | <a href="#">XCZU48DR<sup>(1)</sup></a><br>Production | <a href="#">XCZU63DR<sup>(2)</sup></a><br>Production | <a href="#">XCZU64DR<sup>(2)</sup></a><br>Production |  |
| FFVG1517 | <a href="#">XCZU25DR</a><br>Production               | <a href="#">XCZU27DR</a><br>Production               | <a href="#">XCZU28DR</a><br>Production               |                                                      | <a href="#">XCZU43DR<sup>(1)</sup></a><br>Production | <a href="#">XCZU47DR<sup>(1)</sup></a><br>Production | <a href="#">XCZU48DR<sup>(1)</sup></a><br>Production |                                                      |                                                      |  |
| FFRG1517 | <a href="#">XQZU28DR</a><br>Production               |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |  |
| FSRG1517 | <a href="#">XQZU48DR</a><br>Production               |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |  |
| FSVG1517 | <a href="#">XCZU25DR</a><br>Production               | <a href="#">XCZU27DR</a><br>Production               | <a href="#">XCZU28DR</a><br>Production               |                                                      | <a href="#">XCZU43DR<sup>(1)</sup></a><br>Production | <a href="#">XCZU47DR<sup>(1)</sup></a><br>Production | <a href="#">XCZU48DR<sup>(1)</sup></a><br>Production |                                                      |                                                      |  |
| FFVF1760 | <a href="#">XCZU29DR</a><br>Production               | <a href="#">XCZU39DR</a><br>Production               | <a href="#">XCZU49DR<sup>(1)</sup></a><br>Production |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |  |
| FFVH1760 | <a href="#">XCZU46DR</a><br>Production               |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |  |
| FFRF1760 | <a href="#">XQZU29DR</a><br>Production               |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |  |
| FSRF1760 | <a href="#">XQZU49DR<sup>(1)</sup></a><br>Production |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |  |
| FSVF1760 | <a href="#">XCZU29DR</a><br>Production               | <a href="#">XCZU39DR</a><br>Production               | <a href="#">XCZU49DR<sup>(1)</sup></a><br>Production |                                                      |                                                      |                                                      |                                                      |                                                      |                                                      |  |



Table 3-2: Package/Device Pinout Files for Zynq UltraScale+ RFSocS (Cont’d)

| Footprint Compatible Devices |                                        |
|------------------------------|----------------------------------------|
| Package                      |                                        |
| FSVH1760                     | <a href="#">XCZU46DR</a><br>Production |

Notes:

1. The ZU4xDR and ZU6xDR devices are footprint compatible devices. However, they have a different set of ADC and DAC power sequencing devices. Refer to *Zynq UltraScale+ RFSoc Data Sheet: DC and AC Switching Characteristics (DS926)* for specific power sequencing differences.
2. The XCZU42DR, XCZU63DR, XCZU64DR, XCZU65DR, and XCZU67DR are only partially compatible with other devices in the FFVE1156 and differences in the ADC and DAC architecture. When planning migration between devices, differences that must be addressed include ADC power rail voltage specifications.

3. Migration between the SFVD784 and SFVE784 is possible by following the guidelines in the [Migration Between SFVD784 and SFVE784](#) Package Pinout Files.

# Device Diagrams

## Summary

The diagrams in this chapter show top-view perspective of the package pinout of each Zynq™ UltraScale+ device. [Table 4-1](#) is a cross reference to the device/package diagrams. The I/O-bank diagram shows user I/O, PSMIO, PSDDR, PSCONFIG, and PS-GTR, GTH, and GTY transceiver and the respective bank configuration-power diagram shows the location of every power pin and dedicated as well as multi-function pins in the package. See [Package Specifications Designations in Chapter 3](#) for definitions of [Evaluation On](#) and [Production](#) device diagrams.



**IMPORTANT:** All non-InFO packages are available with eutectic BGA balls. To order these packages, the device type or XA, and the Pb-free signifier in the package name is Q.

Table 4-1: Cross-Reference to Zynq UltraScale+ Device Diagrams by Package

| Footprint Compatible Devices |                                                         |                                                           |
|------------------------------|---------------------------------------------------------|-----------------------------------------------------------|
| SBVA484                      | XCZU1CG<br>XCZU1EG<br>XAZU1EG<br>Production<br>page 138 | XCZU2CG,<br>XCZU2EG,<br>XAZU2EG<br>Production<br>page 140 |
|                              |                                                         | XCZU3CG,<br>XCZU3EG,<br>XAZU3EG<br>Production<br>page 140 |
| SFRA484                      |                                                         | XQZU3EG<br>Production<br>page 140                         |



Table 4-1: Cross-Reference to Zynq UltraScale+ Device Diagrams by Package (Cont'd)

| Footprint Compatible Devices |                                                                                       |
|------------------------------|---------------------------------------------------------------------------------------|
| Packages                     |                                                                                       |
| UBVA494                      | XCZU1CG<br>XCZU1EG<br>Production<br><a href="#">page 142</a>                          |
|                              |                                                                                       |
| UBVA530                      | XCZU2CG,<br>XCZU2EG<br>Production<br><a href="#">page 144</a>                         |
|                              | XCZU3CG,<br>XCZU3EG<br>Production<br><a href="#">page 144</a>                         |
| SFVA625                      | XCZU1CG<br>XCZU1EG<br>XAZU1EG<br>Production<br><a href="#">page 146</a>               |
|                              | XCZU2CG,<br>XCZU2EG,<br>XAZU2EG<br>Production<br><a href="#">page 148</a>             |
| SFVC784                      | XCZU3CG,<br>XCZU3EG,<br>XAZU3EG<br>Production<br><a href="#">page 148</a>             |
|                              | XCZU3CG,<br>XCZU3EG,<br>XAZU3EG<br>Production<br><a href="#">page 152</a>             |
| SFVC784                      | XCZU1CG<br>XCZU1EG<br>XAZU1EG<br>Production<br><a href="#">page 150</a>               |
|                              | XCZU2CG,<br>XCZU2EG,<br>XAZU2EG<br>Production<br><a href="#">page 152</a>             |
| SFVC784                      | XCZU3CG,<br>XCZU3EG,<br>XAZU3EG<br>Production<br><a href="#">page 152</a>             |
|                              | XCZU3TCG,<br>XCZU3TEG<br>Engineering<br>Sample<br><a href="#">page 154</a>            |
| SFVC784                      | XCZU4EV,<br>XCZU5EV,<br>XAZU4EV,<br>XAZU5EV<br>Production<br><a href="#">page 160</a> |
|                              | XCZU4CG,<br>XCZU4EG,<br>XCZU5CG,<br>XCZU5EG<br>Production<br><a href="#">page 158</a> |
| SFVC784                      | XQZU5EV<br>Production<br><a href="#">page 160</a>                                     |
|                              |                                                                                       |
| SFVD784                      | XCZU3TCG,<br>XCZU3TEG<br>Engineering<br>Sample<br><a href="#">page 156</a>            |
|                              |                                                                                       |

Table 4-1: Cross-Reference to Zynq UltraScale+ Device Diagrams by Package (Cont'd)

| Packages               | Footprint Compatible Devices                                          |                                               |                                               |                                                           |                                                           |
|------------------------|-----------------------------------------------------------------------|-----------------------------------------------|-----------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|
| SFVE784 <sup>(1)</sup> |                                                                       |                                               |                                               | XCZU4CG,<br>XCZU4EG,<br>XCZU4EV<br>Production<br>page 164 | XCZU5CG,<br>XCZU5EG,<br>XCZU5EV<br>Production<br>page 164 |
| FBVB900                | XCZU4CG,<br>XCZU4EG,<br>XCZU5CG,<br>XCZU5EG<br>Production<br>page 166 | XCZU4EV,<br>XCZU5EV<br>Production<br>page 168 | XCZU7CG,<br>XCZU7EG<br>Production<br>page 170 | XCZU7EV<br>XAZU7EV<br>Production<br>page 172              |                                                           |
| FFRB900                |                                                                       | XQZU5EV<br>Production<br>page 168             |                                               | XQZU7EV<br>Production<br>page 172                         |                                                           |
| FFVC900                | XCZU6CG,<br>XCZU6EG<br>Production<br>page 174                         | XCZU9CG,<br>XCZU9EG<br>Production<br>page 174 | XCZU15EG<br>Production<br>page 174            |                                                           |                                                           |
| FFRC900                |                                                                       | XQZU9EG<br>Production<br>page 174             | XQZU15EG<br>Production<br>page 174            |                                                           |                                                           |
| FFVB1156               | XCZU6CG,<br>XCZU6EG<br>Production<br>page 176                         | XCZU9CG,<br>XCZU9EG<br>Production<br>page 176 | XCZU15EG<br>Production<br>page 176            |                                                           |                                                           |
| FFRB1156               |                                                                       | XQZU9EG<br>Production<br>page 176             | XQZU15EG<br>Production<br>page 176            |                                                           |                                                           |

Table 4-1: Cross-Reference to Zynq UltraScale+ Device Diagrams by Package (Cont'd)

| Packages             | Footprint Compatible Devices                  |                                                |                                    |                                    |                                    |                                    |                                    |                                    |
|----------------------|-----------------------------------------------|------------------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|
| FFVC1156             | XCZU7CG,<br>XCZU7EG<br>Production<br>page 178 | XCZU7EV<br>Production<br>page 180              | XCZU11EG<br>Production<br>page 182 |                                    |                                    |                                    |                                    |                                    |
| FFRC1156             |                                               | XQZU7EV<br>Production<br>page 180              | XQZU11EG<br>Production<br>page 182 |                                    |                                    |                                    |                                    |                                    |
| FFVD1156             | XCZU21DR<br>Production<br>page 184            |                                                |                                    |                                    |                                    |                                    |                                    |                                    |
| FFRD1156             | XQZU21DR<br>Production<br>page 184            |                                                |                                    |                                    |                                    |                                    |                                    |                                    |
| FFVE1156<br>FSVE1156 | XCZU25DR<br>Production<br>page 186            | XCZU27DR<br>XCZU28DR<br>Production<br>page 188 | XCZU42DR<br>Production<br>page 190 | XCZU43DR<br>Production<br>page 192 | XCZU47DR<br>Production<br>page 194 | XCZU48DR<br>Production<br>page 196 | XCZU63DR<br>Production<br>page 198 | XCZU64DR<br>Production<br>page 200 |
| FFRE1156             |                                               | XQZU28DR<br>Production<br>page 188             |                                    |                                    | XQZU48DR<br>Production<br>page 196 |                                    |                                    |                                    |
| FFVB1517             | XCZU11EG<br>Production<br>page 206            | XCZU17EG<br>Production<br>page 208             | XCZU19EG<br>Production<br>page 208 |                                    |                                    |                                    |                                    |                                    |
| FFRB1517             |                                               |                                                | XQZU19EG<br>Production<br>page 208 |                                    |                                    |                                    |                                    |                                    |

Table 4-1: Cross-Reference to Zynq UltraScale+ Device Diagrams by Package (Cont'd)

| Packages             | Footprint Compatible Devices                  |                                    |                                    |                                    |                                    |
|----------------------|-----------------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|
|                      | XCZU7CG,<br>XCZU7EG<br>Production<br>page 210 | XCZU7EV<br>Production<br>page 212  | XCZU11EG<br>Production<br>page 214 | XAZU11EG<br>Production<br>page 214 |                                    |
| FFVF1517<br>FSVG1517 | XCZU25DR<br>Production<br>page 216            | XCZU27DR<br>Production<br>page 218 | XCZU28DR<br>Production<br>page 218 | XCZU43DR<br>Production<br>page 220 | XCZU47DR<br>Production<br>page 222 |
| FSRG1517             |                                               |                                    |                                    |                                    |                                    |
| FFRG1517             |                                               |                                    | XQZU28DR<br>Production<br>page 218 |                                    |                                    |
| FFVC1760             | XCZU11EG<br>Production<br>page 226            | XCZU17EG<br>Production<br>page 228 | XCZU19EG<br>Production<br>page 228 |                                    |                                    |
| FFRC1760             | XQZU11EG<br>Production<br>page 226            |                                    | XQZU19EG<br>Production<br>page 228 |                                    |                                    |
| FFVD1760             | XCZU17EG<br>Production<br>page 230            | XCZU19EG<br>Production<br>page 230 |                                    |                                    |                                    |
| FFVF1760<br>FSVF1760 | XCZU29DR<br>Production<br>page 232            | XCZU39DR<br>Production<br>page 232 | XCZU49DR<br>Production<br>page 234 | XQZU49DR<br>Production<br>page 234 |                                    |

Table 4-1: Cross-Reference to Zynq UltraScale+ Device Diagrams by Package (Cont'd)

| Packages             |                                                    | Footprint Compatible Devices                       |
|----------------------|----------------------------------------------------|----------------------------------------------------|
| FFVH1760<br>FSVH1760 | XCZU46DR<br>Production<br><a href="#">page 236</a> |                                                    |
|                      | XQZU29DR<br>Production<br><a href="#">page 232</a> |                                                    |
| FFRF1760             | XQZU49DR<br>Production<br><a href="#">page 234</a> |                                                    |
| FSRF1760             | XCZU17EG<br>Production<br><a href="#">page 238</a> | XCZU19EG<br>Production<br><a href="#">page 238</a> |
| FFVE1924             |                                                    |                                                    |

Notes:

1. Migration between the SFVD784 and SFVE784 is possible by following the guidelines in the [Migration Between SFVD784 and SFVE784](#) Pa

# SBVA484 Package—XCZU1CG, XCZU1EG, XAZU1EG

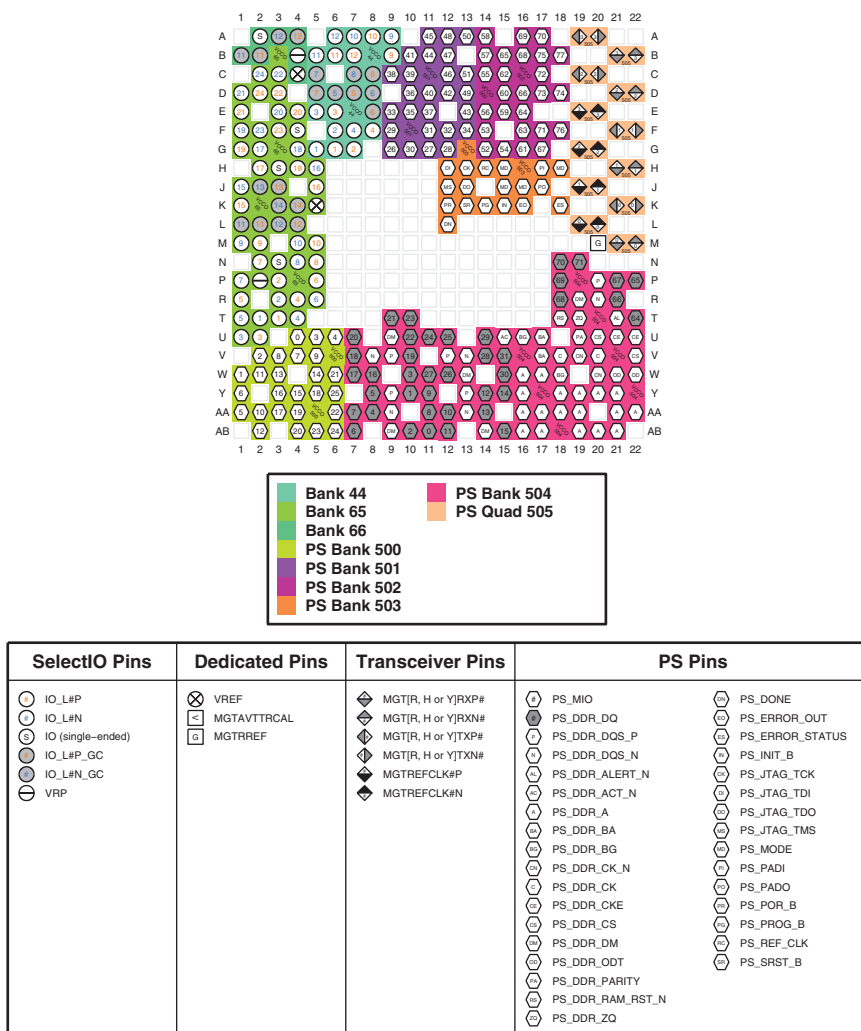


Figure 4-1: SBVA484 Package—XCZU1CG, XCZU1EG, and XAZU1EG I/O Bank Diagram

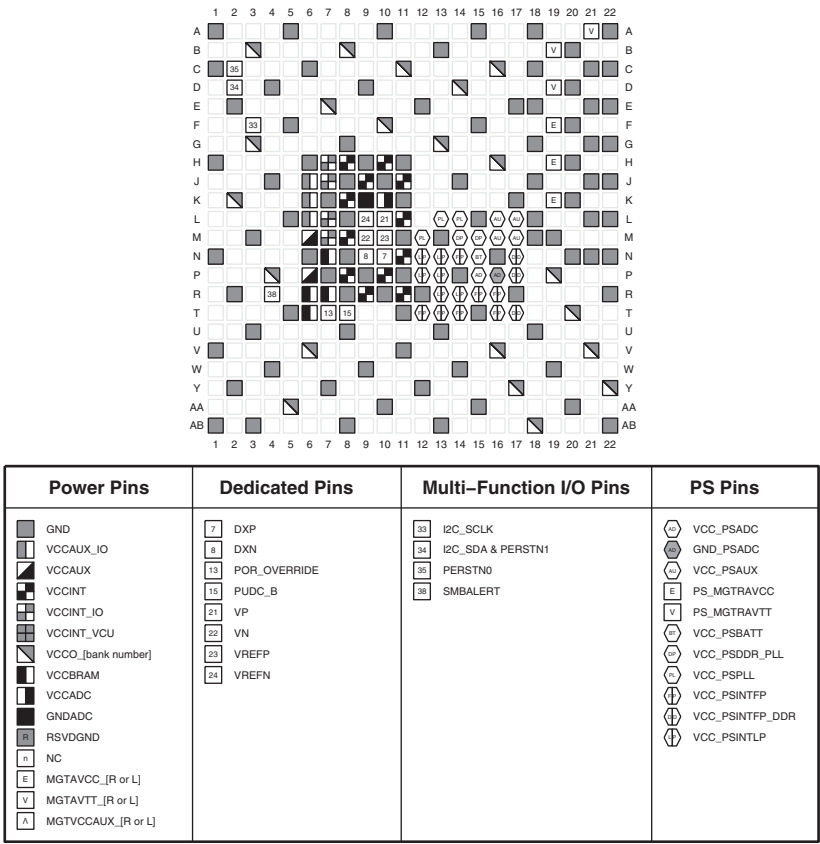


Figure 4-2: SBVA484 Package—XCZU1CG, XCZU1EG, and XAZU1EG Power, Dedicated, and Multi-function Pin Diagram

# SBVA484 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG



**IMPORTANT:** For the devices in the SBVA484 package, the HP I/Os in bank 66 are powered by VCCO\_65.

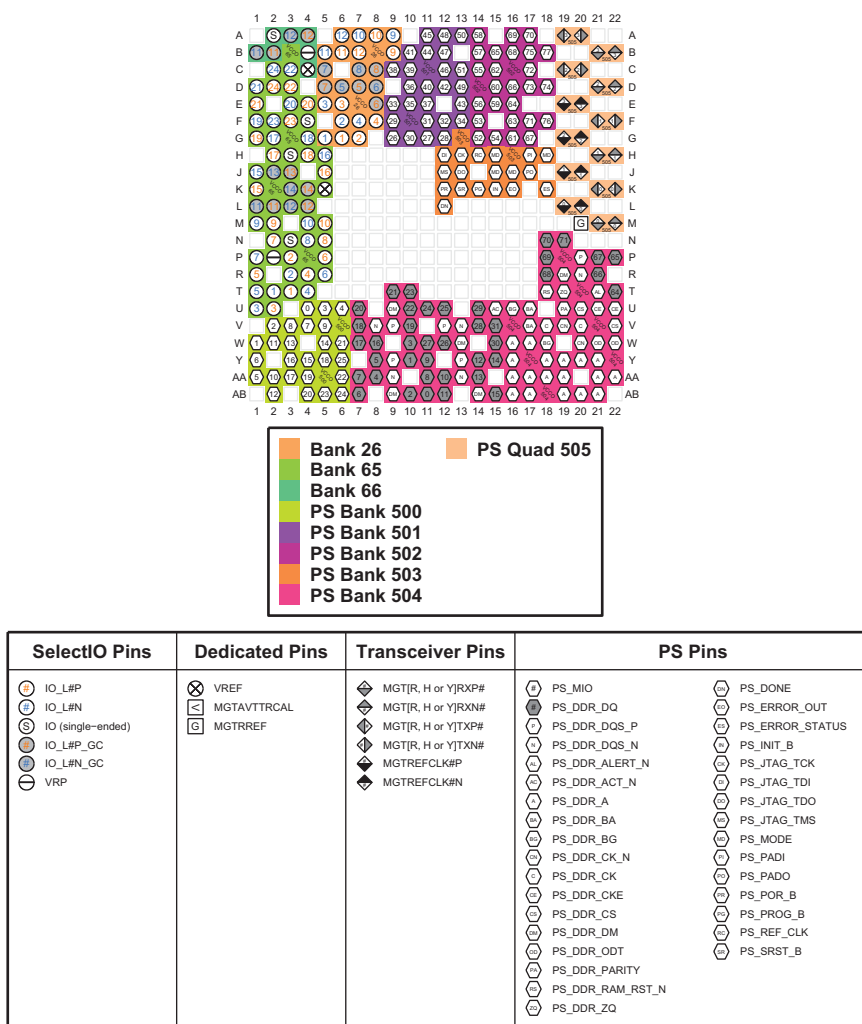


Figure 4-3: SBVA484 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG I/O Bank Diagram



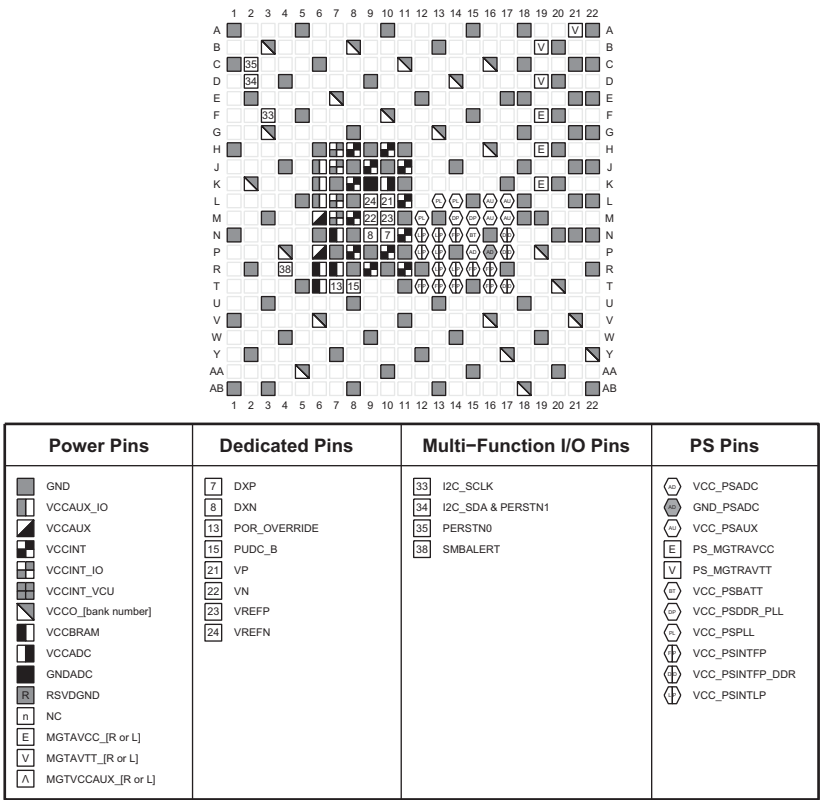


Figure 4-4: SBVA484 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of these devices in the SBVA484 package are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# UBVA494 Package—XCZU1CG, XCZU1EG

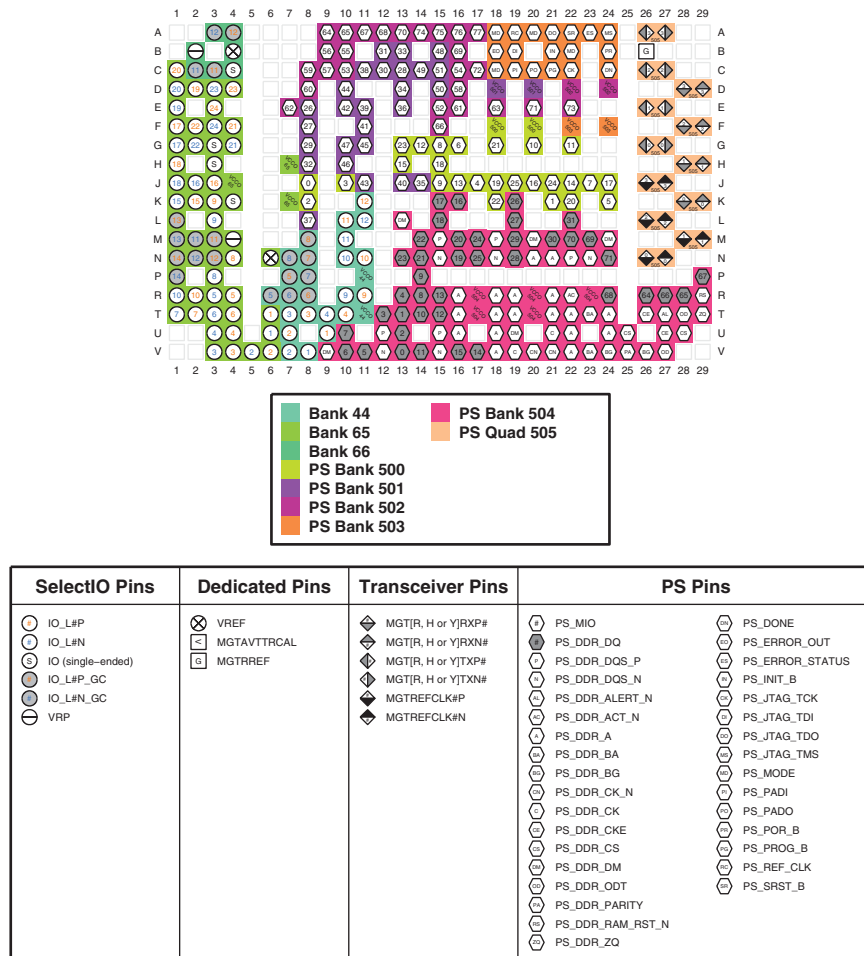


Figure 4-5: UBVA494 Package—XCZU1CG and XCZU1EG I/O Bank Diagram

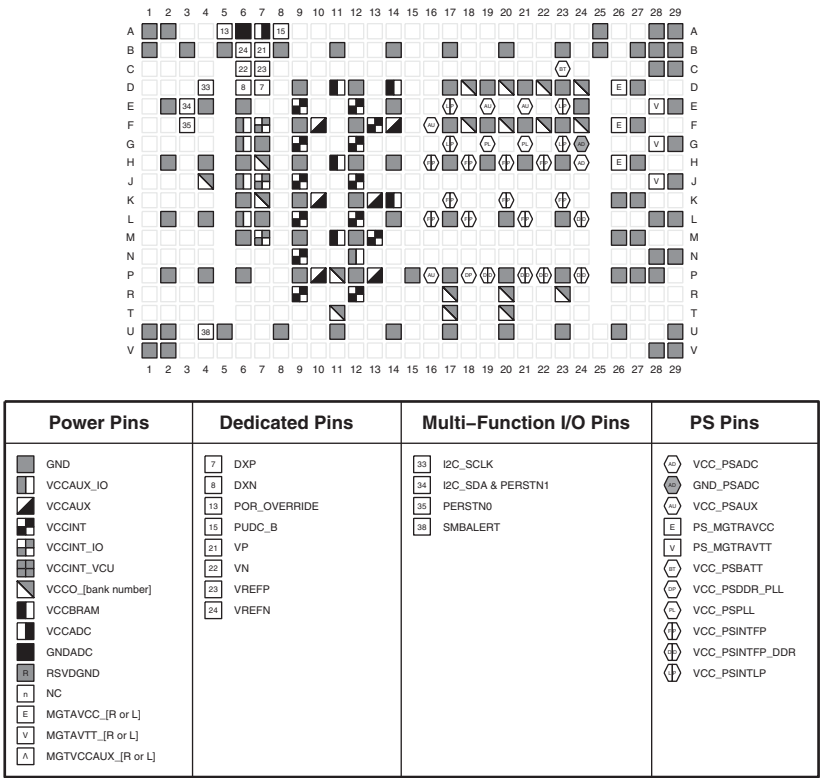


Figure 4-6: UBVA494 Package—XCZU1CG and XCZU1EG Power, Dedicated, and Multi-function Pin Diagram

# UBVA530 Package—XCZU2CG, XCZU2EG, XCZU3CG, and XCZU3EG

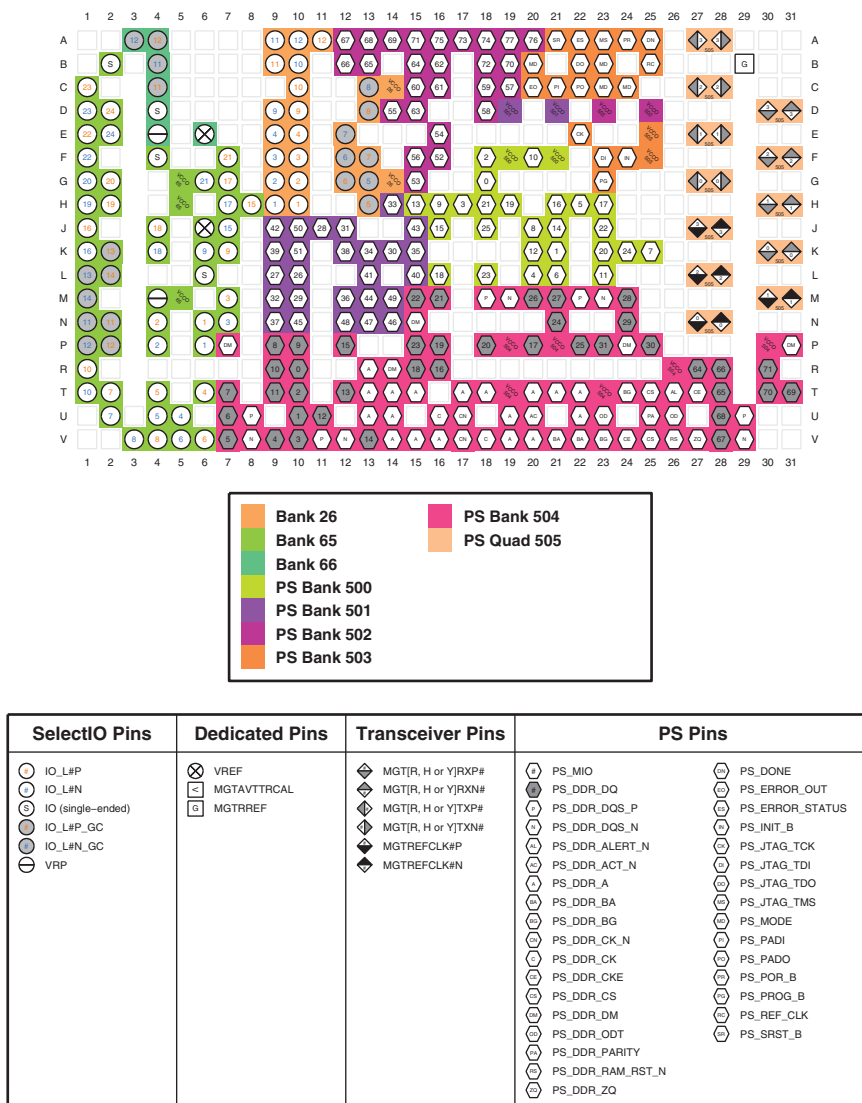


Figure 4-7: UBVA530 Package—XCZU2CG, XCZU2EG, XCZU3CG, and XCZU3EG I/O Bank Diagram

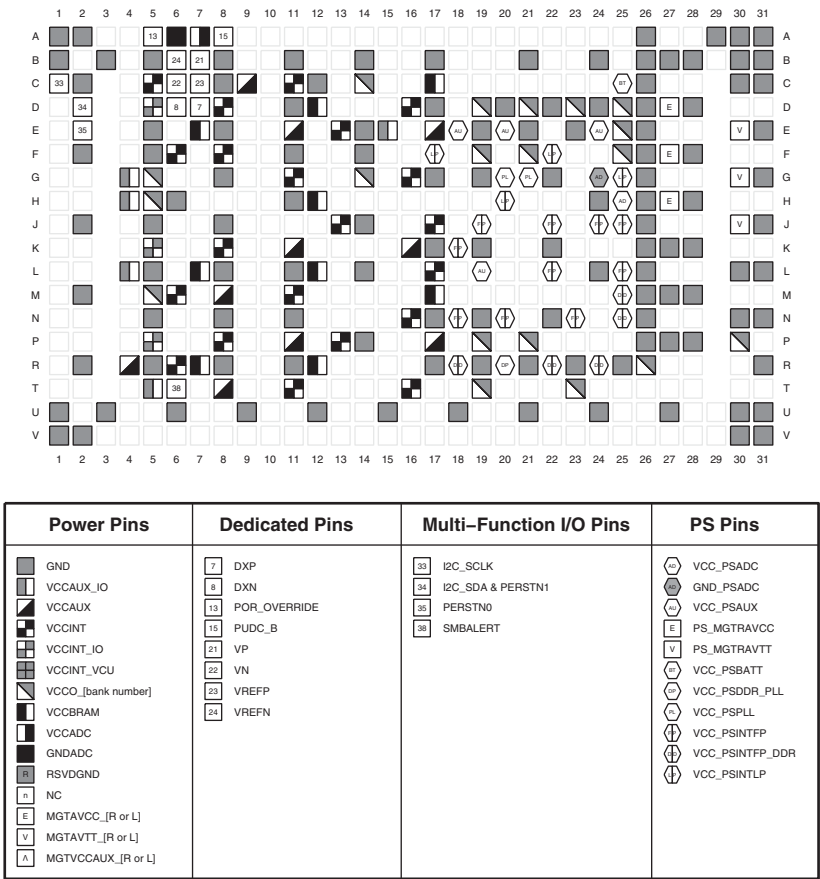


Figure 4-8: UBVA530 Package—XCZU2CG, XCZU2EG, XCZU3CG, and XCZU3EG Power, Dedicated, and Multi-function Pin Diagram

# SFVA625 Package—XCZU1CG, XCZU1EG, XAZU1EG

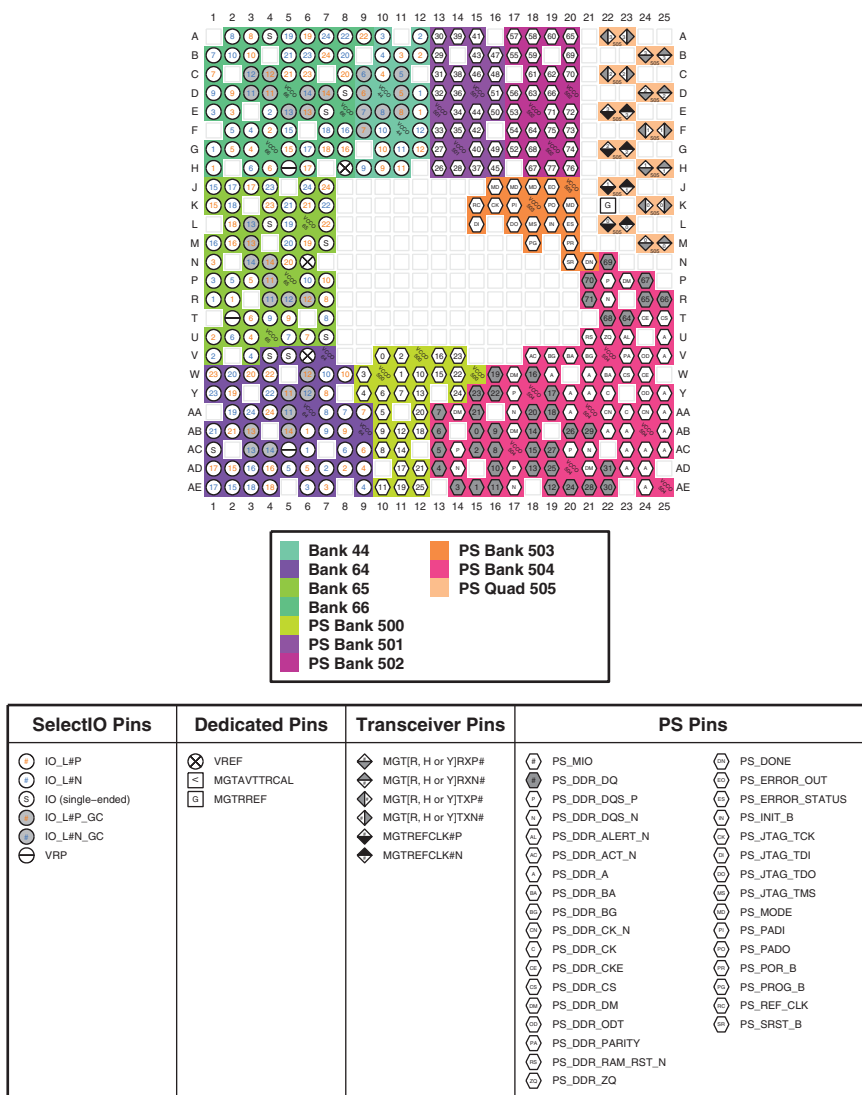


Figure 4-9: SFVA625 Package—XCZU1CG, XCZU1EG, and XAZU1EG I/O Bank Diagram

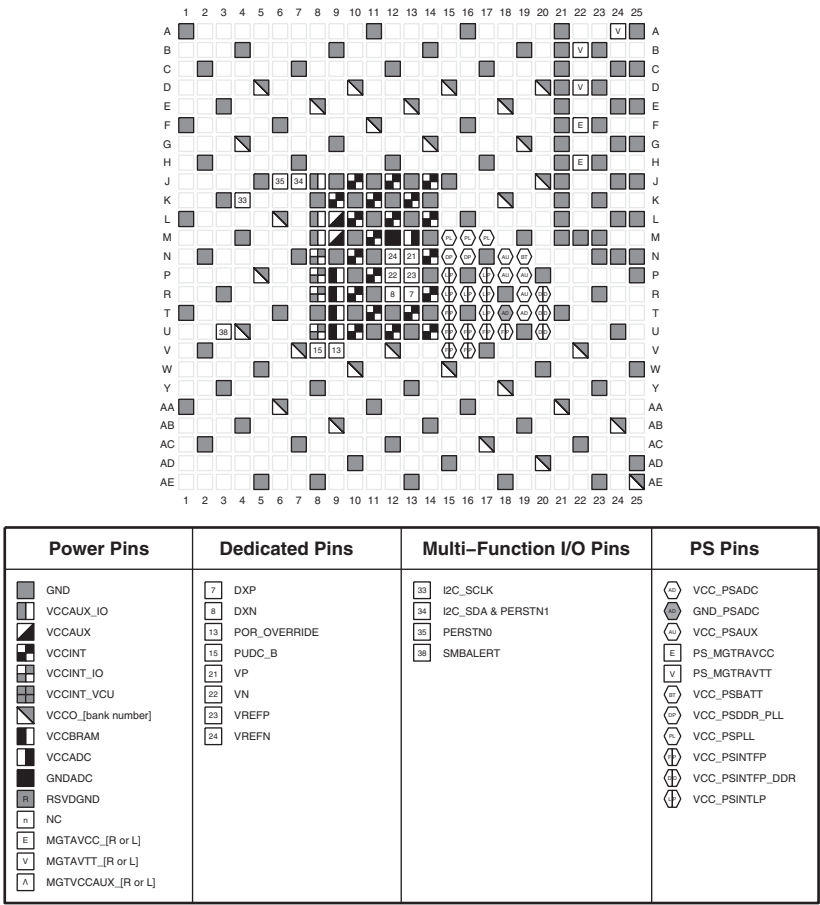


Figure 4-10: SFVA625 Package—XCZU1CG, XCZU1EG, and XAZU1EG Power, Dedicated, and Multi-function Pin Diagram

# SFVA625 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG

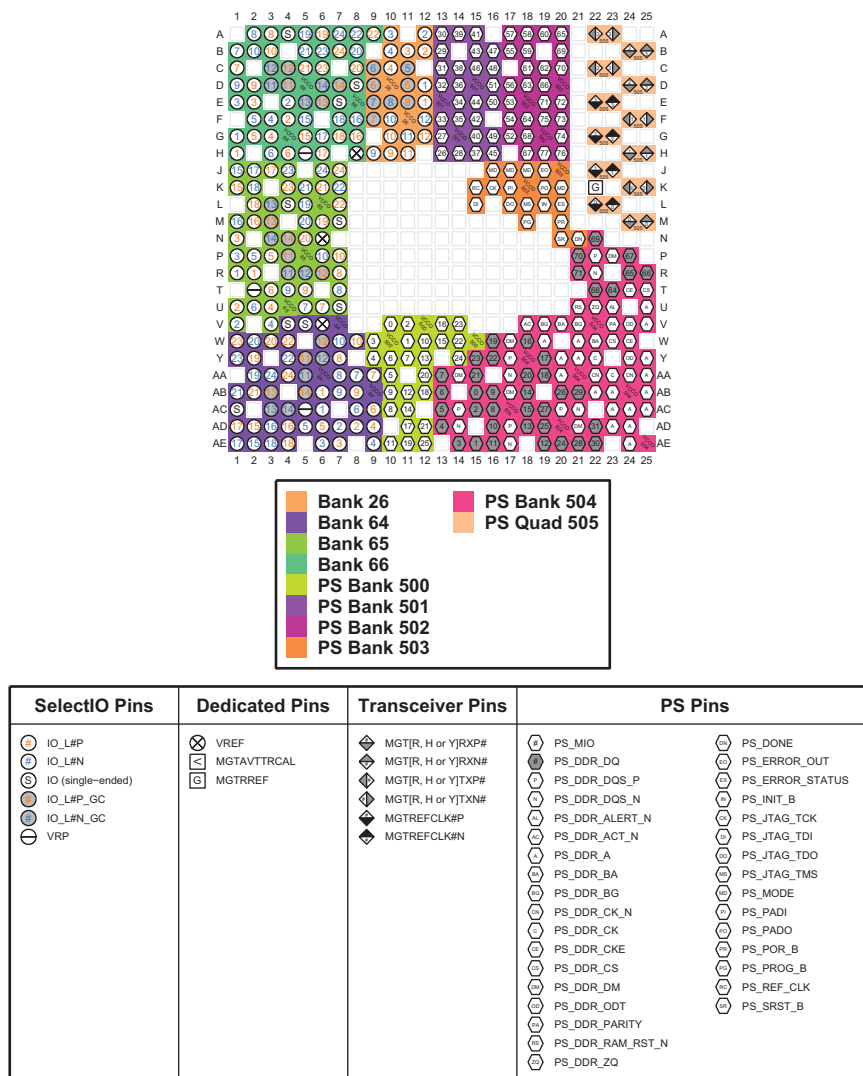


Figure 4-11: SFVA625 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG I/O Bank Diagram



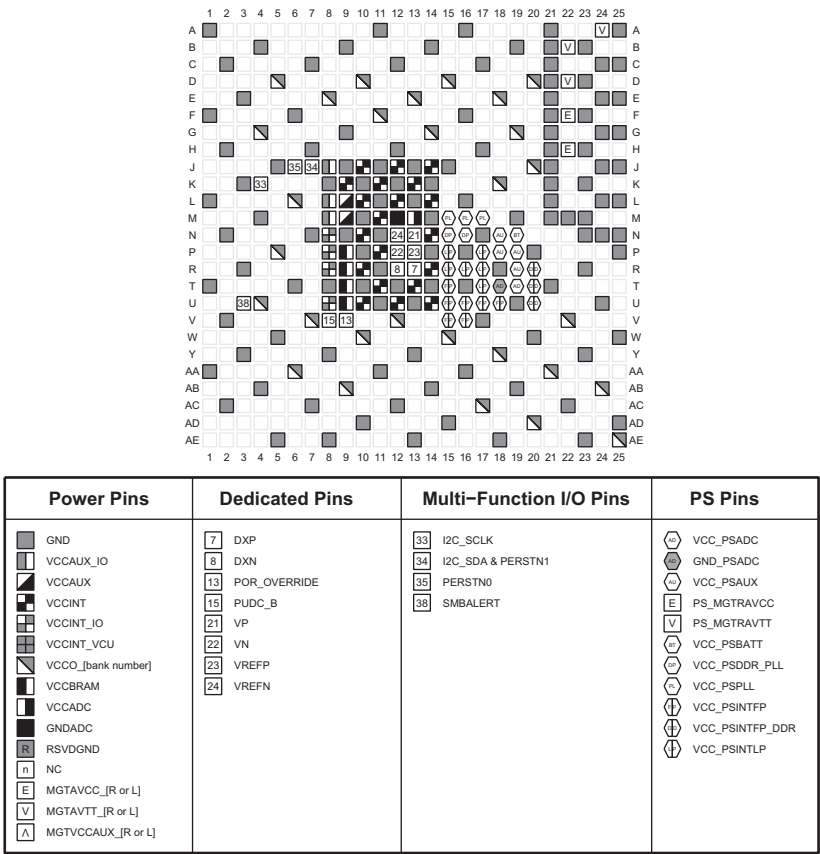


Figure 4-12: SFVA625 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG Power, Dedicated, and Multi-function Pin Diagram

# SFVC784 Package—XCZU1CG, XCZU1EG, XAZU1EG

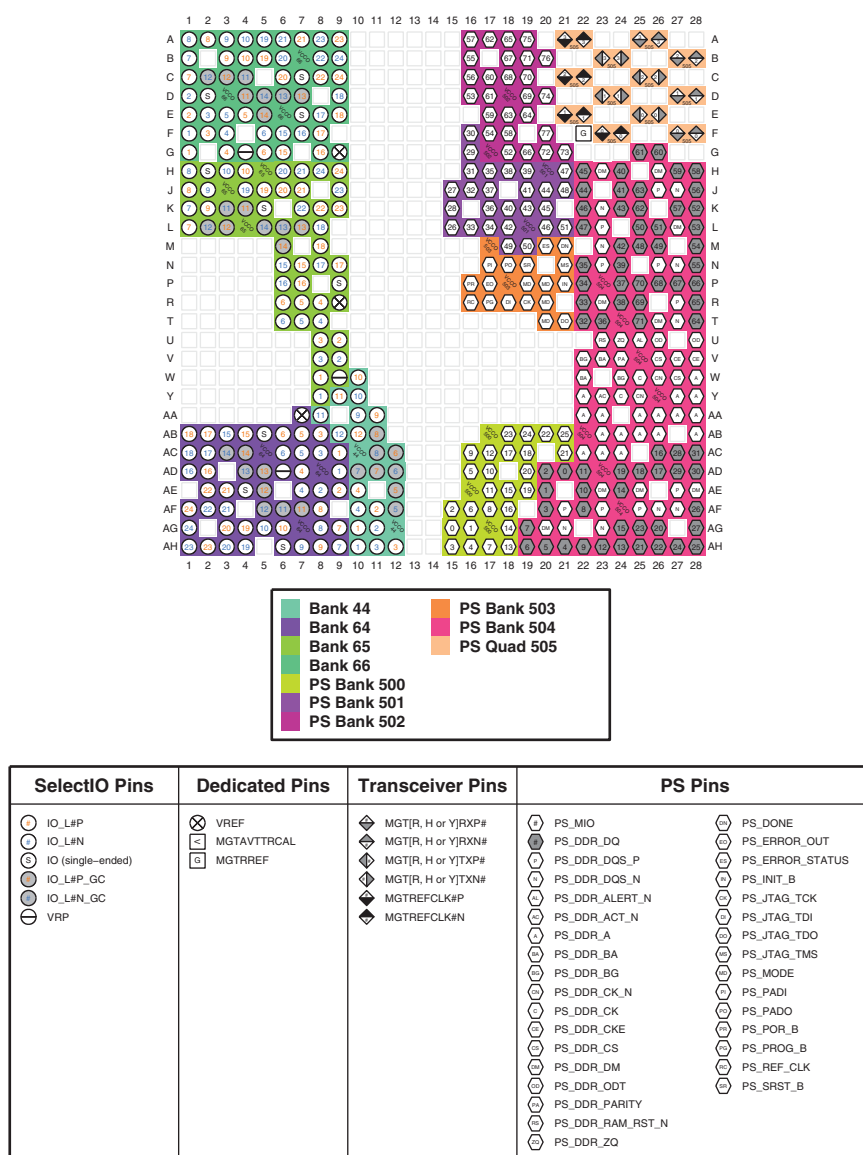


Figure 4-13: SFVC784 Package—XCZU1CG, XCZU1EG, and XAZU1EG I/O Bank Diagram

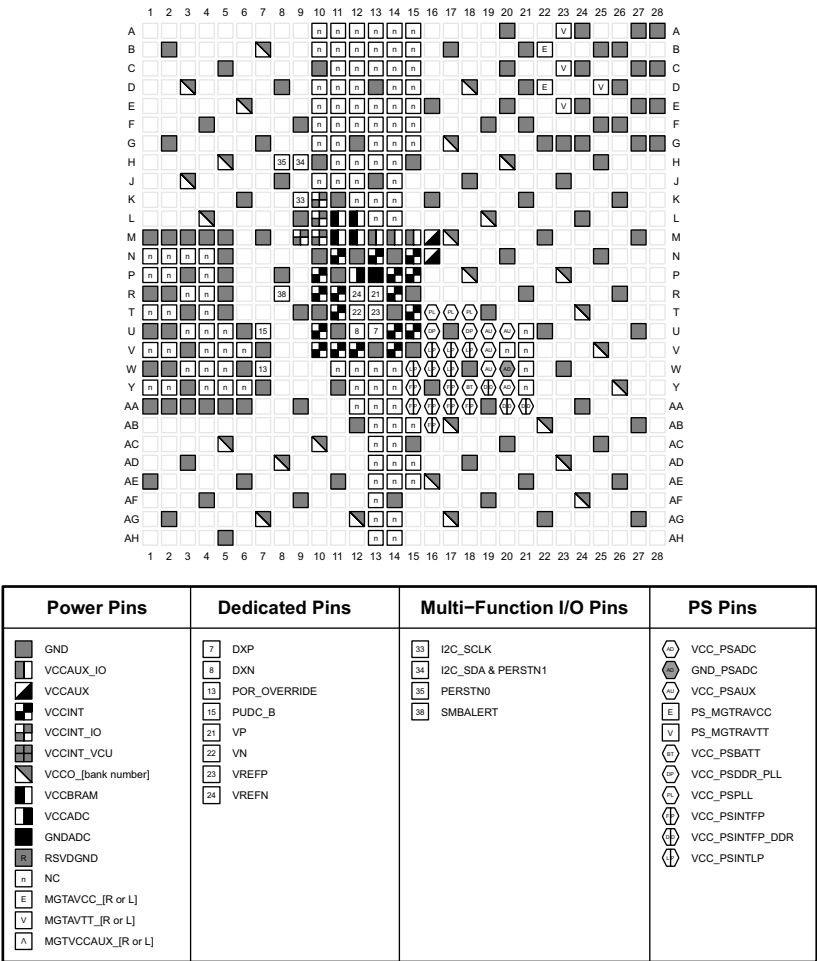


Figure 4-14: SFVC784 Package—XCZU1CG, XCZU1EG, and XAZU1EG Power, Dedicated, and Multi-function Pin Diagram

# SFVC784 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG

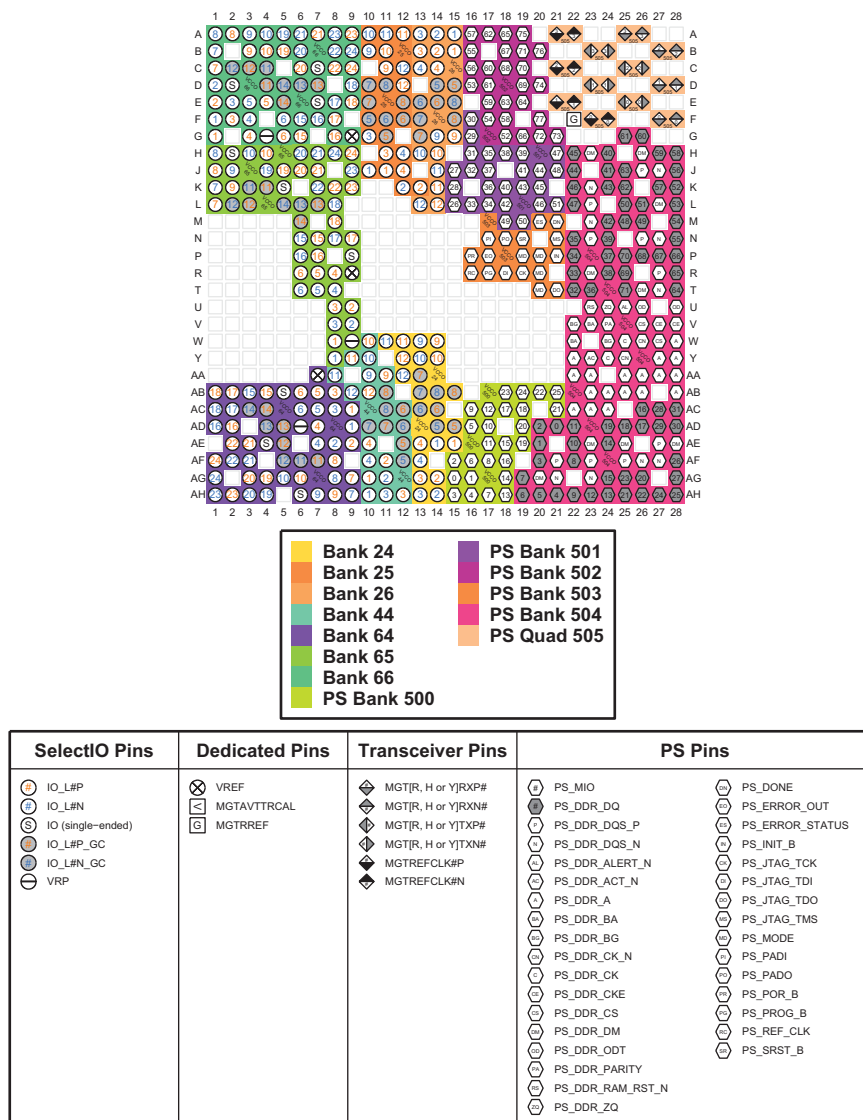


Figure 4-15: SFVC784 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG I/O Bank Diagram

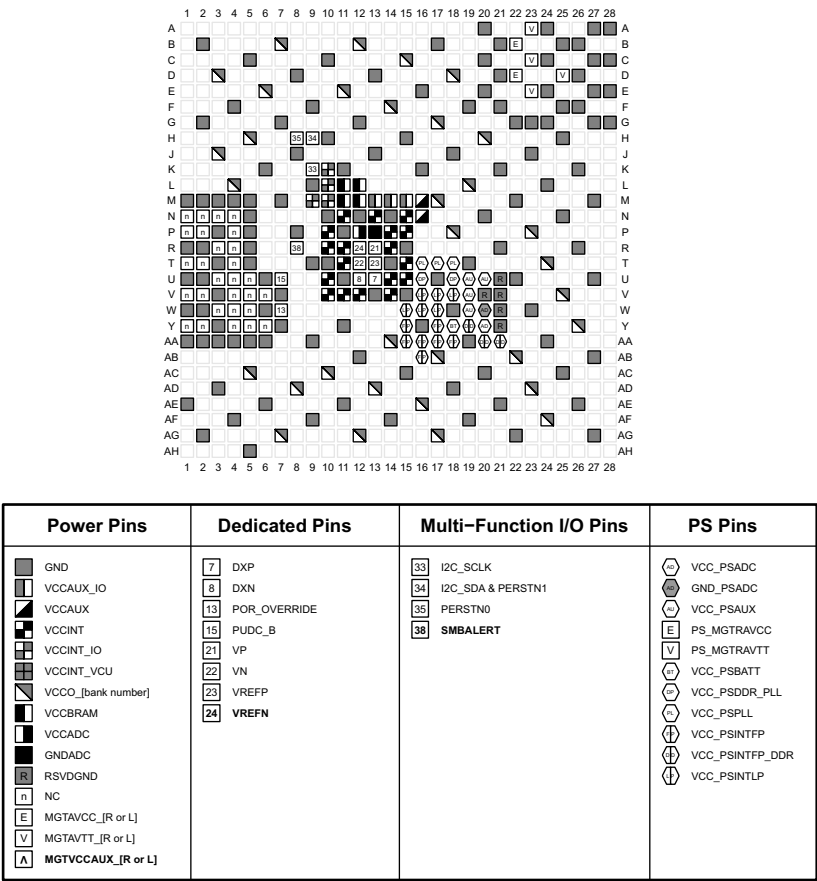


Figure 4-16: SFVC784 Package—XCZU2CG, XCZU2EG, XCZU3CG, XCZU3EG, XAZU2EG, and XAZU3EG Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of these devices in this package are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# SFVC784 Package—XCZU3TCG and XCZU3TEG

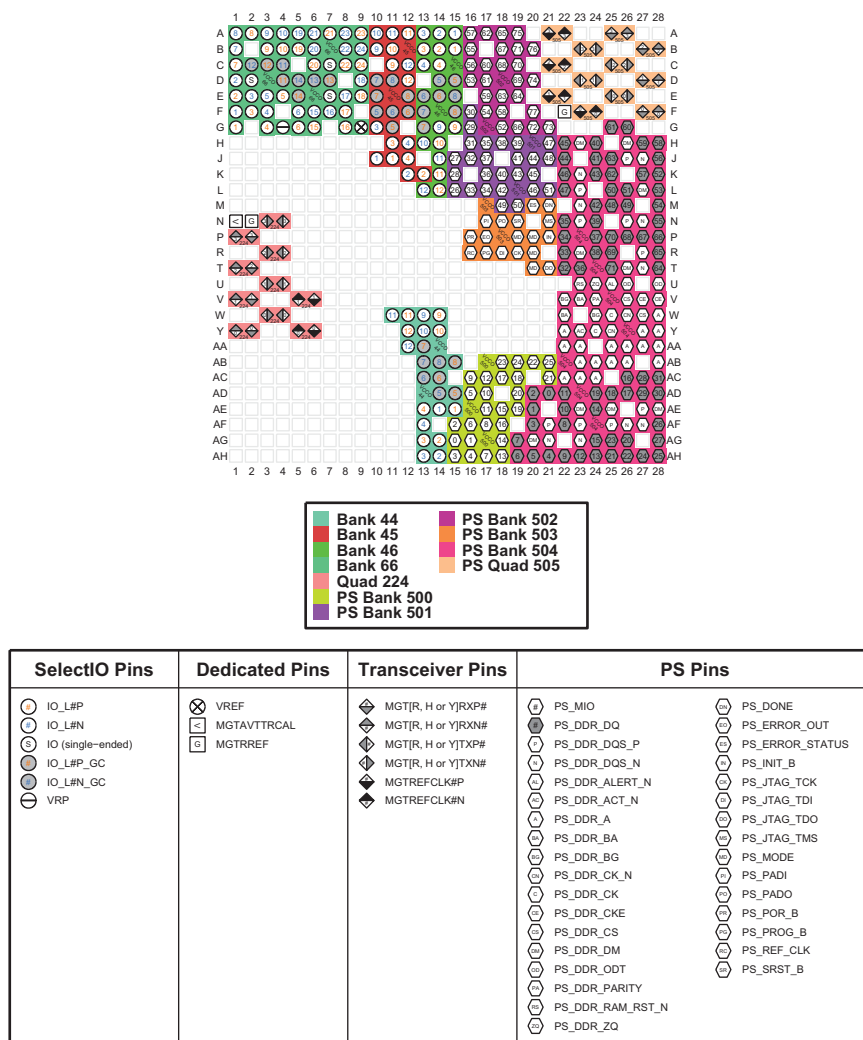


Figure 4-17: SFVC784 Package—XCZU3TCG and XCZU3TEG I/O Bank Diagram

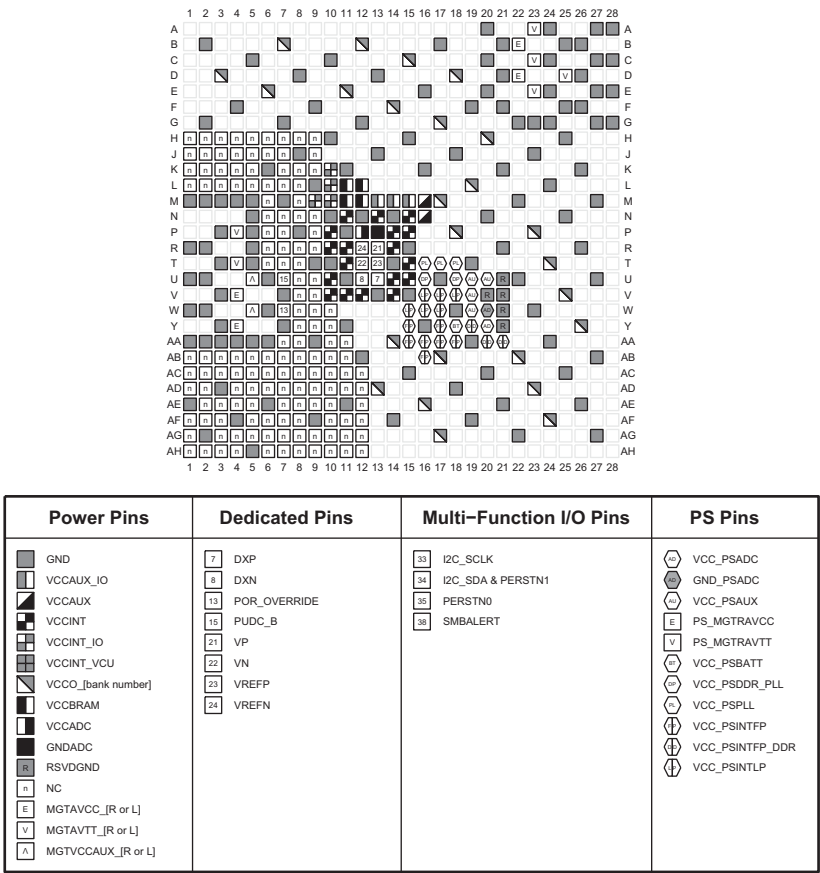


Figure 4-18: SFVC784 Package—XCZU3TCG and XCZU3TEG Power, Dedicated, and Multi-function Pin Diagram

# SFVD784 Package—XCZU3TCG and XCZU3TEG

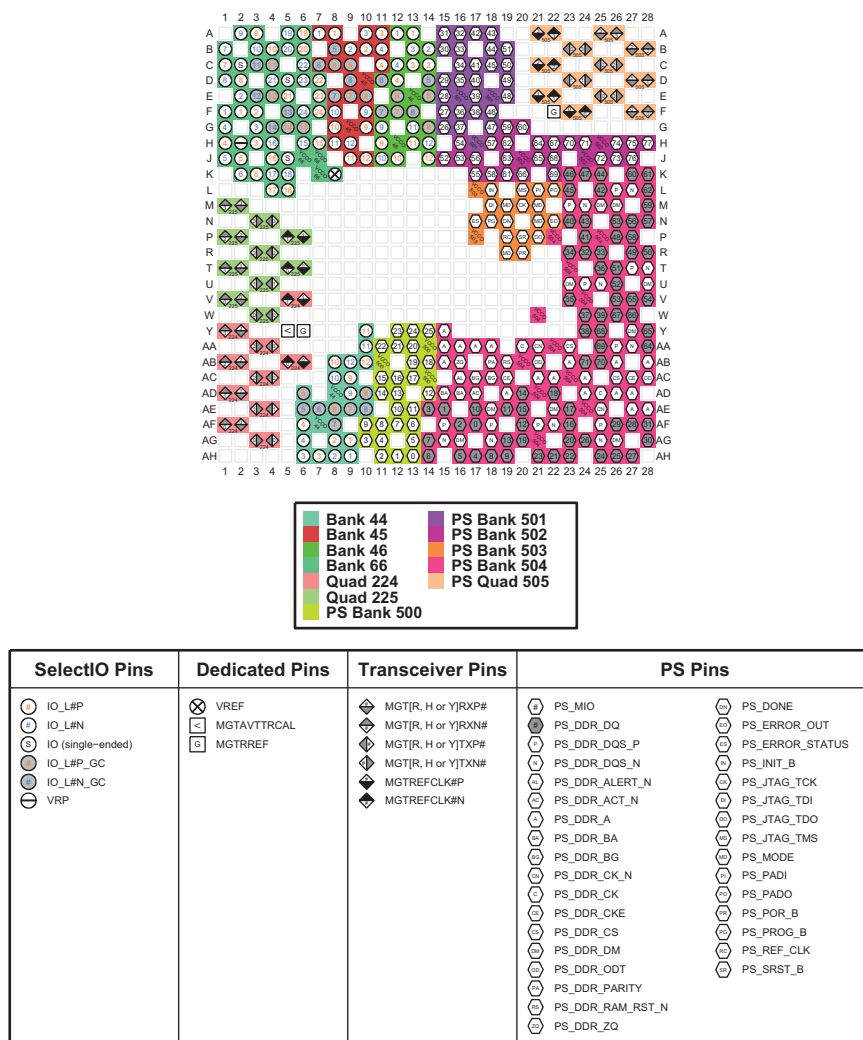


Figure 4-19: SFVD784 Package—XCZU3TCG and XCZU3TEG I/O Bank Diagram



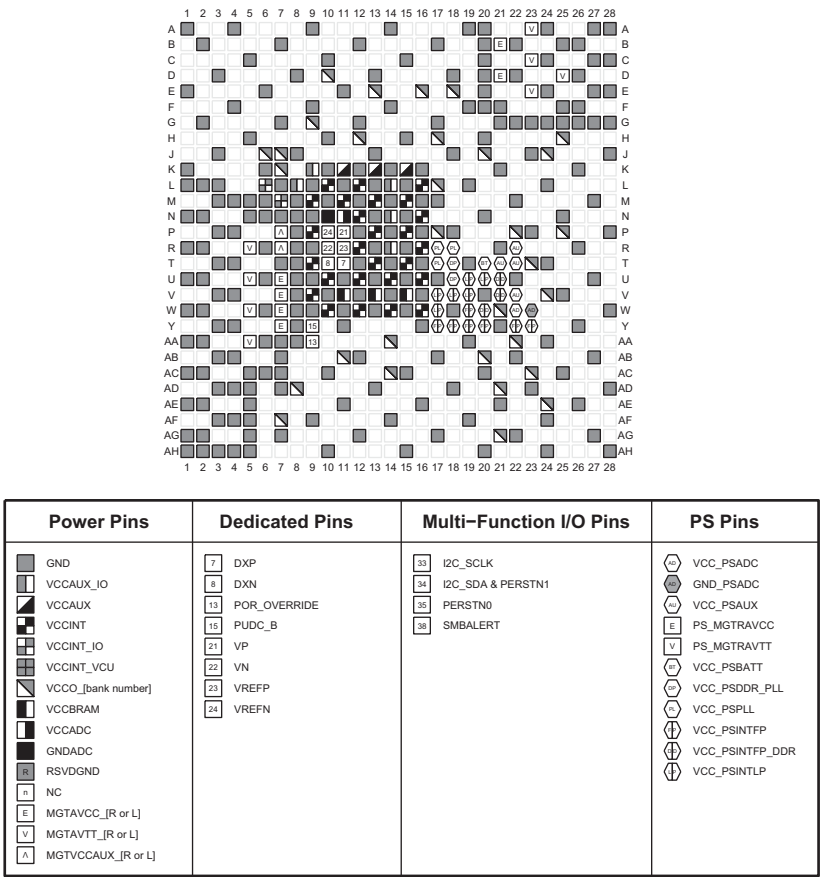


Figure 4-20: SFVD784 Package—XCZU3TCG and XCZU3TEG Power, Dedicated, and Multi-function Pin Diagram

# SFVC784 Package—XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG

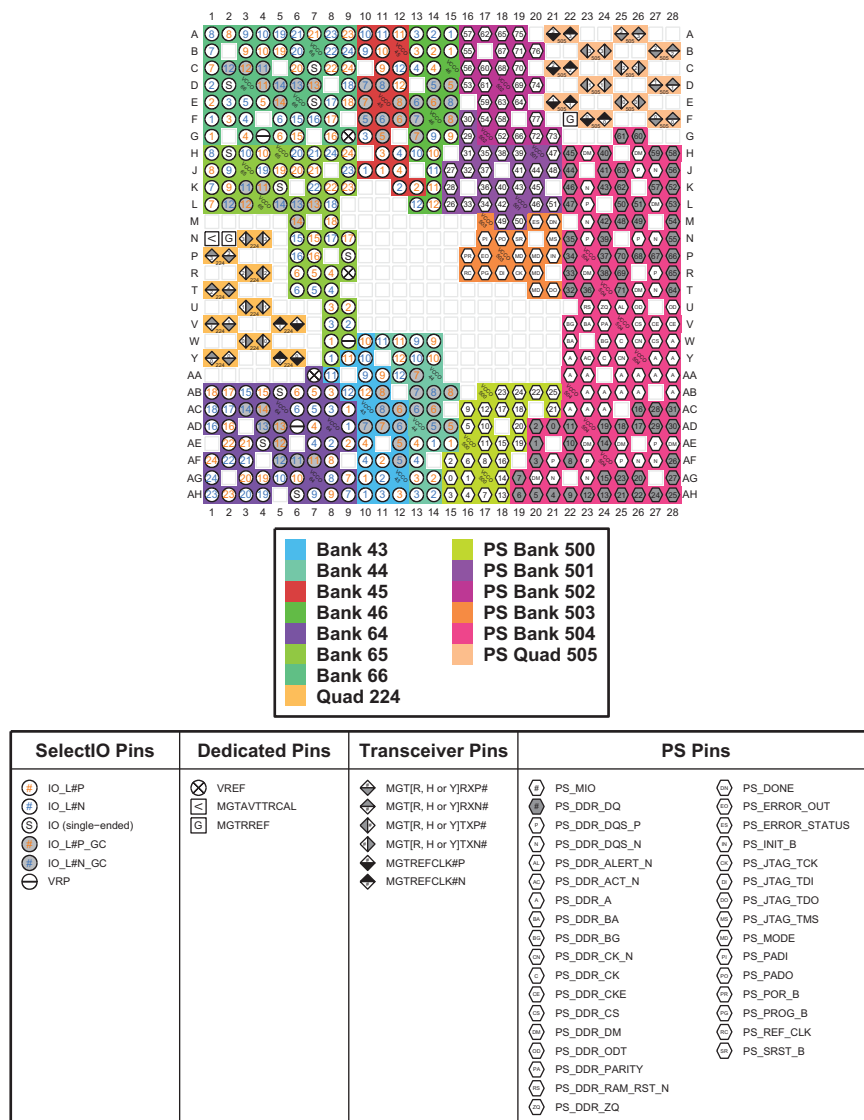


Figure 4-21: SFVC784 Package—XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG I/O Bank Diagram

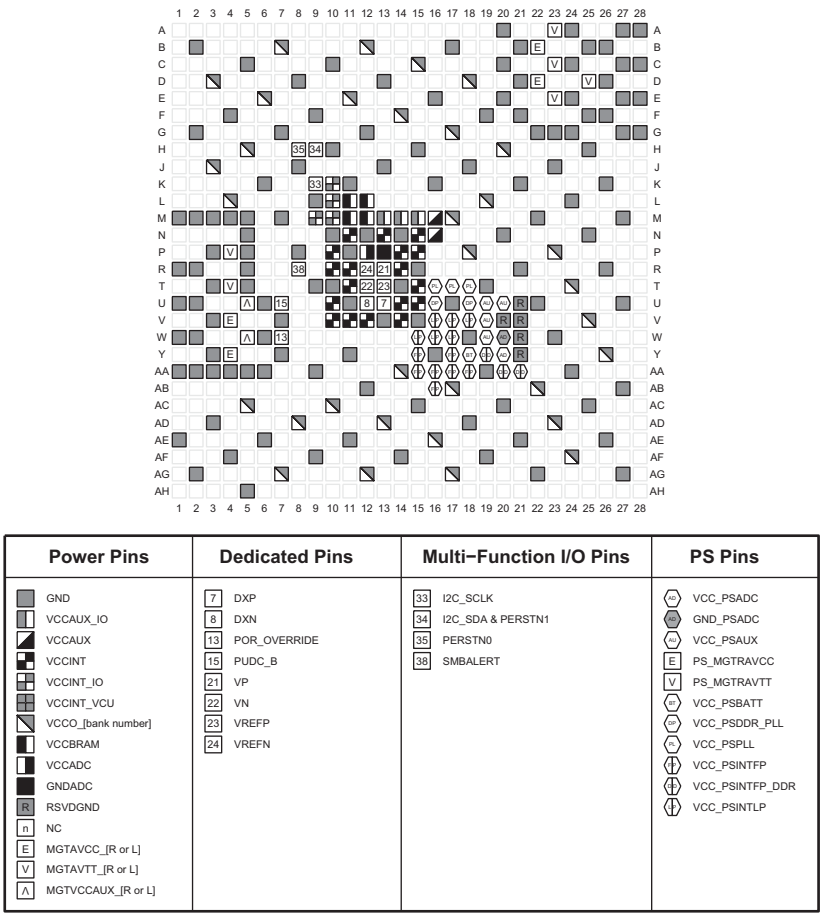


Figure 4-22: SFVC784 Package—XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG Power, Dedicated, and Multi-function Pin Diagram

# SFVC784 Package—XCZU4EV, XCZU5EV, XAZU4EV, and XAZU5EV

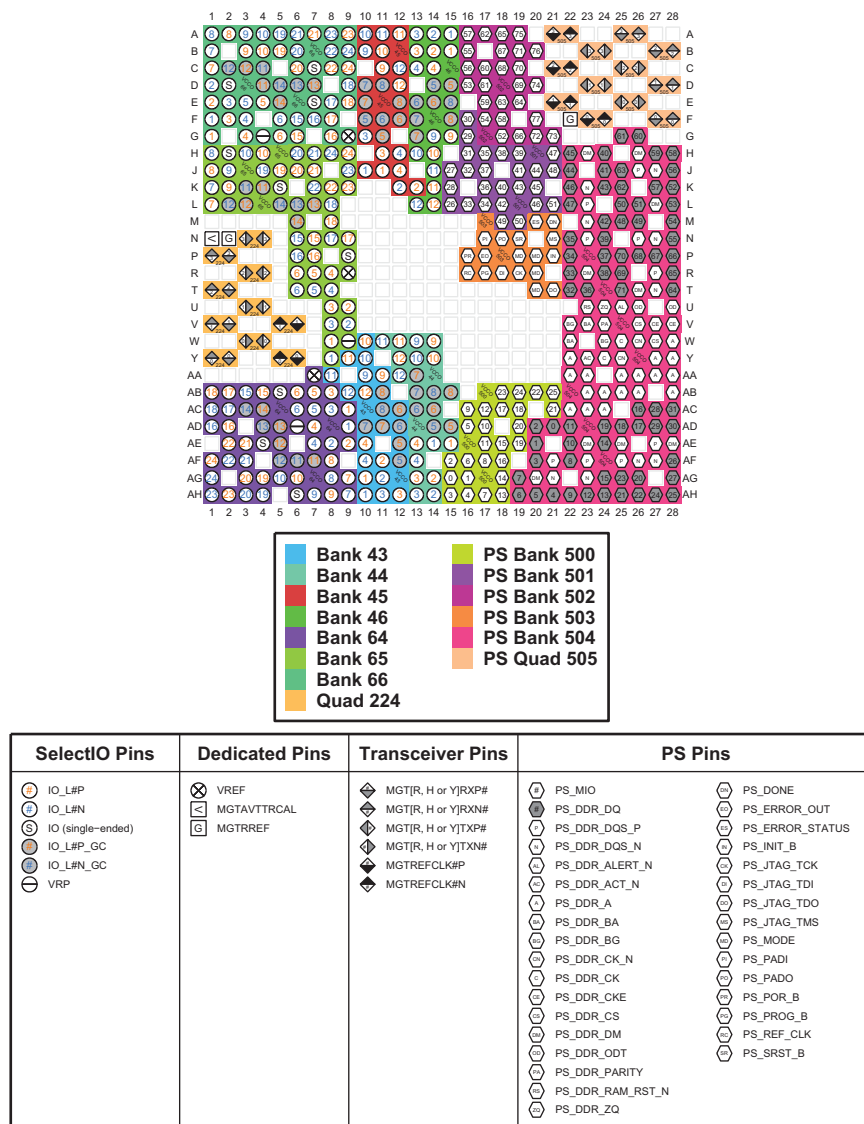


Figure 4-23: SFVC784 Package—XCZU4EV, XCZU5EV, XAZU4EV, and XAZU5EV I/O Bank Diagram

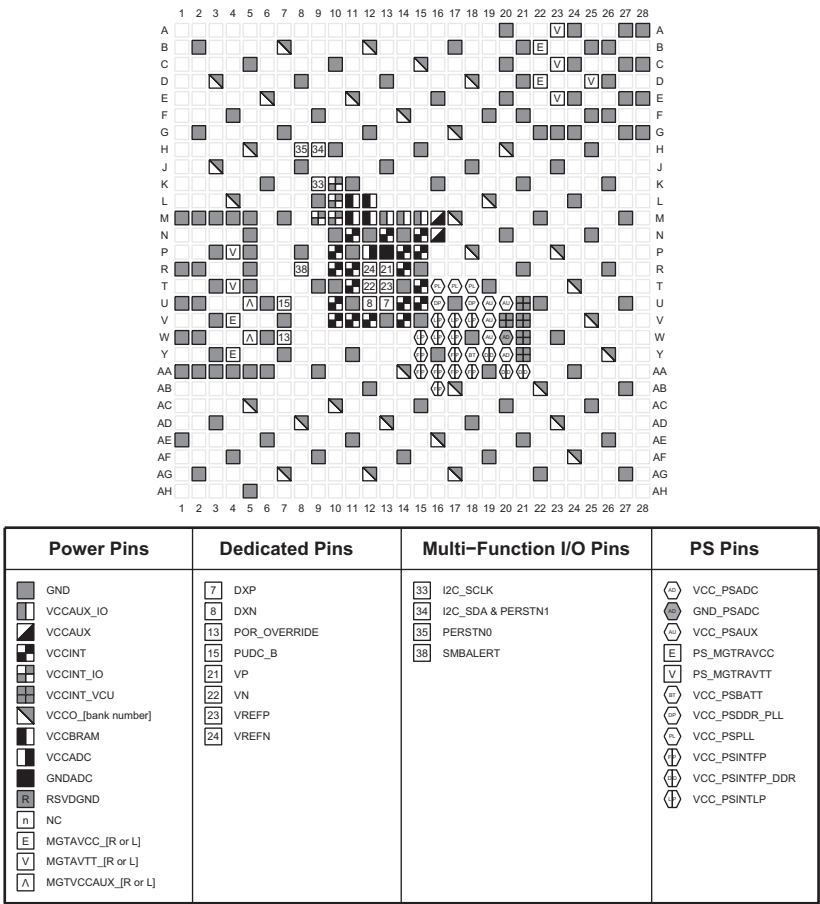
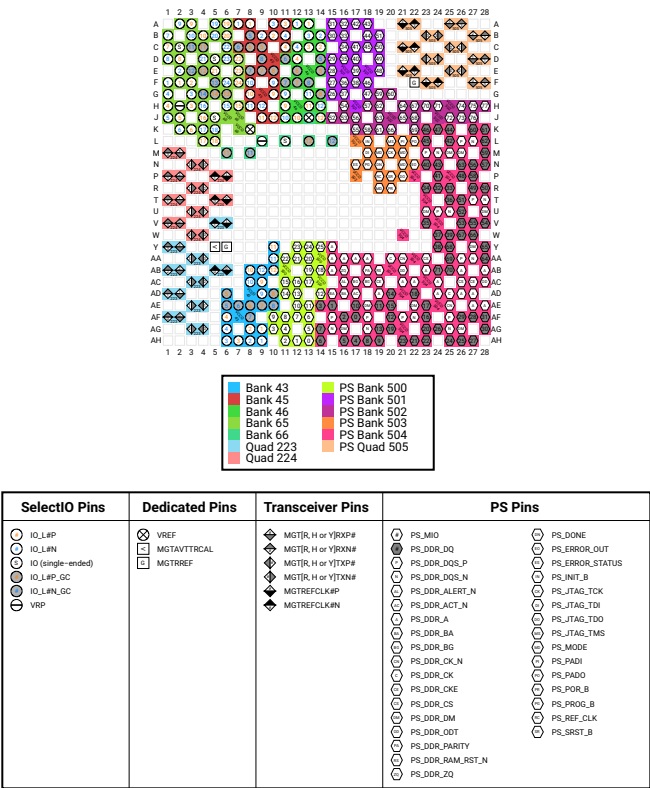


Figure 4-24: SFVC784 Package—XCZU4EV, XCZU5EV, XAZU4EV, and XAZU5EV Power, Dedicated, and Multi-function Pin Diagram

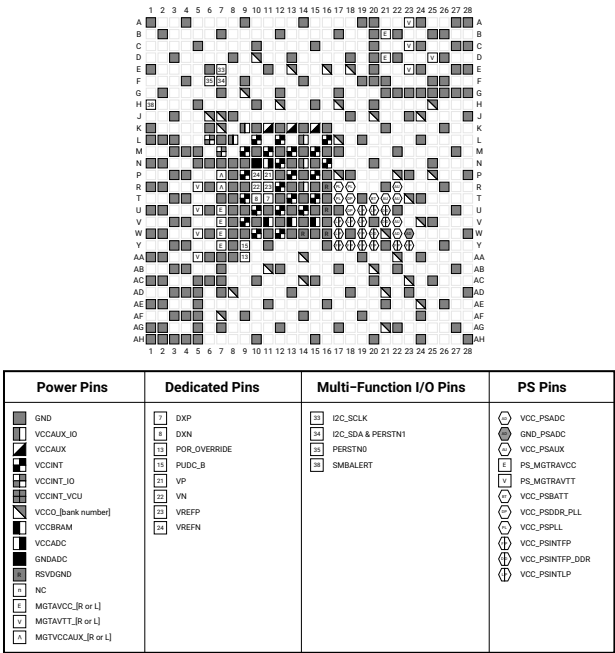
**Note:** VCCAUX\_IO pins for the XQ versions of these devices in this package are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# SFVE784 Package—XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG



X29555-082224

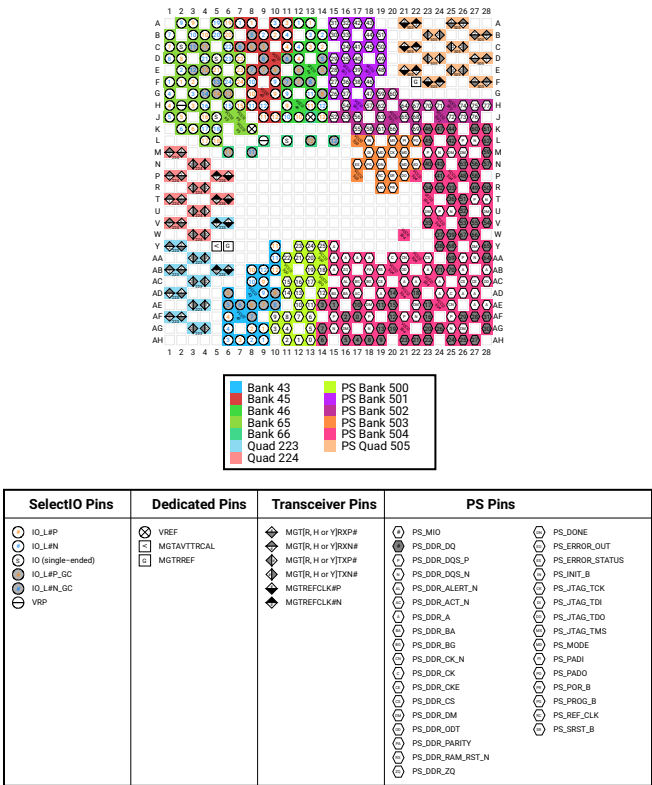
Figure 4-25: SFVE784 Package—XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG I/O Bank Diagram



X29554-082224

Figure 4-26: SFVE784 Package—XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG Power, Dedicated, and Multi-function Pin Diagram

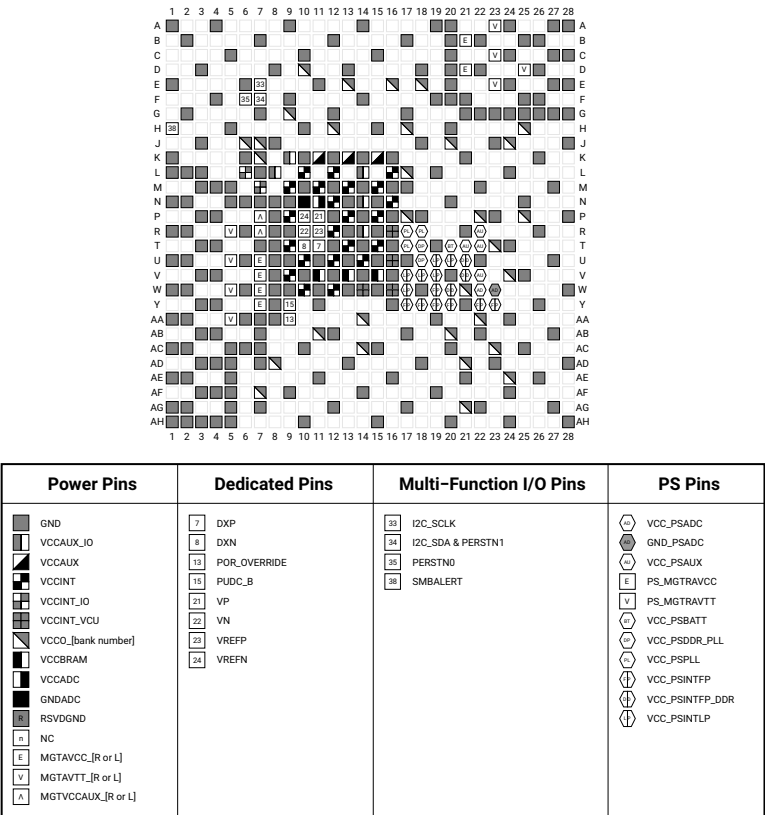
SFVE784 Package—XCZU4EV and XCZU5EV



X29464-072224

Figure 4-27: SFVE784 Package—XCZU4EV and XCZU5EV I/O Bank Diagram





X29461-072224

Figure 4-28: SFVE784 Package—XCZU4EV and XCZU5EV Power, Dedicated, and Multi-function Pin Diagram

# FBVB900 Package—XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG

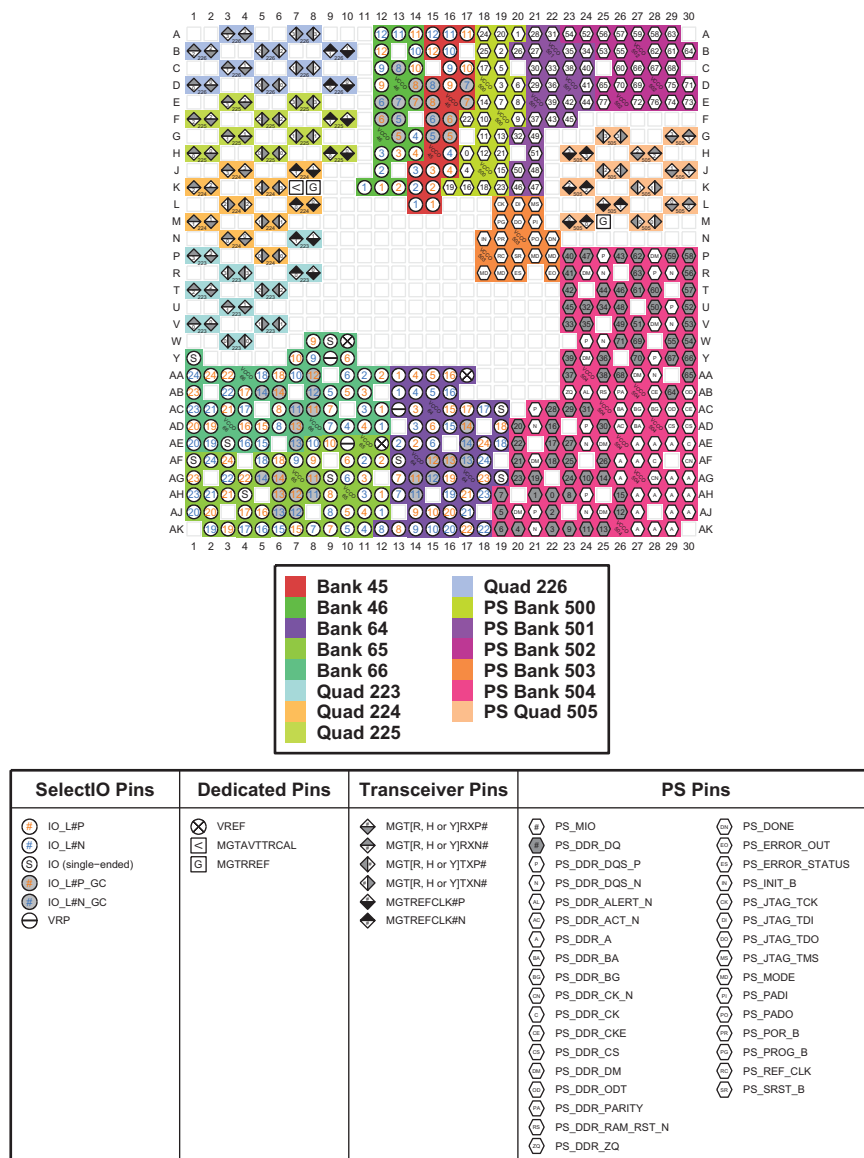


Figure 4-29: FBVB900 Package—XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG I/O Bank Diagram

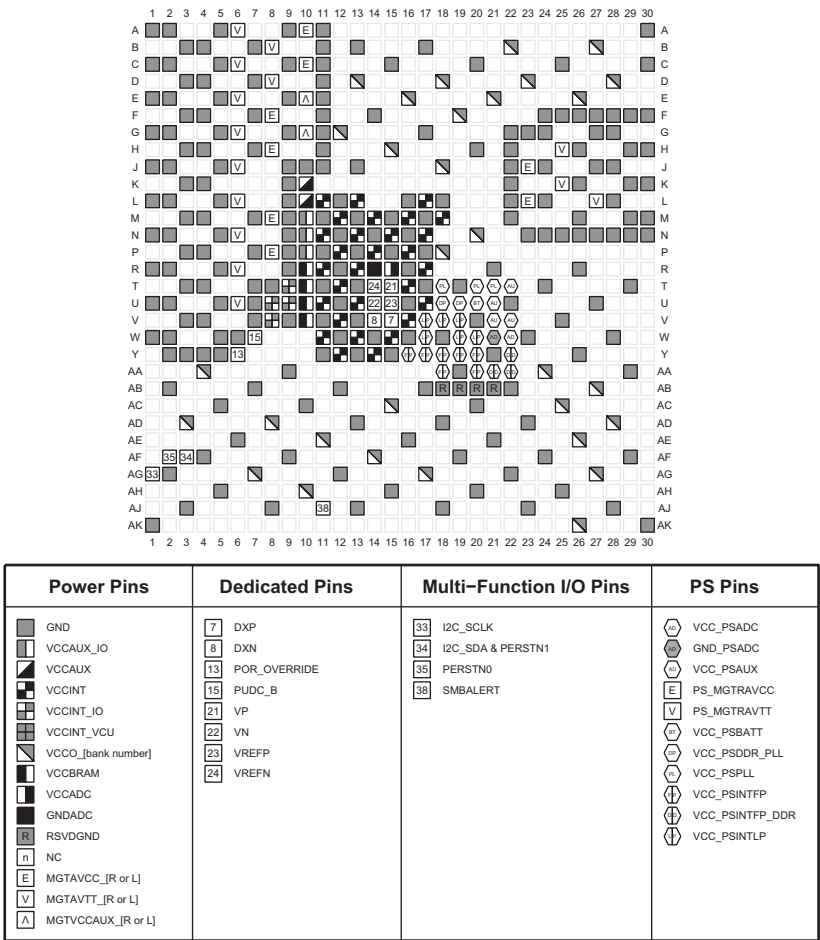


Figure 4-30: FBVB900 Package—XCZU4CG, XCZU4EG, XCZU5CG, and XCZU5EG Power, Dedicated, and Multi-function Pin Diagram

# FBVB900 Package—XCZU4EV and XCZU5EV

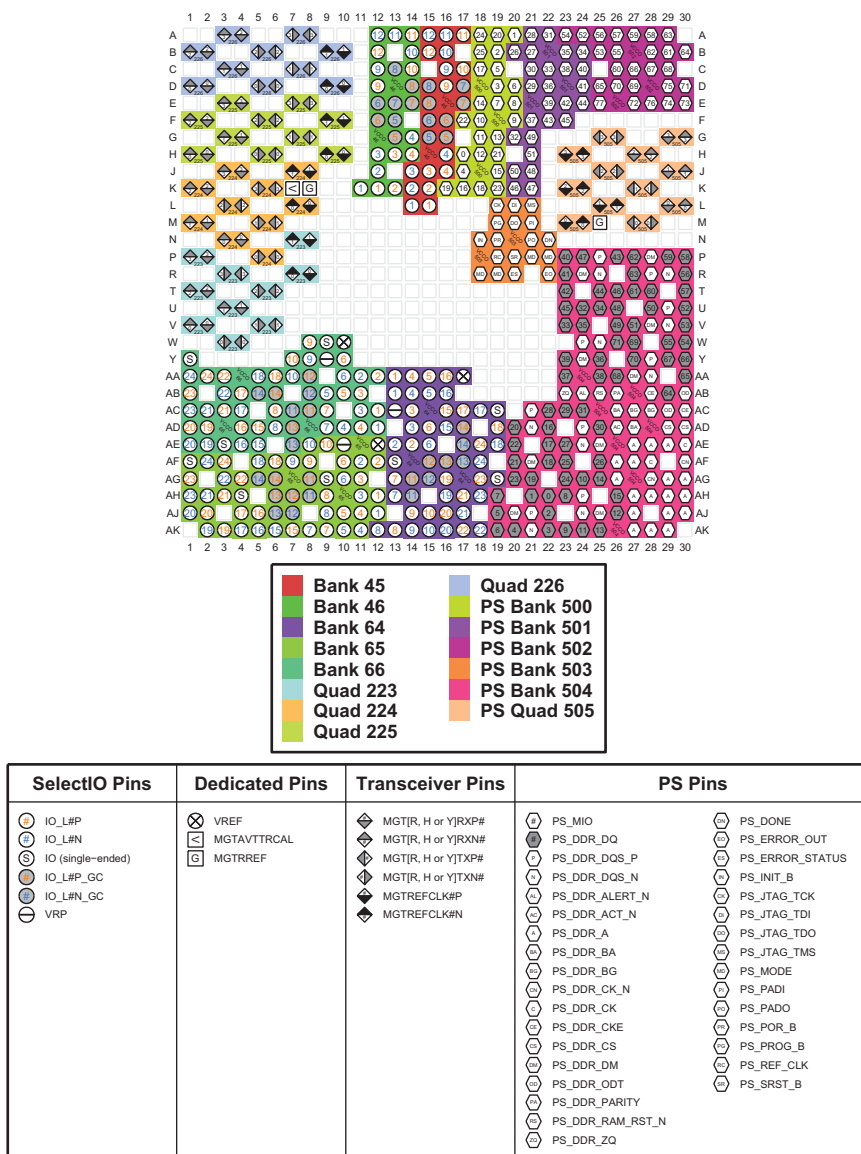


Figure 4-31: FBVB900 Package—XCZU4EV and XCZU5EV I/O Bank Diagram

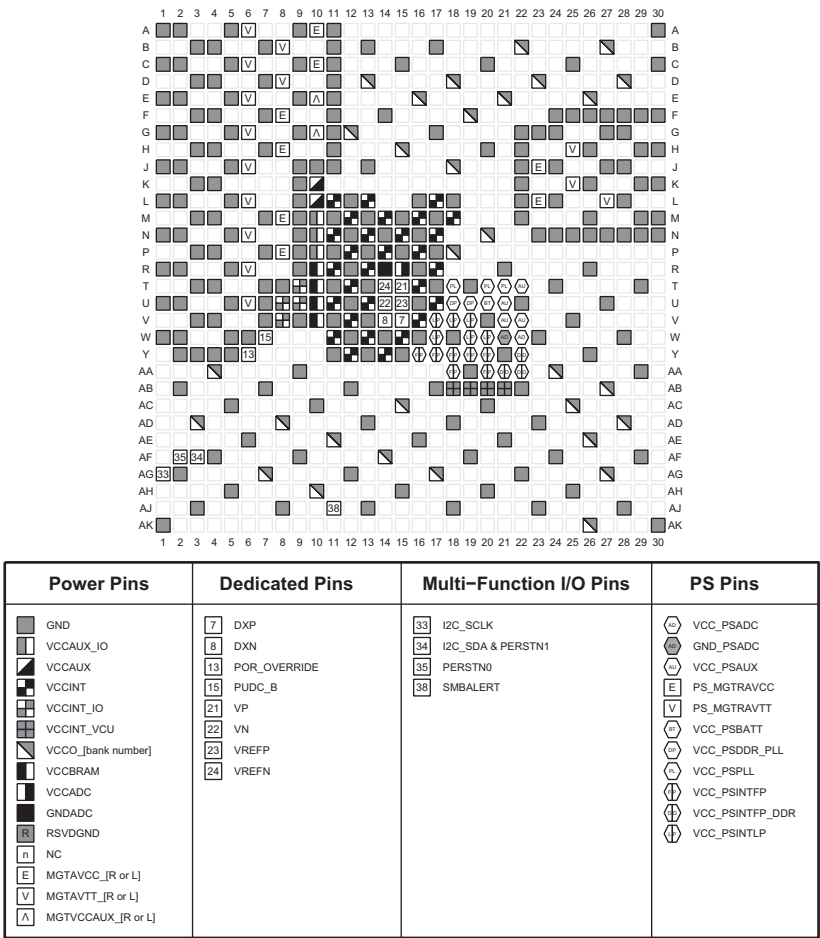


Figure 4-32: FBVB900 Package—XCZU4EV and XCZU5EV  
Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of these devices in this package are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# FBVB900 Package—XCZU7CG and XCZU7EG

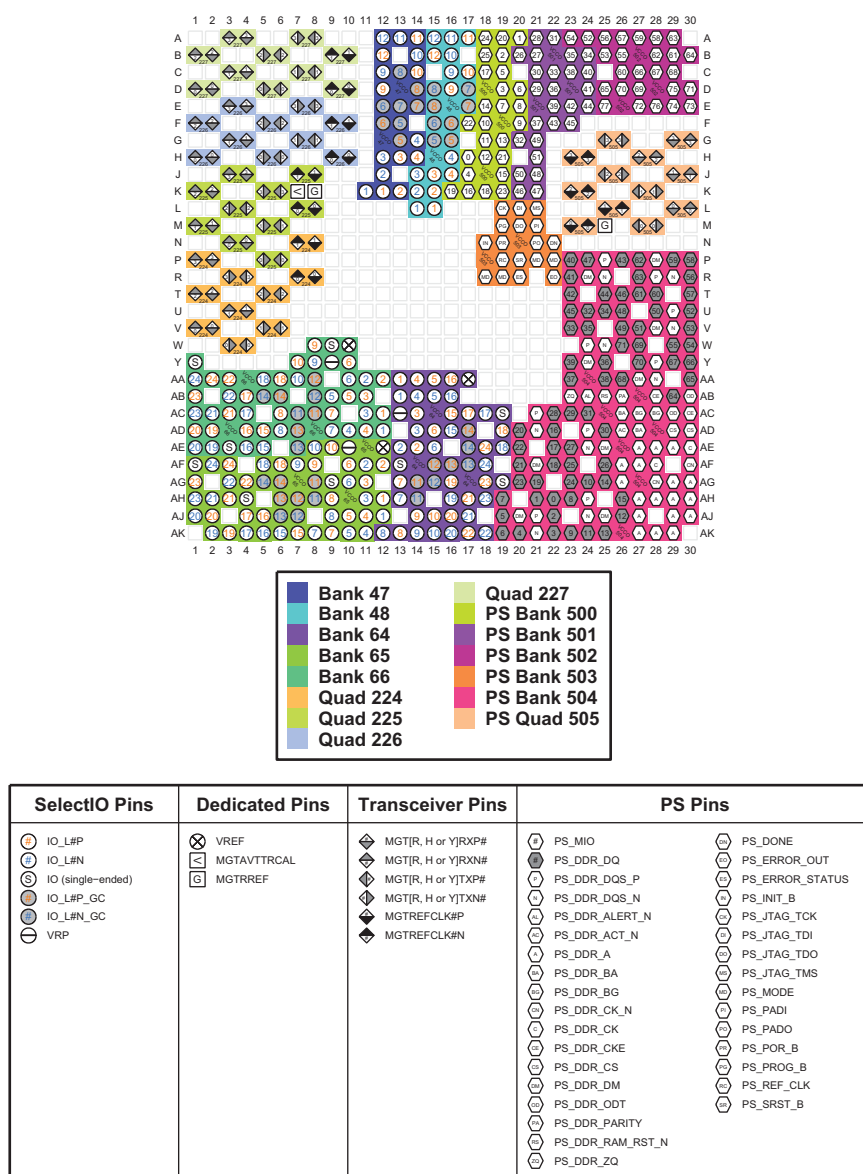


Figure 4-33: FBVB900 Package—I/O Bank Diagram

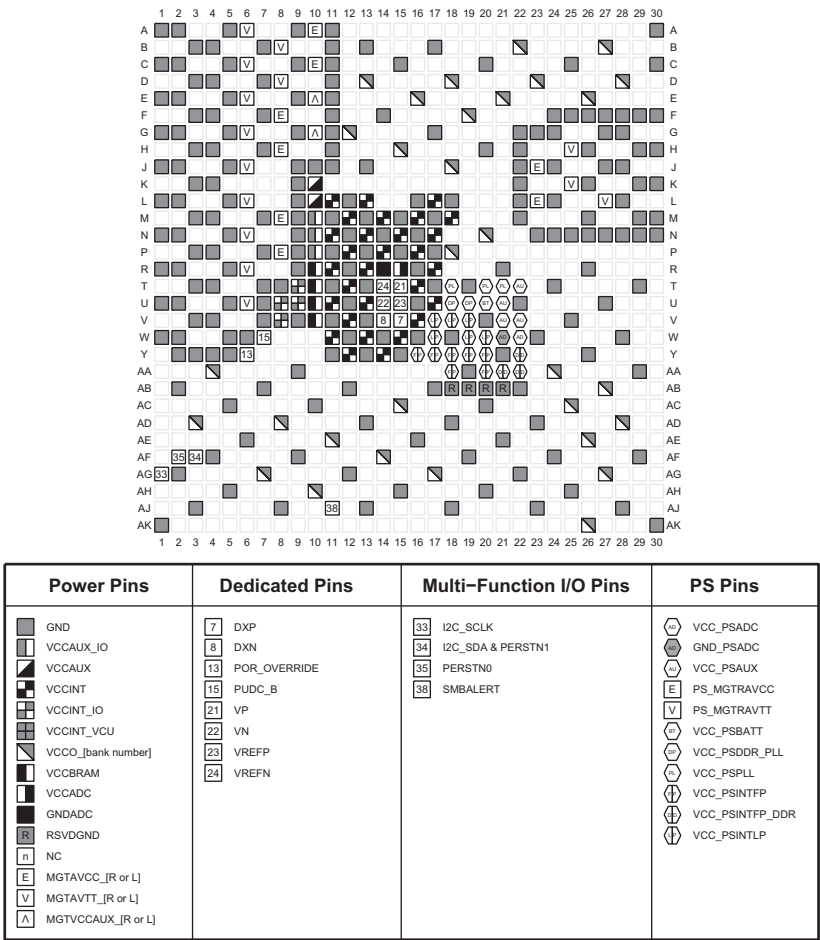


Figure 4-34: FBVB900 Package—XCZU7CG and XCZU7EG  
Power, Dedicated, and Multi-function Pin Diagram

# FBVB900 Package—XCZU7EV

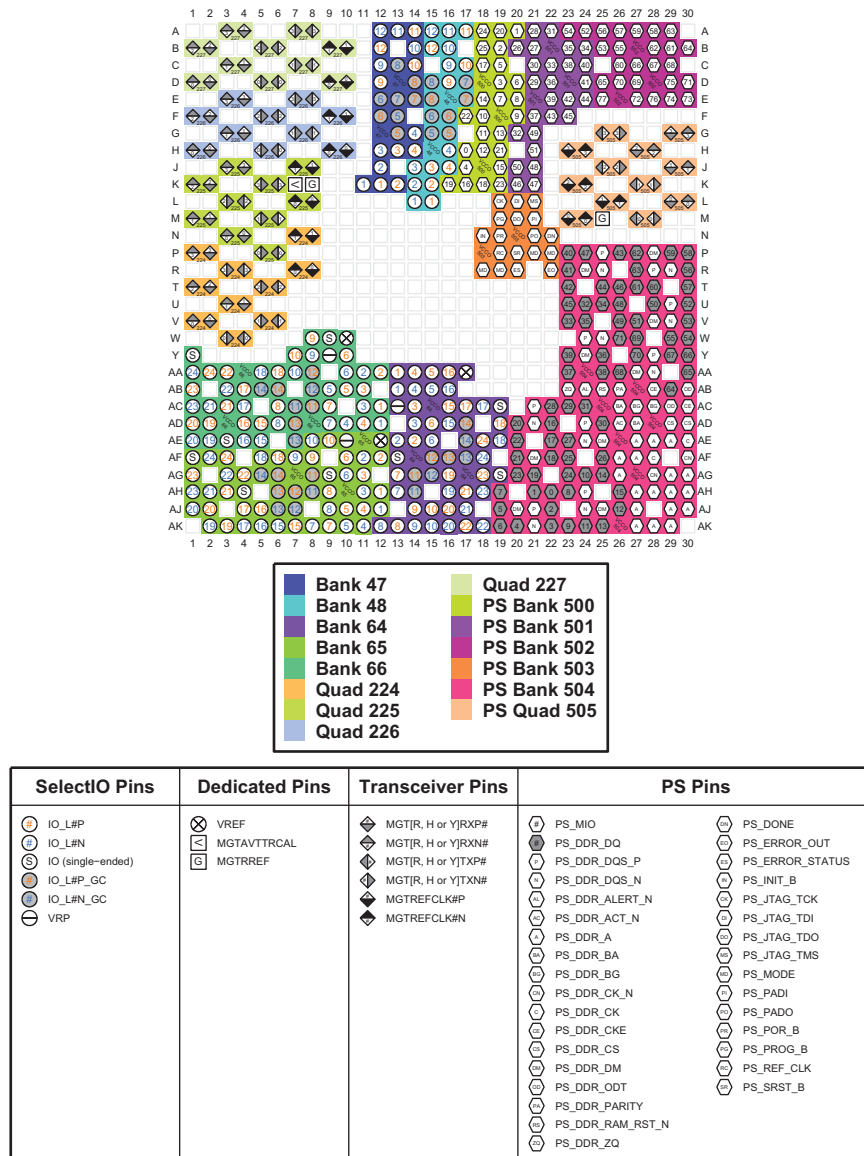


Figure 4-35: FBVB900 Package—XCZU7EV I/O Bank Diagram



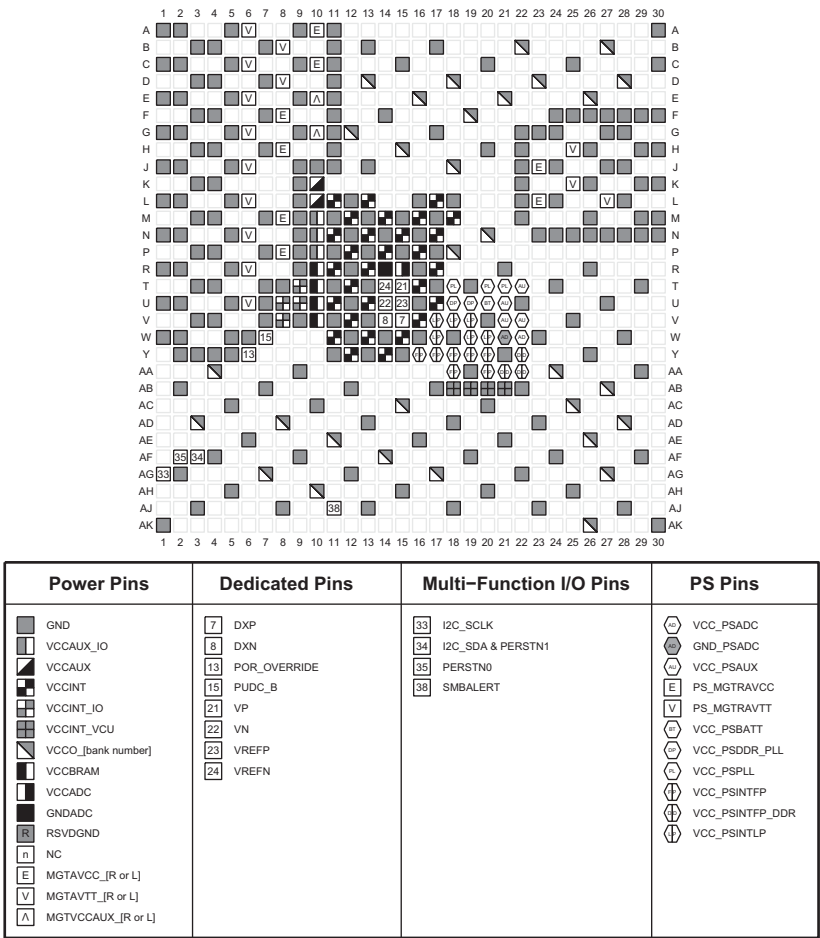


Figure 4-36: FBVB900 Package—XCZU7EV  
Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of these devices in this package are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# FFVC900 Package—XCZU6CG, XCZU6EG, XCZU9CG, XCZU9EG, and XCZU15EG

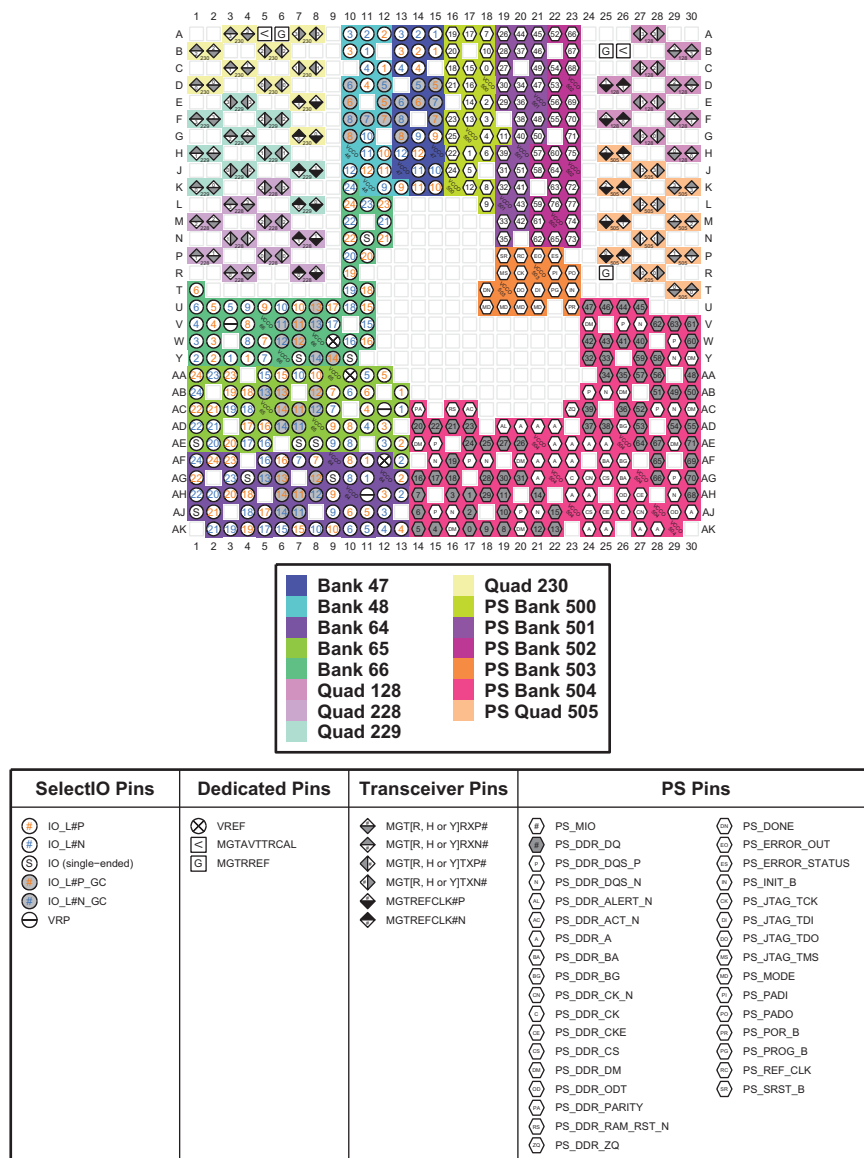


Figure 4-37: FFVC900 Package—XCZU6CG, XCZU6EG, XCZU9CG, XCZU9EG, and XCZU15EG I/O Bank Diagram

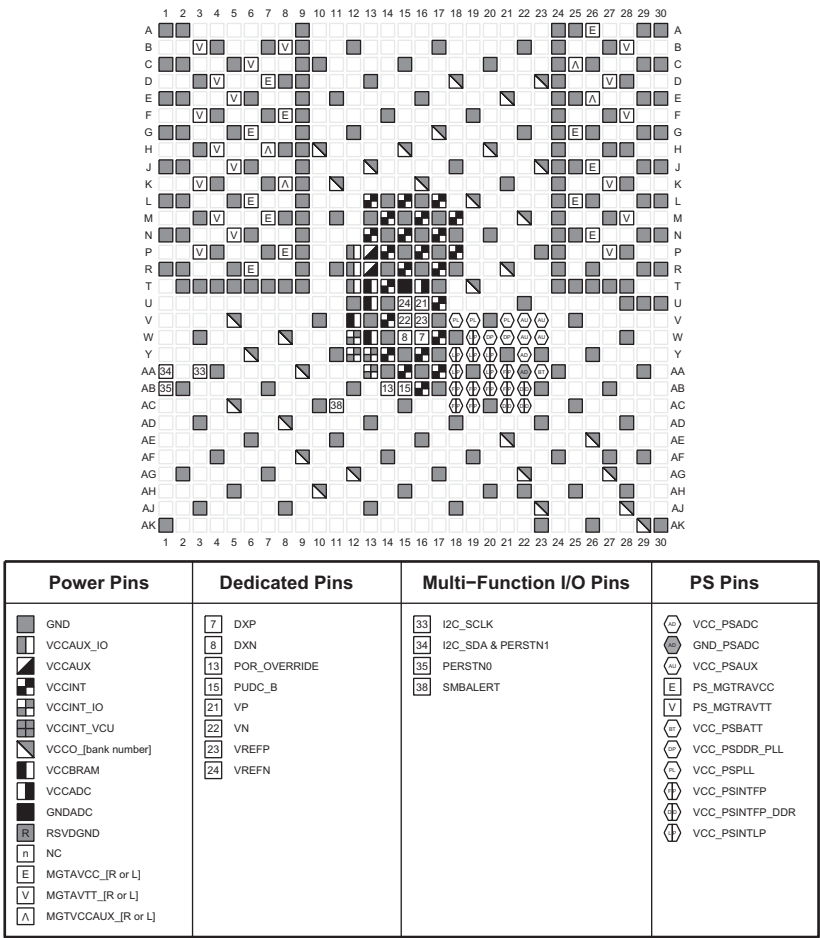


Figure 4-38: FFVC900 Package—XCZU6CG, XCZU6EG, XCZU9CG, XCZU9EG, and XCZU15EG Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of these devices in this package are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# FFVB1156 Package—XCZU6CG, XCZU6EG, XCZU9CG, XCZU9EG, and XCZU15EG

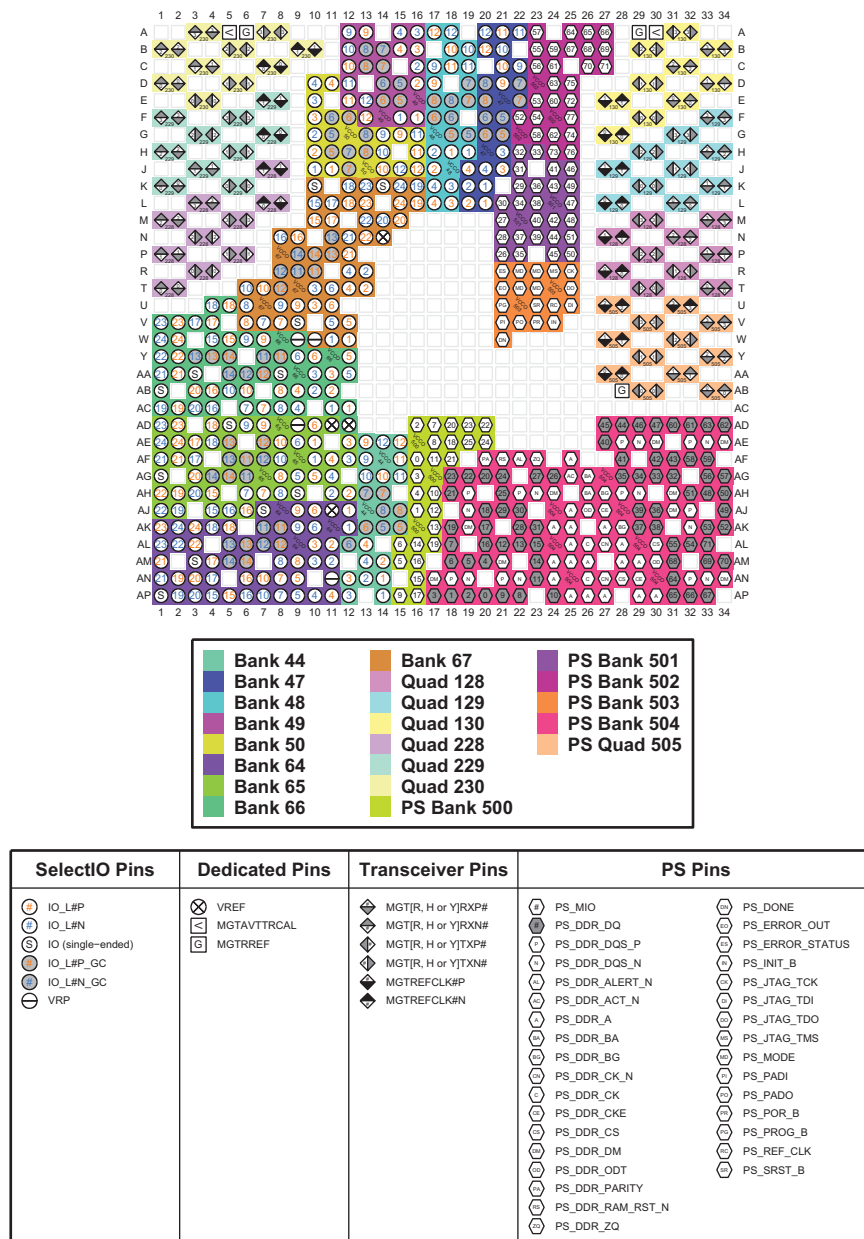


Figure 4-39: FFVB1156 Package—XCZU6CG, XCZU6EG, XCZU9CG, XCZU9EG, and XCZU15EG I/O Bank Diagram

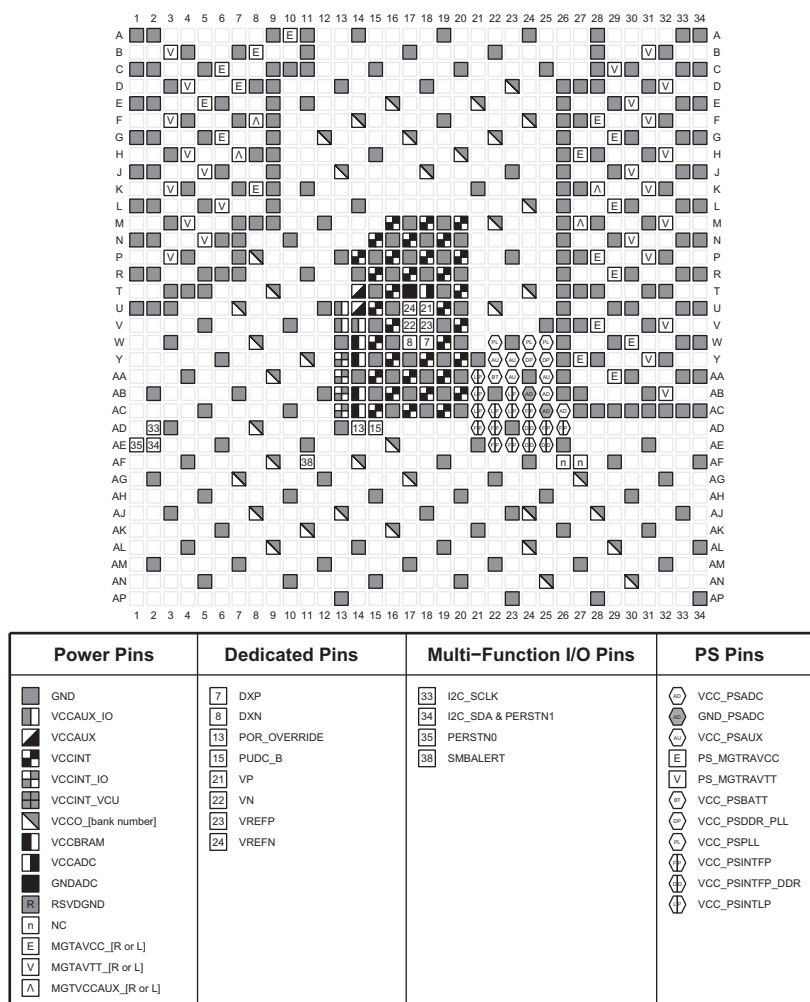


Figure 4-40: FFVB1156 Package—XCZU6CG, XCZU6EG, XCZU9CG, XCZU9EG, and XCZU15EG Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of these devices in this package are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# FFVC1156 Package—XCZU7CG and XCZU7EG

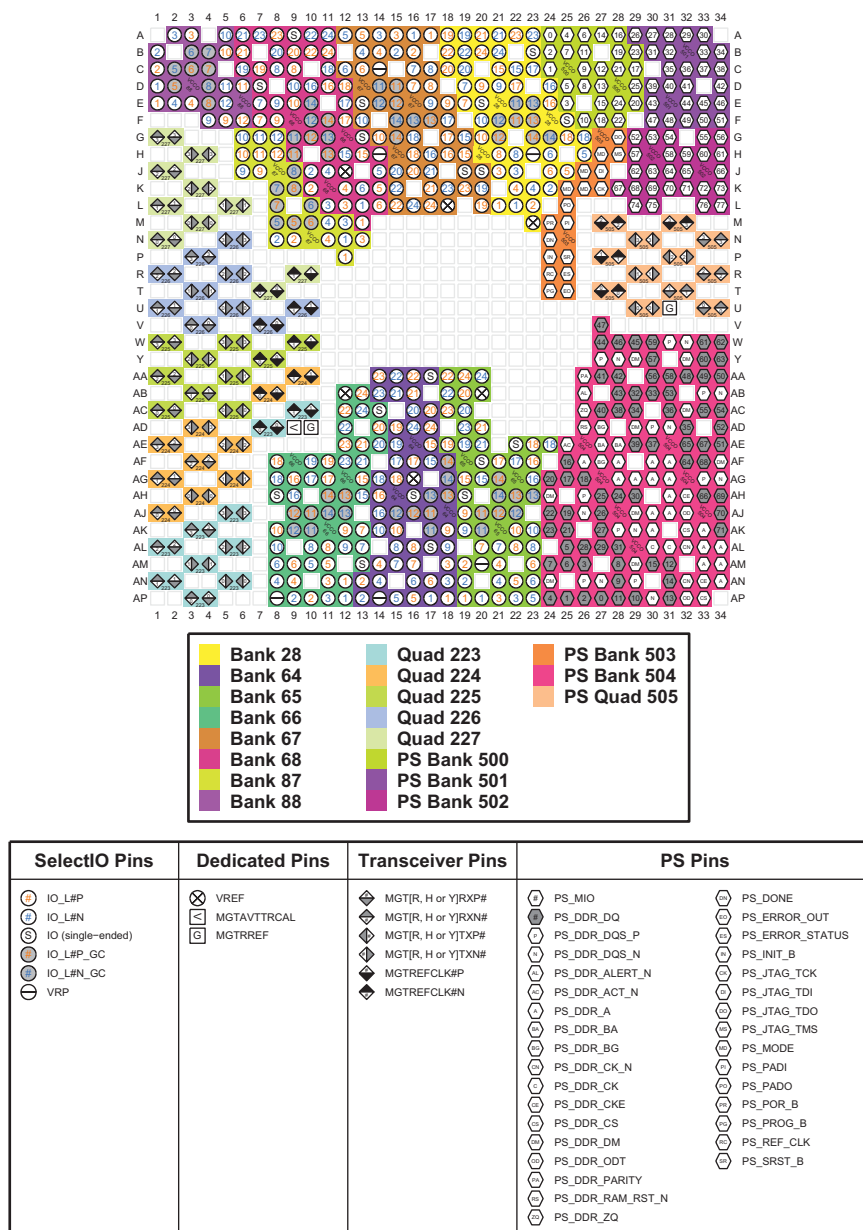


Figure 4-41: FFVC1156 Package—XCZU7CG and XCZU7EG I/O Bank Diagram

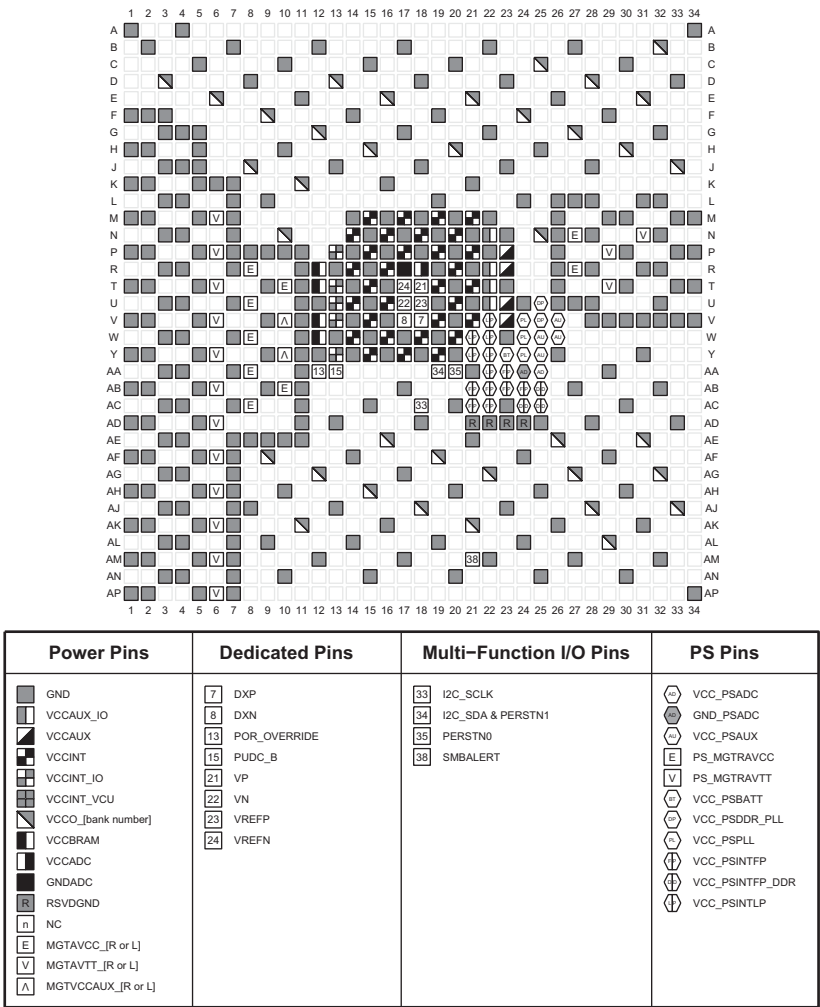


Figure 4-42: FFVC1156 Package—XCZU7CG and XCZU7EG Power, Dedicated, and Multi-function Pin Diagram

# FFVC1156 Package—XCZU7EV

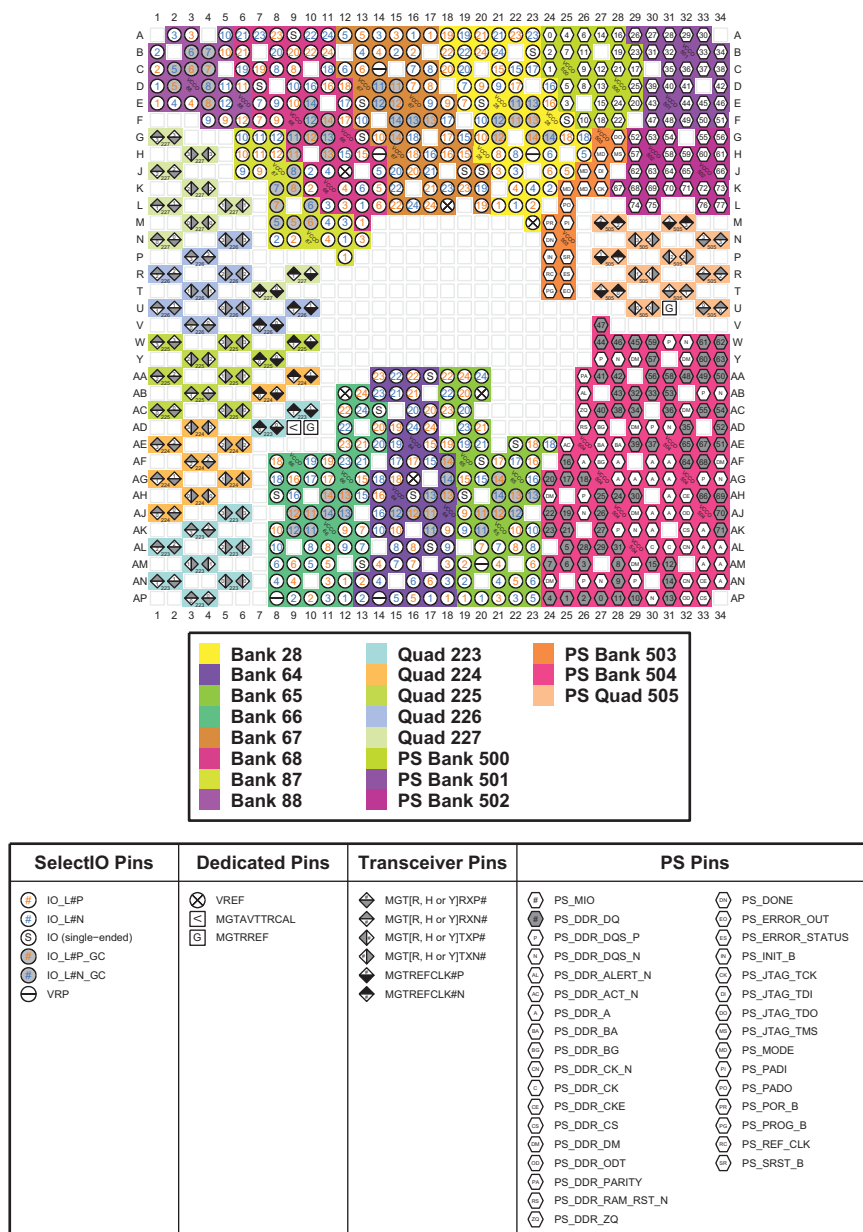


Figure 4-43: FFVC1156 Package—XCZU7EV I/O Bank Diagram



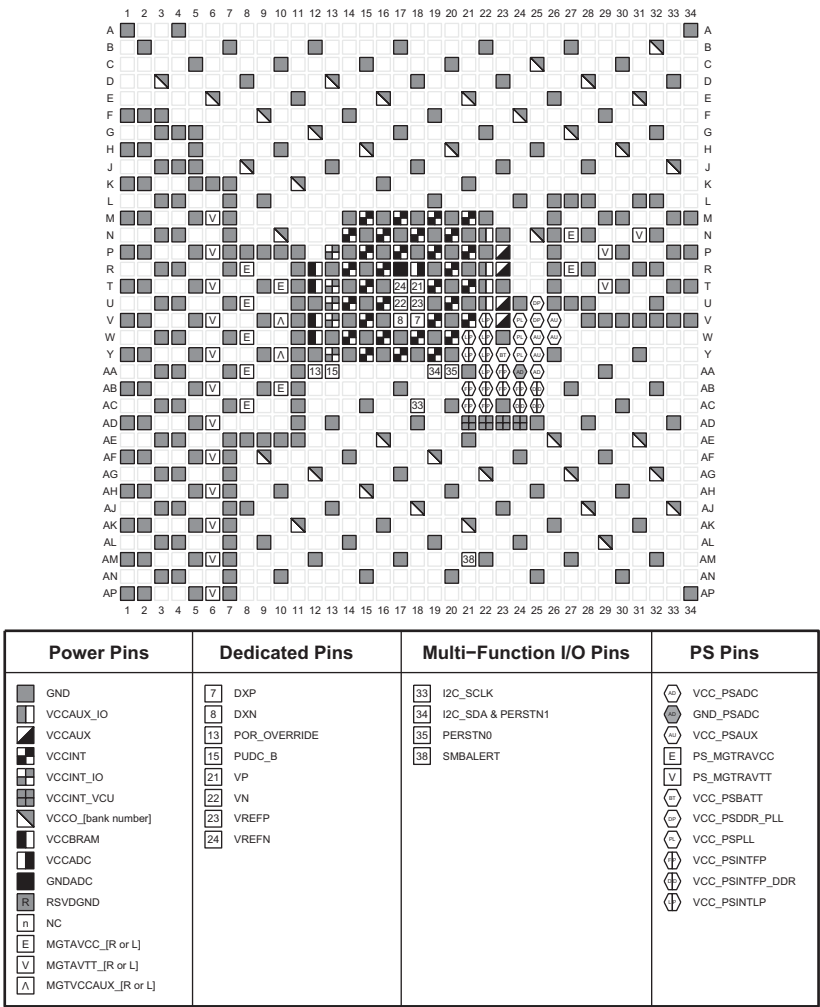


Figure 4-44: FFVC1156 Package—XCZU7EV Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of this device in this package are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# FFVC1156 Package—XCZU11EG

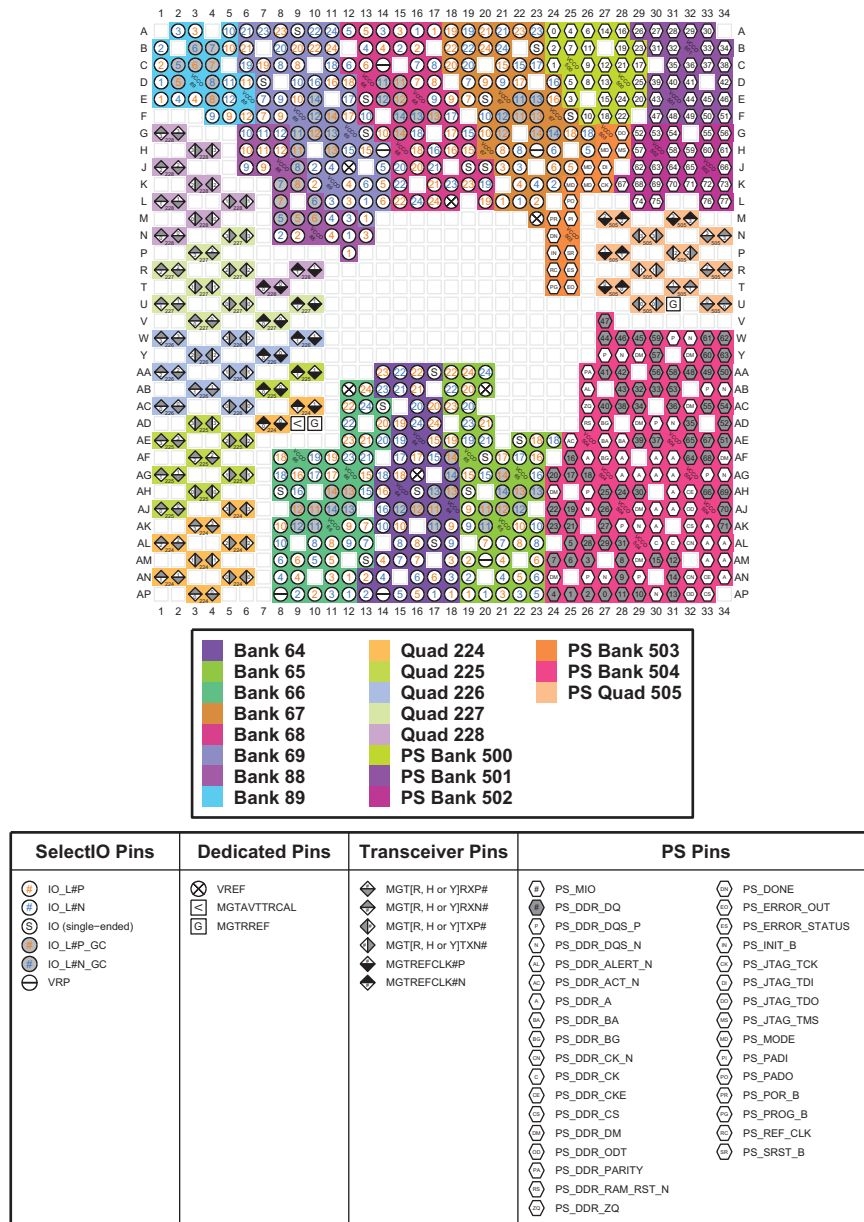


Figure 4-45: FFVC1156 Package—XCZU11EG I/O Bank Diagram

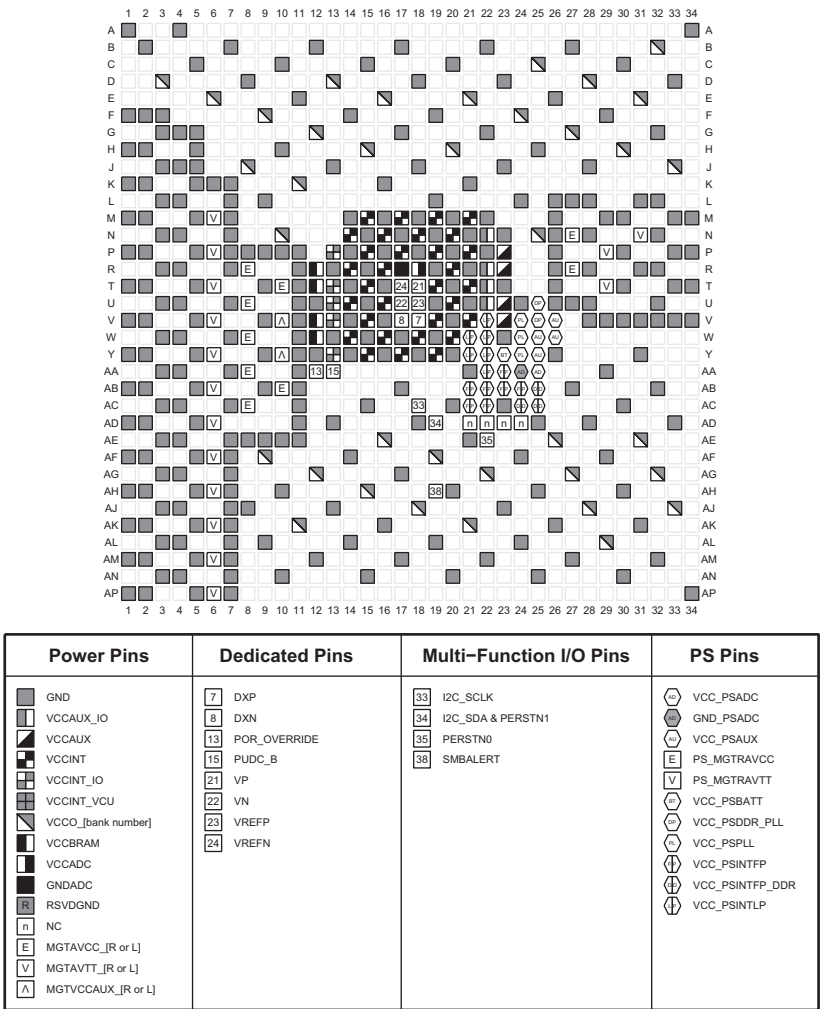


Figure 4-46: FFVC1156 Package—XCZU11EG Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of this device in this package are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# FFVD1156 Package—XCZU21DR

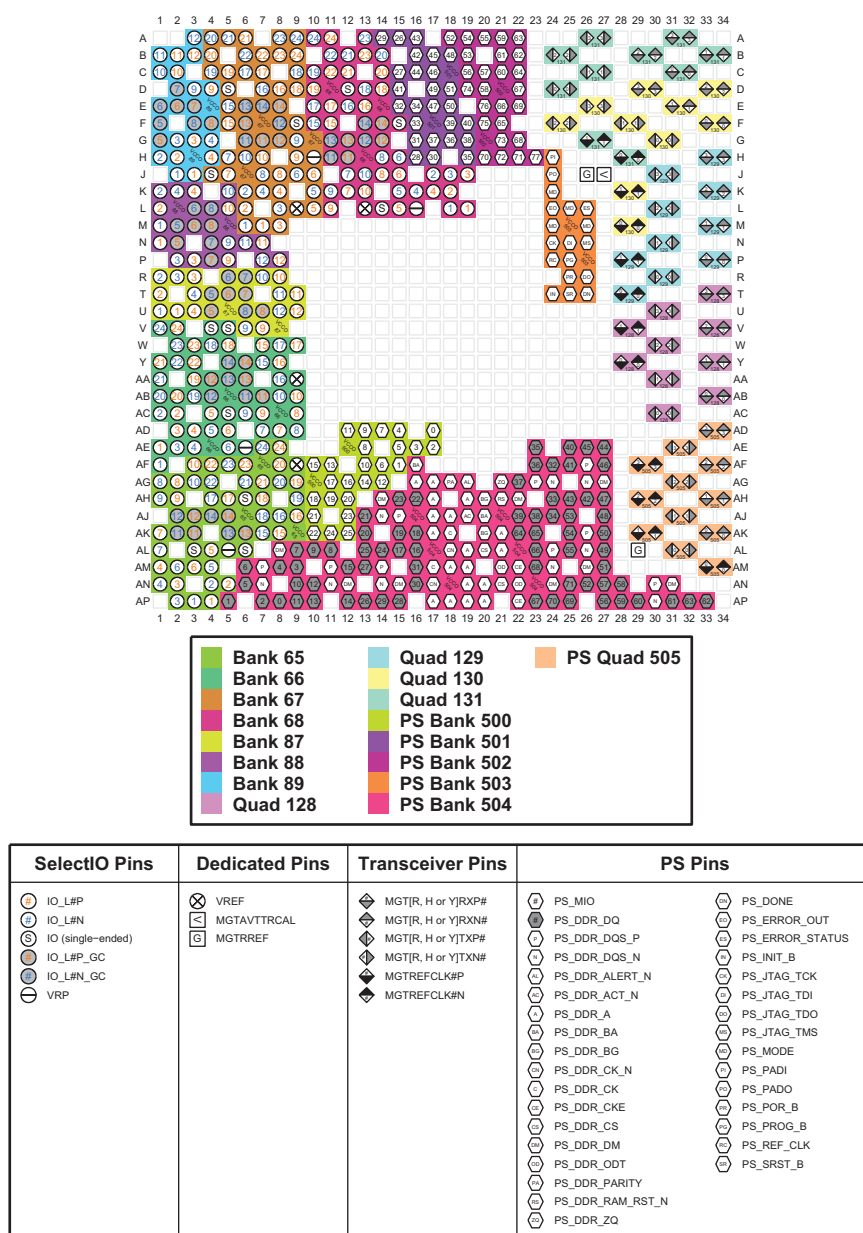


Figure 4-47: FFVD1156 Package—XCZU21DR I/O Bank Diagram

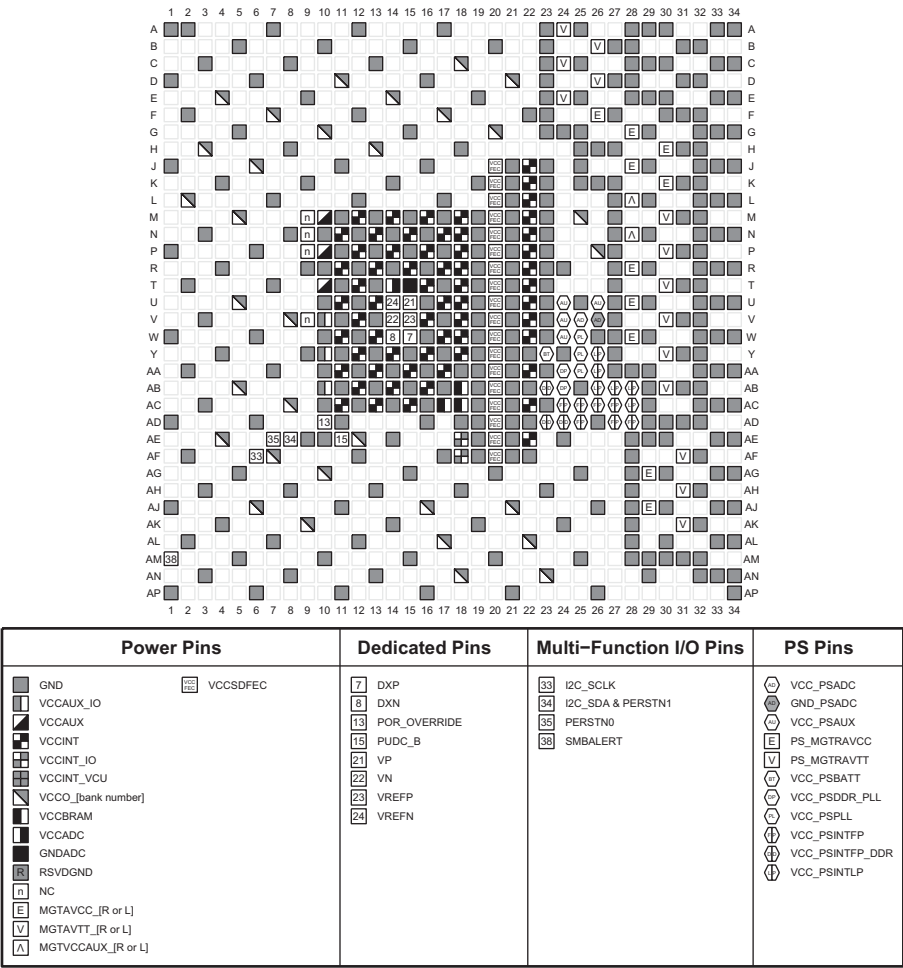


Figure 4-48: FFVD1156 Package—XCZU21DR Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of this device in this package are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# FFVE1156 and FSVE1156 Packages—XCZU25DR

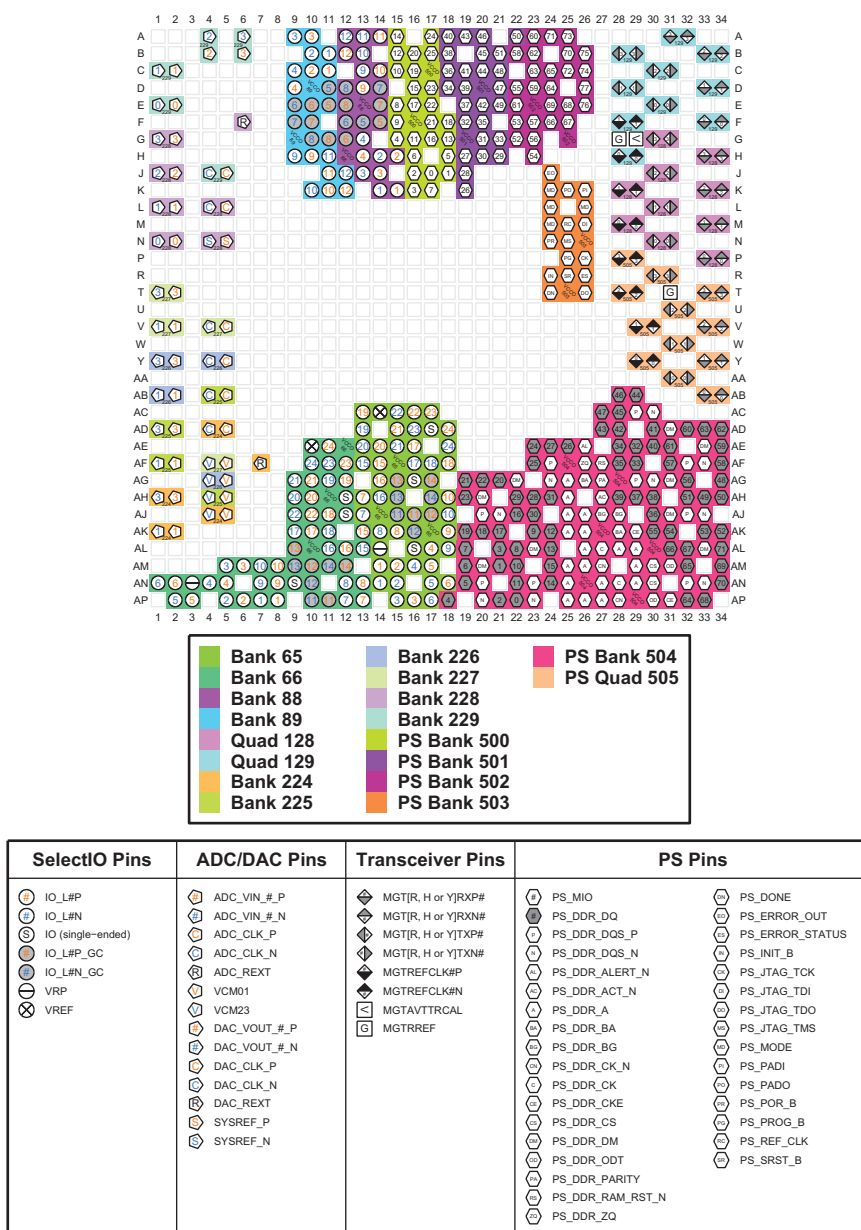


Figure 4-49: FFVE1156 and FSVE1156 Packages—XCZU25DR I/O Bank Diagram

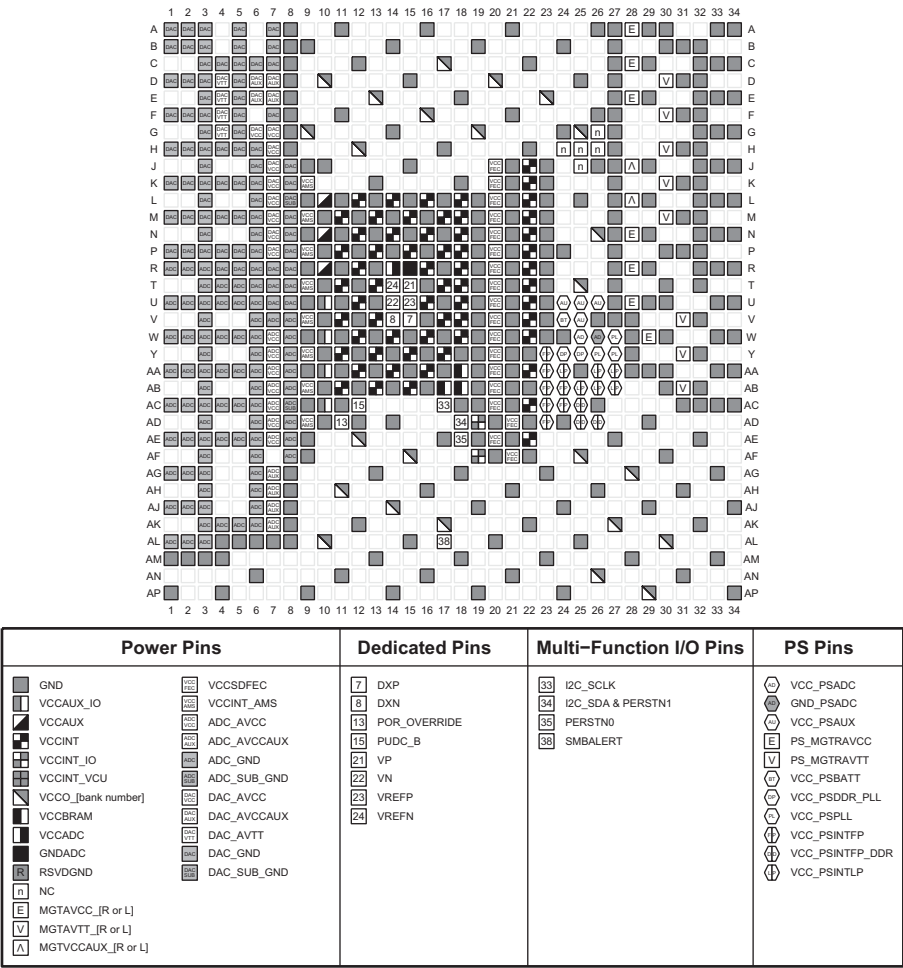


Figure 4-50: FFVE1156 and FSVE1156 Packages—XCZU25DR Power, Dedicated, and Multi-function Pin Diagram

# FFVE1156 and FSVE1156 Packages—XCZU27DR and XCZU28DR

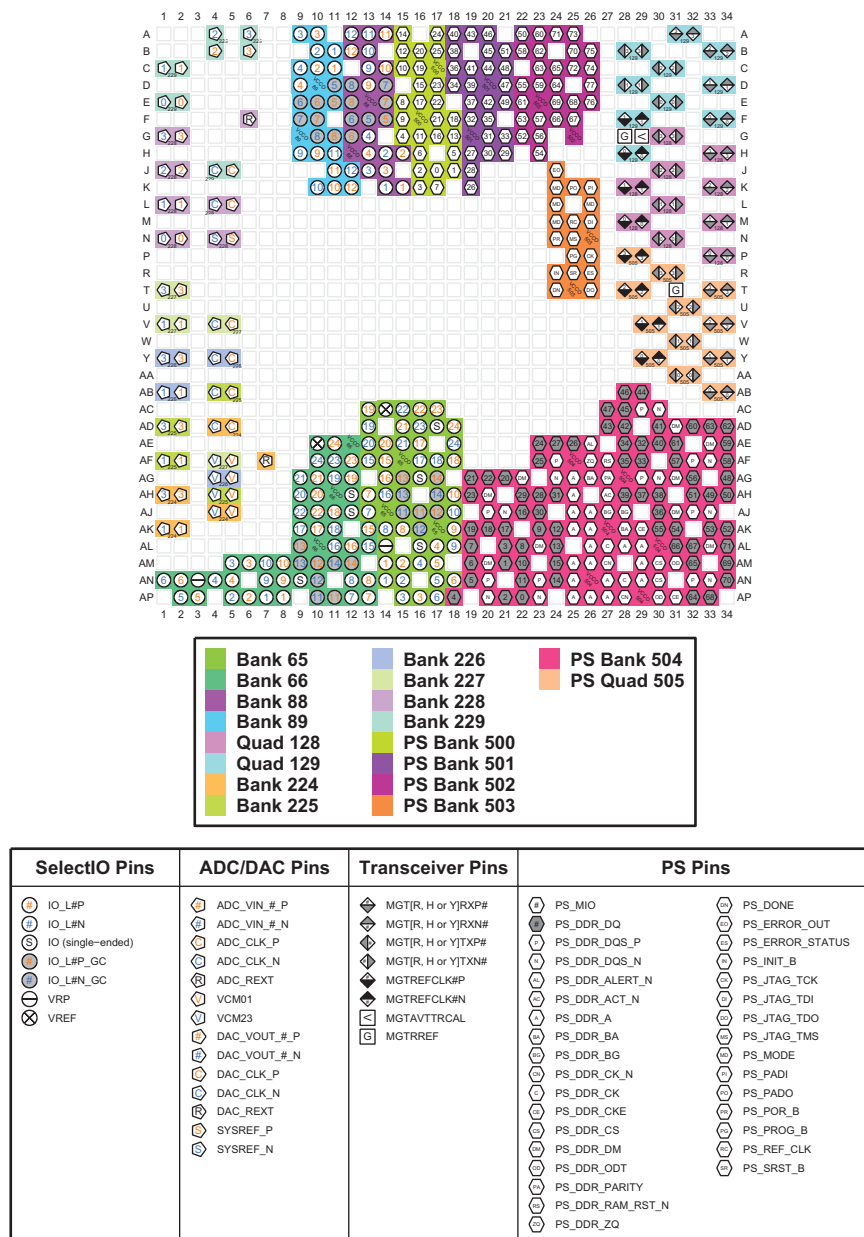


Figure 4-51: FFVE1156 and FSVE1156 Packages—XCZU27DR and XCZU28DR I/O Bank Diagram



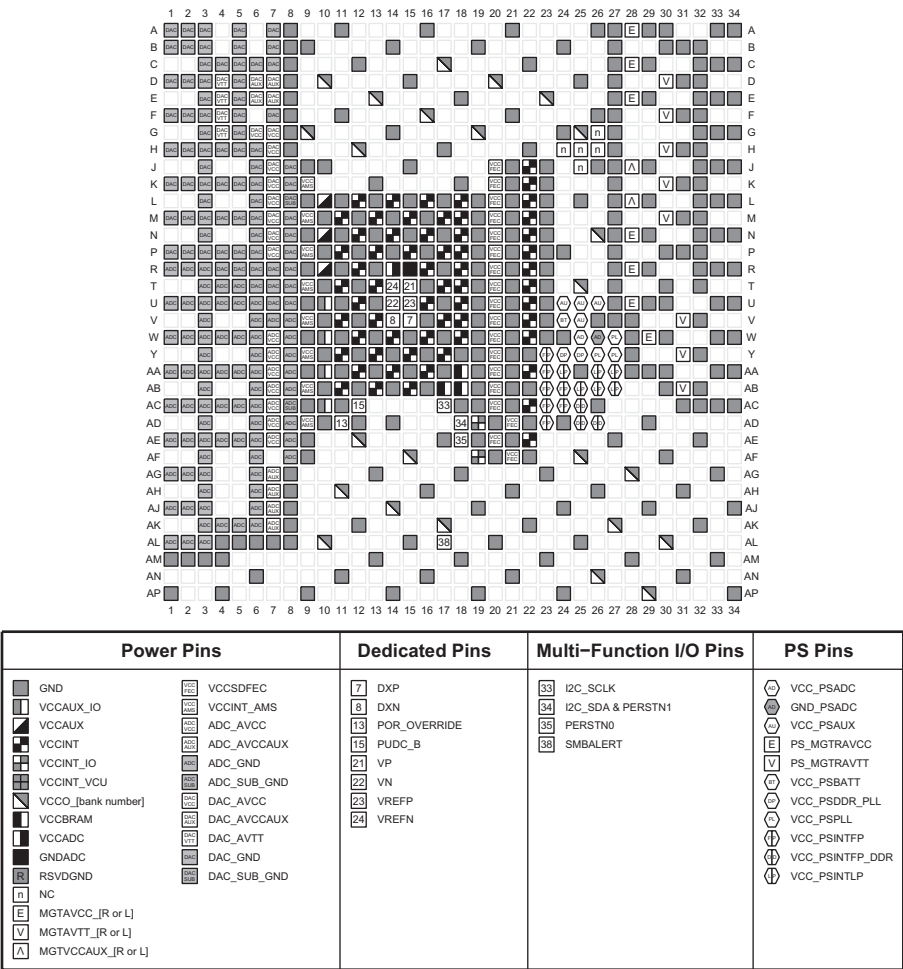


Figure 4-52: FFVE1156 and FSVE1156 Packages—XCZU27DR and XCZU28DR Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of these devices in these packages are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# FFVE1156 and FSVE1156 Packages—XCZU42DR

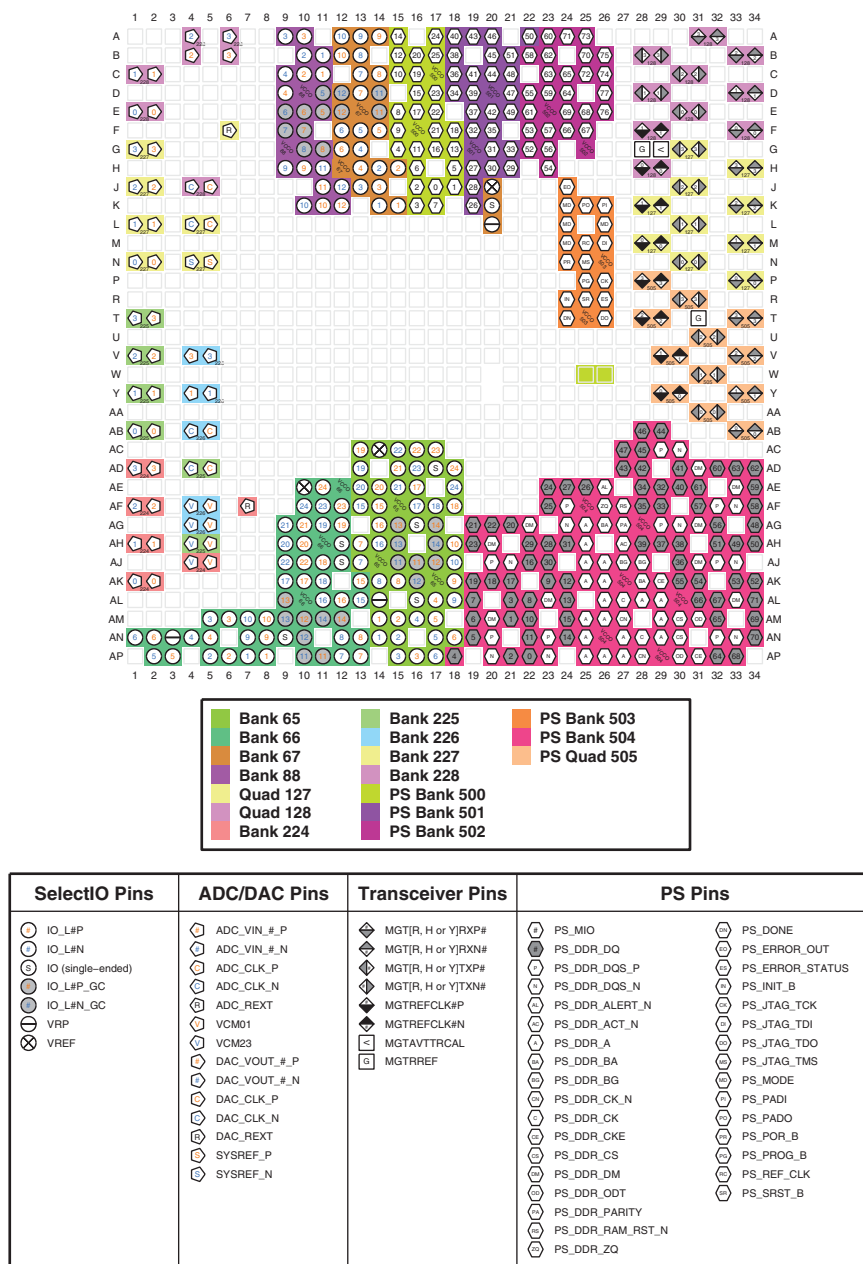


Figure 4-53: FFVE1156 and FSVE1156 Packages—XCZU42DR I/O Bank Diagram

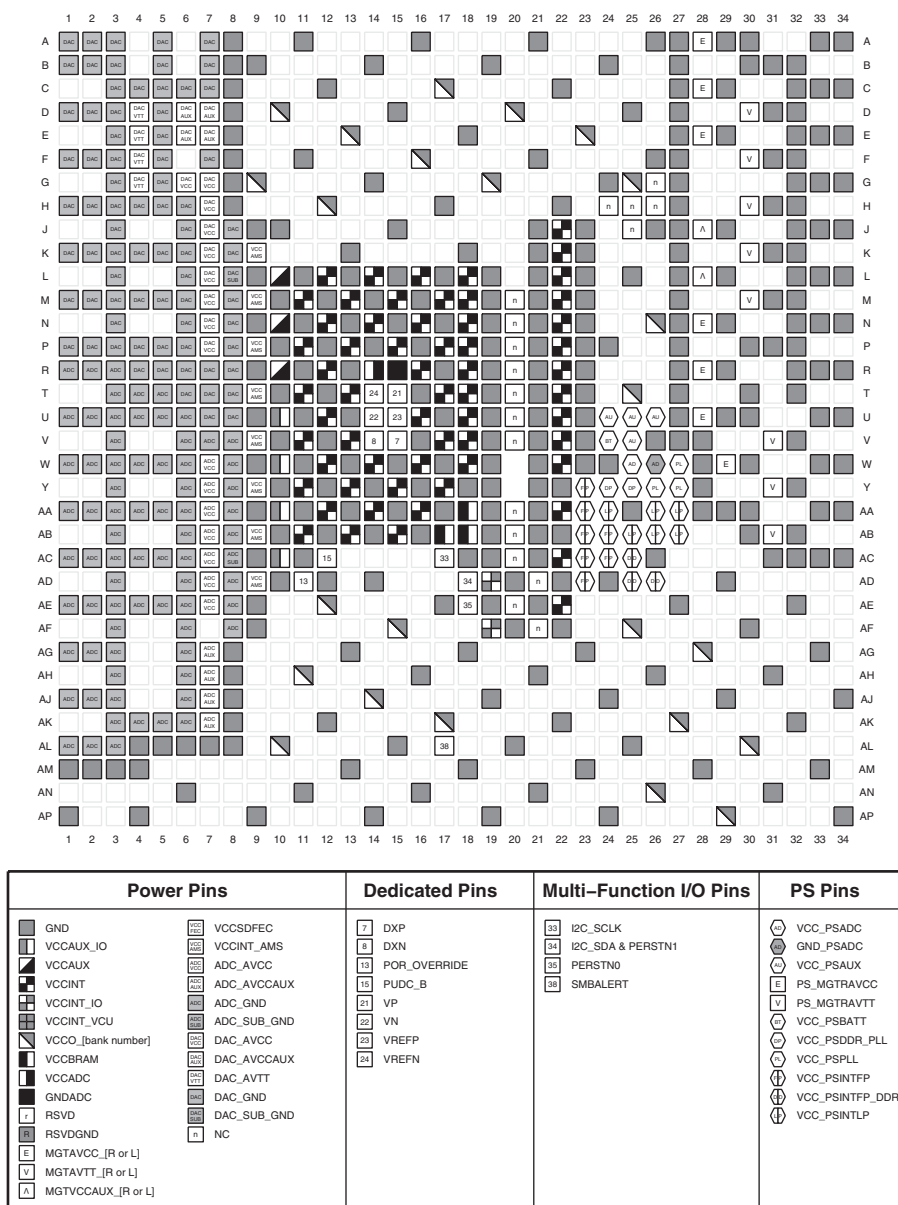


Figure 4-54: FFVE1156 and FSVE1156 Packages—XCZU42DR Power, Dedicated, and Multi-function Pin Diagram

# FFVE1156 and FSVE1156 Packages—XCZU43DR

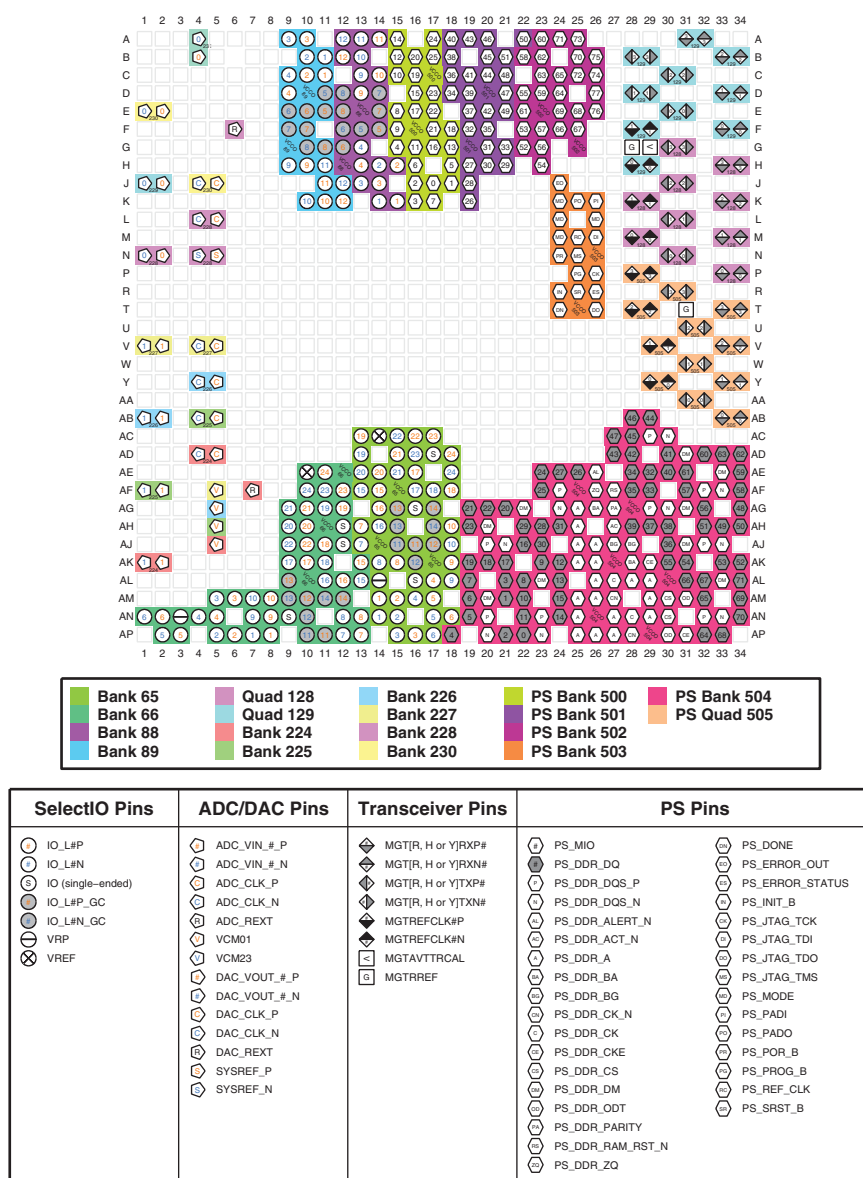


Figure 4-55: FFVE1156 and FSVE1156 Packages—XCZU43DR I/O Bank Diagram

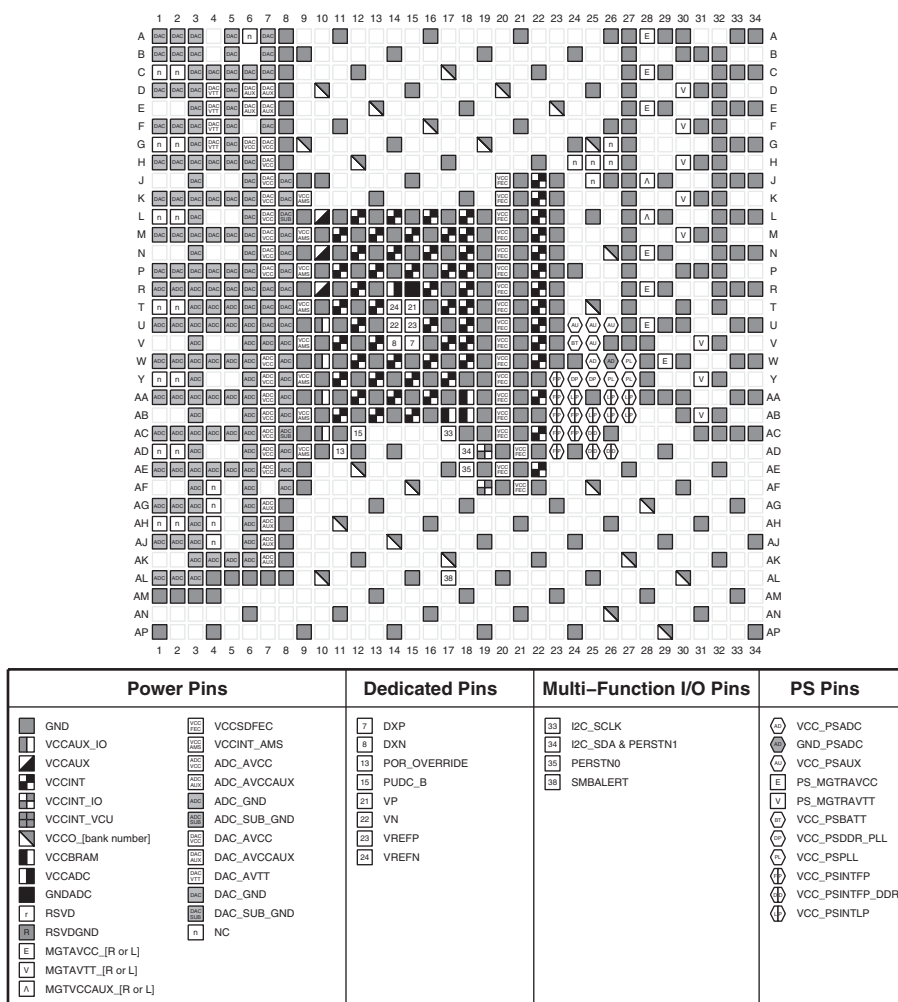


Figure 4-56: FFVE1156 and FSVE1156 Packages—XCZU43DR Power, Dedicated, and Multi-function Pin Diagram

# FFVE1156 and FSVE1156 Packages—XCZU47DR

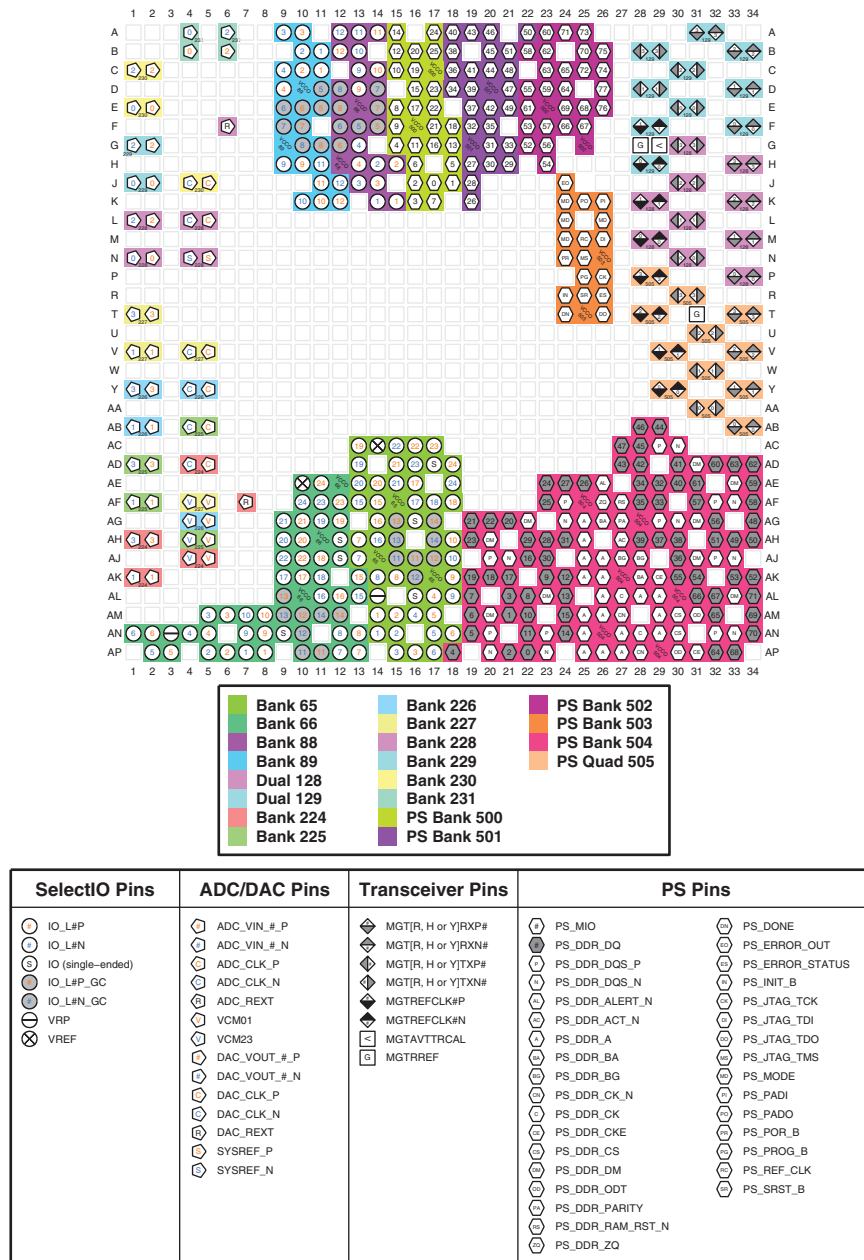
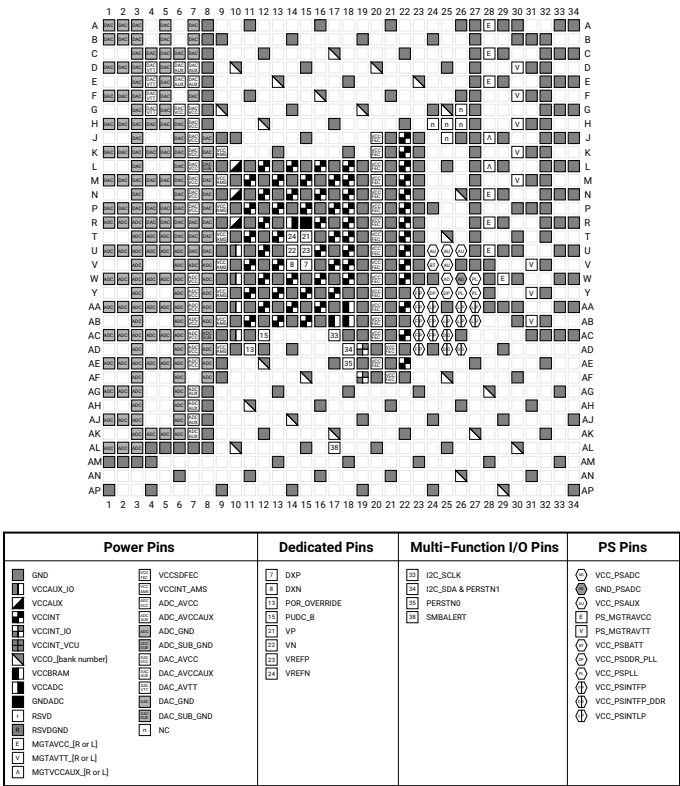


Figure 4-57: FFVE1156 and FSVE1156 Packages—XCZU47DR I/O Bank Diagram



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Figure 4-58: FFVE1156 and FSVE1156 Packages—XCZU47DR Power, Dedicated, and Multi-function Pin Diagram

# FFVE1156 and FSVE1156 Packages—XCZU48DR and XQZU48DR

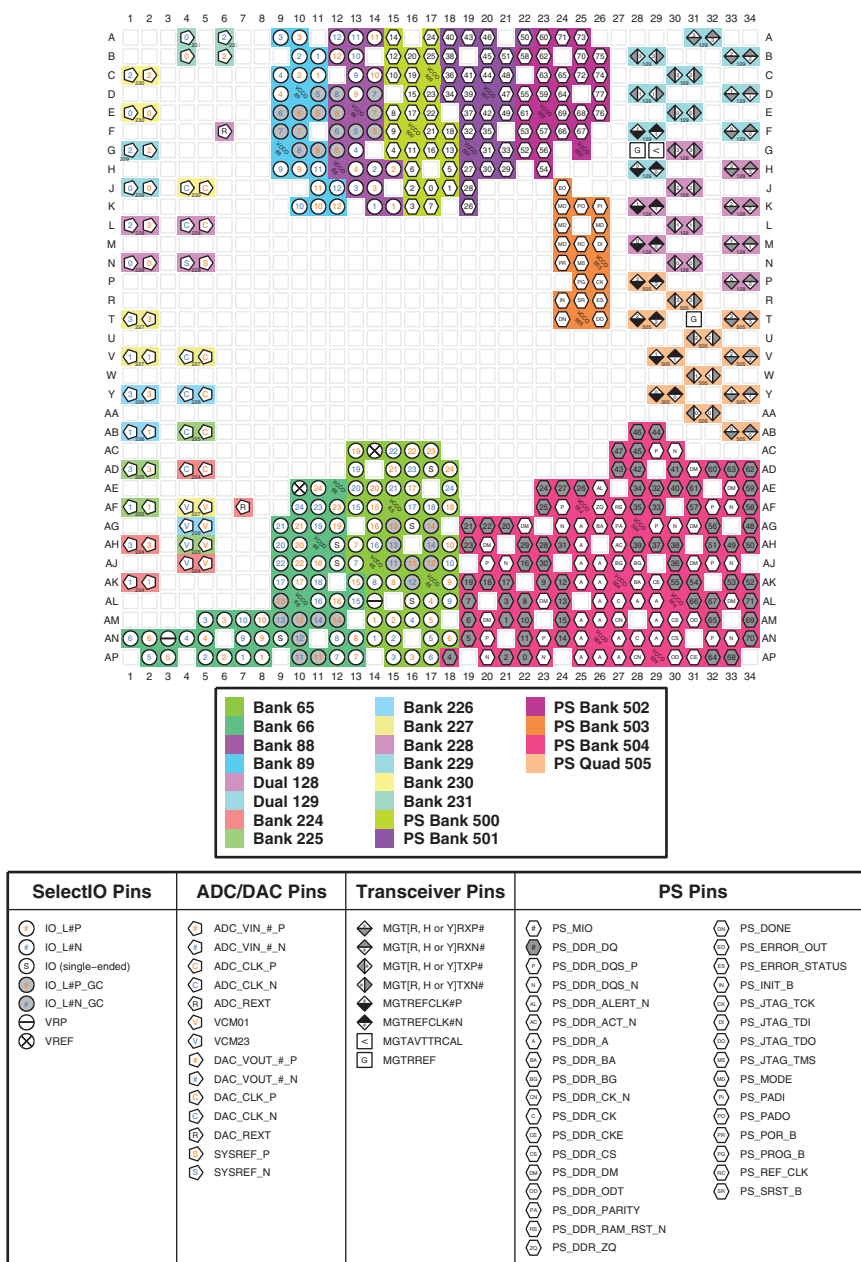


Figure 4-59: FFVE1156 and FSVE1156 Packages—XCZU48DR and XQZU48DR I/O Bank Diagram



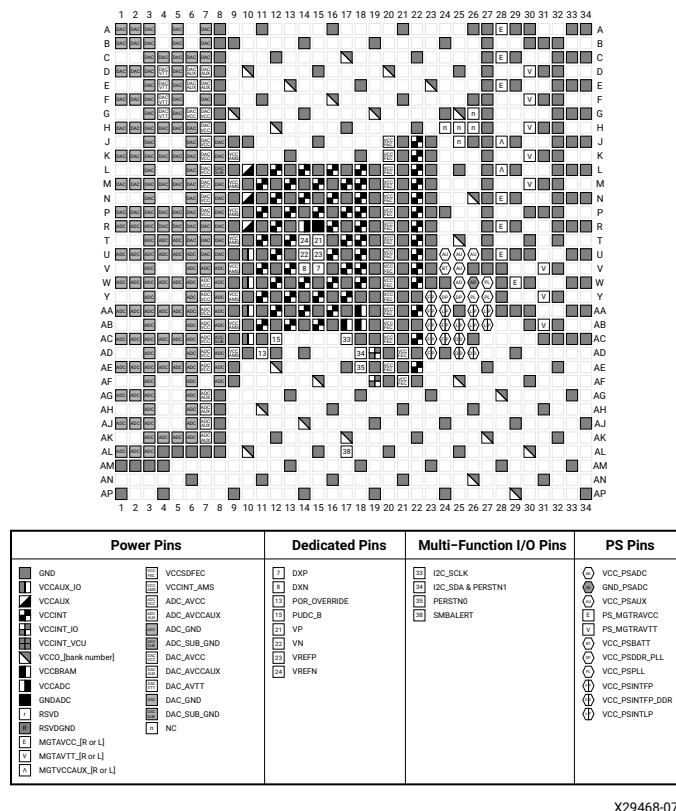


**Figure 4-60: FFVE1156 and FSVE1156 Packages—XCZU48DR and XQZU48DR Power, Dedicated, and Multi-function Pin Diagram**

**Note:** VCCAUX\_IO pins for the XQ versions of these devices in these packages are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# FFVE1156 and FSVE1156 Packages—XCZU63DR

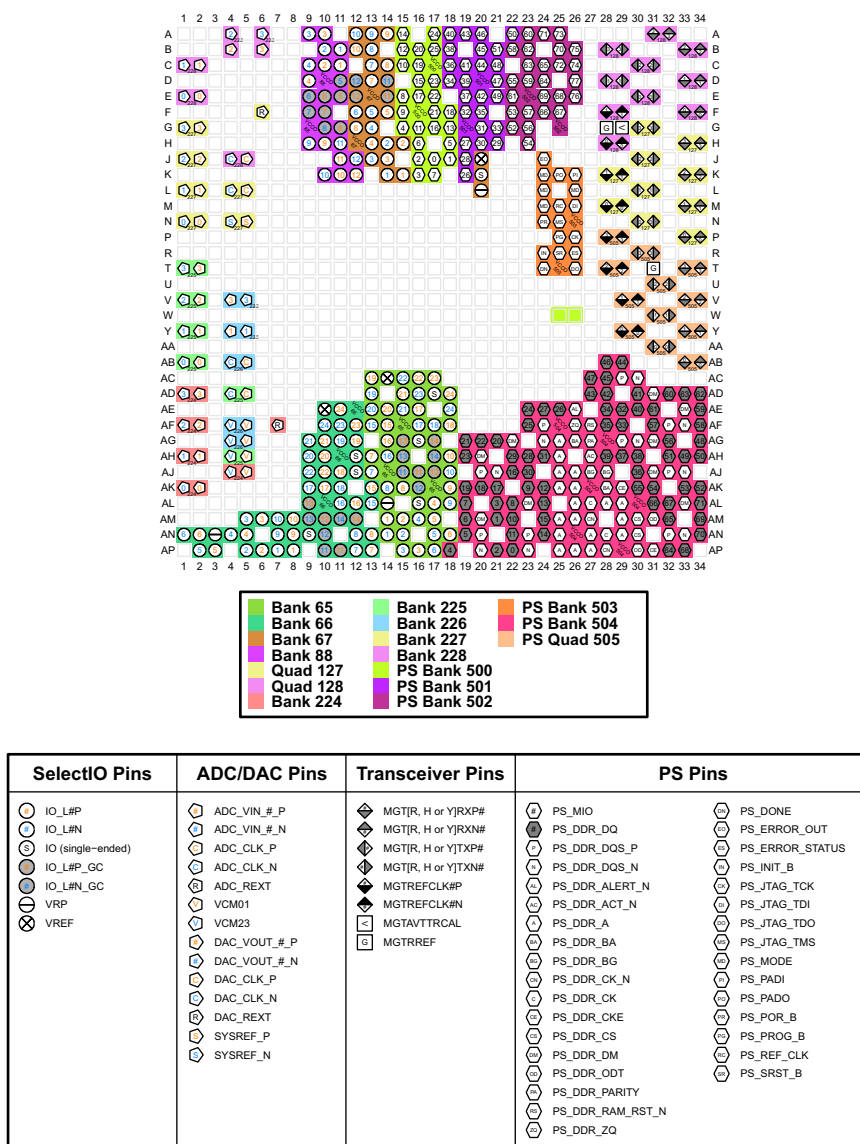


Figure 4-61: FFVE1156 and FSVE1156 Packages—XCZU63DR I/O Bank Diagram

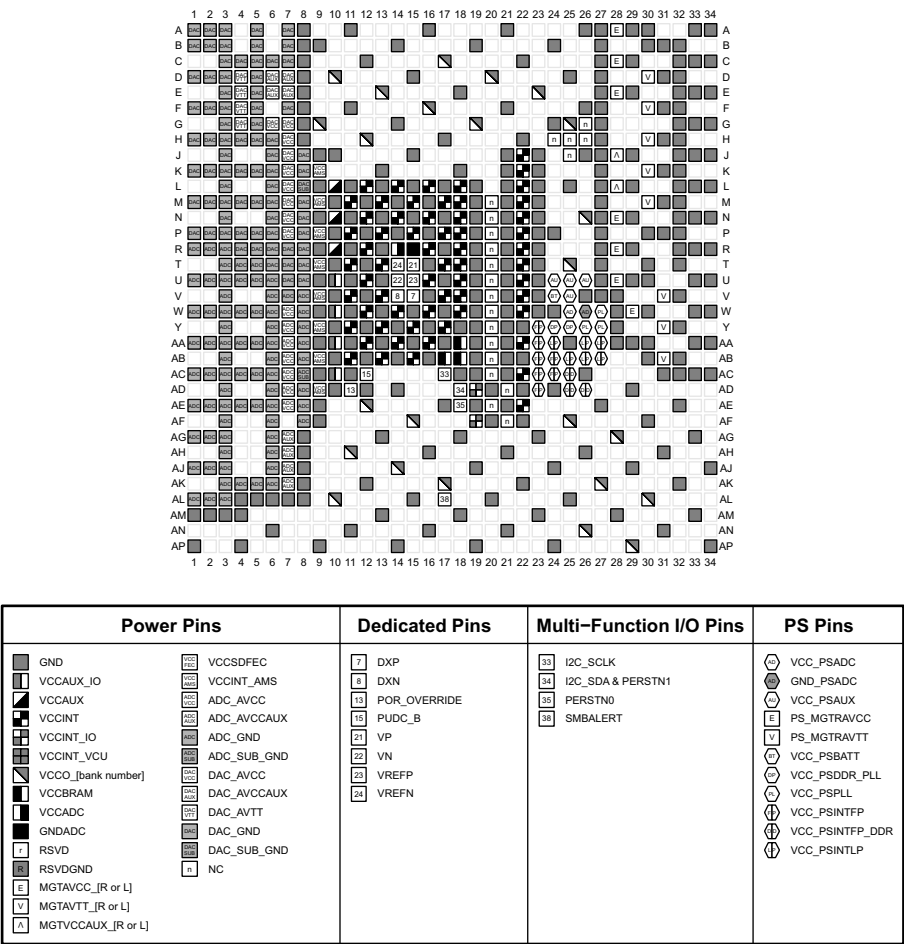


Figure 4-62: FFVE1156 and FSVE1156 Packages—XCZU63DR Power, Dedicated, and Multi-function Pin Diagram

# FFVE1156 and FSVE1156 Packages—XCZU64DR

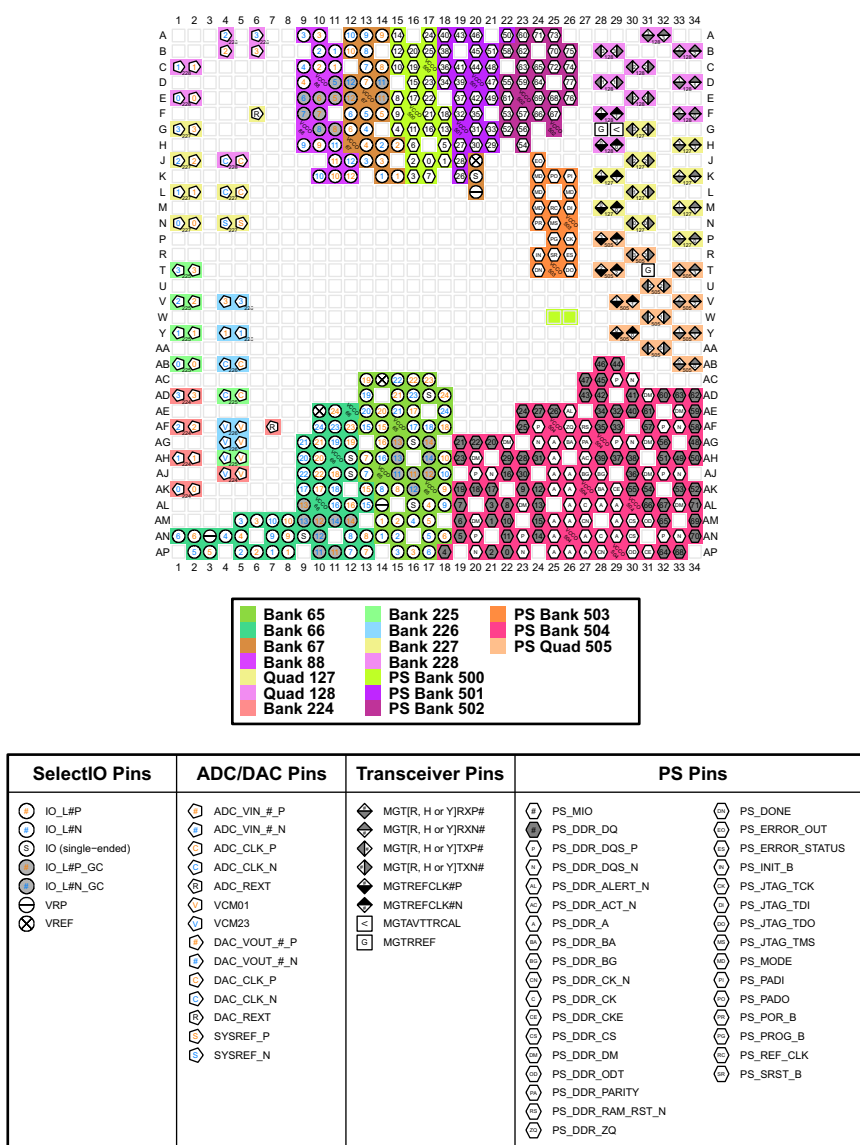


Figure 4-63: FFVE1156 and FSVE1156 Packages—XCZU64DR I/O Bank Diagram

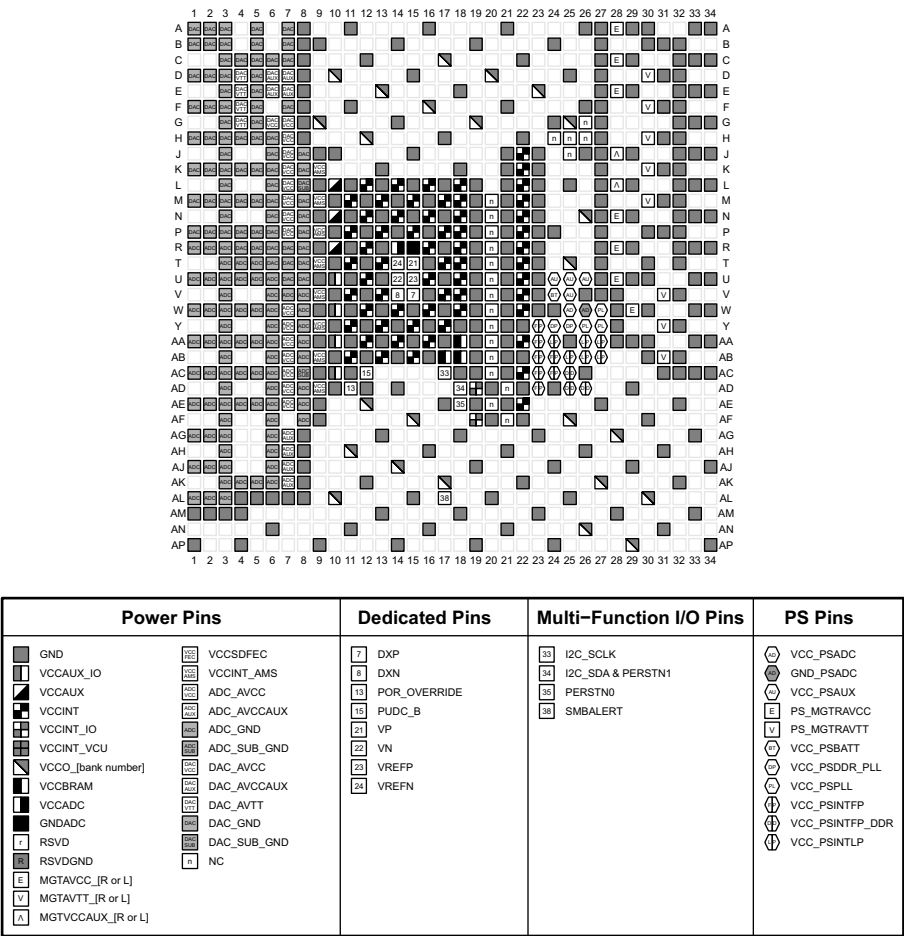


Figure 4-64: FFVE1156 and FSVE1156 Packages—XCZU64DR Power, Dedicated, and Multi-function Pin Diagram

# FFVE1156 and FSVE1156 Packages—XCZU65DR

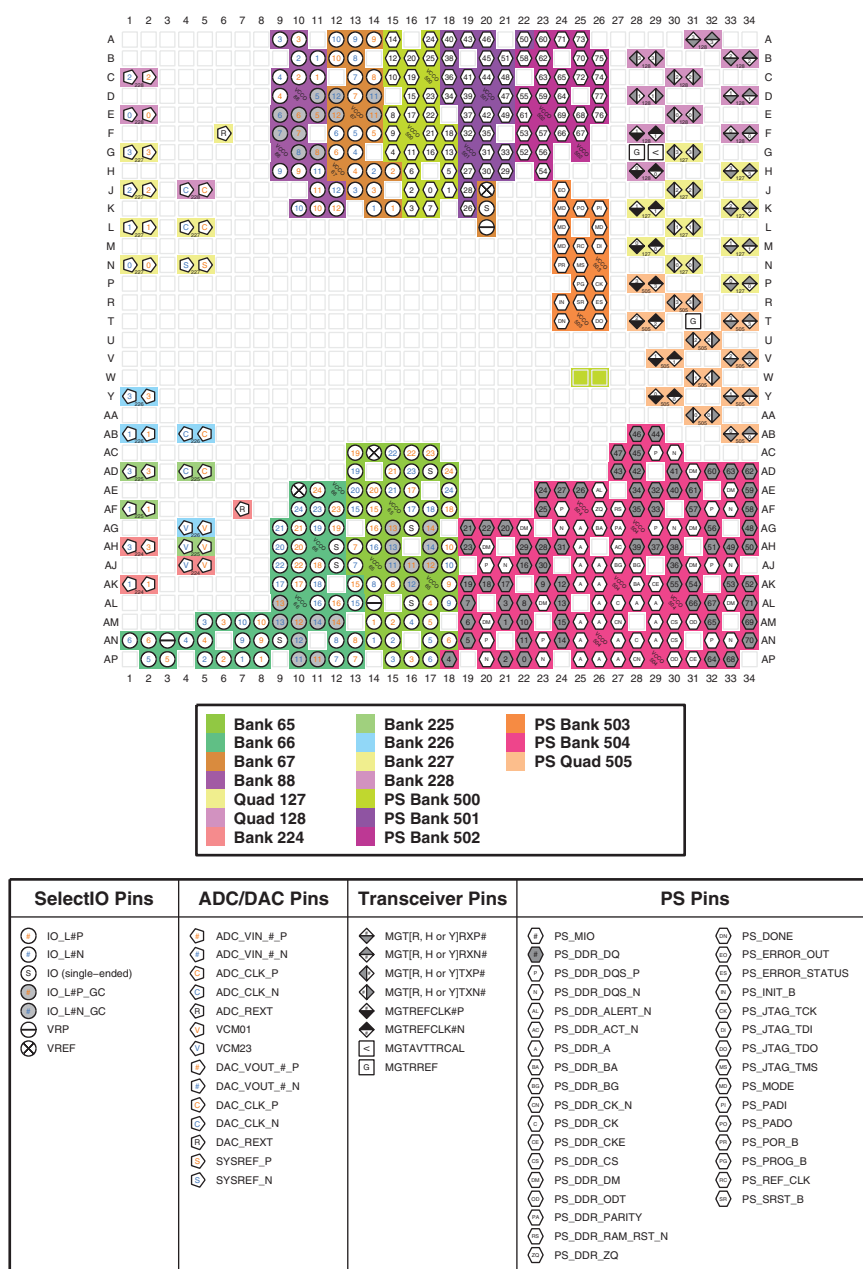


Figure 4-65: FFVE1156 and FSVE1156 Packages—XCZU65DR I/O Bank Diagram

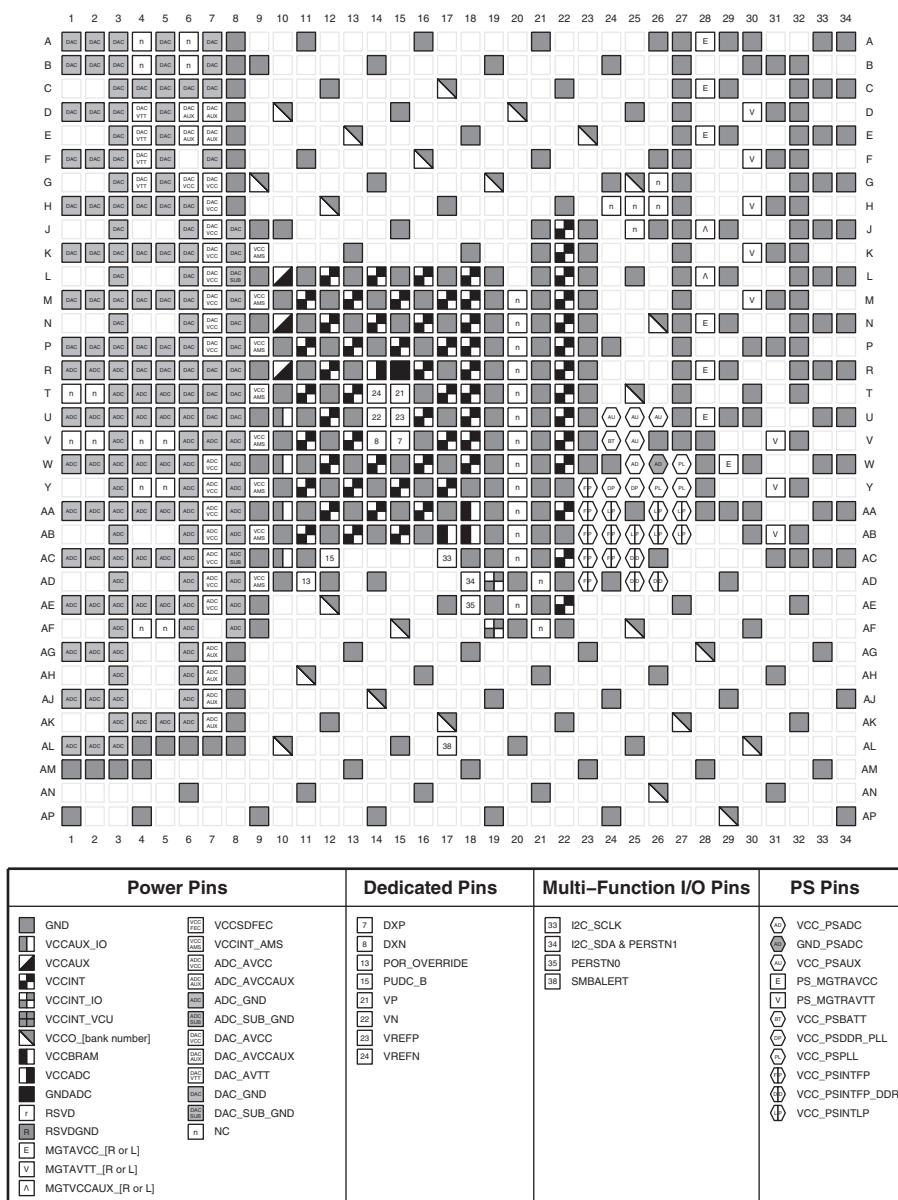


Figure 4-66: FFVE1156 and FSVE1156 Packages—XCZU65DR Power, Dedicated, and Multi-function Pin Diagram

# FFVE1156 and FSVE1156 Packages—XCZU67DR

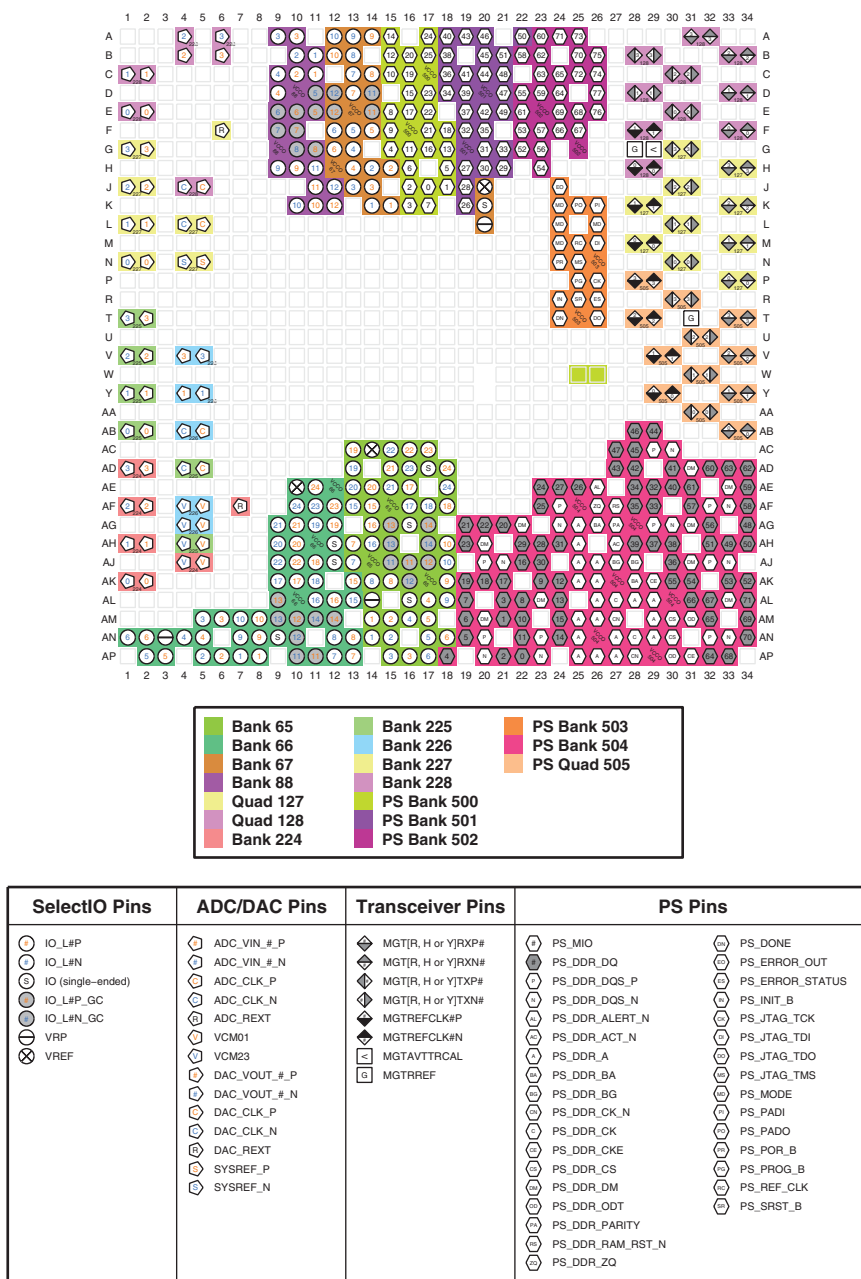


Figure 4-67: FFVE1156 and FSVE1156 Packages—XCZU67DR I/O Bank Diagram



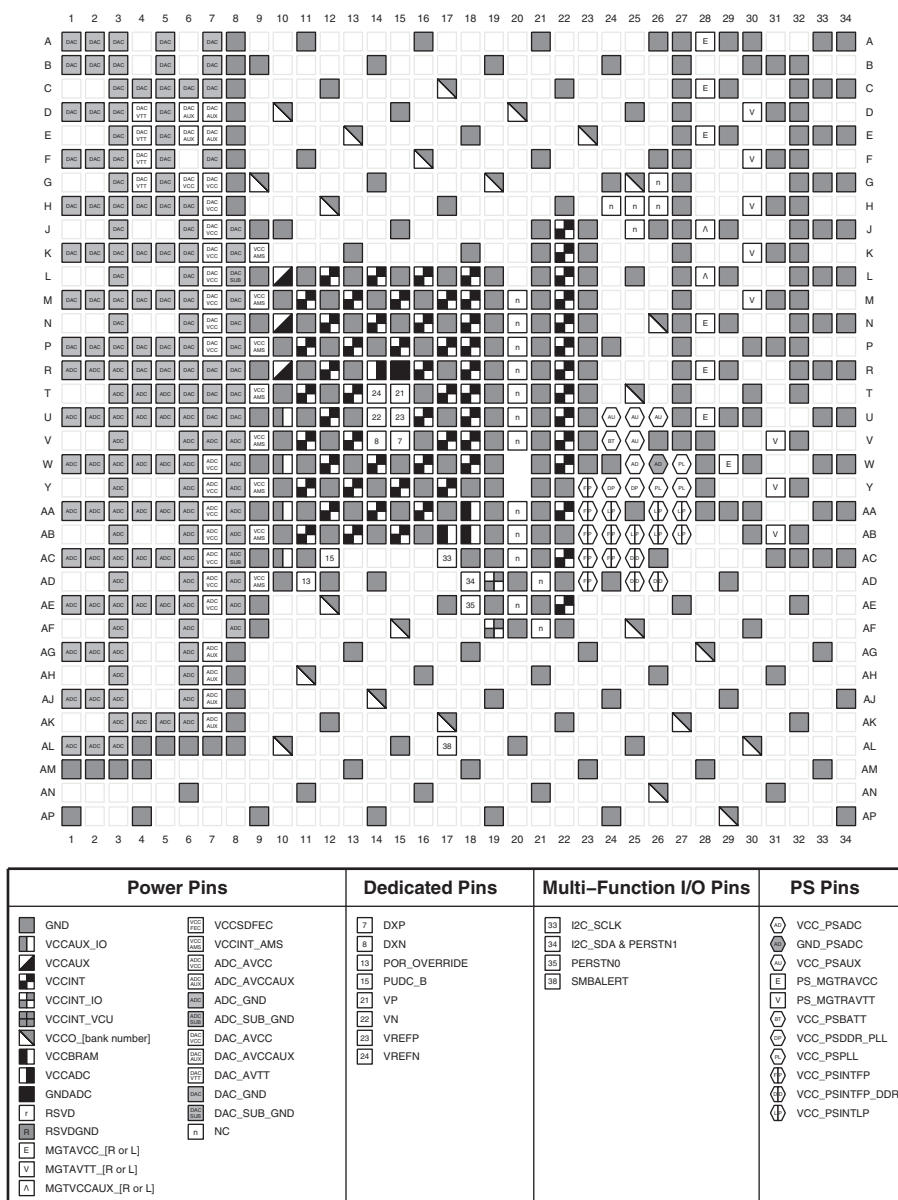


Figure 4-68: FFVE1156 and FSVE1156 Packages—XCZU67DR Power, Dedicated, and Multi-function Pin Diagram

# FFVB1517 Package—XCZU11EG

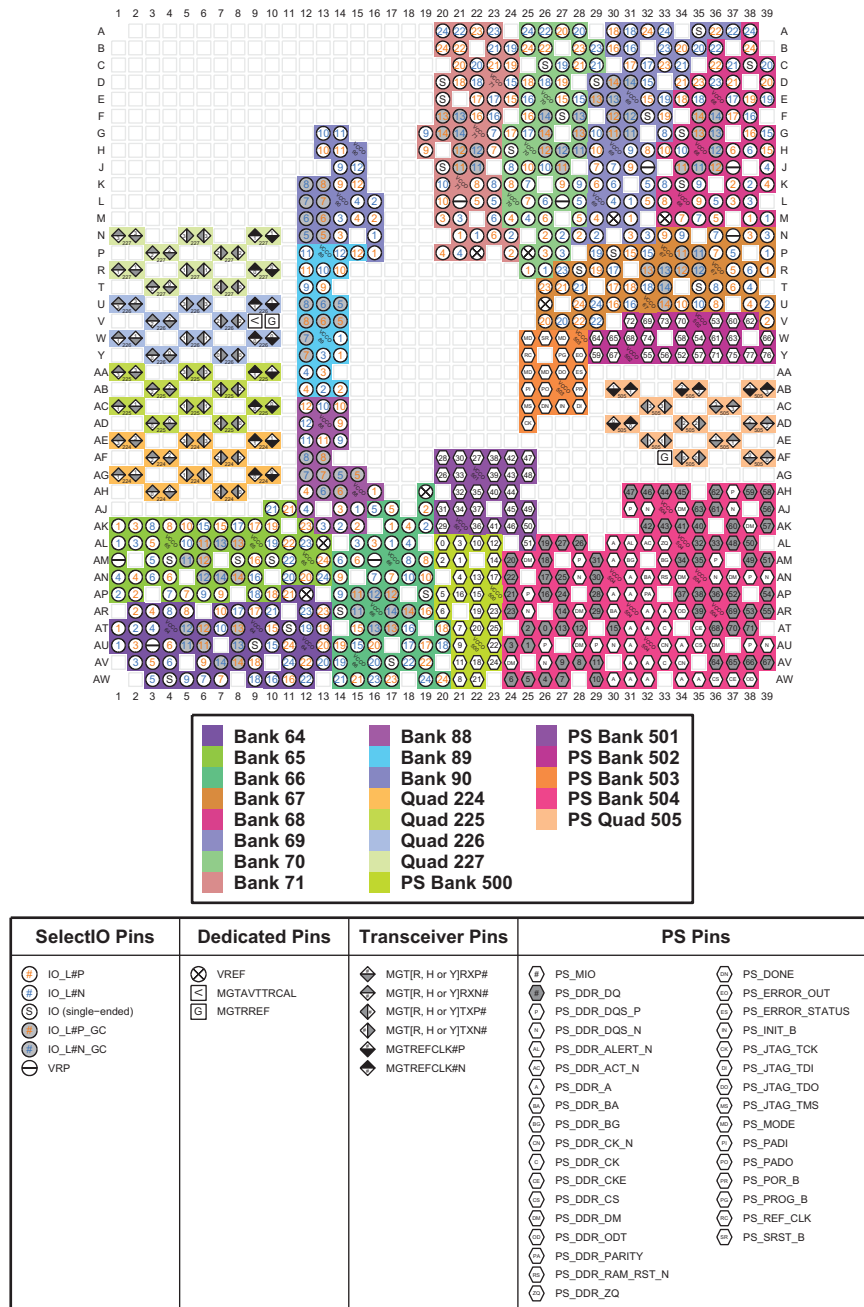


**Figure 4-69: FFVB1517 Package—XCZU11EG I/O Bank Diagram**

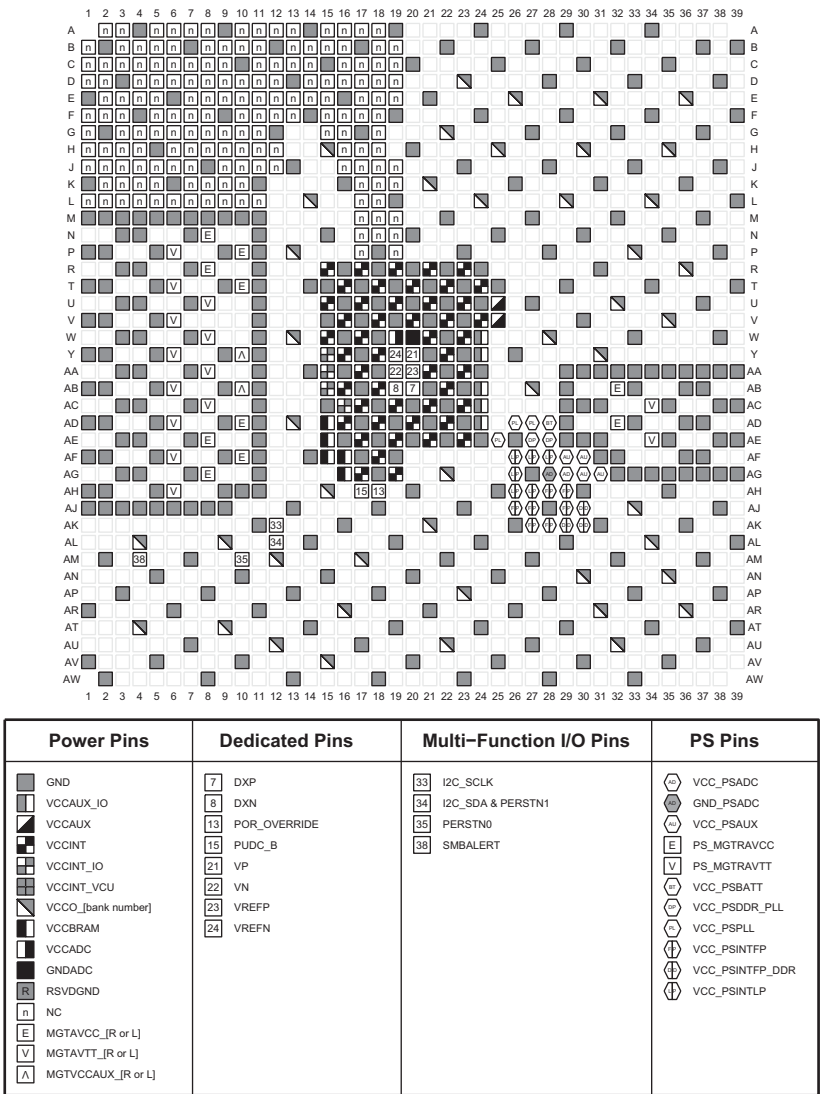


Figure 4-70: FFVB1517 Package—XCZU11EG  
Power, Dedicated, and Multi-function Pin Diagram

# FFVB1517 Package—XCZU17EG and XCZU19EG

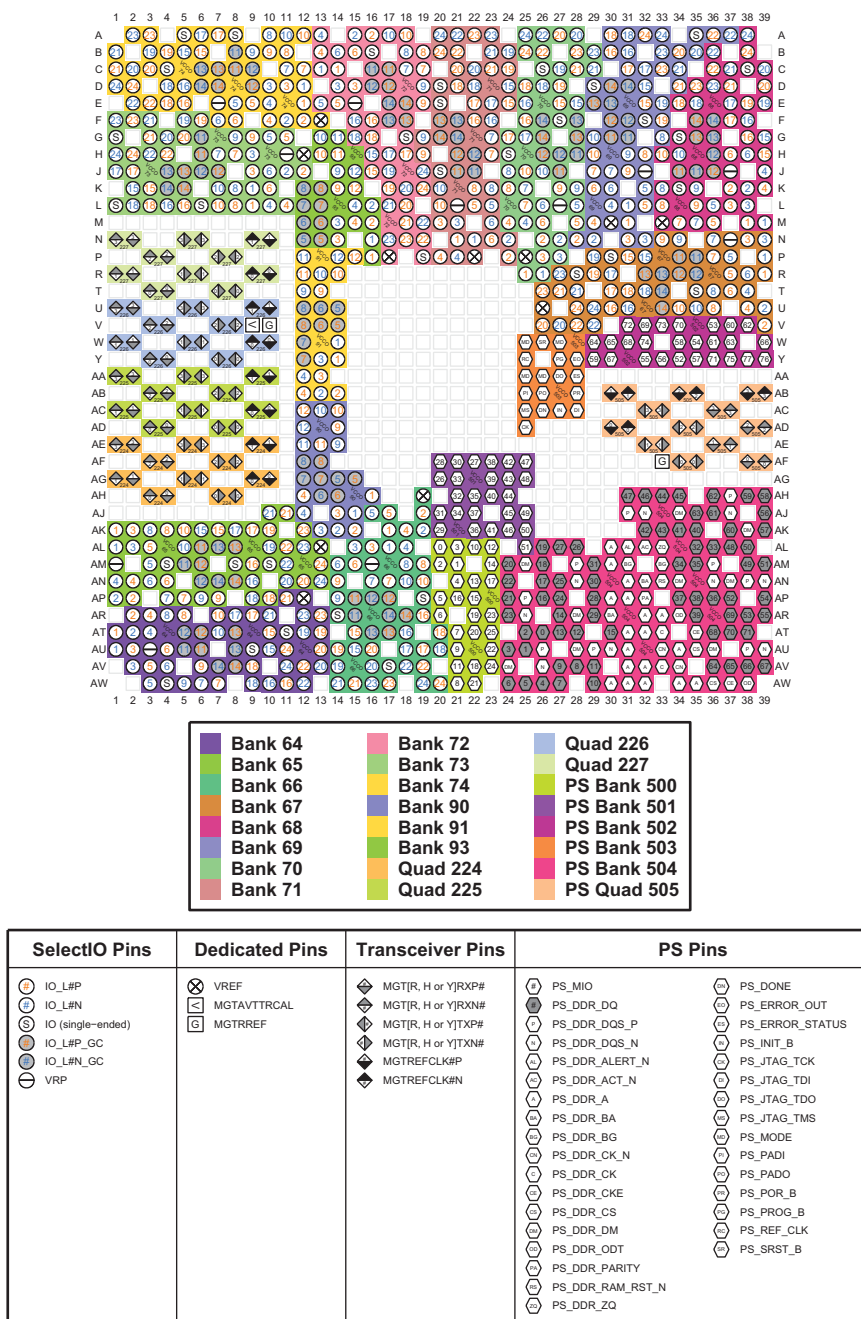


Figure 4-71: FFVB1517 Package—XCZU17EG and XCZU19EG I/O Bank Diagram

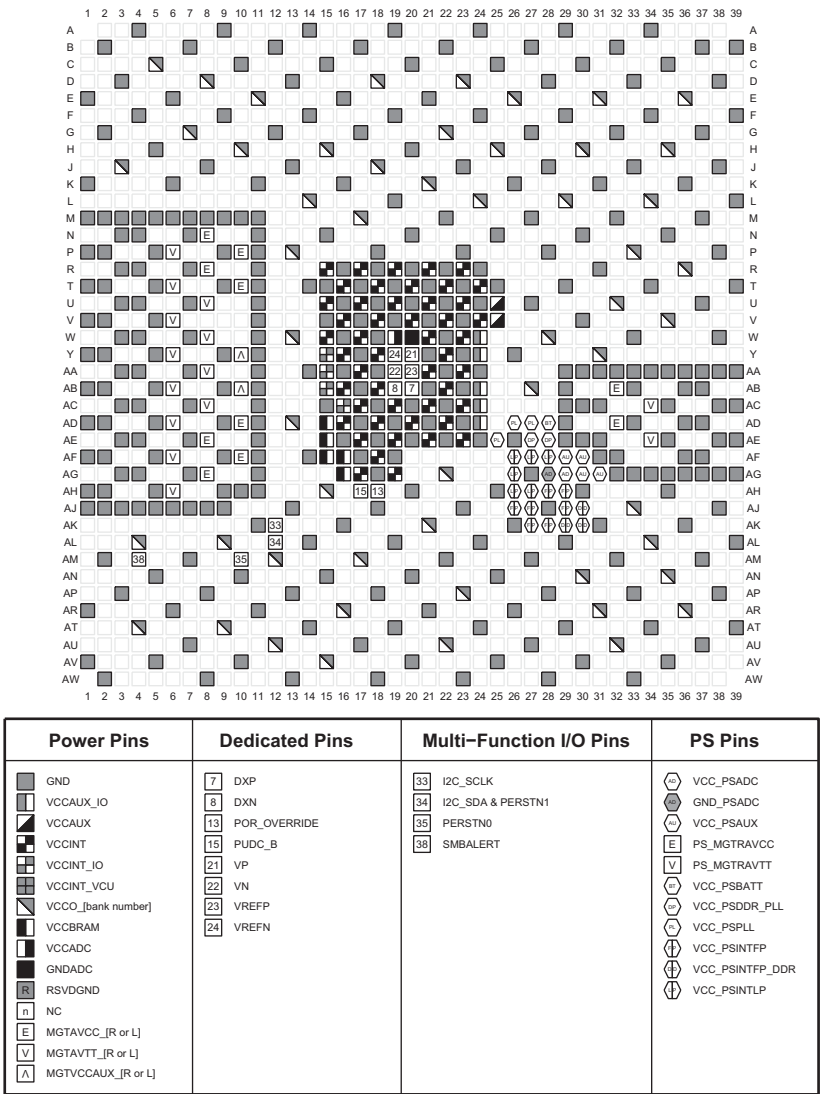


Figure 4-72: FFVB1517 Package—XCZU17EG and XCZU19EG Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of these devices in this package are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# FFVF1517 Package—XCZU7CG and XCZU7EG

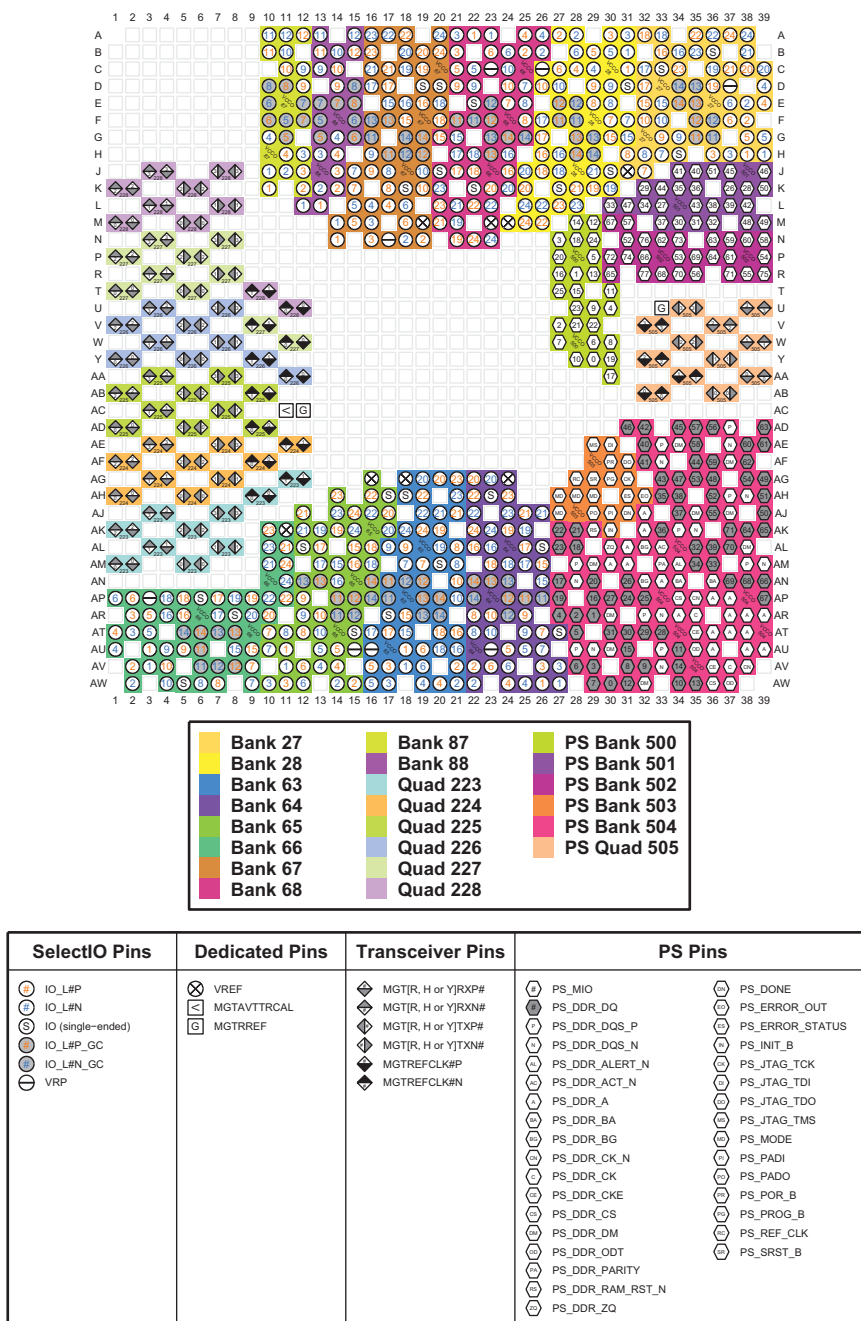


Figure 4-73: FFVF1517 Package—XCZU7CG and XCZU7EG I/O Bank Diagram

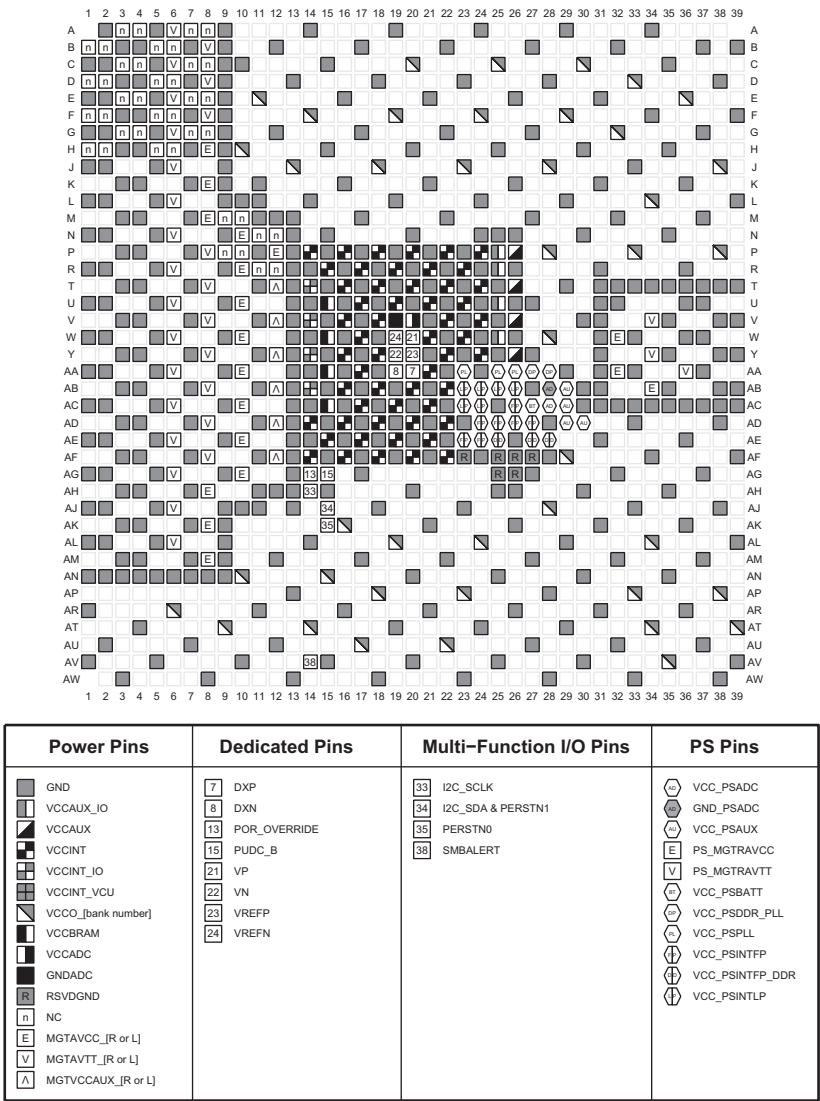


Figure 4-74: FFVF1517 Package—XCZU7CG and XCZU7EG Power, Dedicated, and Multi-function Pin Diagram



# FFVF1517 Package—XCZU7EV

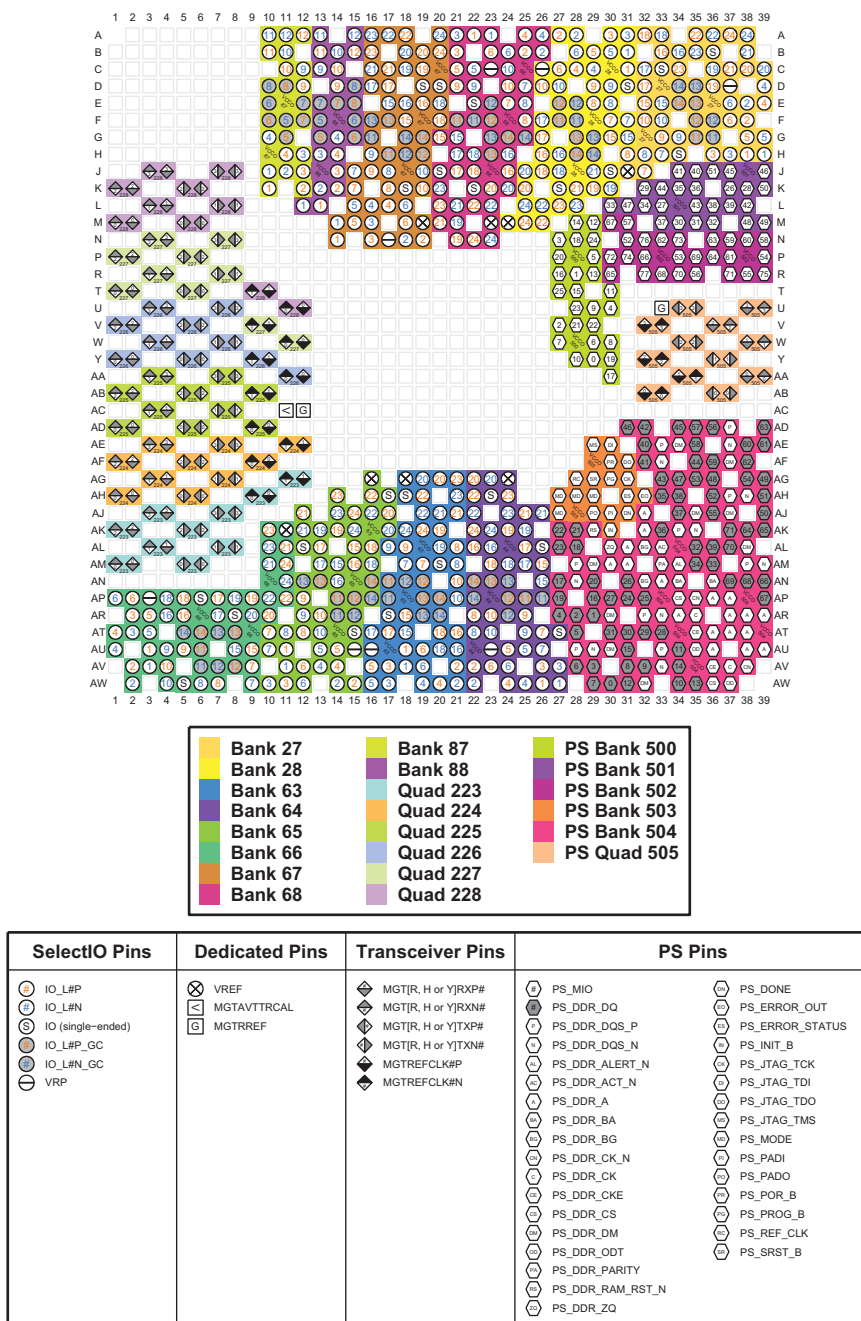


Figure 4-75: FFVF1517 Package—XCZU7EV I/O Bank Diagram



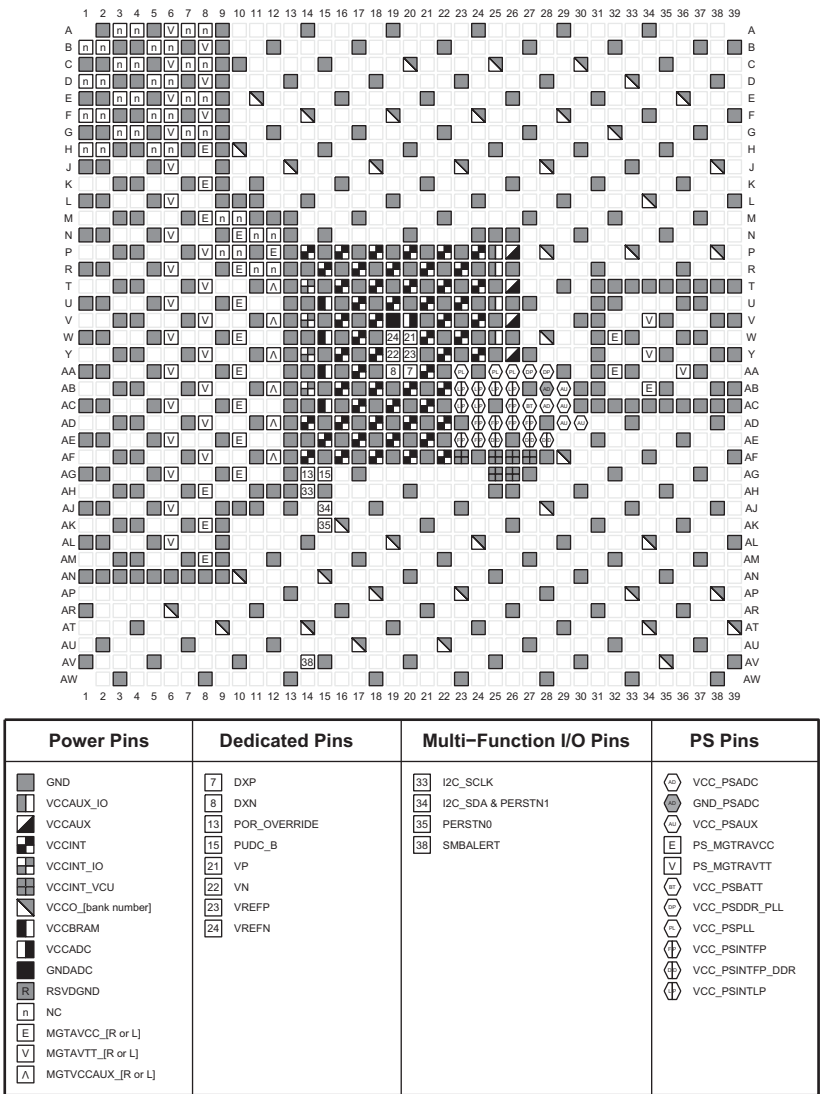


Figure 4-76: FFVF1517 Package—XCZU7EV Power, Dedicated, and Multi-function Pin Diagram

# FFVF1517 Package—XCZU11EG

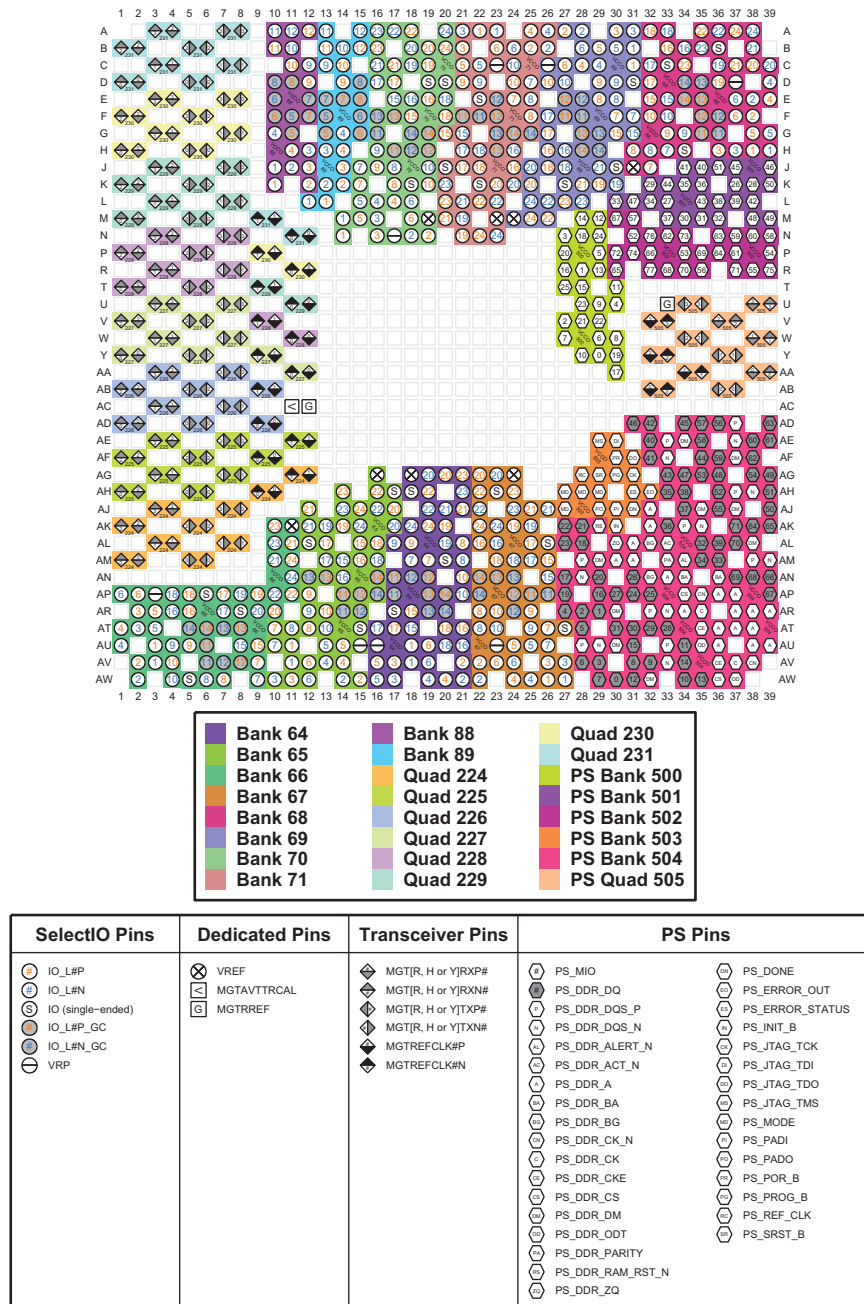


Figure 4-77: FFVF1517 Package—XCZU11EG I/O Bank Diagram

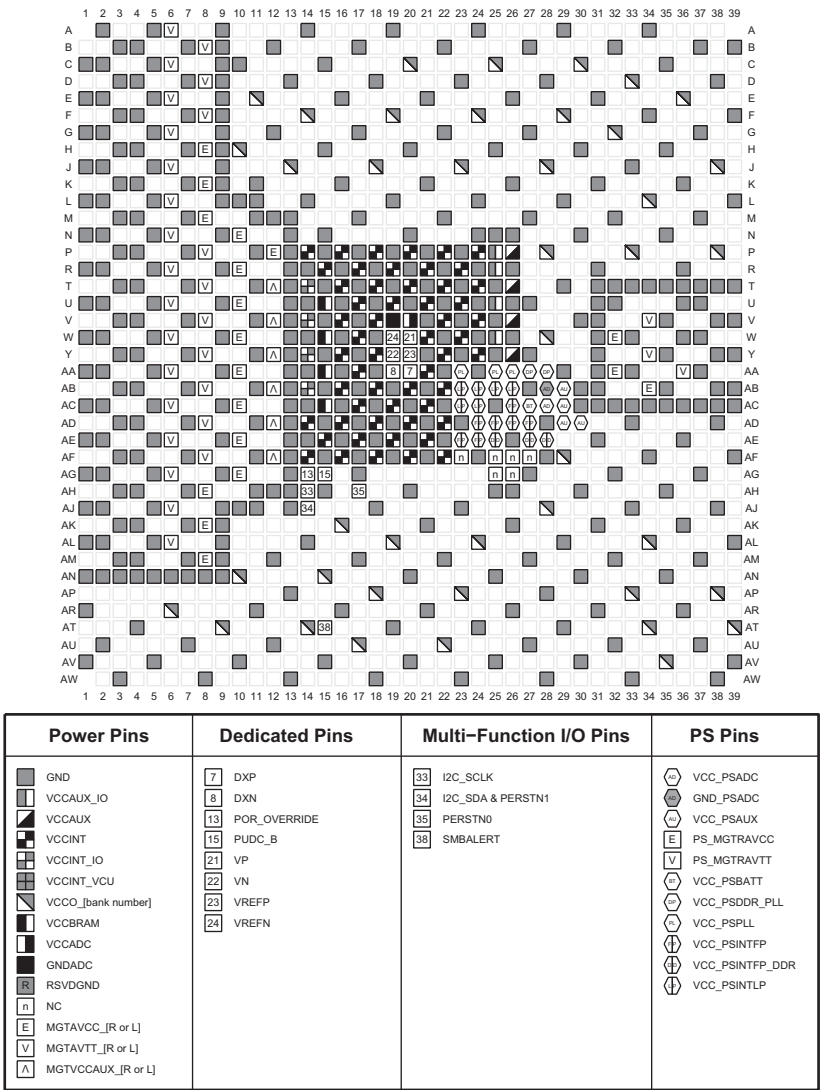


Figure 4-78: FFVF1517 Package—XCZU11EG Power, Dedicated, and Multi-function Pin Diagram

# FFVG1517 and FSVG1517 Packages—XCZU25DR

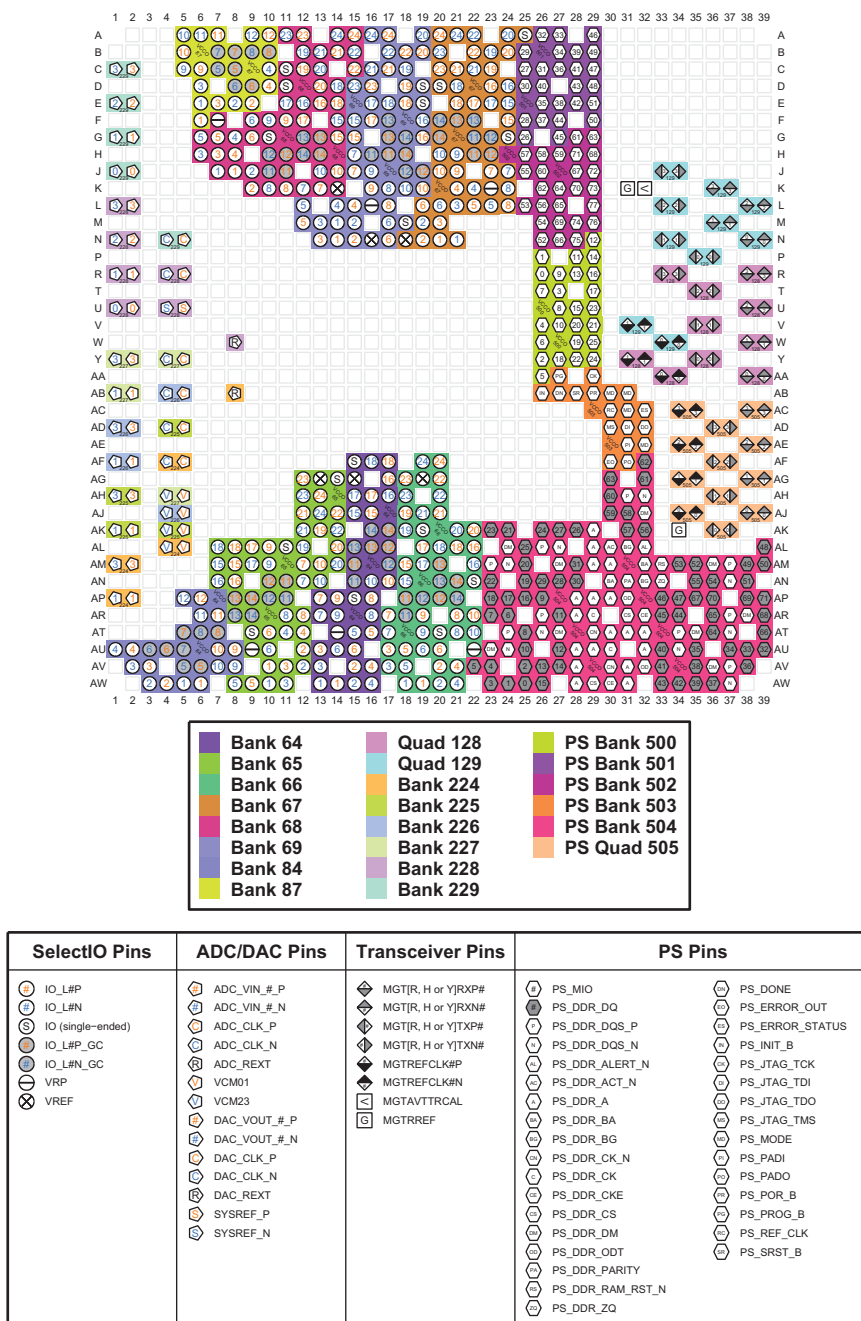


Figure 4-79: FFVG1517 and FSVG1517 Packages—XCZU25DR I/O Bank Diagram

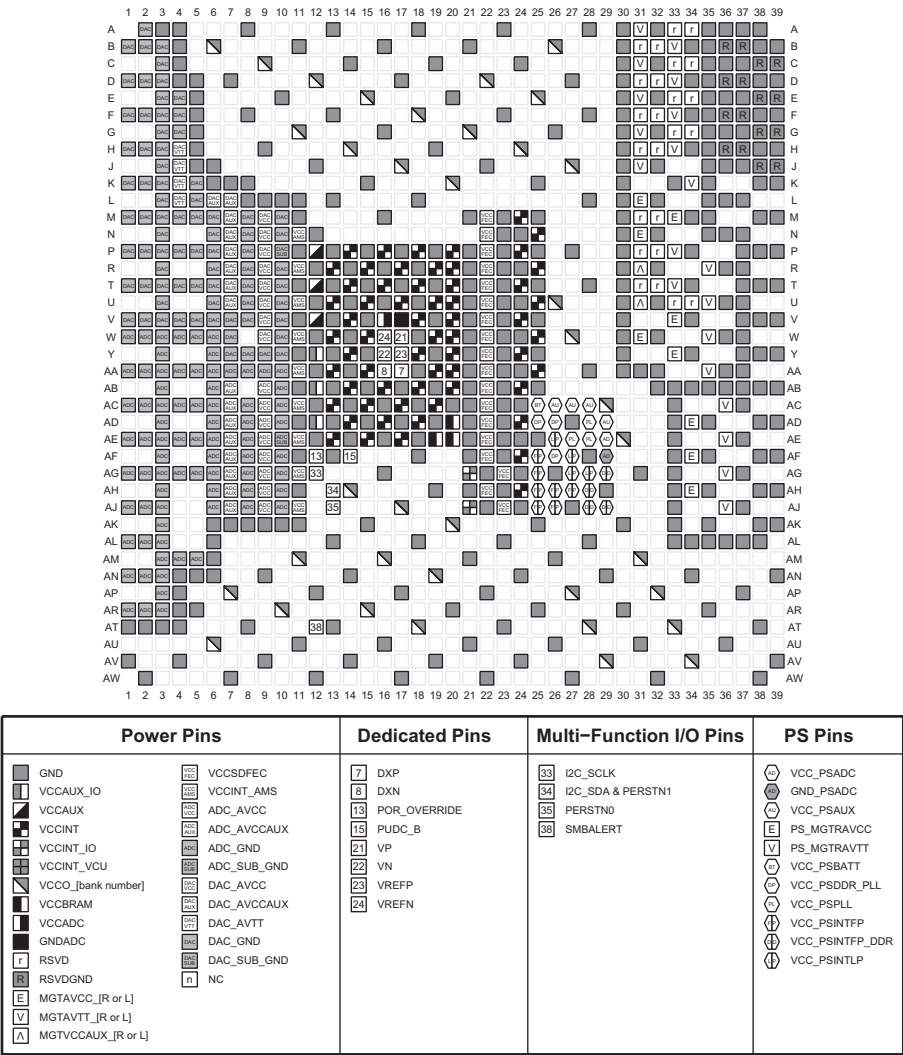


Figure 4-80: FFVG1517 and FSVG1517 Packages—XCZU25DR Power, Dedicated, and Multi-function Pin Diagram

# FFVG1517 and FSVG1517 Packages—XCZU27DR and XCZU28DR

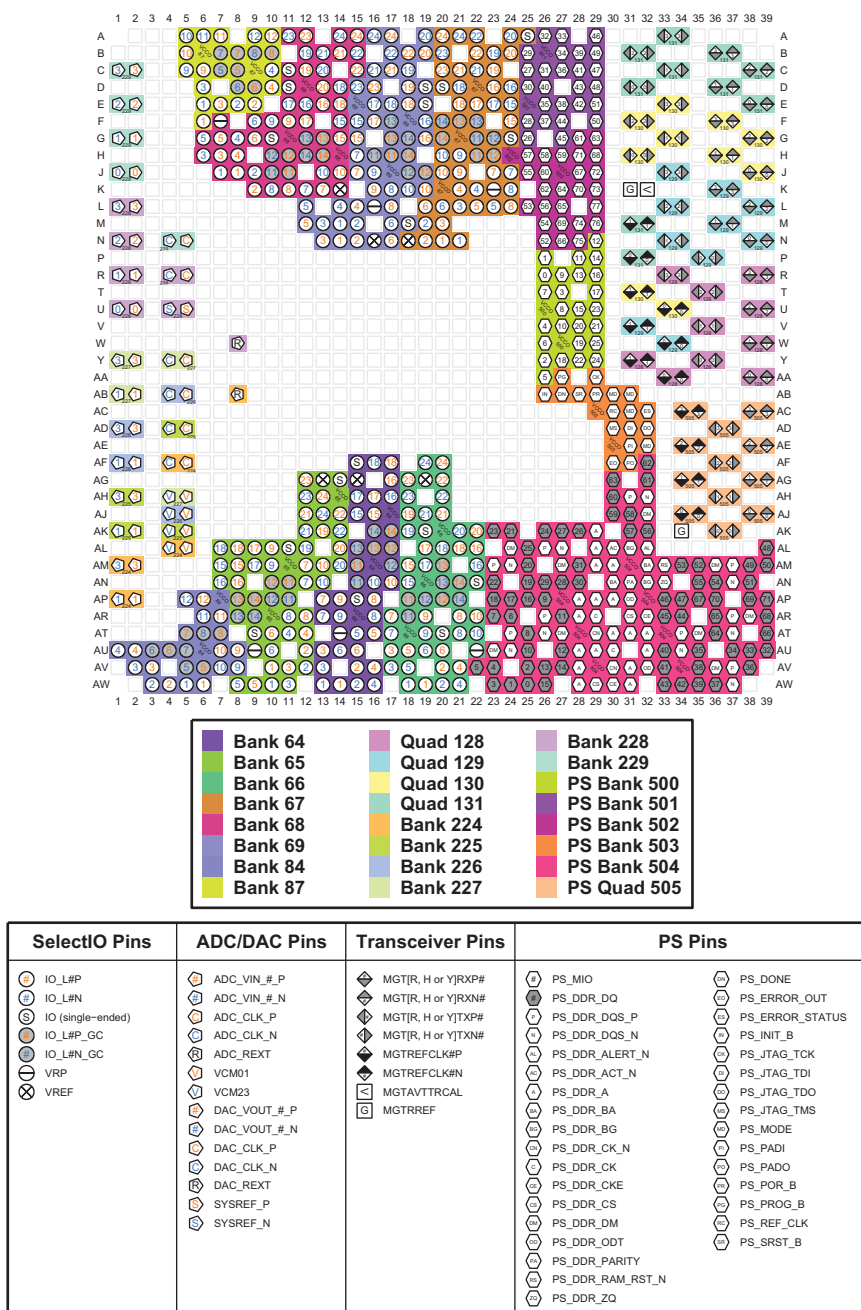


Figure 4-81: FFVG1517 and FSVG1517 Packages—XCZU27DR and XCZU28DR I/O Bank Diagram

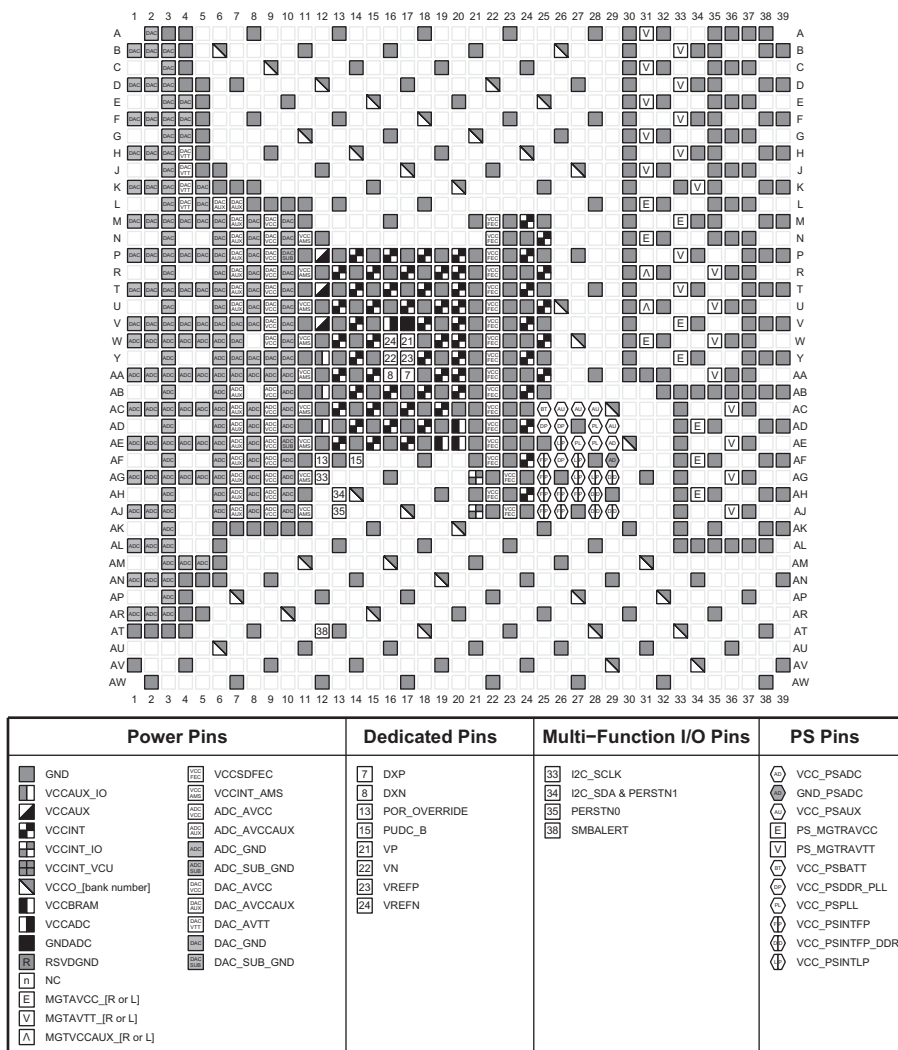


Figure 4-82: FFGV1517 and FSVG1517 Packages—XCZU27DR and XCZU28DR Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of these devices in these packages are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.



# FFVG1517 and FSVG1517 Packages—XCZU43DR

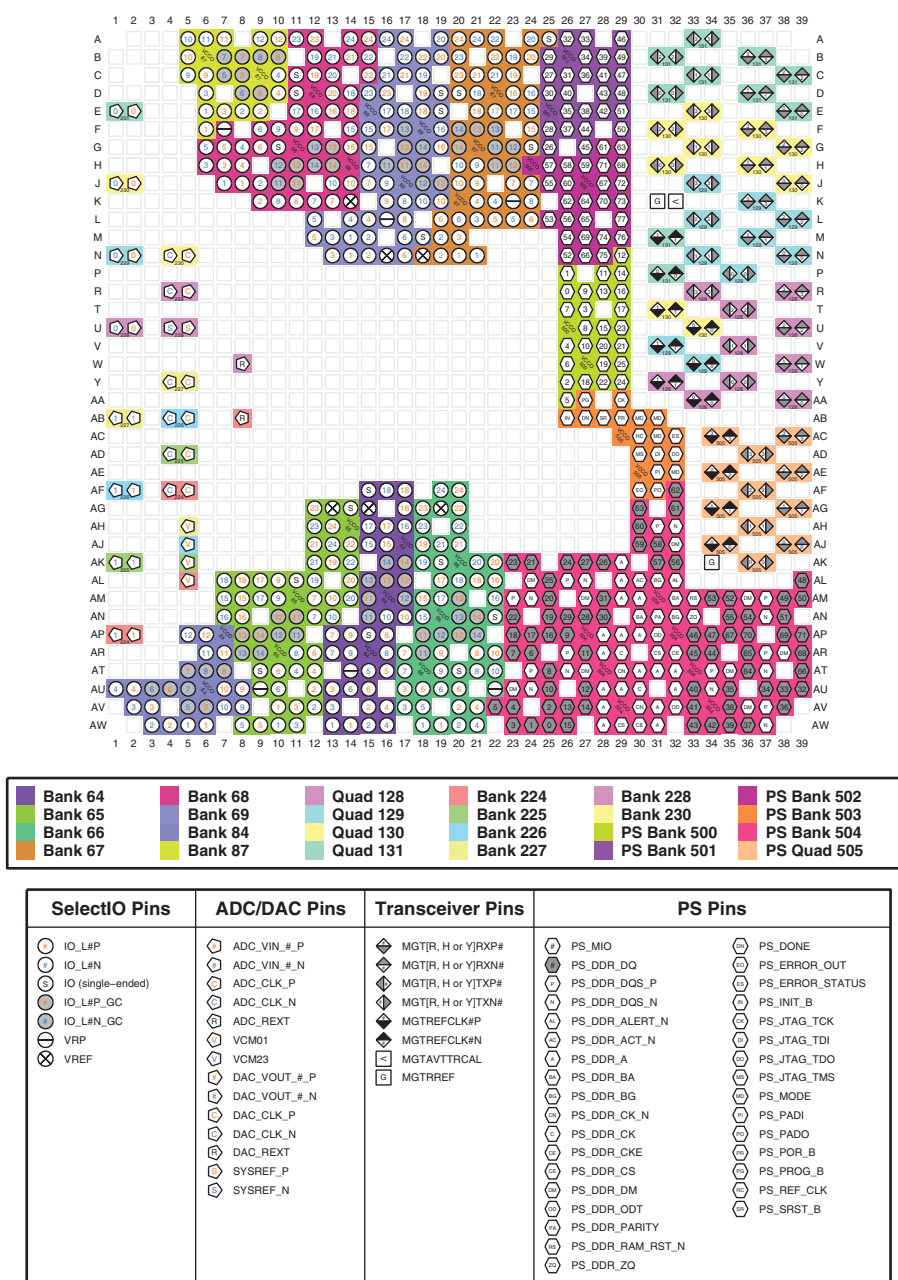


Figure 4-83: FFVG1517 and FSVG1517 Packages—XCZU43DR I/O Bank Diagram



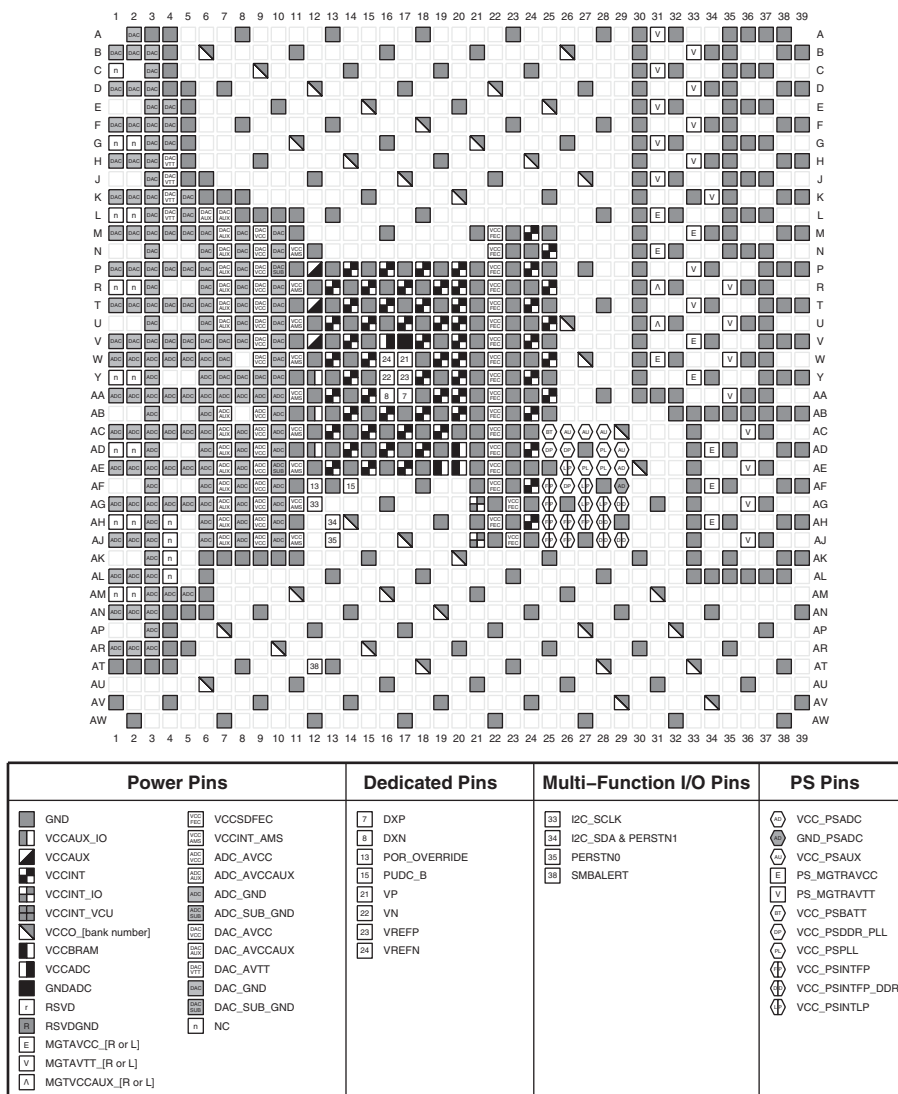


Figure 4-84: FFVG1517 and FSVG1517 Packages—XCZU43DR Power, Dedicated, and Multi-function Pin Diagram

# FFVG1517 and FSVG1517 Packages—XCZU47DR

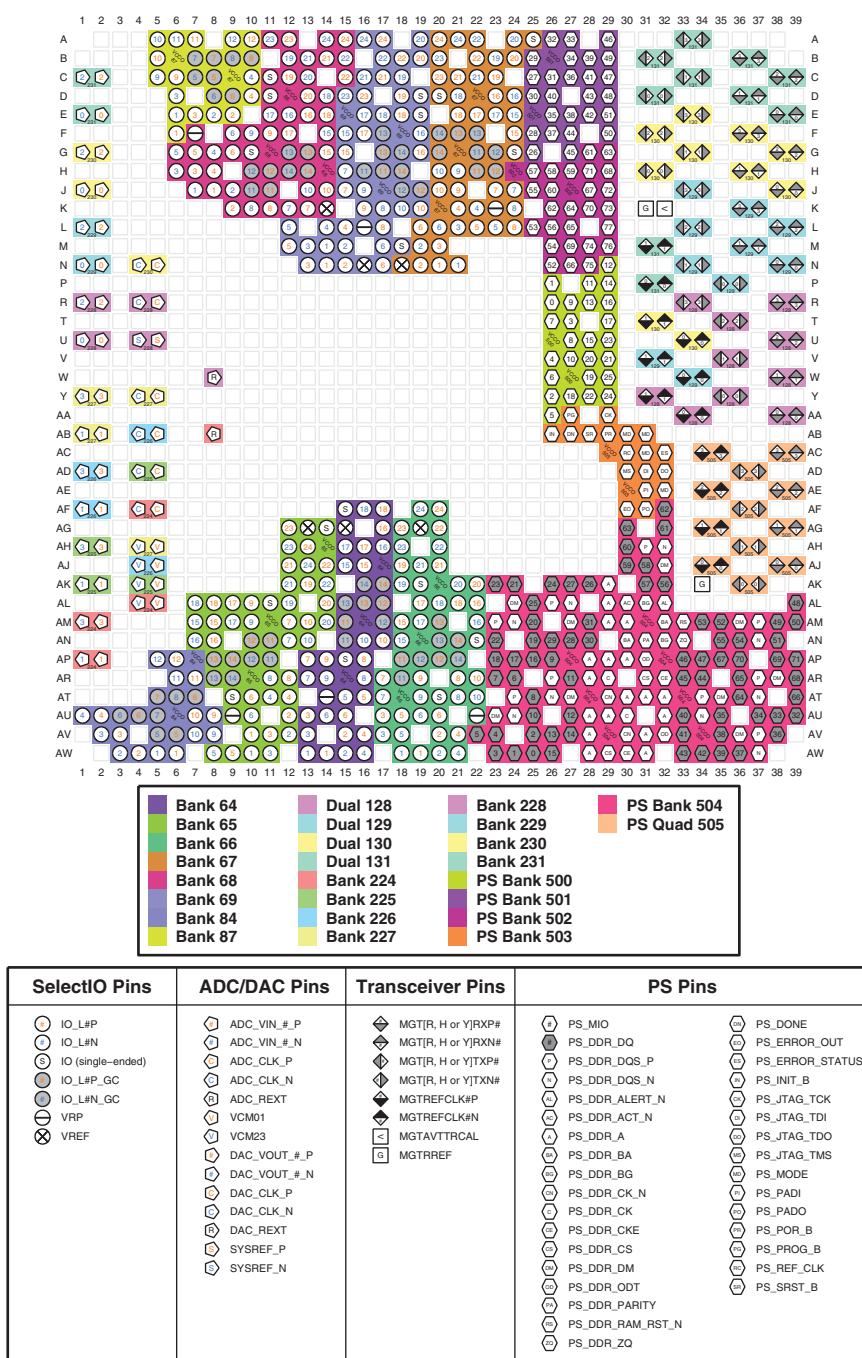
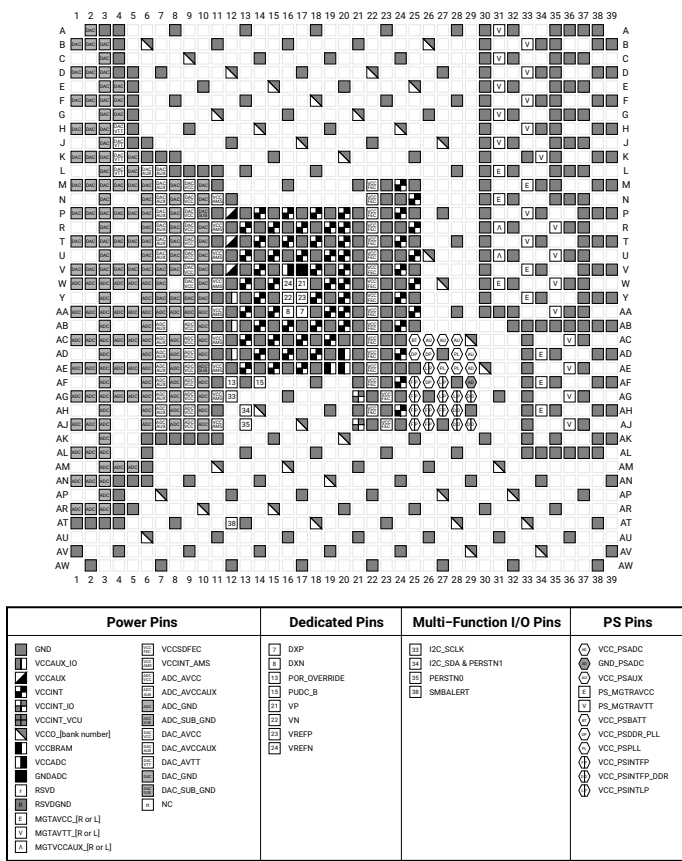


Figure 4-85: FFVG1517 and FSVG1517 Packages—XCZU47DR I/O Bank Diagram



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Figure 4-86: FFVG1517 and FSVG1517 Packages—XCZU47DR Power, Dedicated, and Multi-function Pin Diagram

# FFVG1517, FSVG1517 Packages—XCZU48DR FSRG1517 Package—XQZU48DR

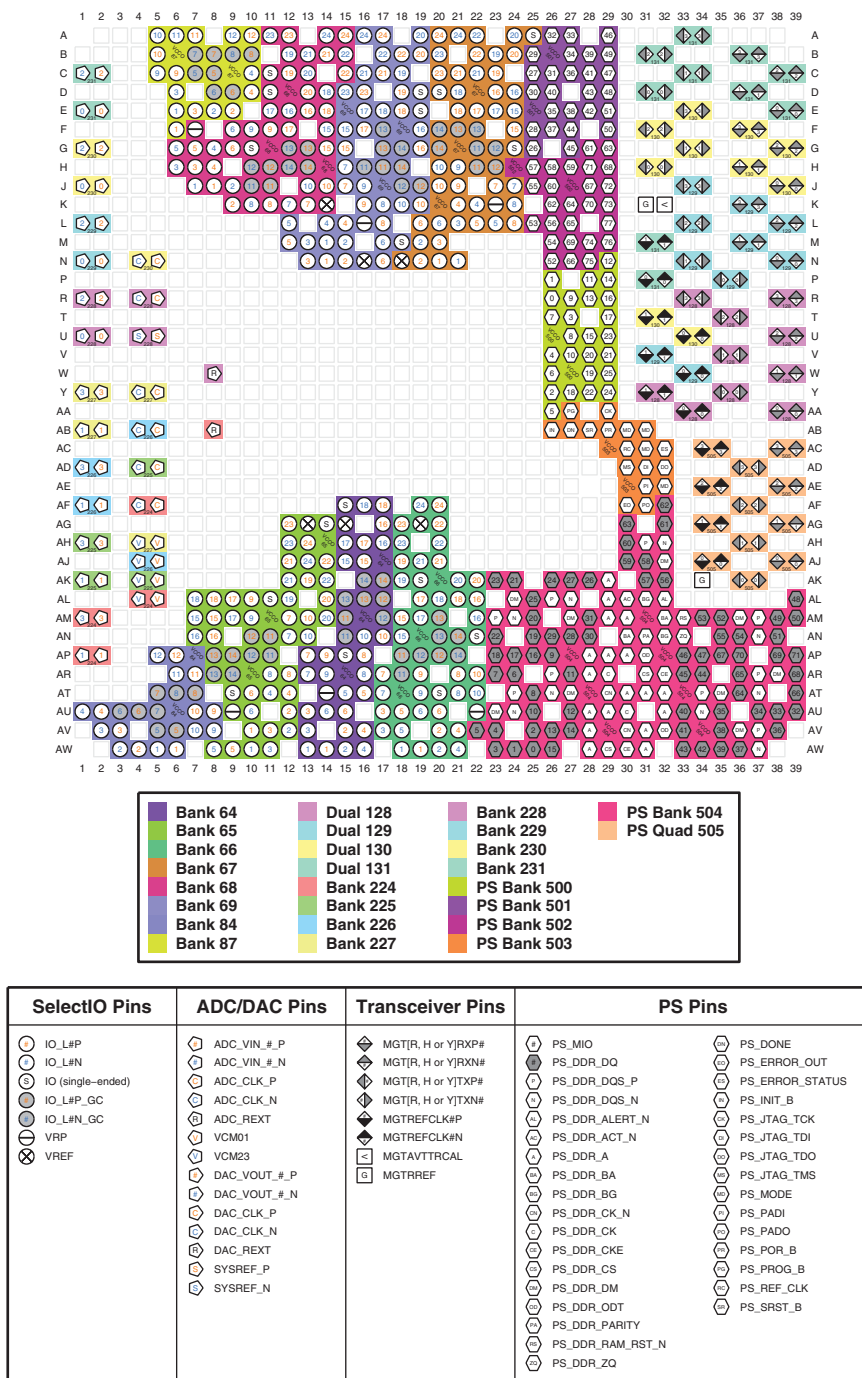


Figure 4-87: FFVG1517, FSVG1517, FSRG1517 Packages—XCZU48DR, XQZU48DR I/O Bank Diagram

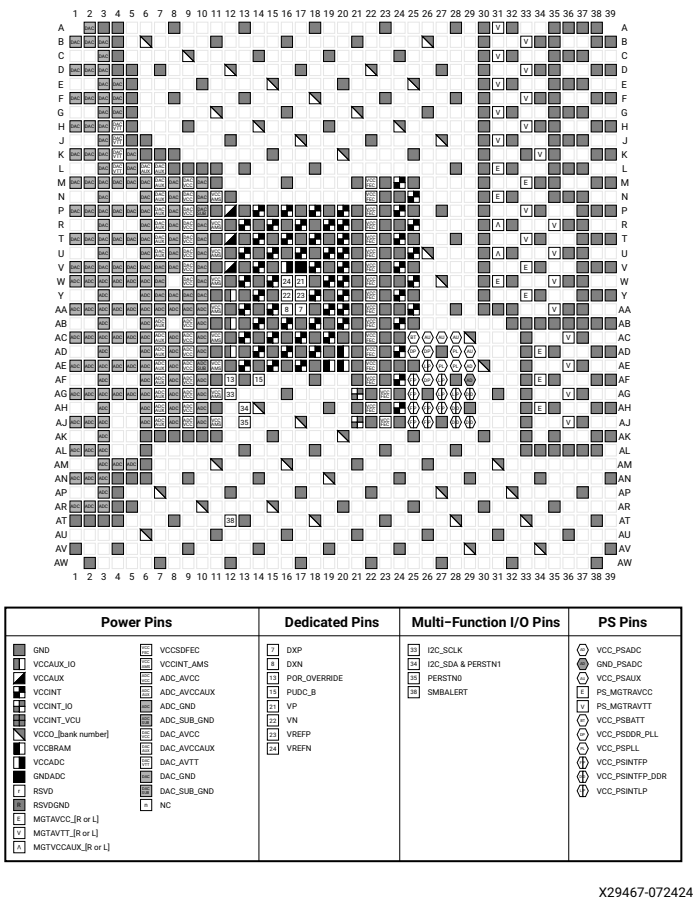


Figure 4-88: FFVG1517, FSVG1517, FSRG1517 Packages—XCZU48DR, XQZU48DR Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of these devices in these packages are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# FFVC1760 Package—XCZU11EG

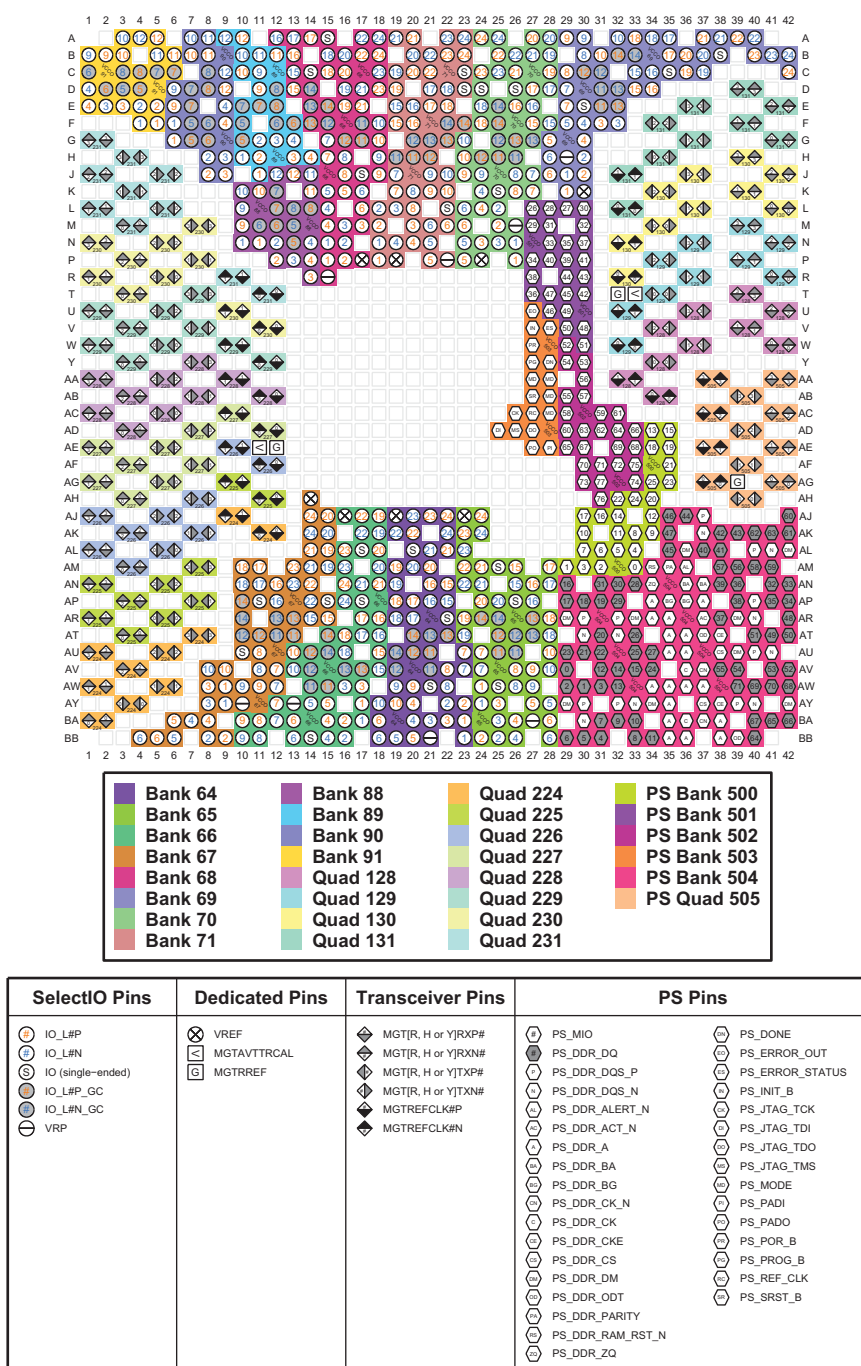


Figure 4-89: FFVC1760 Package—XCZU11EG I/O Bank Diagram

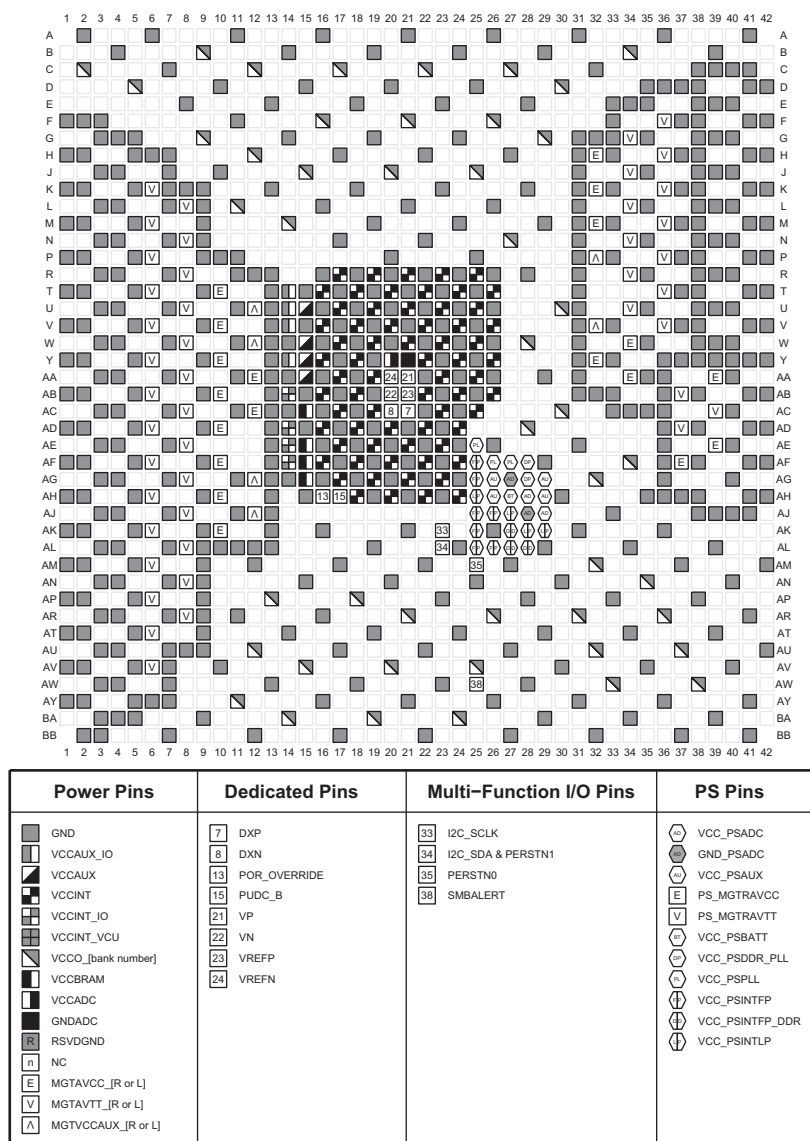


Figure 4-90: FFVC1760 Package—XCZU11EG Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of this device in this package are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.



# FFVC1760 Package—XCZU17EG and XCZU19EG

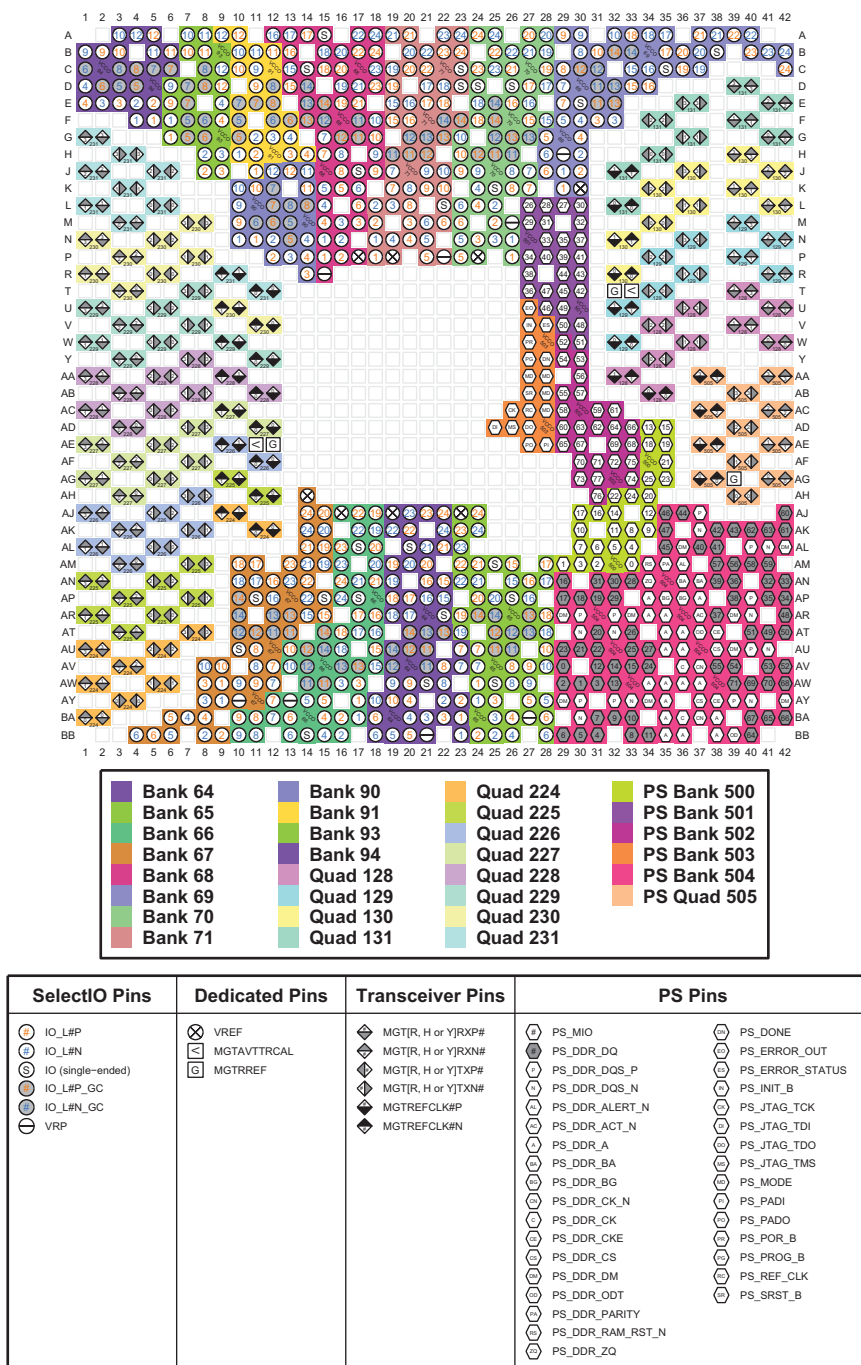


Figure 4-91: FFVC1760 Package—XCZU17EG and XCZU19EG I/O Bank Diagram



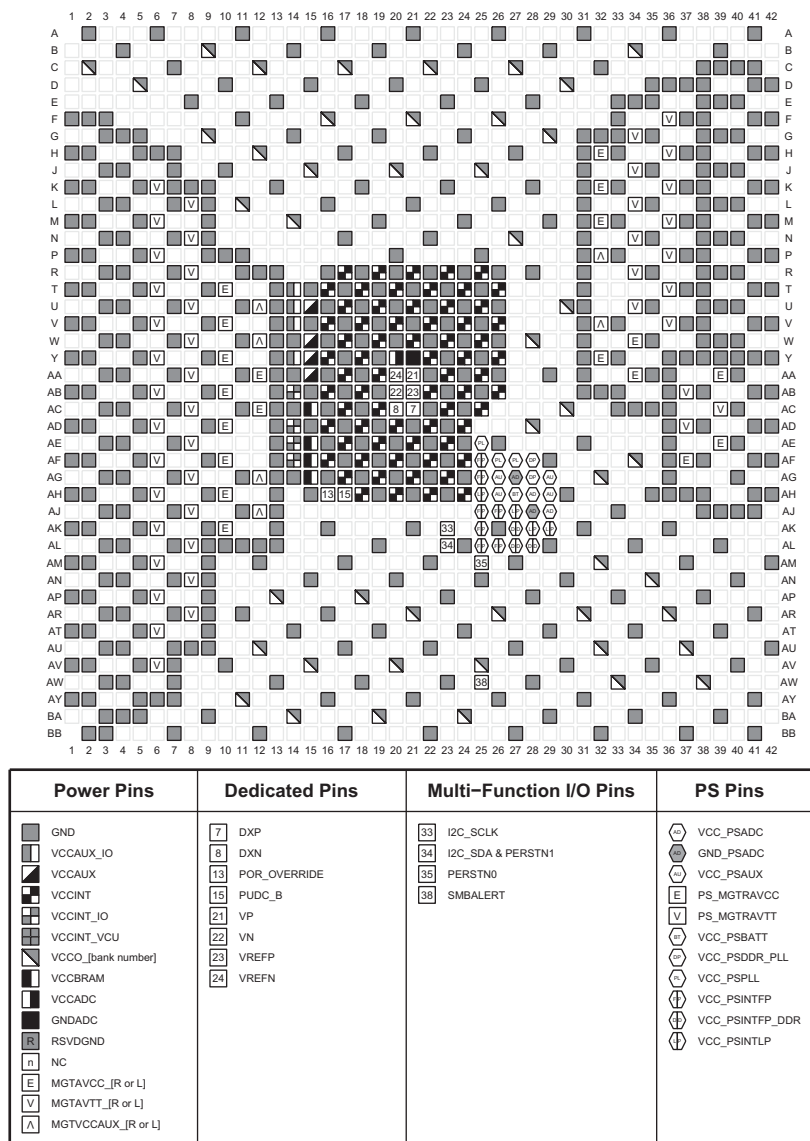


**Figure 4-92: FFVC1760 Package—XCZU17EG and XCZU19EG Power, Dedicated, and Multi-function Pin Diagram**

**Note:** VCCAUX\_IO pins for the XQ versions of these devices in this package are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# FFVD1760 Package—XCZU17EG and XCZU19EG

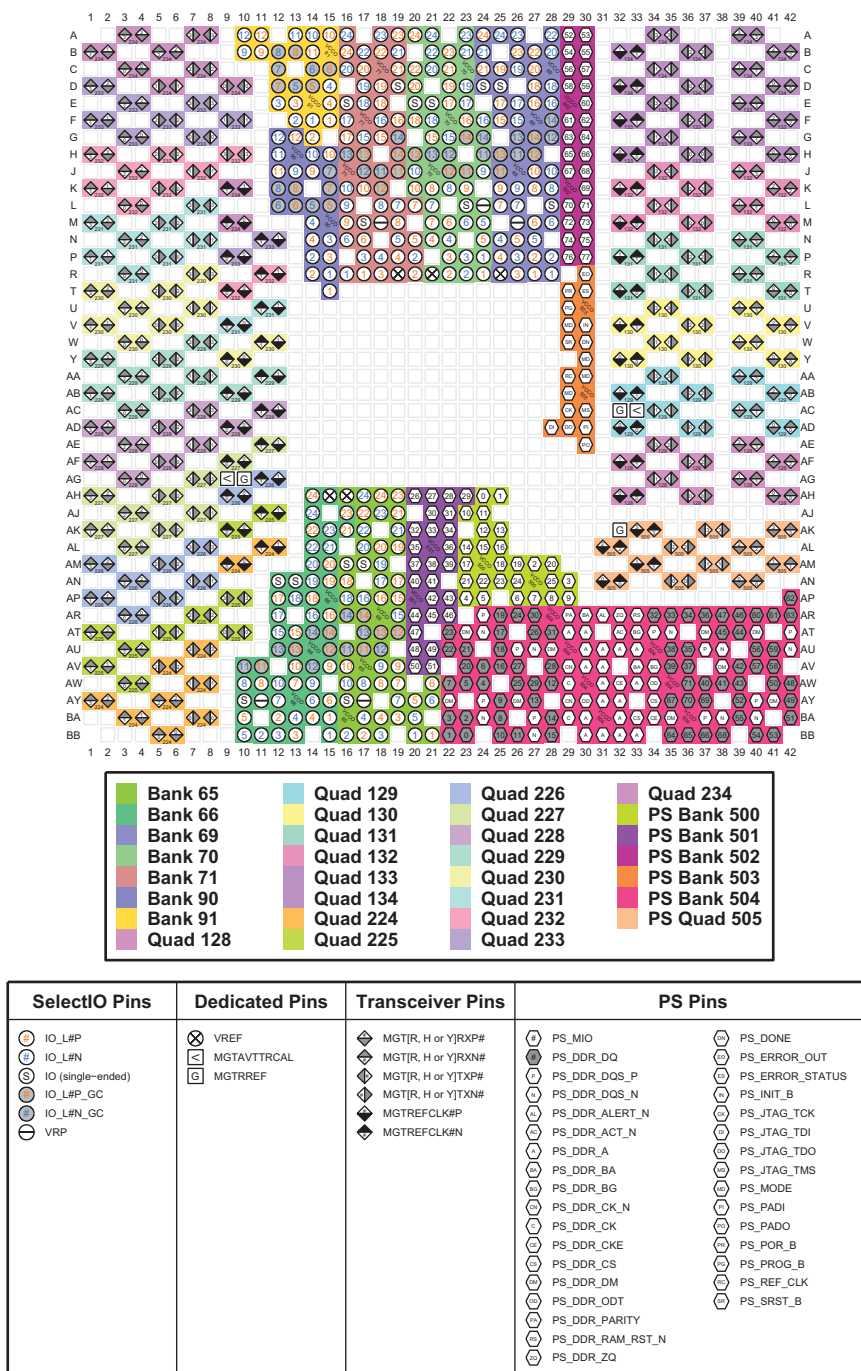


Figure 4-93: FFVD1760 Package—XCZU17EG and XCZU19EG I/O Bank Diagram

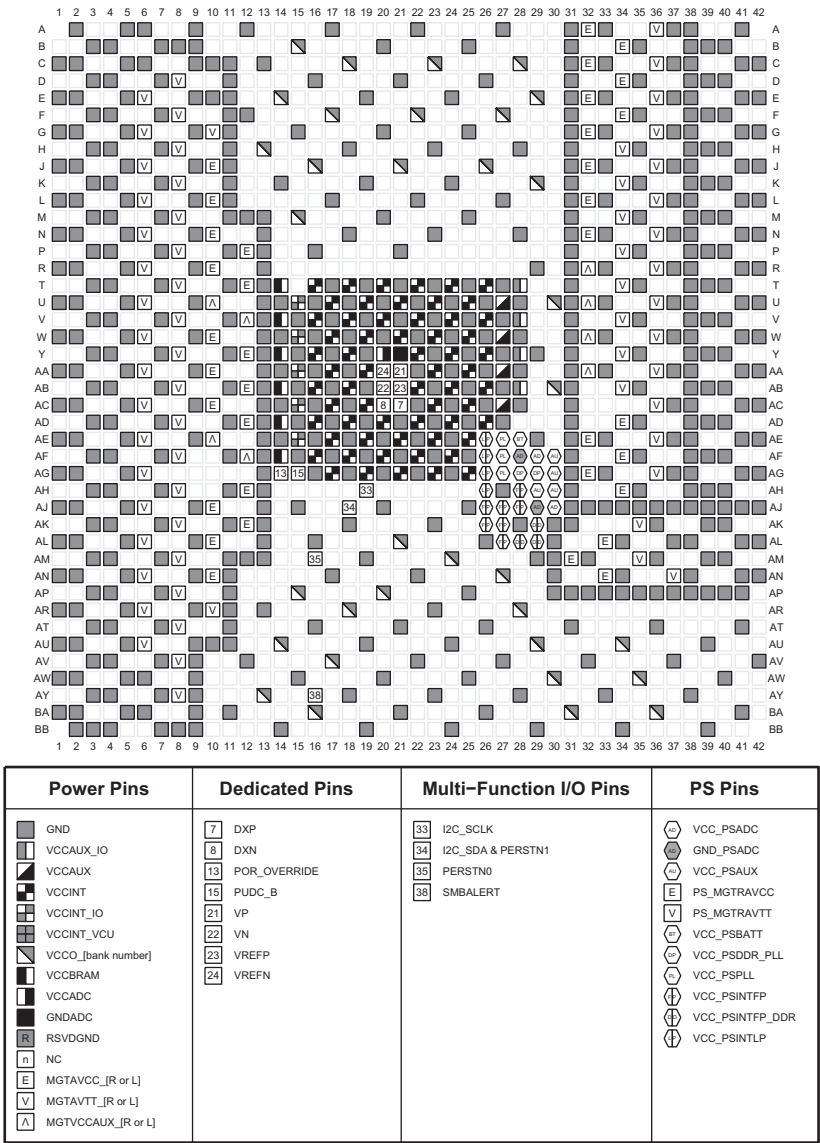


Figure 4-94: FFVD1760 Package—XCZU17EG and XCZU19EG Power, Dedicated, and Multi-function Pin Diagram

# FFVF1760 and FSVF1760 Packages—XCZU29DR and XCZU39DR

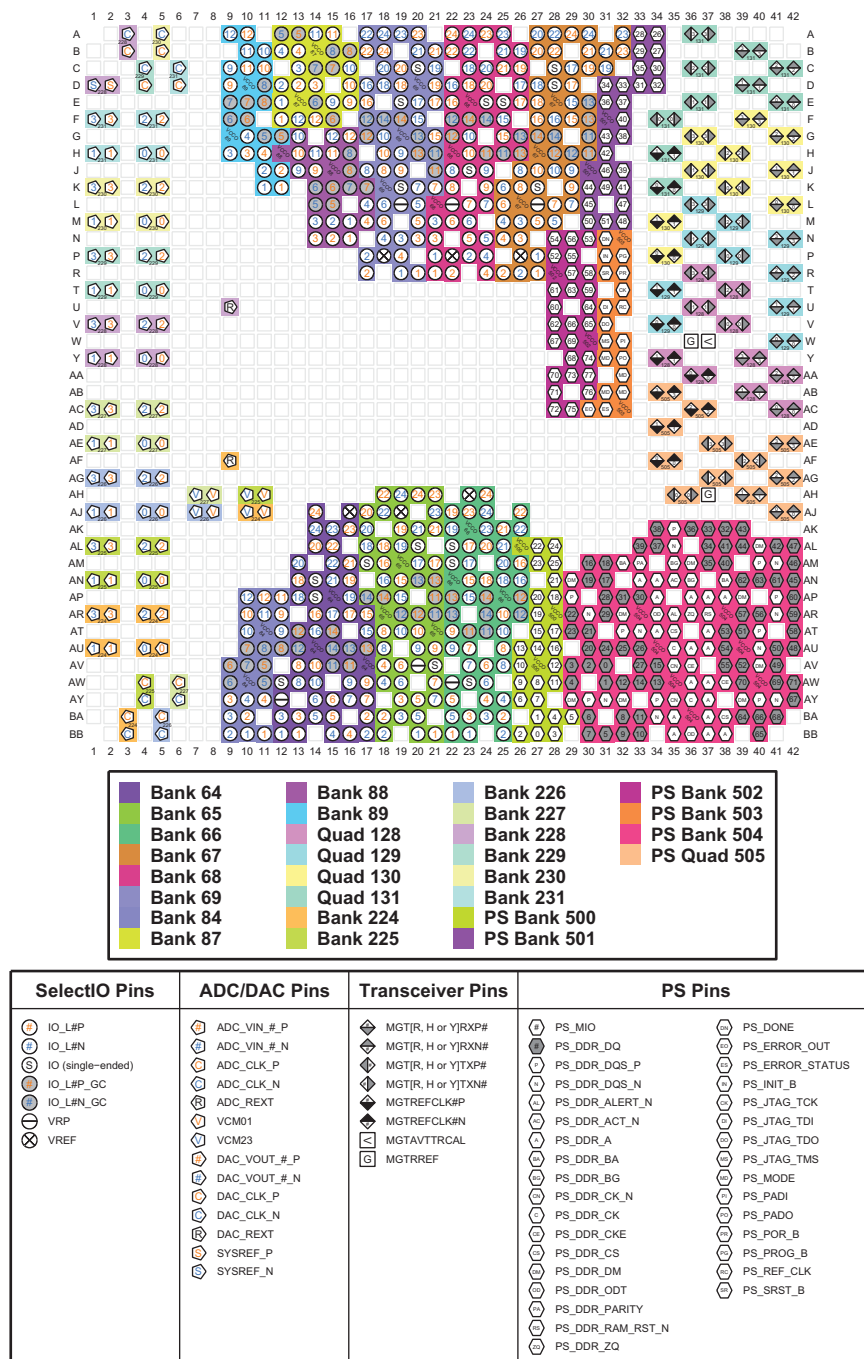


Figure 4-95: FFVF1760 and FSVF1760 Packages—XCZU29DR and XCZU39DR I/O Bank Diagram

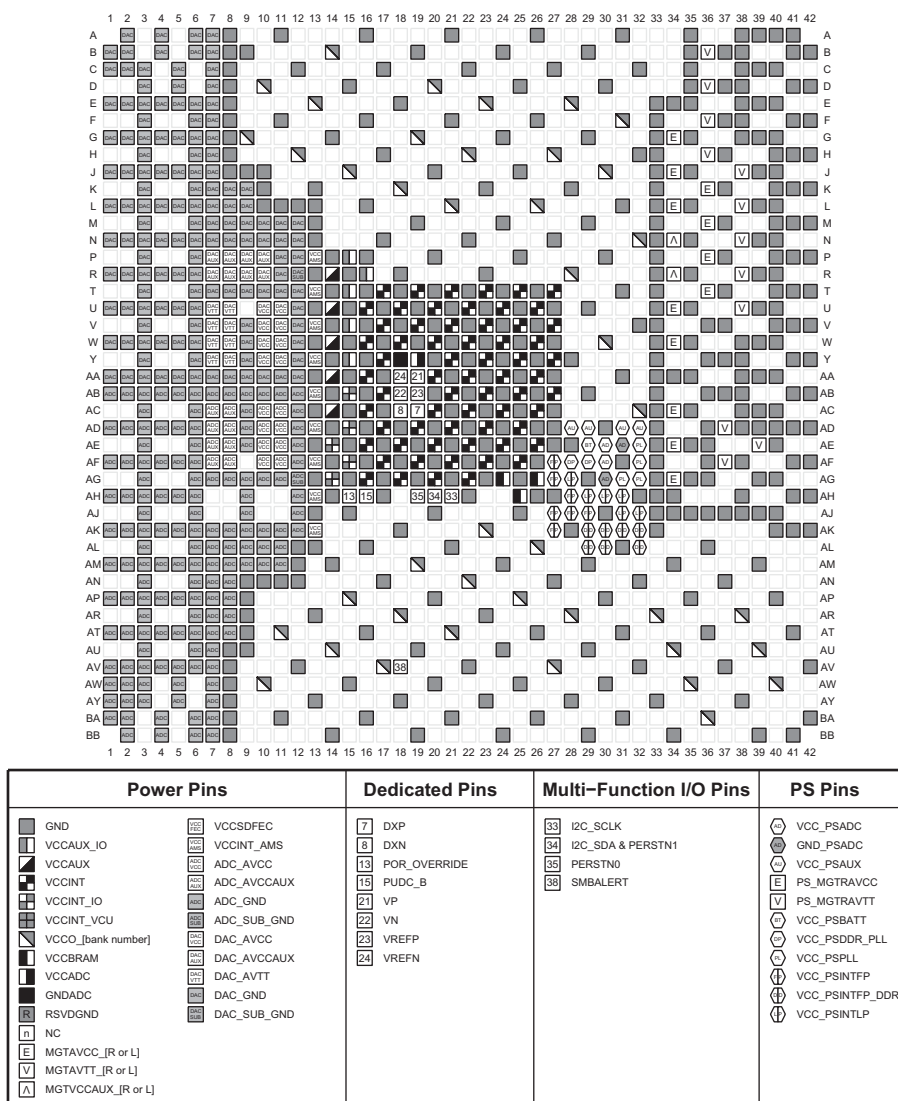


Figure 4-96: FFVF1760 and FSVF1760 Packages—XCZU29DR and XCZU39DR Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of these devices in these packages are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.

# FFVF1760 and FSVF1760 Packages—XCZU49DR FSRF1760 Package—XQZU49DR

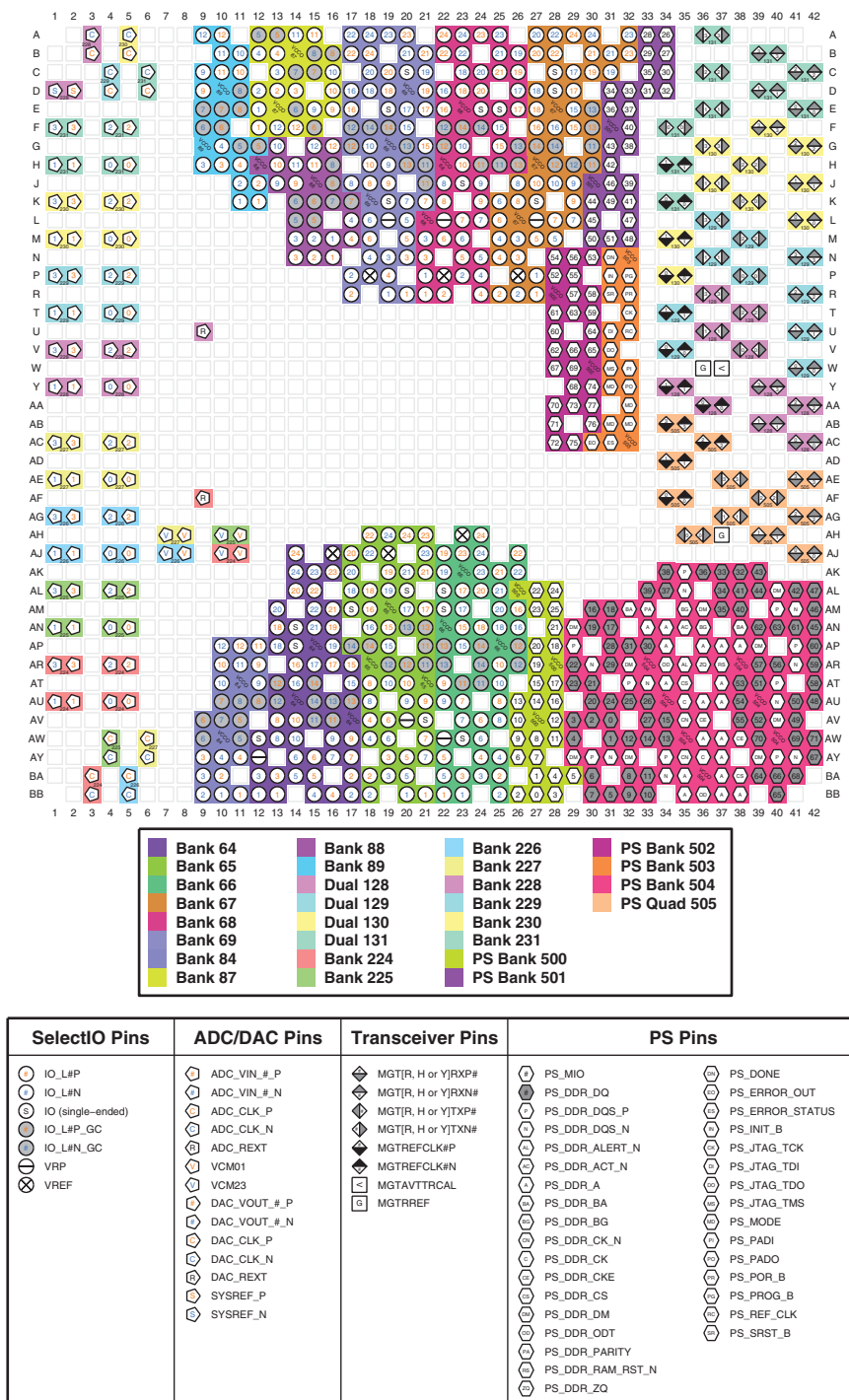
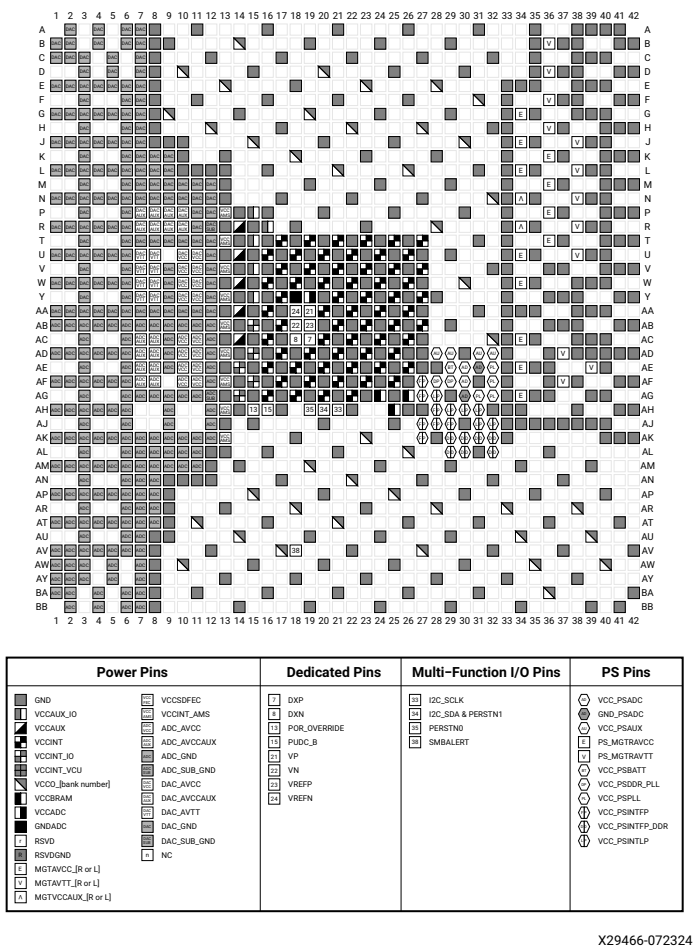


Figure 4-97: FFVF1760, FSVF1760, FSRF1760 Packages—XCZU49DR, XQZU49DR  
I/O Bank Diagram



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Figure 4-98: FFVF1760, FSVF1760, FSRF1760 Packages—XCZU49DR, XQZU49DR Power, Dedicated, and Multi-function Pin Diagram

**Note:** VCCAUX\_IO pins for the XQ versions of these devices in these packages are split into VCCAUX\_HPIO and VCCAUX\_HDIO. Refer to the package files for VCCAUX\_HPIO and VCCAUX\_HDIO pin locations.



# FFVH1760 and FSVH1760 Packages—XCZU46DR

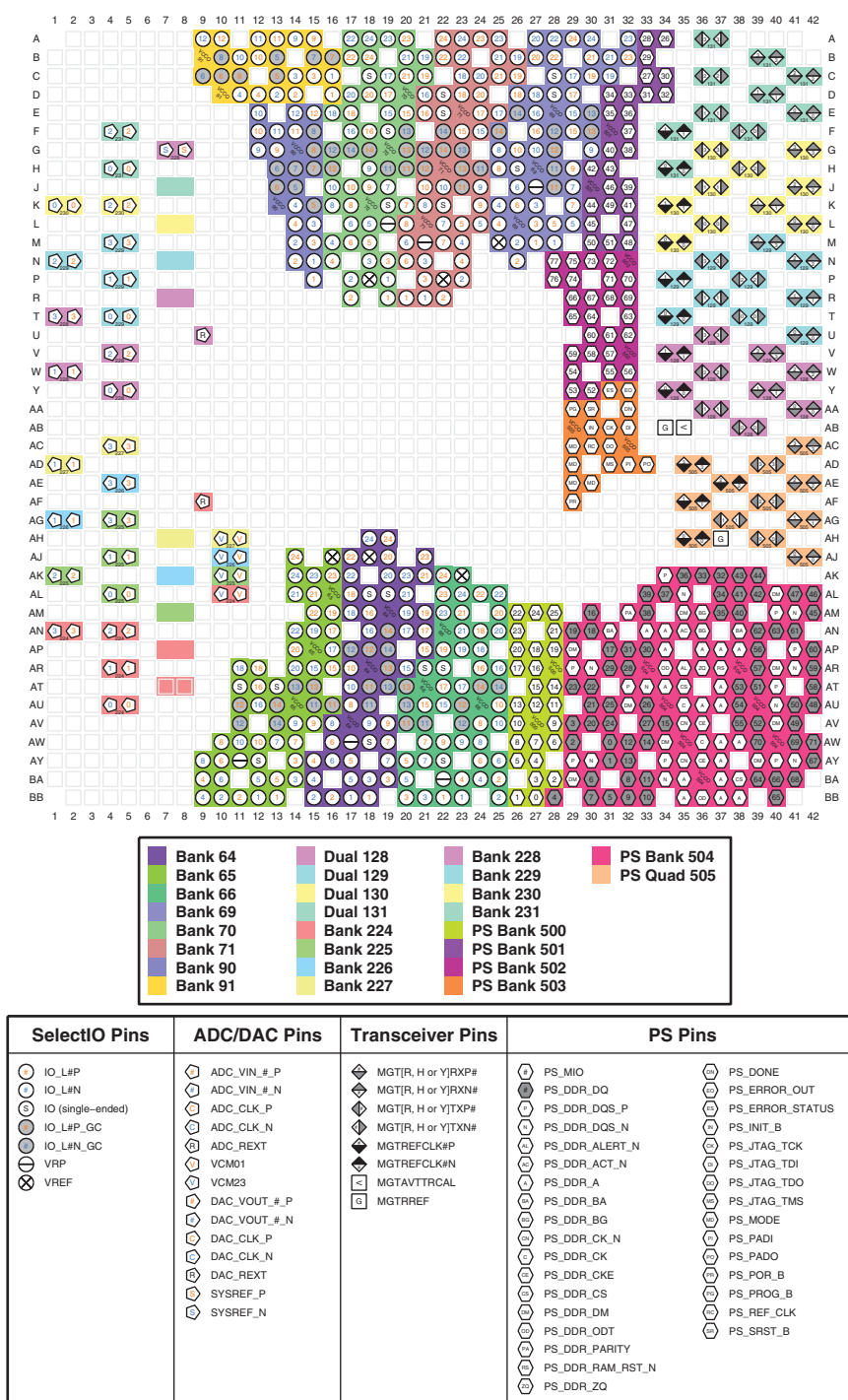
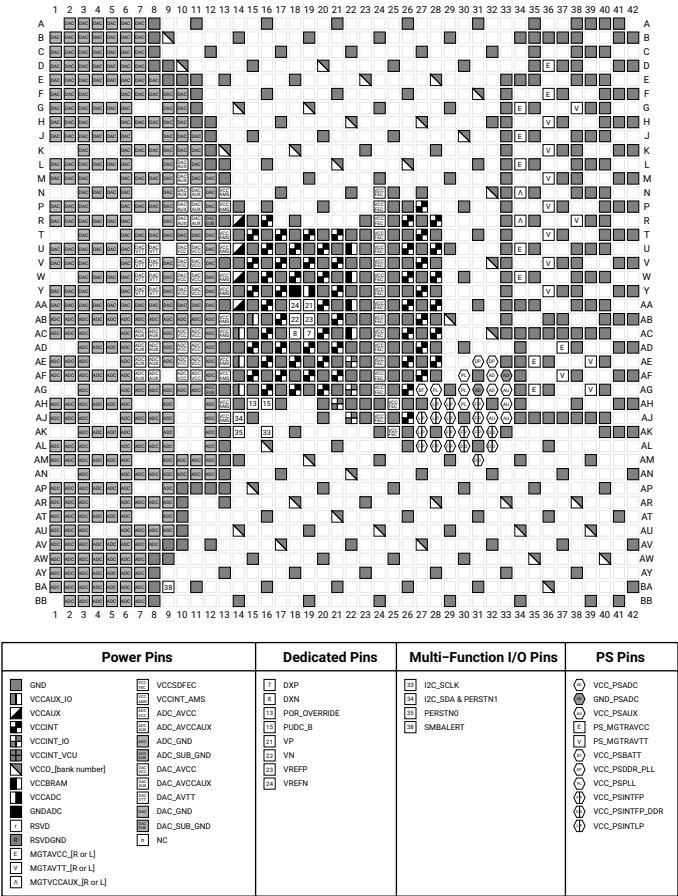


Figure 4-99: FFVH1760 and FSVH1760 Packages—XCZU46DR I/O Bank Diagram





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Figure 4-100: FHVH1760 and FSVH1760 Packages—XCZU46DR Power, Dedicated, and Multi-function Pin Diagram

# FFVE1924 Package—XCZU17EG and XCZU19EG

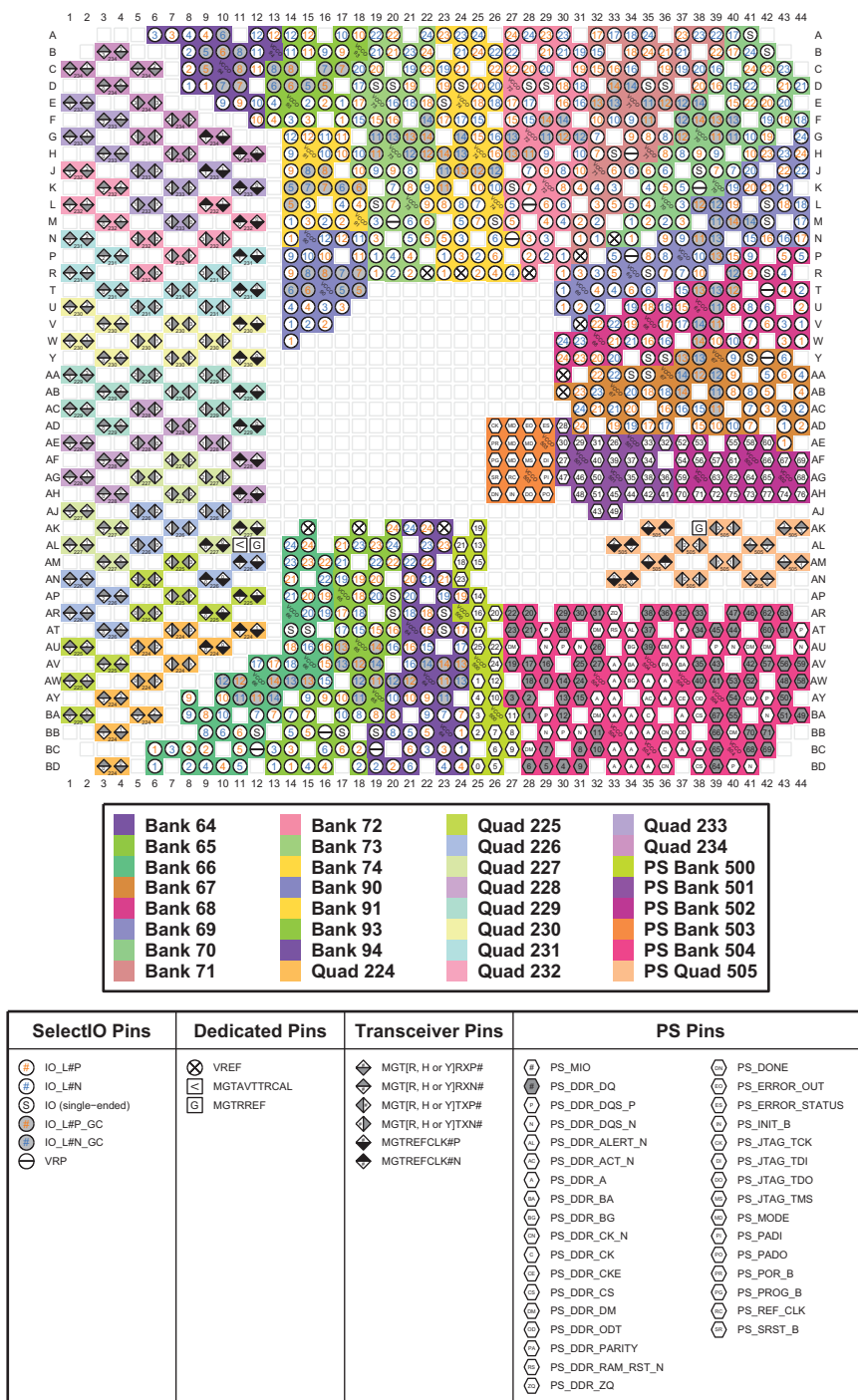


Figure 4-101: FFVE1924 Package—XCZU17EG and XCZU19EG I/O Bank Diagram

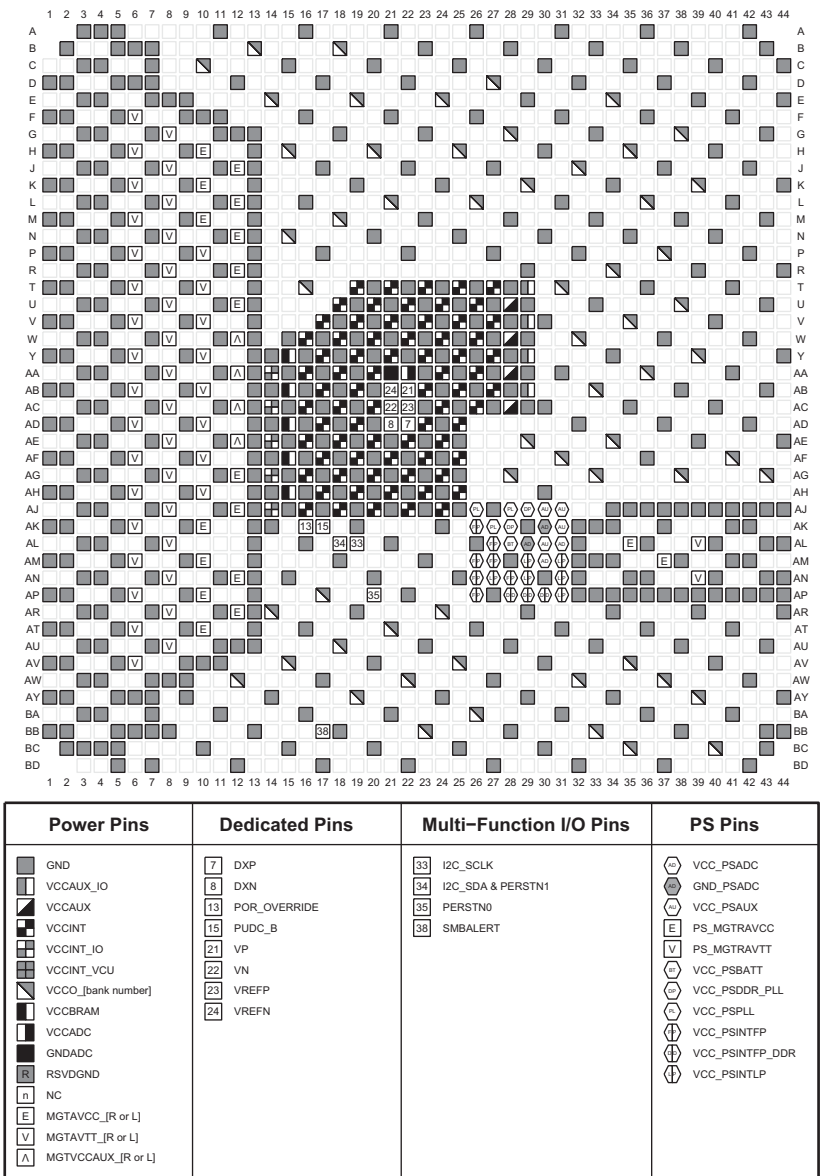


Figure 4-102: FFVE1924 Package—XCZU17EG and XCZU19EG Power, Dedicated, and Multi-function Pin Diagram

# Mechanical Drawings

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## Summary

This chapter provides mechanical drawings (package specifications) of the Zynq™ UltraScale+™ devices. [Table 5-1](#) and [Table 5-2](#) cross-reference to the mechanical drawings by device and package combination. See [Package Specifications Designations in Chapter 3](#) for definitions of [Evaluation Only](#), [Engineering Sample](#), and [Production](#) mechanical drawings.



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**IMPORTANT:** All non-InFO packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC or XA, and the Pb-free signifier in the package name is Q. For the mechanical drawings, refer to the Pb-free version of these packages.

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**TIP:** For information on materials composition and weight of a device, refer to the material declaration data sheet (MDDS). MDDS files: Click on this link to find the Zynq UltraScale+ devices [Packaging Specifications](#). In step 2 select the product category: SoCs, MPSoCs & RFSocS. In step 3, select the product type. In step 4, click on the package specifications selection to find the available MDDS files. All published MDDS files are also available on the [See All Package Specifications](#) page.

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Table 5-1: Cross-Reference to Zynq UltraScale+ MPSoC Mechanical Drawings by Package

| Package | Device                           |                               |                                          |                          |                                          |                                                     |                           |                                                     |                               |                                              |                           |
|---------|----------------------------------|-------------------------------|------------------------------------------|--------------------------|------------------------------------------|-----------------------------------------------------|---------------------------|-----------------------------------------------------|-------------------------------|----------------------------------------------|---------------------------|
|         | XCZU1CG<br>XCZU1EG<br>XAZU1EG    | XCZU2CG<br>XCZU2EG<br>XAZU2EG | XCZU3CG<br>XCZU3EG<br>XAZU3EG<br>XQZU3EG | XCZU3TCG<br>XCZU3TEG     | XCZU4CG<br>XCZU4EG<br>XCZU4EV<br>XAZU4EV | XCZU5CG<br>XCZU5EG<br>XCZU5EV<br>XAZU5EV<br>XQZU5EV | XCZU6CG<br>XCZU6EG        | XCZU7CG<br>XCZU7EG<br>XCZU7EV<br>XAZU7EV<br>XQZU7EV | XCZU9CG<br>XCZU9EG<br>XQZU9EG | XCZU11EG<br>XAZU11EG<br>XQZU11EG<br>XQZU12EG |                           |
| SBVA484 | Figure 5-1<br>Production         | Figure 5-2<br>Production      |                                          |                          |                                          |                                                     |                           |                                                     |                               |                                              |                           |
| SFRA484 |                                  |                               | Figure 5-3<br>Production                 |                          |                                          |                                                     |                           |                                                     |                               |                                              |                           |
| UBVA494 | Figure 5-4<br>Engineering Sample |                               |                                          |                          |                                          |                                                     |                           |                                                     |                               |                                              |                           |
| UBVA530 |                                  | Figure 5-5<br>Production      | Figure 5-5<br>Production                 |                          |                                          |                                                     |                           |                                                     |                               |                                              |                           |
| SFVA625 | Figure 5-6<br>Production         | Figure 5-7<br>Production      |                                          |                          |                                          |                                                     |                           |                                                     |                               |                                              |                           |
| SFRC784 |                                  |                               | Figure 5-8<br>Production                 |                          | Figure 5-8<br>Production                 |                                                     |                           |                                                     |                               |                                              |                           |
| SFVC784 | Figure 5-9<br>Production         |                               | Figure 5-9<br>Production                 | Figure 5-9<br>Production |                                          |                                                     |                           |                                                     |                               |                                              |                           |
| SFVD784 |                                  |                               |                                          |                          | Figure 5-9<br>Production                 |                                                     |                           |                                                     |                               |                                              |                           |
| SFVE784 |                                  |                               |                                          |                          | Figure 5-9<br>Production                 |                                                     |                           |                                                     |                               |                                              |                           |
| FBVB900 |                                  |                               |                                          |                          | Figure 5-10<br>Production                |                                                     | Figure 5-11<br>Production |                                                     |                               |                                              |                           |
| FFRB900 |                                  |                               |                                          |                          | Figure 5-13<br>Production                |                                                     | Figure 5-12<br>Production |                                                     |                               |                                              |                           |
| FFRC900 |                                  |                               |                                          |                          |                                          |                                                     |                           |                                                     |                               | Figure 5-13<br>Production                    | Figure 5-13<br>Production |

Table 5-1: Cross-Reference to Zynq UltraScale+ MPSoC Mechanical Drawings by Package (Cont'd)

| Package  | Device                        |                               |                                          |                      |                                          |                                                     |                           |                                                     |                               |                                  |                                            |                           |
|----------|-------------------------------|-------------------------------|------------------------------------------|----------------------|------------------------------------------|-----------------------------------------------------|---------------------------|-----------------------------------------------------|-------------------------------|----------------------------------|--------------------------------------------|---------------------------|
|          | XCZU1CG<br>XCZU1EG<br>XAZU1EG | XCZU2CG<br>XCZU2EG<br>XAZU2EG | XCZU3CG<br>XCZU3EG<br>XAZU3EG<br>XQZU3EG | XCZU3TCG<br>XCZU3TEG | XCZU4CG<br>XCZU4EG<br>XCZU4EV<br>XAZU4EV | XCZU5CG<br>XCZU5EG<br>XCZU5EV<br>XAZU5EV<br>XQZU5EV | XCZU6CG<br>XCZU6EG        | XCZU7CG<br>XCZU7EG<br>XCZU7EV<br>XAZU7EV<br>XQZU7EV | XCZU9CG<br>XCZU9EG<br>XQZU9EG | XCZU11EG<br>XAZU11EG<br>XQZU11EG | XCZU12EG<br>XCZU12G<br>XAZU12EG<br>XQZU12G |                           |
| FFVC900  |                               |                               |                                          |                      |                                          |                                                     | Figure 5-14<br>Production |                                                     | Figure 5-14<br>Production     |                                  | Figure 5-14<br>Production                  |                           |
| FFRB1156 |                               |                               |                                          |                      |                                          |                                                     |                           |                                                     |                               |                                  |                                            | Figure 5-15<br>Production |
| FFVB1156 |                               |                               |                                          |                      |                                          |                                                     | Figure 5-16<br>Production |                                                     | Figure 5-16<br>Production     |                                  | Figure 5-16<br>Production                  |                           |
| FFRC1156 |                               |                               |                                          |                      |                                          |                                                     |                           |                                                     | Figure 5-17<br>Production     |                                  | Figure 5-17<br>Production                  |                           |
| FFVC1156 |                               |                               |                                          |                      |                                          |                                                     |                           |                                                     | Figure 5-18<br>Production     |                                  | Figure 5-18<br>Production                  |                           |
| FFRB1517 |                               |                               |                                          |                      |                                          |                                                     |                           |                                                     |                               |                                  |                                            |                           |
| FFVB1517 |                               |                               |                                          |                      |                                          |                                                     |                           |                                                     |                               |                                  |                                            | Figure 5-25<br>Production |
| FFVF1517 |                               |                               |                                          |                      |                                          |                                                     |                           |                                                     | Figure 5-25<br>Production     |                                  | Figure 5-25<br>Production                  |                           |
| FFRC1760 |                               |                               |                                          |                      |                                          |                                                     |                           |                                                     |                               |                                  |                                            | Figure 5-31<br>Production |
| FFVC1760 |                               |                               |                                          |                      |                                          |                                                     |                           |                                                     |                               |                                  |                                            | Figure 5-30<br>Production |
| FFVD1760 |                               |                               |                                          |                      |                                          |                                                     |                           |                                                     |                               |                                  |                                            |                           |
| FFVE1924 |                               |                               |                                          |                      |                                          |                                                     |                           |                                                     |                               |                                  |                                            |                           |

Table 5-2: Cross-Reference to Zynq UltraScale+ RFSoc Mechanical Drawings by Package

| Package  | Device                    |                           |                           |                           |                           |                           |                           |                                              |
|----------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|----------------------------------------------|
|          | XCZU21DR<br>XQZU21DR      | XCZU25DR<br>XCZU27DR      | XCZU28DR<br>XQZU28DR      | XCZU29DR<br>XQZU29DR      | XCZU39DR                  | XCZU42DR                  | XCZU43DR                  | XCZU46DR<br>XCZU47DR<br>XCZU48DR<br>XQZU48DR |
| FFRD1156 | Figure 5-19<br>Production |                           |                           |                           |                           |                           |                           |                                              |
| FFVD1156 | Figure 5-21<br>Production |                           |                           |                           |                           |                           |                           |                                              |
| FFRE1156 |                           |                           | Figure 5-20<br>Production |                           |                           |                           |                           | Figure 5-20<br>Production                    |
| FFVE1156 |                           | Figure 5-21<br>Production | Figure 5-21<br>Production |                           |                           | Figure 5-21<br>Production | Figure 5-21<br>Production | Figure 5-21<br>Production                    |
| FSVE1156 |                           | Figure 5-22<br>Production | Figure 5-22<br>Production |                           |                           | Figure 5-22<br>Production | Figure 5-22<br>Production | Figure 5-22<br>Production                    |
| FFRG1517 |                           |                           | Figure 5-26<br>Production |                           |                           |                           |                           |                                              |
| FFVG1517 |                           | Figure 5-27<br>Production | Figure 5-27<br>Production |                           |                           |                           | Figure 5-27<br>Production | Figure 5-27<br>Production                    |
| FSRG1517 |                           |                           |                           |                           |                           |                           |                           | Figure 5-28<br>Production                    |
| FSVG1517 |                           | Figure 5-29<br>Production | Figure 5-29<br>Production |                           |                           |                           | Figure 5-29<br>Production | Figure 5-29<br>Production                    |
| FFRF1760 |                           |                           |                           | Figure 5-33<br>Production |                           |                           |                           |                                              |
| FFVF1760 |                           |                           |                           | Figure 5-32<br>Production | Figure 5-32<br>Production |                           |                           | Figure 5-32<br>Production                    |
| FSRF1760 |                           |                           |                           |                           |                           |                           |                           | Figure 5-32<br>Production                    |

Table 5-2: Cross-Reference to Zynq UltraScale+ RFSoc Mechanical Drawings by Package (Cont'd)

| Package  | Device               |                      |                      |                           |                           |          |          |                                              |
|----------|----------------------|----------------------|----------------------|---------------------------|---------------------------|----------|----------|----------------------------------------------|
|          | XCZU21DR<br>XQZU21DR | XCZU25DR<br>XCZU27DR | XCZU28DR<br>XQZU28DR | XCZU29DR<br>XQZU29DR      | XCZU39DR                  | XCZU42DR | XCZU43DR | XCZU46DR<br>XCZU47DR<br>XCZU48DR<br>XQZU48DR |
| FSVF1760 |                      |                      |                      | Figure 5-34<br>Production | Figure 5-34<br>Production |          |          | Figure 5-32<br>Production                    |
| FFVH1760 |                      |                      |                      |                           |                           |          |          | Figure 5-32<br>Production                    |
| FSVH1760 |                      |                      |                      |                           |                           |          |          | Figure 5-34<br>Production                    |



Table 5-3: Mechanical Drawing Dimension Definitions

| Dimension                      | Definition                                                                                                                                                      |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $\ominus$                      | Bilateral tolerance of package sides with respect to datums A and B                                                                                             |
| $\square$                      | Flatness tolerance of silicon die or package lid top surface                                                                                                    |
| //                             | Bilateral tolerance for parallelism of silicon die or package lid top surface with respect to the seating plane datum C                                         |
| A                              | Thickness of package with respect to the seating plane datum C                                                                                                  |
| A <sub>1</sub>                 | Thickness of BGA balls with respect to the seating plane datum C                                                                                                |
| A <sub>2</sub>                 | Thickness of package body, including stiffener ring or lid and excluding BGA balls, with respect to the seating plane datum C                                   |
| A <sub>3</sub>                 | Distance from top of silicon die to top of stiffener ring or lid with respect to the seating plane datum C                                                      |
| D/E                            | Length/width of package with respect to datums A and B                                                                                                          |
| D <sub>1</sub> /E <sub>1</sub> | Length/width of BGA matrix with respect to datums A and B                                                                                                       |
| e                              | BGA ball pitch measured at the center of each ball                                                                                                              |
| øb                             | BGA ball diameter                                                                                                                                               |
| $\ominus_{aaa}$                | Unidirectional upward tolerance with respect to the seating plane datum C                                                                                       |
| // bbb                         | Bilateral tolerance for parallelism of package surface with respect to the seating plane datum C                                                                |
| øddd                           | BGA ball position tolerance of diameter ddd with respect to datums A and B perpendicular to the seating plane datum C in which the center of each ball must lie |
| øeee                           | BGA ball position tolerance of diameter eee measured with respect to other balls within the BGA matrix in which the center of each ball must lie                |
| M                              | BGA ball matrix size                                                                                                                                            |

# SBVA484 Flip-Chip, Super-Fine-Pitch BGA (XCZU1CG, XCZU1EG, and XAZU1EG)

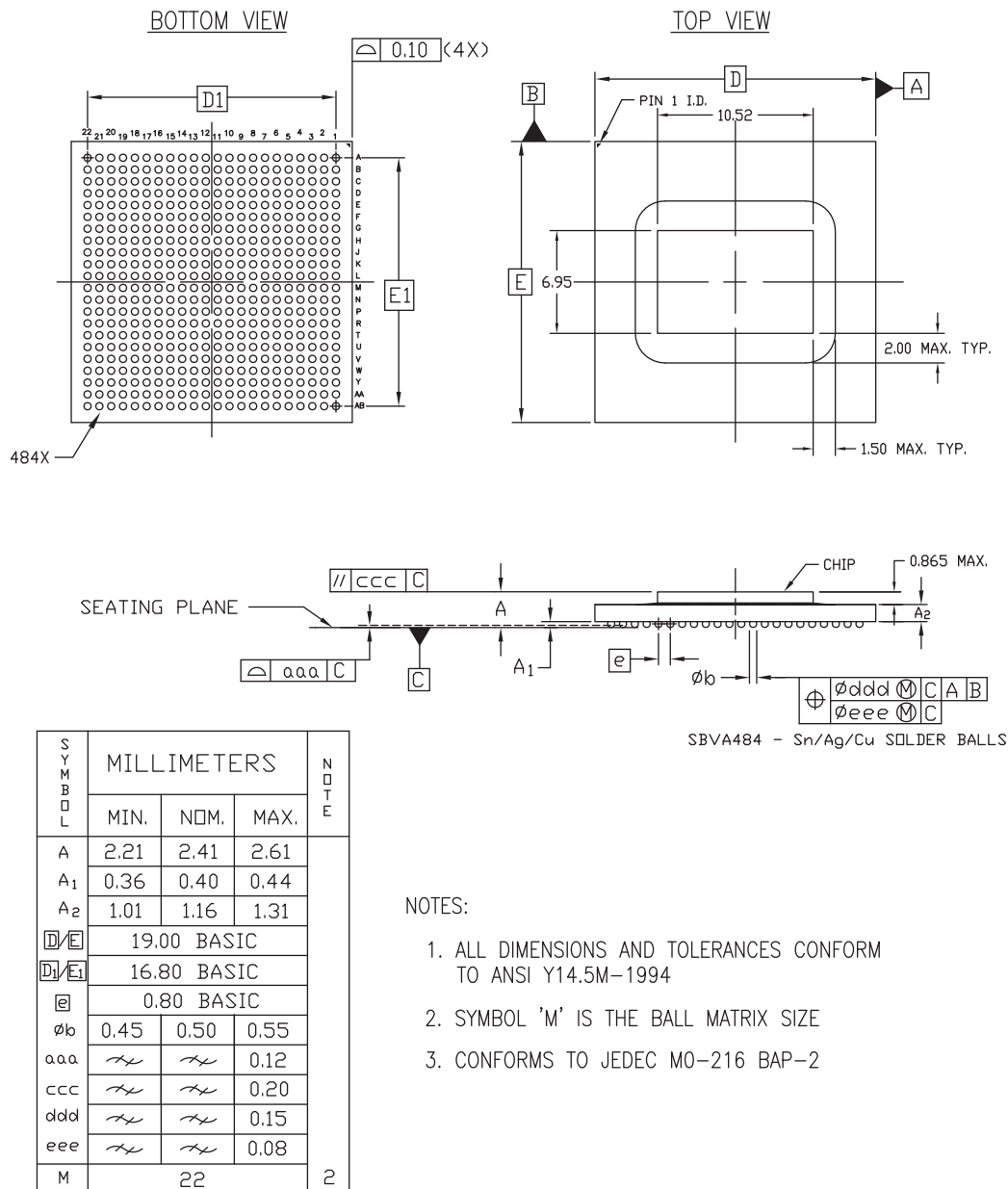


Figure 5-1: Package Dimensions for SBVA484 (XCZU1CG, XCZU1EG, and XAZU1EG)

# SBVA484 Flip-Chip, Super-Fine-Pitch BGA (XCZU2, XCZU3, XAZU2EG, and XAZU3EG)

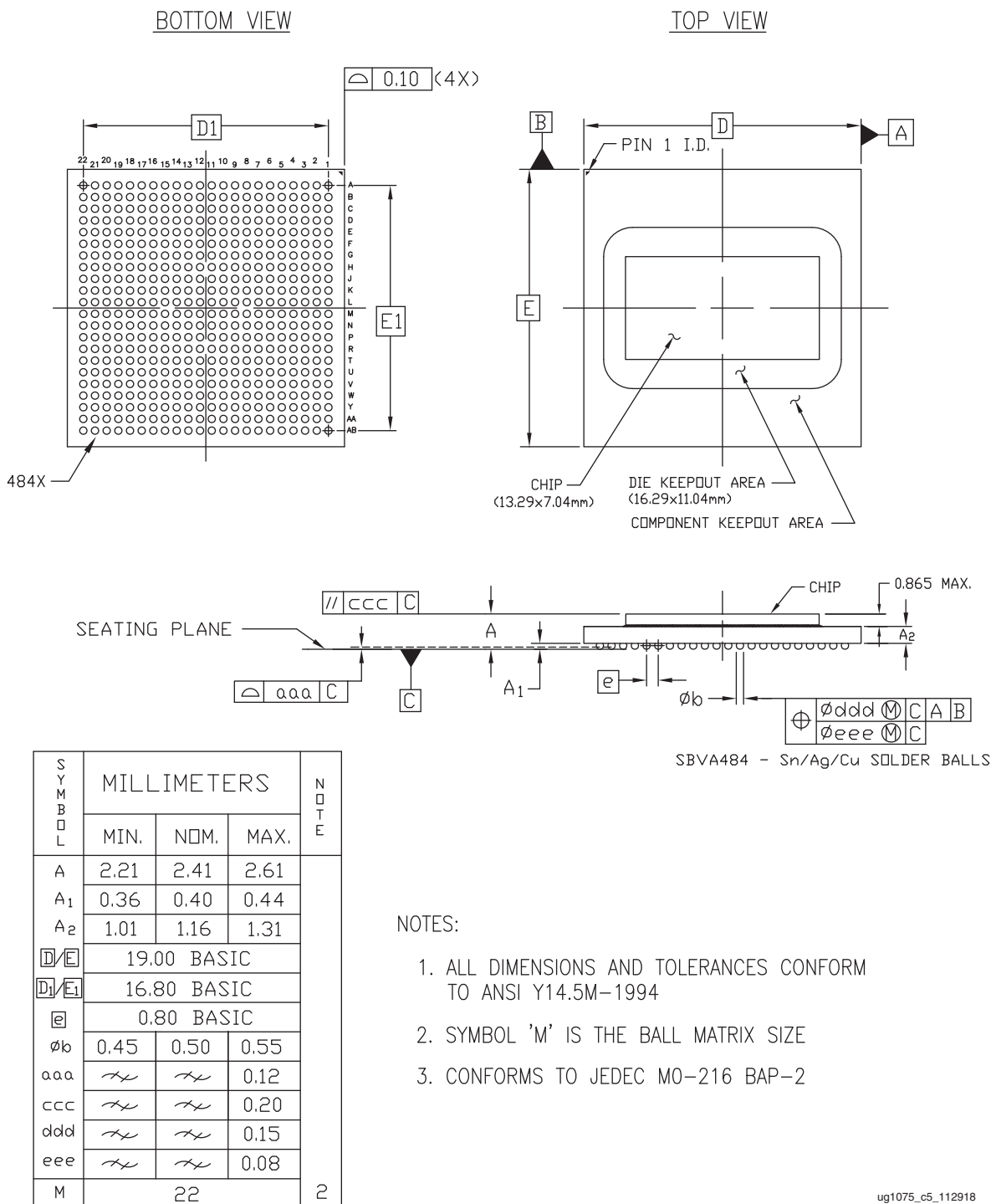
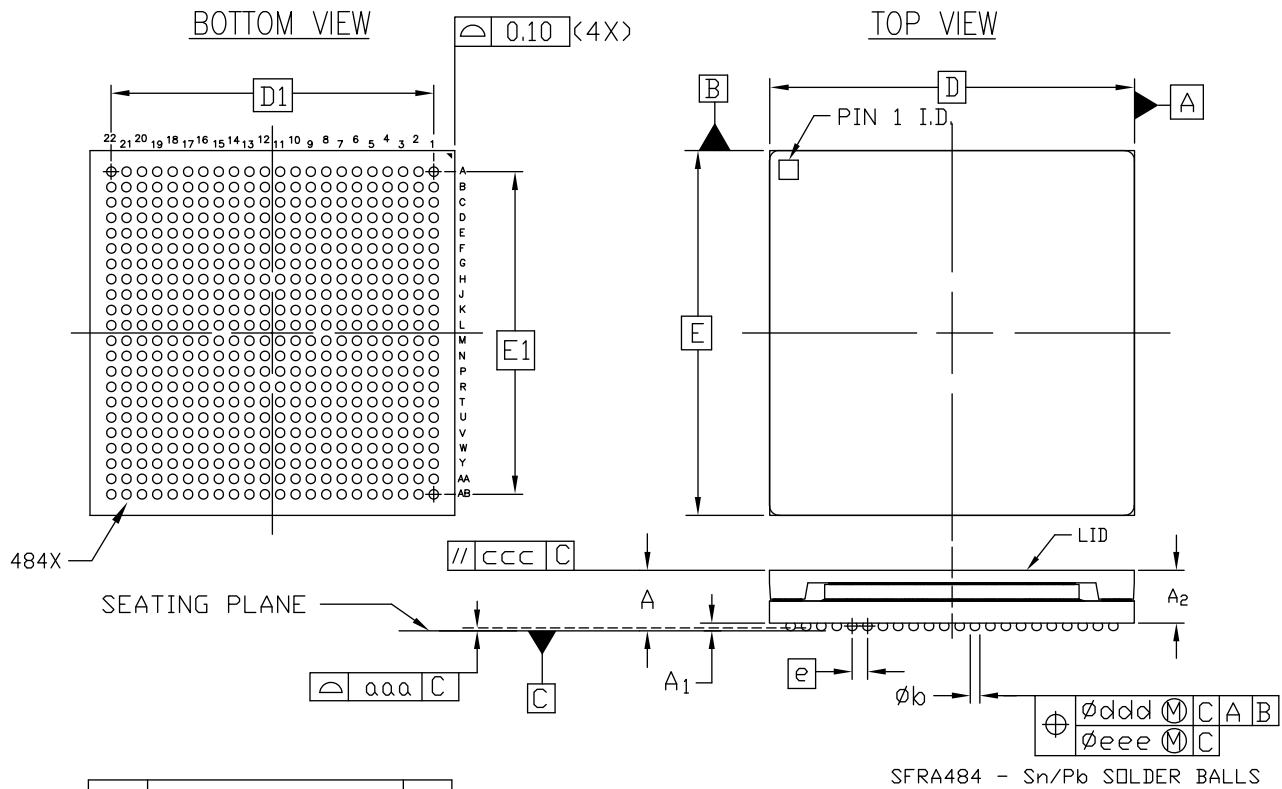


Figure 5-2: Package Dimensions for SBVA484 (XCZU2, XCZU3, XAZU2EG, and XAZU3EG)

# SFRA484 Flip-Chip, Super-Fine-Pitch BGA (XQZU3EG)



| SYMBOL                         | MILLIMETERS                                                                         |                                                                                     |      | NOTE |
|--------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|------|------|
|                                | MIN.                                                                                | NOM.                                                                                | MAX. |      |
| A                              | 2.95                                                                                | 3.15                                                                                | 3.35 | 2    |
| A <sub>1</sub>                 | 0.36                                                                                | 0.40                                                                                | 0.44 |      |
| A <sub>2</sub>                 | 2.55                                                                                | 2.75                                                                                | 2.95 |      |
| D/E                            | 19.00 BASIC                                                                         |                                                                                     |      |      |
| D <sub>1</sub> /E <sub>1</sub> | 16.80 BASIC                                                                         |                                                                                     |      |      |
| ⓔ                              | 0.80 BASIC                                                                          |                                                                                     |      |      |
| øb                             | 0.45                                                                                | 0.50                                                                                | 0.55 |      |
| aaa                            |  |  | 0.12 |      |
| ccc                            |  |  | 0.20 |      |
| ddd                            |  |  | 0.15 |      |
| eee                            |  |  | 0.08 |      |
| M                              | 22                                                                                  |                                                                                     |      |      |

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO-216 BAP-2

X29043-020224

**Figure 5-3: Package Dimensions for SFRA484 (XQZU3EG)**

# UBVA494 Flip-Chip, InFO BGA (XCZU1)

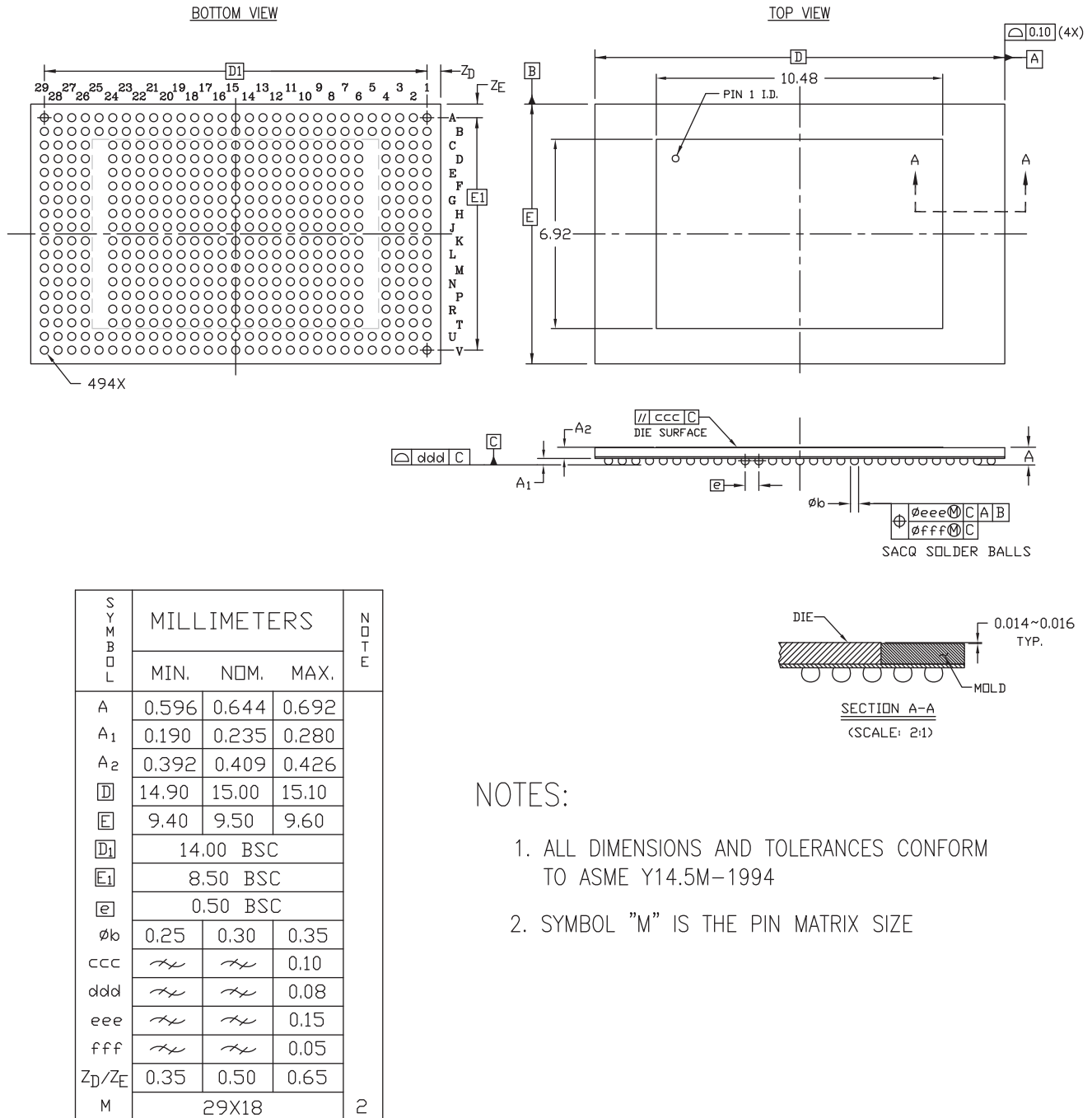
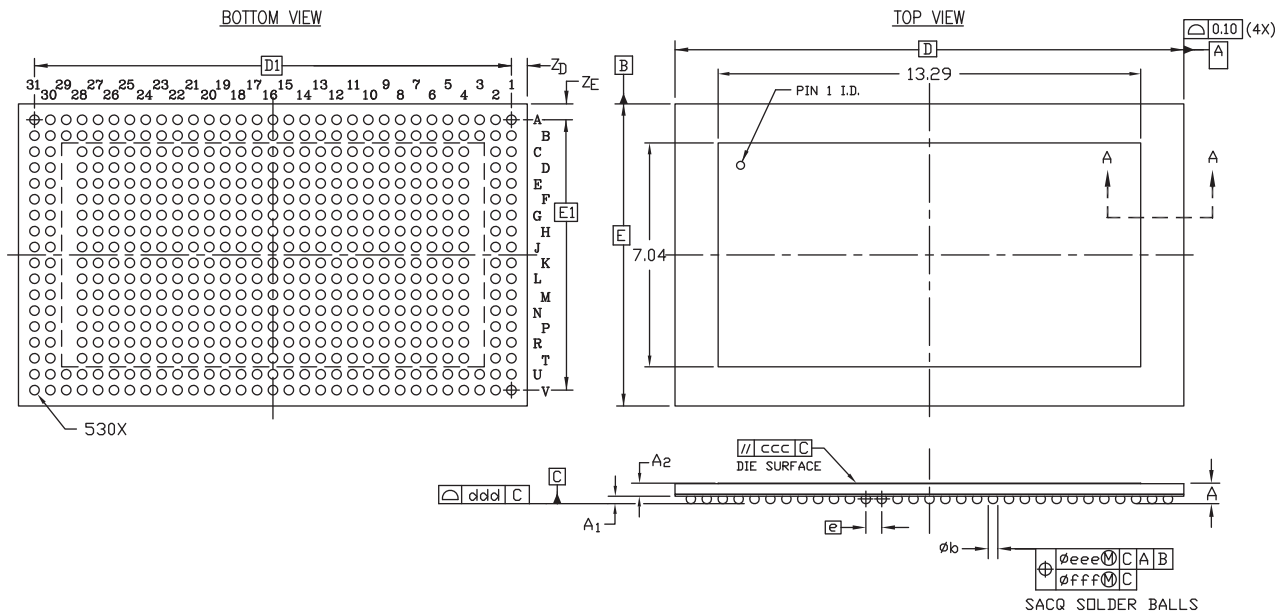
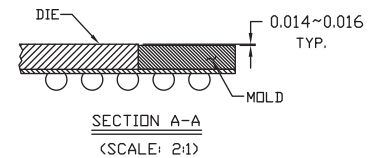


Figure 5-4: Package Dimensions for UBVA494 (XCZU1)

# UBVA530 Flip-Chip, InFO BGA (XCZU2, XCZU3)



| SYMBOL                         | MILLIMETERS |       |       | NOTE |
|--------------------------------|-------------|-------|-------|------|
|                                | MIN.        | NOM.  | MAX.  |      |
| A                              | 0.596       | 0.644 | 0.692 | 2    |
| A <sub>1</sub>                 | 0.190       | 0.235 | 0.280 |      |
| A <sub>2</sub>                 | 0.392       | 0.409 | 0.426 |      |
| D                              | 15.90       | 16.00 | 16.10 |      |
| E                              | 9.40        | 9.50  | 9.60  |      |
| D <sub>1</sub>                 | 15.00 BSC   |       |       |      |
| E <sub>1</sub>                 | 8.50 BSC    |       |       |      |
| e                              | 0.50 BSC    |       |       |      |
| øb                             | 0.25        | 0.30  | 0.35  |      |
| ccc                            | ✓           | ✓     | 0.10  |      |
| ddd                            | ✓           | ✓     | 0.08  |      |
| eee                            | ✓           | ✓     | 0.15  |      |
| fff                            | ✓           | ✓     | 0.05  |      |
| Z <sub>D</sub> /Z <sub>E</sub> | 0.35        | 0.50  | 0.65  |      |
| M                              | 31X18       |       |       |      |



## NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE

Figure 5-5: Package Dimensions for UBVA530 (XCZU2, XCZU3)



**IMPORTANT:** The weight for the UBVA530 is 0.2 grams.

**BOTTOM VIEW**

625X

D1

E1

0.10 (4X)

**TOP VIEW**

D

E

A

B

C

PIN 1 I.D.

0.20

0.20

17.32 SQ. MAX.

18.22 SQ. MAX.

SEATING PLANE

A

A1

A2

e

øb

1.34

1.83

LID

SFVA625 - Sn/Ag/Cu SOLDER BALLS

| SYMBOL                         | MILLIMETERS       |                   |      | NOTE |  |
|--------------------------------|-------------------|-------------------|------|------|--|
|                                | MIN.              | NOM.              | MAX. |      |  |
| A                              | 2.93              | 3.13              | 3.33 | 2    |  |
| A <sub>1</sub>                 | 0.36              | 0.40              | 0.44 |      |  |
| A <sub>2</sub>                 | 2.53              | 2.73              | 2.93 |      |  |
| D/E                            | 21.00 BASIC       |                   |      |      |  |
| D <sub>1</sub> /E <sub>1</sub> | 19.20 BASIC       |                   |      |      |  |
| e                              | 0.80 BASIC        |                   |      |      |  |
| øb                             | 0.45              | 0.50              | 0.55 |      |  |
| aaa                            | $\sqrt{\text{X}}$ | $\sqrt{\text{X}}$ | 0.12 | 2    |  |
| ccc                            | $\sqrt{\text{X}}$ | $\sqrt{\text{X}}$ | 0.20 |      |  |
| ddd                            | $\sqrt{\text{X}}$ | $\sqrt{\text{X}}$ | 0.15 |      |  |
| eee                            | $\sqrt{\text{X}}$ | $\sqrt{\text{X}}$ | 0.08 |      |  |
| M                              | 25                |                   |      | 2    |  |

**NOTES:**

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO-216 BAS-1

**Figure 5-6: Package Dimensions for SFVA625 (XCZU1CG, XCZU1EG, and XAZU1EG)**

# SFVA625 Flip-Chip, Super-Fine-Pitch BGA (XCZU2, XCZU3, XAZU2EG, and XAZU3EG)

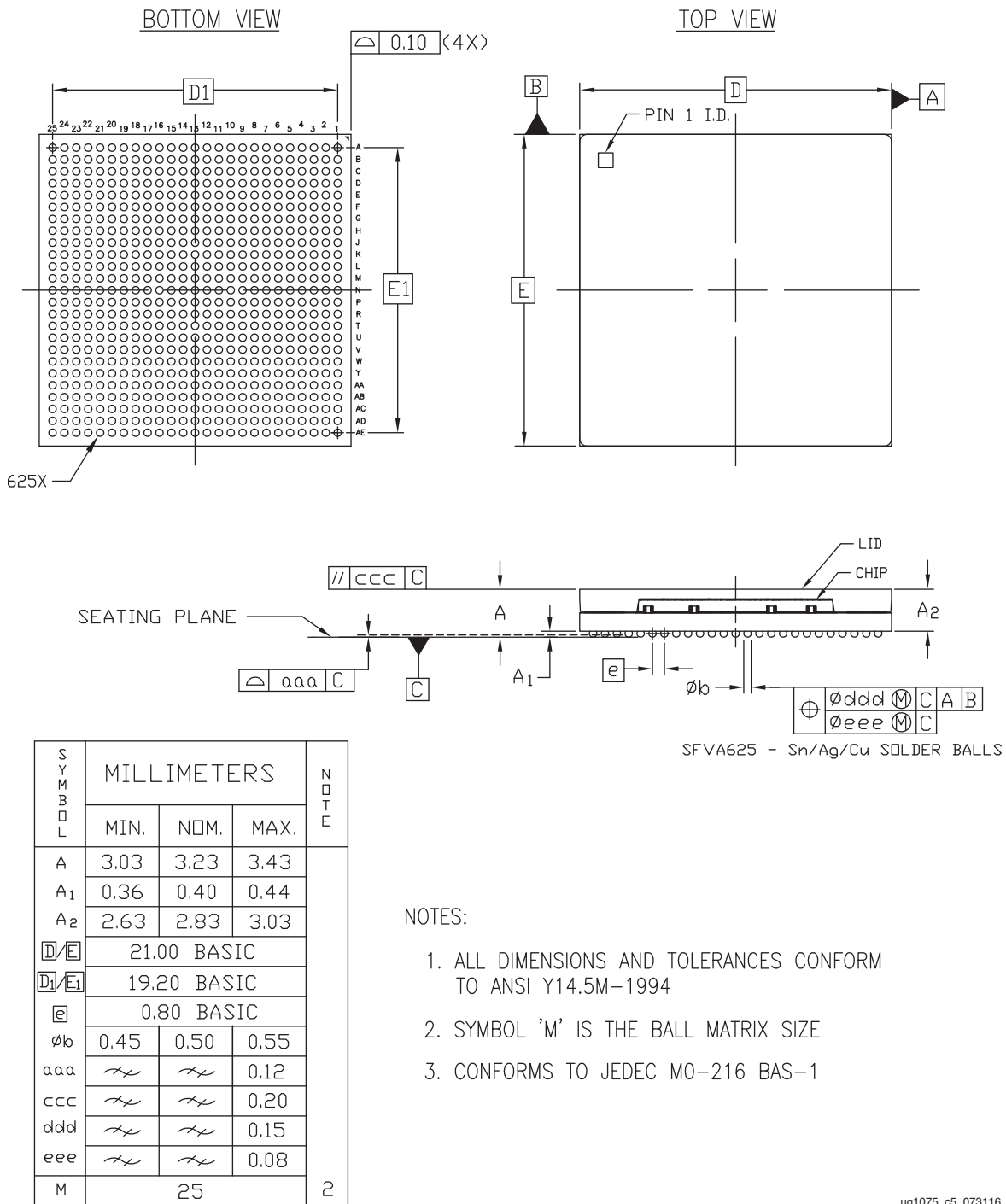


Figure 5-7: Package Dimensions for SFVA625 (XCZU2, XCZU3, XAZU2EG, and XAZU3EG)



# SFRC784 Ruggedized Flip-Chip, Super-Fine-Pitch, BGA (XQZU3EG and XQZU5EV)

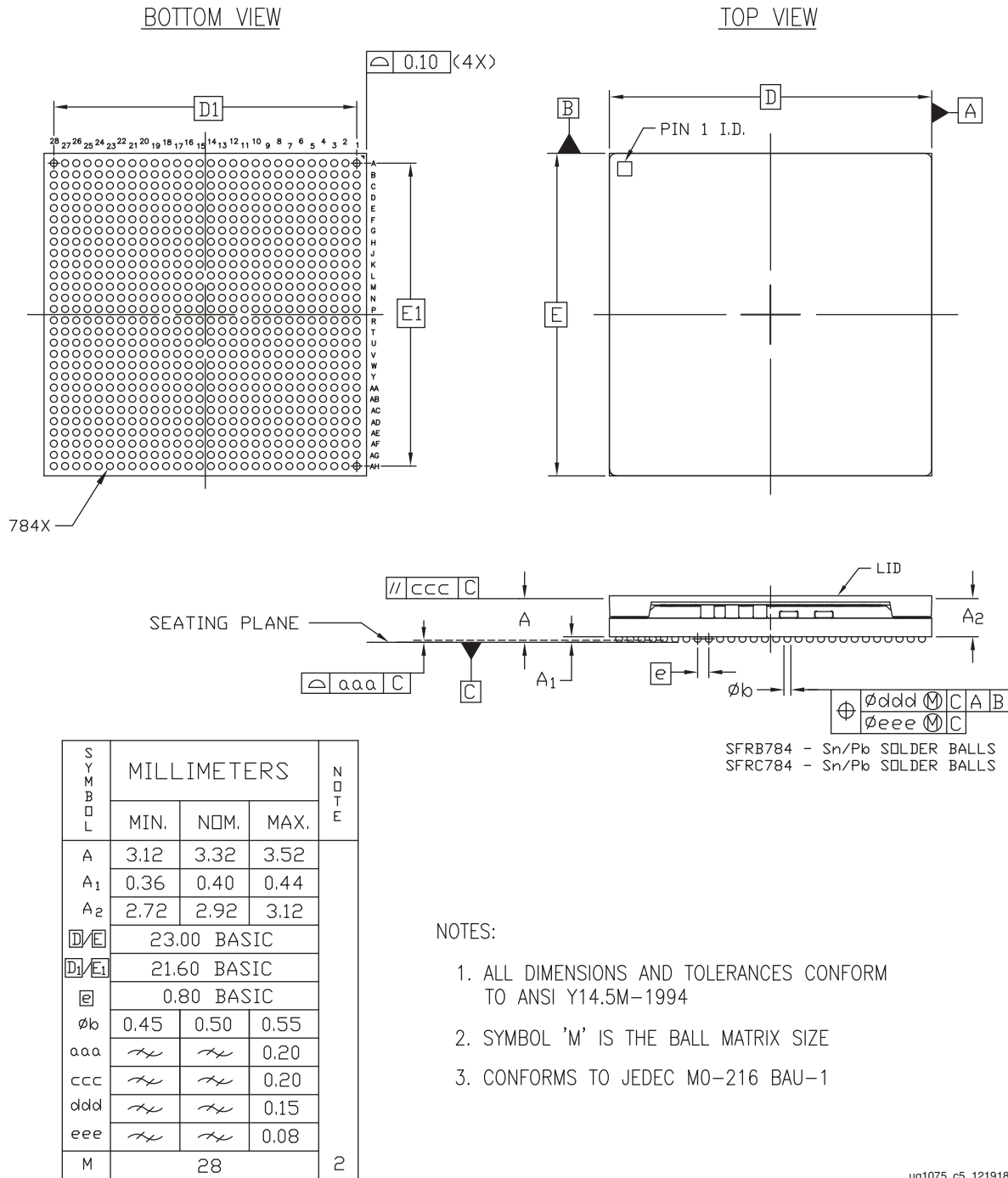
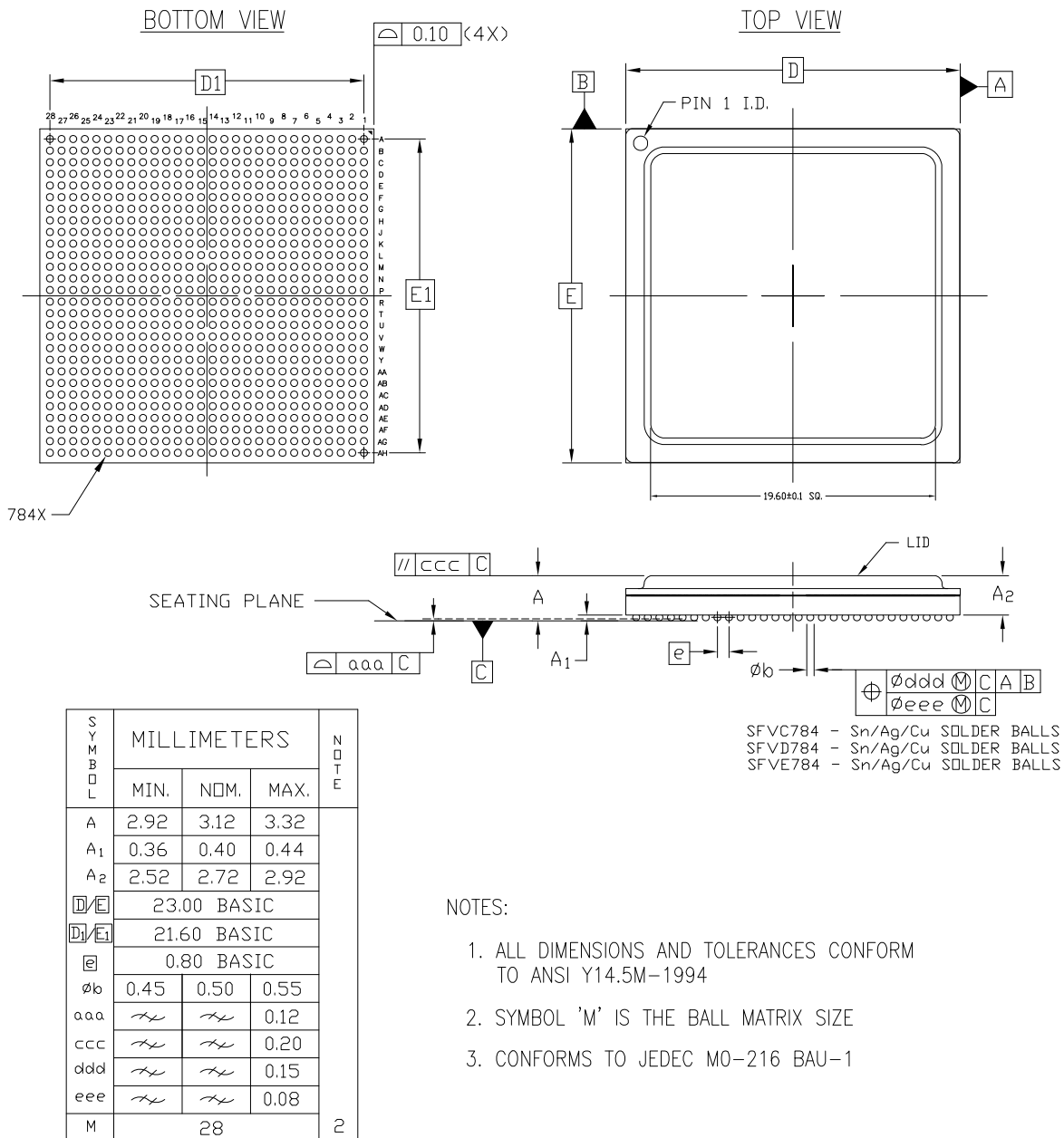


Figure 5-8: Package Dimensions for SFRC784 (XQZU3EG and XQZU5EV)

# SFVC784, SFVD784, and SFVE784, Flip-Chip, Super-Fine-Pitch BGA (XCZU1, XAZU1EG, XCZU2, XAZU2EG, XCZU3, XAZU3EG, XCZU3T, XCZU4, XAZU4EV, XCZU5, and XAZU5EV)



X29462-081924

Figure 5-9: Package Dimensions for SFVC784 (XCZU1, XAZU1EG, XCZU2, XAZU2EG, XCZU3, XAZU3EG, XCZU3T, XCZU4, XAZU4EV, XCZU5, and XAZU5EV)

# FBVB900 Flip-Chip, Fine-Pitch BGA (XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, and XCZU5EV)

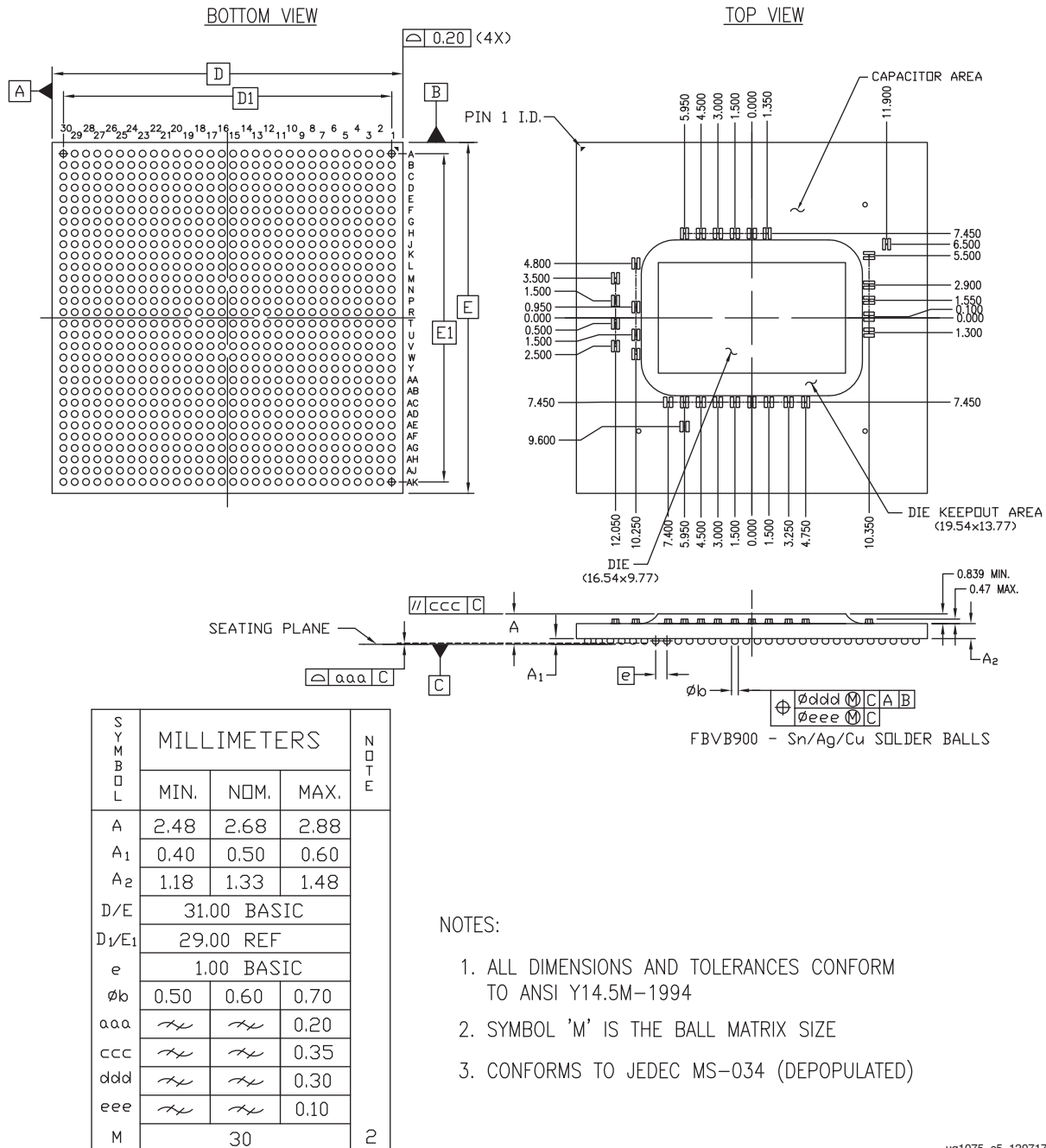


Figure 5-10: Package Dimensions for FBVB900 (XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, and XCZU5EV)

# FBVB900 Flip-Chip, Fine-Pitch BGA (XCZU7CG, XCZU7EG, XCZU7EV, and XAZU7EV)

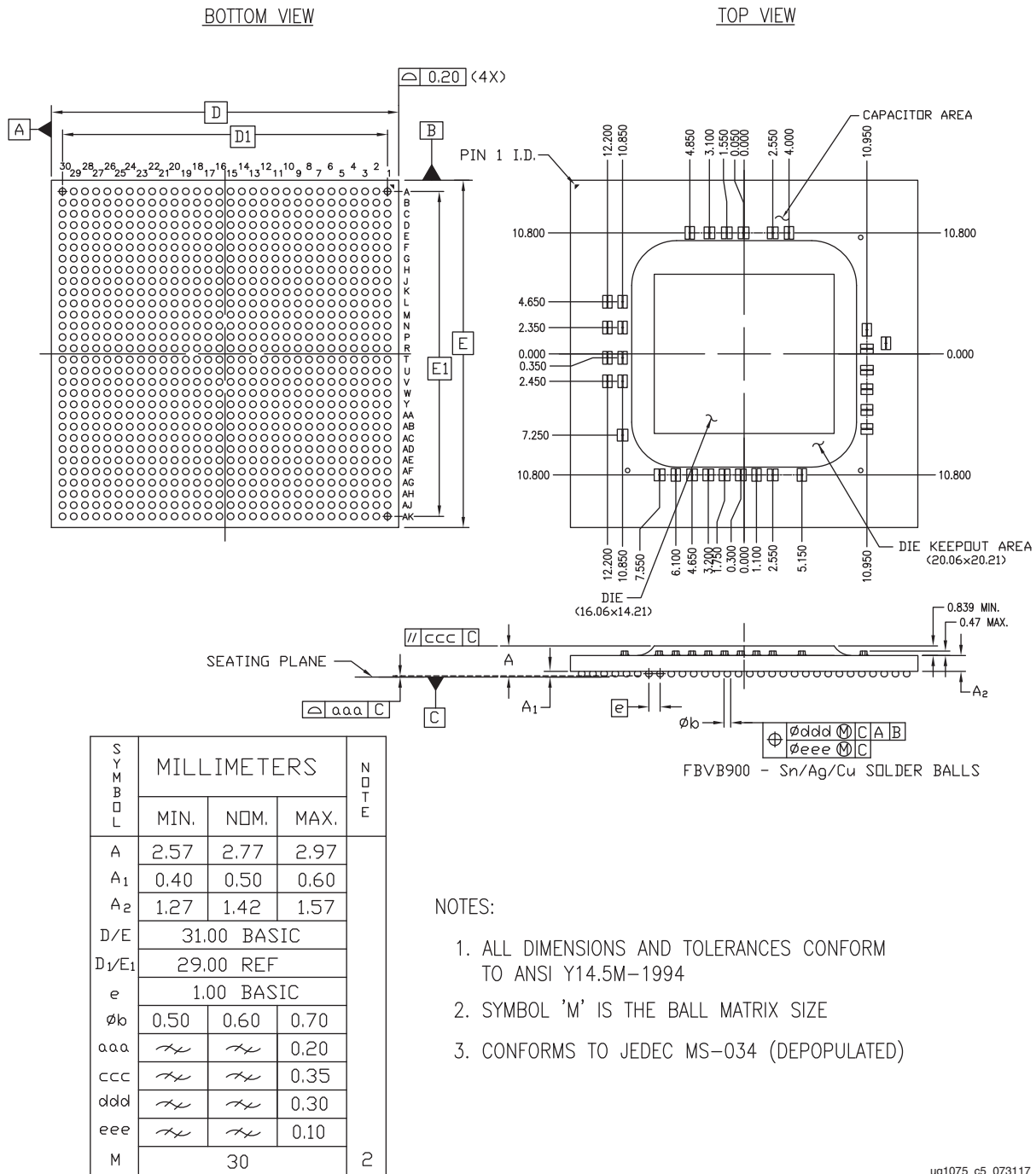


Figure 5-11: Package Dimensions for FBVB900 (XCZU7CG, XCZU7EG, XCZU7EV, and XAZU7EV)

# FFRB900 (XQZU7EV) Ruggedized Flip-Chip Fine-Pitch BGA

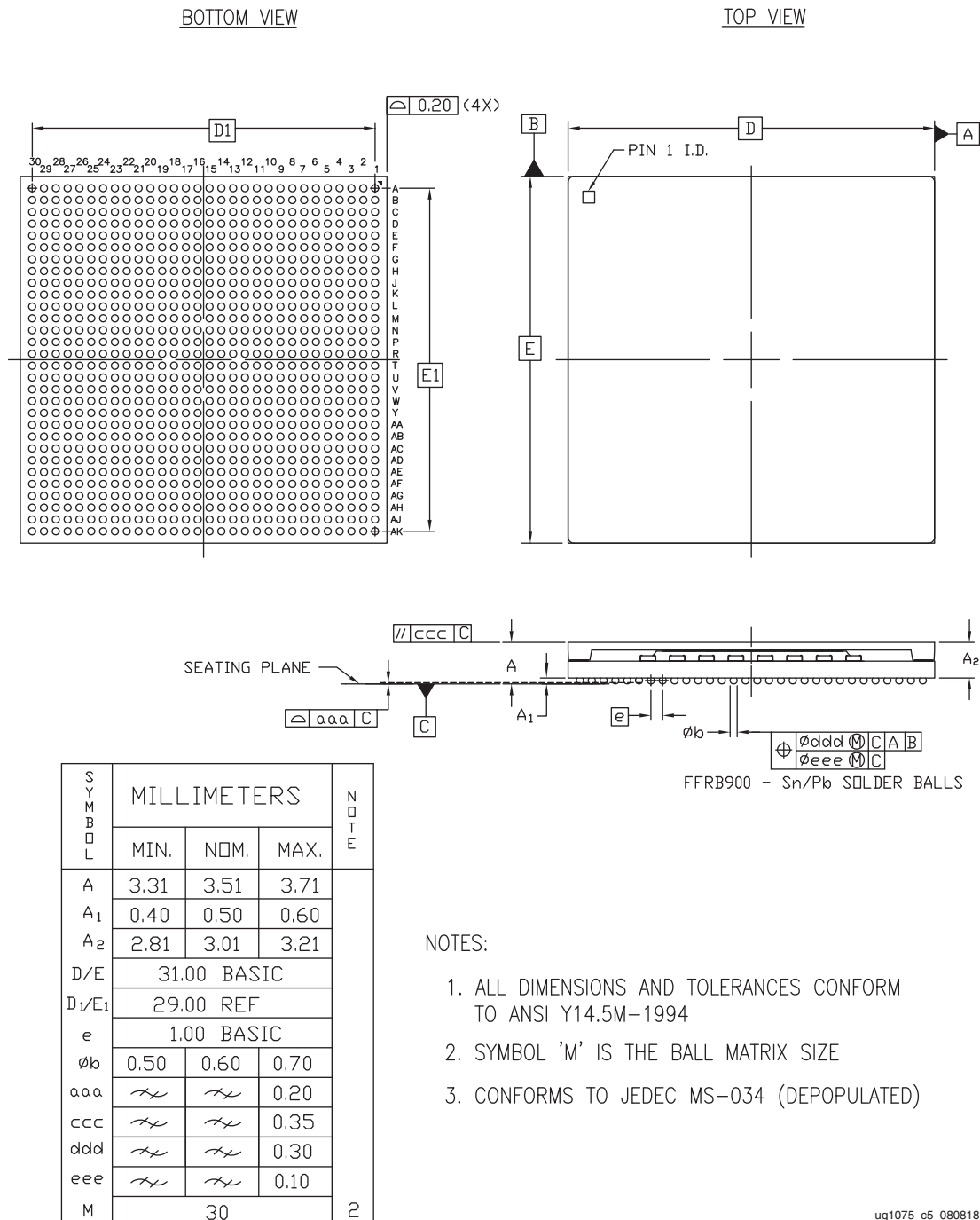
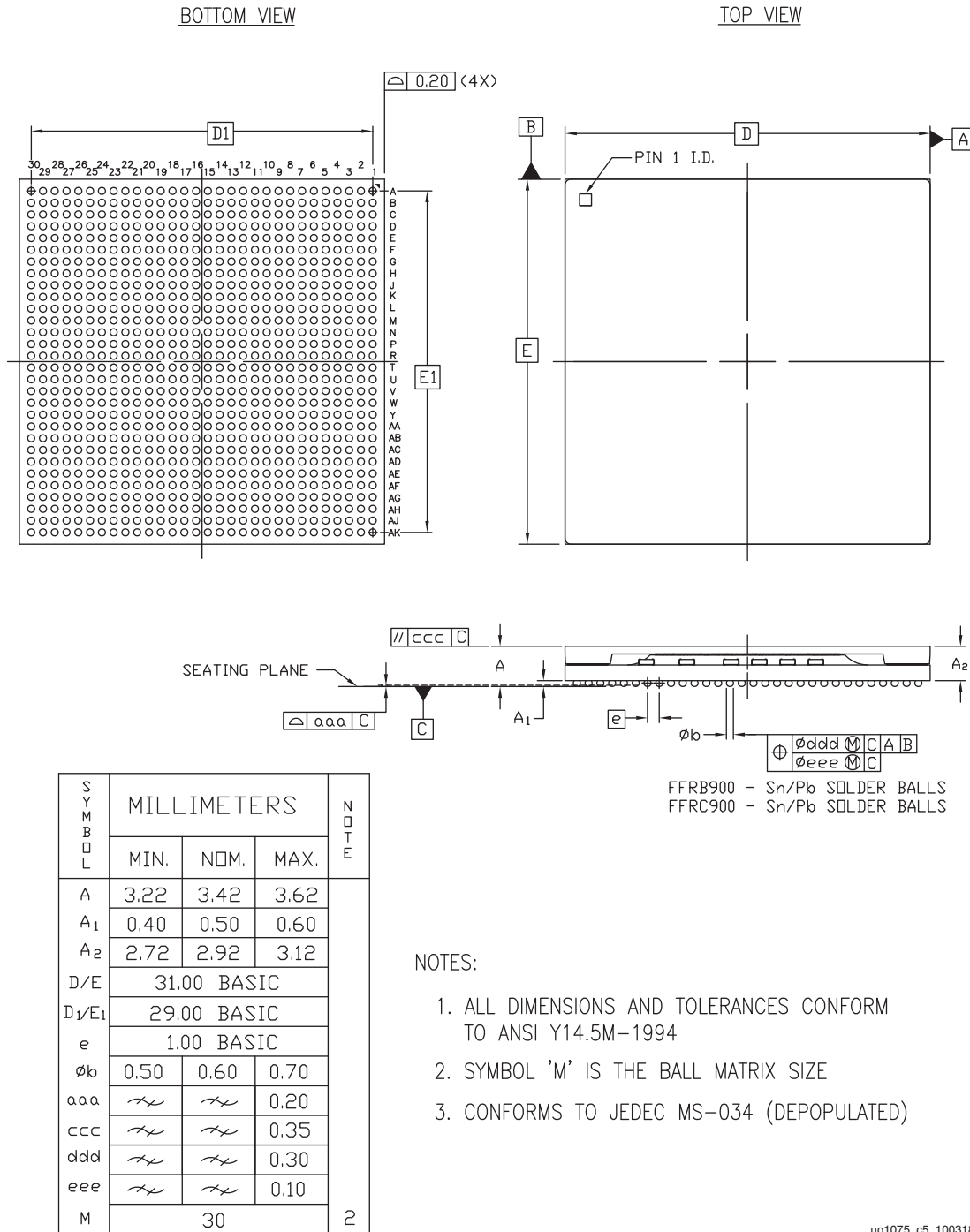


Figure 5-12: Package Dimensions for FFRB900 (XQZU7EV)

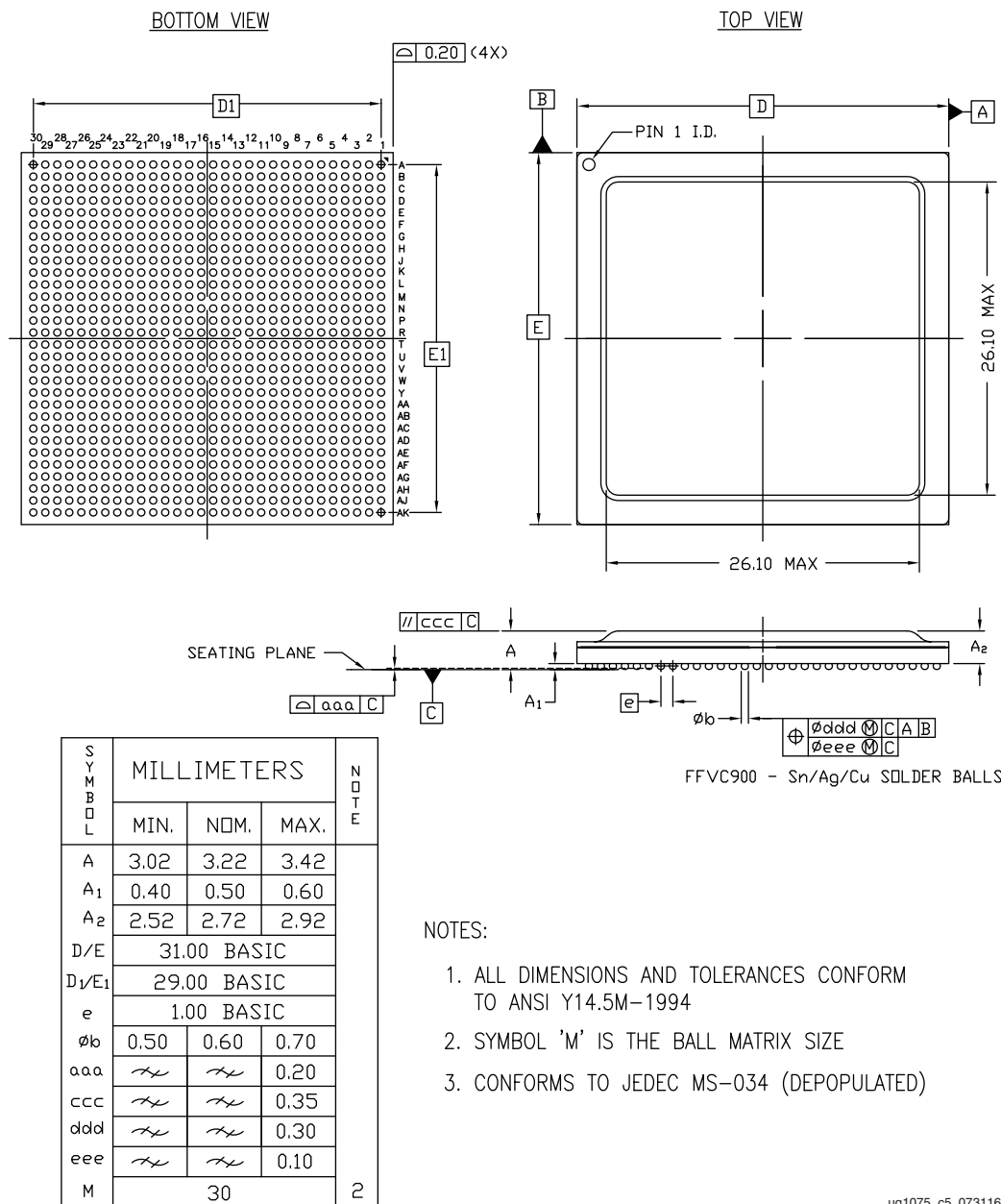
# FFRB900 (XQZU5EV) and FFRC900 (XQZU9EG and XQZU15EG) Ruggedized Flip-Chip Fine-Pitch BGA



ug1075\_c5\_100318

Figure 5-13: Package Dimensions for FFRB900 (XQZU5EV) and FFRC900 (XQZU9EG and XQZU15EG)

# FFVC900 Flip-Chip, Fine-Pitch BGA (XCZU6CG, XCZU6EG, XCZU9CG, XCZU9EG, and XCZU15EG)



ug1075\_c5\_073116

Figure 5-14: Package Dimensions for FFVC900 (XCZU6CG, XCZU6EG, XCZU9CG, XCZU9EG, and XCZU15EG)

# FFRB1156 Ruggedized Flip-Chip, Fine-Pitch, BGA (XQZU9EG and XQZU15EG)

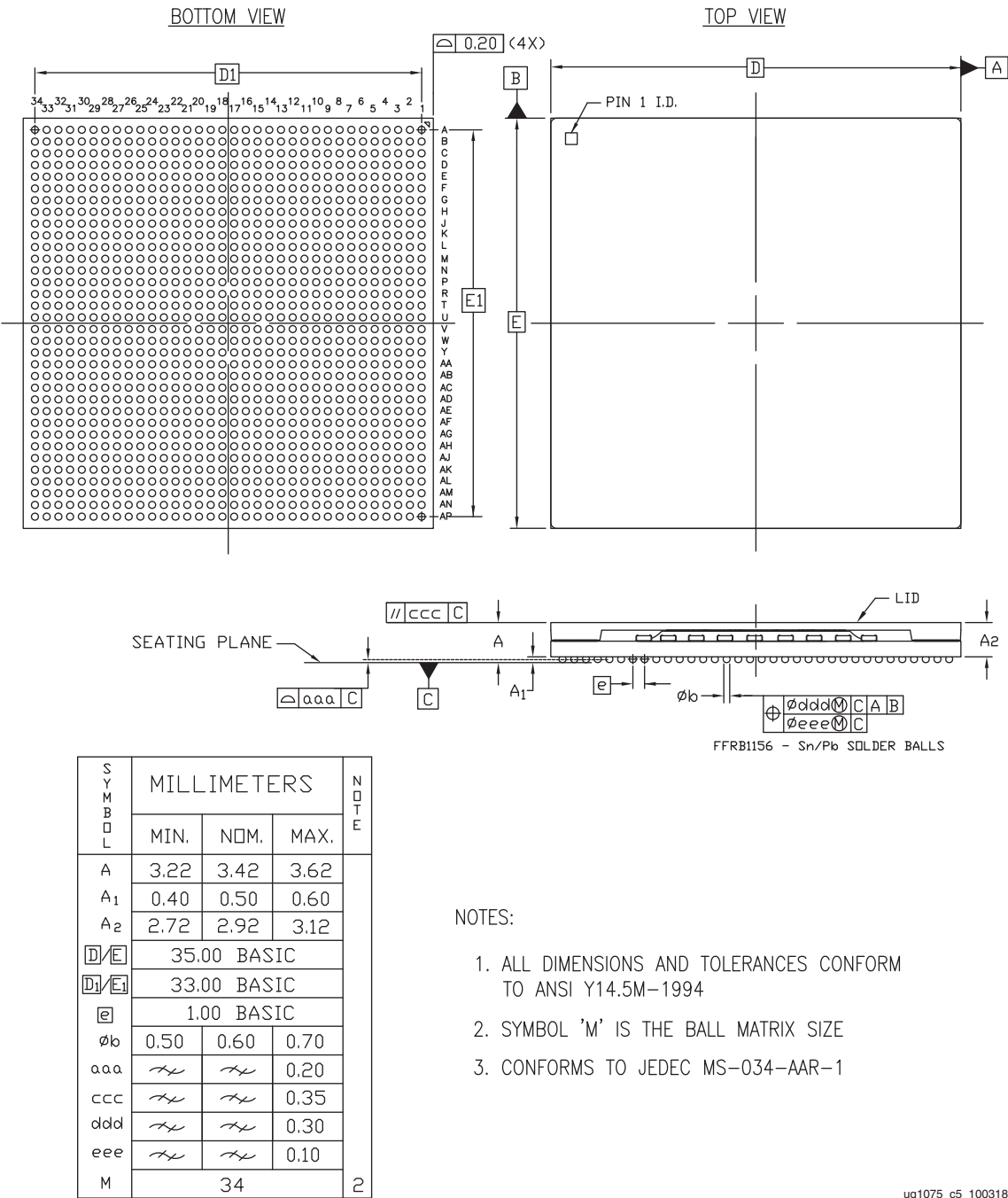


Figure 5-15: Package Dimensions for FFRB1156 (XQZU9EG and XQZU15EG)



# FFVB1156 Flip-Chip, Fine-Pitch BGA (XCZU6CG, XCZU6EG, XCZU9CG, XCZU9EG, and XCZU15EG)

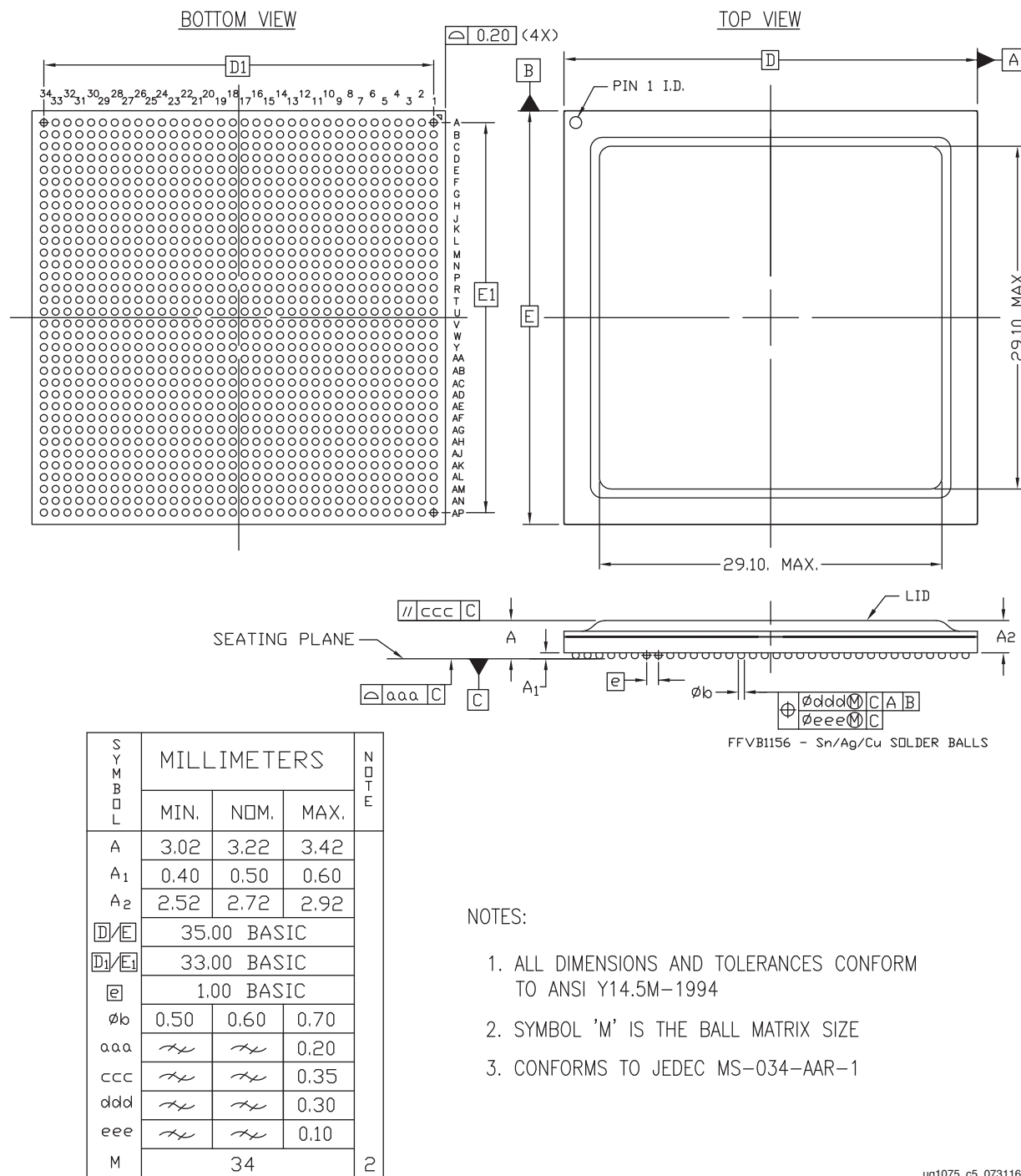


Figure 5-16: Package Dimensions for FFVB1156 (XCZU6CG, XCZU6EG, XCZU9CG, XCZU9EG, and XCZU15EG)

# FFRC1156 Ruggedized Flip-Chip Fine-Pitch BGA (XQZU7EV and XQZU11EG)

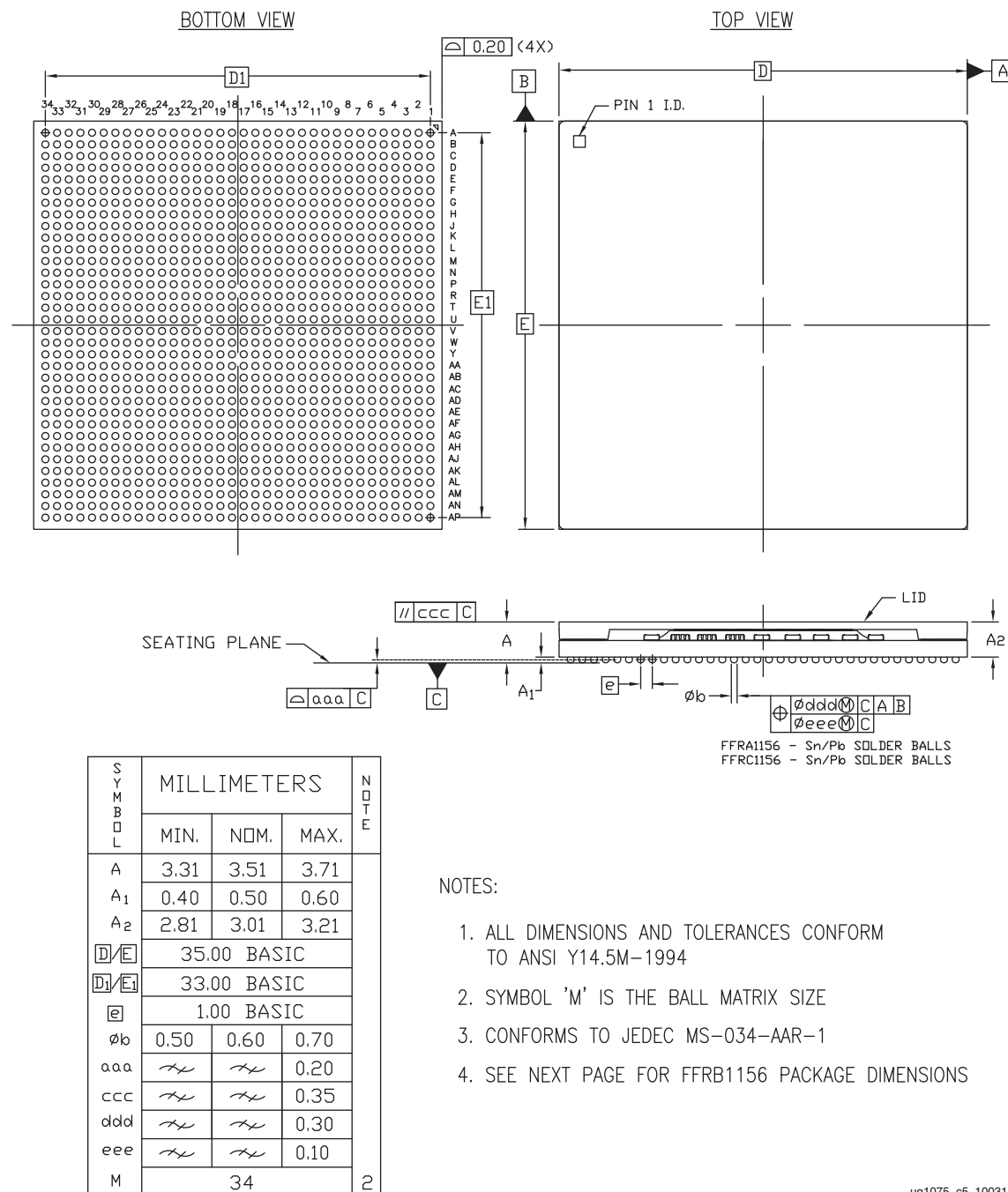
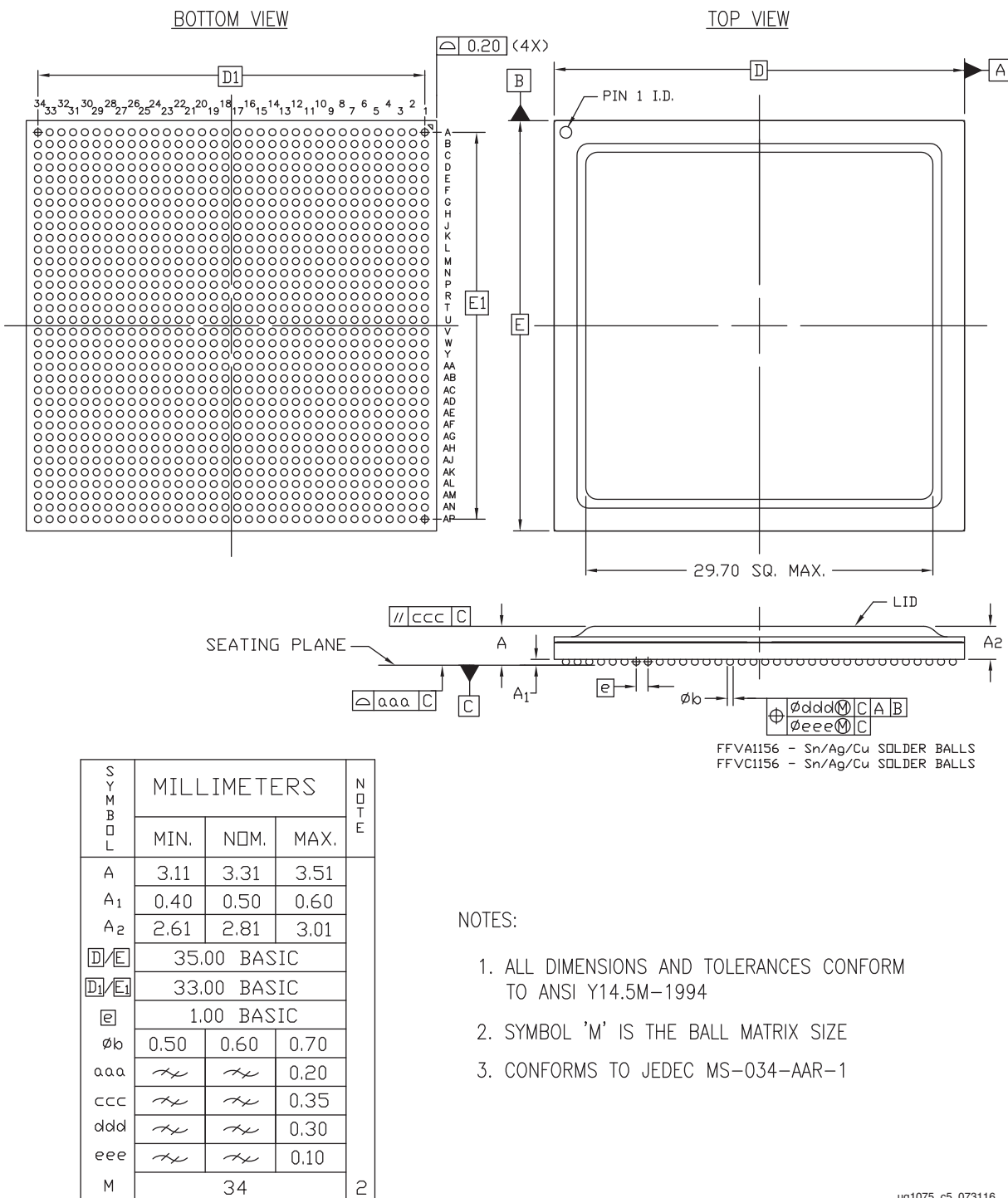


Figure 5-17: Package Dimensions for FFRC1156 (XQZU7EV and XQZU11EG)

# FFVC1156 Flip-Chip, Fine-Pitch BGA (XCZU7CG, XCZU7EG, XCZU7EV, and XCZU11EG)



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Figure 5-18: Package Dimensions for FFVC1156 (XCZU7CG, XCZU7EG, XCZU7EV, and XCZU11EG)

FFRD1156 (XQZU21DR) Ruggedized Flip-Chip  
Fine-Pitch BGA

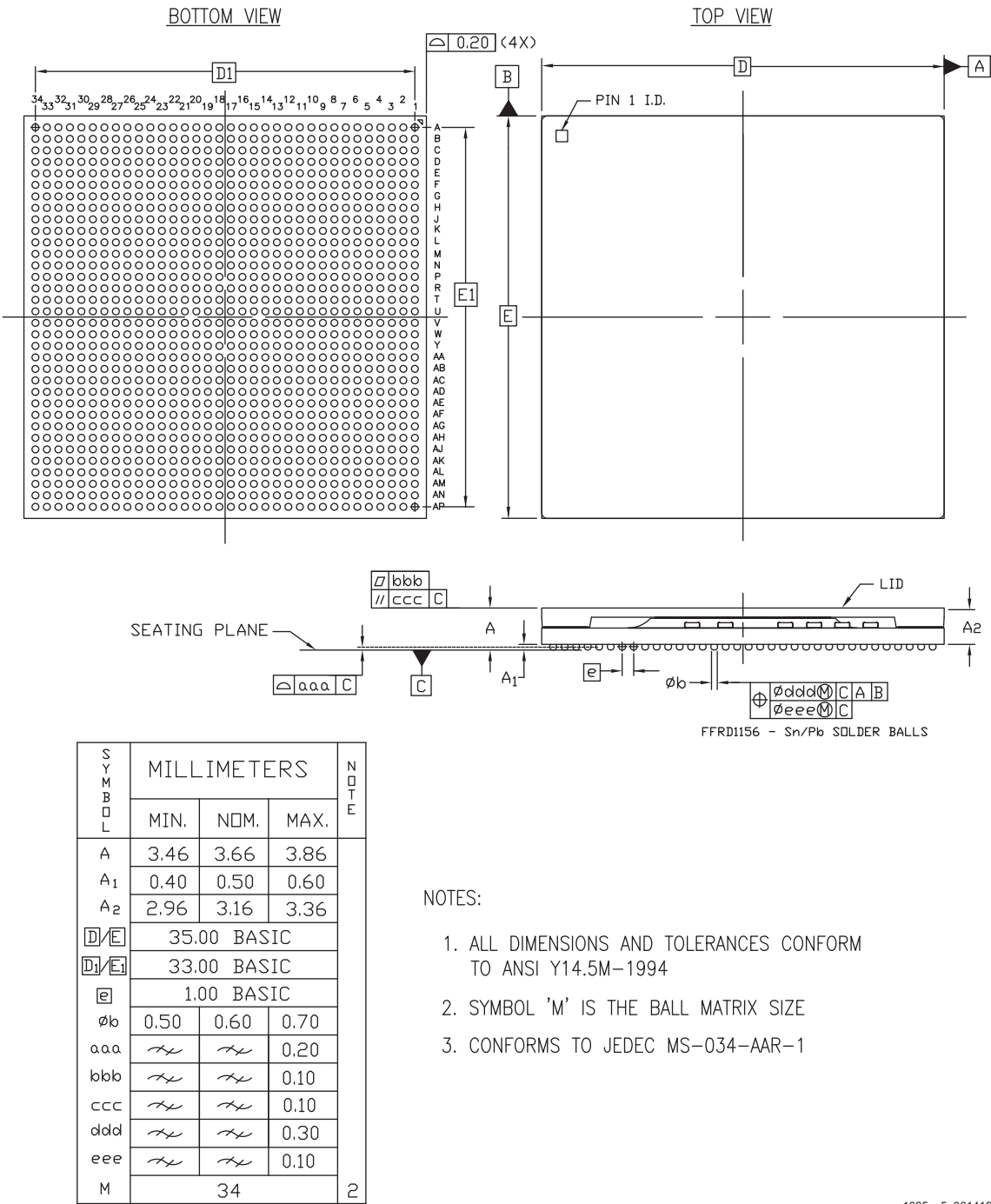


Figure 5-19: Package Dimensions for FFRD1156 (XQZU21DR)

# FFRE1156 (XQZU28DR, XQZU48DR) Ruggedized Flip-Chip Fine-Pitch BGA

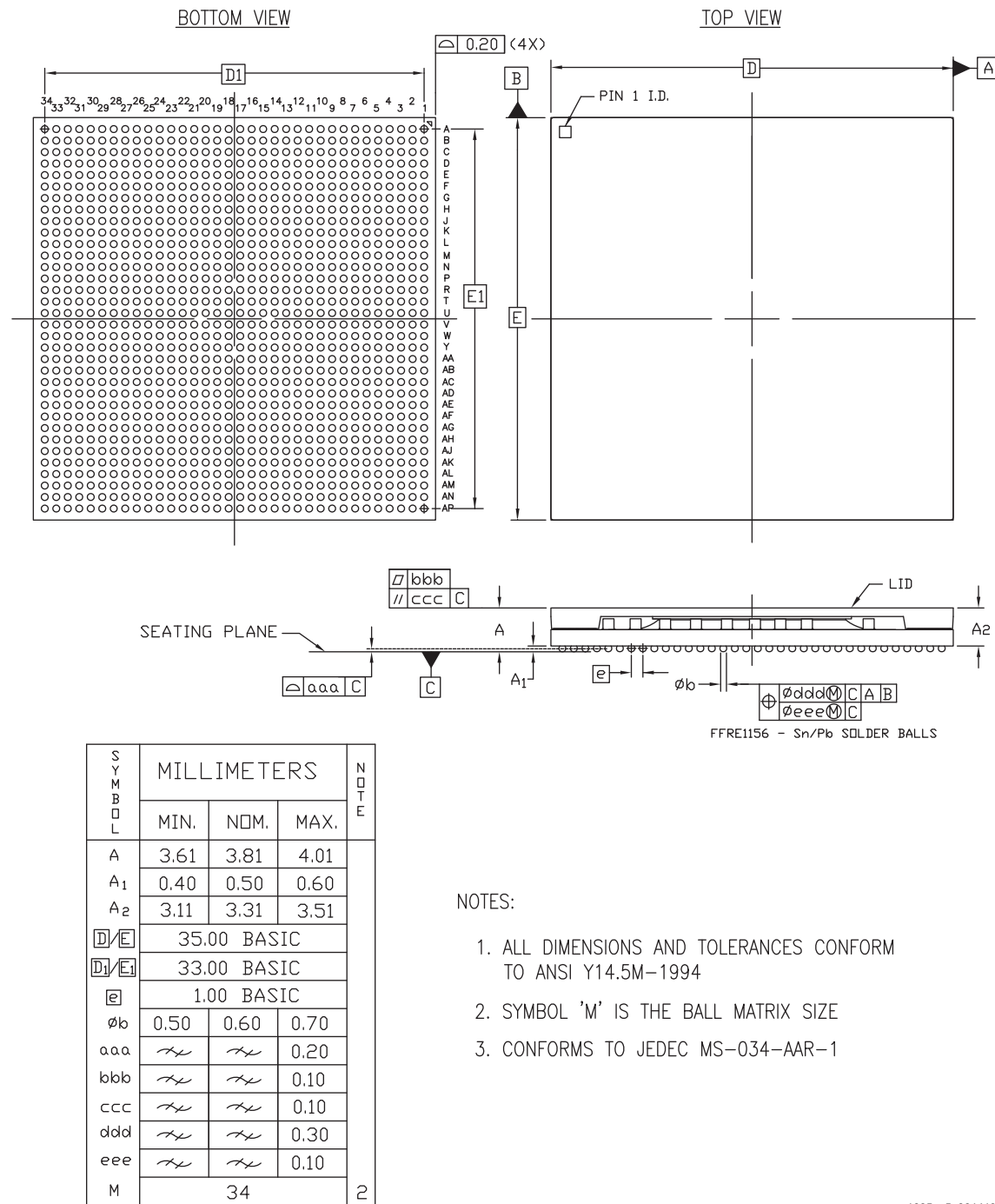


Figure 5-20: Package Dimensions for FFRE1156 (XQZU28DR and XQZU48DR)

**FFVD1156 (XCZU21DR) and FFVE1156 (XCZU25DR, XCZU27DR, XCZU42DR, XCZU48DR, XCZU63DR, XCZU64DR, XCZU65DR, XCZU67DR) Flip-Chip, Fine-Pitch BGA**

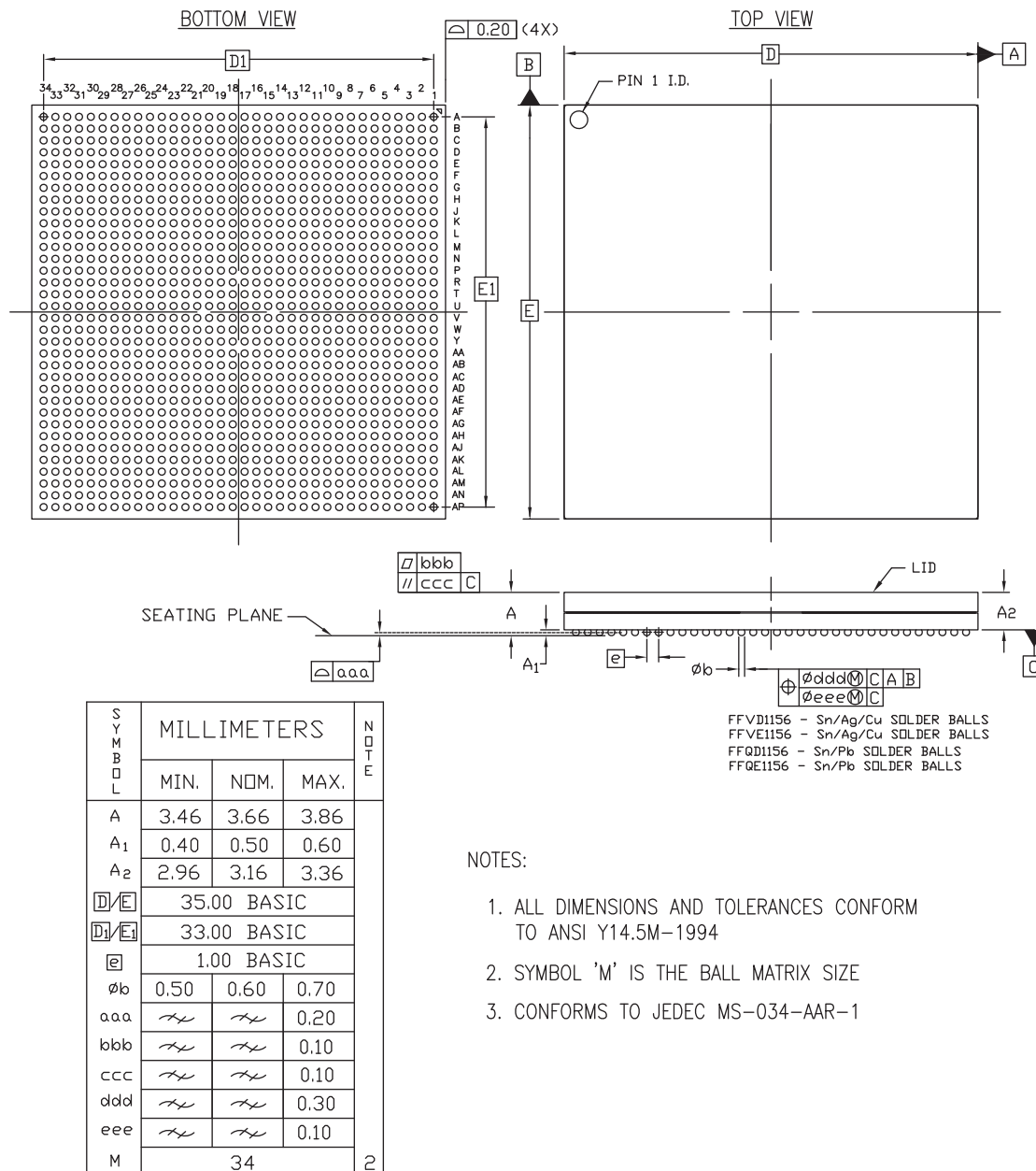


**Figure 5-21: Package Dimensions for FFVE1156 (XCZU21DR) and FFVE1156 (XCZU25DR, XCZU27DR, XCZU28DR, XCZU42DR, XCZU43DR, XCZU47DR, XCZU48DR, XCZU63DR, XCZU64DR, XCZU65DR, XCZU67DR)**

# FSVE1156 (XCZU25DR, XCZU27DR, XCZU28DR, XCZU43DR, XCZU47DR, XCZU48DR) Flip-Chip, Fine-Pitch, Lidless w/Stiffener Ring BGA

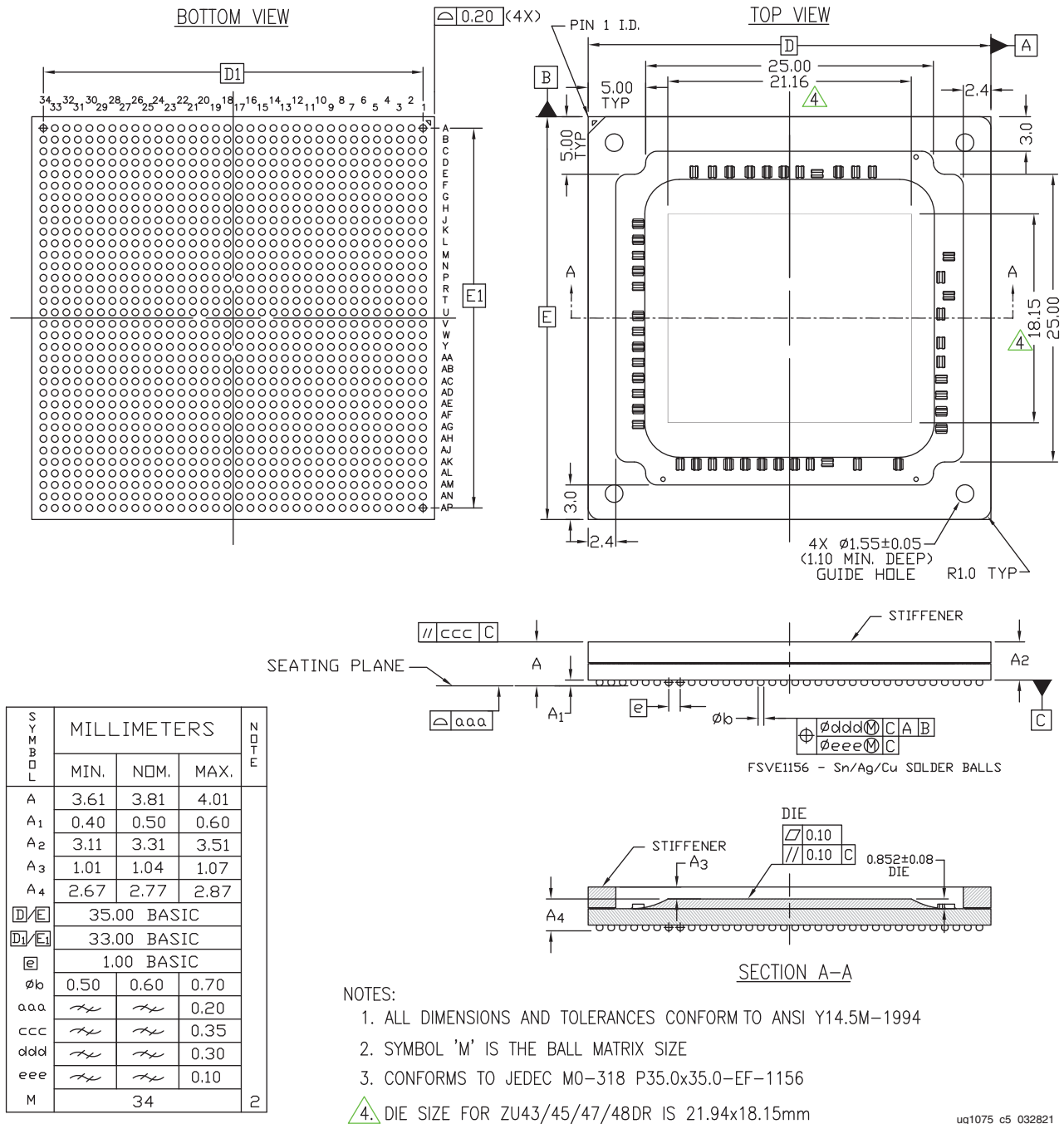


Figure 5-22: Package Dimensions for FSVE1156 (XCZU25DR, XCZU27DR, XCZU28DR, XCZU43DR, XCZU47DR, XCZU48DR)



# FSVE1156 (XCZU42DR, XCZU63DR, XCZU64DR, XCZU65DR, XCZU67DR) Flip-Chip, Fine-Pitch, Lidless w/Stiffener Ring BGA

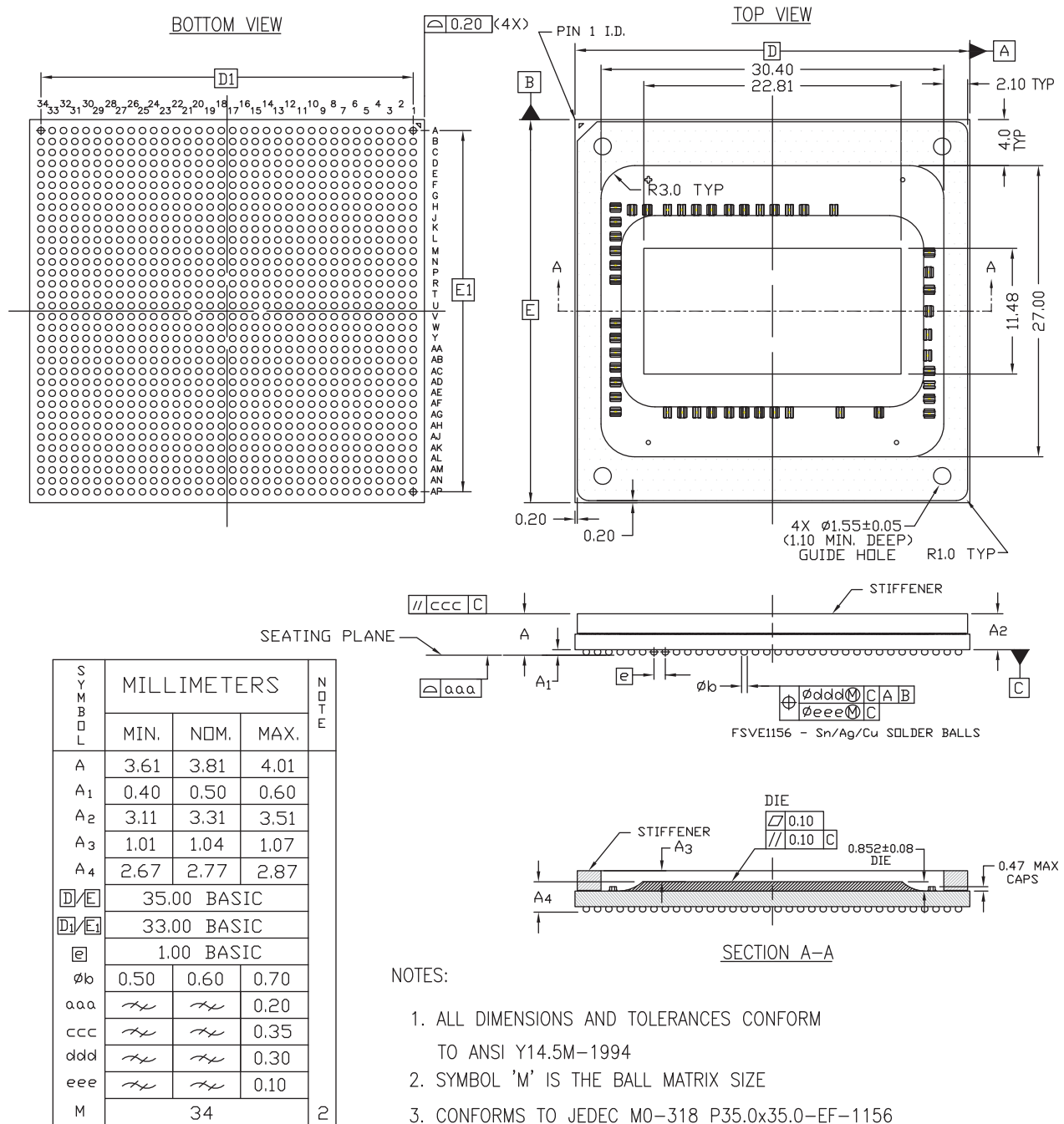


Figure 5-23: Package Dimensions for FSVE1156 (XCZU42DR, XCZU63DR, XCZU64DR, XCZU65DR, XCZU67DR)



# FFRB1517 (XQZU19EG) Ruggedized Flip-Chip Fine-Pitch BGA

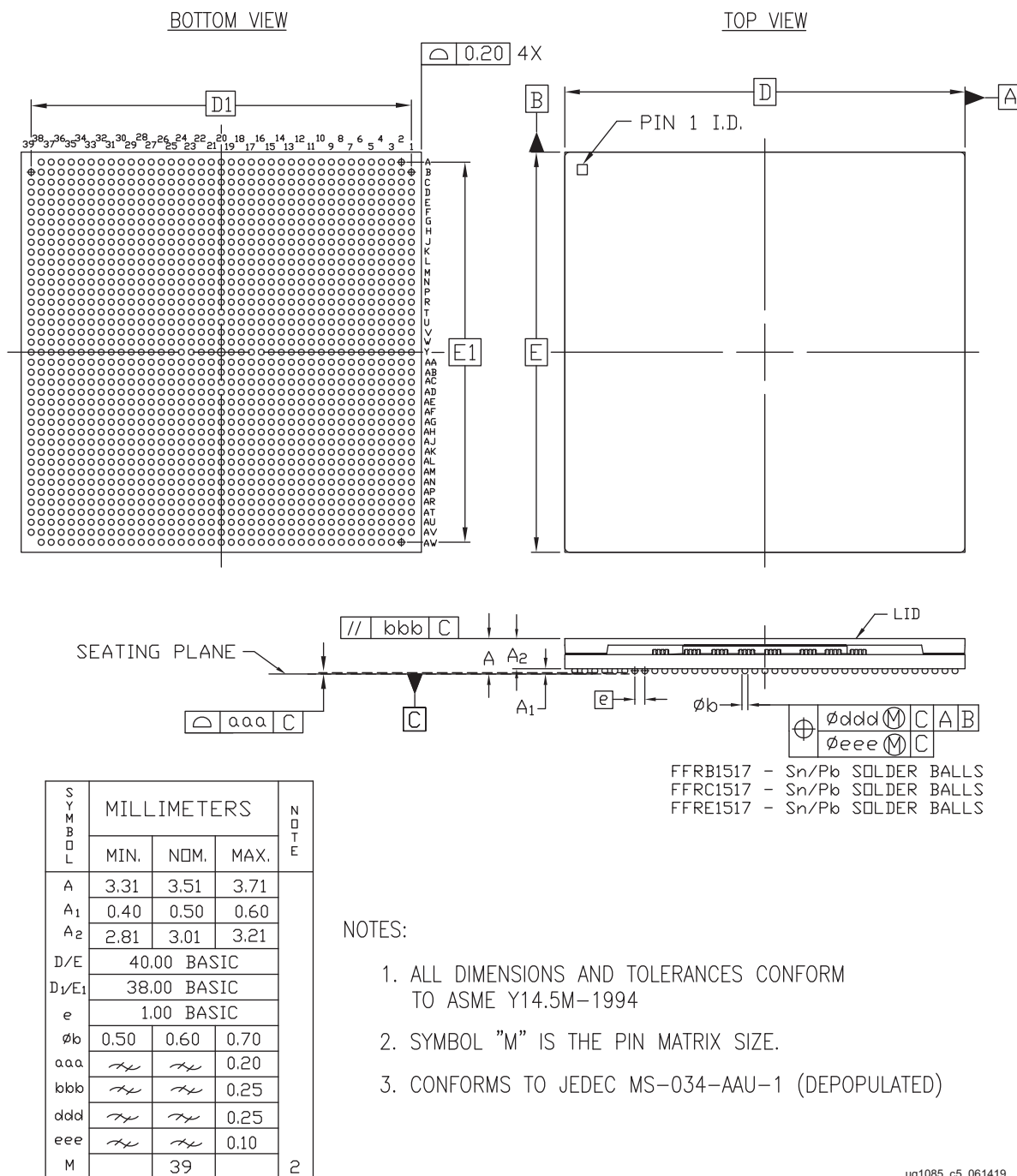


Figure 5-24: Package Dimensions for FFRB1517 (XQZU19EG)

# FFVB1517 (XCZU11EG, XCZU17EG, and XCZU19EG) and FFVF1517 (XCZU7CG, XCZU7EG, XCZU7EV, XCZU11EG, and XAZU11EG) Flip-Chip, Fine-Pitch BGA

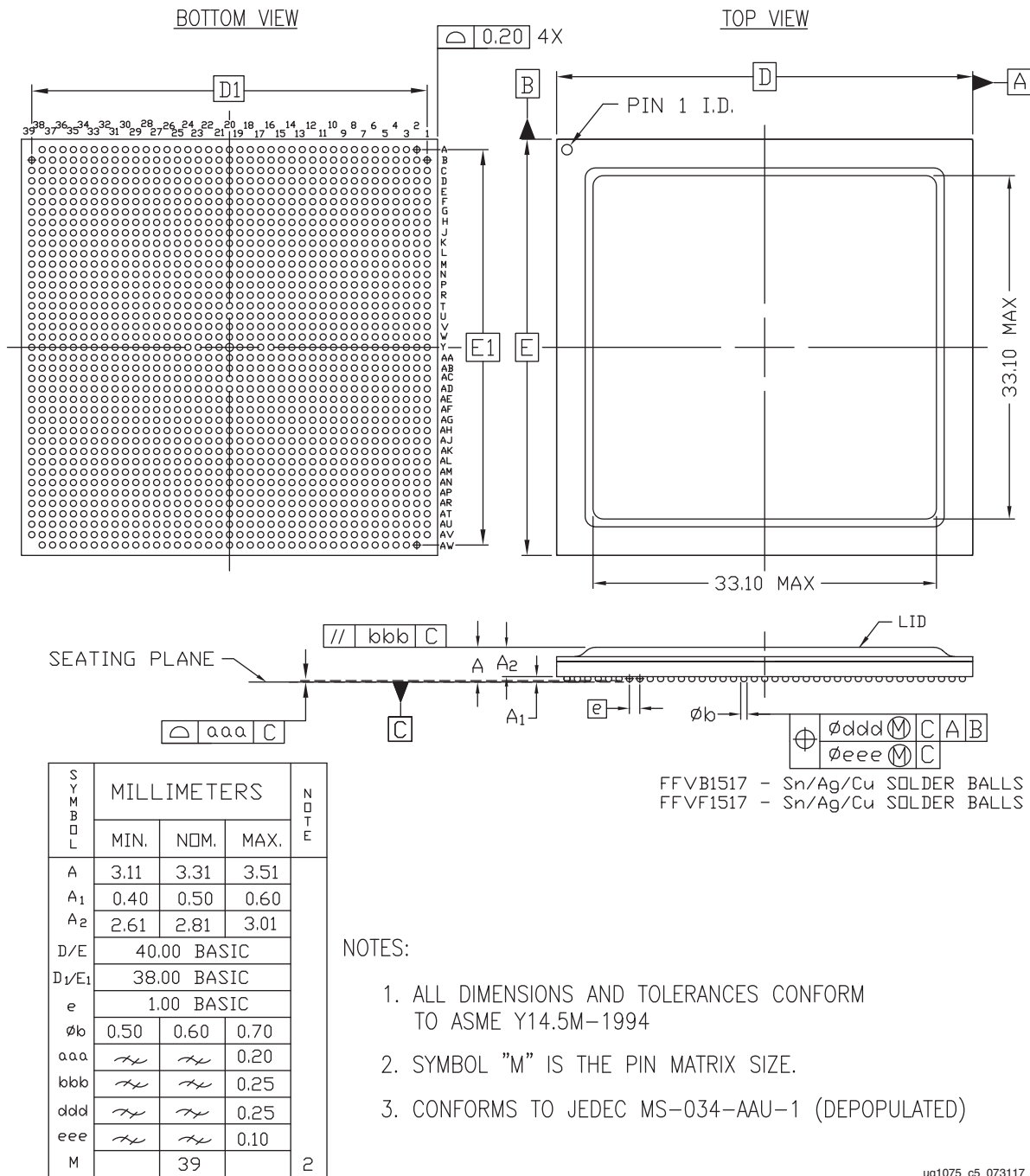


Figure 5-25: Package Dimensions for FFVB1517 (XCZU11EG, XCZU17EG, and XCZU19EG) and FFVF1517 (XCZU7CG, XCZU7EG, XCZU7EV, XCZU11EG, and XAZU11EG)

# FFRG1517 (XQZU28DR) Ruggedized Flip-Chip Fine-Pitch BGA

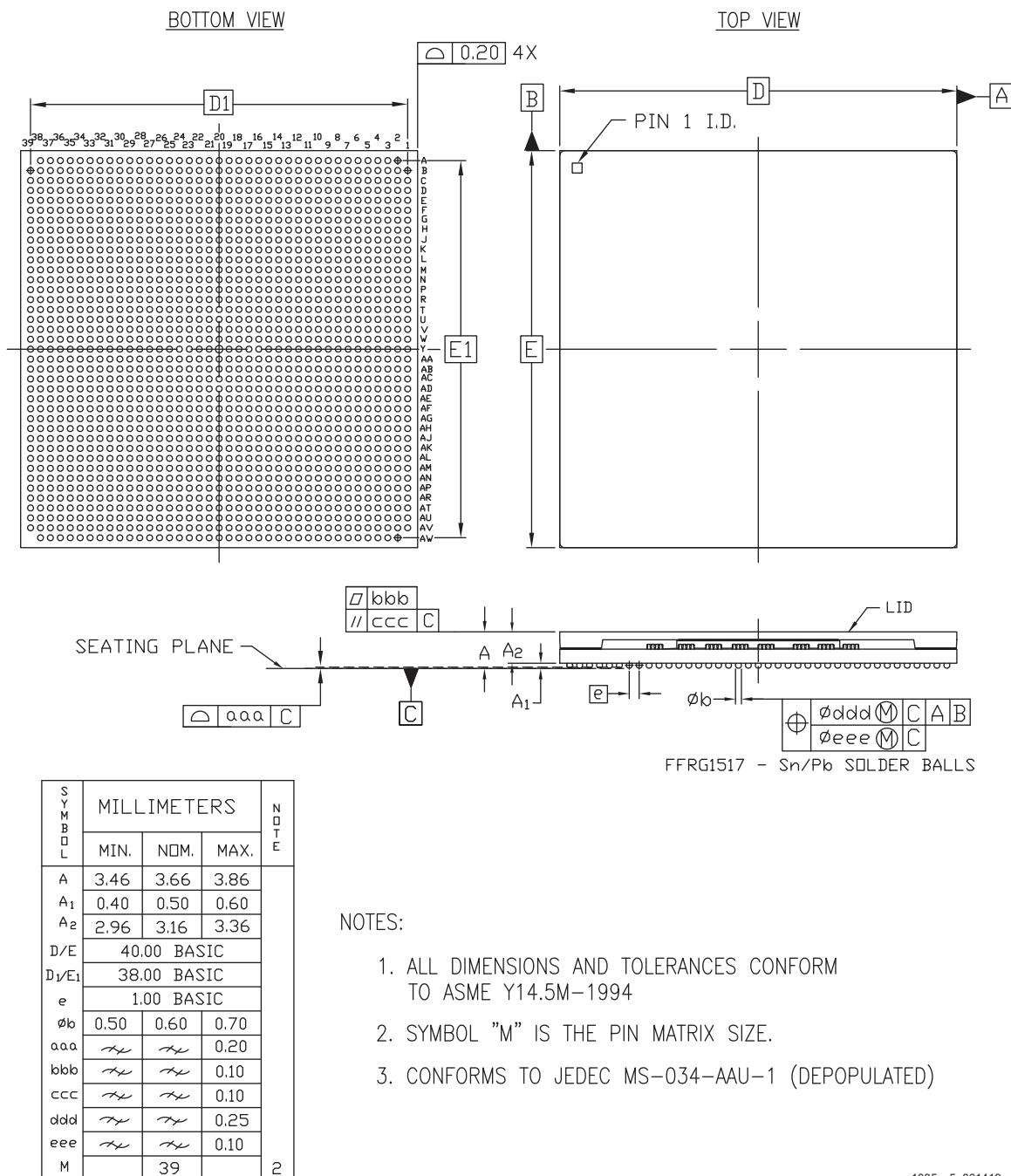


Figure 5-26: Package Dimensions for FFRG1517 (XQZU28DR)

# FFVG1517 (XCZU25DR, XCZU27DR, XCZU28DR, XCZU43DR, XCZU47DR, XCZU48DR) Flip-Chip, Fine-Pitch BGA

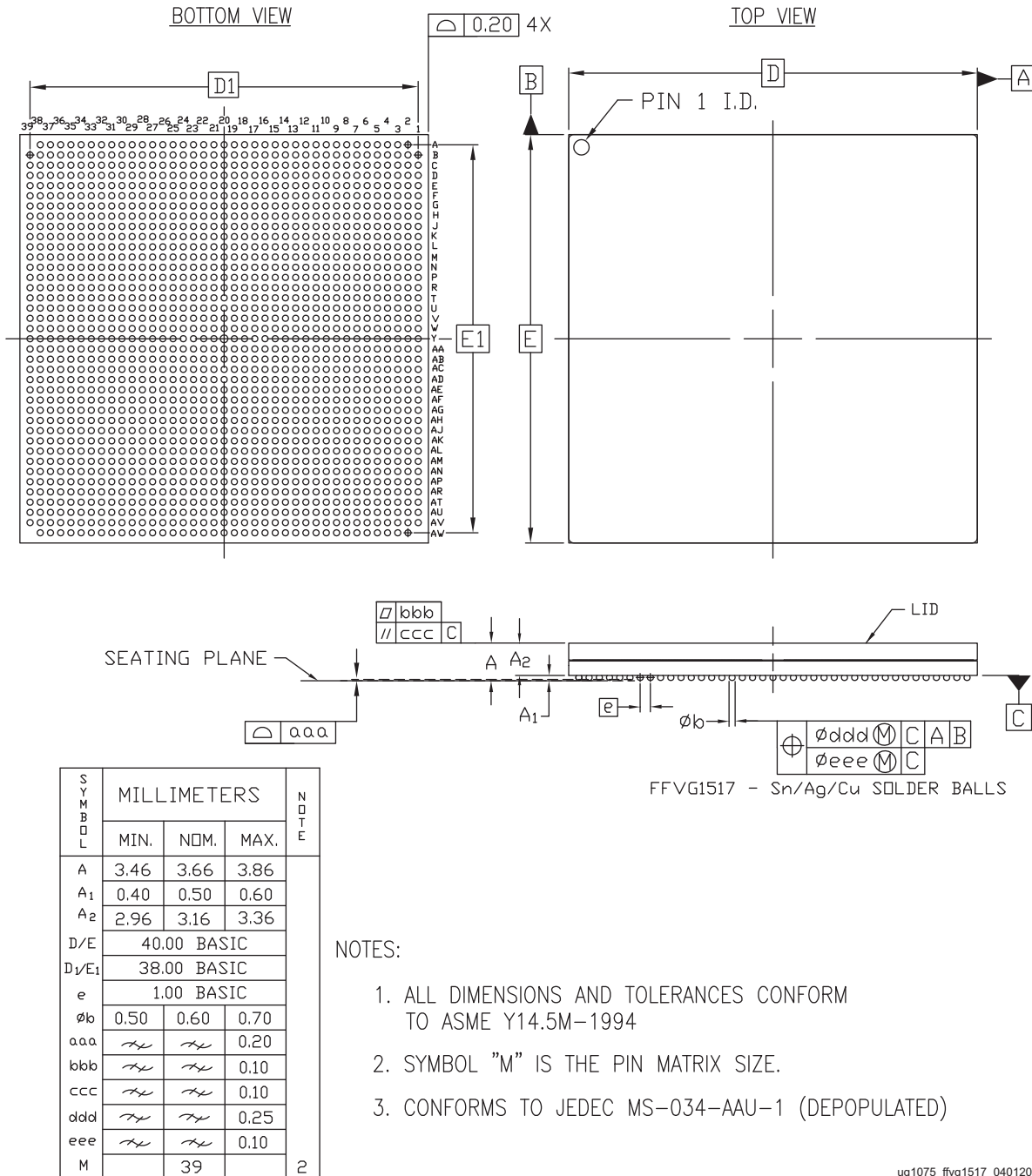


Figure 5-27: Package Dimensions for FFVG1517 (XCZU25DR, XCZU27DR, XCZU28DR, XCZU43DR, XCZU47DR, XCZU48DR)

# FSRG1517 (XQZU48DR) Ruggedized Flip Chip, Fine-Pitch, Lidless with Stiffener Ring BGA

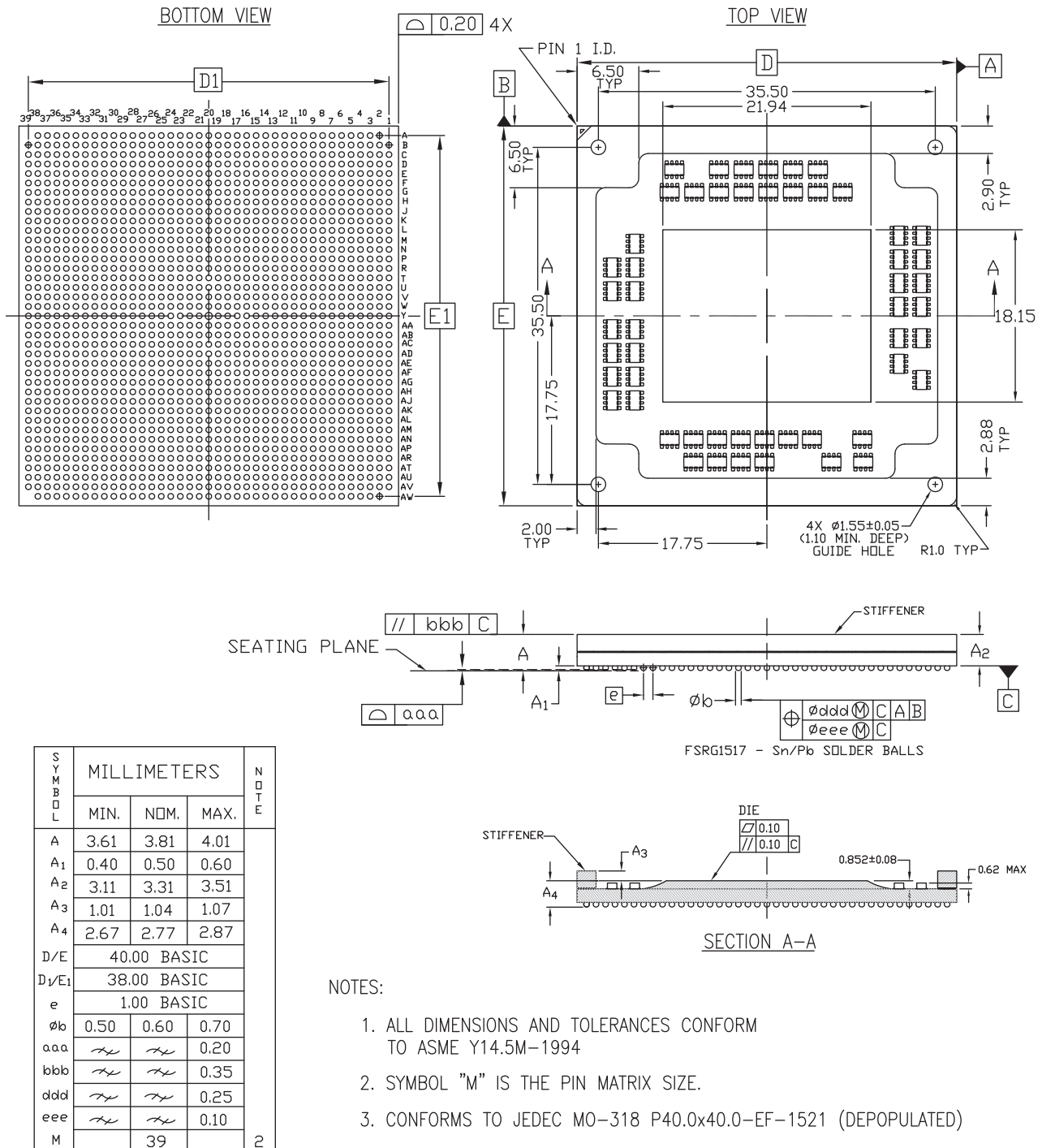


Figure 5-28: Package Dimensions for FSRG1517 (XQZU48DR)

**FSVG1517 (XCZU25DR, XCZU27DR, XCZU28DR, XCZU43DR, XCZU47DR, XCZU48DR) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring BGA**

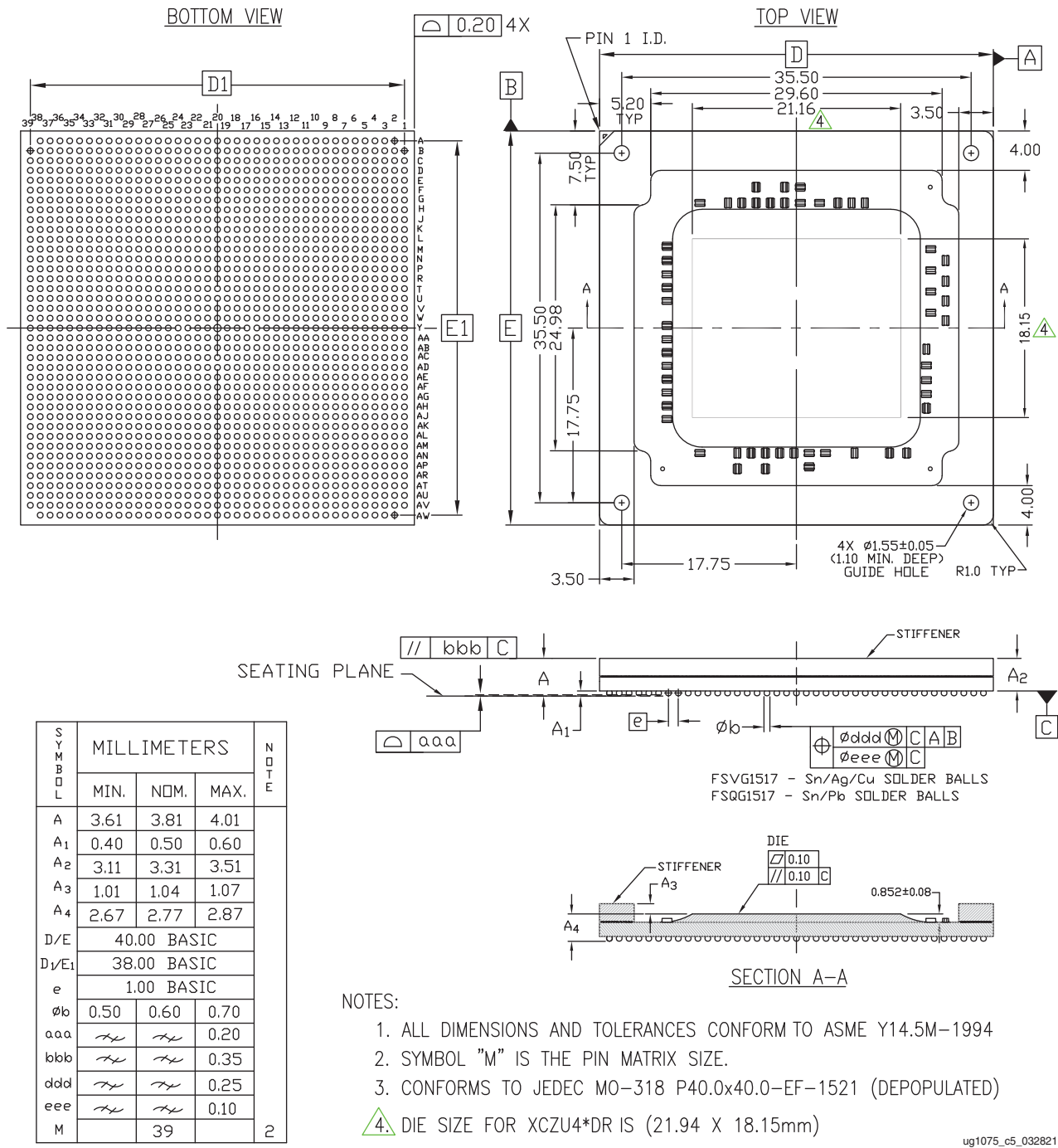
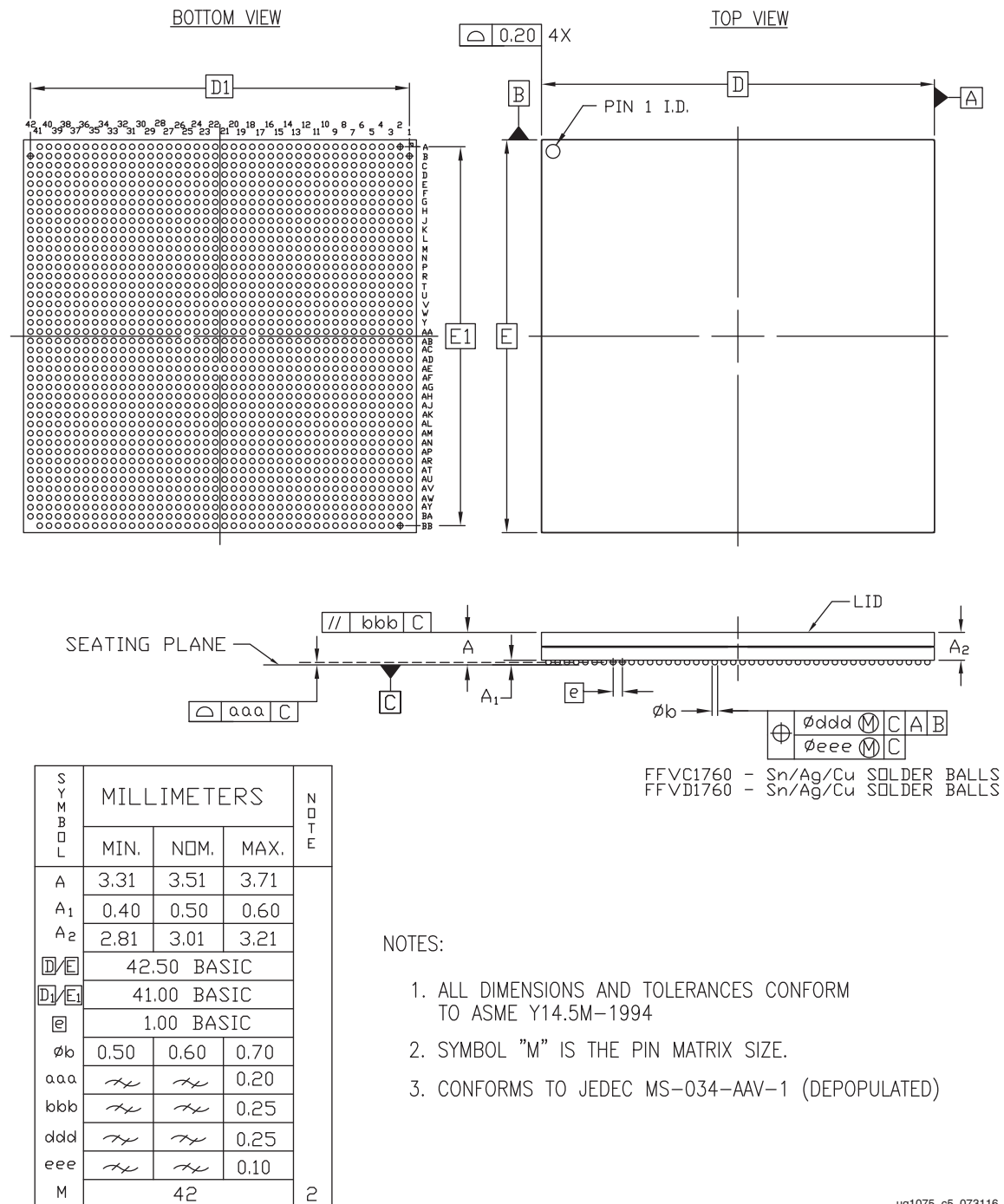


**Figure 5-29: Package Dimensions for FSVG1517 (XCZU25DR, XCZU27DR, XCZU28DR, XCZU43DR, XCZU47DR, XCZU48DR)**



# FFVC1760 and FFVD1760 Flip-Chip, Fine-Pitch BGA (XCZU11EG, XCZU17EG, and XCZU19EG)



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Figure 5-30: Package Dimensions for FFVC1760 and FFVD1760 (XCZU11EG, XCZU17EG, and XCZU19EG)

# FFRC1760 Ruggedized Flip-Chip BGA (XQZU11EG and XQZU19EG)

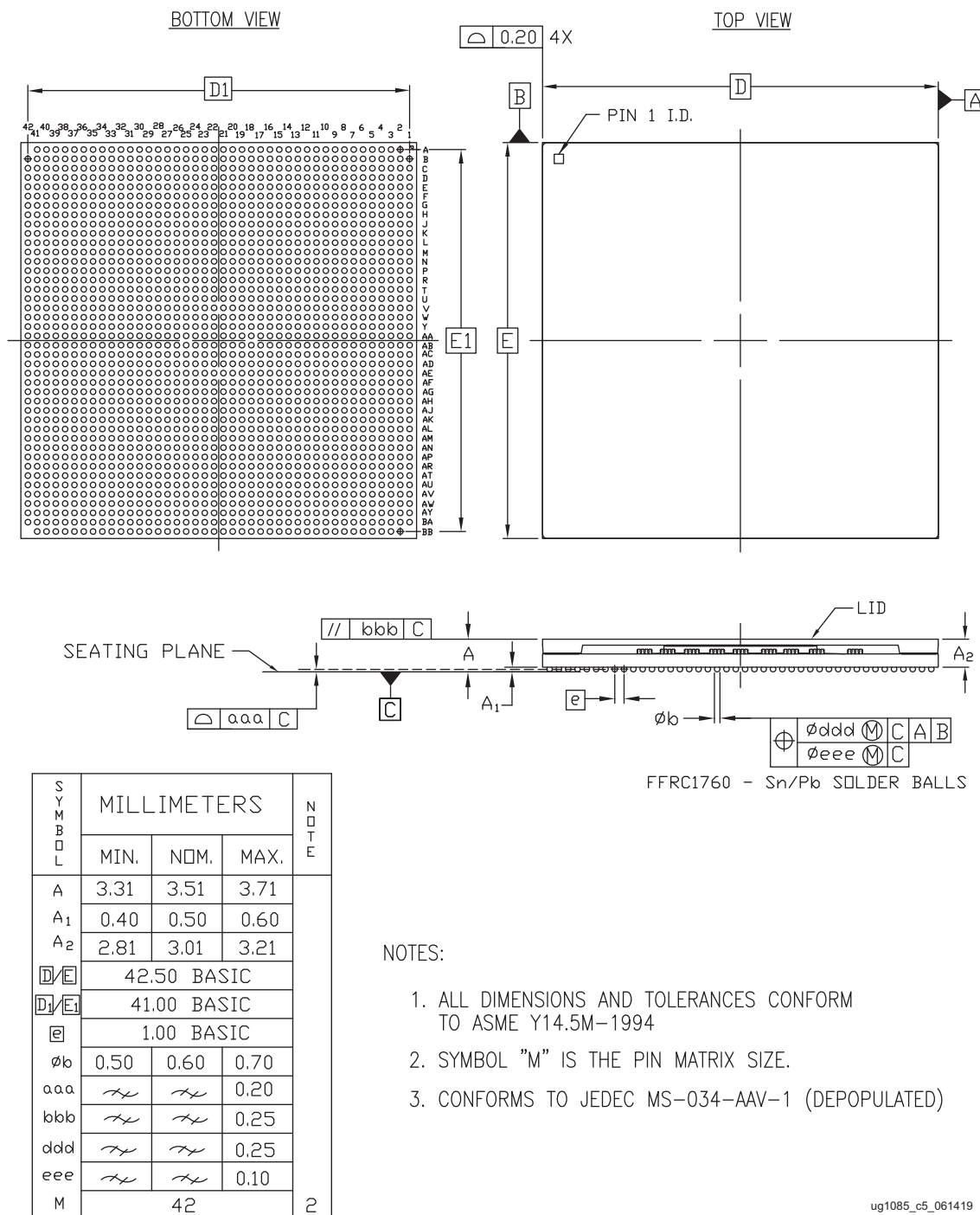


Figure 5-31: Package Dimensions for FFRC1760 (XQZU11EG and XQZU19EG)



# FFVF1760 (XCZU29DR, XCZU39DR, XCZU49DR) and FFVH1760 (XCZU46DR) Flip-Chip, Fine-Pitch BGA

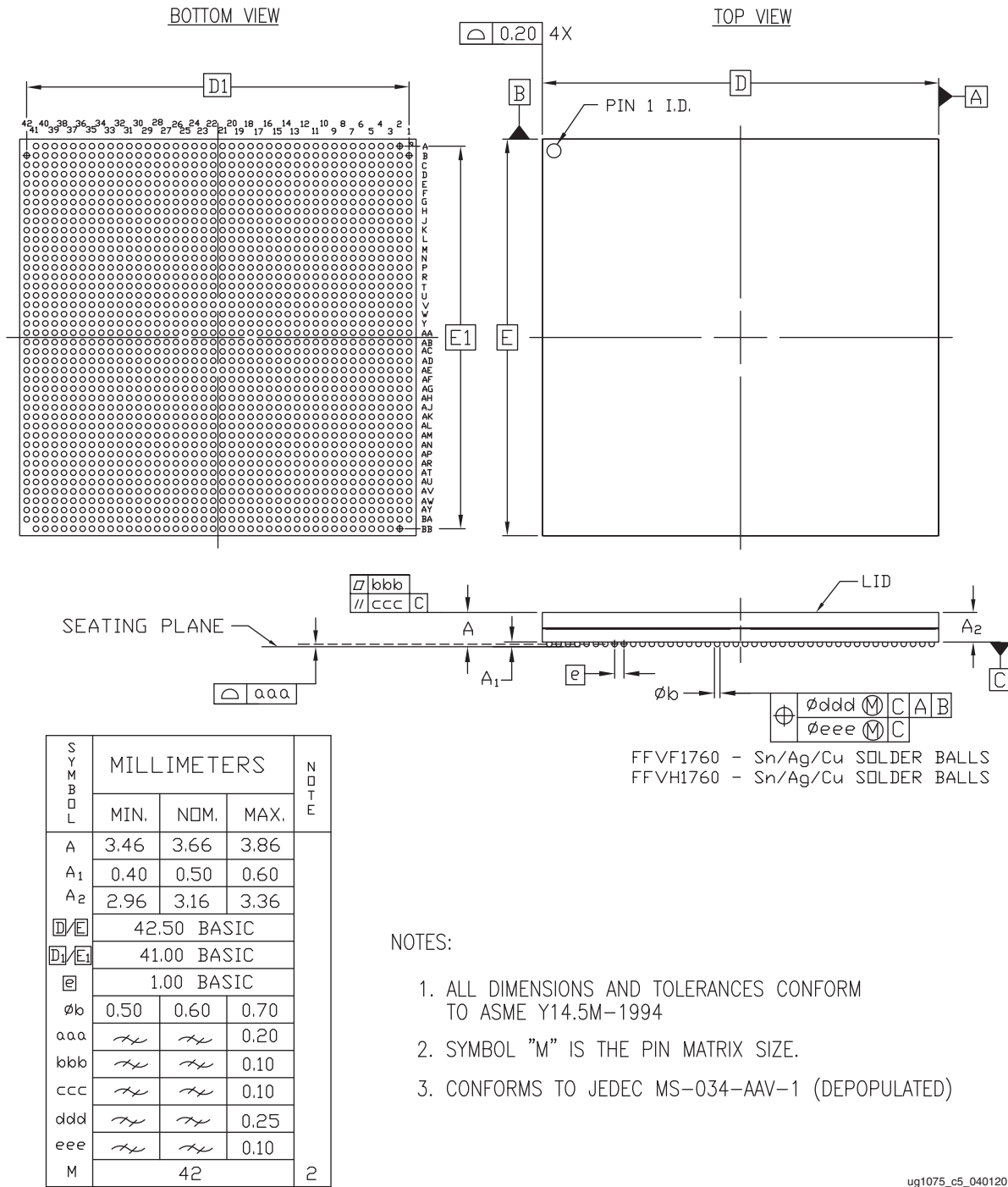


Figure 5-32: Package Dimensions for FFVF1760 (XCZU29DR, XCZU39DR, XCZU49DR) and FFVH1760 (XCZU46DR)

# FFRF1760 (XQZU29DR) Ruggedized Flip-Chip Fine-Pitch BGA

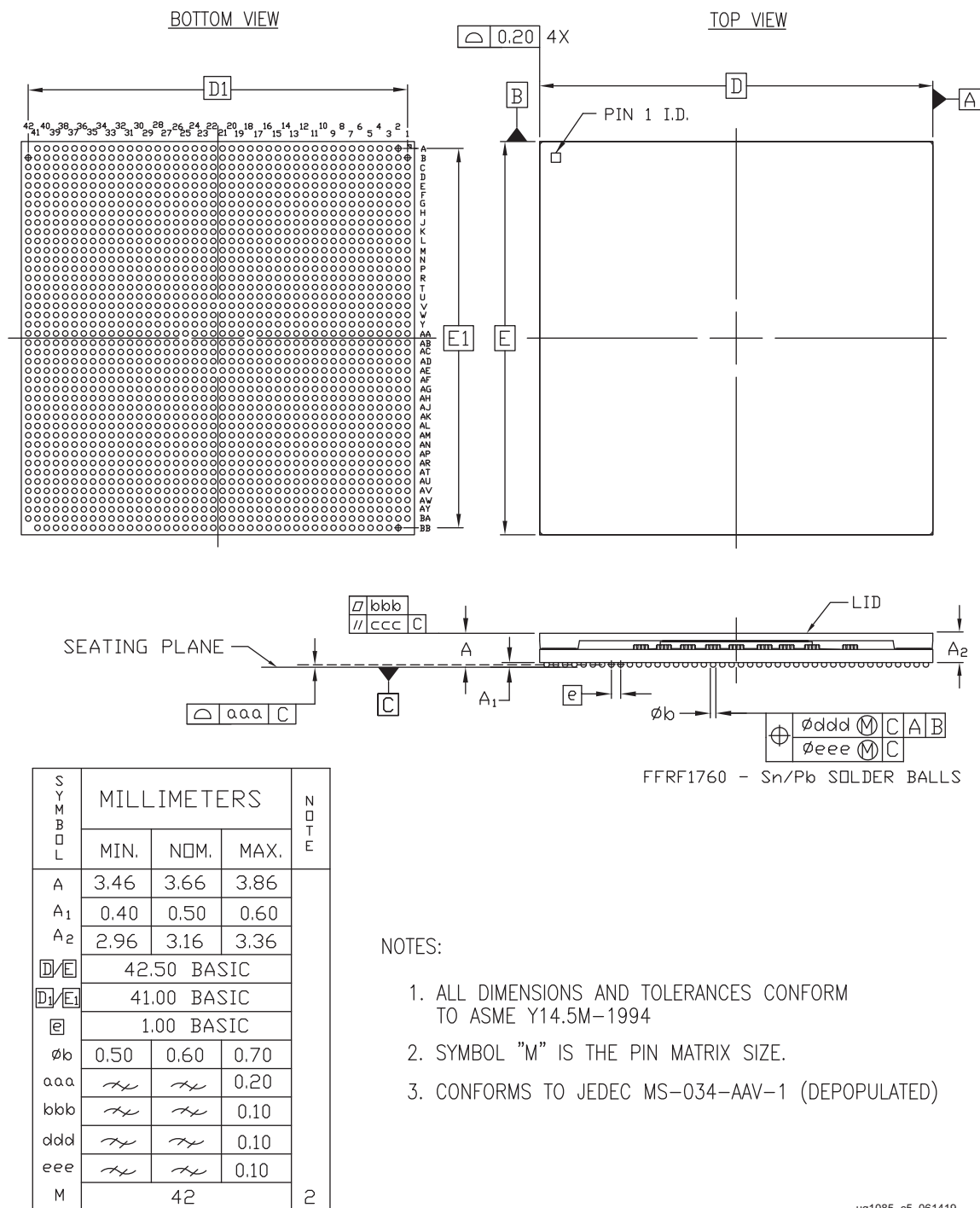
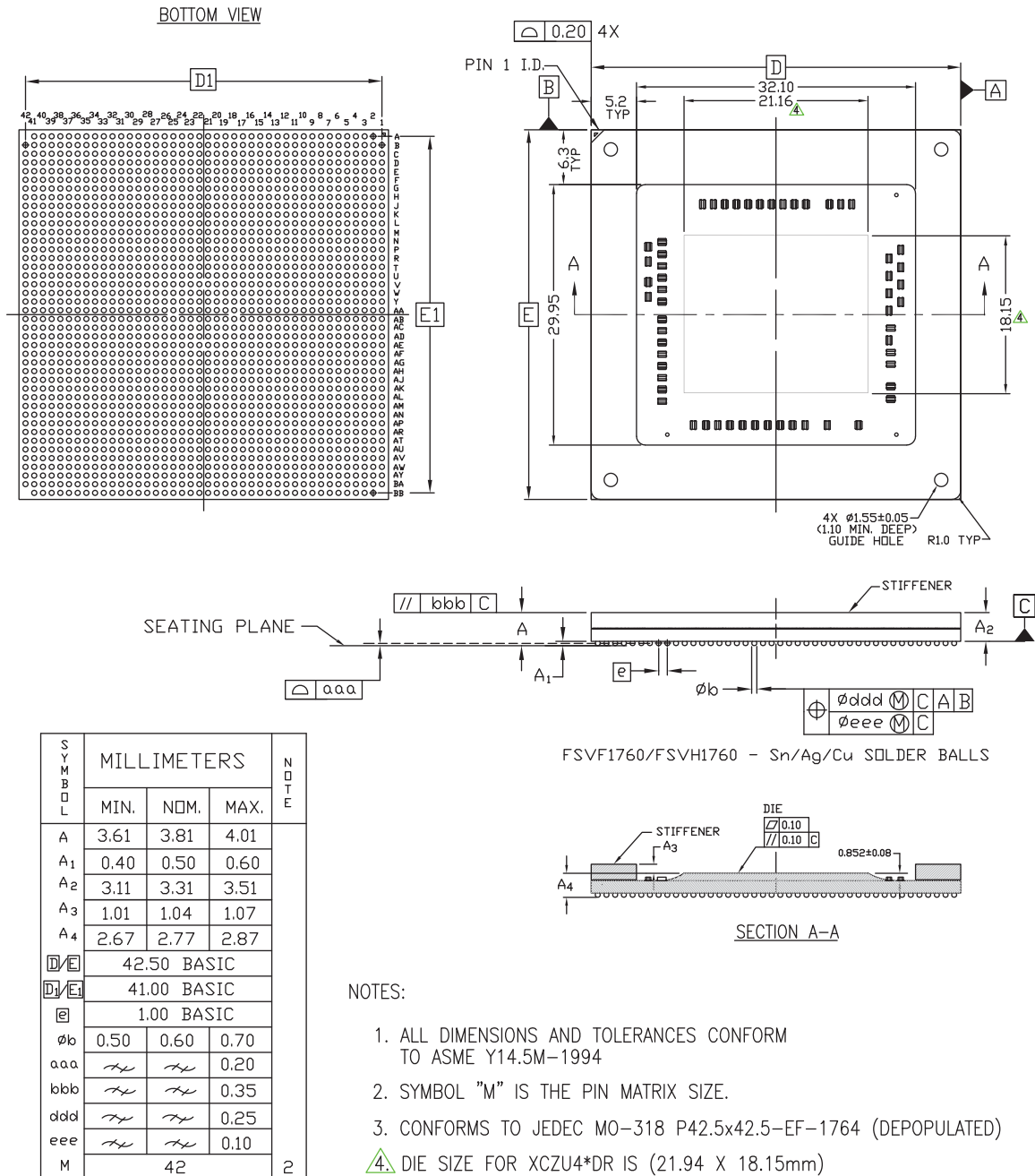


Figure 5-33: Package Dimensions for FFRF1760 (XQZU29DR)

# FSVF1760 (XCZU29DR, XCZU39DR, XCZU49DR) and FSVH1760 (XCZU46DR) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring BGA



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Figure 5-34: Package Dimensions for FSVF1760 (XCZU29DR, XCZU39DR, XCZU49DR) and FSVH1760 (XCZU46DR)

# FSRF1760 (XQZU49DR) Ruggedized Flip Chip, Fine-Pitch Lidless with Stiffener Ring BGA

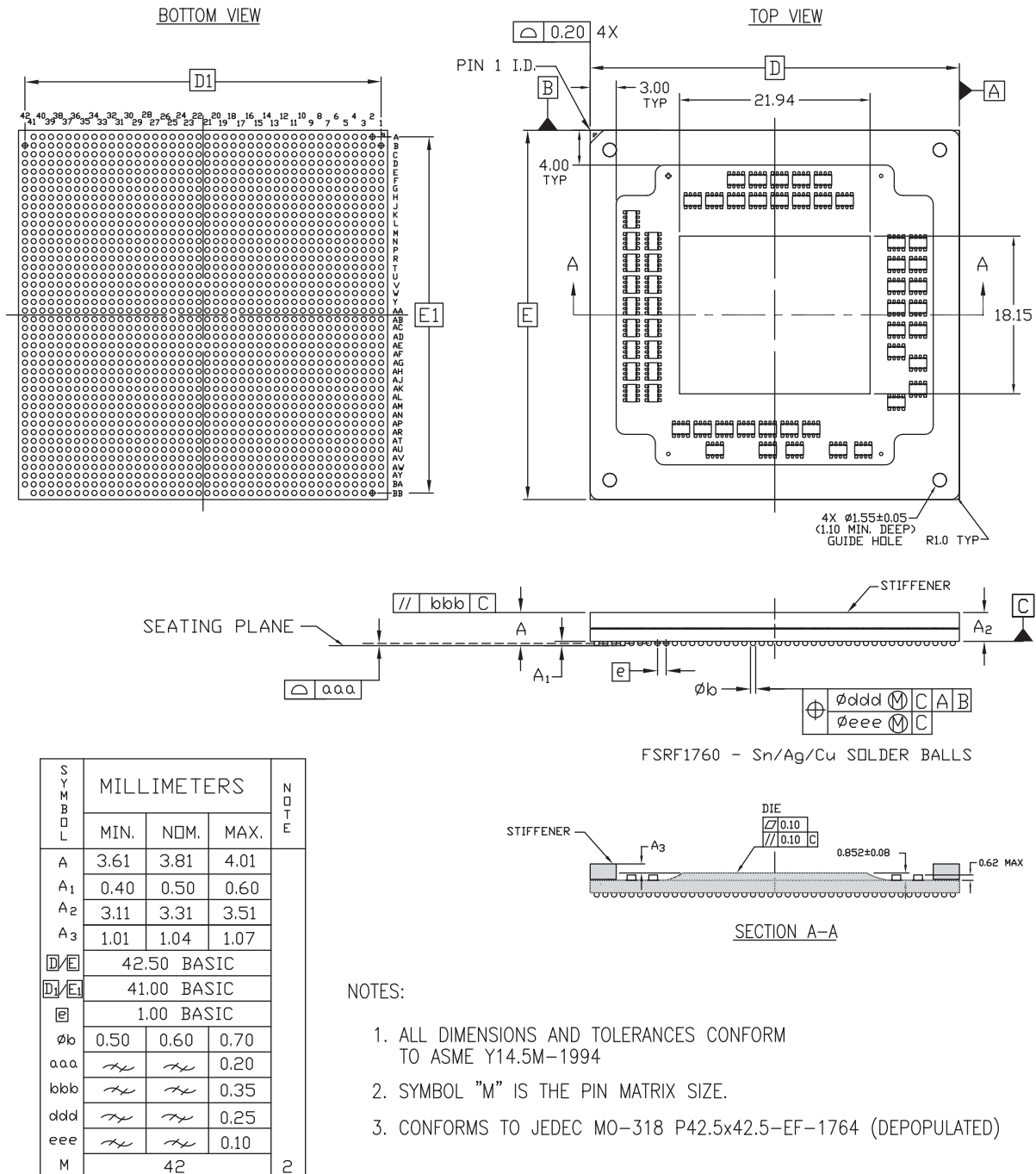


Figure 5-35: Package Dimensions for FSRF1760 (XQZU49DR)

# FFVE1924 Flip-Chip, Fine-Pitch BGA (XCZU17EG, and XCZU19EG)

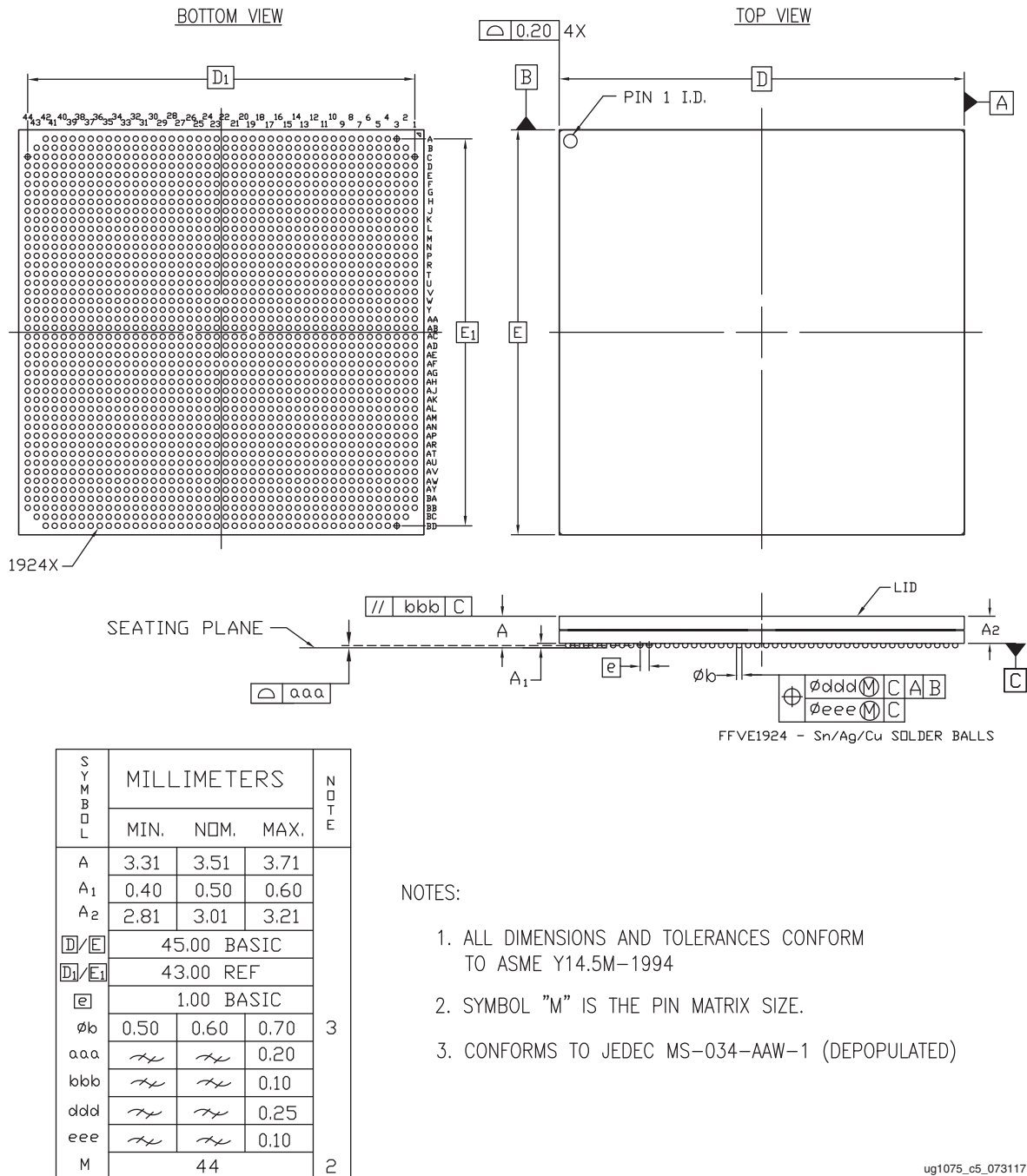


Figure 5-36: Package Dimensions for FFVE1924 (XCZU17EG and XCZU19EG)

# Package Marking

## Introduction

The package top-markings for the XC and XA Zynq™ UltraScale+™ devices are similar to the examples shown in [Figure 6-1](#) and [Figure 6-2](#). In addition to the markings explained in [Table 6-1](#), refer to the *FAQ: Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products* ([XTP424](#)) and ([XTP544](#)).

The package top-markings for the XQ Zynq UltraScale+ devices are as shown in [Figure 6-3](#). On XQ products only the AMD logo and the 2D bar code are marked.

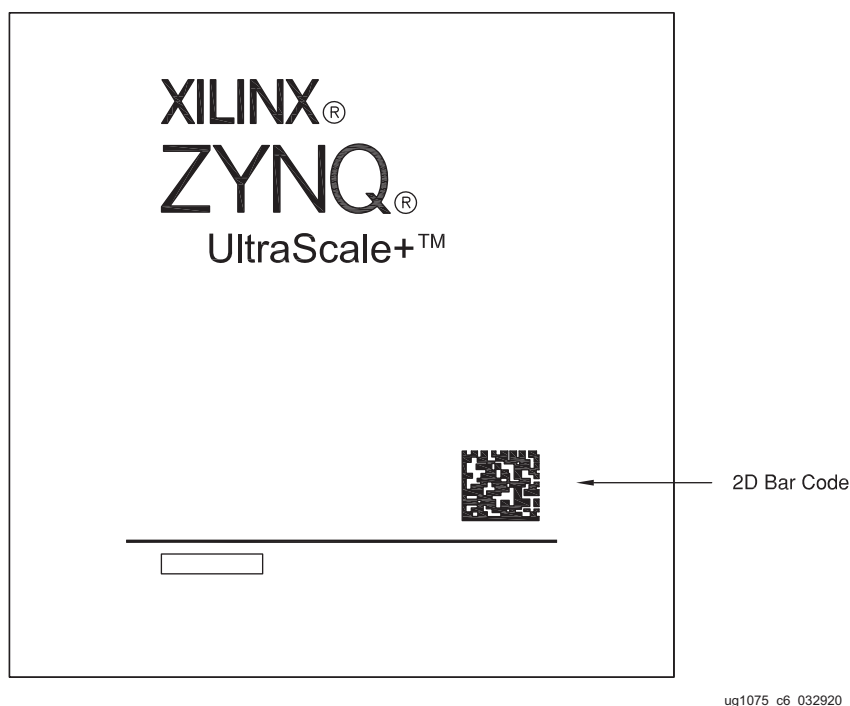
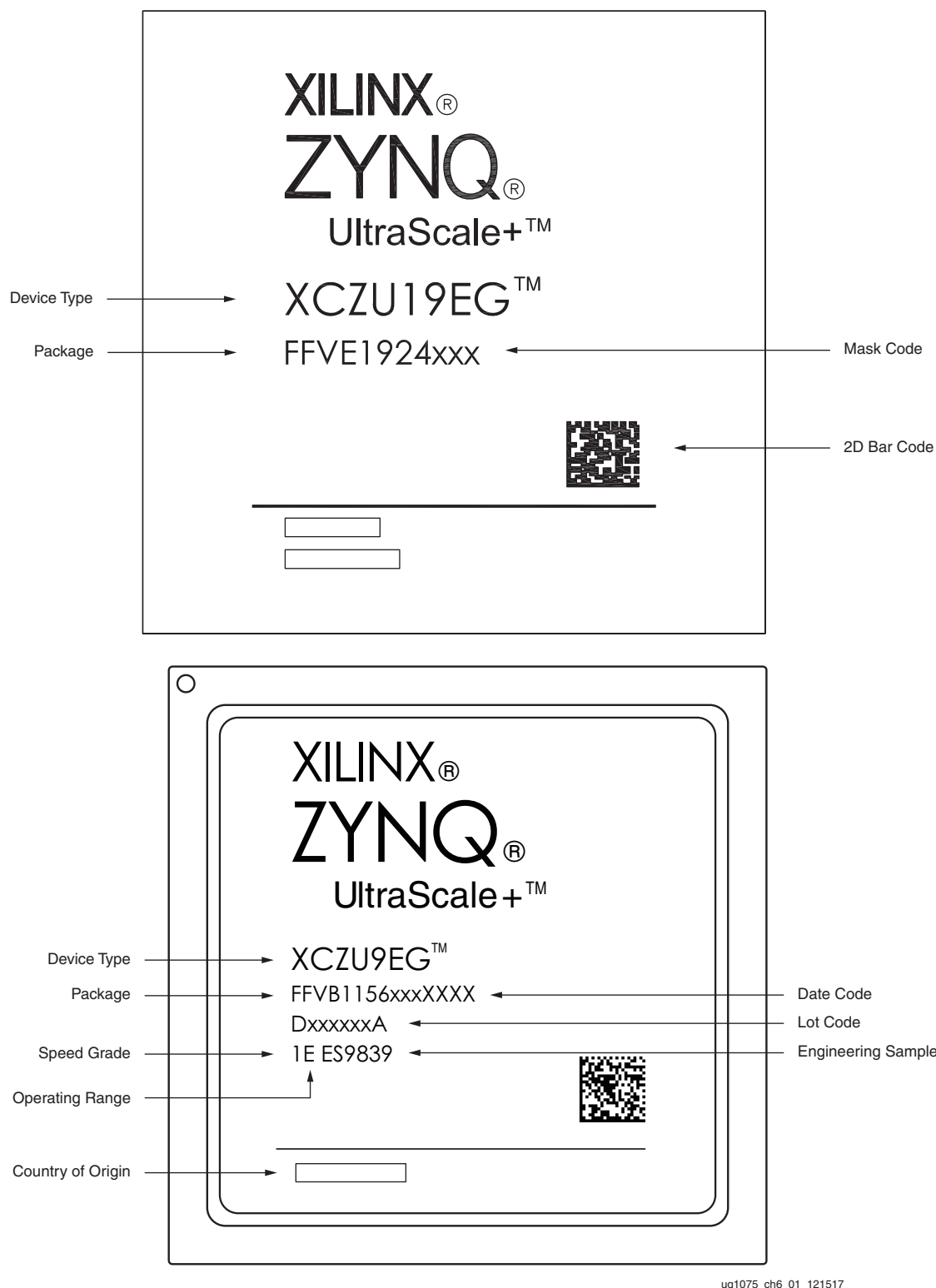


Figure 6-1: XC and XA Zynq UltraScale+ Devices Package Marking



ug1075\_ch6\_01\_121517

Figure 6-2: XC and XA Zynq UltraScale+ Devices Package Marking

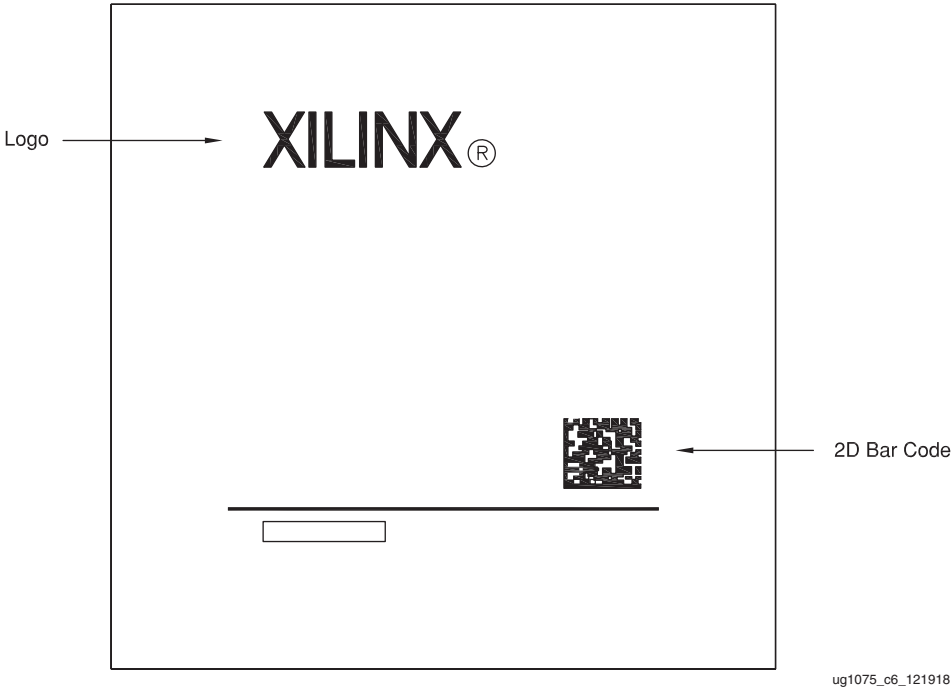


Figure 6-3: XQ Zynq UltraScale+ Devices Package Marking

Table 6-1: XC and XA Device Marking Definition—Example

| Item              | Definition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AMD Logo          | AMD logo, AMD name with trademark, and trademark-registered status.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Family Brand Logo | Device family name with trademark and trademark-registered status. This line is optional and could appear blank.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 1st Line          | Device name. This line is not marked on some devices. Refer to the bar code for more information.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 2nd Line          | <p>This line is not marked on some devices. Refer to the bar code for more information.</p> <ul style="list-style-type: none"><li>• Package code: <b>FF</b><br/>1st digit: F for flip-chip BGA, S for flip-chip BGA with 0.8 mm ball pitch.<br/>2nd digit: F for lidded, B for bare-die.</li><li>• 3rd digit: Pb-free code: <b>V</b> for RoHS 6/6, <b>R</b> or <b>Q</b> for packages with eutectic BGA balls.<br/>All Zynq UltraScale+ devices are available with Pb-free RoHS compliant packaging. For more details on Pb-free and RoHS compliant products, see: <a href="http://www.xilinx.com/pbfree">www.xilinx.com/pbfree</a>.</li><li>• 4th digit: This is the pin out (net list) identifier.</li><li>• 5th–8th digits: These are the physical pin count identifiers: <b>B1156</b> is shown in the <a href="#">Figure 6-2</a> example marking drawing. Example: A package code of FFVB1517 and FFVF1517 means they have a different pinout (net list) but the same physical ball count and physical dimensions.</li><li>• Three letter circuit design revision, the location code for the wafer fab, and the geometry code (<b>xxx</b>).</li><li>• When marked, the date code: <b>YYWW</b>. This code is not marked on some devices. Refer to the bar code for more information.</li></ul> |



Table 6-1: XC and XA Device Marking Definition—Example (Cont’d)

| Item     | Definition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                                                                                                                                                                        |
|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3rd Line | When marked, this line describes ten alphanumeric characters for assembly location, 7-digit lot number, and step information. The last digit is usually an A or an M if a stepping version does not exist.<br><br>This line is not marked on some devices. Refer to the bar code for more information.                                                                                                                                                                                                                                                                 |                                                                                                                                                                                                                                        |
| 4th Line | When marked, this line describes the device speed grade ( <b>1</b> ) and temperature operating range ( <b>E</b> ). When not marked on the package, the product is considered to operate at the extended (E) temperature range. If a bar code is present on the device, the 4th line might be blank or unmarked. In this case, refer to the bar code for speed grade and temperature range information. For more information on the ordering codes, see the <i>Zynq UltraScale+ MPSoC Overview</i> ( <a href="#">DS891</a> ).<br><br>Other variations for the 4th line: |                                                                                                                                                                                                                                        |
|          | L1I                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | The L1I indicates a -1LI device. The -1LI speed grade offers reduced maximum power consumption. For more information, see the <i>Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics</i> ( <a href="#">DS925</a> ). |
|          | 1E xxxx                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | The xxxx indicates a 4-digit SCD device option. An SCD is a special ordering code that is not always marked in the device top mark.                                                                                                    |
|          | 1E ES<br>2I ES<br>L1I ES                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | The addition of an ES after the operating temperature range code indicates an engineering sample.                                                                                                                                      |
| Bar Code | A device-specific bar code is marked on each device. Refer to the <i>FAQ: Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products</i> ( <a href="#">XTP424</a> ).                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                                        |

# Packing and Shipping

## Introduction

Zynq™ UltraScale+™ devices are packed in trays. Trays are used to pack most of the surface-mount devices since they provide excellent protection from mechanical damage. In addition, they are manufactured using antistatic material to provide limited protection against ESD damage and can withstand a bake temperature of 125°C.

**Table 7-1: Standard Device Counts per Tray and Box**

| Package                                                                          | Maximum Number of Devices Per Tray | Maximum Number of Units In One Internal Box |
|----------------------------------------------------------------------------------|------------------------------------|---------------------------------------------|
| SBVA484, SFRA484                                                                 | 84                                 | 420                                         |
| UBVA494                                                                          | 126                                | 630                                         |
| UBVA530                                                                          | 126                                | 630                                         |
| SFVA625                                                                          | 60                                 | 300                                         |
| SFVC784, SFVD784, SFVE784, SFRC784                                               | 60                                 | 300                                         |
| FBVB900, FFVC900, FFRB900, FFRC900                                               | 27                                 | 135                                         |
| FFVB1156, FFRB1156, FFVC1156, FFRC1156<br>FFVD1156, FFRD1156, FFVE1156, FFRE1156 | 24                                 | 120                                         |
| FSVE1156                                                                         | 24                                 | 72                                          |
| FFVB1517, FFRB1517, FFVF1517                                                     | 21                                 | 105                                         |
| FFVG1517, FFRG1517                                                               | 21                                 | 63                                          |
| FSVG1517, FSRG1517                                                               | 21                                 | 63                                          |
| FFVC1760, FFRC1760<br>FFVD1760, FFVF1760, FFRVH1760, FFRF1760                    | 12                                 | 60                                          |
| FSVF1760, FSVH1760, FSRF1760                                                     | 12                                 | 36                                          |
| FFVE1924                                                                         | 12                                 | 36                                          |



**IMPORTANT:** All non-InFO packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC or XA, and the Pb-free signifier in the package name is Q (for example: FFQE1156).

# Soldering Guidelines

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## Soldering Guidelines

To implement and control the production of surface-mount assemblies, the dynamics of the solder reflow process and how each element of the process is related to the end result must be thoroughly understood.



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**RECOMMENDED:** *AMD recommends that customers qualify their custom PCB assembly processes using package samples.*

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The primary phases of the reflow process are:

- Melting the particles in the solder paste
- Wetting the surfaces to be joined
- Solidifying the solder into a strong metallurgical bond

The peak reflow temperature of a surface-mount component body should not be more than 250°C maximum (260°C for dry rework only) for Pb-free packages and 220°C for eutectic packages, and is package size dependent. For multiple BGAs in a single board and because of surrounding component differences, AMD recommends checking all BGA sites for varying temperatures.

The infrared reflow (IR) process is strongly dependent on equipment and loading. Components might overheat due to lack of thermal constraints. Unbalanced loading can lead to significant temperature variation on the board. These guidelines are intended to assist users in avoiding damage to the components; the actual profile should be determined by those using these guidelines. For complete information on package moisture / reflow classification and package reflow conditions, refer to the Joint IPC/JEDEC Standard J-STD-020C.



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**IMPORTANT:** *Following the initial placement and reflow process, devices should not be reflowed more than two additional times and should not be removed from the board. Any additional rework beyond that is likely to cause irreparable damage to the device.*

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## Sn/Pb Reflow Soldering

Figure 8-1 shows typical conditions for solder reflow processing of Sn/Pb soldering using IR/convection. Both IR and convection furnaces are used for BGA assembly. The moisture sensitivity of surface-mount components must be verified prior to surface-mount flow.

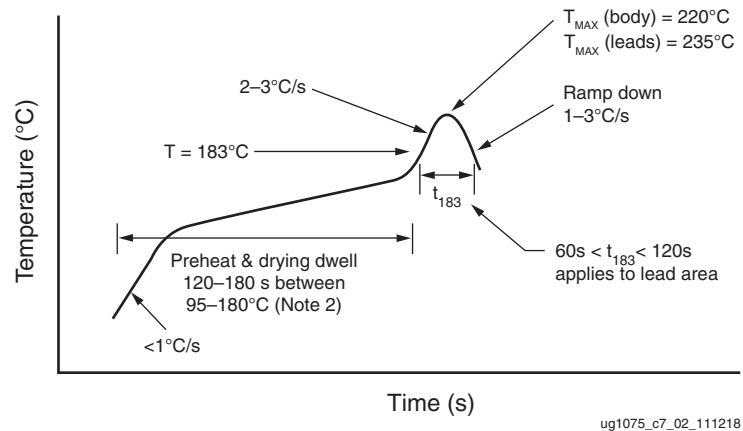


Figure 8-1: Typical Conditions for IR Reflow Soldering of Sn/Pb Solder

Notes for Figure 8-1:

1. Maximum temperature range = 220°C (body). Minimum temperature range before 205°C (leads/balls).
2. Preheat dwell 95–180°C for 120–180 seconds.
3. IR reflow must be performed on dry packages.

## Pb-Free Reflow Soldering

AMD uses SnAgCu solder balls for commercial-grade (XC) and automotive-grade (XA) BGA packages. In addition, suitable package materials are qualified for the higher reflow temperatures (250°C maximum, 260°C for dry rework only) required by Pb-free soldering processes.

AMD does not support soldering SnAgCu BGA packages with SnPb solder paste using a Sn/Pb soldering process. Traditional Sn/Pb soldering processes have a peak reflow temperature of 220°C. At this temperature range, the SnAgCu BGA solder balls do not properly melt and wet to the soldering surfaces. As a result, reliability and assembly yields can be compromised.

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs using thermocouples at multiple locations on the component. In addition, if there is a mixture of devices on the board, then the profile should be checked at various locations on the board. Ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that might damage the smaller, heat sensitive components.

[Table 8-1](#) and [Figure 8-2](#) provide guidelines for profiling Pb-free solder reflow of 0.8 mm and 1.0 mm pitch packages. InFo package guidelines are listed in a separate [Table 8-2](#). In general, a gradual, linear ramp into a spike has been shown by various sources to be the optimal reflow profile for Pb-free solders ([Figure 8-2](#)). This profile has been shown to yield better wetting and less thermal shock than conventional ramp-soak-spike profile for the Sn/Pb system. SnAgCu alloy reaches full liquidus temperature at 235°C. When profiling, identify the possible locations of the coldest solder joints and ensure that those solder joints reach a minimum peak temperature of 235°C for at least 10 seconds. Reflowing at high peak temperatures of 260°C and above can damage the heat sensitive components and cause the board to warp. Users should reference the latest IPC/JEDEC J-STD-020 standard for the allowable peak temperature on the component body. The allowable peak temperature on the component body is dependent on the size of the component. Refer to [Table 8-3](#) for peak package reflow body temperature information. In any case, use a reflow profile with the lowest peak temperature possible.

**Table 8-1: Pb-Free Reflow Soldering Guidelines**

| Profile Feature                            | Convection, IR/Convection                                              |
|--------------------------------------------|------------------------------------------------------------------------|
| Ramp-up rate                               | 2°C/s maximum. 1°C/s maximum for lidless packages with stiffener ring. |
| Preheat temperature 150°–200°C             | 60–120 seconds.                                                        |
| Temperature maintained above 217°C         | 60–150 seconds (60–90 seconds typical).                                |
| Time within 5°C of actual peak temperature | 30 seconds maximum.                                                    |

Table 8-1: Pb-Free Reflow Soldering Guidelines (Cont'd)

| Profile Feature               | Convection, IR/Convection                                                     |
|-------------------------------|-------------------------------------------------------------------------------|
| Peak temperature (lead/ball)  | 230°C–245°C typical (depends on solder paste, board size, component mixture). |
| Peak temperature (body)       | 240°C–250°C, package body size dependent.                                     |
| Ramp-down rate                | 2°C/s maximum.                                                                |
| Time 25°C to peak temperature | 3.5 minutes minimum, 5.0 minutes typical, 8 minutes maximum.                  |

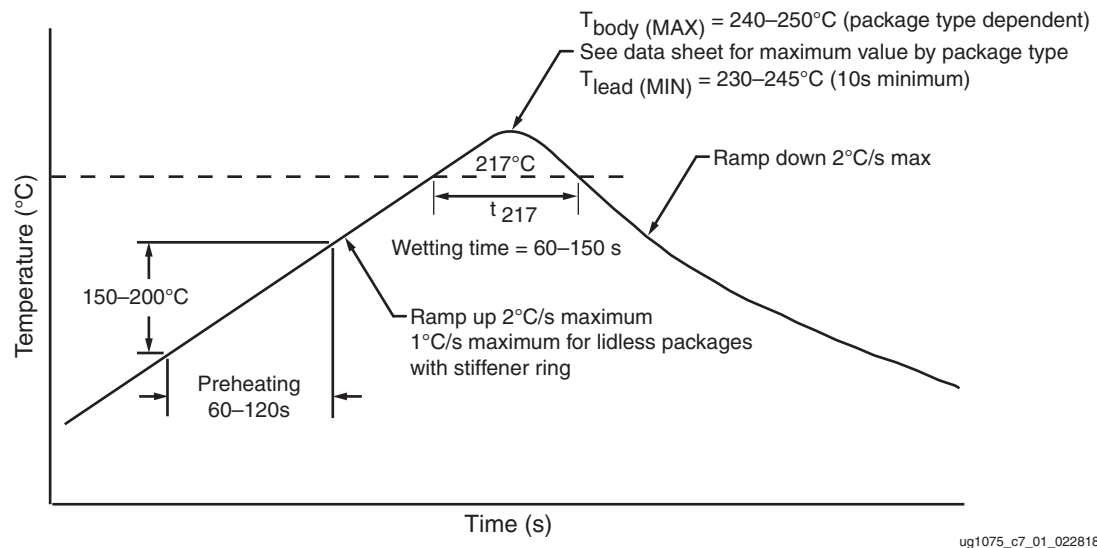


Figure 8-2: Typical Conditions for Pb-Free Reflow Soldering

Table 8-2: InFO Package Reflow Soldering Guidelines

| Profile Feature                            | Convection, IR/Convection                                                    |
|--------------------------------------------|------------------------------------------------------------------------------|
| Ramp-up rate                               | 4°C/s maximum                                                                |
| Preheat temperature 150°–190°C             | 60–100 seconds                                                               |
| Temperature maintained above 217°C         | 45–75 seconds                                                                |
| Time within 5°C of actual peak temperature | 30 seconds maximum                                                           |
| Peak temperature (lead/ball)               | 230°C–235°C typical (depends on solder paste, board size, component mixture) |
| Peak temperature (body)                    | 240°C–245°C                                                                  |
| Ramp-down rate                             | 2°C/s maximum.                                                               |
| Time 25°C to peak temperature              | 3.5 minutes minimum, 5.0 minutes typical, 8 minutes maximum.                 |

## Peak Package Reflow Temperatures

Table 8-3: Peak Package Reflow Body Temperature (Based on J-STD-020 Standard)

| Package                                                                                                                                                                  | Product Category  | Peak Package Reflow Body Temperature    | JEDEC Moisture Sensitivity Level (MSL) |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-----------------------------------------|----------------------------------------|
| SBVA484                                                                                                                                                                  | XC                | Mass reflow: 250°C<br>Dry rework: 260°C | 4                                      |
| SFVA625                                                                                                                                                                  | XA                |                                         | 3                                      |
| SFVC784                                                                                                                                                                  |                   |                                         |                                        |
| SFVD784                                                                                                                                                                  |                   |                                         |                                        |
| UBVA494<br>UBVA530<br>FBVB900, FFVC900<br>FFVB1156, FFVC1156<br>FFVD1156, FFVE1156<br>FFVB1517, FFVF1517, FFVG1517<br>FFVC1760, FFVD1760, FFVF1760, FFVH1760<br>FFVE1924 | XC                | Mass reflow: 245°C<br>Dry rework: 260°C | 4                                      |
| FBVB900<br>FFVF1517                                                                                                                                                      | XA                |                                         | 3                                      |
| FSVE1156<br>FSVG1517<br>FSVF1760, FSVH1760                                                                                                                               | All               | Mass reflow: 240°C<br>Dry rework: 260°C | 4                                      |
| SFRA484, SFRC784<br>FFRB900, FFRC900<br>FFRB1156, FFRC1156<br>FFRD1156, FFRE1156<br>FFRB1517, FFRG1517, FSRG1517<br>FFRC1760, FFRF1760, FSRF1760                         | XQ <sup>(1)</sup> | Mass reflow: 220°C<br>Dry rework: 235°C | 4                                      |

### Notes:

- For devices with the Pb-free signifier in the package name (labeled as Q vs. V) use the temperatures and MSL listed for the XQ product category.

For sophisticated boards with a substantial mix of large and small components, it is critical to minimize the  $\Delta T$  across the board ( $<10^{\circ}\text{C}$ ) to minimize board warpage and thus, attain higher assembly yields. Minimizing the  $\Delta T$  is accomplished by using a slower rate in the warm-up and preheating stages. AMD recommends a heating rate of less than  $1^{\circ}\text{C/s}$  during the preheating and soaking stages, in combination with a heating rate of not more than  $3^{\circ}\text{C/s}$  throughout the rest of the profile.

It is also important to minimize the temperature gradient on the component, between top surface and bottom side, especially during the cooling down phase. The key is to optimize cooling while maintaining a minimal temperature differential between the top surface of the package and the solder joint area. The temperature differential between the top surface

of the component and the solder balls should be maintained at less than 7°C during the critical region of the cooling phase of the reflow process. This critical region is in the part of the cooling phase where the balls are not completely solidified to the board yet, usually between the 200°C–217°C range. To efficiently cool the parts, divide the cooling section into multiple zones, with each zone operating at different temperatures.

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs using thermocouples at multiple locations on the component. In addition, if there is a mixture of devices on the board, then the profile should be checked at various locations on the board, as shown in [Figure 8-3](#) and [Figure 8-4](#). Ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that might damage the smaller, heat sensitive components.

**TOP Profile,**

- TC 1 : U17 Edge 1
- TC 2 : U17 Edge 2
- TC 3 : U17 Edge 3
- TC 4 : U17 Edge 4
- TC 5 : U17 Middle 1
- TC 6 : U17 Middle 2
- TC 7 : U17 Body
- TC 8 : Q25
- TC 9 : U25

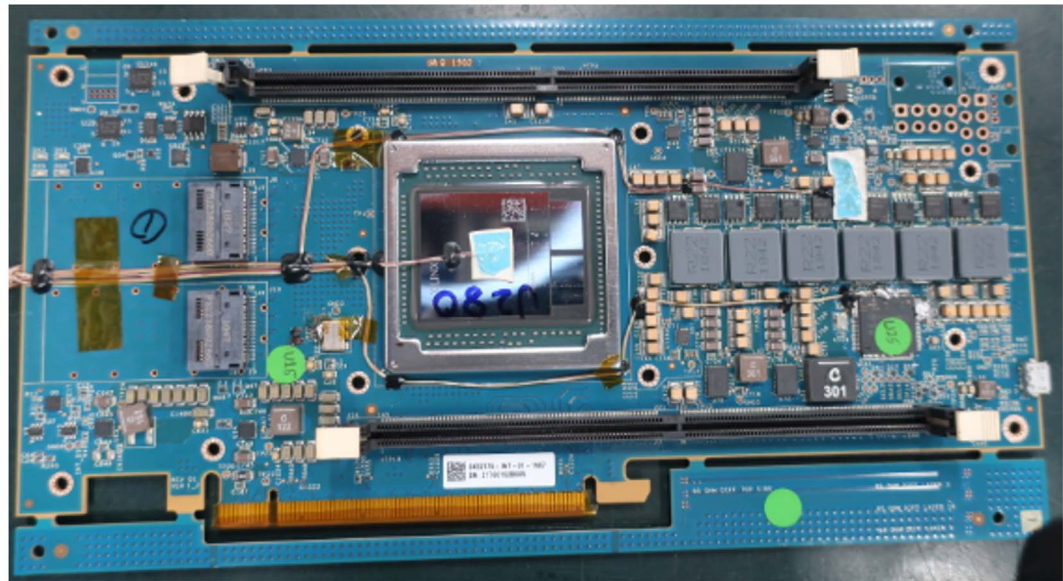


*Figure 8-3: Thermocouple Top*



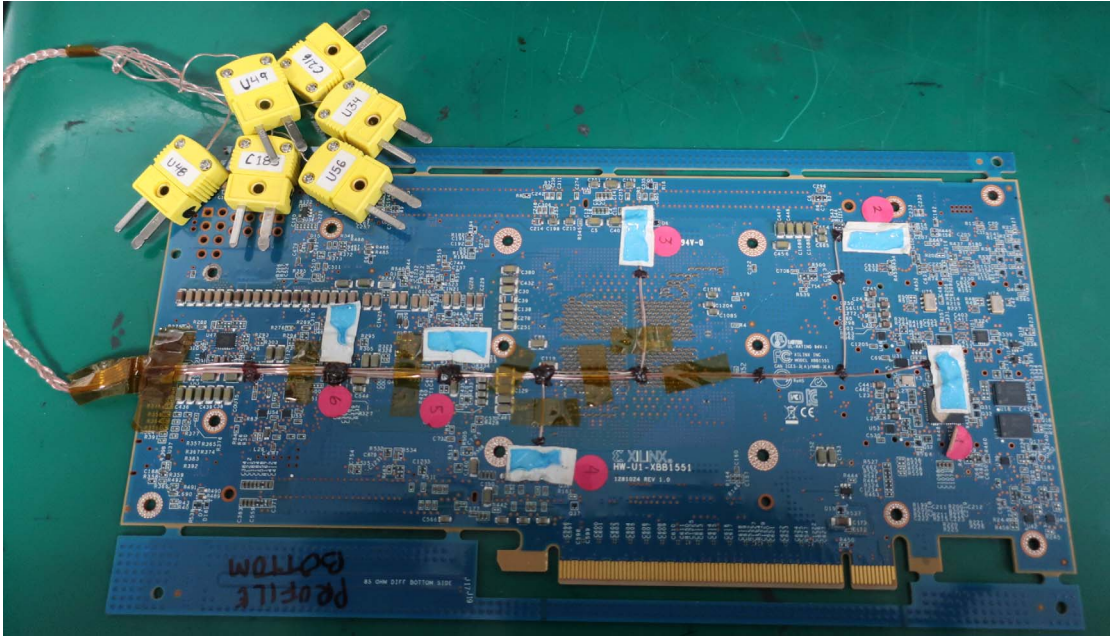


Figure 8-4: Thermocouple Bottom

## Post Reflow/Cleaning/Washing

Many PCB assembly subcontractors use a no-clean process in which no post-assembly washing is required. Although a no-clean process is recommended, if cleaning is required, AMD recommends a water-soluble paste and a washer using a deionized-water. Baking after the water wash is recommended to prevent fluid accumulation.

Cleaning solutions or solvents are not recommended because some solutions contain chemicals that can compromise the lid adhesive, thermal compound, or components inside the package.

---

## Strain Gauge Measurement

Strain gauge measurements are recommended to be done at each process step that has the potential to cause excessive board flexing leading to solder joint cracking. Assembly processes where strain gauge measurements are recommended include:

- PCB Router (during PCB loading/unloading into fixture and during the routing process)
- PTH solder assembly during top-catch loading/unloading
- Press fit assembly during press base and tooling loading/unloading and during machine pressing process
- DIMM memory (during PCB loading/unloading and during insertion/removal of DIMM)

- Heat-sink assembly process (during PCB loading/unloading and during entire screw assembly process)
- X-ray fixture (during PCBA loading/unloading)

Strain gauge measurements should be in the range of  $\pm 500$   $\mu$ strain. Dye and pry analysis is required to confirm if the measured strain causes solder joint cracking. It is recommended to conduct dye and pry analysis for any strain reading greater than 500  $\mu$ strain.

To reduce the effects of strain on a device, edge bonding can be used and is recommended for larger packages. See [Edge Bonding and Underfill Guidelines](#) for implementation details.

---

## Solder Paste

Solder paste consists of solder alloy and a flux system. A typical solder paste composition by volume is split between about 50% alloy and 50% flux. The metal load mass (solder alloy powder) is around 90%, with the remaining 10% mass a flux system. The primary purpose of the flux system is to remove the contaminations from the solder joints during the soldering process. The capability of removing contaminations is determined by the activation level of the type of solder paste. The preferred solder paste metal alloy has a lead-free composition (SnAgCu where Ag is 3–4% and Cu is 0.5–1%). A *no-clean* solder paste is preferred to eliminate any risk of improper cleaning that could leave active residue beneath the device and other BTC components. The paste must be suitable for printing the solder stencil aperture dimensions. Type 4 paste is recommended for better paste release performance. When using a solder paste, you must adhere to the handling recommendations of the paste manufacturer.

---

## Component Placement



**IMPORTANT:** *The following component placement guidelines apply to all package types included in this guide (lidded, lidless, bare-die, etc.).*

---

AMD device packages must be placed accurately according to their geometry outline. Positioning packages manually via hand mounting is not recommended.

Typical component placement accuracies of  $\pm 50$   $\mu$ m can be achieved using standard pick and placement machine equipment with vision system. The PCB and the components are optically checked and measured and the components are placed on the PCB in specific programmed positions based on the PCB CAD information. The pick and placement machine vision system detects the fiducials on the PCB immediately prior to mounting the FPGA. Recognition of the packages is performed by the vision system, to ensure correct centering of the FPGA placement on the PCB pad array.

BGA packages with solder balls can self-align during the reflow process because of the solder high surface tension that enables the pulling and centering of the device, and where a slight offset of the placement is still allowed. For guidance, the maximum tolerable offset of device placement is around 30% of the pad diameter on the PCB for typical non-solder mask defined pads. This means that for device packages the solder ball to PCB pad misalignment must be better than 150  $\mu\text{m}$  to assure a robust mounting process. Generally, this is achievable using a wide range of modern pick and placement systems. The following setup conditions are important for the pick and placement systems:

- The pick and placement nozzle type should be sized to the dimensions of the AMD device. The nozzle needs to firmly hold the device package during the pick and placement stage. The appropriate nozzle type for the device package can be chosen from the manual provided by the pick and placement equipment company.
- The ball recognition capabilities of the placement system should be used and package outline centering should be avoided. This eliminates the solder ball to package edge tolerances of the package. Refer to the specific package outline drawing for details.
- To ensure the proper identification of the device package by the vision system, a suitable lighting system and the correct choice of the features of the measuring method are essential. The most suitable settings can be chosen from the manual provided by the pick and placement equipments company.
- To avoid solder bridging or solder smear, ensure the proper placement force of the device package during placement on the PCB. Excessive placement force can lead to excess solder paste and cause solder bridging. However, a slight placement force can lead to insufficient solder paste contact between the device package solder balls and the solder paste, causing solder defects including open solder joints, badly centered packages, or even head-in-pillow (HIP) defects.

# Recommended PCB Design Rules for BGA Packages

## BGA Packages

AMD provides the diameter of a land pad on the package side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are described in [Figure 9-1](#) and summarized in [Table 9-1](#) for 1.0 mm pitch packages. For AMD BGA packages, non-solder mask defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in [Figure 9-1](#). An example of an NSMD PCB pad solder joint is shown in [Figure 9-2](#). It is recommended to have the board land pad diameter with a 1:1 ratio to the package solder mask defined (SMD) pad for improved board level reliability. The space between the NSMD pad and the solder mask as well as the actual signal trace widths depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

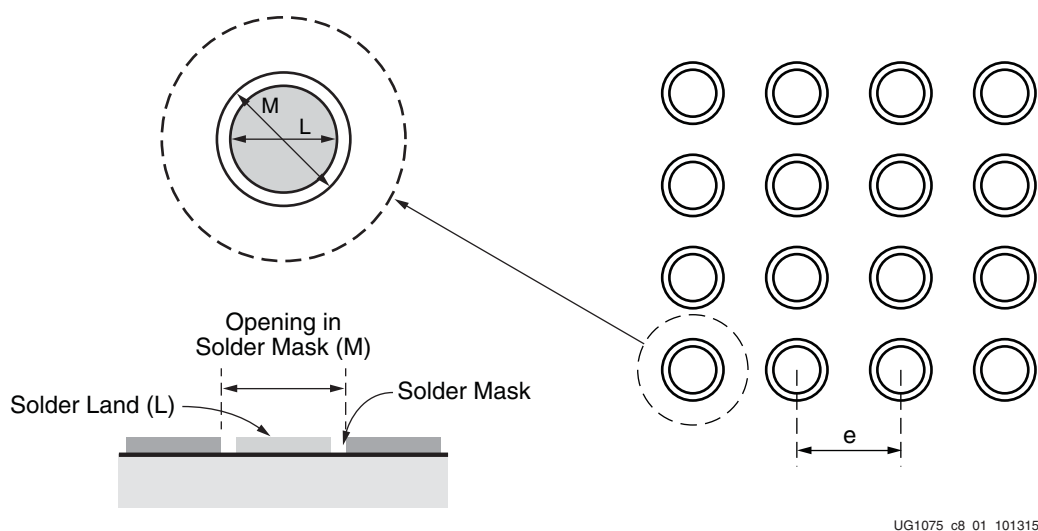
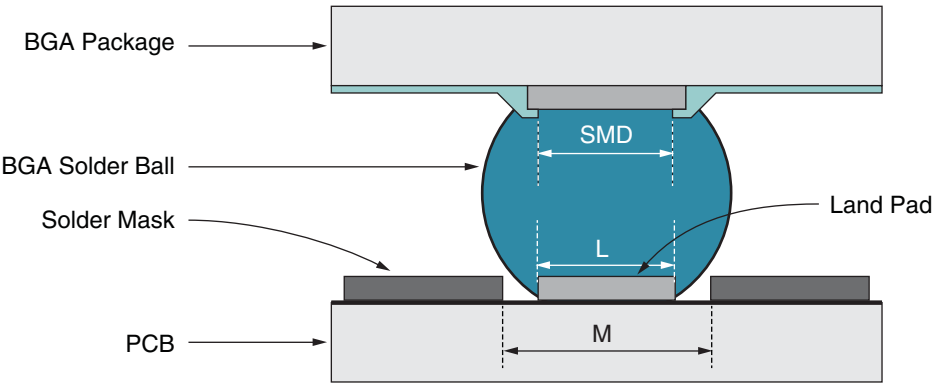


Figure 9-1: Suggested Board Layout of Soldered Pads for BGA Packages



UG1075\_c8\_02\_101315

Figure 9-2: Example of an NSMD PCB Pad Solder Joint

Table 9-1: BGA Package Design Rules

| Flip-Chip BGA Packages                  | 1.0 mm Pitch            | 0.8 mm Pitch        | 0.5 mm Pitch        |
|-----------------------------------------|-------------------------|---------------------|---------------------|
| Design Rule                             | Dimensions in mm (mils) |                     |                     |
| Package land pad opening (SMD)          | 0.53 mm (20.9 mils)     | 0.40 mm (15.7 mils) | 0.28 mm (11.0 mils) |
| Maximum PCB solder land (L) diameter    | 0.53 mm (20.9 mils)     | 0.40 mm (15.7 mils) | 0.30 mm (12.0 mils) |
| Opening in PCB solder mask (M) diameter | 0.63 mm (24.8 mils)     | 0.50 mm (19.7 mils) | 0.41 mm (16.0 mils) |
| Solder ball land pitch (e)              | 1.00 mm (39.4 mils)     | 0.80 mm (31.5 mils) | 0.50 mm (19.7 mils) |

Notes:

1. Controlling dimension in mm.

## Stencil

Solder paste is applied to PCB metal pads by screen printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. In most cases, the thickness of a stencil must be matched to the needs of all components on the PCB. Stencil apertures should be a circular shape. To ensure a uniform and high-solder paste transfer to the PCB, laser-cut stencil, made from mostly stainless steel, is typically used. Nickel blank stencils, referring to stencils where the entire foil is laser-cut from a sheet of pure nickel material, can also be used. However, high-quality nano-coated stencils (laser cut from stainless steel) can perform as well as or better than nickel blanks.

### Uniform Stencil Aperture Design

- For packages with 1 mm or 0.8 mm ball pitch, a uniform stencil aperture opening of 19.7 mils to 20.0 mils round is recommended.
- For InFO packages with 0.5 mm ball pitch, a uniform stencil with squared aperture openings (rounded corners) of 12 mils and pitch of 19.8 mils, as show in [Figure 9-3](#) is recommended. A stencil thickness of 4 mils is also recommended.

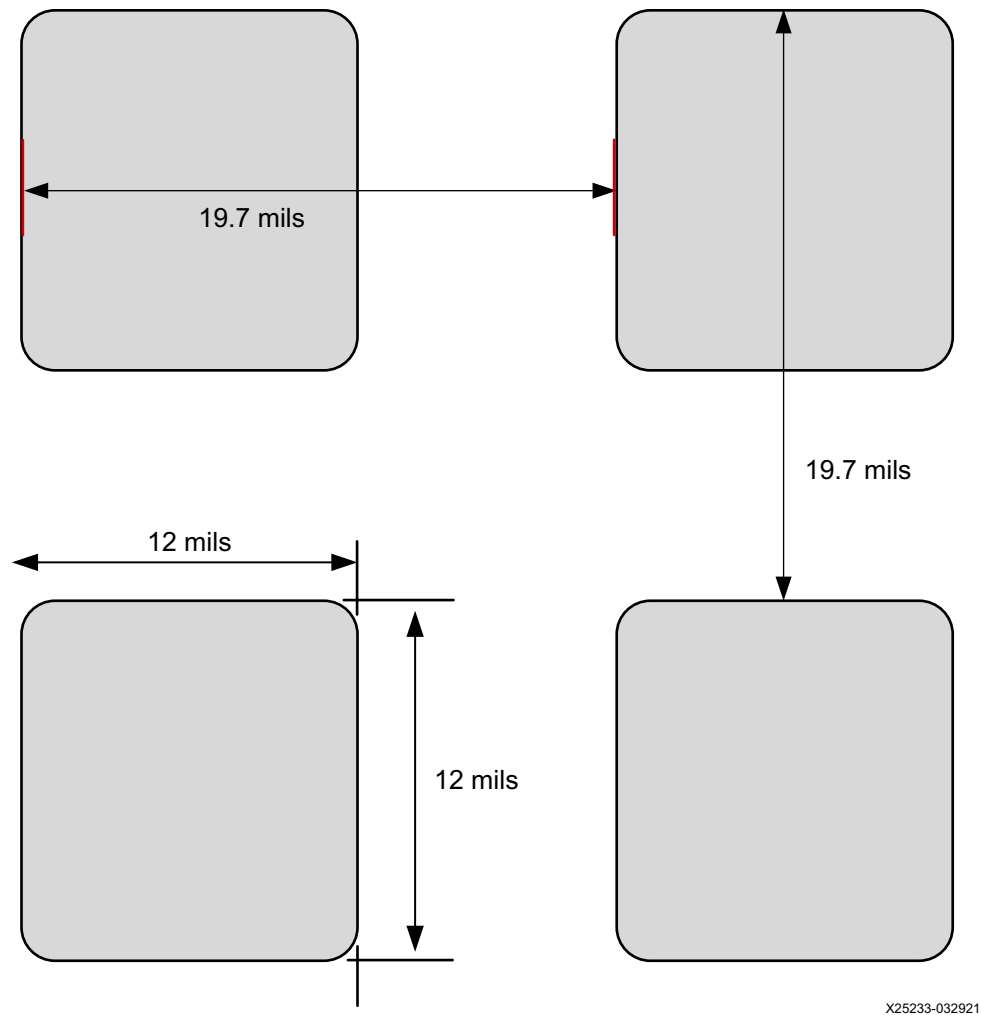


Figure 9-3: Recommended Stencil Design for InFO Packages

# Edge Bonding and Underfill Guidelines

## Summary

The edge bonding technique uses high-adhesion adhesives dispensed along the periphery of a component, as shown in [Figure 10-1](#). AMD recommends edge bonding for increased mechanical reliability in cases where the device is exposed to extensive temperature cycling or extreme shock and vibration, such as space, defense, and telecommunications applications. Designers are expected to evaluate the need for edge bonding based on the requirements of the specific application implementation.

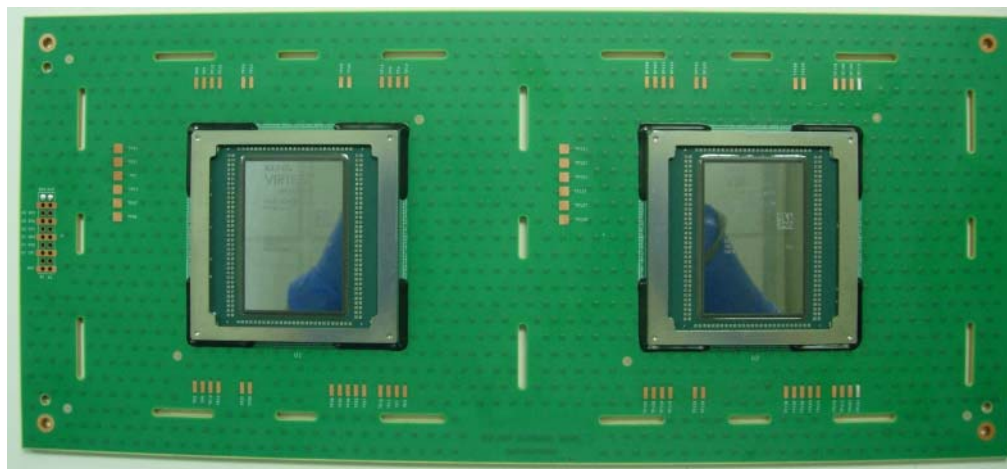


*Figure 10-1:* Edge Bonded BGA Packages



# Edge Bonding Implementation

Edge bonding is the dispensing of an epoxy material around the periphery of the package after board mount. The following guidelines are based on evaluation using the [Zymet UA-2605-B](#) edge bonding material.

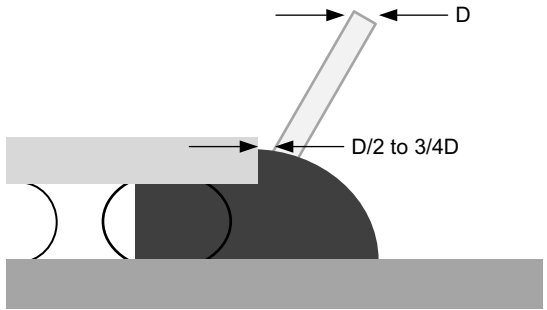
This technique allows for component rework and improves the robustness of the mounted component by controlling the expansion and warpage of the board during normal operating conditions.



**IMPORTANT:** *Following the initial placement and reflow process, devices should not be reflowed more than two additional times and should not be removed from the board. Any additional rework beyond that is likely to cause irreparable damage to the device.*

To place the adhesive while using an in-line soldering robot, AMD recommends the parameters shown in [Table 10-1](#).

Table 10-1: Process Parameters for Edge Bonding

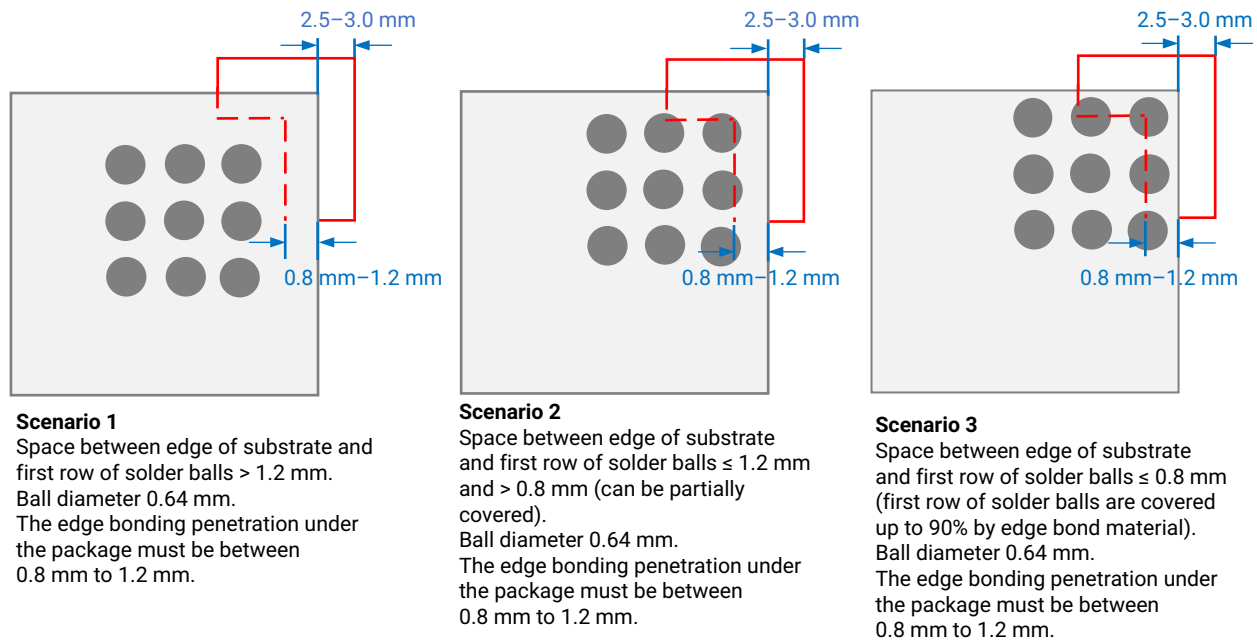
| Process Parameter     | Range Specification                                                                                                                                              |
|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Needle size           | 25—15, where needle diameter (D) is 20 gauge (0.91 mm) typical                                                                                                   |
| Needle height         | Above the device edge midpoint, or 0 to 1.5 mm below the device top surface (1.0 mm typical)                                                                     |
| Needle edge spacing   | Half to three quarters of the needle outer diameter (D)<br><br>X23147-041322 |
| Dispense needle speed | 0.1 to 200 mm/second (typical 6 mm/sec)                                                                                                                          |
| Valve pressure        | 10 to 60 psi (typical 14 psi)                                                                                                                                    |

The adhesive is dispensed along the perimeter of the assembled component at a width of 3 mm and a height of 50% to 90% the substrate height, leaving a small section at the center of each edge unbonded, as illustrated in [Figure 10-3](#). This is to ensure that there is an outlet for any expansion of the air during processing. AMD recommends centering the opening on each side with a width of 25–30% the length of the package substrate. The exact locations and size of the openings can be varied depending on the design and rework.

To ensure proper mechanical bonding between the package and PCB, the edge bonding feature must penetrate the edge bonding material under the package substrate by 0.8 mm. This requirement is necessary for packages with coplanarity  $\leq 200 \mu\text{m}$ , and BGA pitch of 1 mm or 0.92 mm, to pass physical qualification tests such as thermal cycle, power cycle, and shock and vibration requirements. It is necessary for special applications such as telecom, industrial, and data center applications.

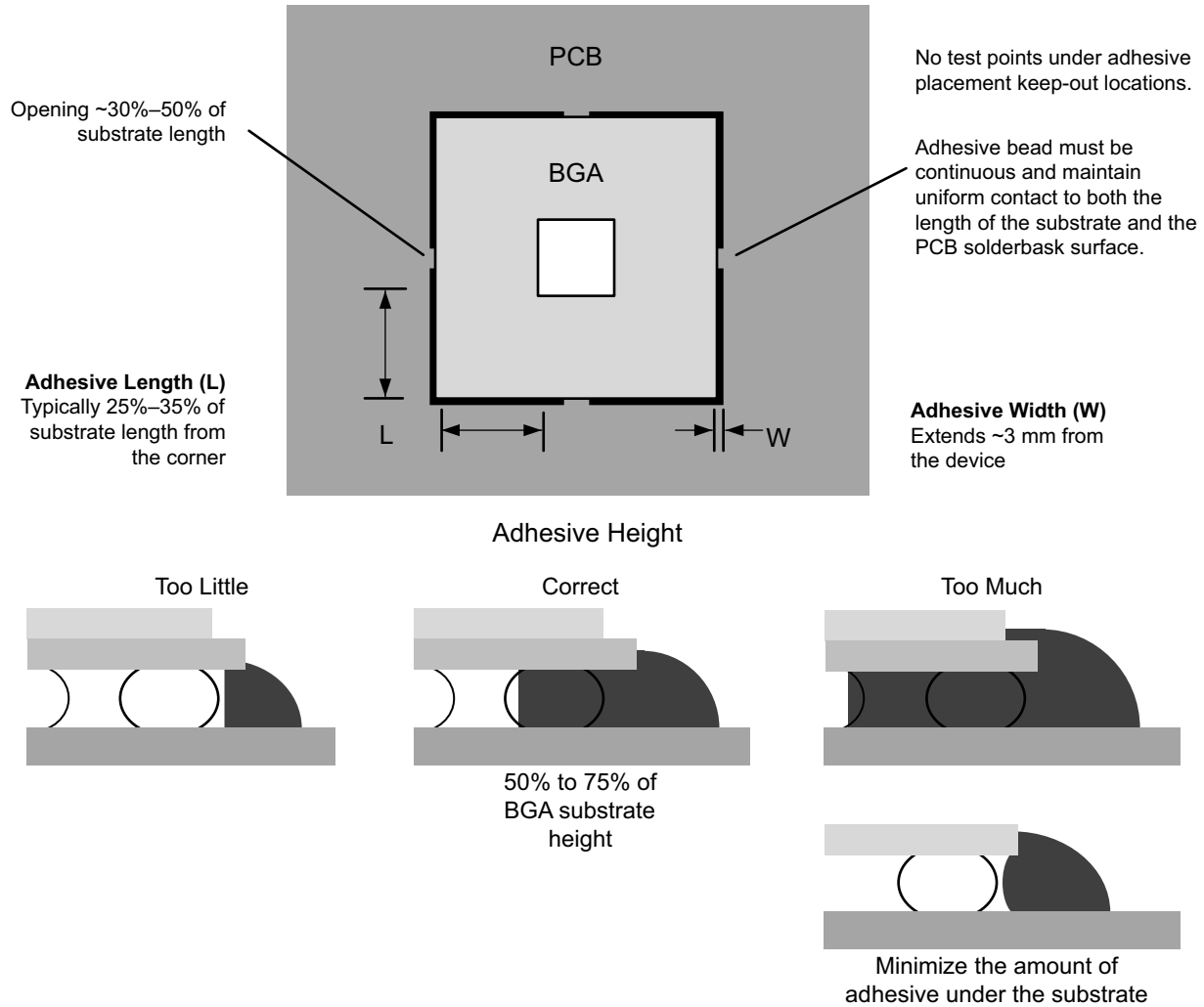


**IMPORTANT:** Some package devices have an overhang substrate that can result in the first row of the BGA not being covered by edge-bonding material. In other scenarios, the first BGA row could cover up to 90% of the BGA. See the following scenarios.



X27880-092424

Figure 10-2: Edge Bonding Scenarios



X23146-041322

Figure 10-3: Edge Bonding Adhesive Placement Parameters



**RECOMMENDED:** Curing condition of the [Zymet UA-2605-B](#) edge-bonding material is 140°C for 5 minutes.

## Component Clearance Surrounding Edge Bond

An adjacent component clearance surrounding the AMD device is necessary to have the 30° to 45° angle required by the for the edge bond dispenser to dispense the edge bond adhesive material. The surrounding component height and distance from the device is validated based on each unique product design layout.

## Edge Bond Removal

Edge bond material can be removed by heating to 170–180°C, and scraping using a stiff probe made of stable organic material such as a non-resinous wood or Teflon. Use a hot air blower on the edge bond area and slowly remove the edge bond adhesive from side to side. Do not use force to remove the edge bond adhesive. Excess adhesive on the PCB can be removed using a chisel-tip soldering iron, with sufficient precautions to limit damage to the PCB surface.

## Underfill Guidelines

To meet the mechanical reliability standards for most applications, high-adhesion underfill between the package and the PCB is required for all InFO packages (e.g., UBVA530). This allows for improved robustness of the mounted component by controlling the expansion and warpage of the package and board during normal operating conditions. The following sections detail the recommended implementation of underfill on a pre-mounted InFO package.

### Underfill Implementation

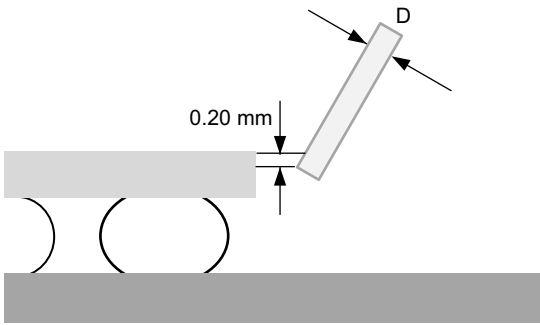
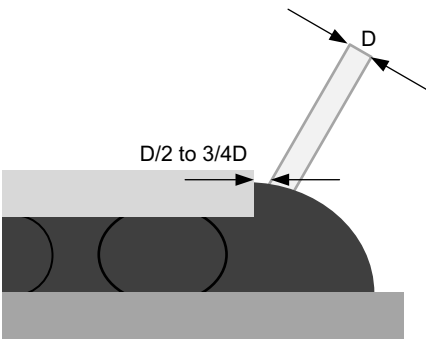
The recommended underfill process comprises of dispensing an epoxy material along one side of the package after board mount and allowing flow by way of capillary action through the BGA field. Based on the evaluation, the recommended dispensing pattern and process are detailed in the following tables.

**Note:** Underfill recommendations are based on evaluation with AMD devices using LOCTITE® ECCOBOND UF 3812 epoxy underfill.

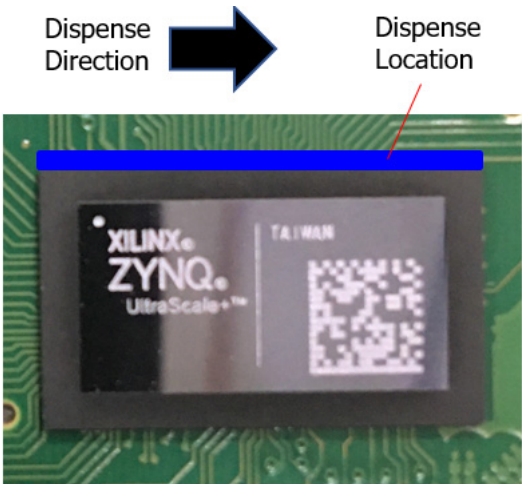
Table 10-2: Underfill Pattern

| Dispensing Pattern              | Multiple-Pass Variable Length                                                                   |
|---------------------------------|-------------------------------------------------------------------------------------------------|
| Dispensing length               | 75% & 100% of package body length                                                               |
| Dispensing speed                | 15 mm/sec                                                                                       |
| Number of passes                | 4                                                                                               |
| Pass number and dispense length | Pass 1 & 2: 75% of package body length<br>Pass 3 & 4: 100% of package body length               |
| Interval between each pass      | Between pass 1 & 2: 4 seconds<br>Between Pass 2 & 3: 6 seconds<br>Between Pass 3 & 4: 9 seconds |

Table 10-3: Underfill Process Parameters

| Process Parameter     | Range Specification                                                                                                                                                                                                                                 |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Needle size           | Range: 25—20 gauge<br>Recommended: 23 gauge. Needle diameter (D) is 0.64mm                                                                                                                                                                          |
| Needle height         | Range: Above the device edge midpoint, or 0 to 0.2 mm below the device top surface<br>Recommended: 0.2 mm from the top surface of the device<br><br>X27743-020823 |
| Needle edge spacing   | Range: Half to three quarters of the needle outer diameter (D)<br>Recommendation: D/2, half of the needle diameter, approximately 0.32 mm<br><br>X27744-020823   |
| Dispense needle speed | Range: 0.1 to 200 mm/sec<br>Recommendation: 15 mm/sec                                                                                                                                                                                               |
| Valve pressure        | Range: 10 to 60 psi<br>Recommendation: 14.5 psi                                                                                                                                                                                                     |

The following image is an example of underfill adhesive placement on a typical InFo package.



X27745-020823

Figure 10-4: Underfill Dispensing Location



**RECOMMENDED:** Curing time and temperature varies by the type of underfill used. Based on evaluation, oven curing temperature setting conditions are typically 155°C for 12 minutes. In this case, the temperature profile for the underfill material should be 150°C for 7 minutes.

## Underfill Keep-out Requirements

To ensure that underfill bleed-out does not impact surrounding components, the keep-out requirements shown in the following table must be considered.

Table 10-4: Underfill Keep-out Requirements

| Keep-Out Between Components            | Minimum Spacing (mm) |
|----------------------------------------|----------------------|
| Underfilled BGA to underfilled BGA     | 5.0                  |
| Underfilled BGA to non-underfilled BGA | 2.5                  |
| Underfilled BGA to passive components  | 2.5                  |

## Underfill Rework

The following steps detail the underfill rework process based on evaluation on a typical InFO package. This process is only possible with re-workable epoxy underfill and varies depending on the underfill type and manufacturer.

Required Instrumentation:

- Equipment: SRT machine, SRT nozzle, and pallet
- Materials: Tacky flux
- Hand tools: Tweezers, steel probe with round pointed tip, solder wick, and cotton swab



X27746-020823

Figure 10-5: Underfill Rework Tools

### Step 1: Pre-bake

Boards are required to bake at least 4 hours at 125°C to avoid any moisture induced failure during the rework process.

**Step 2: SRT Machine Program Creation**

An SRT machine is highly recommended for the underfill rework process. An SRT machine allows you to control temperature and time at multiple stages. The underfill rework program for an SRT machine needs to be created with three stages, shown in the following table. The bottom heater temperature should be set at 150°C for all stages to allow efficient ramp time, control board warping, and minimize unnecessary heating of neighboring components.

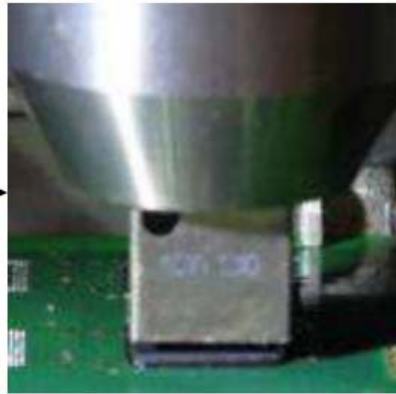
Table 10-5: Underfill Rework SRT Machine Program

| Stage   | Nozzle Temperature | Time (seconds) | Description                                                      |
|---------|--------------------|----------------|------------------------------------------------------------------|
| Stage 1 | 200°C              | 100            | Pre-heating and underfill fillet removal engulfing the component |
| Stage 2 | 220°C to 230°C     | 100            | Component Removal                                                |
| Stage 3 | 200°C to 225°C     | 150            | Rework site cleaning—scrape underfill residue                    |



**Step 3: Machine and Board Setup**

- a. Select and load the program. Measure the thermal profile prior to underfill rework to validate the program is within specifications.
- b. Use the pallet to clamp and secure the board position on the SRT machine. Sufficient support is needed to prevent the board from flexing or warping during rework.
- c. Assemble the nozzle to the SRT machine top heater. Use a nozzle that is slightly larger (+1mm) than the component on all sides. This is to allow even heat and air flow to the component and to control excess heat exposure to nearby components. Thermal shielding can also be applied to nearby component to minimize excess heat.
- d. To begin the pre-heating process, lower the SRT nozzle to the top of the rework surface (2 mm to 3 mm above), as shown in the following figure.



X27751-020923

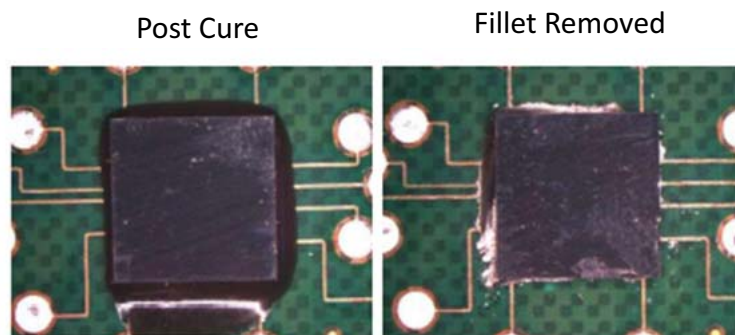
**Figure 10-6: SRT Nozzle Lowered 2 mm to 3 mm from Component Top Surface**

**Step 4 (Stage 1): Pre-Heating**

During pre-heating, allow the component to reach 200°C. Use non-abrasive tools (a wooden probe) to scrape off the underfill fillet around the component. If using a steel probe with a round pointed tip, ensure that the tip is directed away from the component side wall to prevent any damage to the solder mask.



Figure 10-7: Removing Underfill Using Steel Probe



X27753-020923

Figure 10-8: Removing the Underfill Fillet (Before and After)

**Step 5 (Stage 2): Component Removal**

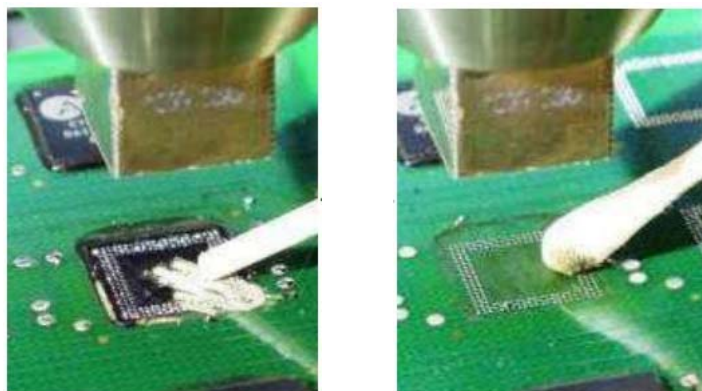
After underfill fillet removal is complete, ramp up the temperature above 220°C prior to component removal. Considering that the solder paste (SAC305) melting point is from 217°C to 220°C, ensure the rework component achieves an even temperature of 220°C or above to avoid potential defects such as pad lifting.



Figure 10-9: Component Removal

**Step 6 (Stage 3): Rework Site Cleaning**

The final stage is rework site cleaning. After component removal, use a non-abrasive tool (wooden probe) to scrape off the underfill residue. Use a flux saturated cotton swab to pick up and clean the remaining underfill residue.



X27754-020923

Figure 10-10: Scrape Away Underfill Residue and Clean with a Flux Saturated Cotton Swab

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## Conformal Coating

AMD does not have information regarding the reliability of flip-chip BGA packages on a board after exposure to any specific conformal coating process. Therefore, any process using conformal coating should be qualified for the specific use case to cover the materials and process steps.

Ruggedized XQ packages are designed to support conformal coating, with vented lids that ensure proper cleaning can occur after the etching process and prior to conformal coating.



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**RECOMMENDED:** *When a conformal coating is required, Parylene-based material should be used to avoid potential risk of weakening the lid or stiffener ring adhesive used in AMD packages.*

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# Thermal Specifications

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## Introduction

Zynq™ UltraScale+™ devices are offered exclusively in thermally efficient flip-chip BGA packages. These flip-chip packages range in pin-count from the smaller 19 x 19 mm SBVA484 to the 45 x 45 mm FFVE1924. This suite of packages is used to address the various power requirements of the Zynq UltraScale+ devices. Zynq UltraScale+ devices are implemented in the 16 nm process technology.

Unlike features in an ASIC, the combination of Zynq UltraScale+ device features used in a user application is not known to the component supplier. Therefore, it remains a challenge for AMD to predict the power requirements of a given Zynq UltraScale+ device when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, AMD offers and supports a suite of integrated device power analysis tools to help users quickly and accurately estimate their design power requirements. Zynq UltraScale+ devices are supported similarly to previous products. The uncertainty of design power requirements makes it difficult to apply canned thermal solutions to fit all users. Therefore, AMD devices do not come with preset thermal solutions. Your design's operating conditions dictate the appropriate solution.

## Thermal Resistance Data

Table 11-1 shows the thermal resistance data for Zynq UltraScale+ devices (grouped in the packages offered). The data includes junction-to-ambient in still air, junction-to-case, and junction-to-board data based on standard JEDEC four-layer measurements.



**IMPORTANT:** The data in Table 11-1 is for device/package comparison purposes only. Attempts to recreate this data are only valid using the transient 2-phase measurement techniques outlined in JESD51-14. Do not use these values for thermal simulations. Use the [Package Thermal Models](#).



**TIP:** The thermal data query for all available devices by package is available on the AMD website: [www.xilinx.com/cgi-bin/thermal/thermal.pl](http://www.xilinx.com/cgi-bin/thermal/thermal.pl).



**IMPORTANT:** All non-InFO packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC or XA, and the Pb-free signifier in the package name is Q (for example: FFQE1156). Refer to the Pb-free version of these packages for their thermal resistance data and thermal models.

Table 11-1: Thermal Resistance Data

| Package | Package Body Size | Devices | $\theta_{JB}^{(1)}$<br>(°C/W) | $\theta_{JC}^{(1)}$<br>(°C/W) | $\theta_{JA}^{(1)}$<br>(°C/W) | $\theta_{JA\text{-Effective}}^{(2)}$ (°C/W) |          |          |
|---------|-------------------|---------|-------------------------------|-------------------------------|-------------------------------|---------------------------------------------|----------|----------|
|         |                   |         |                               |                               |                               | @250 LFM                                    | @500 LFM | @750 LFM |
| SBVA484 | 19 x 19           | XCZU1   | 3.35                          | 0.09                          | 16.9                          | 12.5                                        | 10.5     | 9.7      |
|         |                   | XCZU2   | 2.46                          | 0.06                          | 14.9                          | 11.5                                        | 9.6      | 8.9      |
|         |                   | XCZU3   | 2.46                          | 0.06                          | 14.9                          | 11.5                                        | 9.6      | 8.9      |
|         |                   | XAZU1EG | 3.35                          | 0.09                          | 16.9                          | 12.5                                        | 10.5     | 9.7      |
|         |                   | XAZU2EG | 2.46                          | 0.06                          | 14.9                          | 11.5                                        | 9.6      | 8.9      |
|         |                   | XAZU3EG | 2.46                          | 0.06                          | 14.9                          | 11.5                                        | 9.6      | 8.9      |
| SFRA484 | 19 x 19           | XQZU3EG | 2.70                          | 0.43                          | 15.3                          | 11.7                                        | 9.8      | 9.1      |
| UBVA494 | 15 x 9.5          | XCZU1   | 2.28                          | 0.03                          | 22.4                          | 19.7                                        | 16.5     | 15.0     |
| UBVA530 | 16 x 9.5          | XCZU2   | 2.28                          | 0.03                          | 22.4                          | 19.7                                        | 16.5     | 15.0     |
|         |                   | XCZU3   | 2.28                          | 0.03                          | 22.4                          | 19.7                                        | 16.5     | 15.0     |
| SFVA625 | 21 x 21           | XCZU1   | 2.58                          | 0.52                          | 13.8                          | 10.2                                        | 8.6      | 8.0      |
|         |                   | XCZU2   | 2.22                          | 0.38                          | 13.2                          | 9.9                                         | 8.3      | 7.8      |
|         |                   | XCZU3   | 2.22                          | 0.38                          | 13.2                          | 9.9                                         | 8.3      | 7.8      |
|         |                   | XAZU1EG | 2.58                          | 0.52                          | 13.8                          | 10.2                                        | 8.6      | 8.0      |
|         |                   | XAZU2EG | 2.22                          | 0.38                          | 13.2                          | 9.9                                         | 8.3      | 7.8      |
|         |                   | XAZU3EG | 2.22                          | 0.38                          | 13.2                          | 9.9                                         | 8.3      | 7.8      |

Table 11-1: Thermal Resistance Data (Cont'd)

| Package  | Package Body Size | Devices  | $\theta_{JB}^{(1)}$<br>(°C/W) | $\theta_{JC}^{(1)}$<br>(°C/W) | $\theta_{JA}^{(1)}$<br>(°C/W) | $\theta_{JA\text{-Effective}}^{(2)}$ (°C/W) |          |          |
|----------|-------------------|----------|-------------------------------|-------------------------------|-------------------------------|---------------------------------------------|----------|----------|
|          |                   |          |                               |                               |                               | @250 LFM                                    | @500 LFM | @750 LFM |
| SFVC784  | 23 x 23           | XCZU1    | 2.50                          | 0.49                          | 12.5                          | 9.1                                         | 7.6      | 7.1      |
|          |                   | XCZU2    | 2.67                          | 0.50                          | 12.8                          | 9.2                                         | 7.8      | 7.2      |
|          |                   | XCZU3    | 2.67                          | 0.50                          | 12.8                          | 9.2                                         | 7.8      | 7.2      |
|          |                   | XCZU4    | 2.28                          | 0.27                          | 12.2                          | 8.9                                         | 7.4      | 7.0      |
|          |                   | XCZU5    | 2.28                          | 0.27                          | 12.2                          | 8.9                                         | 7.4      | 7.0      |
|          |                   | XAZU1EG  | 2.50                          | 0.49                          | 12.5                          | 9.1                                         | 7.6      | 7.1      |
|          |                   | XAZU2EG  | 2.67                          | 0.50                          | 12.8                          | 9.2                                         | 7.8      | 7.2      |
|          |                   | XAZU3EG  | 2.67                          | 0.50                          | 12.8                          | 9.2                                         | 7.8      | 7.2      |
|          |                   | XAZU4EV  | 2.28                          | 0.27                          | 12.2                          | 8.9                                         | 7.4      | 7.0      |
|          |                   | XAZU5EV  | 2.28                          | 0.27                          | 12.2                          | 8.9                                         | 7.4      | 7.0      |
| SFVE784  | 23 x 23           | XCZU4    | 2.28                          | 0.27                          | 12.2                          | 8.9                                         | 7.4      | 7.0      |
|          |                   | XCZU5    | 2.28                          | 0.27                          | 12.2                          | 8.9                                         | 7.4      | 7.0      |
| SFRC784  | 23 x 23           | XQZU3EG  | 2.44                          | 0.42                          | 12.4                          | 9.0                                         | 7.6      | 7.1      |
|          |                   | XQZU5EV  | 2.26                          | 0.27                          | 12.1                          | 8.9                                         | 7.4      | 7.0      |
| FBVB900  | 31 x 31           | XCZU4    | 2.62                          | 0.04                          | 9.6                           | 6.3                                         | 5.3      | 5.0      |
|          |                   | XCZU5    | 2.62                          | 0.04                          | 9.6                           | 6.3                                         | 5.3      | 5.0      |
|          |                   | XCZU7    | 2.32                          | 0.03                          | 9.2                           | 6.1                                         | 5.1      | 4.8      |
|          |                   | XAZU7    | 2.32                          | 0.03                          | 9.2                           | 6.1                                         | 5.1      | 4.8      |
| FFRB900  | 31 x 31           | XQZU5EV  | 2.26                          | 0.27                          | 9.1                           | 6.1                                         | 5.1      | 4.8      |
|          |                   | XQZU7EV  | 2.14                          | 0.19                          | 8.9                           | 6.0                                         | 5.0      | 4.8      |
| FFVC900  | 31 x 31           | XCZU6    | 2.33                          | 0.25                          | 9.2                           | 6.1                                         | 5.1      | 4.9      |
|          |                   | XCZU9    | 2.33                          | 0.25                          | 9.2                           | 6.1                                         | 5.1      | 4.9      |
|          |                   | XCZU15   | 2.25                          | 0.18                          | 9.1                           | 6.1                                         | 5.1      | 4.8      |
| FFRC900  | 31 x 31           | XQZU9EG  | 2.10                          | 0.18                          | 8.9                           | 6.0                                         | 5.0      | 4.7      |
|          |                   | XQZU15EG | 2.07                          | 0.17                          | 8.9                           | 6.0                                         | 5.0      | 4.7      |
| FFVB1156 | 35 x 35           | XCZU6    | 2.40                          | 0.20                          | 8.3                           | 5.3                                         | 4.5      | 4.2      |
|          |                   | XCZU9    | 2.40                          | 0.20                          | 8.3                           | 5.3                                         | 4.5      | 4.2      |
|          |                   | XCZU15   | 2.09                          | 0.23                          | 7.9                           | 5.1                                         | 4.3      | 4.1      |
| FFRB1156 | 35 x 35           | XQZU9EG  | 2.09                          | 0.18                          | 7.9                           | 5.1                                         | 4.3      | 4.1      |
|          |                   | XQZU15EG | 2.06                          | 0.17                          | 7.9                           | 5.1                                         | 4.3      | 4.1      |
| FFVC1156 | 35 x 35           | XCZU7    | 2.39                          | 0.21                          | 8.3                           | 5.3                                         | 4.5      | 4.2      |
|          |                   | XCZU11   | 2.20                          | 0.16                          | 8.0                           | 5.2                                         | 4.3      | 4.1      |
| FFRC1156 | 35 x 35           | XQZU7EV  | 2.12                          | 0.19                          | 7.9                           | 5.2                                         | 4.3      | 4.1      |
|          |                   | XQZU11EG | 2.01                          | 0.15                          | 7.8                           | 5.1                                         | 4.3      | 4.1      |

Table 11-1: Thermal Resistance Data (Cont'd)

| Package  | Package Body Size | Devices  | $\theta_{JB}^{(1)}$<br>(°C/W) | $\theta_{JC}^{(1)}$<br>(°C/W) | $\theta_{JA}^{(1)}$<br>(°C/W) | $\theta_{JA\text{-Effective}}^{(2)}$ (°C/W) |          |          |
|----------|-------------------|----------|-------------------------------|-------------------------------|-------------------------------|---------------------------------------------|----------|----------|
|          |                   |          |                               |                               |                               | @250 LFM                                    | @500 LFM | @750 LFM |
| FFVD1156 | 35 x 35           | XCZU21DR | 1.94                          | 0.16                          | 7.8                           | 5.1                                         | 4.2      | 4.0      |
| FFRD1156 | 35 x 35           | XQZU21DR | 1.94                          | 0.16                          | 7.8                           | 5.1                                         | 4.2      | 4.0      |
| FFVE1156 | 35 x 35           | XCZU25DR | 1.94                          | 0.16                          | 7.8                           | 5.1                                         | 4.2      | 4.0      |
|          |                   | XCZU27DR | 1.94                          | 0.16                          | 7.8                           | 5.1                                         | 4.2      | 4.0      |
|          |                   | XCZU28DR | 1.94                          | 0.16                          | 7.8                           | 5.1                                         | 4.2      | 4.0      |
|          |                   | XCZU42DR | 1.94                          | 0.16                          | 7.8                           | 5.1                                         | 4.2      | 4.0      |
|          |                   | XCZU43DR | 1.94                          | 0.16                          | 7.8                           | 5.1                                         | 4.2      | 4.0      |
|          |                   | XCZU47DR | 1.94                          | 0.16                          | 7.8                           | 5.1                                         | 4.2      | 4.0      |
|          |                   | XCZU48DR | 1.94                          | 0.16                          | 7.8                           | 5.1                                         | 4.2      | 4.0      |
|          |                   | XCZU63DR | 1.94                          | 0.16                          | 7.8                           | 5.1                                         | 4.2      | 4.0      |
|          |                   | XCZU64DR | 1.94                          | 0.16                          | 7.8                           | 5.1                                         | 4.2      | 4.0      |
|          |                   | XCZU65DR | 1.94                          | 0.16                          | 7.8                           | 5.1                                         | 4.2      | 4.0      |
|          |                   | XCZU67DR | 1.94                          | 0.16                          | 7.8                           | 5.1                                         | 4.2      | 4.0      |
| FFRE1156 | 35 x 35           | XQZU28DR | 1.93                          | 0.11                          | 7.7                           | 5.1                                         | 4.2      | 4.0      |
|          |                   | XQZU48DR | 1.94                          | 0.16                          | 7.8                           | 5.1                                         | 4.2      | 4.0      |
| FSVE1156 | 35 x 35           | XCZU25DR | 2.40                          | 0.02                          | 8.3                           | 5.3                                         | 4.4      | 4.2      |
|          |                   | XCZU27DR | 2.40                          | 0.02                          | 8.3                           | 5.3                                         | 4.4      | 4.2      |
|          |                   | XCZU28DR | 2.40                          | 0.02                          | 8.3                           | 5.3                                         | 4.4      | 4.2      |
|          |                   | XCZU42DR | 2.40                          | 0.02                          | 8.3                           | 5.3                                         | 4.4      | 4.2      |
|          |                   | XCZU43DR | 2.40                          | 0.02                          | 8.3                           | 5.3                                         | 4.4      | 4.2      |
|          |                   | XCZU47DR | 2.40                          | 0.02                          | 8.3                           | 5.3                                         | 4.4      | 4.2      |
|          |                   | XCZU48DR | 2.40                          | 0.02                          | 8.3                           | 5.3                                         | 4.4      | 4.2      |
|          |                   | XCZU63DR | 2.40                          | 0.02                          | 8.3                           | 5.3                                         | 4.4      | 4.2      |
|          |                   | XCZU64DR | 2.40                          | 0.02                          | 8.3                           | 5.3                                         | 4.4      | 4.2      |
|          |                   | XCZU65DR | 2.40                          | 0.02                          | 8.3                           | 5.3                                         | 4.4      | 4.2      |
|          |                   | XCZU67DR | 2.40                          | 0.02                          | 8.3                           | 5.3                                         | 4.4      | 4.2      |
| FFVB1517 | 40 x 40           | XCZU11   | 2.22                          | 0.16                          | 7.1                           | 4.4                                         | 3.7      | 3.5      |
|          |                   | XCZU17   | 2.17                          | 0.11                          | 7.0                           | 4.4                                         | 3.7      | 3.5      |
|          |                   | XCZU19   | 2.17                          | 0.11                          | 7.0                           | 4.4                                         | 3.7      | 3.5      |
| FFRB1517 | 40 x 40           | XQZU19EG | 1.90                          | 0.11                          | 6.8                           | 4.3                                         | 3.5      | 3.4      |
| FFVF1517 | 40 x 40           | XCZU7    | 2.38                          | 0.21                          | 7.3                           | 4.5                                         | 3.8      | 3.6      |
|          |                   | XCZU11   | 2.22                          | 0.16                          | 7.1                           | 4.4                                         | 3.7      | 3.5      |
|          |                   | XAZU11   | 2.22                          | 0.16                          | 7.1                           | 4.4                                         | 3.7      | 3.5      |



Table 11-1: Thermal Resistance Data (Cont'd)

| Package  | Package Body Size | Devices  | $\theta_{JB}^{(1)}$<br>(°C/W) | $\theta_{JC}^{(1)}$<br>(°C/W) | $\theta_{JA}^{(1)}$<br>(°C/W) | $\theta_{JA-Effective}^{(2)}$ (°C/W) |          |          |
|----------|-------------------|----------|-------------------------------|-------------------------------|-------------------------------|--------------------------------------|----------|----------|
|          |                   |          |                               |                               |                               | @250 LFM                             | @500 LFM | @750 LFM |
| FFVG1517 | 40 x 40           | XCZU25DR | 1.93                          | 0.16                          | 6.8                           | 4.3                                  | 3.6      | 3.4      |
|          |                   | XCZU27DR | 1.93                          | 0.16                          | 6.8                           | 4.3                                  | 3.6      | 3.4      |
|          |                   | XCZU28DR | 1.93                          | 0.16                          | 6.8                           | 4.3                                  | 3.6      | 3.4      |
|          |                   | XCZU43DR | 1.93                          | 0.16                          | 6.8                           | 4.3                                  | 3.6      | 3.4      |
|          |                   | XCZU47DR | 1.93                          | 0.16                          | 6.8                           | 4.3                                  | 3.6      | 3.4      |
|          |                   | XCZU48DR | 1.93                          | 0.16                          | 6.8                           | 4.3                                  | 3.6      | 3.4      |
| FFRG1517 | 40 x 40           | XQZU28DR | 1.93                          | 0.16                          | 6.8                           | 4.3                                  | 3.6      | 3.4      |
| FSRG1517 | 40 x 40           | XQZU48DR | 2.43                          | 0.02                          | 7.3                           | 4.5                                  | 3.8      | 3.6      |
| FSVG1517 | 40 x 40           | XCZU25DR | 2.43                          | 0.02                          | 7.3                           | 4.5                                  | 3.8      | 3.6      |
|          |                   | XCZU27DR | 2.43                          | 0.02                          | 7.3                           | 4.5                                  | 3.8      | 3.6      |
|          |                   | XCZU28DR | 2.43                          | 0.02                          | 7.3                           | 4.5                                  | 3.8      | 3.6      |
|          |                   | XCZU43DR | 2.43                          | 0.02                          | 7.3                           | 4.5                                  | 3.8      | 3.6      |
|          |                   | XCZU47DR | 2.43                          | 0.02                          | 7.3                           | 4.5                                  | 3.8      | 3.6      |
|          |                   | XCZU48DR | 2.43                          | 0.02                          | 7.3                           | 4.5                                  | 3.8      | 3.6      |
| FFVC1760 | 42.5 x 42.5       | XCZU11   | 1.96                          | 0.14                          | 6.4                           | 4.0                                  | 3.3      | 3.2      |
|          |                   | XCZU17   | 1.77                          | 0.10                          | 6.3                           | 3.9                                  | 3.2      | 3.1      |
|          |                   | XCZU19   | 1.77                          | 0.10                          | 6.3                           | 3.9                                  | 3.2      | 3.1      |
| FFRC1760 | 42.5 x 42.5       | XQZU11EG | 1.96                          | 0.14                          | 6.4                           | 4.0                                  | 3.3      | 3.2      |
|          |                   | XQZU19EG | 1.77                          | 0.10                          | 6.3                           | 3.9                                  | 3.2      | 3.1      |
| FFVD1760 | 42.5 x 42.5       | XCZU17   | 1.77                          | 0.10                          | 6.3                           | 3.9                                  | 3.2      | 3.1      |
|          |                   | XCZU19   | 1.77                          | 0.10                          | 6.3                           | 3.9                                  | 3.2      | 3.1      |
| FFVF1760 | 42.5 x 42.5       | XCZU29DR | 2.04                          | 0.17                          | 6.5                           | 4.0                                  | 3.3      | 3.2      |
|          |                   | XCZU39DR | 2.04                          | 0.17                          | 6.5                           | 4.0                                  | 3.3      | 3.2      |
|          |                   | XCZU49DR | 2.04                          | 0.17                          | 6.5                           | 4.0                                  | 3.3      | 3.2      |
| FFVH1760 | 42.5 x 42.5       | XCZU46DR | 2.04                          | 0.17                          | 6.5                           | 4.0                                  | 3.3      | 3.2      |
| FFRF1760 | 42.5 x 42.5       | XQZU29DR | 2.04                          | 0.17                          | 6.5                           | 4.0                                  | 3.3      | 3.2      |
| FSRF1760 | 42.5 x 42.5       | XQZU49DR | 2.47                          | 0.02                          | 7.0                           | 4.3                                  | 3.5      | 3.6      |
| FSVF1760 | 42.5 x 42.5       | XCZU29DR | 2.47                          | 0.02                          | 7.0                           | 4.3                                  | 3.5      | 3.6      |
|          |                   | XCZU39DR | 2.47                          | 0.02                          | 7.0                           | 4.3                                  | 3.5      | 3.6      |
|          |                   | XCZU49DR | 2.47                          | 0.02                          | 7.0                           | 4.3                                  | 3.5      | 3.6      |
| FSVH1760 | 42.5 x 42.5       | XCZU46DR | 2.47                          | 0.02                          | 7.0                           | 4.3                                  | 3.5      | 3.6      |

Table 11-1: Thermal Resistance Data (Cont'd)

| Package  | Package Body Size | Devices | $\theta_{JB}^{(1)}$<br>(°C/W) | $\theta_{JC}^{(1)}$<br>(°C/W) | $\theta_{JA}^{(1)}$<br>(°C/W) | $\theta_{JA-Effective}^{(2)}$ (°C/W) |          |          |
|----------|-------------------|---------|-------------------------------|-------------------------------|-------------------------------|--------------------------------------|----------|----------|
|          |                   |         |                               |                               |                               | @250 LFM                             | @500 LFM | @750 LFM |
| FFVE1924 | 45 x 45           | XCZU17  | 1.77                          | 0.10                          | 5.9                           | 3.6                                  | 3.0      | 2.9      |
|          |                   | XCZU19  | 1.77                          | 0.10                          | 5.9                           | 3.6                                  | 3.0      | 2.9      |

**Notes:**

1. This data is for device/package comparison purposes only. Attempts to recreate this data are only valid using the transient 2-phase measurement techniques outlined in JESD51-14. Do not use these values for thermal simulations. Use the [Package Thermal Models](#).
2. All  $\theta_{JA-Effective}$  values assume no heat sink and include thermal dissipation through a standard JEDEC four-layer board. The power estimation tools (Vivado™ Power Analysis, and XPE), which require detailed board dimensions and layer counts, are useful for deriving more precise  $\theta_{JA-Effective}$  values.

## Support for Thermal Models

Table 11-1 provides the traditional thermal resistance data for Zynq UltraScale+ devices. These resistances are measured using a prescribed JEDEC standard that might not necessarily reflect your actual board conditions and environment. The quoted  $\theta_{JA}$  and  $\theta_{JC}$  numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature prediction, these might not be enough, and a system-level thermal simulation might be required.

Though AMD continues to support these figures of merit data, for Zynq UltraScale+ devices, boundary conditions independent thermal resistor network (Delphi) models are offered for all Zynq UltraScale+ devices. These compact models seek to capture the thermal behavior of the packages more accurately at predetermined critical points (junction, case, top, leads, and so on) with the reduced set of nodes as illustrated in Figure 11-1.

Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. Delphi models are available for download on the AMD website (under the [Device Model tab](#)).

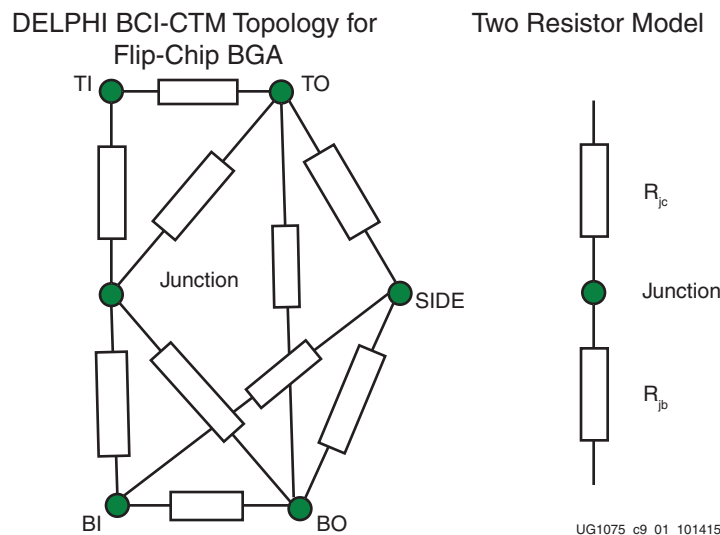


Figure 11-1: Thermal Model Topologies



**RECOMMENDED:** AMD recommends the use of the Delphi thermal model. AMD also recommends a best practice review of manufacturing variations on the thermal performance of the device from both the thermal interface material parameters and thermal solution variations. Examples of manufacture variations include the tolerance in airflow from a fan, the tolerance on performance of the heat pipe and vapor chamber, and manufacturing variations of the attachment of fins to the heat-sink base and the flatness of the surface.

# Thermal Management Strategy

## Introduction

As described in this section, AMD relies on a multi-pronged approach to consuming less power and dissipating heat for systems using Zynq™ UltraScale+™ devices.

## Flip-Chip Packages

Zynq UltraScale+ devices are offered in flip-chip BGA packages, which present a low thermal path. With the exception of the bare-die packages, the flip-chip BGA packages incorporate a heat spreader with an additional thermal interface material (TIM), as shown in [Figure 12-1](#).

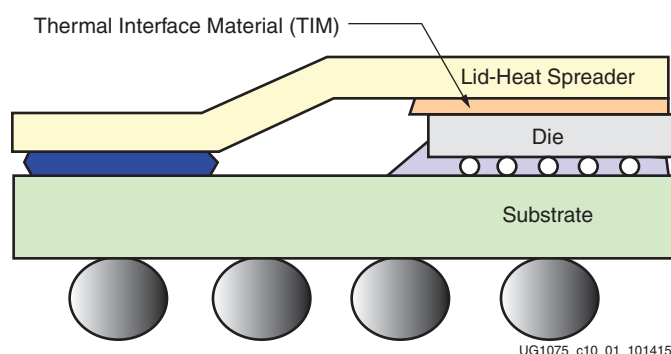


**Figure 12-1: Heat Spreader with Thermal Interface Material**

Materials with better thermal conductivity and consistent process deliver low thermal resistance to the heat spreader.

A parallel effort to ensure optimized package electrical return paths produces the added benefit of enhanced power and ground plane arrangement in the packages. A boost in copper density on the planes improves the overall thermal conductivity through the laminate. In addition, the extra dense and distributed via fields in the package increase the vertical thermal conductivity.

## System Level Heat Sink Solutions

To complete a comprehensive thermal management strategy, an overall thermal budget that includes custom or OEM heat sink solutions depends on the physical and mechanical constraints of the system. A heat-sink solution, managed by the system-level designer, should be tailored to the design and specific system constraints. This includes understanding the inherent device capabilities for delivering heat to the surface.

By considering the system's physical, mechanical, and environmental constraints, the overall thermal budget is maintained and does not exceed the device's maximum operating temperature. The heat sink is an integral part of the thermal management solution to maintain a safe operating temperature. As a result, the system-level designer must be aware of the following:

- For lidless packages, the nominal stiffener height can be different from the height of the die. Therefore, the heat sink must have an island to contact the die.
- Especially for lidless packages, AMD advises against direct use of the  $\theta_{JC}$  parameters (see [Table 11-1](#)) to determine the thermal performance of the device in your application. The calculation of these parameters are done in accordance with the JEDEC standard JESD51 where system parameters differ greatly from most applications. Instead, run thermal simulations of the system in worst-case environmental conditions using Delphi thermal models, which more accurately represent the device thermal performance under all boundary conditions.
- Consider the mechanical specifications of the package as well as the selection of the thermal interface between the die and the thermal management solution to ensure the lowest thermal contact resistance.
- The total thermal contact of the thermal interface material is determined based on parameters from the thermal interface supplier's data sheet.
- See the applied pressure recommendation on [page 324](#). Lower pressure runs the risk of poor thermal contact and higher pressure runs the risk of damaging the device; therefore, strict control of pressure is required.
- Consider all uncertainties in thermal modeling, including manufacturing variations from the thermal solutions (for example, fan airflow tolerance, heat pipe or vapor chamber performance tolerance, variation of the attachment of fins to heat sink base, and surface flatness).

## Thermal Interface Material

When installing heat sinks for Zynq UltraScale+ devices, a suitable thermal interface material (TIM) must be used. This thermal material significantly aids the transfer of heat from the component to the heat sink.

For bare-die flip-chip BGAs, the surface of the silicon contacts the heat sink. For lidded flip-chip BGAs, the lid contacts the heat sink. The surface size of the bare-die flip-chip BGA and lidded flip-chip BGAs are different. AMD recommends a different type of thermal material for long-term use with each type of flip-chip BGAs package.

Thermal interface material is needed because even the largest heat sink and fan cannot effectively cool an Zynq UltraScale+ device unless there is good physical contact between the base of the heat sink and the top of the Zynq UltraScale+ device. The surfaces of both the heat sink and the Zynq UltraScale+ device silicon are not absolutely smooth. This surface roughness is observed when examined at a microscopic level. Because surface roughness reduces the effective contact area, attaching a heat sink without a thermal interface material is not sufficient due to inadequate surface contact.

A thermal interface material such as phase-change material, thermal grease, or thermal pads fills these gaps and allows effective transference of heat between the Zynq UltraScale+ device die and the heat sink.

The selection of the thermal interface (TIM) between the package and the thermal management solution is critical to ensure the lowest thermal contact resistance. Therefore, the following parameters must be considered.

1. The flatness of the lid and the flatness of the contact surface of the thermal solution.
2. The applied pressure of the thermal solution on the package, which must be within the allowable maximum pressure that can be applied on the package.
3. The total thermal contact of the thermal interface material. This value is determined based on the parameters in [step 1](#) and [step 2](#), which are published in the data sheet of the thermal interface supplier.

## Types of TIM

There are many type of TIM available for sale. The most commonly used thermal interface materials are listed.

- Thermal grease
- Thermal pads
- Phase change material
- Thermal paste
- Thermal adhesives
- Thermal tape

## Guidelines for Thermal Interface Materials

Five factors affect the choice, use, and performance of the interface material used between the processor and the heat sink:

- [Thermal Conductivity of the Material](#)
- [Electrical Conductivity of the Material](#)
- [Spreading Characteristics of the Material](#)
- [Long-Term Stability and Reliability of the Material](#)
- [Ease of Application](#)
- [Applied Pressure from Heat Sink to the Package via Thermal Interface Materials](#)

### ***Thermal Conductivity of the Material***

Thermal conductivity is the quantified ability of any material to transfer heat. The thermal conductivity of the interface material has a significant impact on its thermal performance. The higher the thermal conductivity, the more efficient the material is at transferring heat. Materials that have a lower thermal conductivity are less efficient at transferring heat, causing a higher temperature differential to exist across the interface. To overcome this less efficient heat transfer, a better cooling solution (typically, a more costly solution) must be used to achieve the desired heat dissipation.

### ***Electrical Conductivity of the Material***

Some metal-based TIM compounds are electrically conductive. Ceramic-based compounds are typically not electrically conductive. Manufacturers produce metal-based compounds with low-electrical conductivity, but some of these materials are not completely electrically inert. Metal-based thermal compounds are not hazardous to the Zynq UltraScale+ device die itself, but other elements on the Zynq UltraScale+ device or motherboard can be at risk

if they become contaminated by the compound. For this reason, AMD does not recommend the use of electrically conductive thermal interface material.

### ***Spreading Characteristics of the Material***

The spreading characteristics of the thermal interface material determines its ability, under the pressure of the mounted heat sink, to spread and fill in or eliminate the air gaps between the Zynq UltraScale+ device and the heat sink. Because air is a very poor thermal conductor, the more completely the interface material fills the gaps, the greater the heat transference.

### ***Long-Term Stability and Reliability of the Material***

The long-term stability and reliability of the thermal interface material is described as the ability to provide a sufficient thermal conductance even after an extended time or extensive. Low-quality compounds can harden or leak out over time (the pump-out effect), leading to overheating or premature failure of the Zynq UltraScale+ device. High-quality compounds provide a stable and reliable thermal interface material throughout the lifetime of the device. Thermal greases with higher viscosities are typically more resistant to pump out effects on bare-die devices.

### ***Ease of Application***

A spreadable thermal grease requires the surface mount supplier to carefully use the appropriate amount of material. Too much or too little material can cause problems. The thermal pad is a fixed size and is therefore easier to apply in a consistent manner.

### ***Applied Pressure from Heat Sink to the Package via Thermal Interface Materials***



**IMPORTANT:** *The following table shows the required applied pressure on the thermal interface material (TIM) between the package and the heat sink. Thermocouples should not be present between the package and the heat sink, as their presence will degrade the thermal contact and result in incorrect thermal measurements. The best practice is to select the appropriate pressure for the optimum thermal contact performance between the package and the thermal system solution, and the mechanical integrity of the package (with the thermal solution to pass all mechanical stress and vibration qualification tests).*

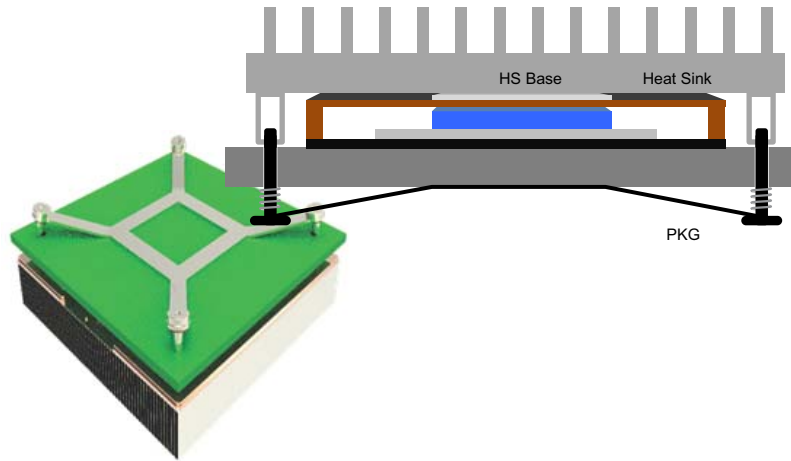
**Table 12-1: Required Applied Pressure by Package Type**

| Package Type                  | Supported Pressure Range (PSI)   |
|-------------------------------|----------------------------------|
| 0.8 mm and 1.0 mm pitch       | 20 to 50 PSI                     |
| InFO packages (e.g., UBVA530) | 3 to 20 PSI (underfill required) |





**RECOMMENDED:** AMD recommends using dynamic mounting around the four corners of the device package. On the PCB, use a bracket clip as part of the heat sink attachment to provide mechanical package support. See [Figure 12-2](#).



X15431-111316

Figure 12-2: Dynamic Mounting and Bracket Clips on Heat Sink Attachment

## Heat Sink Removal

When removing or reworking heat sinks, the phase-change material residue must be removed from the surface of the die. Laird Technologies, Inc. provides the following guidance for complete removal of the phase-change material from the component.

### Instructions for Removal of Phase-change Material

1. [Separate the Components](#)
2. [Scrape Away Thick Residue](#)
3. [Clean Remaining Residue with Solvent](#)
4. [Working with Laird Material](#)

#### ***Separate the Components***

At room temperature, if possible, use a back and forth twisting motion to break the bond between the phase-change thermal interface material and mated components (i.e., heat sink and Zynq UltraScale+ device). See [Figure 12-3](#).

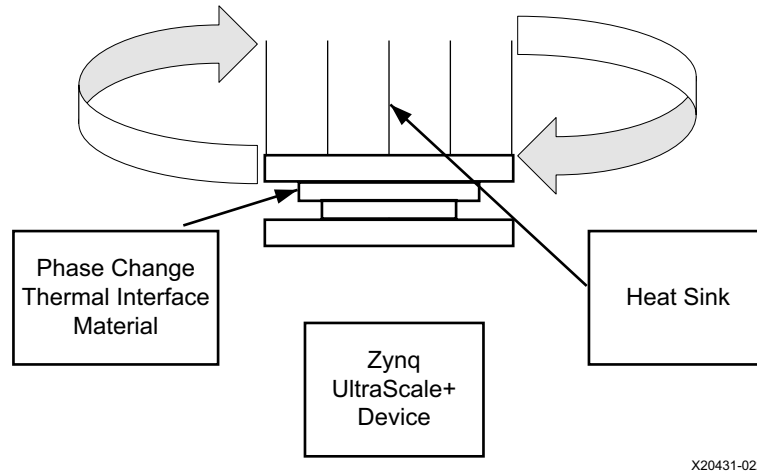


**Figure 12-3: Breaking the Bond between Thermal Interface Material and Mated Components**

For smaller components (typically 15 mm x 15 mm or less), the bond usually breaks free easily at room temperature. For larger components, in situations where minimal movement is available, or if using fragile components, heat the component (preferred) or heat sink to about 40°C–60°C before removal.

The guideline is 40°C–60°C, however, you might find that for your application, heating to 35°C is adequate. You might prefer to heat to 70°C which makes the phase-change thermal interface material very soft and the components can be easily separated.

### ***Scrape Away Thick Residue***

For a faster clean-up once components are separated, scrape away any large residual material amounts with a plastic spatula or a wooden tongue depressor. A clean dry rag can be used to wipe away excess material.

### ***Clean Remaining Residue with Solvent***

Using a clean cloth/wipe, wet it with your choice of solvent (see the following list) and wipe away any remaining residue.

- Toluene (easiest)
- Acetone (very good)
- Isoparaffinic hydrocarbon: Isopar, Soltrol (trade names) (very good)
- Isopropyl alcohol (OK)

### ***Working with Laird Material***

Safe handling, disposal, and first-aid measures for working with phase-change material are included in the Laird Technologies material safety data sheet (MSDS). Read the MSDS before using or handling. See the Laird Technologies, Inc. website, [www.lairdtech.com](http://www.lairdtech.com).

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## **Measurement Debug**

When performing in-system thermal testing, to ensure accurate data and not incur damage to the device, do not place a thermocouple in between the device and the heat sink. On the extreme side, it might cause additional mechanical and/or thermal stress to the device, leading to damage. Even if damage does not occur, it often leads to a thicker and or uneven thermal interface material thickness, leading to a thermal performance difference from a system without a thermocouple. To obtain the device temperature, use the System Monitor as a non-invasive means to get accurate device measurements while debugging the system.

# Heat Sink Guidelines for Bare-die Flip-Chip Packages

## Heat Sink Attachments for Bare-die FB Packages

Heat sinks can be attached to the package in multiple ways. For heat to dissipate effectively, the advantages and disadvantages of each heat sink attachment method must be considered. Factors influencing the selection of the heat sink attachment method include the package type, contact area of the heat source, and the heat sink type.

### Silicon and Decoupling Capacitors Height Consideration

When designing heat sink attachments for bare-die flip-chip BGA packages, the height of the die above the substrate and also the height of decoupling capacitors must be considered (Figure 13-1). This is to prevent electrical shorting between the heat sink (metal) and the decoupling capacitors.

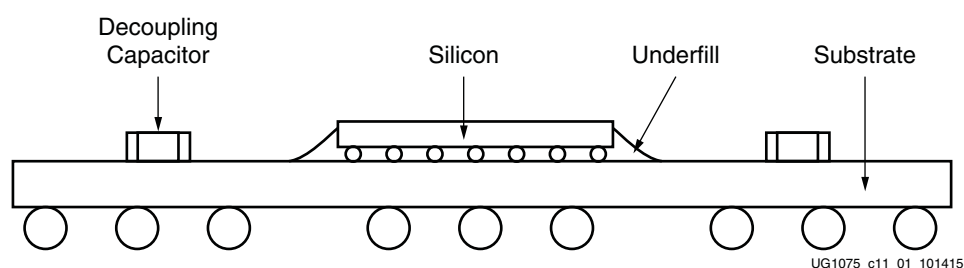


Figure 13-1: Cross Section of Bare-die Flip-chip BGA

# Types of Heat Sink Attachments

There are six main methods for heat sink attachment. [Table 13-1](#) lists their advantages and disadvantages.

- [Thermal tape](#)
- [Thermally conductive adhesive or glue](#)
- [Wire form Z-clips](#)
- [Plastic clip-ons](#)
- [Threaded stand-offs \(PEMs\) and compression springs](#)
- [Push-pins and compression springs](#)

Table 13-1: Heat Sink Attachment Methods

| Attachment Method                     | Advantages                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Disadvantages                                                                                                                                                                                                                                                                                                                                           |
|---------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Thermal tape                          | <ul style="list-style-type: none"><li>• Generally easy to attach and is inexpensive.</li><li>• Lowest cost approach for aluminum heat sink attachment.</li><li>• No additional space required on the PCB.</li></ul>                                                                                                                                                                                                                                                                              | <ul style="list-style-type: none"><li>• The surfaces of the heat sink and the chip must be very clean to allow the tape to bond correctly.</li><li>• Because of the small contact area, the tape might not provide sufficient bond strength.</li><li>• Tape is a moderate to low thermal conductor that could affect the thermal performance.</li></ul> |
| Thermally conductive adhesive or glue | <ul style="list-style-type: none"><li>• Outstanding mechanical adhesion.</li><li>• Fairly inexpensive, costs a little more than tape.</li><li>• No additional space required on the PCB.</li></ul>                                                                                                                                                                                                                                                                                               | <ul style="list-style-type: none"><li>• Adhesive application process is challenging and it is difficult to control the amount of adhesive to use.</li><li>• Difficult to rework.</li><li>• Because of the small contact area, the adhesive might not provide sufficient bond strength.</li></ul>                                                        |
| Wire form Z-clips                     | <ul style="list-style-type: none"><li>• It provides a strong and secure mechanical attachment. In environments that require shock and vibration testing, this type of strong mechanical attachment is necessary.</li><li>• Easy to apply and remove. Does not cause the semiconductors to be destroyed (epoxy and occasionally tape can destroy the device).</li><li>• It applies a preload onto the thermal interface material (TIM). Pre-loads actually improve thermal performance.</li></ul> | <ul style="list-style-type: none"><li>• Requires additional space on the PCB for anchor locations.</li></ul>                                                                                                                                                                                                                                            |

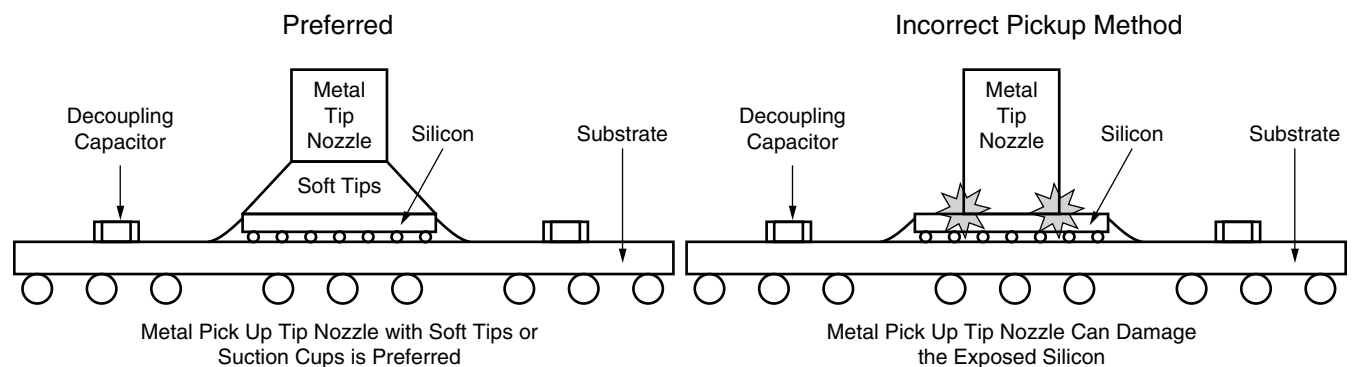
Table 13-1: Heat Sink Attachment Methods (Cont'd)

| Attachment Method                                  | Advantages                                                                                                                                                                                                                                                                                                               | Disadvantages                                                                                                                                                                                                                                                         |
|----------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Plastic clip-ons                                   | <ul style="list-style-type: none"> <li>Suitable for designs where space on the PCB is limited.</li> <li>Easy to rework by allowing heat sinks to be easily removed and reapplied without damaging the PCB board.</li> <li>Can provide a strong enough mechanical attachment to pass shock and vibration test.</li> </ul> | <ul style="list-style-type: none"> <li>Needs a keep out area around the silicon devices to use the clip.</li> <li>Caution is required when installing or removing clip-ons because localized stress can damage the solder balls or chip substrate.</li> </ul>         |
| Threaded stand-offs (PEMs) and compression springs | <ul style="list-style-type: none"> <li>Provides stable attachments to heat source and transfers load to the PCB, backing plate, or chassis.</li> <li>Suitable for high mass heat sinks.</li> <li>Allows for tight control over mounting force and load placed on chip and solder balls.</li> </ul>                       | <ul style="list-style-type: none"> <li>Holes are required in the PCB taking valuable space that can be used for trace lines.</li> <li>Tends to be expensive, especially since holes need to be drilled or predrilled onto the PCB board to use stand-offs.</li> </ul> |
| Push-pins and compression springs                  | <ul style="list-style-type: none"> <li>Provides a stable attachment to a heat source and transfers load to the PCB.</li> <li>Allows for tight control over mounting force and load placed on chip and solder balls.</li> </ul>                                                                                           | <ul style="list-style-type: none"> <li>Requires additional space on the PCB for push-pin locations.</li> </ul>                                                                                                                                                        |

## Heat Sink Attachment

### Component Pick-up Tool Consideration

For pick-and-place machines to place bare-die flip-chip BGAs onto PCBs, AMD recommends using soft tips or suction cups for the nozzles. This prevents chipping, scratching, or even cracking of the bare die (Figure 13-2).



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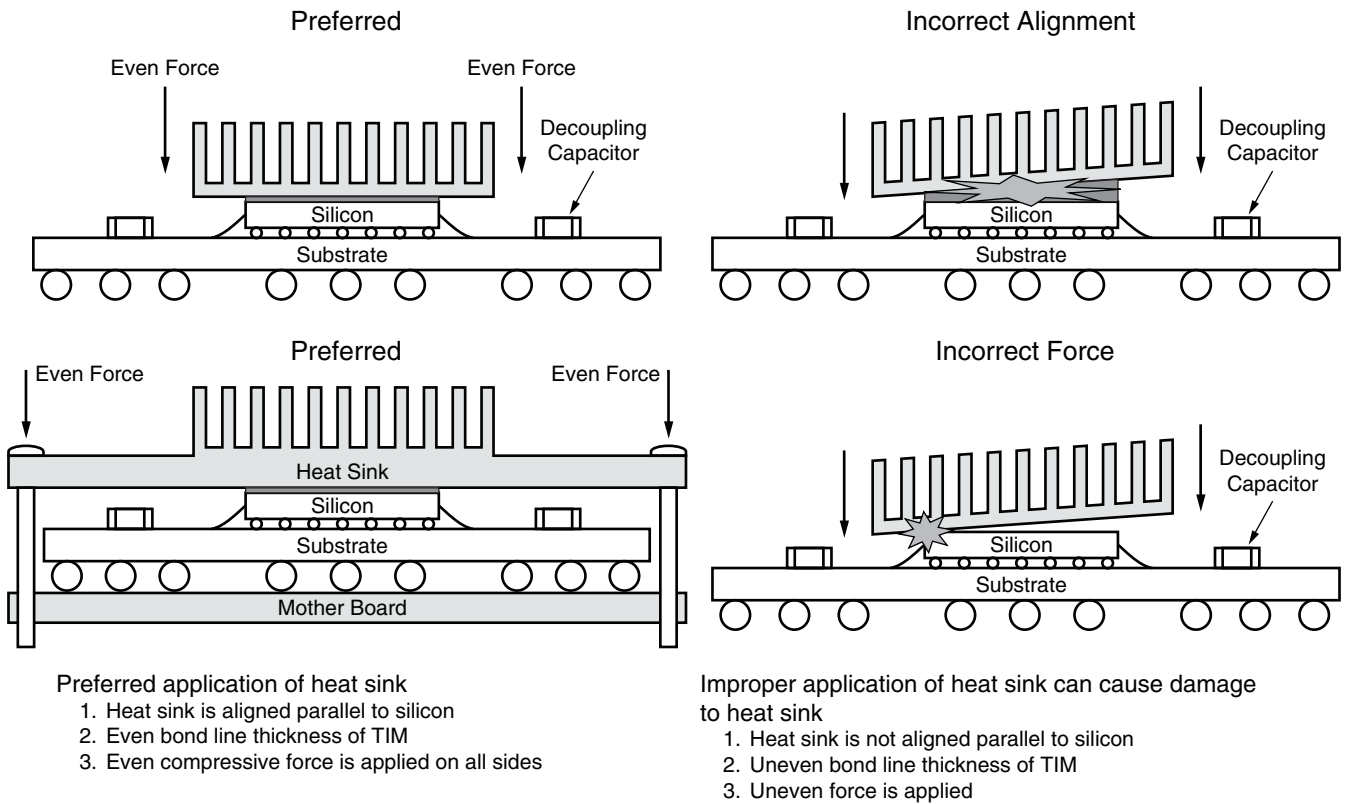
Figure 13-2: Recommended Method For Using Pick-up Tools

Heat Sink Attachment Process Considerations

After the component is placed onto the PCBs, when attaching a heat sink to the bare-die package, the factors in Table 13-2 must be carefully considered (see Figure 13-3).

Table 13-2: Heat Sink Attachment Considerations

| Consideration(s)                                                                                      | Effect(s)                                                                                                                                                                   | Recommendation(s)                                                                                                                                                                                                                       |
|-------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| In heat sink attach process, what factors can cause damage to the exposed die and passive capacitors? | <ul style="list-style-type: none"><li>• Uneven heat sink placement</li><li>• Uneven TIM thickness</li><li>• Uneven force applied when placing heat sink placement</li></ul> | <ul style="list-style-type: none"><li>• Even heat sink placement</li><li>• Even TIM thickness</li><li>• Even force applied when placing heat sink placement</li></ul>                                                                   |
| Does the heat sink tilt or tip the post attachment?                                                   | Uneven heat sink placement will damage the silicon and can cause field failures.                                                                                            | <ul style="list-style-type: none"><li>• Careful handling not to contact the heat sink with the post attachment.</li><li>• Use a fixture to hold the heat sink in place with post attachment until it is glued to the silicon.</li></ul> |



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Figure 13-3: Recommended Application of Heat Sink

### Standard Heat Sink Attach Process with Thermal Conductive Adhesive

Prior to attaching the heat sink, the Zynq UltraScale+ device needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermoset material (electrically non-conductive) is applied over the backside surface of silicon in a pattern using automated dispensing equipment. Automated dispensers are often used to provide a stable process speed at a relatively low cost. The optimum dispensing pattern needs to be determined by the SMT supplier.

**Note:** Minimal volume coverage of the backside of the silicon can result in non-optimum heat transfer.

3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the adhesive spreads to cover the backside silicon. A force transducer is normally used to measure and limit the placement force.
4. The epoxy is cured with heat at a defined time.

**Note:** The epoxy curing temperature and time is based on manufacturer's specifications.

### Standard Heat Sink Attach Process with Thermal Adhesive Tape

Prior to attaching the heat sink, the Zynq UltraScale+ device needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermal adhesive tape cut to the size of the heat sink is applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.
3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the thermal adhesive tape is glued to the backside of the silicon. A force transducer is normally used to measure and limit the placement force.
4. A uniform and constant pressure is applied uniformly over the heat sink and held for a defined time.

**Note:** The thermal adhesive tape hold time is based on manufacturer's specifications.



### Push-Pin and Shoulder Screw Heat Sink Attachment Process with Phase Change Material (PCM) Application

Prior to attaching the heat sink, the Zynq UltraScale+ device needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.

**Note:** The jig or fixture needs to account for the push pin depth of the heat sink.

2. PCM tape, cut to the size of the heat sink, is applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.
3. Using the push-pin tool, heat sinks are applied over the packages ensuring a pin locking action with the PCB holes. The compression load from springs applies the appropriate mounting pressure required for proper thermal interface material performance.

**Note:** Heat sinks must not tilt during installation. This process cannot be automated due to the mechanical locking action which requires manual handling. The PCB drill hole tolerances need to be close enough to eliminate any issues concerning the heat sink attachment.

# Additional Resources and Legal Notices

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## Finding Additional Documentation

### Technical Information Portal

The AMD Technical Information Portal is an online tool that provides robust search and navigation for documentation using your web browser. To access the Technical Information Portal, go to <https://docs.amd.com>.

### Documentation Navigator

Documentation Navigator (DocNav) is an installed tool that provides access to AMD Adaptive Computing documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado™ IDE, select **Help > Documentation and Tutorials**.
- On Windows, click the **Start** button and select **Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

**Note:** For more information on DocNav, see the [Documentation Navigator](#) web page.

### Design Hubs

AMD Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- Go to the [Design Hubs](#) web page.

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## Support Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Support](#).

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## References

1. Zynq UltraScale+ MPSoC Overview ([DS891](#))
2. Zynq UltraScale+ RFSoc Overview ([DS889](#))
3. XQ UltraScale Architecture Data Sheet: Overview ([DS895](#))
4. XA Zynq UltraScale+ MPSoC Data Sheet: Overview ([DS894](#))
5. Zynq UltraScale+ device [Packaging Specifications](#)
6. UltraScale Architecture SelectIO Resources User Guide ([UG571](#))
7. UltraScale Architecture Clocking Resources User Guide ([UG572](#))
8. Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics ([DS925](#))
9. Zynq UltraScale+ RFSoc Data Sheet: DC and AC Switching Characteristics ([DS926](#))
10. Zynq UltraScale+ Device Technical Reference Manual ([UG1085](#))
11. UltraScale Architecture GTH Transceiver User Guide ([UG576](#))
12. UltraScale Architecture GTY Transceiver User Guide ([UG578](#))
13. UltraScale Architecture System Monitor User Guide ([UG580](#))
14. UltraScale Architecture PCB Design Guide ([UG583](#))
15. UltraScale Architecture-Based Memory Interface Solutions Product Guide ([PG150](#))
16. UltraScale Architecture Configuration User Guide ([UG570](#))
17. FAQ: Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products ([XTP424](#))
18. FAQ: Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products ([XTP544](#))
19. All published MDDS files are available on the [See All Package Specifications](#) page.

20. The following websites contain additional information on heat management and contact information.
- Wakefield: [www.wakefield-vette.com](http://www.wakefield-vette.com)
  - Aavid: [www.aavid.com](http://www.aavid.com)
  - Advanced Thermal Solutions: [www.qats.com](http://www.qats.com)
  - Radian Thermal Products: [www.radianheatsinks.com](http://www.radianheatsinks.com)
  - Thermo Cool: [www.thermocoolcorp.com](http://www.thermocoolcorp.com)
  - CTS: [www.ctscorp.com](http://www.ctscorp.com)
21. Refer to the following websites for interface material sources:
- Henkel: [www.henkel.com](http://www.henkel.com)
  - Bergquist Company: [www.bergquistcompany.com](http://www.bergquistcompany.com)
  - AOS Thermal Compound: [www.aosco.com](http://www.aosco.com)
  - Chomerics: [www.chomerics.com](http://www.chomerics.com)
  - Kester: [www.kester.com](http://www.kester.com)
22. Refer to the following websites for CFD tools AMD supports with thermal models.
- Mentor Flotherm: [www.mentor.com/products/mechanical/flotherm/flotherm/](http://www.mentor.com/products/mechanical/flotherm/flotherm/)
  - ANSYS Icepak: [www.ansys.com](http://www.ansys.com)
23. Refer to the [Package Thermal Models](#) on xilinx.com.
24. The following papers are referenced for more information on thermal modeling.
- Lemczyk, T.F., Mack, B., Culham, J.R., and Yovanovich, M.M., 1992, "Printed Circuit Board Trace Thermal Analysis and Effective Conductivity", ASME J. Electronic Packaging, Vol. 114, pp. 413-419.50.
  - Refai-Ahmed, G. and Karimanal, K., 2003, "Validation of Compact Conduction Models of BGA Under Realistic Boundary," J. of Components and Packaging Technology, Vol. 26, No. 3, pp. 610-615.
  - Sansoucy, E., Refai-Ahmed, G., and Karimanal, K., 2002, "Thermal Characterization of TBGA Package for an integration in Board Level Analysis," Eighth Intersociety on Thermal Conference Phenomena in Electronic Systems, San Diego., USA.
  - Karimanal, K. and Refai-Ahmed, G., 2002, "Validation of Compact Conduction Models of BGA Under Realistic Boundary Conditions," Eighth Intersociety on Thermal Conference Phenomena in Electronic Systems, San Diego, USA.
  - Karimanal, K. and Refai-Ahmed, G., 2001, "Compact conduction Model (CCM) of Microelectronic Packages- A BGA Validation Study," APACK Conference on Advance in Packaging, Singapore.

## Revision History

The following table shows the revision history for this document.

| Date       | Version | Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10/11/2024 | 1.13    | <p>Added the XCZU4CG, XCZU4EG, XCZU4EV, XCZU5CG, XCZU5EG, XCZU5EV, XCZU63DR, and XCZU64DR devices throughout.</p> <p>Updated <a href="#">Figure 4-58</a>, <a href="#">Figure 4-60</a>, <a href="#">Figure 4-60</a>, <a href="#">Figure 4-88</a>, <a href="#">Figure 4-98</a>, and <a href="#">Figure 4-100</a>.</p> <p>Added notes to VCCAUX_IO pins for XQ devices to <a href="#">Figure 4-4</a>, <a href="#">Figure 4-24</a>, <a href="#">Figure 4-32</a>, <a href="#">Figure 4-38</a>, <a href="#">Figure 4-40</a>, <a href="#">Figure 4-44</a>, <a href="#">Figure 4-46</a>, <a href="#">Figure 4-48</a>, <a href="#">Figure 4-52</a>, <a href="#">Figure 4-60</a>, <a href="#">Figure 4-72</a>, <a href="#">Figure 4-82</a>, <a href="#">Figure 4-88</a>, <a href="#">Figure 4-90</a>, <a href="#">Figure 4-92</a>, <a href="#">Figure 4-96</a>, <a href="#">Figure 4-98</a>.</p> <p>Updated the legend in <a href="#">Figure 4-14</a>. Updated the diagram in <a href="#">Figure 4-16</a> and added the XQ specific note.</p> <p>Updated the M dimension in <a href="#">Figure 5-3</a>. Added devices to <a href="#">Figure 5-9</a>.</p> <p>Updated the XA devices in <a href="#">Table 8-3</a>.</p> <p>Updated the 0.5 mm pitch values for L and M diameter design rules in <a href="#">Table 9-1</a>.</p> <p>Moved the <a href="#">Conformal Coating</a> section to <a href="#">Chapter 10</a>. Updated the <a href="#">Edge Bonding Implementation</a> section.</p> <p>Updated the supported pressure range for InFO packages in <a href="#">Table 12-1</a>.</p> |
| 2/23/2023  | 1.12    | <p>Added the XCZU3TCG and XCZU3TEG devices throughout.</p> <p>Added the XAZU1EG device throughout. Added missing UBVA530 package and XQZU48DR (FFRE1156) device references throughout.</p> <p>Updated the ADC_VIN_[0 to 3 or _I01 and _I23]_[P or N] pin name in <a href="#">Table 1-4</a>.</p> <p>In <a href="#">Chapter 10</a>, updated the <a href="#">Summary</a> and <a href="#">Edge Bonding Implementation</a> sections (including new images) and added the <a href="#">Underfill Guidelines</a> section.</p> <p>Moved <a href="#">Revision History</a> location.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1/18/2022  | 1.11    | <p>Added the XCZU1CG, XCZU1EG, XCZU42DR, XCZU65DR, and XCZU67DR devices throughout document. Added XQZU48DR and XQZU49DR. Added the UBVA494, FSRG1517, and FSRF1760 packages where applicable.</p> <p><a href="#">Chapter 1, Packaging Overview</a>: Added <a href="#">Note 1</a> to <a href="#">Table 1-5</a> and updated links to <a href="#">Note 2</a> in <a href="#">Table 1-7</a>. Updated and corrected bank diagrams <a href="#">Figure 1-42</a> and <a href="#">Figure 1-60</a>.</p> <p><a href="#">Chapter 2, PS Memory Interface Pin Guidelines</a>: Corrected the Important note on <a href="#">page 105</a>. Updated some of the descriptions in <a href="#">Table 2-1</a> and <a href="#">Table 2-2</a> to avoid confusion. In <a href="#">Table 2-4</a>, corrected the PS_DDR_ODT1 for LPDDR3 64-bit entry (can be left unconnected).</p> <p><a href="#">Chapter 5, Mechanical Drawings</a>: Added links to the MDDS file information. Updated <a href="#">Figure 5-21</a> with the correct diagram.</p> <p><a href="#">Chapter 8, Soldering Guidelines</a>: Updated the Important note on <a href="#">page 287</a>.</p> <p><a href="#">Chapter 10, Edge Bonding and Underfill Guidelines</a>: Added the Important note on <a href="#">page 301</a>.</p> <p><a href="#">Chapter 12, Thermal Management Strategy</a>: Updated the <a href="#">Applied Pressure from Heat Sink to the Package via Thermal Interface Materials</a> and added <a href="#">Table 12-1</a>.</p>                                                                                  |

| Date      | Version | Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7/01/2021 | 1.10    | <p>Added InFO package (UBVA530) throughout.</p> <p><a href="#">Chapter 5, Mechanical Drawings</a>: Added <a href="#">Figure 5-21</a> and <a href="#">Figure 5-22</a>. Updated A<sub>3</sub> and A<sub>4</sub> dimensions in <a href="#">Figure 5-21</a>, <a href="#">Figure 5-29</a>, and <a href="#">Figure 5-34</a>.</p> <p><a href="#">Chapter 8, Soldering Guidelines</a>: Updated <a href="#">Pb-Free Reflow Soldering</a> to include <a href="#">Table 8-2</a>, <a href="#">Figure 8-3</a>, and <a href="#">Figure 8-4</a>. Added the <a href="#">Strain Gauge Measurement</a>, <a href="#">Solder Paste</a>, and <a href="#">Component Placement</a> sections.</p> <p><a href="#">Chapter 9, Recommended PCB Design Rules for BGA Packages</a>: Added <a href="#">Stencil</a> section.</p> <p><a href="#">Chapter 10, Edge Bonding and Underfill Guidelines</a>: Added chapter.</p>                                                                                                                                                                              |
| 6/24/2020 | 1.9     | <p>Added the XCZU43DR, XCZU47DR, XCZU46DR, XCZU48DR, and XCZU49DR devices throughout document. Added the FFVH1760 and FSVH1760 packages throughout document.</p> <p><a href="#">Chapter 2, PS Memory Interface Pin Guidelines</a>: Updated the <a href="#">DDR3/3L Pinout Example for Supported Configurations</a>, <a href="#">DDR4 Pin Rules</a>, <a href="#">DDR4 Pinout Example for Supported Configurations</a>, and <a href="#">LPDDR3 Pinout Example for Supported Configurations</a> sections. Clarified the headings in <a href="#">Table 2-4</a> and updated the LPDDR3 64-bit column for PS_DDR_CKE0, PS_DDR_CKE1, PS_DDR_CS_N0, and PS_DDR_ODT0.</p> <p><a href="#">Chapter 6, Package Marking</a>: Added a new top-mark diagram (<a href="#">Figure 6-1</a>).</p> <p><a href="#">Chapter 8, Soldering Guidelines</a>: Updated and removed notes linking to data sheets for reflow body temperatures.</p> <p><a href="#">Chapter 11, Thermal Specifications</a>: Added links to <a href="#">Package Thermal Data Query</a> for thermal simulation data.</p> |
| 7/12/2019 | 1.8     | <p>Added the XAZU7EV, XAZU11EG, XCZU39DR, XQZU3EG, XQZU9EG, XQZU11EG, XQZU19EG, XQZU21DR, XQZU28DR, and XQZU29DR devices throughout. Added the SFRA484, FFRD1156, FFRE1156, FFRB1517, FFRG1517, FFRC1760, and FFRF1760 packages where applicable.</p> <p>Updated the recommended applied pressure range on <a href="#">page 324</a>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

| Date      | Version | Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
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| 1/31/2019 | 1.7     | <p><b>Chapter 1:</b> Added an Important Note about XQ devices with eutectic BGA balls on <a href="#">page 8</a>. Added the XQZU5EV (SFRC784, FFRB900), XQZU7EV (FFRB900, FFRC1156), and XQZU15EG (FFRC900, FFRB1156) device/package combinations to <a href="#">Table 1-1</a>, <a href="#">Table 1-2</a>, <a href="#">Table 1-3</a>, <a href="#">Table 1-7</a>, <a href="#">Table 1-8</a>, and the associated bank diagram figures in this section. In <a href="#">Table 1-4</a>, added the type and direction data for <a href="#">VCCO_PSIO[0:3]_ [500:503]</a> and <a href="#">VCCO_PSDDR</a>. Added a note for XQ ruggedized packages to <a href="#">VCCAUX_IO</a>. Revised the GTH Quad 229 coordinates in <a href="#">Figure 1-27</a>. Fixed GTH Quad location errors in <a href="#">Figure 1-33</a> through <a href="#">Figure 1-35</a>.</p> <p><b>Chapter 2:</b> Updated the <a href="#">DDR3/3L Pinout Example for Supported Configurations</a> description and added <a href="#">VCCO_PSDDR</a> and <a href="#">Note 1</a> to <a href="#">Table 2-1</a>. Updated the <a href="#">DDR4 Pinout Example for Supported Configurations</a> description and added <a href="#">VCCO_PSDDR</a> to <a href="#">Table 2-2</a> and <a href="#">Note 1</a>. Also in <a href="#">Table 2-2</a>, added to guidelines for PS_DDR_A17, and PS_DDR_DQ32 to PS_DDR_DQ63. Updated the <a href="#">LPDDR4 Pinout Example for Supported Configurations</a> description and added <a href="#">VCCO_PSDDR</a> to <a href="#">Table 2-3</a> and <a href="#">Note 1</a>. Updated the <a href="#">LPDDR3 Pinout Example for Supported Configurations</a> description and added <a href="#">VCCO_PSDDR</a> to <a href="#">Table 2-4</a> and <a href="#">Note 1</a>.</p> <p><b>Chapter 3:</b> Added an Important Note about XQ devices with eutectic BGA balls on <a href="#">page 127</a>. Added the XQZU5EV (SFRC784, FFRB900), XQZU7EV (FFRB900, FFRC1156), and XQZU15EG (FFRC900, FFRB1156) device/package combinations to <a href="#">Table 3-1</a> labeled as production.</p> <p><b>Chapter 4:</b> Added an Important Note about XQ devices with eutectic BGA balls on <a href="#">page 132</a>. In <a href="#">Table 4-1</a>, added the XQZU5EV (SFRC784, FFRB900), XQZU7EV (FFRB900, FFRC1156), and XQZU15EG (FFRC900, FFRB1156) device/package combinations.</p> <p><b>Chapter 5:</b> Added an Important Note about XQ devices with eutectic BGA balls on <a href="#">page 240</a>. In <a href="#">Table 5-1</a>, added the XQZU5EV (SFRC784, FFRB900), XQZU7EV (FFRB900, FFRC1156), and XQZU15EG (FFRC900, FFRB1156) device/package combinations. Added <a href="#">Figure 5-8</a>, <a href="#">Figure 5-13</a>, <a href="#">Figure 5-16</a>, and <a href="#">Figure 5-17</a>.</p> <p><b>Chapter 6:</b> Updated <a href="#">Table 6-1</a> and added <a href="#">Figure 6-3</a>.</p> <p><b>Chapter 7:</b> Added an Important Note about XQ devices with eutectic BGA balls on <a href="#">page 286</a>. In <a href="#">Table 7-1</a>, added the ruggedized packages (SFRC784, FFRB900, FFRC900, FFRB1156, and FFRC1156).</p> <p><b>Chapter 8:</b> Updated the chapter with more information on eutectic packages including adding the <a href="#">Sn/Pb Reflow Soldering</a> section. In <a href="#">Table 8-3</a>, added the ruggedized packages (SFRC784, FFRB900, FFRC900, FFRB1156, and FFRC1156).</p> <p><b>Chapter 11:</b> Added an Important Note about XQ devices with eutectic BGA balls on <a href="#">page 314</a>. In <a href="#">Table 11-1</a>, added the XQZU5EV (SFRC784, FFRB900), XQZU7EV (FFRB900, FFRC1156), and XQZU15EG (FFRC900, FFRB1156) device/package combinations.</p> |

| Date      | Version | Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
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| 8/20/2018 | 1.6     | <p><b>Chapter 1:</b> Added the XAZU4EV and XAZU5EV devices in the SFVC784 package. This includes updates to <a href="#">Table 1-2</a>, <a href="#">Table 1-3</a>, <a href="#">Table 1-5</a>, <a href="#">Table 1-7</a>, <a href="#">Table 1-8</a>, <a href="#">Figure 1-17</a>, and <a href="#">Figure 1-18</a>. Corrected the <a href="#">VCCO_PSDDR</a> pin name (from <a href="#">VCCO_PSDDR_504</a>) in <a href="#">Table 1-4</a>. Added a note to <a href="#">Figure 1-10</a> on <a href="#">page 53</a>.</p> <p><b>Chapter 2:</b> Clarified what a byte lane includes in the pin swapping restrictions discussions on <a href="#">page 105</a> and <a href="#">page 109</a>.</p> <p><b>Chapter 3:</b> Added the XAZU4EV and XAZU5EV devices to <a href="#">Table 3-1</a>. Labeled all of the devices in <a href="#">Table 3-2</a> as production.</p> <p><b>Chapter 4:</b> In <a href="#">Table 4-1</a>, added the XAZU4EV and XAZU5EV devices and changed the XCZU21DR, XCZU25DR, XCZU27DR, XCZU28DR, and XCZU29DR device labels to production. Added a note above <a href="#">Figure 4-3</a> on <a href="#">page 140</a>. Added the XAZU4EV and XAZU5EV devices in the SFVC784 package to <a href="#">Figure 4-23</a> and <a href="#">Figure 4-24</a>.</p> <p><b>Chapter 5:</b> Added the XAZU4EV and XAZU5EV devices to <a href="#">Table 5-1</a> and <a href="#">Figure 5-9</a>. Labeled all of the devices in <a href="#">Table 5-2</a> as production.</p> <p><b>Chapter 11:</b> Added the XAZU4EV and XAZU5EV devices to <a href="#">Table 11-1</a>.</p>                                                                                                                                                                     |
| 4/10/2018 | 1.5     | <p><b>Chapter 1:</b> Added the XCZU21DR, XCZU25DR, XCZU27DR, XCZU28DR, and XCZU29DR devices. This includes updates to <a href="#">Table 1-1</a>, <a href="#">Table 1-2</a>, <a href="#">Table 1-3</a>, <a href="#">Table 1-4</a>, <a href="#">Table 1-5</a>, <a href="#">Table 1-7</a>, and <a href="#">Table 1-8</a>. Added <a href="#">Figure 1-42</a> through <a href="#">Figure 1-53</a>.</p> <p><b>Chapter 3:</b> Added the XCZU21DR, XCZU25DR, XCZU27DR, XCZU28DR, and XCZU29DR ASCII file links, see <a href="#">Table 3-2</a>.</p> <p><b>Chapter 4:</b> Added the XCZU21DR, XCZU25DR, XCZU27DR, XCZU28DR, and XCZU29DR devices to <a href="#">Table 4-1</a>.</p> <p><b>Chapter 5:</b> Added the XCZU21DR, XCZU25DR, XCZU27DR, XCZU28DR, and XCZU29DR mechanical drawings, see <a href="#">Table 5-2</a>.</p> <p><b>Chapter 7:</b> Added the FFVD1156, FFVE1156, FSVE1156, FFVG1517, FSVG1517, FFVF1760, and FSVF1760 packages to <a href="#">Table 7-1</a>.</p> <p><b>Chapter 8:</b> Revised the guidelines in <a href="#">Table 8-1</a> for <a href="#">Ramp-up rate</a>, <a href="#">Peak temperature (lead/ball)</a>, and <a href="#">Peak temperature (body)</a>. Revised the same information in <a href="#">Figure 8-2</a>. Added the FFVD1156, FFVE1156, FSVE1156, FFVG1517, FSVG1517, FFVF1760, and FSVF1760 packages to <a href="#">Table 8-3</a>.</p> <p><b>Chapter 11:</b> Added the XCZU21DR, XCZU25DR, XCZU27DR, XCZU28DR, and XCZU29DR devices to <a href="#">Table 11-1</a> and added <a href="#">Note 1</a>.</p> <p><b>Chapter 12:</b> Updated the <a href="#">System Level Heat Sink Solutions</a> section and added the <a href="#">Heat Sink Removal</a> and <a href="#">Measurement Debug</a> sections.</p> |



| Date       | Version | Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
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| 12/21/2017 | 1.4     | <p>Added the XAZU2EG and XAZU3EG devices throughout the document.</p> <p><b>Chapter 1:</b> Revise the VCCINT_VCU description in <a href="#">Table 1-4</a>. Updated the ZU11EG (<a href="#">Figure 1-28</a> through <a href="#">Figure 1-32</a>) PCIE4 bank coordinates.</p> <p><b>Chapter 2:</b> Updated <a href="#">LPDDR4 Pin Swapping Restrictions</a> and <a href="#">DDR4 Pin Swapping Restrictions</a> and removed <a href="#">Figure 2-1: DDR Controller Implementation of DQ Mapping</a>. In <a href="#">Table 2-2</a>, updated the PS_DDR_ZQ connections.</p> <p><b>Chapter 5:</b> Revised <a href="#">Figure 5-10</a>: Symbol A from (2.57/2.77/2.97) to (2.48/2.68/2.88) and Symbol A2 from (1.27/1.42/1.62) to (1.18/1.33/1.48).</p> <p><b>Chapter 6:</b> Revised the top mark diagram to show both older device versions and newer ones with a 2D bar code.</p> <p><b>Chapter 8:</b> Added an Important note on <a href="#">page 287</a> about reflow rework.</p> <p><b>Chapter 11:</b> Updated the SFVC784, FFVC900, FFVB1156, FFVC1156, FFVB1517, FFVF1517 data to account for the stamped lid in <a href="#">Table 11-1</a>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 8/29/2017  | 1.3     | <p>In <a href="#">Chapter 1</a>, updated <a href="#">Figure 1-10</a>, <a href="#">Figure 1-25</a>, <a href="#">Figure 1-26</a>, <a href="#">Figure 1-27</a>, <a href="#">Figure 1-33</a>, <a href="#">Figure 1-34</a>, <a href="#">Figure 1-35</a>, <a href="#">Figure 1-36</a>, <a href="#">Figure 1-37</a>, <a href="#">Figure 1-38</a>, <a href="#">Figure 1-39</a>, and <a href="#">Figure 1-40</a>. Revise the VCCINT_VCU description in <a href="#">Table 1-4</a>.</p> <p>In <a href="#">Chapter 2</a>, updated the <a href="#">DDR4 Pin Rules</a> and the <a href="#">DDR4 Pin Swapping Restrictions</a>. In <a href="#">Table 2-2</a>, updated the configurations for PS_DDR_CK_N1 (DDR4 1Rank).</p> <p>In <a href="#">Chapter 3</a>, updated the package specification designation of many of the packages listed in <a href="#">Table 3-1</a>.</p> <p>In <a href="#">Chapter 4</a>, updated <a href="#">Table 4-1</a> and added the following device diagrams: <a href="#">SFVC784 Package–XCZU4CG</a>, <a href="#">XCZU4EG</a>, <a href="#">XCZU5CG</a>, and <a href="#">XCZU5EG</a>, <a href="#">SFVC784 Package–XCZU4EV</a>, <a href="#">XCZU5EV</a>, <a href="#">XAZU4EV</a>, and <a href="#">XAZU5EV</a>, <a href="#">FBVB900 Package–XCZU4CG</a>, <a href="#">XCZU4EG</a>, <a href="#">XCZU5CG</a>, and <a href="#">XCZU5EG</a>, <a href="#">FBVB900 Package–XCZU4EV</a> and <a href="#">XCZU5EV</a>, <a href="#">FFVF1517 Package–XCZU7CG</a> and <a href="#">XCZU7EG</a>, <a href="#">FFVC1156 Package–XCZU7EV</a>, <a href="#">FFVC1156 Package–XCZU11EG</a>, <a href="#">FFVB1517 Package–XCZU11EG</a>, <a href="#">FFVF1517 Package–XCZU11EG</a>, and <a href="#">FFVC1760 Package–XCZU11EG</a>.</p> <p>In <a href="#">Chapter 5</a>, replaced <a href="#">Figure 5-9</a>, added <a href="#">Figure 5-10</a>, <a href="#">Figure 5-11</a>, <a href="#">Figure 5-25</a>, and <a href="#">Figure 5-36</a>.</p> <p>In <a href="#">Table 8-3</a>, update the FFV packages to a mass reflow of 245°C.</p> |
| 1/13/2017  | 1.2     | <p>Added the following devices throughout: <a href="#">XCZU2CG</a>, <a href="#">XCZU3CG</a>, <a href="#">XCZU4CG</a>, <a href="#">XCZU4EG</a>, <a href="#">XCZU5CG</a>, <a href="#">XCZU5EG</a>, <a href="#">XCZU6CG</a>, <a href="#">XCZU7CG</a>, <a href="#">XCZU7EG</a>, and <a href="#">XCZU9CG</a>. In <a href="#">Table 1-3</a>, revised the available PS I/O pin values for the SBVA484 and SFVA625 packages. In <a href="#">Table 1-4</a>, updated the PS_MODE directions and the pin descriptions in the <a href="#">Power/Ground Pins</a> section. In <a href="#">Table 1-7</a>, revised the XCZU4 bank numbers and updated the FBVB900 mapping. Revised the mapping for the FBVB900 package in <a href="#">Table 1-8</a>. Revised the <a href="#">Bank Locations of Dedicated and Multi-Function Pins</a> section. Updated the HD I/O bank numbers in <a href="#">Figure 1-32</a>.</p> <p>Added <a href="#">Chapter 2, PS Memory Interface Pin Guidelines</a>. Added the <a href="#">Chapter 3, Package Specifications Designations</a> section. In <a href="#">Table 3-1</a>, updated links. <a href="#">Chapter 4, Device Diagrams</a> and <a href="#">Chapter 5, Mechanical Drawings</a> have updated tables and new diagrams. Revised the <a href="#">Bar Code</a> section of <a href="#">Table 6-1</a> to include changes outlined in <a href="#">XCN16014: Top Marking change for 7 Series, UltraScale, and UltraScale+ Products</a>. Updated the <a href="#">AUTOMOTIVE APPLICATIONS DISCLAIMER</a>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

| Date       | Version | Revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
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| 6/14/2016  | 1.1     | In <a href="#">Table 1-3</a> , updated <a href="#">Note 1</a> and the SBVA484 package total user HP I/Os. Clarified the I2C_SCLK and I2C_SDA descriptions and added SMBALERT and VCCINT_VCU to <a href="#">Table 1-4</a> . Also updated the <a href="#">Multi-gigabit Serial Transceiver Pins (GTHE4, GTYE4, and PS-GTR)</a> descriptions, Added further descriptions in the <a href="#">Die Level Bank Numbering Overview</a> including adding an example device diagram ( <a href="#">Figure 1-3</a> ). In <a href="#">Chapter 4</a> , added new figures and updated all of the graphics because the PERSTN pins and SMBALERT pins have moved. Updated <a href="#">Figure 5-16</a> and added <a href="#">Figure 5-18</a> . Added the bar code description in <a href="#">Chapter 6</a> . |
| 1/20/2016  | 1.0.2   | Replaced the missing graphics in <a href="#">Chapter 1</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 12/18/2015 | 1.0.1   | Updated the package file links in <a href="#">Chapter 3</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 11/24/2015 | 1.0     | Initial AMD release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

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