THE DATASHEET OF

AS6214-AWLT-S

QPA1019

4.5 – 7.0 GHz 10 W GaN Power Amplifier

Product Overview

Qorvo's QPA1019 is a packaged high-power, C-band amplifier fabricated on Qorvo's production 0.15 um GaN on SiC process (QGaN15). Covering 4.5 – 7.0 GHz, the QPA1019 provides greater than 10 W of saturated output power and 19 dB of large-signal gain while achieving greater than 39% power-added efficiency.

The QPA1019 is packaged in a plastic overmold QFN with a Cu paddle offering easy handling with good thermal properties. As a result, the QPA1019 has bias flexibility allowing the user to vary the voltage to achieve optimum system performance while maintaining high reliability.

The QPA1019 is matched to 50 ohms with integrated DC blocking caps on both I/O ports. With the high performance, good thermal characteristics and ease of handling and system integration, the QPA1019 is ideal for radar and satellite communication systems.

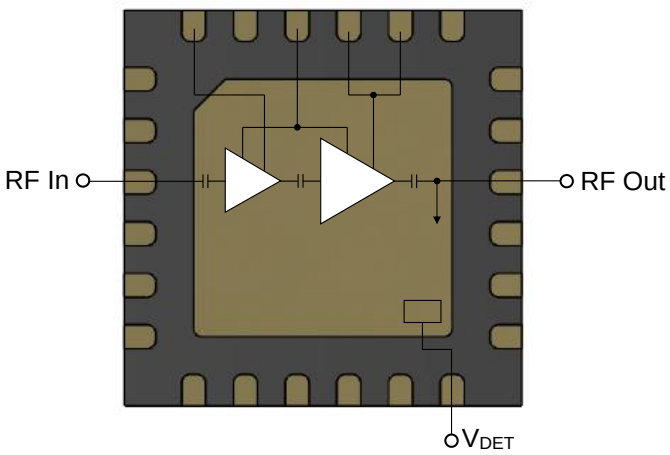
Lead-free and RoHS compliant.

Key Features

- Frequency Range: 4.5 – 7.0 GHz
- P_{SAT} (P_{IN}=22 dBm): > 40 dBm
- PAE (P_{IN}=22 dBm): > 40 %
- Power Gain (P_{IN}=22 dBm): > 19 dB
- Integrated Power Detector
- Bias: V_D = 22 V, I_{DQ} = 290 mA, V_G = −2.5 V typical
- Package Dimensions: 5.0 x 5.0 x 0.85 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- C-Band Radar
- Satellite Communication

Ordering Information

Part No.	Description
QPA1019	4.5 – 7.0GHz 10W GaN Power Amplifier
QPA1019S2	Samples (2 pcs. pack)
QPA1019TR7	250 pieces on a 7" reel (standard)
QPA1019EVB	Evaluation Board for QPA1019

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5
Gate Voltage Range (V_G)	−6 to 0 V
Drain Current (I_{D1}, I_{D2})	0.52, 2.0 A
Gate Current (I_G)	See chart
Power Dissipation (P_{DISS}), CW, 85°C	25.2 W
Input Power (P_{IN}), CW, 50 Ω, V_D=22 V, I_{DQ}=290 mA, 85 °C	28 dBm
Input Power (P_{IN}), CW, 4:1 VSWR, V_D=22 V , I_{DQ}=290 mA, 85 °C	25 dBm
Channel Temperature (T_{CH})	275 °C
Mounting Temperature (30 seconds)	260 °C
Storage Temperature	−55 to 150 °C

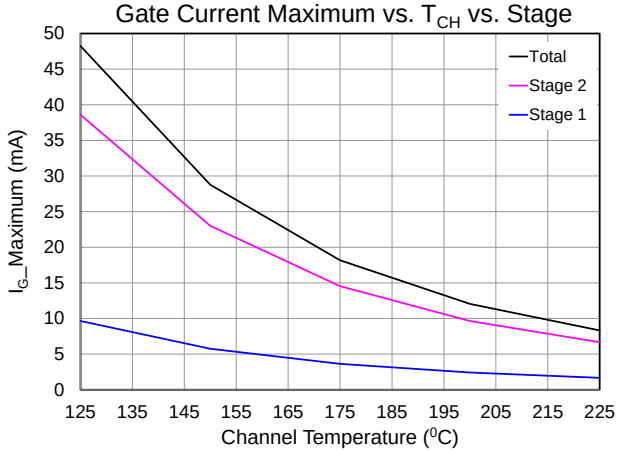
Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_D)		+22		V
Drain Current, Quiescent (I_{DQ})		290		mA
Drain Current, RF (I_{D_Drive})	See charts page 3 - 8			mA
Gate Voltage Typ. Range (V_G)	−2 to -2.8			V
Gate Current, RF (I_{G_Drive})	See charts page 5 - 8			mA
Operating Temp. Range	−40	+25	+85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Gate Current Maximum vs. T_{CH} vs. Stage



Electrical Specifications

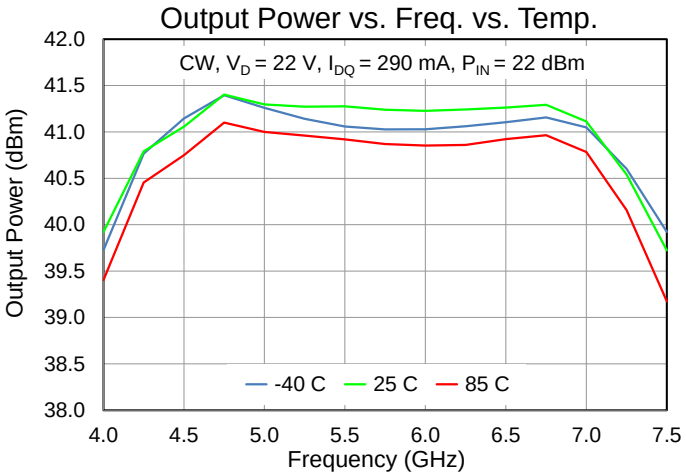
Parameter	Conditions (1) (2)	Min	Typ	Max	Units
Operational Frequency Range		4.5		7.0	GHz
Output Power at Saturation, P_{SAT}	P_{IN} = +22 dBm	39	41		dBm
Power Added Efficiency, PAE	P_{IN} = +22 dBm; Frequency = 4.5 – 5.5 GHz	35	45		%
	P_{IN} = +22 dBm; Frequency = 6.0 – 7.0 GHz		40		
Small Signal Gain, S21			30		dB
Input Return Loss, IRL			15		dB
Output Return Loss, ORL			7		dB
3RD Intermodulation Products, IM3	$P_{OUT/TONE}$ = +32 dBm; Frequency = 5.7 GHz		−25		dBc
P_{SAT} Temperature Coefficient	T_{DIFF} = +25°C to +85°C; P_{IN} = +22 dBm		−0.007		dBm/°C
S21 Temperature Coefficient	T_{DIFF} = −40°C to +85°C		−0.050		dB/°C

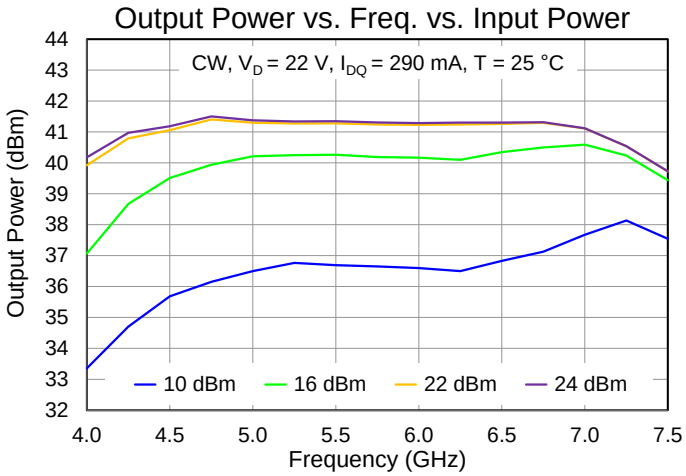
Notes:

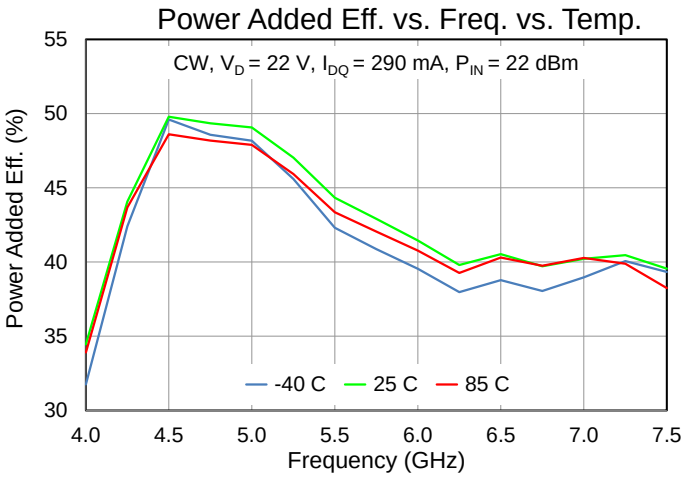
1. Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 290 mA, V_G = -2.5V +/- typical , T_{BASE} = +25 °C, Z_0 = 50 Ω
2. T_{BASE} is back side of package

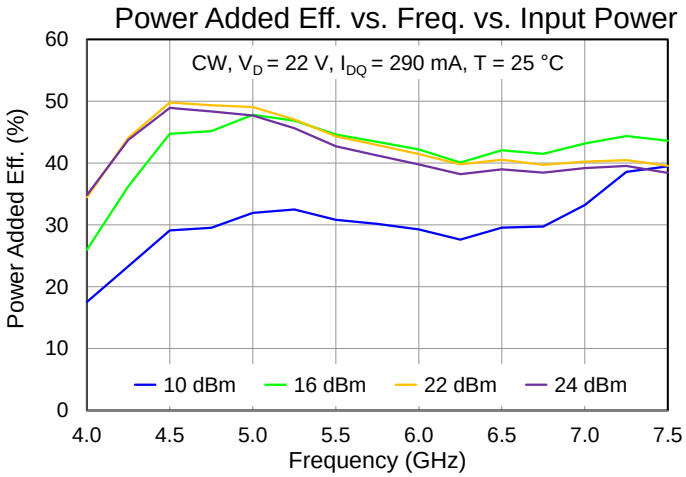
Performance Plots – Large Signal

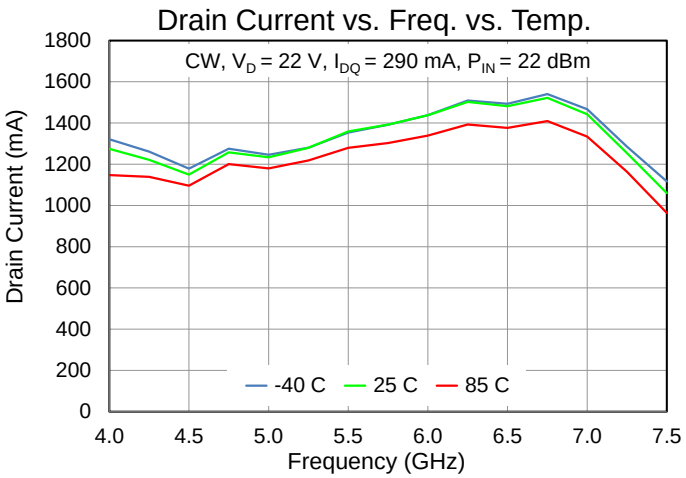
Test conditions unless otherwise noted: **CW** V_D = 22 V, I_{DQ} = 290 mA, CW input power, T=+25 °C

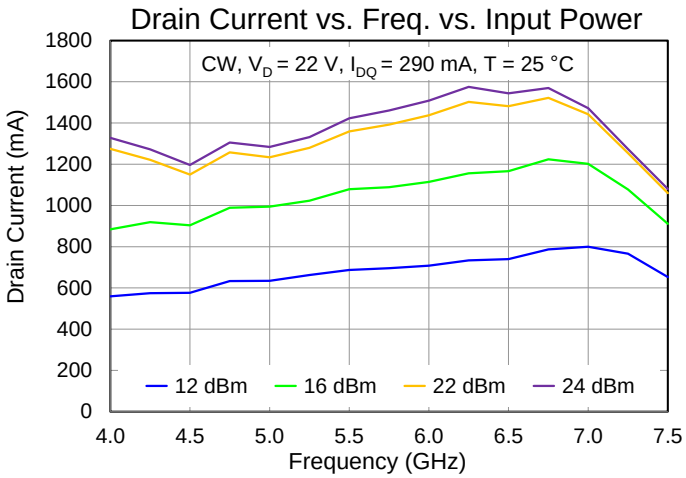






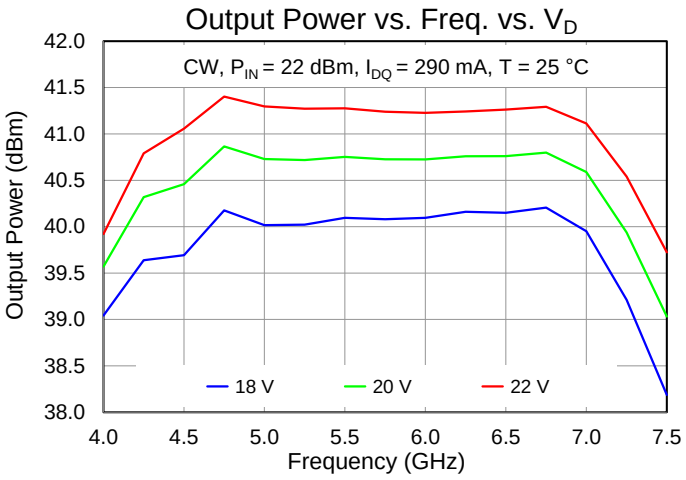


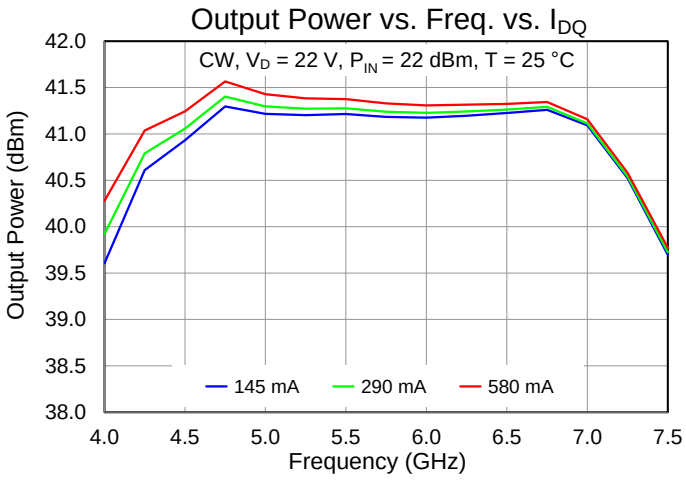


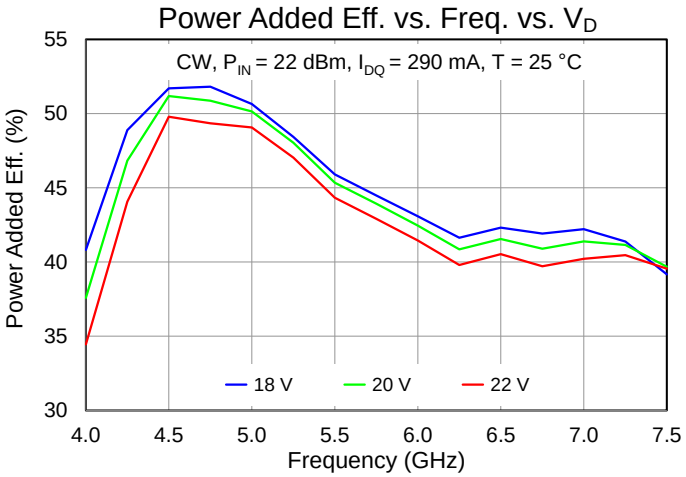


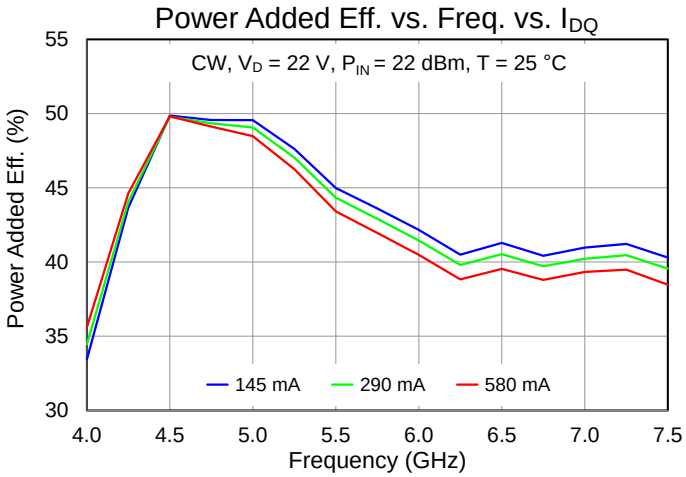
Performance Plots – Large Signal

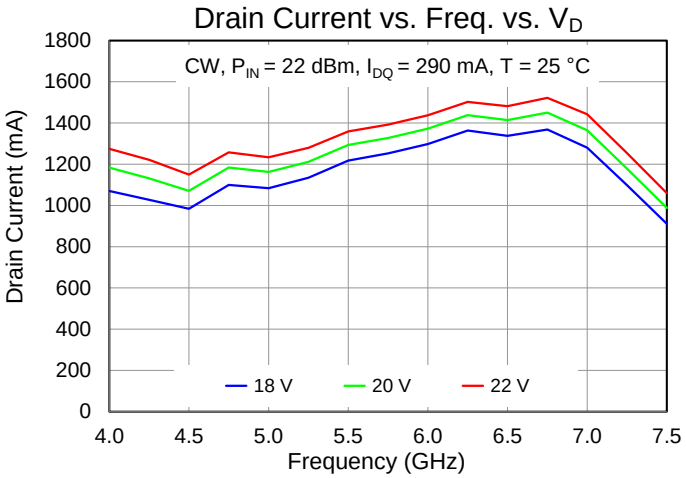
Test conditions unless otherwise noted: **CW** V_D = 22 V, I_{DQ} = 290 mA, CW input power, T=+25 °C

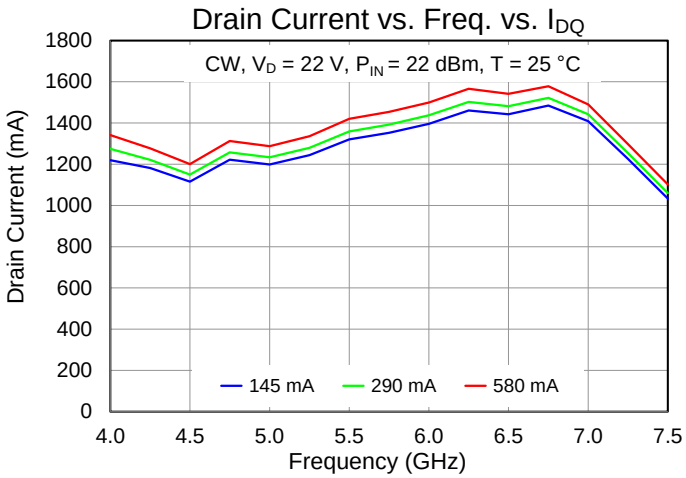








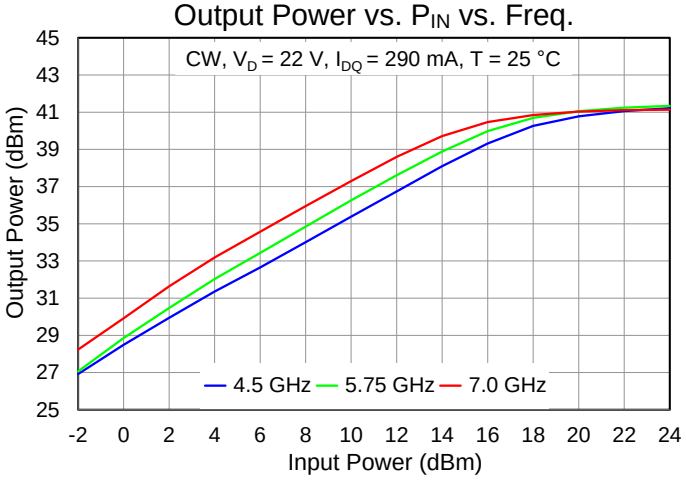




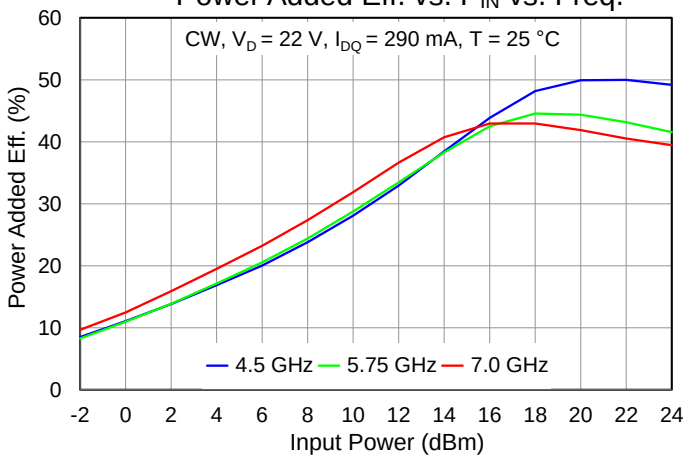
Performance Plots – Large Signal

Test conditions unless otherwise noted: **CW** V_D = 22 V, I_{DQ} = 290 mA, CW input power, T=+25 °C

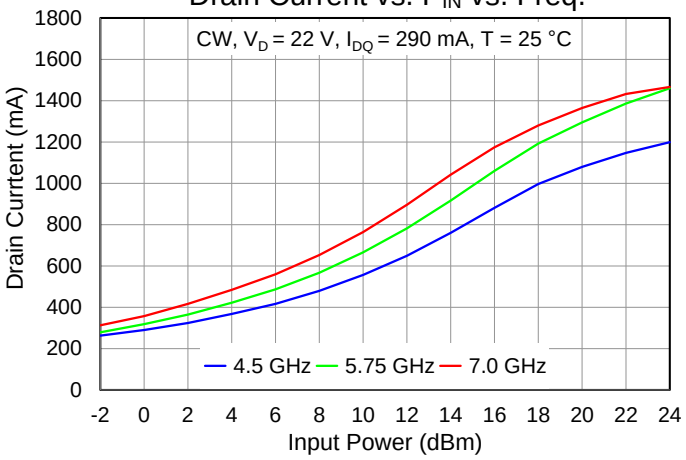
Output Power vs. P_{IN} vs. Freq.



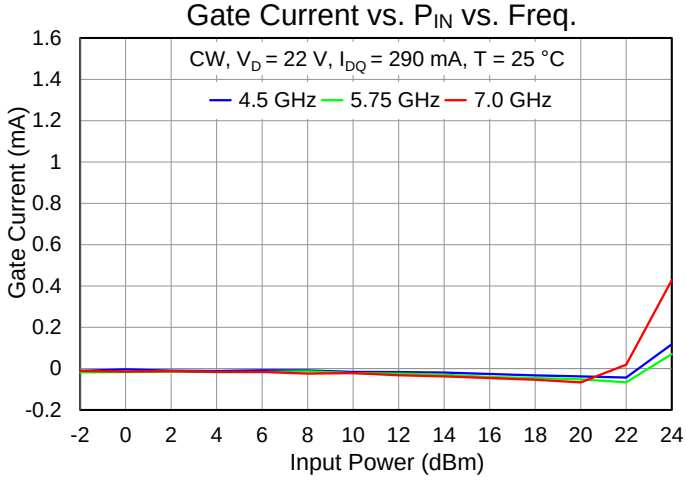
Power Added Eff. vs. P_{IN} vs. Freq.



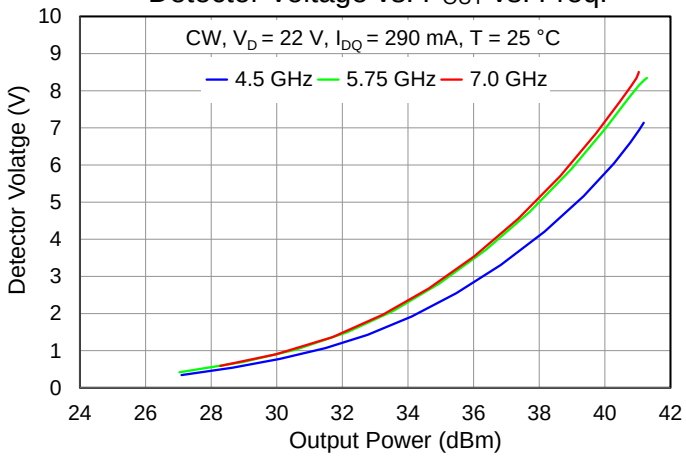
Drain Current vs. P_{IN} vs. Freq.



Gate Current vs. P_{IN} vs. Freq.



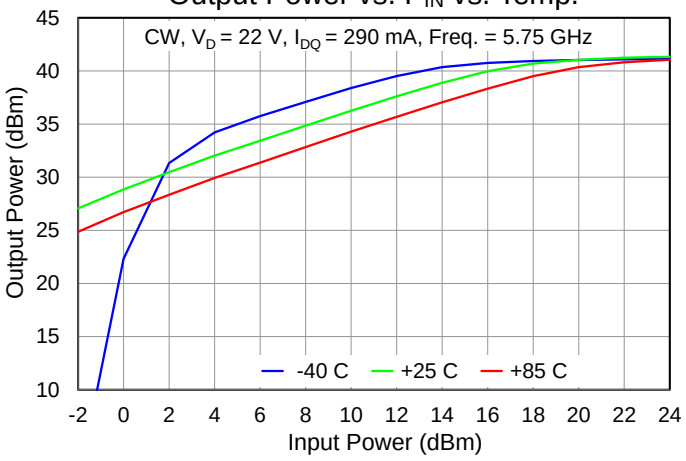
Detector Voltage vs. P_{OUT} vs. Freq.



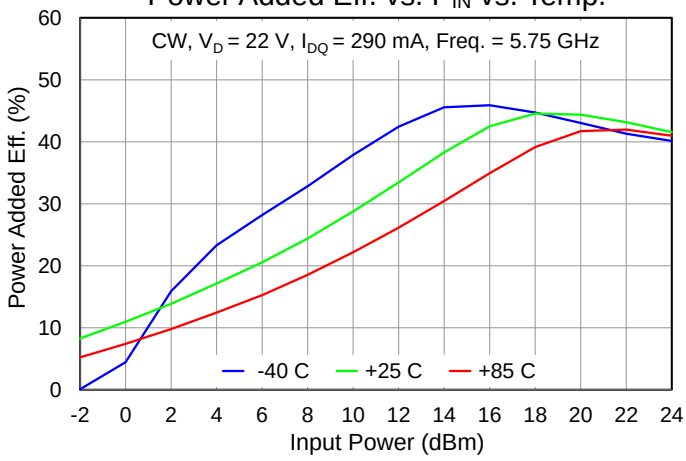
Performance Plots – Large Signal

Test conditions unless otherwise noted: **CW** V_D = 22 V, I_{DQ} = 290 mA, CW input power, T=+25 °C

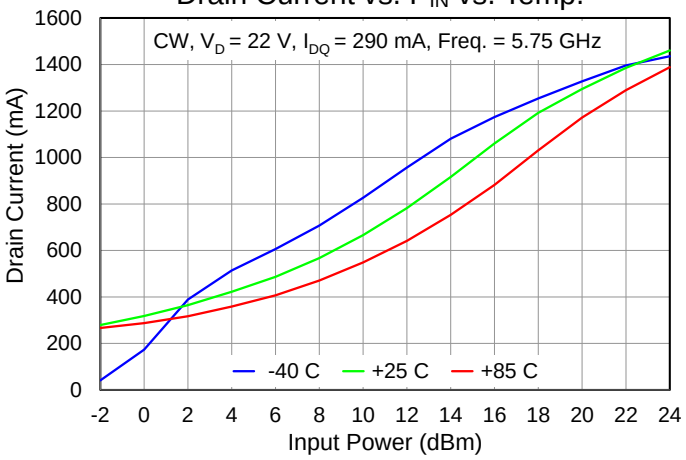
Output Power vs. P_{IN} vs. Temp.



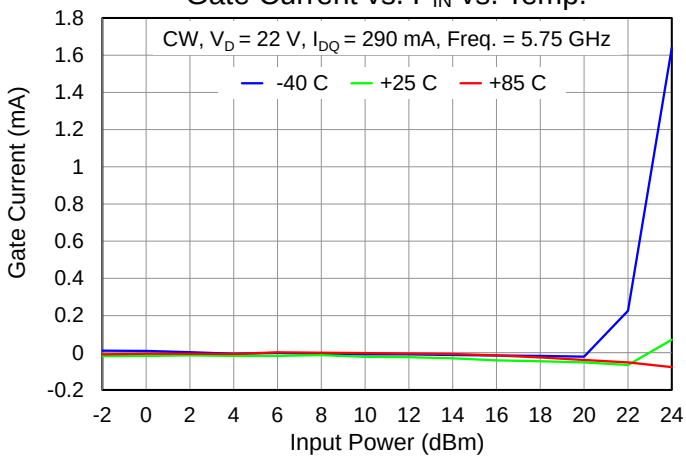
Power Added Eff. vs. P_{IN} vs. Temp.



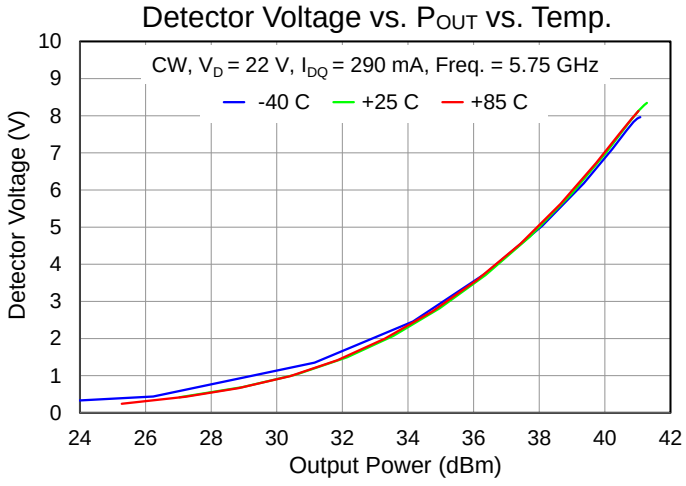
Drain Current vs. P_{IN} vs. Temp.



Gate Current vs. P_{IN} vs. Temp.



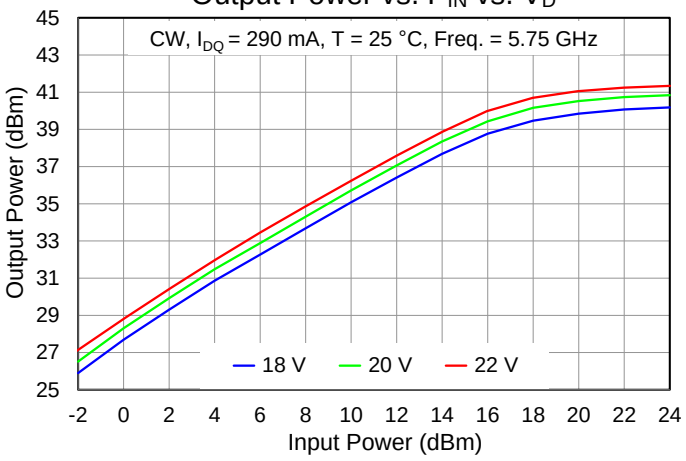
Detector Voltage vs. P_{OUT} vs. Temp.



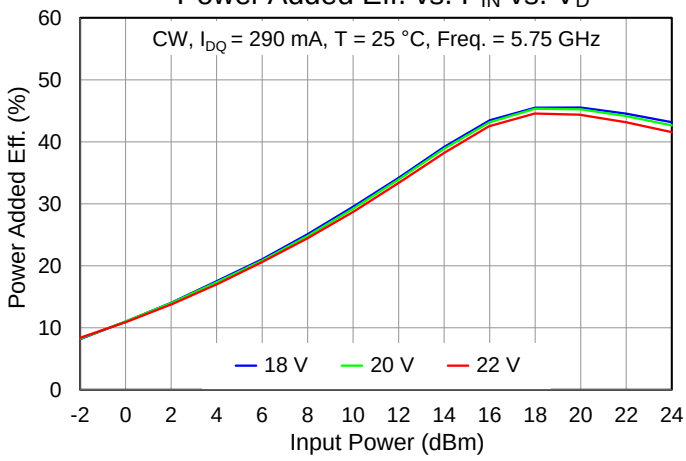
Performance Plots – Large Signal

Test conditions unless otherwise noted: **CW** V_D = 22 V, I_{DQ} = 290 mA, CW input power, T=+25 °C

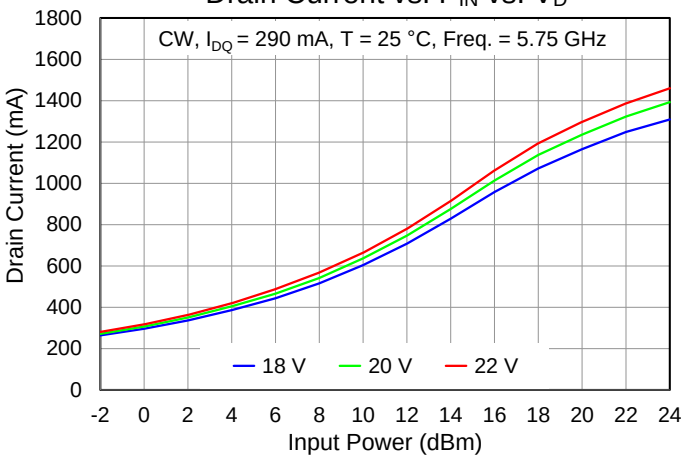
Output Power vs. P_{IN} vs. V_D



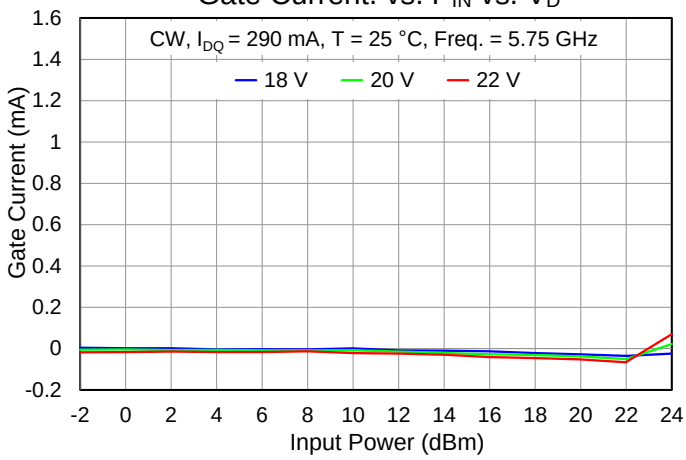
Power Added Eff. vs. P_{IN} vs. V_D



Drain Current vs. P_{IN} vs. V_D



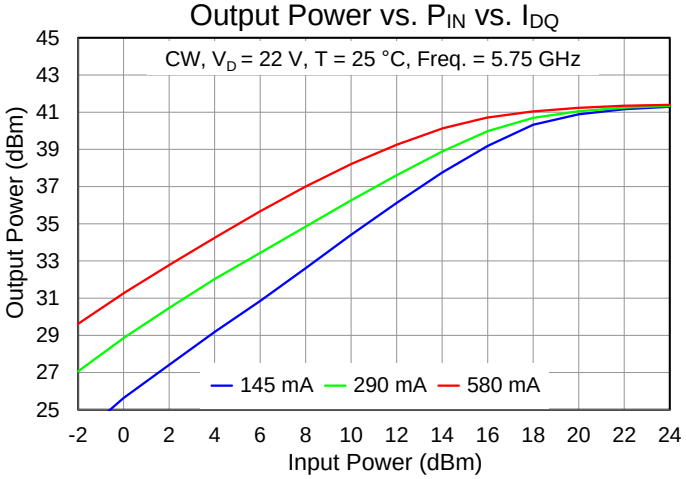
Gate Current. vs. P_{IN} vs. V_D



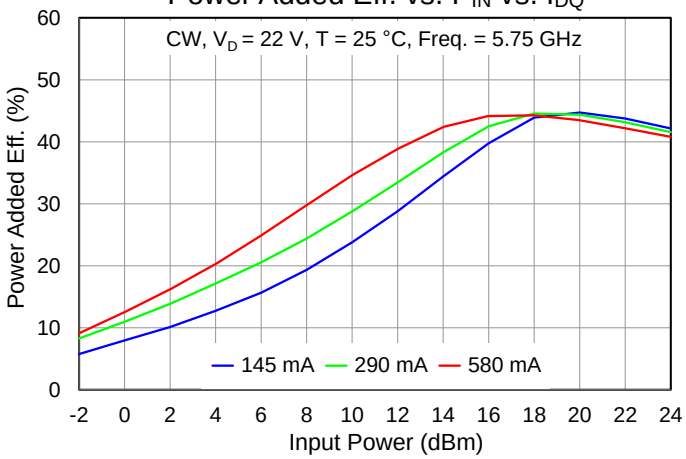
Performance Plots – Large Signal

Test conditions unless otherwise noted: **CW** V_D = 22 V, I_{DQ} = 290 mA, CW input power, T=+25 °C

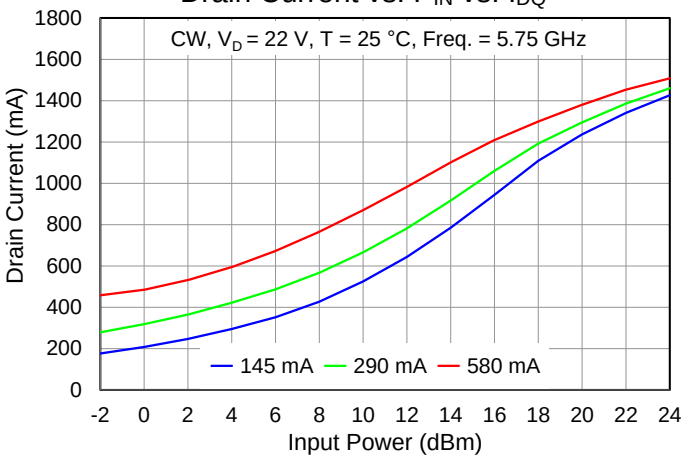
Output Power vs. P_{IN} vs. I_{DQ}



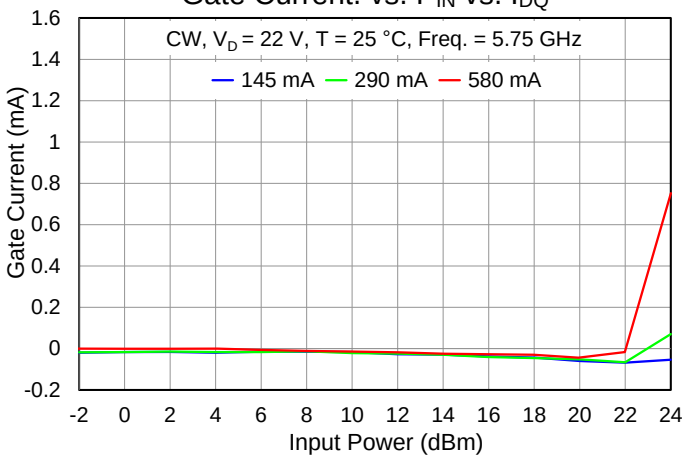
Power Added Eff. vs. P_{IN} vs. I_{DQ}



Drain Current vs. P_{IN} vs. I_{DQ}

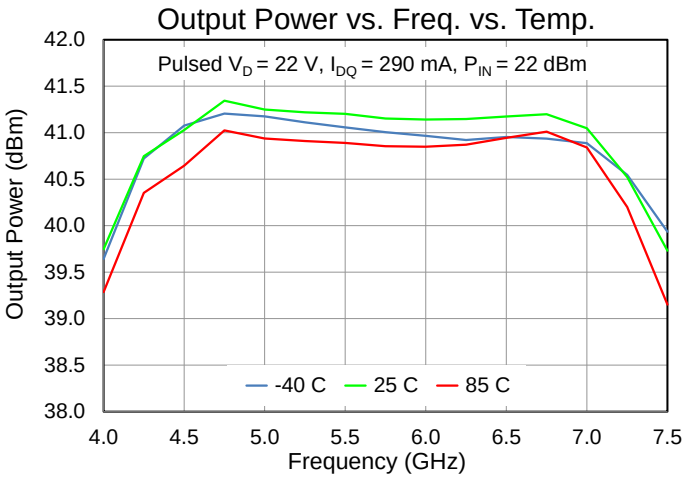


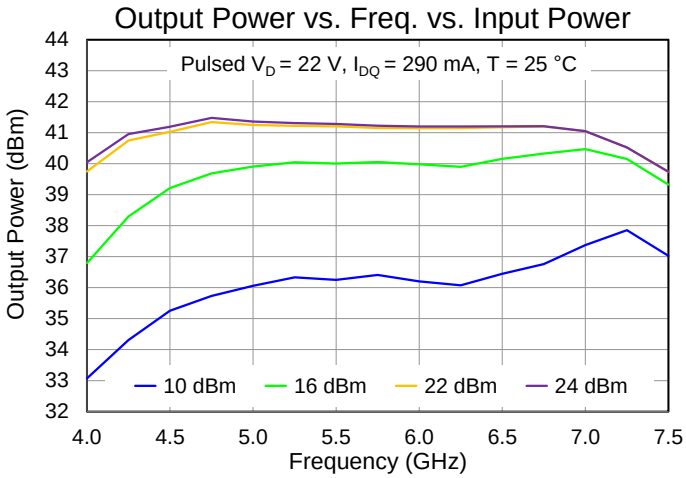
Gate Current. vs. P_{IN} vs. I_{DQ}

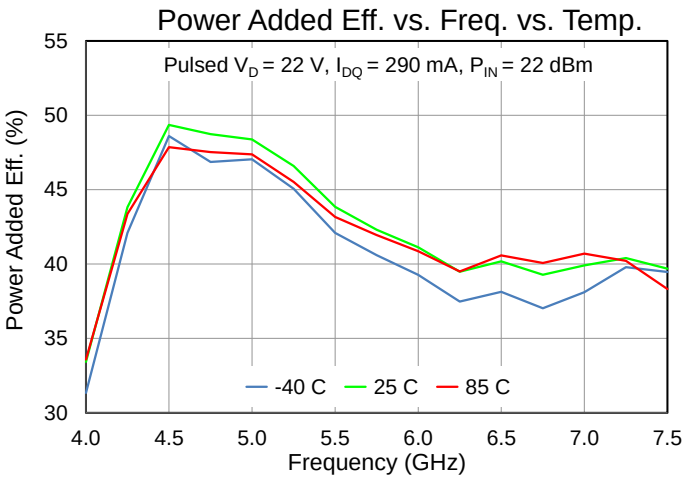


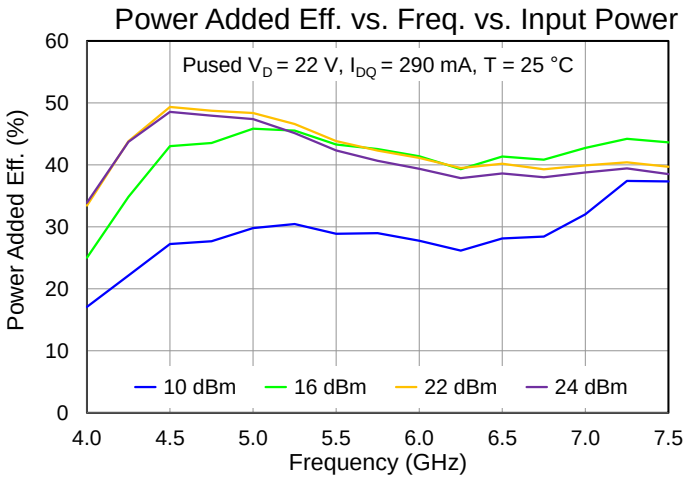
Performance Plots – Large Signal

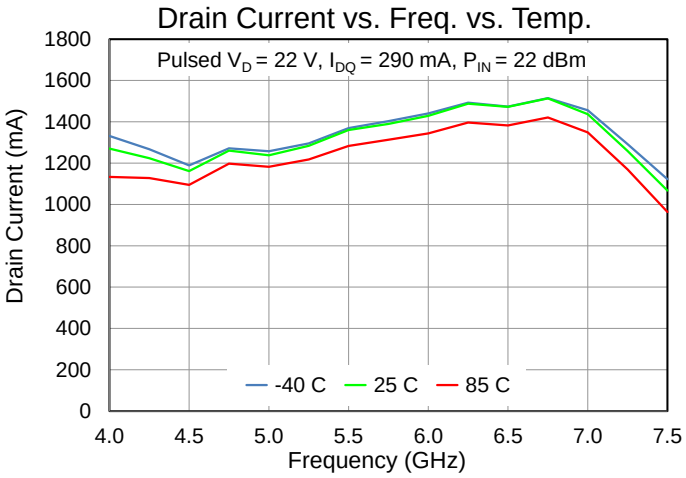
Test conditions unless otherwise noted: **Pulsed** V_D = 22 V, I_{DQ} = 290 mA, Duty Cycle = 10%, PW = 100 us, CW input power, T=+25 °C

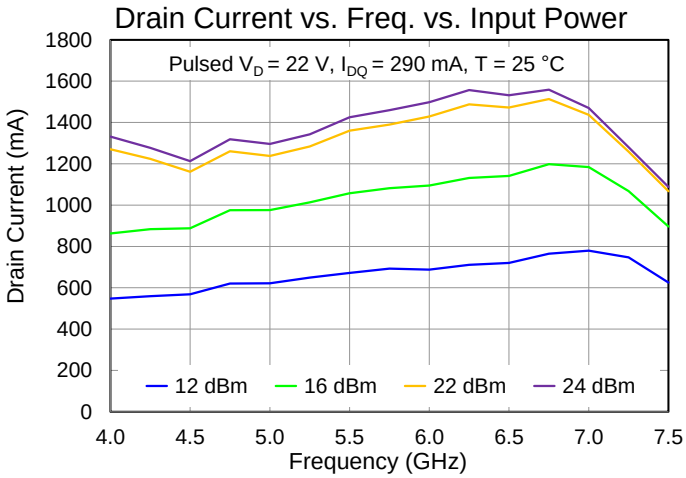








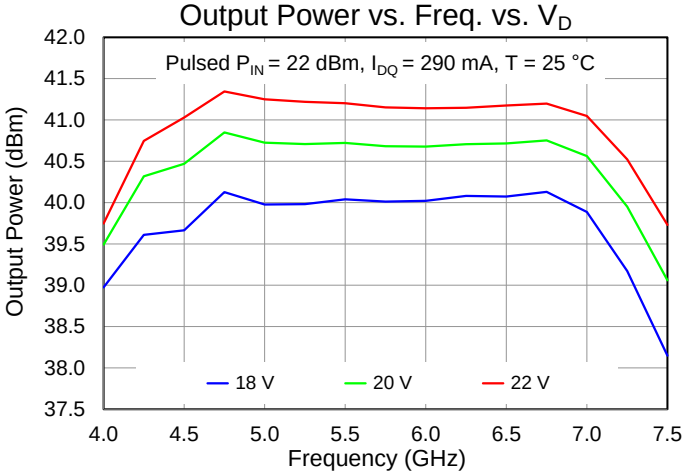




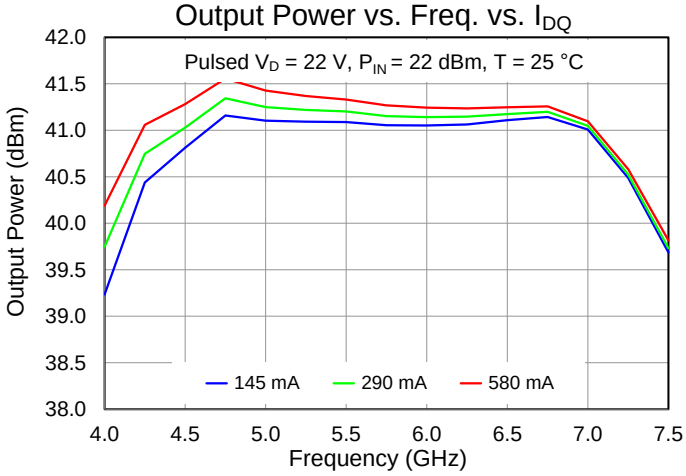
Performance Plots – Large Signal

Test conditions unless otherwise noted: **Pulsed** V_D = 22 V, I_{DQ} = 290 mA, Duty Cycle = 10%, PW = 100 us CW input power, T=+25 °C

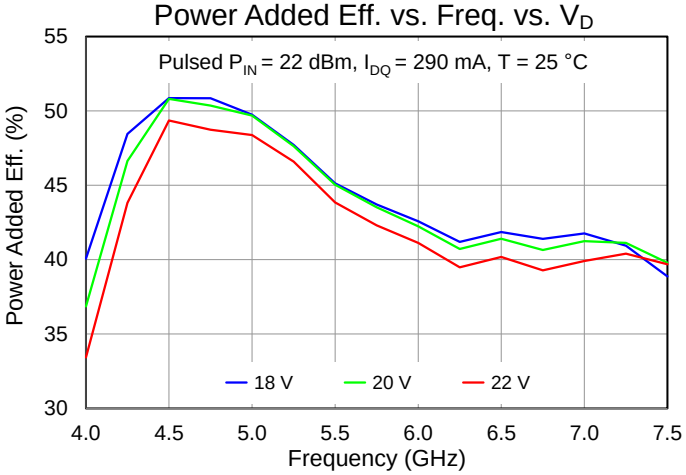
Output Power vs. Freq. vs. V_D



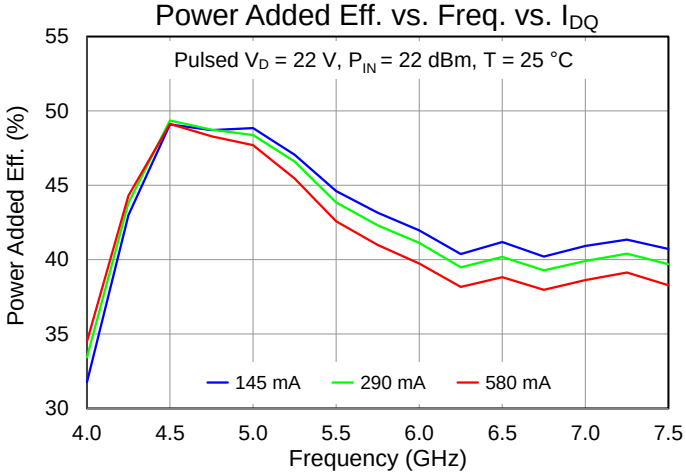
Output Power vs. Freq. vs. I_{DQ}



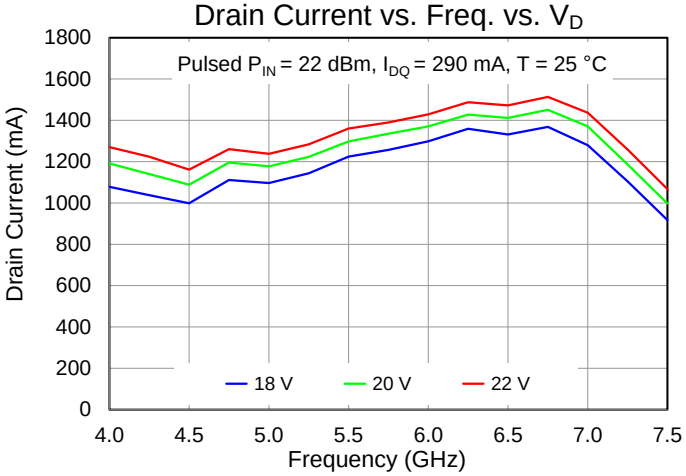
Power Added Eff. vs. Freq. vs. V_D



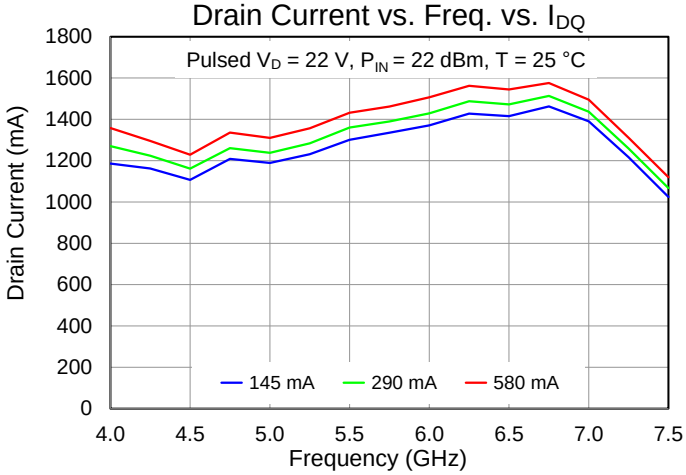
Power Added Eff. vs. Freq. vs. I_{DQ}



Drain Current vs. Freq. vs. V_D



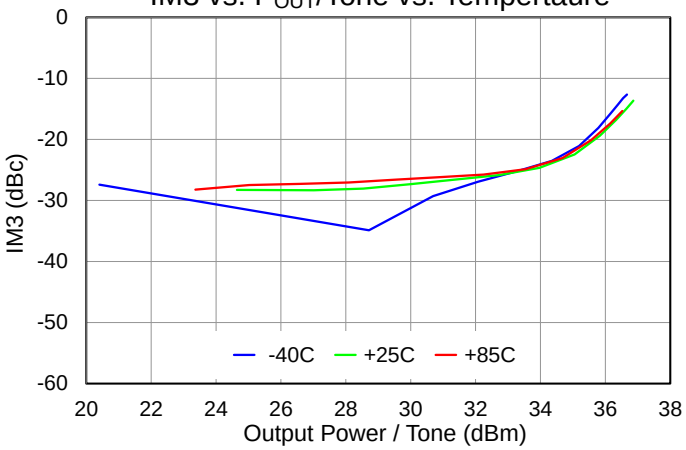
Drain Current vs. Freq. vs. I_{DQ}



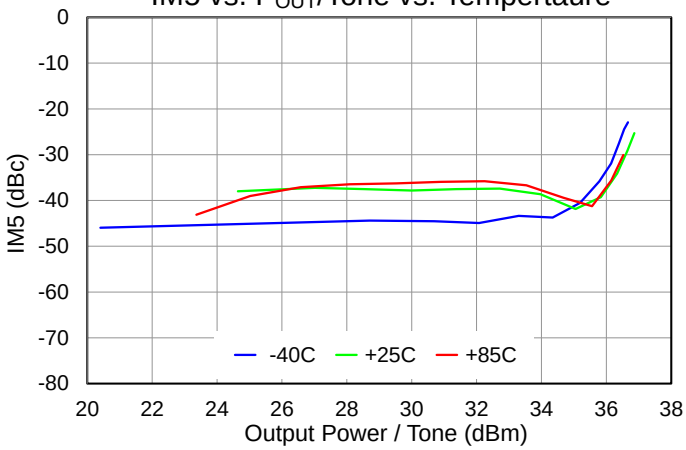
Performance Plots – Linearity

Test conditions unless otherwise noted: CW V_D = 22 V, I_{DQ} = 290 mA, CW input power, T=+25 °C, Freq. = 5.7 GHz, ΔF = 10 MHz

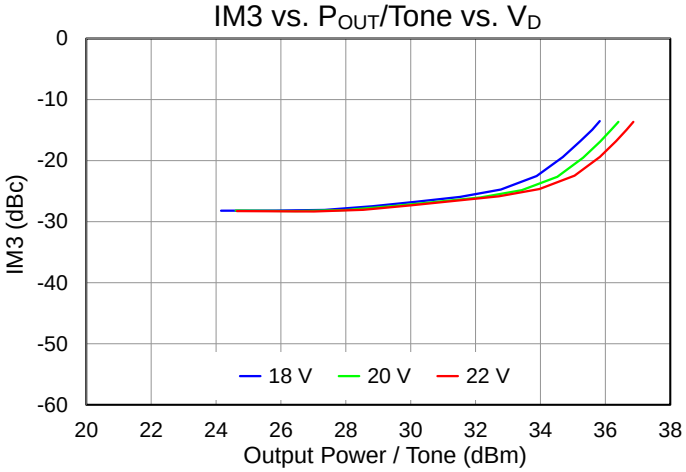
IM3 vs. P_{OUT}/Tone vs. Tempertaure



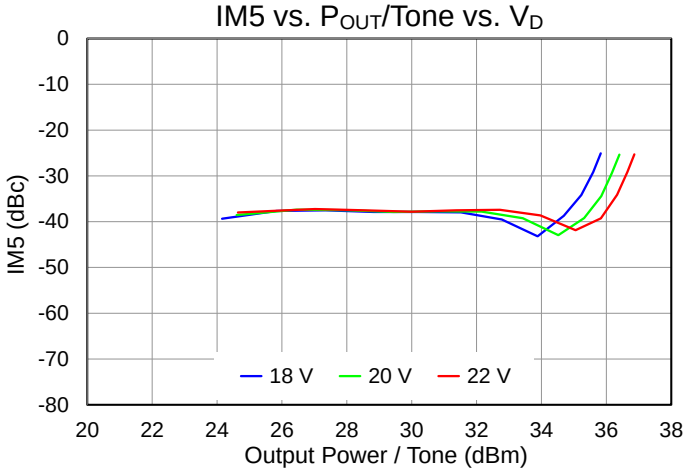
IM5 vs. P_{OUT}/Tone vs. Tempertaure



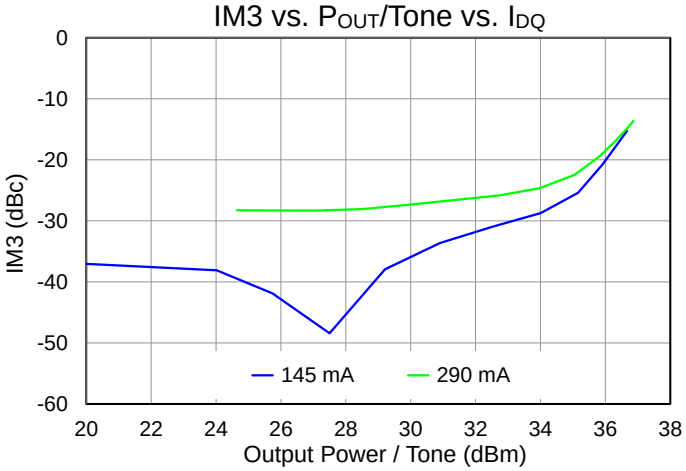
IM3 vs. P_{OUT}/Tone vs. V_D



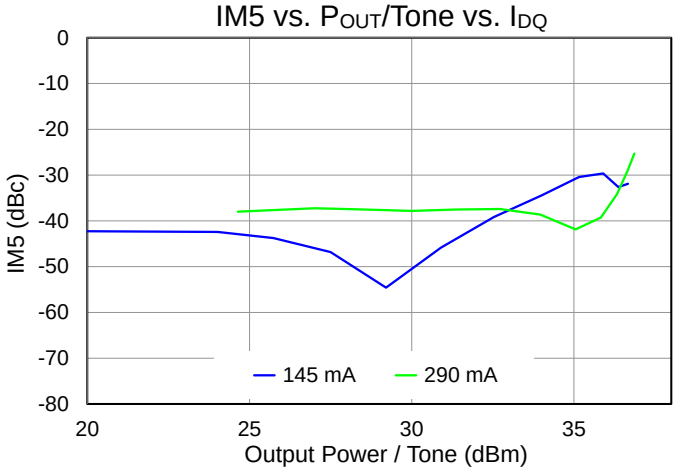
IM5 vs. P_{OUT}/Tone vs. V_D



IM3 vs. P_{OUT}/Tone vs. I_{DQ}



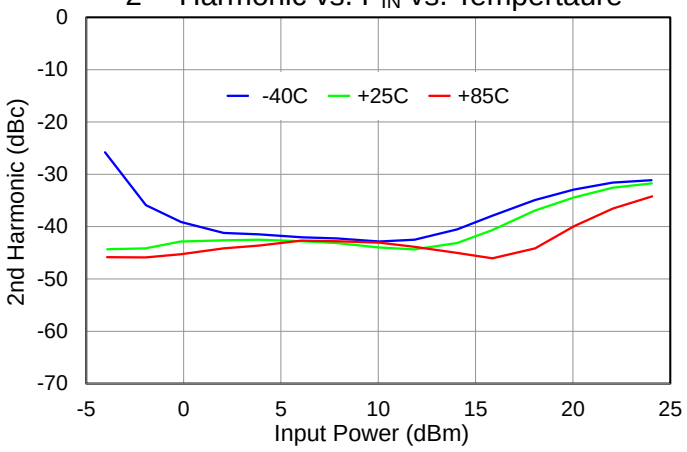
IM5 vs. P_{OUT}/Tone vs. I_{DQ}



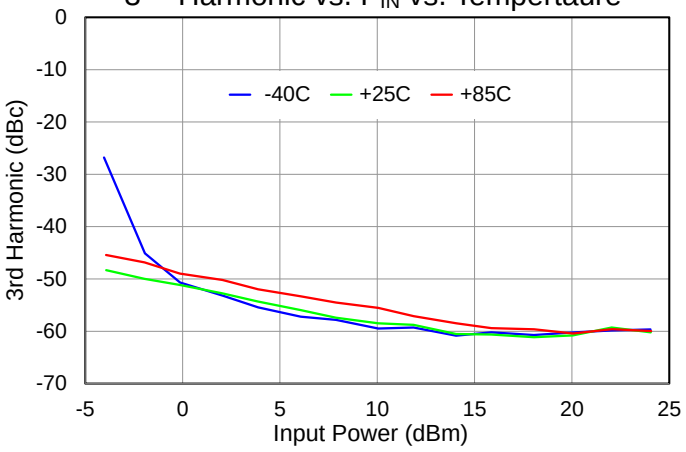
Performance Plots – Harmonics

Test conditions unless otherwise noted: CW V_D = 20 V, I_{DQ} = 290 mA, CW input power, T=+25 °C, Freq. = 5.7 GHz

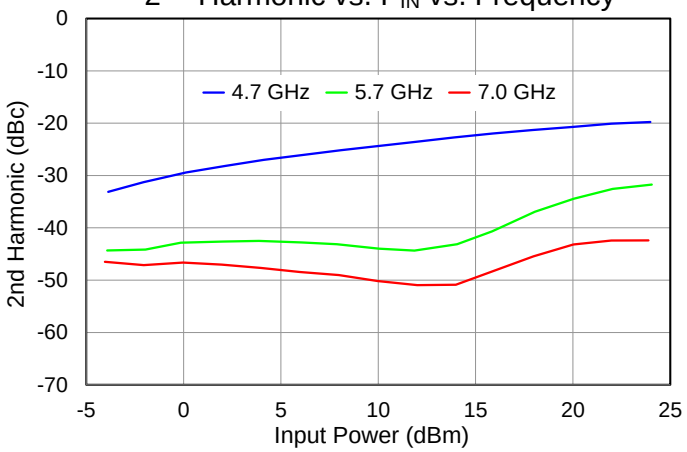
2ND Harmonic vs. P_{IN} vs. Tempertaure



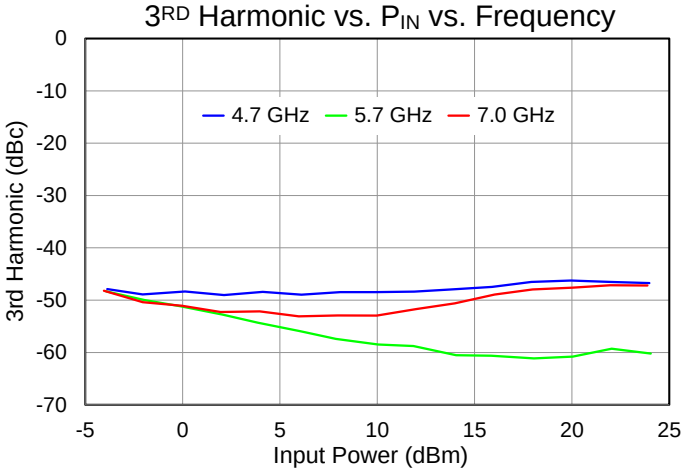
3RD Harmonic vs. P_{IN} vs. Tempertaure



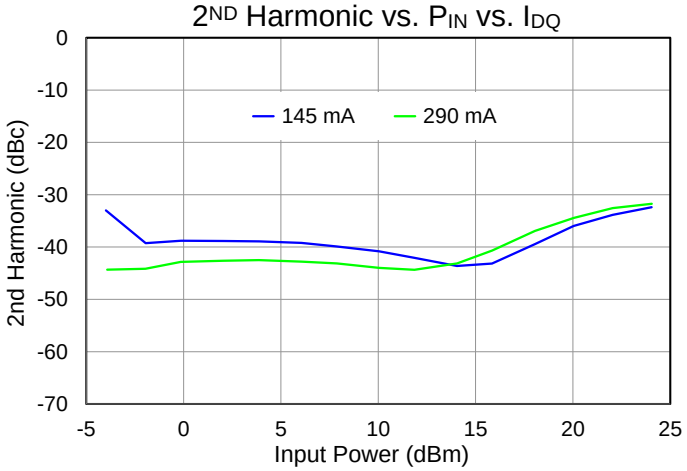
2ND Harmonic vs. P_{IN} vs. Frequency



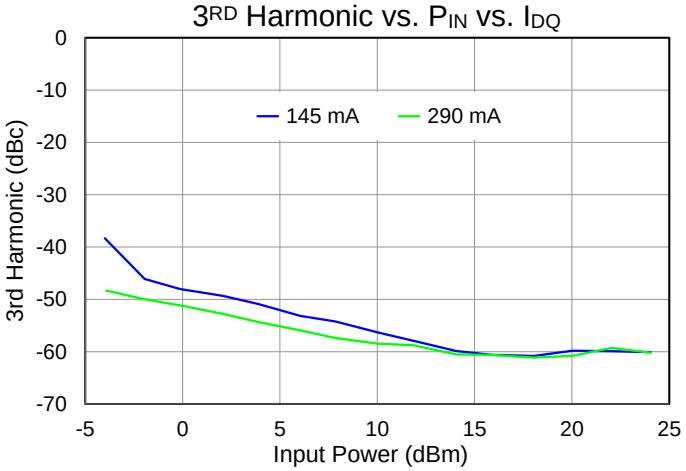
3RD Harmonic vs. P_{IN} vs. Frequency



2ND Harmonic vs. P_{IN} vs. I_{DQ}



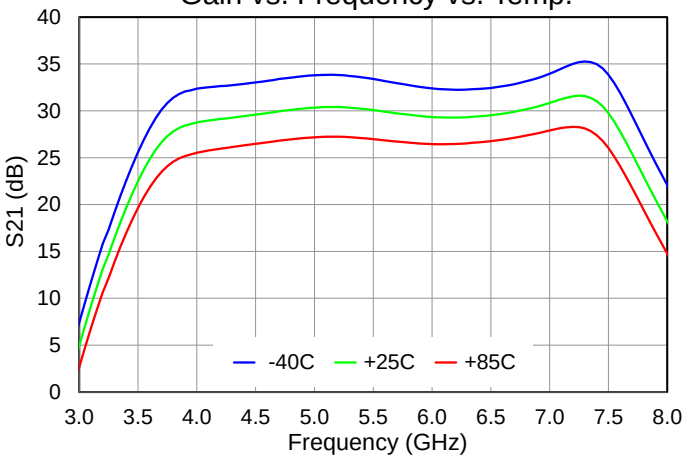
3RD Harmonic vs. P_{IN} vs. I_{DQ}



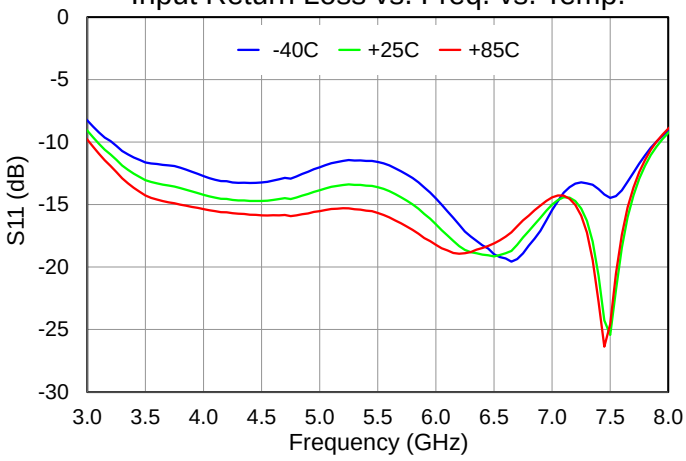
Performance Plots – Small Signal

Test conditions unless otherwise noted: CW V_D = 22 V, I_{DQ} = 290 mA, CW input power, T=+25 °C

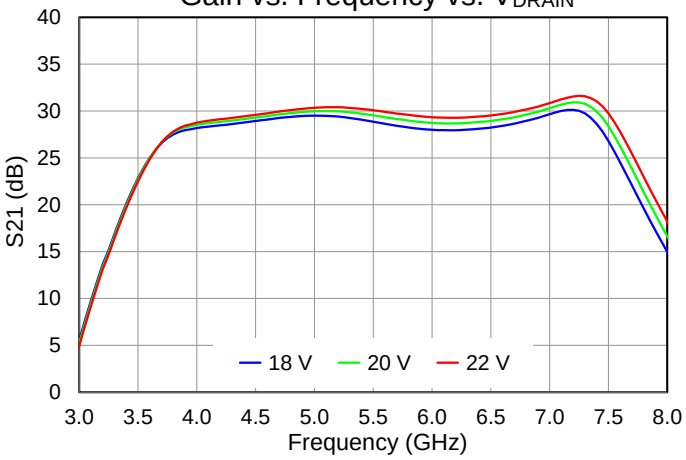
Gain vs. Frequency vs. Temp.



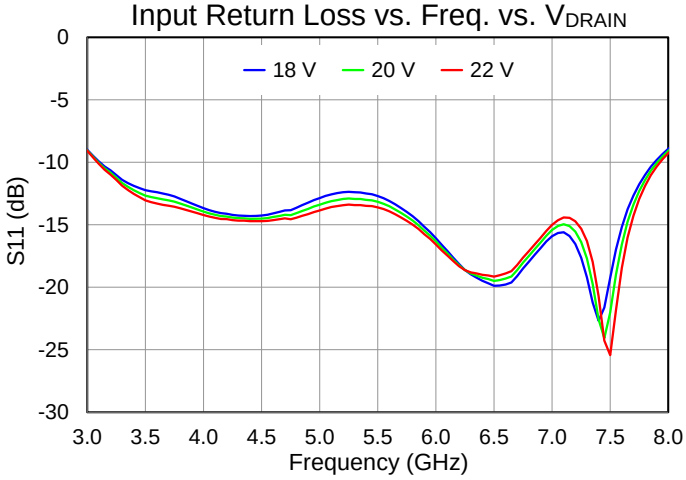
Input Return Loss vs. Freq. vs. Temp.



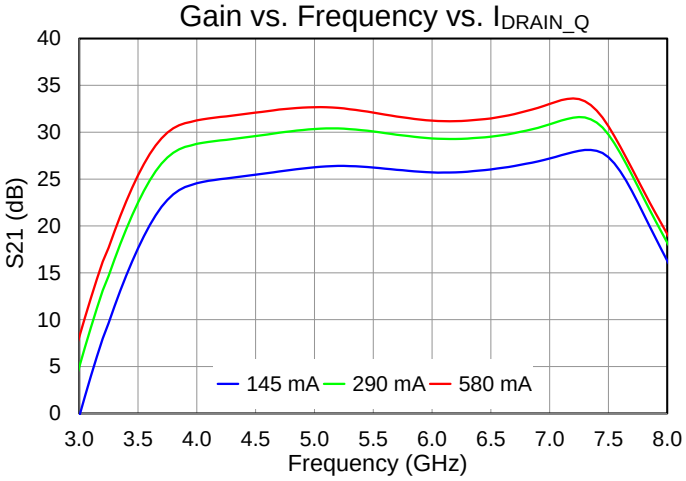
Gain vs. Frequency vs. V_{DRAIN}



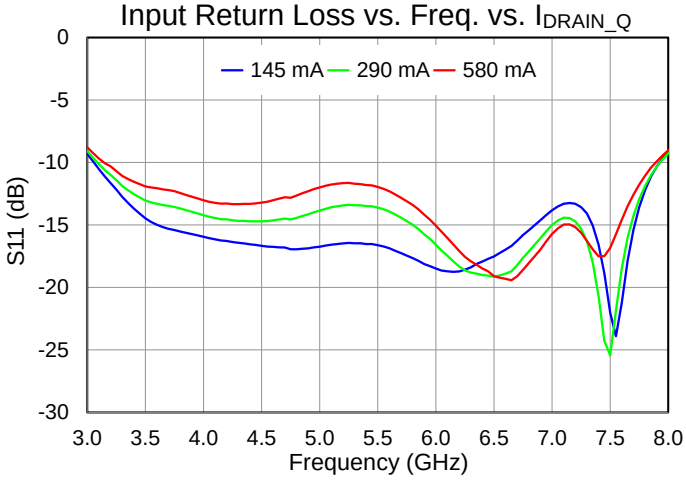
Input Return Loss vs. Freq. vs. V_{DRAIN}



Gain vs. Frequency vs. I_{DRAIN_Q}

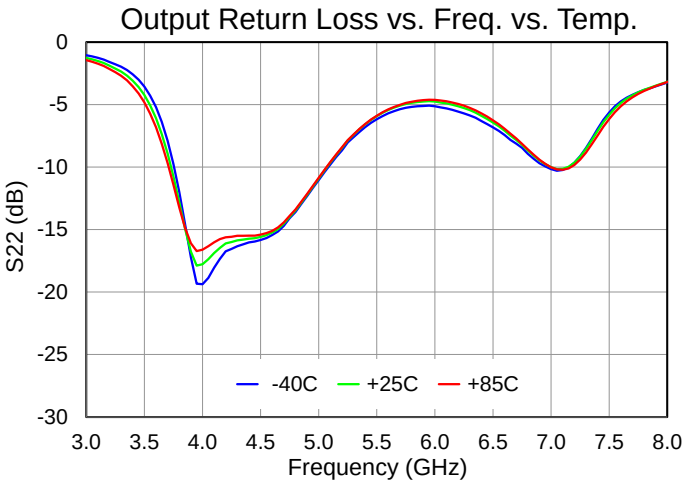


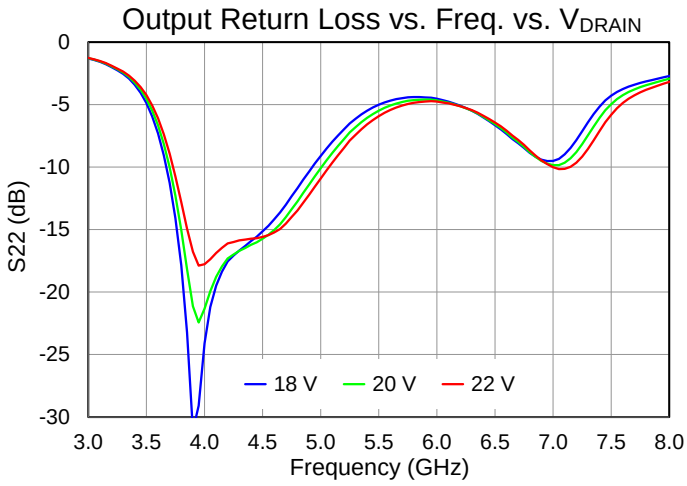
Input Return Loss vs. Freq. vs. I_{DRAIN_Q}

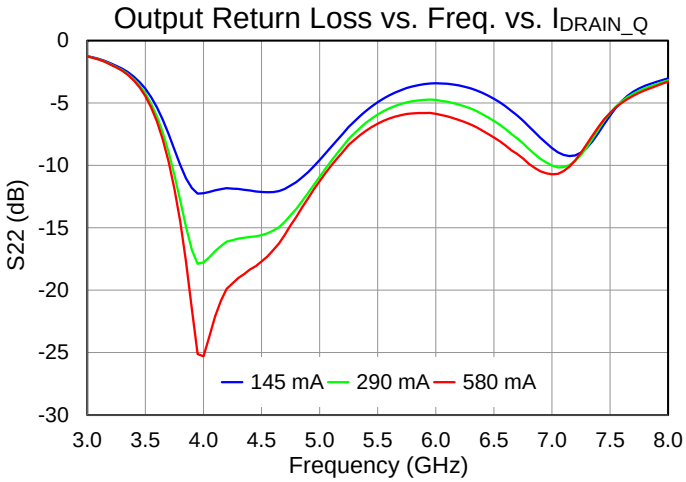


Performance Plots – Small Signal

Test conditions unless otherwise noted: CW V_D = 22 V, I_{DQ} = 290 mA, CW input power, T=+25 °C



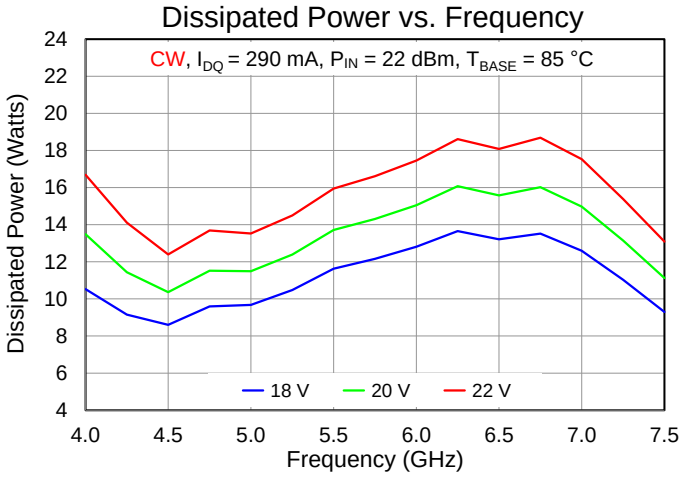


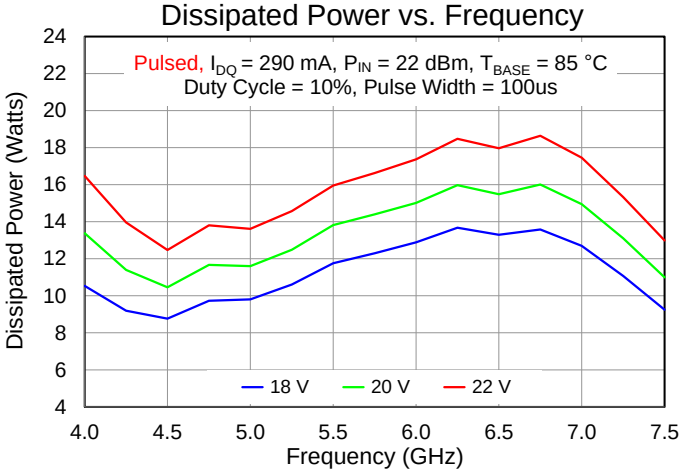


Thermal and Reliability Information

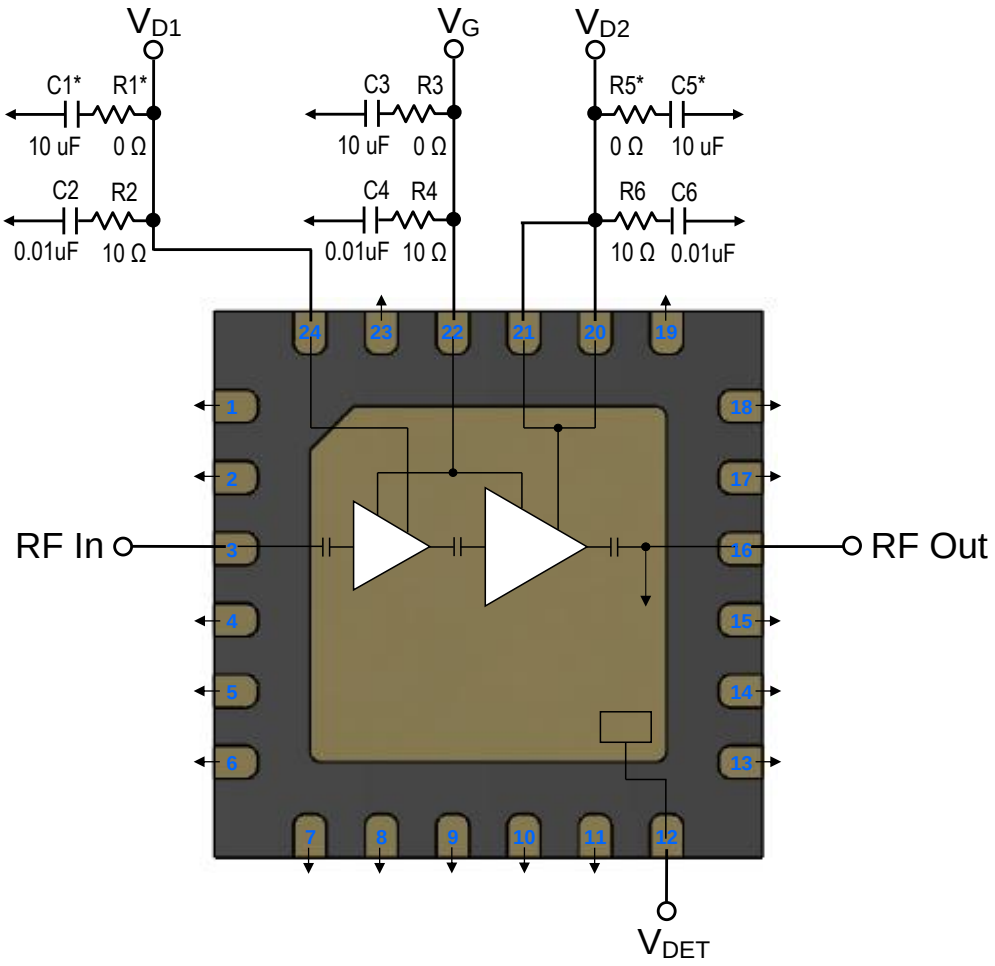
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C V_D = 22 V, I_{DQ} = 290 mA P_{DISS} = 6.38 W	3.20	ºC/W
Channel Temperature, T_{CH} (Quiescent) (2)		105	°C
Median Lifetime (T_M)		6.5E+11	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, CW V_D = 22 V, I_{DQ} = 290 mA, Freq = 6.5 GHz, I_{D_Drive} = 1.38 A, P_{IN} = 22 dBm, P_{OUT} = 41 dBm, P_{DISS} = 17.9 W	3.26	ºC/W
Channel Temperature, T_{CH} (Under RF) (2)		143	°C
Median Lifetime (T_M)		7.6E+08	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, Pulsed V_D = 22 V, I_{DQ} = 290 mA, Freq = 6.5 GHz, I_{D_Drive} = 1.38 A, P_{IN} = 22 dBm, P_{OUT} = 41 dBm, P_{DISS} = 17.9 W	2.13	ºC/W
Channel Temperature, T_{CH} (Under RF) (2)		123	°C
Median Lifetime (T_M)		2.3E+10	Hrs

Notes:
1. Thermal resistance determined to the back of package (85 °C)
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note “GaN Device TCHMAX Theta-JC and Reliability Estimates,” located here https://www.qorvo.com/products/d/da006480





Applications Circuit



* Remove C1, C5, R1, R5 for pulsed drain operation

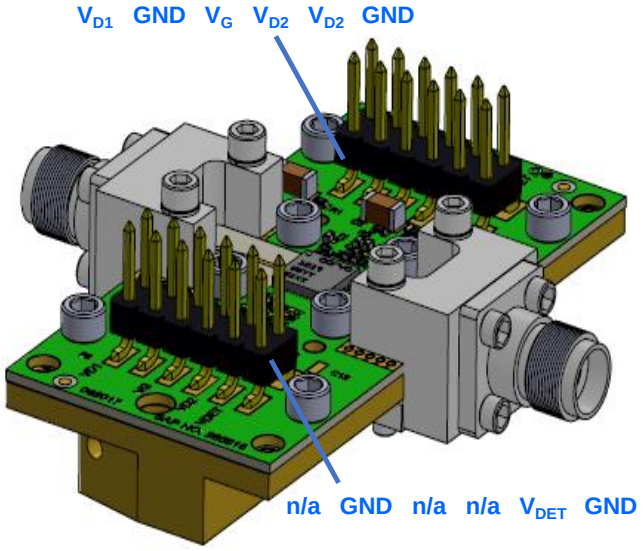
Bias-Up Procedure

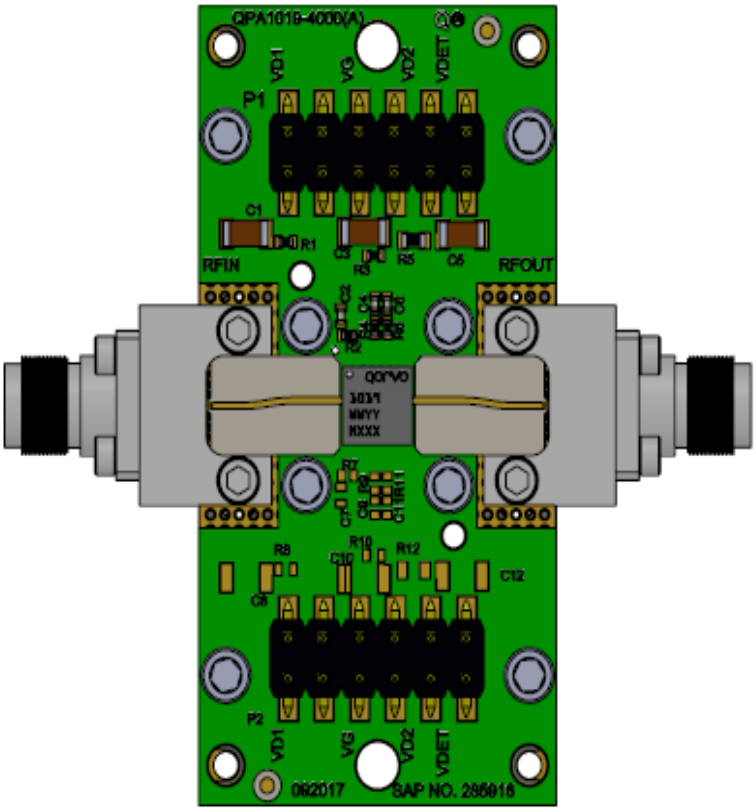
1. Set I_D limit (CW) to 2000 mA, I_G limit to 20 mA
2. Set V_G to −5.0 V
4. Set V_D +22 V
5. Adjust V_G more positive until I_{DQ} ≈ 290 mA (V_G ~ −2.5 V +/- Typical)
6. Apply RF signal

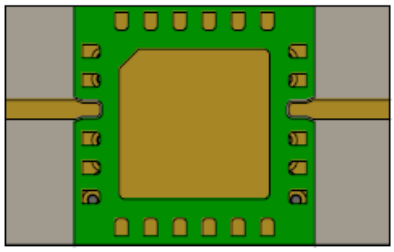
Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to −5.0 V. Ensure I_{DQ} ~ 0mA
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_G supply

Application Evaluation Board (CW)







PCB Mounting

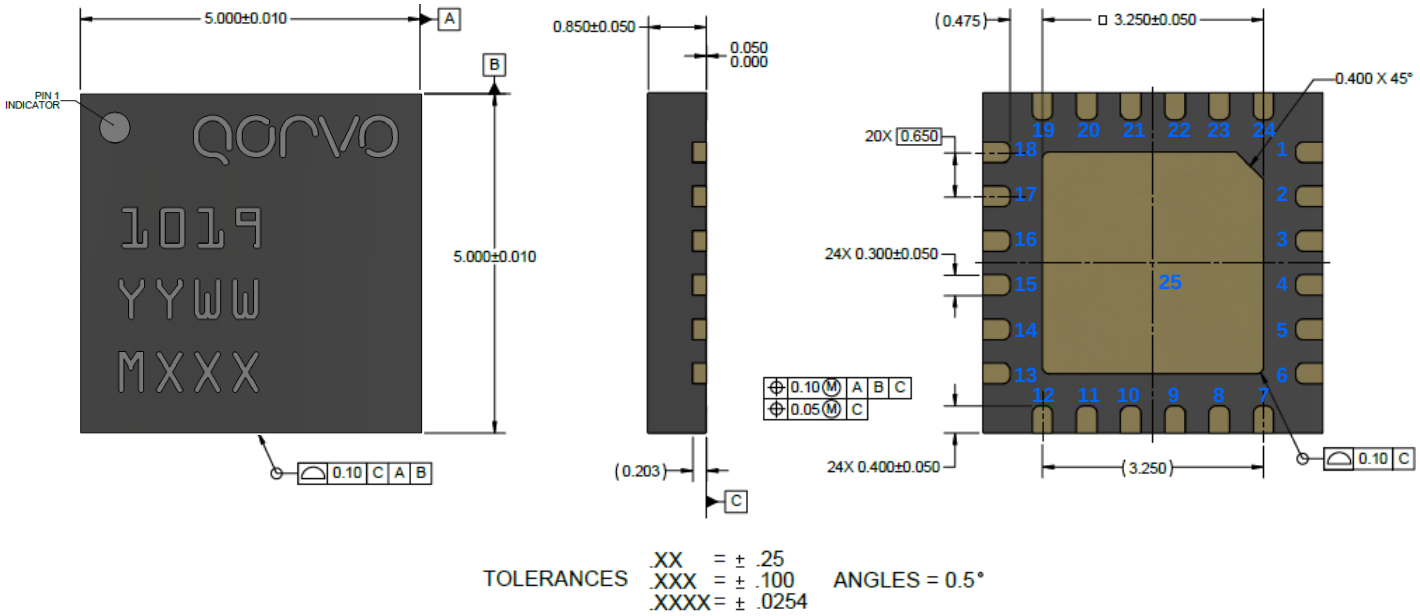
Notes:

1. RF PCB is Rogers 4003C; dielectric is 8 mil thick, copper cladding is ½ oz. copper both sides, plated to 1 oz
2. Copper Slug placed under the DUT to improve thermal and electrical performance

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1, C3, C5	10 uF	CAP, 10uF, 20%, 50V, 20%, X5R, 1206	Various	
C2, C4, C6	0.01 uF	CAP, 0.01uF, ±10%, 50V, X7R, 0402	Various	
R1, R3	0 Ω	RES, 0 OHM, JMPR, 0402	Various	
R2, R4, R6	10 Ω	RES, 10 OHM, 5%, 0.1W, 0402	Various	
R5	0 Ω	RES, 0 OHM, JMPR, 0603	Various	
H1, H2	-	Header, connector 2x6, SMD		
J1, J2	-	Connector, Female, End Launch, 1092-01A-5	Southwest Microwave	1092-01A-5
S1 – S7		Screw, Cap, socket head, 2-56x1/8”		
PCB	-	Rogers 4003C, 8 mil dielectric, 1 oz. copper (gold plated), 2 layers	Rogers Corp.	Custom
Carrier	-	T-Carrier, Copper C110, 1.744 x 2.201 x 0.275”		Custom
Solder	-	Paste, solder, syntech, Sn62/Pb36/Ag2		
Epoxy	-	Preform Epoxy, 0.986 x 1.996 x 0.003T		

Mechanical Information



Notes: unless otherwise specified;

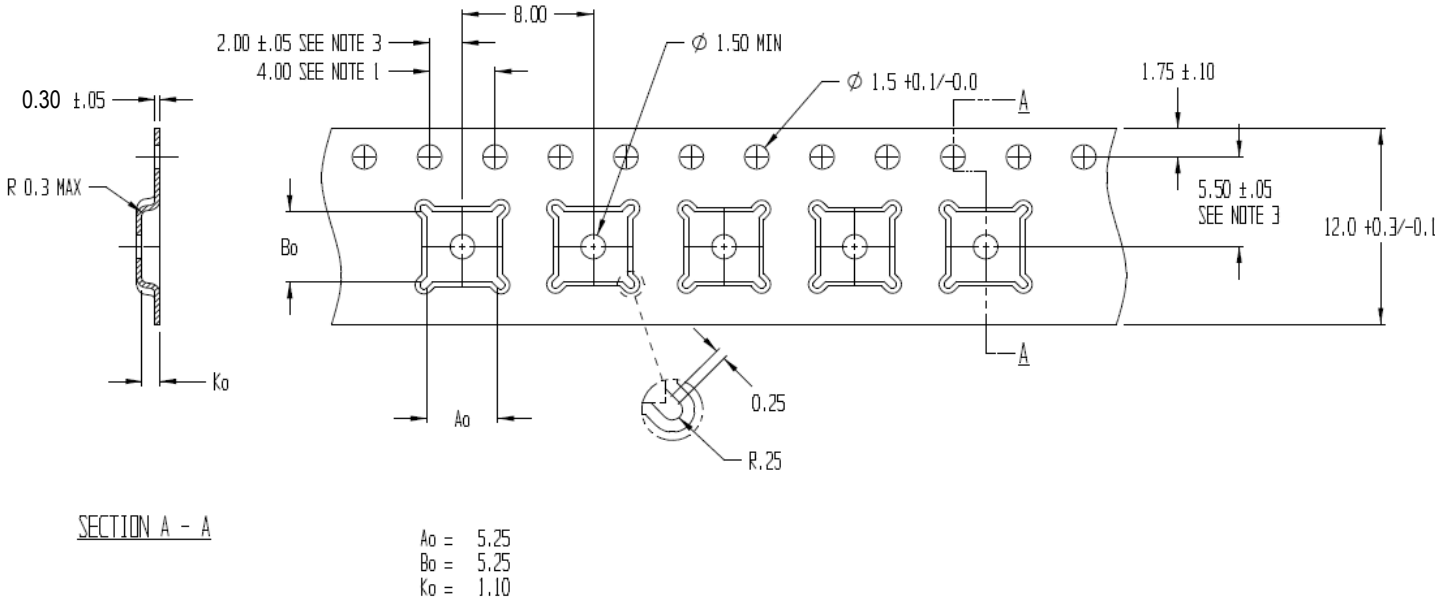
1. Dimensions: millimeters (mm)
2. Package leads are gold (Au) plated
3. Marking: YY is calendar year; WW is assembly week; MXXX is batch ID

Pin Description

Pin Number	Symbol	Description
1-2, 4-11, 13-15, 17-19, 23	NC	No internal connection. Recommend grounding at the PCB level.
3	RF Input	RF Input; matched to 50 Ω, DC blocked
12	V_{DET}	Output Power Detector Voltage
16	RF Output	RF Output; matched to 50 Ω, DC blocked, DC grounded
20, 21	V_{D2}	Drain voltage for stage 2. Bias network is required; see Application Circuit on page 14 as an example.
22	V_G	Gate voltage. Bias network is required; see Application Circuit on page 14 as an example.
24	V_{D1}	Drain voltage for stage 1. Bias network is required; see Application Circuit on page 14 as an example.
25	GND	Ground connection (center pad)

Tape and reel Information

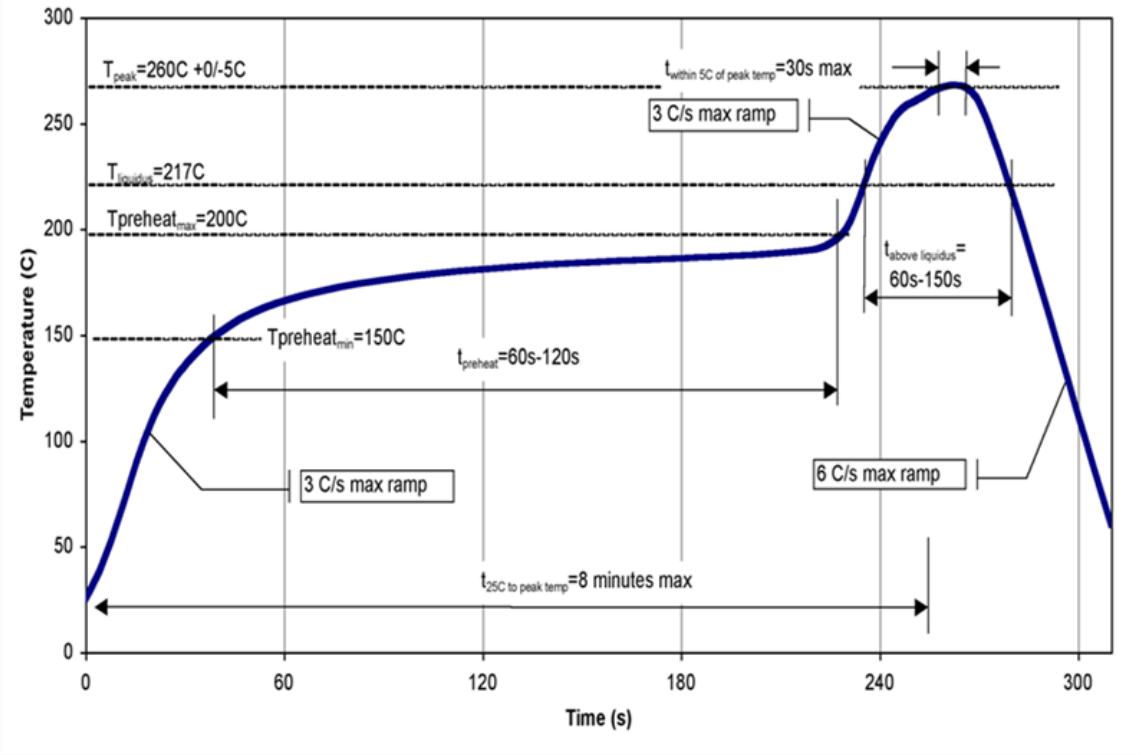
Standard T/R size = 250 pieces on a 7” reel
Dimensions: millimeters (mm)
Tolerances unless otherwise noted: .X = ± .2; .XX = ± .10



Solderability

- Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C
- Do not expose the package lid to temperatures > 280 °C

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	C3	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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