Qualcomm Technologies, Inc.

QRB2210 Data Sheet

Data Sheet
80-30843-1 Rev. AE
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Device description

The QRB2210 chip is the next generation entry-tier IoT platform based on the Snapdragon® processor.

Key processor and memory characteristics include:

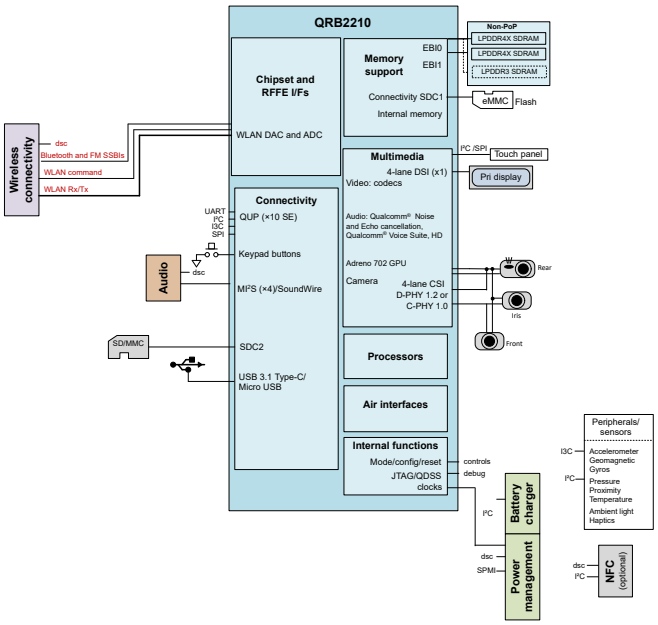
- 12 mm × 12.4 mm non-package-on-package (non-PoP), 0.4 mm pitch
- Customized 64-bit Arm Cortex-A53 Quad-core applications processor at 2.0 GHz
- Qualcomm® Adreno™ 702 graphics processing unit (GPU) 845 MHz with 64-bit addressing
- Dedicated DSP shared between Snapdragon sensor core and low-power audio subsystem
- Dual-channel non-PoP high-speed memory, LPDDR4X SDRAM designed for 1804 MHz clock (2 × 16 bit) and LPDDR3 SDRAM designed for 933 MHz clock (1 × 32 bit)
- Always-on subsystem with RPM for power management

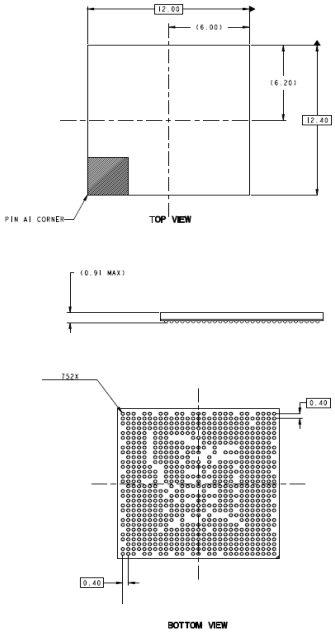
Key features

See Section 1.2 for more information.

- Qualcomm® Universal bandwidth compression (UBWC) with GPU
- Display support: HD+, 720 × 1680 at 60 Hz, 10 bit end-to-end, and up to four hardware layer composition. Features Qualcomm® Low-Power Picture Enhancement (SVI, CABL, VRR, and Q-Sync) and Qualcomm® True Palette Display (Color tuning, picture adjust, and gamut mapping).
- One 4-lane DSI D-PHY 1.2 at 1.5 Gbps per lane with split link support
- 2x ISP (13 MP + 13 MP or 25 MP) at 30 fps ZSL
- Two 4-lane CSIs (4/4 or 4/2/1) D-PHY 1.2 at 2.5 Gbps per lane or C-PHY 1.0 at 10 Gbps (3.42 Gbps/trio)
- Support for eMMC 5.1, SD 3.0, and USB 3.1 Type-C/Micro USB
- WCN3910: WLAN 1 × 1 802.11b/g/n, Bluetooth 5.0, and FM
- WCN3950: WLAN 1 × 1 802.11a/b/g/n/ac, Bluetooth 5.0, and FM

QRB2210 high-level block diagram and NSP752 drawing





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1 Introduction

This topic provides the functional block diagram and the device features.

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

This functional block diagram shows the overall representation of the subsystems on this chipset.

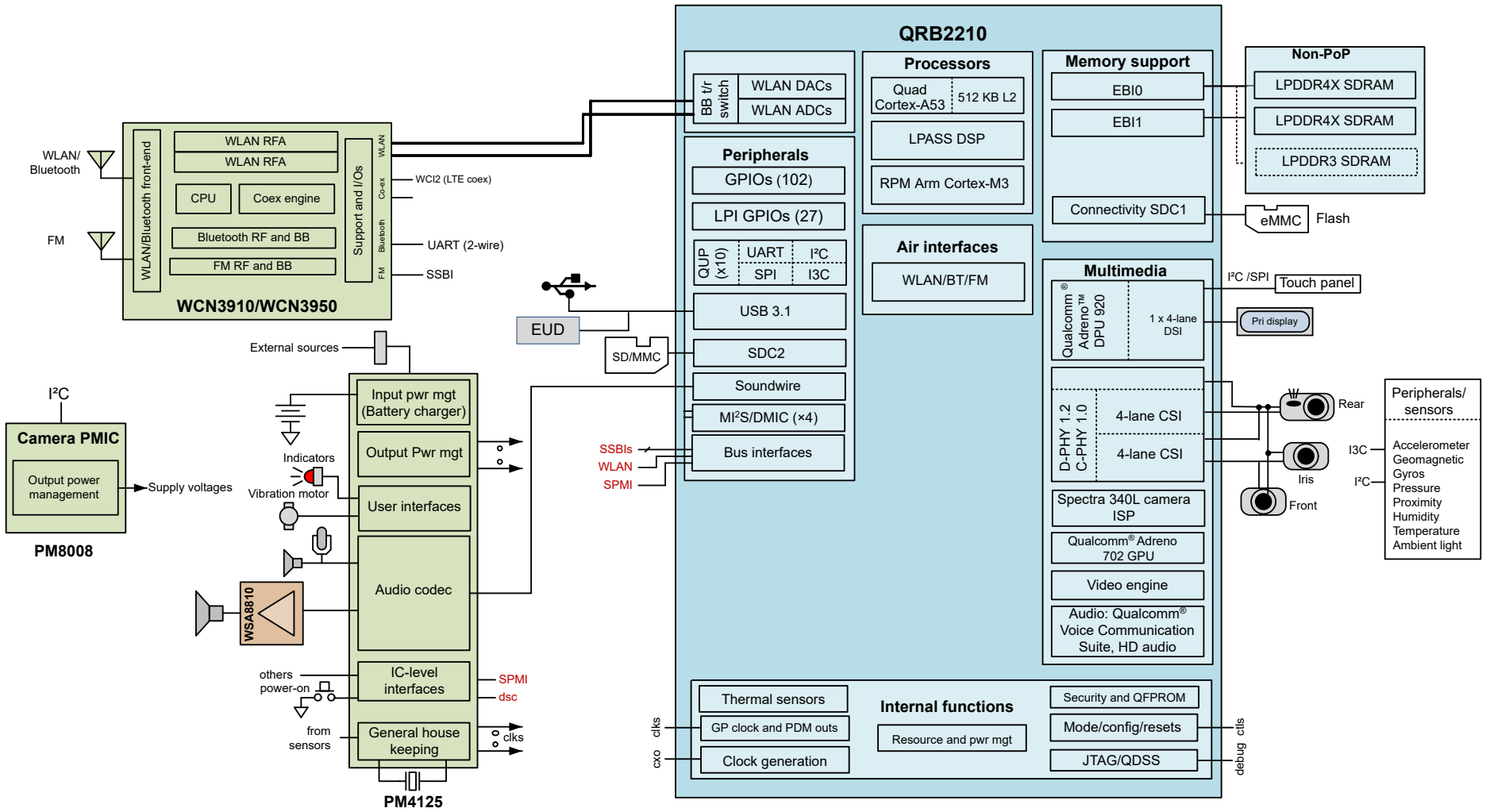


Figure 1-1 QRB2210 functional block diagram

1.2 QRB2210 features

This table lists the comprehensive features of the QRB2210 chipset and its capabilities.

NOTE Some hardware features integrated within the QRB2210 chip must be enabled by software. See the latest revision of the applicable software release notes to identify the enabled QRB2210 features.

Processors

Function	Description
Applications	64-bit applications processor ■ Arm Cortex-A53 quad-cores at 2.0 GHz with 512 kB L2 cache
Always-on system	Always-on subsystem with always-on processor power management (RPM) for voltage control and regulation, clock management, and resource communication
LPASS	QDSP6 v66 K ■ 512 kB L2 cache ■ Audio and sensor processing

Memory support

Function	Description
System memory via EBI	■ Dual-channel non-PoP high-speed memory – LPDDR4X SDRAM designed for a 1804 MHz clock (2 × 16-bit) ■ Single-channel non-PoP high-speed memory – LPDDR3 SDRAM designed for a 933 MHz clock (1 × 32-bit)

External memory

Function	Description
Via	eMMC 5.1 and SD 3.0

RF support

Function	Description
WLAN/Bluetooth	Yes (with WCN3910 and WCN3950)
Antenna sharing	Antenna shared between Wi-Fi and WAN

Multimedia

Function	Description
Display support	
MIPI-DSI	One 4-lane DSI D-PHY 1.2 port, up to 1.5 Gbps per lane with split link support
General display features	■ HD+, 720 × 1680 at 60 Hz, 10-bit end-to-end, and up to four hardware layer composition ■ Features Qualcomm® Low-Power Picture Enhancement (SVI, CABL, VRR, and Q-Sync) and Qualcomm® True Palette Display (color tuning, picture adjust, and gamut mapping)
Mobile display processor	Adreno DPU 920
Camera support	

Function	Description
Camera interfaces	2x ISP (13 MP + 13 MP or 25 MP) at 30 fps ZSL
MIPI-CSI	MIPI combination D-PHY 1.2 /C-PHY 1.0 configurable in 4/4 or 4/2/1 ■ D-PHY: 2.5 Gbps/lane ■ C-PHY: ~10 Gbps (3.42 Gbps/trio on three trios per port)
Performance	■ Real-time sensor input resolution: 25 MP or 13 MP + 13 MP ■ 25 MP 30 ZSL with a dual ISP ■ 48 MP resolution in nZSL mode ■ 13 MP 30 ZSL with a single ISP
Video applications performance	
Encode	■ 1080p30 8-bit HEVC (H.265) ■ 1080p30 8-bit H.264
Decode	■ 1080p30 8-bit H.264 ■ 1080p30 8-bit HEVC (H.265), VP9
Concurrency	1080p 30 decode + 720p 30 encode
HFR capture	480p 120
Graphics performance	
Graphics	■ Adreno 702 at 845 MHz, 3D graphics accelerator with 64-bit addressing ■ OpenGL ES 3.1, Vulkan 1.1 ■ OpenCL 2.0
Audio Integrated codec in PM4125, WSA8810 (optional)	
Voice UI	■ Support for two voice activation engines ■ Integrated low-power island for voice activation ■ Supports always-on noise suppression
Low-power voice activation	Supported
Low-power audio	Low power; 7.1 surround sound
Speaker amplifier	WSA8810 in analog mode
Audio interfaces	SLIMbus: WCN Bluetooth/FM SLIMbus SWR: SoundWire interface (two Tx and two Rx data lines) for codec Digital mic: Four DMICs 4 × MI2S: Three MI2S with 2x data lanes to support full duplex stereo, or up to 4 channel Tx/Rx application One MI2S supports four data lanes for up to eight channels Tx/Rx application
Voice codec	EVS, EVRC, EVRC-B, EVRC-WB G.711 and G.729A/AB GSM-FR, GSM-EFR, and GSM-HR AMR-NB and AMR-WB
Voice processing	Qualcomm® Noise and Echo Cancellation and Qualcomm® Voice Suite
Audio codec support	MP3; AAC; HE AAC v1, v2; FLAC; APE; ALAC; AIFF
Enhanced audio	DSP-offload for low-power audio playback
Sensors	QUP (×4 in LPI) dedicated for sensors

Connectivity

Interface	Description
Qualcomm universal peripheral (QUP) ports	10 serial engines
UART	UART interface; six on GPIO and three on LPI GPIO
I^2C	I^2C interface; six on GPIO and three on LPI GPIO for touch, sensors, and NFC; dedicated controller for each port
I3C	I3C interface; one on GPIO and two on LPI GPIO
SPI	SPI interfaces; six on GPIO and one on LPI GPIO for sensors and so on.
CCI I^2C	Two dedicated I^2C interfaces for camera.
USB	USB 3.1 Type-C/Micro USB
PWM	Nine
Secure digital interfaces	■ 8-bit port SDC1 and 4-bit port SDC2; eMMC5.1 and SD 3.0 ■ SDC2 is dual-voltage
Wireless connectivity	WCN3910 1 × 1 802.11b/g/n WCN3950 1 × 1 802.11a/b/g/n/ac
Touchscreen support	Capacitive panels via ext IC (I^2C, SPI, and interrupts)

Configurable GPIOs

Function	Description
Number of GPIO ports	102
Number of LPI GPIO ports	27
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs

Internal functions

Function	Description
Security	
General hardware security features	Secure boot, secure debug, secure key provisioning, TrustZone, Qualcomm ® Trusted Execution Environment, hardware supported KeyStore
Crypto engines	Crypto engine v5 (CE5), DRBG/PRNG (FIPS-compliant), inline crypto engine (FIPS-compliant), HWKM and HW ECC
TrustZone services	Secure file system, fast trusted storage
DRM support in hardware	PlayReady SL2000/SL3000, Widevine level 1, ISDB-T, and CPZ for GPU and DSP
PLLs and clocks	■ Multiple clock regimes; watchdog and sleep timers ■ Input: 19.2 MHz CXO ■ General-purpose outputs: M/N counter and PDM
Debug	JTAG, QDSS, embedded USB debug (EUD), and ETM
Others	Thermal sensors, modes and resets, and peripheral subsystem

Chipset and Qualcomm RF interface features

Function	Description
Power management	■ PM4125 □ Four switching regulators and 22 LDOs □ Chipset clock subsystem and general housekeeping □ Integrated switching charger □ Qualcomm® Battery Gauge and user interfaces supply ■ PM8008 □ Dedicated camera PMIC with seven LDOs
Wireless connectivity	
WLAN baseband data	I/Q differential pair interface
Bluetooth	UART interface

Fabrication technology and package

Function	Description
Non-PoP – small, thermally efficient package	NSP752: 12 mm × 12.4 mm × 0.91 mm; 0.4 mm pitch

2 Pin definitions

This topic explains the pin assignments of the QRB2210 chipsets. The figure and table within this topic provide details on pinouts, pad attributes, and their corresponding definitions.

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (interfaces does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High impedance (Hi-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
EBI	Pad group for EBI pads
P2	Pad group 2 (SDC2); 1.8 V or 2.95 V
P3	Pad group 3 (most peripherals); 1.8 V
P5	Pad group 5; 1.8 V or 2.95 V
P6	Pad group 6; 1.8 V or 2.95 V
P7	Pad group 7 (eMMC); tied to VDD_P7 pins (1.8 V only)
P11	Pad group 11 (CXO); 1.8 V
CSI	Supply voltage for MIPI_CSI circuits and I/Os; tied to VDD_MIPI_CSI_1P2 (1.2 V)
DSI	Supply voltage for MIPI_DSI circuits and I/Os; tied to VDD_MIPI_DSI_1P2 (1.2 V)

2.2 Pin assignments

2.2.1 Pin map

The QRB2210 is available in the package NSP752. A high-level view of the pin assignments is shown in the following figure. For more information about package details and to create printed circuit board (PCB) footprint, see Chapter 4.

QRB2210 Pin Assignment and GPIO Configuration Spreadsheet (80-30843-1A) lists all QRB2210 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

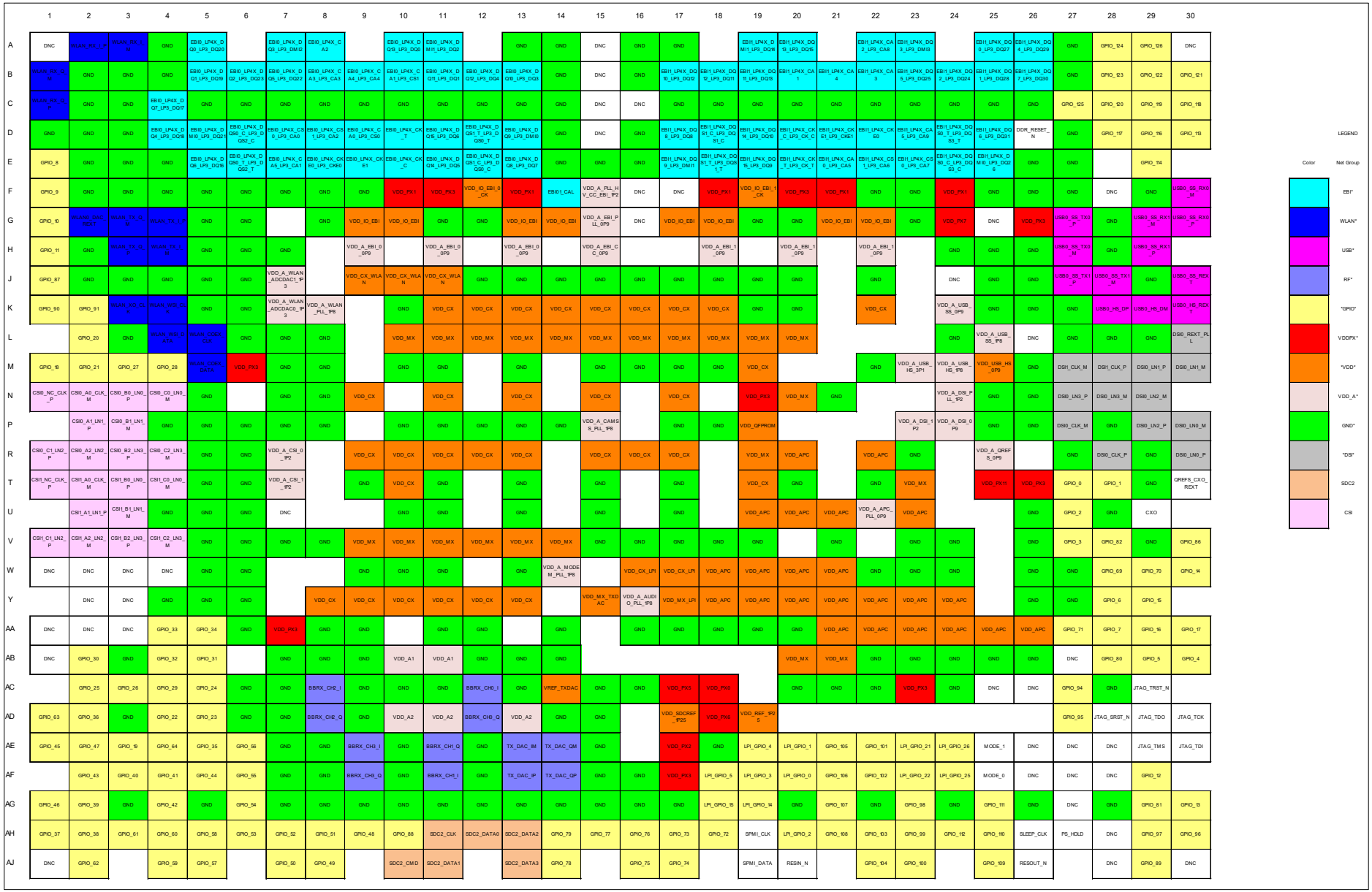


Figure 2-1 QRB2210 pin assignments

2.2.2 Pin descriptions

The pins are described in Table 2-2 through Table 2-4.

Table 2-2 Pin descriptions – general pins

Pad number	Pin name	Pad name or alternate function	Pad characteristics		Functional description
			Pad voltage	Pad type	
N2	CSI0_A0_CLK_M	–	CSI	AI, AO	MIPI CSI 0 (DPHY), differential clock – minus MIPI CSI 0 (CPHY), trio lane 0 – A
P2	CSI0_A1_LN1_P	–	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 1 – plus MIPI CSI 0 (CPHY), trio lane 1 – A
R2	CSI0_A2_LN2_M	–	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 2 – minus MIPI CSI 0 (CPHY), trio lane 2 – A
N3	CSI0_B0_LN0_P	–	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 0 – plus MIPI CSI 0 (CPHY), trio lane 0 – B
P3	CSI0_B1_LN1_M	–	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 1 – minus MIPI CSI 0 (CPHY), trio lane 1 – B
R3	CSI0_B2_LN3_P	–	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 3 – plus MIPI CSI 0 (CPHY), trio lane 2 – B
N4	CSI0_C0_LN0_M	–	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 0 – minus MIPI CSI 0 (CPHY), trio lane 0 – C
R1	CSI0_C1_LN2_P	–	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 2 – plus MIPI CSI 0 (CPHY), trio lane 1 – C
R4	CSI0_C2_LN3_M	–	CSI	AI, AO	MIPI CSI 0 (DPHY), differential lane 3 – minus MIPI CSI 0 (CPHY), trio lane 2 – C
N1	CSI0_NC_CLK_P	–	CSI	AI, AO	MIPI CSI 0 (DPHY), differential clock – plus MIPI CSI 0 (CPHY), no connect
T2	CSI1_A0_CLK_M	–	CSI	AI, AO	MIPI CSI 1 (DPHY), differential clock – minus MIPI CSI 1 (CPHY), trio lane 0 – A
U2	CSI1_A1_LN1_P	–	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 1 – plus MIPI CSI 1 (CPHY), trio lane 1 – A

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pin name	Pad name or alternate function	Pad characteristics		Functional description
			Pad voltage	Pad type	
V2	CSI1_A2_LN2_M	–	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 2 – minus MIPI CSI 1 (CPHY), trio lane 2 – A
T3	CSI1_B0_LN0_P	–	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 0 – plus MIPI CSI 1 (CPHY), trio lane 0 – B
U3	CSI1_B1_LN1_M	–	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 1 – minus MIPI CSI 1 (CPHY), trio lane 1 – B
V3	CSI1_B2_LN3_P	–	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 3 – plus MIPI CSI 1 (CPHY), trio lane 2 – B
T4	CSI1_C0_LN0_M	–	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 0 – minus MIPI CSI 1 (CPHY), trio lane 0 – C
V1	CSI1_C1_LN2_P	–	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 2 – plus MIPI CSI 1 (CPHY), trio lane 1 – C
V4	CSI1_C2_LN3_M	–	CSI	AI, AO	MIPI CSI 1 (DPHY), differential lane 3 – minus MIPI CSI 1 (CPHY), trio lane 2 – C
T1	CSI1_NC_CLK_P	–	CSI	AI, AO	MIPI CSI 1 (DPHY), differential clock – plus MIPI CSI 1 (CPHY), no connect
U29	CXO	–	PX_11	DI	Core crystal oscillator (digital 19.2 MHz system clock)
D26	DDR_RESET_N	–	EBI	DO	LPDDRx reset (shared by EBIs)
P27	DSI0_CLK_M	–	DSI	AI, AO	MIPI DSI0 (DPHY), differential clock – minus
R28	DSI0_CLK_P	–	DSI	AI, AO	MIPI DSI0 (DPHY), differential clock – plus
P30	DSI0_LN0_M	–	DSI	AI, AO	MIPI DSI0 (DPHY), differential lane 0 – minus
R30	DSI0_LN0_P	–	DSI	AI, AO	MIPI DSI0 (DPHY), differential lane 0 – plus
M30	DSI0_LN1_M	–	DSI	AI, AO	MIPI DSI0 (DPHY), differential lane 1 – minus
M29	DSI0_LN1_P	–	DSI	AI, AO	MIPI DSI0 (DPHY), differential lane 1 – plus
N29	DSI0_LN2_M	–	DSI	AI, AO	MIPI DSI0 (DPHY), differential lane 2 – minus
P29	DSI0_LN2_P	–	DSI	AI, AO	MIPI DSI0 (DPHY), differential lane 2 – plus
N28	DSI0_LN3_M	–	DSI	AI, AO	MIPI DSI0 (DPHY), differential lane 3 – minus

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pin name	Pad name or alternate function	Pad characteristics		Functional description
			Pad voltage	Pad type	
N27	DSI0_LN3_P	–	DSI	AI, AO	MIPI DSI0 (DPHY), differential lane 3 – plus
L30	DSI0_REXT_PLL	–	DSI	AI, AO	DSI external resistor
M27	DSI1_CLK_M	–	DSI	AI, AO	MIPI DSI1 (DPHY), differential clock – minus
M28	DSI1_CLK_P	–	DSI	AI, AO	MIPI DSI1 (DPHY), differential clock – plus
F14	EBI01_CAL	–	EBI	AI	EBI01 calibration resistor
D9	EBI0_LP4X_CA0_LP3_CS0	–	EBI	DO	EBI0 LPDDR4X command/address 0 LP3 chips select 0
B10	EBI0_LP4X_CA1_LP3_CS1	–	EBI	DO	EBI0 LPDDR4X command/address 1 LP3 chips select 1
A8	EBI0_LP4X_CA2	–	EBI	DO	EBI0 LPDDR4X command/address 2
B8	EBI0_LP4X_CA3_LP3_CA3	–	EBI	DO	EBI0 LPDDR4X command/address 3 LP3 command/address 3
B9	EBI0_LP4X_CA4_LP3_CA4	–	EBI	DO	EBI0 LPDDR4X command/address 4 LP3 command/address 4
E7	EBI0_LP4X_CA5_LP3_CA1	–	EBI	DO	EBI0 LPDDR4X command/address 5 LP3 command/address 1
E8	EBI0_LP4X_CKE0_LP3_CKE0	–	EBI	DO	EBI0 LPDDR4X clock enable 0 LP3 clock enable 0
E9	EBI0_LP4X_CKE1	–	EBI	DO	EBI0 LPDDR4X clock enable 1
E10	EBI0_LP4X_CK_C	–	EBI	DO	EBI0 LPDDR4X differential clock – minus
D10	EBI0_LP4X_CK_T	–	EBI	DO	EBI0 LPDDR4X differential clock – plus
D7	EBI0_LP4X_CS0_LP3_CA0	–	EBI	DO	EBI0 LPDDR4X chip select 0 LP3 command/address 0
D8	EBI0_LP4X_CS1_LP3_CA2	–	EBI	DO	EBI0 LPDDR4X chip select 1 LP3 command/address 2
D5	EBI0_LP4X_DMI0_LP3_DQ21	–	EBI	B	EBI0 LPDDR4X data mask 0 LP3 data bit 21

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pin name	Pad name or alternate function	Pad characteristics		Functional description
			Pad voltage	Pad type	
A11	EBI0_LP4X_DMI1_LP3_DQ2	–	EBI	B	EBI0 LPDDR4X data mask 1 LP3 data bit 2
A5	EBI0_LP4X_DQ0_LP3_DQ20	–	EBI	B	EBI0 LPDDR4X data bit 0 LP3 data bit 20
B13	EBI0_LP4X_DQ10_LP3_DQ3	–	EBI	B	EBI0 LPDDR4X data bit 10 LP3 data bit 3
B11	EBI0_LP4X_DQ11_LP3_DQ1	–	EBI	B	EBI0 LPDDR4X data bit 11 LP3 data bit 1
B12	EBI0_LP4X_DQ12_LP3_DQ4	–	EBI	B	EBI0 LPDDR4X data bit 12 LP3 data bit 4
A10	EBI0_LP4X_DQ13_LP3_DQ0	–	EBI	B	EBI0 LPDDR4X data bit 13 LP3 data bit 0
E11	EBI0_LP4X_DQ14_LP3_DQ5	–	EBI	B	EBI0 LPDDR4X data bit 14 LP3 data bit 5
D11	EBI0_LP4X_DQ15_LP3_DQ6	–	EBI	B	EBI0 LPDDR4X data bit 15 LP3 data bit 6
B5	EBI0_LP4X_DQ1_LP3_DQ19	–	EBI	B	EBI0 LPDDR4X data bit 1 LP3 data bit 19
B6	EBI0_LP4X_DQ2_LP3_DQ23	–	EBI	B	EBI0 LPDDR4X data bit 2 LP3 data bit 23
A7	EBI0_LP4X_DQ3_LP3_DMI2	–	EBI	B	EBI0 LPDDR4X data bit 3 LP3 data mask 2
D4	EBI0_LP4X_DQ4_LP3_DQ18	–	EBI	B	EBI0 LPDDR4X data bit 4 LP3 data bit 18
B7	EBI0_LP4X_DQ5_LP3_DQ22	–	EBI	B	EBI0 LPDDR4X data bit 5 LP3 data bit 22
E5	EBI0_LP4X_DQ6_LP3_DQ16	–	EBI	B	EBI0 LPDDR4X data bit 6 LP3 data bit 16

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pin name	Pad name or alternate function	Pad characteristics		Functional description
			Pad voltage	Pad type	
C4	EBI0_LP4X_DQ7_LP3_DQ17	–	EBI	B	EBI0 LPDDR4X data bit 7 LP3 data bit 17
E13	EBI0_LP4X_DQ8_LP3_DQ7	–	EBI	B	EBI0 LPDDR4X data bit 8 LP3 data bit 7
D13	EBI0_LP4X_DQ9_LP3_DMI0	–	EBI	B	EBI0 LPDDR4X data bit 9 LP3 data mask 0
D6	EBI0_LP4X_DQS0_C_LP3_DQS2_C	–	EBI	B	EBI0 LPDDR4X differential data strobe 0 – minus LP3 differential data strobe 2 – minus
E6	EBI0_LP4X_DQS0_T_LP3_DQS2_T	–	EBI	B	EBI0 LPDDR4X differential data strobe 0 – plus LP3 differential data strobe 2 – plus
E12	EBI0_LP4X_DQS1_C_LP3_DQS0_C	–	EBI	B	EBI0 LPDDR4X differential data strobe 1 – minus LP3 differential data strobe 0 – minus
D12	EBI0_LP4X_DQS1_T_LP3_DQS0_T	–	EBI	B	EBI0 LPDDR4X differential data strobe 1 – plus LP3 differential data strobe 0 – plus
E21	EBI1_LP4X_CA0_LP3_CA5	–	EBI	DO	EBI1 LPDDR4X command/address 0 LP3 command/address 5
B20	EBI1_LP4X_CA1	–	EBI	DO	EBI1 LPDDR4X command/address 1
A22	EBI1_LP4X_CA2_LP3_CA8	–	EBI	DO	EBI1 LPDDR4X command/address 2 LP3 command/address 8
B22	EBI1_LP4X_CA3	–	EBI	DO	EBI1 LPDDR4X command/address 3
B21	EBI1_LP4X_CA4	–	EBI	DO	EBI1 LPDDR4X command/address 4
D23	EBI1_LP4X_CA5_LP3_CA9	–	EBI	DO	EBI1 LPDDR4X command/address 5 LP3 command/address 9
D22	EBI1_LP4X_CKE0	–	EBI	DO	EBI1 LPDDR4X clock enable 0
D21	EBI1_LP4X_CKE1_LP3_CKE1	–	EBI	DO	EBI1 LPDDR4X clock enable 1 LP3 clock enable 1
D20	EBI1_LP4X_CK_C_LP3_CK_C	–	EBI	DO	EBI1 LPDDR4X differential clock – minus LP3 differential clock – minus

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pin name	Pad name or alternate function	Pad characteristics		Functional description
			Pad voltage	Pad type	
E20	EBI1_LP4X_CK_T_LP3_CK_T	–	EBI	DO	EBI1 LPDDR4X differential clock – plus LP3 differential clock – plus
E23	EBI1_LP4X_CS0_LP3_CA7	–	EBI	DO	EBI1 LPDDR4X chip select 0 LP3 command/address 7
E22	EBI1_LP4X_CS1_LP3_CA6	–	EBI	DO	EBI1 LPDDR4X chip select 1 LP3 command/address 6
E25	EBI1_LP4X_DMI0_LP3_DQ26	–	EBI	B	EBI1 LPDDR4X data mask 0 LP3 data bit 26
A19	EBI1_LP4X_DMI1_LP3_DQ14	–	EBI	B	EBI1 LPDDR4X data mask 1 LP3 data bit 14
A25	EBI1_LP4X_DQ0_LP3_DQ27	–	EBI	B	EBI1 LPDDR4X data bit 0 LP3 data bit 27
B17	EBI1_LP4X_DQ10_LP3_DQ12	–	EBI	B	EBI1 LPDDR4X data bit 10 LP3 data bit 12
B19	EBI1_LP4X_DQ11_LP3_DQ13	–	EBI	B	EBI1 LPDDR4X data bit 11 LP3 data bit 13
B18	EBI1_LP4X_DQ12_LP3_DQ11	–	EBI	B	EBI1 LPDDR4X data bit 12 LP3 data bit 11
A20	EBI1_LP4X_DQ13_LP3_DQ15	–	EBI	B	EBI1 LPDDR4X data bit 13 LP3 data bit 15
D19	EBI1_LP4X_DQ14_LP3_DQ10	–	EBI	B	EBI1 LPDDR4X data bit 14 LP3 data bit 10
E19	EBI1_LP4X_DQ15_LP3_DQ9	–	EBI	B	EBI1 LPDDR4X data bit 15 LP3 data bit 9
B25	EBI1_LP4X_DQ1_LP3_DQ28	–	EBI	B	EBI1 LPDDR4X data bit 1 LP3 data bit 28
B24	EBI1_LP4X_DQ2_LP3_DQ24	–	EBI	B	EBI1 LPDDR4X data bit 2 LP3 data bit 24

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pin name	Pad name or alternate function	Pad characteristics		Functional description
			Pad voltage	Pad type	
A23	EBI1_LP4X_DQ3_LP3_DMI3	–	EBI	B	EBI1 LPDDR4X data bit 3 LP3 data mask 3
A26	EBI1_LP4X_DQ4_LP3_DQ29	–	EBI	B	EBI1 LPDDR4X data bit 4 LP3 data bit 29
B23	EBI1_LP4X_DQ5_LP3_DQ25	–	EBI	B	EBI1 LPDDR4X data bit 5 LP3 data bit 25
D25	EBI1_LP4X_DQ6_LP3_DQ31	–	EBI	B	EBI1 LPDDR4X data bit 6 LP3 data bit 31
B26	EBI1_LP4X_DQ7_LP3_DQ30	–	EBI	B	EBI1 LPDDR4X data bit 7 LP3 data bit 30
D17	EBI1_LP4X_DQ8_LP3_DQ8	–	EBI	B	EBI1 LPDDR4X data bit 8 LP3 data bit 8
E17	EBI1_LP4X_DQ9_LP3_DMI1	–	EBI	B	EBI1 LPDDR4X data bit 9 LP3 data mask 1
E24	EBI1_LP4X_DQS0_C_LP3_DQS3_C	–	EBI	B	EBI1 LPDDR4X differential data strobe 0 – minus LP3 differential data strobe 3 – minus
D24	EBI1_LP4X_DQS0_T_LP3_DQS3_T	–	EBI	B	EBI1 LPDDR4X differential data strobe 0 – plus LP3 differential data strobe 3 – plus
D18	EBI1_LP4X_DQS1_C_LP3_DQS1_C	–	EBI	B	EBI1 LPDDR4X differential data strobe 1 – minus LP3 differential data strobe 1 – minus
E18	EBI1_LP4X_DQS1_T_LP3_DQS1_T	–	EBI	B	EBI1 LPDDR4X differential data strobe 1 – plus LP3 differential data strobe 1 – plus
AF25	MODE_0	–	PX_3	DI	Mode control bit 0 – unconnected for native mode
AE25	MODE_1	–	PX_3	DI	Mode control bit 1 – unconnected for native mode
AH19	SPMI_CLK	–	PX_0	B	Slave and PBUS interface for PMICs – clock
AJ19	SPMI_DATA	–	PX_0	B	Slave and PBUS interface for PMICs – data
AH27	PS_HOLD	–	PX_3	DO	Power–supply hold signal to PMIC
T30	QREFS_CXO_REXT	–	–	AI, AO	External resistor for on-die clocking

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pin name	Pad name or alternate function	Pad characteristics		Functional description
			Pad voltage	Pad type	
AJ20	RESIN_N	–	PX_3	DI	Reset input
AJ26	RESOUT_N	–	PX_3	DO	Reset output
AH11	SDC2_CLK	–	PX_2	BH-NP: pdpukp	Secure digital controller 2 clock
AJ10	SDC2_CMD	–	PX_2	BH-PD: nppukp	Secure digital controller 2 command
AH12	SDC2_DATA0	–	PX_2	BH-PD: nppukp	Secure digital controller 2 data bit 0
AJ11	SDC2_DATA1	–	PX_2	BH-PD: nppukp	Secure digital controller 2 data bit 1
AH13	SDC2_DATA2	–	PX_2	BH-PD: nppukp	Secure digital controller 2 data bit 2
AJ13	SDC2_DATA3	–	PX_2	BH-PD: nppukp	Secure digital controller 2 data bit 3
AH26	SLEEP_CLK	–	PX_3	DI	Sleep clock
AD28	JTAG_SRST_N	–	PX_3	DI-PU	JTAG reset for debug
AD30	JTAG_TCK	–	PX_3	DI-PU	JTAG clock input
AE30	JTAG_TDI	–	PX_3	DI-PU: nppdkp	JTAG data input
AD29	JTAG_TDO	–	PX_3	DO-Z	JTAG data output
AE29	JTAG_TMS	–	PX_3	DI-PU: nppdkp	JTAG mode select input
AC29	JTAG_TRST_N	–	PX_3	DI-PD: nppukp	JTAG reset
AC12	BBRX_CH0_I	–	–	AI	Baseband receiver input, channel 0, inphase
AF11	BBRX_CH1_I	–	–	AI	Baseband receiver input, channel 1, in-phase
AC8	BBRX_CH2_I	–	–	AI	Baseband receiver input, channel 2, in-phase
AE9	BBRX_CH3_I	–	–	AI	Baseband receiver input, channel 3, in-phase
AD12	BBRX_CH0_Q	–	–	AI	Baseband receiver input, channel 0, quadrature
AE11	BBRX_CH1_Q	–	–	AI	Baseband receiver input, channel 1, quadrature
AD8	BBRX_CH2_Q	–	–	AI	Baseband receiver input, channel 2, quadrature
AF9	BBRX_CH3_Q	–	–	AI	Baseband receiver input, channel 3, quadrature
AE13	TX_DAC_IM	–	–	AO	TXDAC in-phase – minus
AF13	TX_DAC_IP	–	–	AO	TXDAC in-phase – plus
AE14	TX_DAC_QM	–	–	AO	TXDAC quadrature – minus
AF14	TX_DAC_QP	–	–	AO	TXDAC quadrature – plus

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pin name	Pad name or alternate function	Pad characteristics		Functional description
			Pad voltage	Pad type	
K29	USB0_HS_DM	–	–	AI, AO	USB 0 high-speed data – minus
K28	USB0_HS_DP	–	–	AI, AO	USB 0 high-speed data – plus
K30	USB0_HS_REXT	–	–	AI	USB 0 high-speed external resistor
J30	USB0_SS_REXT	–	–	AI	USB 0 super-speed external resistor
F30	USB0_SS_RX0_M	–	–	AI	USB 0 super-speed receive 0 – minus
G30	USB0_SS_RX0_P	–	–	AI	USB 0 super-speed receive 0 – plus
G29	USB0_SS_RX1_M	–	–	AI	USB 0 super-speed receive 1 – minus
H29	USB0_SS_RX1_P	–	–	AI	USB 0 super-speed receive 1 – plus
H27	USB0_SS_TX0_M	–	–	AO	USB 0 super-speed transmit 0 – minus
G27	USB0_SS_TX0_P	–	–	AO	USB 0 super-speed transmit 0 – plus
J28	USB0_SS_TX1_M	–	–	AO	USB 0 super-speed transmit 1 – minus
J27	USB0_SS_TX1_P	–	–	AO	USB 0 super-speed transmit 1 – plus
AC14	VREF_TXDAC	–	–	AI, AO	Transmitter DAC voltage reference
G2	WLAN0_DAC_REXT	–	–	AI, AO	WLAN chain 0 external resistor
K4	WLAN_WSI_CLK	–	–	DO	WLAN baseband clock
L4	WLAN_WSI_DATA	–	–	B	WLAN baseband data
L5	WLAN_COEX_CLK	–	–	DO	WLAN coexistence module command clock
M5	WLAN_COEX_DATA	–	–	B	WLAN coexistence module command data
A3	WLAN_RX_I_M	–	–	AI	WLAN receive in-phase – minus
A2	WLAN_RX_I_P	–	–	AI	WLAN receive in-phase – plus
B1	WLAN_RX_Q_M	–	–	AI	WLAN receive quadrature – minus
C1	WLAN_RX_Q_P	–	–	AI	WLAN receive quadrature – plus
H4	WLAN_TX_I_M	–	–	AO	WLAN transmits in-phase – minus
G4	WLAN_TX_I_P	–	–	AO	WLAN transmits in-phase – plus
G3	WLAN_TX_Q_M	–	–	AO	WLAN transmit quadrature – minus

Table 2-2 Pin descriptions – general pins (cont.)

Pad number	Pin name	Pad name or alternate function	Pad characteristics		Functional description
			Pad voltage	Pad type	
H3	WLAN_TX_Q_P	–	–	AO	WLAN transmit quadrature – plus
K3	WLAN_XO_CLK	–	–	AI	WLAN reference clock

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. See Table 2-3 for a list of all supported functions for each GPIO.

NOTE Handset designers must examine each GPIOs external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input vs. output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, Qualcomm Technologies, Inc. (QTI) provides an Excel spreadsheet that lists all QRB2210 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE Click *QRB2210 Pin Assignment and GPIO Configuration Spreadsheet (80-30843-1A)* to download the document from the Qualcomm website.

Table 2-3 Pin descriptions – general-purpose input/output ports

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
T27	GPIO_0	Y		PX_3	B-PD:nppukp	Configurable I/O
			SPI_MISO		DI	QUP 0 SE0, lane 0: SPI_MISO
			UART_CTS		DI	QUP 0 SE0, lane 0: UART_CTS
			I2C_SDA		B	QUP 0 SE0, lane 0: I2C_SDA
			I3C_SDA		B	QUP 0 SE0, lane 0: I3C_SDA
			QDSS_GPIO_TRACEDATA_LOCB[8]		DO	QDSS trace data bit 8 B
T28	GPIO_1	N		PX_3	B-PD:nppukp	Configurable I/O
			SPI_MOSI		DO	QUP 0 SE0, lane 1: SPI_MOSI

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
			UART_RFR		DO	QUP 0 SE0, lane 1: UART_RFR
			I2C_SCL		DO	QUP 0 SE0, lane 1: I2C_SCL
			I3C_SCL		DO	QUP 0 SE0, lane 1: I3C_SCL
			QDSS_GPIO_TRACEDATA_LOCB[9]		DO	QDSS trace data bit 9 B
U27	GPIO_2	N		PX_3	B-PD:nppukp	Configurable I/O
			SPI_SCLK		DO	QUP 0 SE0, lane 2: SPI_SCLK
			UART_TX		DO	QUP 0 SE0, lane 2: UART_TX
			QDSS_GPIO_TRACEDATA_LOCB[10]		DO	QDSS trace data bit 10 B
V27	GPIO_3	Y		PX_3	B-PD:nppukp	Configurable I/O
			SPI_CS_N_0		DO	QUP 0 SE0, lane 3:SPI_CS_N
			UART_RX		DI	QUP 0 SE0, lane 3: UART_RX
			QDSS_GPIO_TRACEDATA_LOCB[11]		DO	QDSS trace data bit 11 B
AB30	GPIO_4	Y		PX_3	B-PD:nppukp	Configurable I/O
			SPI_MISO		DI	QUP 0 SE1, lane 0: SPI_MISO
			UART_CTS		DI	QUP 0 SE1, lane 0: UART_CTS
			I2C_SDA		B	QUP 0 SE1, lane 0: I2C_SDA
AB29	GPIO_5	N		PX_3	B-PD:nppukp	Configurable I/O
			SPI_MOSI		DO	QUP 0 SE1, lane 1: SPI_MOSI
			UART_RFR		DO	QUP 0 SE1, lane 1: UART_RFR
			I2C_SCL		DO	QUP 0 SE1, lane 1: I2C_SCL
Y28	GPIO_6	Y		PX_3	B-PD:nppukp	Configurable I/O
			SPI_MISO		DI	QUP 0 SE2, lane 0: SPI_MISO
			UART_CTS		DI	QUP 0 SE2, lane 0: UART_CTS
			I2C_SDA		B	QUP 0 SE2, lane 0: I2C_SDA
AA28	GPIO_7	N		PX_3	B-PD:nppukp	Configurable I/O
			SPI_MOSI		DO	QUP 0 SE2, lane 1:SPI_MOSI
			UART_RFR		DO	QUP 0 SE2, lane 1:UART_RFR
			I2C_SCL		DO	QUP 0 SE2, lane 1:I2C_SCL

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
E1	GPIO_8	Y		PX_3	B-PD:nppukp	Configurable I/O
			SPI_MISO		DI	QUP 0 SE3, lane 0: SPI_MISO
			UART_CTS		DI	QUP 0 SE3, lane 0: UART_CTS
			I2C_SDA		B	QUP 0 SE3, lane 0: I2C_SDA
			QDSS_GPIO_TRACECLK_LOCA		DO	QDSS trace clock A
F1	GPIO_9	N		PX_3	B-PD:nppukp	Configurable I/O
			SPI_MOSI		DO	QUP 0 SE3, lane 1: SPI_MOSI
			UART_RFR		DO	QUP 0 SE3, lane1:UART_RFR
			I2C_SCL		DO	QUP 0 SE3, lane1: I2C_SCL
			QDSS_GPIO_TRACECTL_LOCA		DO	QDSS trace control A
G1	GPIO_10	N		PX_3	B-PD:nppukp	Configurable I/O
			SPI_SCLK		DO	QUP 0 SE3, lane 2: SPI_SCLK
			UART_TX		DO	QUP 0 SE3, lane 2: UART_TX
			QDSS_GPIO_TRACEDATA_LOCA[0]		DO	QDSS trace data bit 0 A
H1	GPIO_11	Y		PX_3	B-PD:nppukp	Configurable I/O
			SPI_CS_N		DO	QUP 0 SE3, lane 3: SPI_CS_N
			UART_RX		DI	QUP 0 SE3, lane 3: UART_RX
			QDSS_GPIO_TRACEDATA_LOCA[1]		DO	QDSS trace data bit 1 A
AF29	GPIO_12	N		PX_3	B-PD:nppukp	Configurable I/O
			UART_TX		DO	QUP 0 SE4, lane 2: UART_TX
			SPI_SCLK		DO	QUP 0 SE4, lane 2: SPI_SCLK
AG30	GPIO_13	Y		PX_3	B-PD:nppukp	Configurable I/O
			UART_RX		DI	QUP 0 SE4, lane 3: UART_RX
			SPI_CS_N		DO	QUP 0 SE4, lane 3: SPI_CS_N
W30	GPIO_14	Y		PX_3	B-PD:nppukp	Configurable I/O
			SPI_MISO		DI	QUP 0 SE5, lane 0: SPI_MISO
			UART_CTS		DI	QUP 0 SE5, lane 0: UART_CTS
			I2C_SDA		B	QUP 0 SE5, lane 0: I2C_SDA
			QDSS_GPIO_TRACEDATA_LOCB[4]		DO	QDSS trace data bit 4B

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
Y29	GPIO_15	N		PX_3	B-PD:nppukp	Configurable I/O
			SPI_MOSI		DO	QUP 0 SE5, lane 1: SPI_MOSI
			UART_RFR		DO	QUP 0 SE5, lane 1: UART_RFR
			I2C_SCL		DO	QUP 0 SE5, lane1: I2C_SCL
			QDSS_GPIO_TRACEDATA_LOCB[5]		DO	QDSS trace data bit 5 B
AA29	GPIO_16	N		PX_3	B-PD:nppukp	Configurable I/O
			UART_TX		DO	QUP 0 SE5, lane 2: UART_TX
			SPI_SCLK		DO	QUP 0 SE5, lane 2 :SPI_SCLK
			QDSS_GPIO_TRACEDATA_LOCB[6]		DO	QDSS trace data bit 6 B
AA30	GPIO_17	Y		PX_3	B-PD:nppukp	Configurable I/O
			UART_RX		DI	QUP 0 SE5, lane 3: UART_RX
			SPI_CS_N		DO	QUP 0 SE5, lane 3 :SPI_CS_N
			QDSS_GPIO_TRACEDATA_LOCB[7]		DO	QDSS trace data bit 7 B
M1	GPIO_18	Y		PX_3	B-PD:nppukp	Configurable I/O
			QDSS_GPIO_TRACEDATA_LOCA[2]		DO	QDSS trace data bit 2 A
			PWM[0]		DO	PWM output 0
AE3	GPIO_19	Y		PX_3	B-PD:nppukp	Configurable I/O
			QDSS_GPIO_TRACEDATA_LOCA[3]		DO	QDSS trace data bit 3 A
L2	GPIO_20	N		PX_3	B-PD:nppukp	Configurable I/O
			CAM_MCLK0		DO	Camera master clock 0
			QDSS_GPIO_TRACEDATA_LOCA[4]		DO	QDSS trace data bit 4 A
M2	GPIO_21	N		PX_3	B-PD:nppukp	Configurable I/O
			CAM_MCLK1		DO	Camera master clock 1
			QDSS_GPIO_TRACEDATA_LOCA[5]		DO	QDSS trace data bit 5 A
AD4	GPIO_22	N		PX_3	B-PD:nppukp	Configurable I/O
			CCI_I2C_SDA0		B	Dedicated camera control interface I^2C 0 serial data
			QDSS_GPIO_TRACEDATA_LOCA[6]		DO	QDSS trace data bit 6 A

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
AD5	GPIO_23	N		PX_3	B-PD:nppukp	Configurable I/O
			CCI_I2C_SCL0		DO	Dedicated camera control interface I^2C 0 clock
			QDSS_GPIO_TRACEDATA_LOCA[7]		DO	QDSS trace data bit 7 A
AC5	GPIO_24	Y		PX_3	B-PD:nppukp	
			CCI_TIMER1		DO	Camera control interface timer 1
			GCC_GP1_CLK_MIRA		DO	Global general–purpose clock 1
			QDSS_GPIO_TRACEDATA_LOCA[8]		DO	QDSS trace data bit 8 A
AC2	GPIO_25	Y		PX_3	B-PD:nppukp	Configurable I/O
			CCI_ASYNC_IN0		DI	Camera control interface async 0
			CCI_TIMER0		DO	Camera control interface timer 0
			QDSS_GPIO_TRACEDATA_LOCA[9]		DO	QDSS trace data bit 9 A
AC3	GPIO_26	N		PX_3	B-PD:nppukp	Configurable I/O
			QDSS_GPIO_TRACEDATA_LOCA[10]		DO	QDSS trace data bit 10 A
M3	GPIO_27	Y		PX_3	B-PD:nppukp	Configurable I/O
			CAM_MCLK2		DO	Camera master clock 2
			QDSS_CTI_TRIG0_IN_MIRB		DI	QDSS trigger input 0 B
M4	GPIO_28	Y		PX_3	B-PD:nppukp	Configurable I/O
			CAM_MCLK3		DO	Camera master clock 3
			CCI_TIMER2		DO	Camera control interface timer 2
			QDSS_CTI_TRIG0_OUT_MIRB		DO	QDSS trigger output 0 B
			PWM[1]		DO	PWM output 1
AC4	GPIO_29	N		PX_3	B-PD:nppukp	Configurable I/O
			CCI_I2C_SDA1		B	Dedicated camera control interface I^2C 1 serial data
AB2	GPIO_30	N		PX_3	B-PD:nppukp	Configurable I/O
			CCI_I2C_SCL1		DO	Dedicated camera control interface I^2C 1 clock
AB5	GPIO_31	Y		PX_3	B-PD:nppukp	Configurable I/O
			GP_PDM_MIRB[0]		DO	General-purpose PDM_Mirror_B 0

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
AB4	GPIO_32	Y		PX_3	B-PD:nppukp	Configurable I/O
			CCI_TIMER3		DO	Camera control interface timer 3
			GP_PDM_MIRB[1]		DO	General-purpose PDM_Mirror_B 1
AA4	GPIO_33	Y		PX_3	B-PD:nppukp	Configurable I/O
			GP_PDM_MIRB[2]		DO	General-purpose PDM_Mirror_B 2
AA5	GPIO_34	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AE5	GPIO_35	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AD2	GPIO_36	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AH1	GPIO_37	N		PX_3	B-PD:nppukp	Configurable I/O
AH2	GPIO_38	N		PX_3	B-PD:nppukp	Configurable I/O
AG2	GPIO_39	Y		PX_3	B-PD:nppukp	Configurable I/O
AF3	GPIO_40	N		PX_3	B-PD:nppukp	Configurable I/O
AF4	GPIO_41	N		PX_3	B-PD:nppukp	Configurable I/O
AG4	GPIO_42	N		PX_3	B-PD:nppukp	Configurable I/O
			NAV_GPIO_1_MIRA		B	Generic I/O
AF2	GPIO_43	N		PX_3	B-PD:nppukp	Configurable I/O
			BOOT_CONFIG[8]		DI	Boot configuration control bit 8
AF5	GPIO_44	N		PX_3	B-PD:nppukp	Configurable I/O
			BOOT_CONFIG[9]		DI	Boot configuration control bit 9
AE1	GPIO_45	N		PX_3	B-PD:nppukp	Configurable I/O
			BOOT_CONFIG[10]		DI	Boot configuration control bit 10
AG1	GPIO_46	Y		PX_3	B-PD:nppukp	Configurable I/O
			BOOT_CONFIG[11]		DI	Boot configuration control bit 11
AE2	GPIO_47	N		PX_3	B-PD:nppukp	Configurable I/O
			NAV_GPIO_0_MIRA		B	Generic I/O
			QDSS_GPIO_TRACEDATA_LOCA[14]		DO	QDSS trace data bit 14 A

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
AH9	GPIO_48	N		PX_3	B-PD:nppukp	Configurable I/O
			QDSS_GPIO_TRACEDATA_LOCA[15]		DO	QDSS trace data bit 15 A
			BOOT_CONFIG[0]		DI	Boot configuration control bit 0
AJ8	GPIO_49	N		PX_3	B-PD:nppukp	Configurable I/O
			PA_INDICATOR_OR		DO	PA transmit indicator
AJ7	GPIO_50	N		PX_3	B-PD:nppukp	Configurable I/O
			BOOT_CONFIG[1]		DI	Boot configuration control bit 1
AH8	GPIO_51	N		PX_3	B-PD:nppukp	Configurable I/O
			BOOT_CONFIG[2]		DI	Boot configuration control bit 2
			PWM[2]		DO	PWM output 2
AH7	GPIO_52	N		PX_3	B-PD:nppukp	Configurable I/O
			NAV_GPIO_2_MIRA		B	Generic I/O
AH6	GPIO_53	N		PX_3	B-PD:nppukp	Configurable I/O
			BOOT_CONFIG[3]		DI	Boot configuration control bit 3
AG6	GPIO_54	N	–	PX_3	B-PD:nppukp	Configurable I/O
AF6	GPIO_55	N		PX_3	B-PD:nppukp	Configurable I/O
			BOOT_CONFIG[4]		DI	Boot configuration control bit 4
AE6	GPIO_56	N	–	PX_3	B-PD:nppukp	Configurable I/O
AJ5	GPIO_57	N		PX_3	B-PD:nppukp	Configurable I/O
			BOOT_CONFIG[5]		DI	Boot configuration control bit 5
AH5	GPIO_58	N		PX_3	B-PD:nppukp	Configurable I/O
AJ4	GPIO_59	N		PX_3	B-PD:nppukp	Configurable I/O
			SSBI_WGR_TX		DO	Single serial bus interface transmiter
			BOOT_CONFIG[6]		DI	Boot configuration control bit 6
AH4	GPIO_60	N		PX_3	B-PD:nppukp	Configurable I/O
			SSBI_WGR_RX		DI	Single serial bus interface receiver
AH3	GPIO_61	N		PX_3	B-PD:nppukp	Configurable I/O
			BOOT_CONFIG[7]		DI	Boot configuration control bit 7

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
AJ2	GPIO_62	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AD1	GPIO_63	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AE4	GPIO_64	Y	–	PX_3	B-PD:nppukp	Configurable I/O
W28	GPIO_69	Y		PX_3	B–PU:nppukp	Configurable I/O
			SPI_SCLK		DO	QUP 0 SE1, lane 2 :SPI_SCLK
			UART_TX		DO	QUP 0 SE1, lane 2: UART_TX
			GCC_GP2_CLK_MIRA		DO	Global general purpose clock 2 A
			QDSS_GPIO_TRACEDATA_LOCB[12]		DO	QDSS trace data bit 12 B
W29	GPIO_70	Y		PX_3	B-PD:nppukp	Configurable I/O
			SPI_CS_N		DO	QUP 0 SE1, lane 3 :SPI_CS_N
			UART_RX		DI	QUP 0 SE1, lane 3: UART_RX
			GCC_GP3_CLK_MIRA		DO	Global general purpose clock 3 A
			QDSS_GPIO_TRACEDATA_LOCB[13]		DO	QDSS trace data bit 13 B
AA27	GPIO_71	N		PX_3	B-PD:nppukp	Configurable I/O
			SPI_SCLK		DO	QUP 0 SE2, lane 2 :SPI_SCLK
			UART_TX		DO	QUP 0 SE 2, lane 2: UART_TX
AH18	GPIO_72	Y		PX_6	B-PD:nppukp	Configurable I/O
			QDSS_CTI_TRIG1_IN_MIRB		DI	QDSS trigger input 1 B
			PWM[3]		DO	PWM output 3
AH17	GPIO_73	N		PX_6	B-PD:nppukp	Configurable I/O
			QDSS_CTI_TRIG1_OUT_MIRB		DO	QDSS trigger output 1 B
AJ17	GPIO_74	N		PX_6	B-PD:nppukp	Configurable I/O
			PWM[4]		DO	PWM output 4
AJ16	GPIO_75	Y		PX_3	B-PD:nppukp	Configurable I/O
			PWM[5]		DO	PWM output 5
AH16	GPIO_76	N	–	PX_5	B-PD:nppukp	Configurable I/O
AH15	GPIO_77	N	–	PX_5	B-PD:nppukp	Configurable I/O
AJ14	GPIO_78	N	–	PX_5	B-PD:nppukp	Configurable I/O

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
AH14	GPIO_79	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AB28	GPIO_80	Y		PX_3	B-PD:nppukp	Configurable I/O
			SPI_CS_N		DO	QUP 0 SE2, lane 3 :SPI_CS_N
			UART_RX		DI	QUP 0 SE2, lane 3: UART_RX
AG29	GPIO_81	Y		PX_3	B-PD:nppukp	Configurable I/O
			MDP_VSYNC_OUT_0		DO	MDP vertical sync – output 0
			MDP_VSYNC_OUT_1		DO	MDP vertical sync – output 1
			MDP_VSYNC_P		DI	MDP vertical sync – primary
V28	GPIO_82	N		PX_3	B-PD:nppukp	Configurable I/O
			SPI_CS_N_1		DO	QUP 0 SE0, lane 4 :SPI_CS_N_1
			PWM[6]		DO	PWM output 6
V30	GPIO_86	Y		PX_3	B-PD:nppukp	Configurable I/O
			SPI_CS_N_2		DO	QUP 0 SE0, lane 5 :SPI_CS_N_2
			GCC_GP1_CLK_MIRB		DO	Global general purpose clock 1 B
J1	GPIO_87	Y		PX_3	B-PD:nppukp	Configurable I/O
			QDSS_GPIO_TRACEDATA_LOCA[11]		DO	QDSS trace data bit 11 A
AH10	GPIO_88	Y	–	PX_3	B-PD:nppukp	Configurable I/O
AJ29	GPIO_89	Y		PX_3	B-PD:nppukp	Configurable I/O
			USB_PHY_PS		DI	USB PHY port select
			PWM[7]		DO	PWM output 7
K1	GPIO_90	N		PX_3	B-PD:nppukp	Configurable I/O
			MSS_LTE_COXM_TXD		DO	UART Tx for LTE coex
			QDSS_GPIO_TRACEDATA_LOCA[12]		DO	QDSS trace data bit 12 A
K2	GPIO_91	Y		PX_3	B-PD:nppukp	Configurable I/O
			MSS_LTE_COXM_RXD		DI	UART Rx for LTE coex
			QDSS_GPIO_TRACEDATA_LOCA[13]		DO	QDSS trace data bit 13 A

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
AC27	GPIO_94	Y		PX_3	B-PD:nppukp	Configurable I/O
			GP_MN		DO	General-purpose M/N:D counter output
			QDSS_GPIO_TRACEDATA_LOCB[14]		DO	QDSS trace data bit 14 B
			FORCED_USB_BOOT_POL_SEL		DI	Forced USB boot polarity select
AD27	GPIO_95	Y		PX_3	B-PD:nppukp	Configurable I/O
			NAV_GPIO_0_MIRC		B	Generic I/O
			GP_PDM_MIRA[0]		DO	General-purpose PDM_Mirror_A 0
			QDSS_GPIO_TRACEDATA_LOCB[15]		DO	QDSS trace data bit 15 B
			FORCED_USB_BOOT		DI	Forced USB boot
AH30	GPIO_96	Y		PX_3	B-PD:nppukp	Configurable I/O
			SPI_MISO		DI	QUP 0 SE4, lane 0: SPI_MISO
			UART_CTS		DI	QUP 0 SE4, lane 0: UART_CTS
			I2C_SDA		B	QUP 0 SE4, lane 0: I2C_SDA
			NAV_GPIO_1_MIRC		B	Generic I/O
			MDP_VSYNC_E		DI	MDP vertical sync – external
			GP_PDM_MIRA[1]		DO	General-purpose PDM_Mirror_A 1
			SD_WRITE_PROTECT		DO	SD card write protect
			QDSS_CTI_TRIG0_IN_MIRA		DI	QDSS trigger input 0 A
			QDSS_CTI_TRIG1_OUT_MIRA		DO	QDSS trigger output 1 A
AH29	GPIO_97	Y		PX_3	B-PD:nppukp	Configurable I/O
			SPI_MOSI		DO	QUP 0 SE4, lane 1: SPI_MOSI
			UART_RFR		DO	QUP 0 SE4, lane 1: UART_RFR
			I2C_SCL		DO	QUP 0 SE4, lane1: I2C_SCL
			NAV_GPIO_2_MIRC		B	Generic I/O
			MDP_VSYNC_S		DI	MDP vertical sync – secondary
			GP_PDM_MIRA[2]		DO	General-purpose PDM_Mirror_A 2
			QDSS_CTI_TRIG0_OUT_MIRA		DO	QDSS trigger output 0 A
			QDSS_CTI_TRIG1_IN_MIRA		DI	QDSS trigger input 1 A

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
AG23	GPIO_98 [a]	N		PX_3	B-PD:nppukp	Configurable I/O
			LPI_GPIO_6:LPI_DMIC1_CLK		DO	LPI_Digital MIC 1 Clock
			LPI_GPIO_6:LPI_MI2S0_CLK		DO	LPI_MI2S 0 Clock
AH23	GPIO_99 [a]	Y		PX_3	B-PD:nppukp	Configurable I/O
			LPI_GPIO_7:LPI_DMIC1_DATA		DI	LPI_Digital MIC 1 data
			LPI_GPIO_7:LPI_MI2S0_WS		DO	LPI_MI2S 0 Word Select
AJ23	GPIO_100 [a]	N		PX_3	B-PD:nppukp	Configurable I/O
			LPI_GPIO_8:LPI_DMIC2_CLK		DO	LPI_Digital MIC 2 Clock
			LPI_GPIO_8:LPI_MI2S0_DATA0		B	LPI_MI2S 0 Data 0
AE22	GPIO_101 [a]	Y		PX_3	B-PD:nppukp	Configurable I/O
			LPI_GPIO_9:LPI_DMIC2_DATA		DI	LPI_Digital MIC 2 Data
			LPI_GPIO_9:LPI_MI2S0_DATA1		B	LPI_MI2S 0 Data 1
			LPI_GPIO_9:MI2S_MCLK1_B		DO	Master Clock 1 B
AF22	GPIO_102 [a]	Y		PX_3	B-PD:nppukp	Configurable I/O
			LPI_GPIO_10:LPI_MI2S1_CLK		DO	LPI_MI2S 1 Clock
			LPI_GPIO_10:LPI_DMIC4_CLK		DO	LPI_Digital MIC 4 Clock
AH22	GPIO_103 [a]	Y		PX_3	B-PD:nppukp	Configurable I/O
			LPI_GPIO_11:LPI_MI2S1_WS		DO	LPI_MI2S 1 Word Select
			LPI_GPIO_11:LPI_DMIC4_DATA		DI	LPI_Digital MIC 4 Data
AJ22	GPIO_104 [a]	Y		PX_3	B-PD:nppukp	Configurable I/O
			QDSS_GPIO_TRACEDATA_LOCB[1]		DO	QDSS trace data bit 1 B
			LPI_GPIO_12:LPI_DMIC3_CLK		DO	LPI_Digital MIC 3 Clock
			LPI_GPIO_12:LPI_MI2S1_DATA0		B	LPI_MI2S 1 Data 0
			PWM[8]		DO	PWM output 8

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
AE21	GPIO_105	Y		PX_3	B-PD:nppukp	Configurable I/O
			QDSS_GPIO_TRACECLK_LOCB		DO	QDSS trace clock B
			LPI_GPIO_13:LPI_DMIC3_DATA		DI	LPI_Digital MIC 3 Data
			LPI_GPIO_13:LPI_MI2S1_DATA1		B	LPI_MI2S 1 Data 1
			LPI_GPIO_13:MI2S_MCLK0_A		DO	MI2S Master Clock 0 A
AF21	GPIO_106 [a]	Y		PX_3	B-PD:nppukp	Configurable I/O
			NAV_GPIO_0_MIRB		B	Generic I/O
			GCC_GP3_CLK_MIRB		DO	Global general purpose clock 3 B
			QDSS_GPIO_TRACECTL_LOCB		DO	QDSS trace control B
			LPI_GPIO_16:LPI_MI2S2_DATA0		B	LPI_MI2S 2 Data 0
AG21	GPIO_107 [a]	Y		PX_3	B-PD:nppukp	Configurable I/O
			NAV_GPIO_1_MIRB		B	Generic I/O
			GCC_GP2_CLK_MIRB		DO	Global general purpose clock 2 B
			QDSS_GPIO_TRACEDATA_LOCB[0]		DO	QDSS trace data bit 0 B
			LPI_GPIO_17:LPI_MI2S2_DATA1		B	LPI_MI2S 2 Data 1
			LPI_GPIO_17:MI2S_MCLK1_C		DO	MI2S Master Clock 1_C
AH21	GPIO_108 [a]	N		PX_3	B-PD:nppukp	Configurable I/O
			NAV_GPIO_2_MIRB		B	Generic I/O
			LPI_GPIO_18:MI2S_MCLK1_A		DO	MI2S Master Clock 1_A
			LPI_GPIO_18:SWR_TX_DATA2		B	SoundWire transmit data 2
AJ25	GPIO_109 [a]	Y		PX_3	B-PD:nppukp	Configurable I/O
			QDSS_GPIO_TRACEDATA_LOCB[2]		DO	QDSS trace data bit 2 B
			LPI_GPIO_19:I2C_SDA		B	LPI_ QUP 0 SE0, lane 0: I2C_SDA
			LPI_GPIO_19:I3C_SDA		B	LPI_ QUP 0 SE0, lane 0: I3C_SDA
AH25	GPIO_110 [a]	N		PX_3	B-PD:nppukp	Configurable I/O
			QDSS_GPIO_TRACEDATA_LOCB[3]		DO	QDSS trace data bit 3 B
			LPI_GPIO_20:I2C_SCL		DO	LPI_ QUP 0 SE0, lane 1: I2C_SCL
			LPI_GPIO_20:I3C_SCL		DO	LPI_ QUP 0 SE0, lane 1: I3C_SCL

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
AG25	GPIO_111 [a]	N		PX_3	B-PD:nppukp	Configurable I/O
			LPI_GPIO_23:UART_CTS		DI	LPI_ QUP 0 SE5, lane 0 :UART_CTS
			LPI_GPIO_23:I2C_SDA		B	LPI_QUP 0 SE5, lane 0: I2C_SDA
			LPI_GPIO_23:UART_TX		DO	LPI_ QUP 0 SE5, lane 2:UART_TX
AH24	GPIO_112 [a]	Y		PX_3	B-PD:nppukp	Configurable I/O
			LPI_GPIO_24:UART_RFR		DO	LPI_QUP 0 SE5, lane 1 :UART_RFR
			LPI_GPIO_24:I2C_SCL		DO	LPI_ QUP 0 SE5, lane1: I2C_SCL
			LPI_GPIO_24:UART_RX		DI	LPI_ QUP 0 SE5, lane 3:UART_RX
D30	GPIO_113	N	–	PX_7	B-PD:nppukp	Configurable I/O
E29	GPIO_114	N	–	PX_7	B-PD:nppukp	Configurable I/O
D29	GPIO_116	N		PX_7	B-PD:nppukp	Configurable I/O
			SDC1_DATA7		B	Secure digital controller 1 data bit 7
D28	GPIO_117	N		PX_7	B-PD:nppukp	Configurable I/O
			SDC1_DATA6		B	Secure digital controller 1 data bit 6
C30	GPIO_118	N		PX_7	B-PD:nppukp	Configurable I/O
			SDC1_DATA5		B	Secure digital controller 1 data bit 5
C29	GPIO_119	N		PX_7	B-PD:nppukp	Configurable I/O
			SDC1_DATA4		B	Secure digital controller 1 data bit 4
C28	GPIO_120	Y		PX_7	B-PD:nppukp	Configurable I/O
			SDC1_DATA3		B	Secure digital controller 1 data bit 3
B30	GPIO_121	N		PX_7	B-PD:nppukp	Configurable I/O
			SDC1_DATA2		B	Secure digital controller 1 data bit 2
B29	GPIO_122	Y		PX_7	B-PD:nppukp	Configurable I/O
			SDC1_DATA1		B	Secure digital controller 1 data bit 1
B28	GPIO_123	N		PX_7	B-PD:nppukp	Configurable I/O
			SDC1_DATA0		B	Secure digital controller 1 data bit 0
A28	GPIO_124	N		PX_7	B-PD:nppukp	Configurable I/O
			SDC1_RCLK		DI	Secure digital controller 1 return clock

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
C27	GPIO_125	N		PX_7	B-PD:nppukp	Configurable I/O
			SDC1_CMD		B	Secure digital controller 1 command
A29	GPIO_126	N		PX_7	B-PD:nppukp	Configurable I/O
			SDC1_CLK		DO	Secure digital controller 1 clock
AF20	LPI_GPIO_0	N		PX_3	B-PD:nppukp	Configurable I/O
			SWR_TX_CLK		DO	SoundWire transmit clock
			LPI_MI2S3_CLK		DO	LPI_MI2S 3 clock
AE20	LPI_GPIO_1	Y		PX_3	B-PD:nppukp	Configurable I/O
			SWR_TX_DATA0		B	SoundWire transmit data 0
			LPI_MI2S3_WS		DO	LPI_MI2S 3 Word Select
AH20	LPI_GPIO_2	N		PX_3	B-PD:nppukp	Configurable I/O
			SWR_TX_DATA1		B	SoundWire transmit data 1
			LPI_MI2S3_DATA0		B	LPI_MI2S 3 Data 0
AF19	LPI_GPIO_3	N		PX_3	B-PD:nppukp	Configurable I/O
			SWR_RX_CLK		DO	SoundWire receive data 0
			LPI_MI2S3_DATA1		B	LPI_MI2S 3 Data 1
AE19	LPI_GPIO_4	Y		PX_3	B-PD:nppukp	Configurable I/O
			SWR_RX_DATA0		B	SoundWire receive data 0
			LPI_MI2S3_DATA2		B	LPI_MI2S 3 Data 2
AF18	LPI_GPIO_5	N		PX_3	B-PD:nppukp	Configurable I/O
			SWR_RX_DATA1		B	SoundWire receive data 1
			MI2S_MCLK0_B		DO	MI2S Master Clock 0 B
			LPI_MI2S 3		B	LPI_MI2S 3 Data 3
AG19	LPI_GPIO_14	N		PX_3	B-PD:nppukp	Configurable I/O
			LPI_MI2S2_CLK		DO	LPI_MI2S 2 Clock
			BTFM_SLIMBUS_CLK		DO	Bluetooth/FM SLIMbus clock

Table 2-3 Pin descriptions – general-purpose input/output ports (cont.)

Pad number	Pad name	Wake-up function	Configurable functions	Pad characteristics		Functional description
				Voltage	Type	
AG18	LPI_GPIO_15	Y		PX_3	B-PD:nppukp	Configurable I/O
			LPI_MI2S2_WS		DO	LPI_MI2S 2 Word Select
			BTFM_SLIMBUS_DATA		B	Bluetooth/FM SLIMbus data
AE23	LPI_GPIO_21	Y		PX_3	B-PD:nppukp	Configurable I/O
			SPI_MISO		DI	LPI_QUP 0 SE1, lane 0: SPI_MISO
			UART_CTS		DI	LPI_QUP 0 SE1, lane 0: UART_CTS
			I2C_SDA		B	LPI_QUP 0 SE1, lane 0: I2C_SDA
			I3C_SDA		B	LPI_QUP 0 SE1, lane 0: I3C_SDA
AF23	LPI_GPIO_22	N		PX_3	B-PD:nppukp	Configurable I/O
			SPI_MOSI		DO	LPI_QUP 0 SE1, lane 1: SPI_MOSI
			UART_RFR		DO	LPI_QUP 0 SE1, lane 1: UART_RFR
			I2C_SCL		DO	LPI_QUP 0 SE1, lane 1: I2C_SCL
			I3C_SCL		DO	LPI_QUP 0 SE1, lane 1: I3C_SDA
AF24	LPI_GPIO_25	N		PX_3	B-PD:nppukp	Configurable I/O
			SPI_SCLK		DO	LPI_QUP 0 SE1, lane 2: SPI_SCLK
			UART_TX		DO	LPI_QUP 0 SE1, lane 2: UART_TX
			UART_TX			LPI_QUP 0 SE6, lane 2: UART_TX
AE24	LPI_GPIO_26	Y		PX_3	B-PD:nppukp	Configurable I/O
			SPI_CS_N		DO	LPI_QUP 0 SE1, lane 3: SPI_CS_N
			UART_RX		DI	LPI_QUP 0 SE1, lane 3: UART_RX
			UART_RX		DI	LPI_QUP 0 SE6, lane 3: UART_RX

[a] LPI_GPIO functions are selected when EGPIO_ENABLE is low.

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins

Pad number	Pad name	Functional description
AD10, AD11, AD13	VDD_A2	Power for analog circuits – high voltage
AB10, AB11	VDD_A1	Power for analog circuits – low voltage
U22	VDD_A_APC_PLL_0P9	Power for the APC PLL circuits

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad number	Pad name	Functional description
Y16	VDD_A_AUDIO_PLL_1P8	Power for the audio PLL circuits
P15	VDD_A_CAMSS_PLL_1P8	Power for the camera PLL circuits
H15	VDD_A_EBI_CC_0P9	Power for the EBI clock circuits
R7	VDD_A_CSI_0_1P2	Power for the CSI0 1.2 V circuits
T7	VDD_A_CSI_1_1P2	Power for the CSI1 1.2 V circuits
P23	VDD_A_DSI_1P2	Power for the DSI 1.2 V circuits
P24	VDD_A_DSI_0P9	Power for the DSI 0.9 V circuits
N24	VDD_A_DSI_PLL_1P2	Power for the DSI PLL circuits
H9, H11, H13	VDD_A_EBI_0_0P9	Power for EBI0 circuits
H18, H20, H22	VDD_A_EBI_1_0P9	Power for EBI1 circuits
G15	VDD_A_EBI_PLL_0P9	Power for EBI PLL circuits
W14	VDD_A_MODEM_PLL_1P8	Power for modem PLL circuits
F15	VDD_A_PLL_HV_CC_EBI_1P2	Power for EBI PLL high-voltage circuits
R25	VDD_A_QREFS_0P9	Reference voltage for QREF 0.9 V circuits
M24	VDD_A_USB_HS_1P8	Power for the USB HS 1.8 V circuits
M23	VDD_A_USB_HS_3P1	Power for the USB HS 3.1 V circuits
K7	VDD_A_WLAN_ADCDAC0_1P3	Power for the WLAN ADC and DAC 0
J7	VDD_A_WLAN_ADCDAC1_1P3	Power for the WLAN ADC and DAC 1
K8	VDD_A_WLAN_PLL_1P8	Power for the WLAN PLL circuits
K24	VDD_A_USB_SS_0P9	Power for USB SS 0.9 V circuits
K11, K12, K13, K14, K15, K16, K17, K18, K22, M19, N9, N11, N13, N15, N17, R9, R10, R11, R12, R13, R15, R16, R17, T10, T19, Y8, Y9, Y10, Y11, Y12, Y13	VDD_CX	Power for the digital core circuits
F12	VDD_IO_EBI_0_CK	Power for the EBI0 I/O clock circuits
F19	VDD_IO_EBI_1_CK	Power for the EBI1 I/O clock circuits
G9, G10, G13, G14, G17, G18, G21, G22	VDD_IO_EBI	Power for the EBI I/O circuits
L25	VDD_A_USB_SS_1P8	Power for USB SS 1.8 V circuits
AB20, AB21, L10, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, N20, R19, T23, V9, V10, V11, V12, V13, V14	VDD_MX	Power for on-chip memory

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad number	Pad name	Functional description
Y15	VDD_MX_TXDAC	Power for TXDAC memory circuits
AC18	VDD_PX0	Power for the pad group 0
T25	VDD_PX11	Power for the CXO pads
F10, F13, F18, F21, F24	VDD_PX1	Power for the EBI I/O circuits
AE17	VDD_PX2	Power for the pad group 2 – SDC2 pads
AA7, AC23, AF17, G26, M6, T26, F11, F20, N19	VDD_PX3	Power for the pad group 3 – most I/O pads
AC17	VDD_PX5	Power for the pad group 5
AD18	VDD_PX6	Power for the pad group 6
G24	VDD_PX7	Power for the pad group 7 – eMMC pads
AD17	VDD_SDCREF_1P25	Reference voltage for SDC
AD19	VDD_REF_1P25	Reference voltage
AA21, AA22, AA23, AA24, AA25, AA26, R20, R22, U19, U20, U21, U23, W18, W19, W20, W21, Y18, Y19, Y20, Y21, Y22, Y23, Y24	VDD_APC	Power for the application processor
W16, W17	VDD_CX_LPI	Power for LPI digital core circuits
Y17	VDD_MX_LPI	Power for LPI memory circuits
P19	VDD_QFPROM	Power for programming the QFPROM
M25	VDD_USB_HS_0P9	Power for the USB HS 0.9 V circuits
J9, J10, J11	VDD_CX_WLAN	Power for the WLAN core circuits

Table 2-4 Pin descriptions – DNC, ground, and power-supply pins (cont.)

Pad number	Pad name	Functional description
A4, A13, A14, A16, A17, A27, AA6, AA8, AA9, AA11, AA12, AA14, AA16, AA17, AA18, AA19, AA20, AB3, AB7, AB8, AB9, AB12, AB13, AB14, AB22, AB23, AB24, AB25, AB26, AC6, AC7, AC9, AC10, AC11, AC13, AC15, AC16, AC20, AC21, AC22, AC24, AC28, AD3, AD6, AD7, AD9, AD14, AD15, AE7, AE8, AE10, AE12, AE15, AE18, AF7, AF8, AF10, AF12, AF15, AF16, AG3, AG5, AG7, AG8, AG9, AG10, AG11, AG12, AG13, AG14, AG15, AG16, AG17, AG20, AG22, AG24, AG26, AG28, B2, B3, B4, B14, B16, B27, C2, C3, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, D1, D2, D3, D14, D16, D27, E2, E3, E4, E14, E15, E16, E26, E27, F2, F3, F4, F5, F6, F7, F8, F9, F22, F23, F25, F26, F27, F29, G5, G6, G8, G11, G12, G19, G20, G23, G28, H2, H5, H6, H7, H24, H25, H26, H28, J2, J3, J4, J5, J6, J12, J13, J14, J15, J16, J17, J18, J19, J20, J22, J25, J26, J29, K5, k6, K10, K19, K20, K25, K26, K27, L3, L6, L7, L8, L24, L27, L28, L29, M7, M8, M10, M11, M13, M15, M16, M17, M18, M22, M26, N5, N7, N8, N21, N25, N26, P4, P5, P6, P7, P8, P10, P11, P12, P13, P14, P17, P18, P25, P26, P28, R5, R6, R23, R27, R29, T5, T6, T9, T11, T13, T15, T17, T20, T22, T29, U4, U5, U6, U10, U11, U13, U15, U17, U26, U28, V5, V6, V7, V8, V15, V16, V17, V18, V19, V21, V23, V24, V26, V29, W5, W6, W9, W10, W11, W13, W22, W23, W24, W26, W27, Y4, Y5, Y6, Y26, Y27	GND	Ground
A1, A30, AJ1, AJ30, AC26, AC25, F17, F28, AB27, L26, W2, Y2, AB1, W3, Y3, AA2, W4, AA1, AA3, W1, C16, B15, C15, D15, A15, G16, F16, G25, J24, U7, AE28, AF28, AH28, AJ28, AE27, AF27, AG27, AE26, AF26	DNC	Do not connect; connected internally, do not connect externally.

3 Electrical specifications

This topic defines the device electrical performance specifications, including absolute maximum ratings, operating conditions, and subsystem (such as memory and connectivity) parameters, which are useful in deploying the device with optimal processing capabilities and high efficiency.

3.1 Absolute maximum ratings

The absolute maximum ratings table reflects the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Minimum	Maximum	Unit
Power supply voltages				
VDD_APC	Kryo application processor	-0.30	1.36	V
VDD_CX	Digital core circuit	-0.30	1.18	V
VDD_CX_WLAN	WLAN core circuit	-0.30	0.86	V
VDD_MX VDD_MX_TXDAC VDD_A_APC_PLL_0P9 VDD_A_EBI_0_0P9 VDD_A_EBI_1_0P9 VDD_A_DSI_0P9 VDD_A_EBI_CC_0P9	On-chip memory TXDAC memory circuit APC PLL circuit EBI0 circuit EBI1 circuit DSI 0.9 V circuit EBI clock circuit	-0.30	1.18	V
VDD_CX_LPI	LPI digital core circuit	-0.30	1.18	V
VDD_MX_LPI	LPI memory circuit	-0.30	1.18	V
VDD_A_EBI_PLL_0P9 VDD_A_QREFS_0P9	EBI PLL circuit Reference voltage for QREFS 0P9 circuit	-0.30	1.04	V
VDD_A_USB_HS_1P8 VDD_A_USB_SS_1P8 VDD_A_AUDIO_PLL_1P8 VDD_A_CAMSS_PLL_1P8 VDD_PX11 VDD_QFPROM VDD_A2 VDD_A_WLAN_PLL_1P8 VDD_A_MODEM_PLL_1P8	USB HS 1.8 V circuit USB SS 1.8 V circuit Audio PLL circuit Camera PLL circuit CXO pad QFPROM circuit High voltage – analog circuit WLAN PLL circuit Modem PLL circuit	-0.3	2.06	V
VDD_A_CSI_0_1P2 VDD_A_CSI_1_1P2 VDD_A_DSI_PLL_1P2 VDD_A_DSI_1P2 VDD_A1	CSI0 1.2 V circuit CSI1 1.2 V circuit DSI PLL circuit DSI 1.2 V circuit Low voltage – analog circuit	-0.3	1.39	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Minimum	Maximum	Unit
VDD_A_PLL_HV_CC_EBI_1P2	EBI PLL high voltage circuit			
VDD_IO_EBI_0_CK VDD_IO_EBI_1_CK VDD_IO_EBI	EBI0 I/O clock circuit EBI1 I/O clock circuit EBI I/O circuit	-0.3	1.37	V
VDD_A_WLAN_ADCDAC0_1P3 VDD_A_WLAN_ADCDAC1_1P3	WLAN ADC and DAC 0 WLAN ADC and DAC 1	-0.3	1.43	V
VDD_A_USB_SS_0P9 VDD_USB_HS_0P9	USB SS 0P9 circuit USB HS 0.9 V circuit	0.3	1.04	V
VDD_A_USB_HS_3P1	USB HS 3.1 V circuit	-0.3	3.52	V
VDD_SDCREF_1P25 VDD_REF_1P25	Reference voltage for SDC Reference voltage	-0.3	1.43	V
VDD_PX0	Pad group 0	-0.3	2.09	V
VDD_PX1	EBI I/O circuit	-0.3	1.37	V
VDD_PX2	Pad group 2 – SDC2 pad Low voltage High voltage	-0.3	3.41	V
VDD_PX3	Pad group 3 – most I/O pad	-0.3	2.09	V
VDD_PX5	Pad group 5 Low voltage High voltage	-0.3	3.41	V
VDD_PX6	Pad group 6 Low voltage High voltage	-0.3	3.41	V
VDD_PX7	Pad group 7 – eMMC pad	-0.30	2.09	V
T_S	Storage temperature [a] [b]	-55	150	°C

[a] The storage temperature range applies when the device is in the OFF state (the device is not assembled in any platform and is not electrically connected to any voltage or I/O signals). Damage may occur when the device is subjected to this temperature for any length of time.

[b] For devices shipped in tape and reel, the storage temperature range is [+15°C~35°C] and < -90% relative humidity (RH). QTI recommends allowing the device to return to ambient room temperature before usage.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-3). The QRB2210 meets all performance specifications listed in Section 3.3 through Section 3.12, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions for voltage rails with AVS Type-1

Parameter [a]		Min	Max	Unit
Power supply voltages				
VDD_APC	Kryo application processor Turbo-L2	 0.87	 1.23	V

Table 3-2 Operating conditions for voltage rails with AVS Type-1 (cont.)

Parameter [a]		Min	Max	Unit
	Turbo-L1	0.82	1.16	
	Turbo	0.76	1.07	
	Nominal-L1	0.71	1.00	
	Nominal	0.68	0.94	
	SVS-L1	0.62	0.86	
	SVS	0.57	0.78	
	Low-SVS	0.57	0.69	
VDD_CX	Digital core circuits			V
	Turbo-L1	0.79	1.07	
	Turbo	0.73	1.07	
	Nominal-L1	0.69	1.00	
	Nominal	0.66	0.94	
	SVS-U1	0.60	0.86	
	SVS	0.55	0.78	
	Low-SVS	0.49	0.69	
VDD_CX_LPI	LPI digital core circuits			V
	Turbo	0.73	1.07	
	Nominal	0.66	0.94	
	SVS_U1	0.6	0.86	
	SVS	0.55	0.78	
	Low_SVS	0.49	0.69	
VDD_MX_LPI	LPI memory circuits			V
	Turbo	0.79	1.07	
	Nominal	0.79	1.00	
VDD_MX VDD_MX_TXDAC VDD_A_APC_PLL_0P9 VDD_A_EBI_0_0P9 VDD_A_EBI_1_0P9 VDD_A_DSI_0P9 VDD_A_EBI_CC_0P9	Memory and analog PLL circutis Turbo Nominal	 0.79 0.79	 1.07 1.00	V
VDD_CX_WLAN	WLAN core circuits			V
	Nominal	0.55	0.78	

[a] Parts with voltages outside of the specified ranges are not guaranteed to operate properly.

Table 3-3 Operating conditions

Parameter [a]		Min	Typ [b]	Max	Unit
Power supply voltages					
VDD_A_EBI_PLL_0P9 VDD_A_QREFS_0P9	EBI PLL circuit Reference voltage for QREFS 0P9 circuit	0.89	0.92	0.95	V
VDD_A_USB_HS_1P8 VDD_A_USB_SS_1P8 VDD_A_AUDIO_PLL_1P8 VDD_A_CAMSS_PLL_1P8 VDD_PX11 VDD_QFPROM VDD_A2 VDD_A_WLAN_PLL_1P8 VDD_A_MODEM_PLL_1P8	USB HS 1.8 V circuit USB SS 1.8 V circuit Audio PLL circuit Camera PLL circuit CXO pad QFPROM circuit High voltage – analog circuit WLAN PLL circuit Modem PLL circuit	1.74	1.80	1.87	V
VDD_A_CSI_0_1P2 VDD_A_CSI_1_1P2 VDD_A_DSI_PLL_1P2 VDD_A_DSI_1P2 VDD_A1 VDD_A_PLL_HV_CC_EBI_1P2	CSI0 1.2 V circuit CSI1 1.2 V circuit DSI PLL circuit DSI 1.2 V circuit Low voltage – analog circuit EBI PLL high voltage circuit	1.15	1.20	1.26	V
VDD_IO_EBI_0_CK VDD_IO_EBI_1_CK VDD_IO_EBI	EBI0 I/O clock circuit EBI1 I/O clock circuit EBI I/O circuit (**Note:** This value is for LPDDR4X)	0.59	0.60	0.63	V
	EBI0 I/O clock circuit EBI1 I/O clock circuit EBI I/O circuit (**Note:** This value is for LPDDR3)	1.15	1.20	1.25	V
VDD_A_WLAN_ADCDAC0_1P3 VDD_A_WLAN_ADCDAC1_1P3	WLAN ADC and DAC 0 WLAN ADC and DAC 1	1.25	–	1.30	V
VDD_A_USB_SS_0P9 VDD_USB_HS_0P9	USB SS 0.9 V circuit USB HS 0.9 V circuit	0.89	0.92	0.95	V
VDD_A_USB_HS_3P1	USB HS 3.1 V circuit	2.95	3.10	3.20	V
VDD_SDCREF_1P25 VDD_REF_1P25	Reference voltage for SDC Reference voltage	1.15	1.25	1.30	V
VDD_PX0	Pad group 0	1.7	1.8	1.9	V
VDD_PX1	EBI I/O circuit (**Note:** This value is for LPDDR4X)	1.05	1.10	1.15	V

Table 3-3 Operating conditions (cont.)

Parameter [a]		Min	Typ [b]	Max	Unit
	EBI I/O circuit (**Note:** This value is for LPDDR3)	1.15	1.20	1.25	V
VDD_PX2	Pad group 2 – SDC2 pad				V
	Low voltage	1.70	1.80	1.90	
	High voltage	2.70	2.95	3.10	
VDD_PX3	Pad group 3 – most I/O pad	1.70	1.80	1.90	V
VDD_PX5	Pad group 5				V
	Low voltage	1.70	1.80	1.90	
	High voltage	2.70	2.95	3.10	
VDD_PX6	Pad group 6				V
	Low voltage	1.70	1.80	1.90	
	High voltage	2.70	2.95	3.10	
VDD_PX7	Pad group 7 – eMMC pad	1.70	1.80	1.90	V
Thermal conditions					
T	Device operating temperature	$T_{ambient}$ = -30	–	$T_{junction}$ = +95	°C

[a] Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
[b] Typical voltages represent the recommended output settings of the companion PMIC device.

3.2.1 Core and memory voltage minimization (retention mode)

The MPM supports VDD minimization, also known as VDD_CORE and VDD_MEM retention mode. This technique reduces the leakage of the digital logic by reducing VDD to the minimum required to maintain the register and memory state.

The V(MIN) for state retention is found through characterization.

Table 3-4 Core voltage in retention mode

VDD_CORE	Bit 31 (MSB)	Bit 30	Bit 29 (LSB)
0.4 V	1	0	0
0.45 V	0	1	1
0.5 V	0	1	0
0.55 V	0	0	1
0.6 V	0	0	0

NOTE
1. The VDD_CORE voltages specified are PMIC settings.
2. For fuse locations listed in this table, see register 0x1B40184.

Table 3-5 Memory voltage in retention mode

VDD_MEM	Bit 19 (MSB)	Bit 18	Bit 17 (LSB)
0.49 V	1	0	0
0.55 V	0	1	1

Table 3-5 Memory voltage in retention mode (cont.)

VDD_MEM	Bit 19 (MSB)	Bit 18	Bit 17 (LSB)
0.58 V	0	1	0
0.65 V	0	0	1
0.7 V	0	0	0

NOTE
1. The VDD_MEM voltages specified are PMIC settings.
2. For fuse locations listed in this table, see register 0x1B40198.

3.3 Power delivery network specification

The following subsections contain the maximum impedance specifications for the power delivery network (PDN).

Table 3-6 QRB2210 PDN specifications

PMIC regulator	Power domain	PDN ports	Maximum DC resistance (mΩ)	Maximum effective impedance Z [a] (mΩ)		Positive pins	Negative pins
				R_{mid_freq} (mΩ)	Inductance (pH)		
VREG_S1A	VDD_APC	1	4	6	100	AA26, AA25, AA24, AA23, AA22, AA21, Y24, Y23, Y22, Y21, Y20, Y19, Y18, W21, W20, W19, W18, U23, U21, U20, U19, R22, R20	AB26, AB25, AB24, AB23, AB22, AA20, AA19, AA18, AA17, Y27, Y26, W24, W23, W22, V24, V21, V19, V18, T22, T20, R23
VREG_S2A	VDD_CX	1	4	11	220	Y13, Y12, Y11, Y10, Y9, Y8	AA14, AA12, AA11, AA9, AA8, W13, W11, W10, W9
		2	4	9	75	T19, R17, R16, R15, R13, R12, R11, R10, R9, N17, N15, N13, N11, N9, M19, K22, K18, K17, K16, K15, K14, K13, K12, K11, T10	T20, T17, T15, T13, T11, T9, P18, P17, P14, P13, P12, P11, P10, P8, N8, M18, M17, M16, M15, M13, M11, M10, K20, K19, K10, J22, J20, J19, J18, J17, J16, J15, J14, J13, J12
VREG_L1A	VDD_MX	1	26	37	630	AB21, AB20	AC22, AC21, AC20, AB22, AA20, AA19
		2	22	30	205	V14, V13, V12, V11, V10, V9	W13, W11, W10, W9, V15, V8, U15, U13, U11, U10
		3	19	23	126	U22, R19, N20, L20, L19, L18, L17, L16, L15, L14, L13, L12, L11, L10	V23, T22, T20, P18, N21, M18, M17, M16, M15, M13, M11, M10, K20, K19, K10
		4	28	35	620	T23	R23, T22
VREG_L7A	VDD_CX_WLAN	1	84	132	650	J9, J10, J11	K10, J12
VREG_L8A	VDD_CX_LPI	1	71	109	800	W16, W17	V15, V16, V17
VREG_L9A	VDD_MX_LPI	1	170	190	1360	Y17	AA17, AA18

a The PDN AC impedance specification (mask) is obtained by plotting Impedance Z_{spec} using R_{mid_freq} and inductance (L) values from this table. Z_{spec} $Z_{spec} = \sqrt{R_{mid_freq}^2 + (2\pi f L)^2}$

Table 3-7 LPDDR4X PDN specifications

Power regulator	Power domain	PDN ports	Maximum DC resistance (mΩ)	Maximum effective impedance Z [a] (mΩ)		Positive pins	Negative pins
				$R_{mid\text{-}freq}$ (mΩ)	Inductance (pH)		
VREG_L3A	VDD_IO_EBI	VDD_IO_EBI_A	45	145	2250	G9, G10	F8, F9, G8, G11
		VDD_IO_EBI_B	45	145	2250	G13, G14	G12
		VDD_IO_EBI_C	45	145	2250	G17, G18	G19
		VDD_IO_EBI_D	45	145	2250	G21, G22	F22, F23, G20
	VDD_IO_EBI_CK	VDD_IO_EBI_0_CK	45	145	2250	F12	G11, G12
		VDD_IO_EBI_1_CK	45	145	2250	F19	G19, G20
VREG_L2A	VDD_PX1	VDD_PX1_A	45	136	2550	F10	F9, G11
		VDD_PX1_B	45	136	2550	F13	E14, G12
		VDD_PX1_C	45	136	2550	F18	G19
		VDD_PX1_D	45	136	2550	F21	F22, G20
		VDD_PX1_E	45	136	2550	F24	F23, G23, F25
VREG_L1A	VDD_A_EBI	VDD_A_EBI0_0P9_A	35	135	1835	H9	G8
		VDD_A_EBI0_0P9_B	35	135	1835	H11	G11, G12
		VDD_A_EBI_0_0P9_C	35	135	1835	H13	G12, J12, J13, J14
		VDD_A_EBI_1_0P9_A	35	135	1835	H18	G19, J17, J18, J19
		VDD_A_EBI_1_0P9_B	35	135	1835	H20	G19, G20, J19, J20
		VDD_A_EBI_1_0P9_C	35	135	1835	H22	G23, J22

a

The PDN AC impedance specification (mask) is obtained by plotting Impedance Z_{spec} using R_{mid_freq} and inductance (L) values from this table. Z_{spec} $Z_{spec} = \sqrt{R_{mid_freq}^2 + (2\pi f L)^2}$

Table 3-8 LPDDR3 PDN specifications

Power regulator	Power domain	PDN ports	Maximum DC resistance (mΩ)	Maximum effective impedance Z [a] (mΩ)		Positive pins	Negative pins
				$R_{mid\text{-}freq}$ (mΩ)	Inductance (pH)		
VREG_L2A	VDD_IO_EBI	VDD_IO_EBI_A	45	145	2520	G9, G10	F8, F9, G8, G11
		VDD_IO_EBI_B	45	145	2520	G13, G14	G12
		VDD_IO_EBI_C	45	145	2520	G17, G18	G19
		VDD_IO_EBI_D	45	145	2520	G21, G22	F22, F23, G20

Table 3-8 LPDDR3 PDN specifications (cont.)

Power regulator	Power domain	PDN ports	Maximum DC resistance (mΩ)	Maximum effective impedance Z [a] (mΩ)		Positive pins	Negative pins
				$R_{mid\text{-}freq}$ (mΩ)	Inductance (pH)		
	VDD_IO_CK_EBI	VDD_IO_EBI_0_CK	45	145	2520	F12	G11, G12
		VDD_IO_EBI_1_CK	45	145	2520	F19	G19, G20
	VDD_PX1	VDD_PX1_A	40	136	2550	F10	F9, G11
		VDD_PX1_B	40	136	2550	F13	E14, G12
		VDD_PX1_C	40	136	2550	F18	G19
		VDD_PX1_D	40	136	2550	F21	F22, G20
		VDD_PX1_E	40	136	2550	F24	F23, G23, F25
VREG_L1A	VDD_A_EBI	VDD_A_EBI0_0P9_A	35	135	1835	H9	G8
		VDD_A_EBI0_0P9_B	35	135	1835	H11	G11, G12
		VDD_A_EBI_0_0P9_C	35	135	1835	H13	G12, J12, J13, J14
		VDD_A_EBI_1_0P9_A	35	135	1835	H18	G19, J17, J18, J19
		VDD_A_EBI_1_0P9_B	35	135	1835	H20	G19, G20, J19, J20
		VDD_A_EBI_1_0P9_C	35	135	1835	H22	G23, J22

a

The PDN AC impedance specification (mask) is obtained by plotting Impedance Z_{spec} using R_{mid_freq} and inductance (L) values from this table. Z_{spec} $Z_{spec} = \sqrt{R_{mid_freq}^2 + (2\pi f L)^2}$

Table 3-9 SerDes PDN specifications

Power regulator	Power domain	PDN ports	Maximum DC resistance (mΩ) lumped port	Maximum DC resistance (mΩ)	Maximum impedance Z [a] (mΩ)		Positive pins	Negative pins
					R_{mid_freq} (mΩ)	Inductance (pH)		
VREG_L13A	VDD_A_USB_HS_1P8	1	68	700	235	1500	M24	L24
	VDD_A_USB_SS_DP_1P8	2	68	1300	235	1500	L25	L24, K25
VREG_L21A	VDD_A_USB_HS_3P1	1	–	700	235	1500	M23	L24, M22
VREG_L5A	VDD_A_DSI_1P2	1	97	1350	157	1000	P23	R23
	VDD_A_DSI_PLL	2	97	4000	235	1500	N24	N25, P25
	VDD_A_CSI_0_1P2	3	97	450	235	1500	R7	P6, P7, P8, R6, T6
	VDD_A_CSI_1_1P2	4	97	450	235	1500	T7	R6, T6, U6

Table 3-9 SerDes PDN specifications (cont.)

Power regulator	Power domain	PDN ports	Maximum DC resistance (mΩ) lumped port	Maximum DC resistance (mΩ)	Maximum impedance Z [a] (mΩ)		Positive pins	Negative pins
					R_{mid_freq} (mΩ)	Inductance (pH)		
VREG_L12A	VDD_A_USB_SS_0P9	1	128	130	157	1000	K24	J25, K25
	VDD_USB_HS_0P9	2	128	1400	157	1020	M25	M26, N26, N25
VREG_L1A	VDD_A_DSI_0P9	1	–	450	235	1500	P24	P25, R23

a

The PDN AC impedance specification (mask) is obtained by plotting Impedance Z_{spec} using R_{mid_freq} and inductance (L) values from this table. Z_{spec} $Z_{spec} = \sqrt{R_{mid_freq}^2 + (2\pi f L)^2}$

3.4 DC power characteristics

3.4.1 Average operating current

Detailed current consumption information and details about the operating modes tested are available in the document *QRB2210 Linux Android Current Consumption Data (80-30843-7; to be released)*.

3.4.2 Dhrystone and rock bottom maximum power

Table 3-10 Dhrystone and rock bottom maximum power

SDM version	Quad core at 2 GHz, Dhrystone (W) at +95°C (Tj) [a] [b] [c]	Rock bottom (mW) at 30°C (Tj) [d]
QRB2210	1.5	10.4

[a] Temperature reading is from the QRB2210 device's internal temperature sensor.
[b] Dhrystone power should be measured on the VDD_APC rail, right before PDN capacitors (with a small serial sampling resistor inserted, if necessary).
[c] Measurement sampling rate should be > 1.25 Msps (or < 0.8 µs), and the average window should be > 1 ms (or > 1250 samples).
[d] Rock bottom (VDD_CORE and VDD_MEM) power should be measured at VDD_CORE and VDD_MEM rails when VDD_CORE and VDD_MEM are at retention voltage. See AIR1 in Table 3.1 (Test definitions) in the *QRB2210 Android Current Consumption Data (80-30843-7; to be released)*.

3.5 Power sequencing

The PMIC includes power-on circuits that provide the proper power sequencing for the entire QRB2210 chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of some PMIC pins. See the appropriate PMIC device specification, such as the *PM4125 Power Management IC Data Sheet (80-PW090-1)*.

A high-level summary of the required default power-on sequence is:

Sequence	Power domain
1.	VDD_MX, VDD_MX_TXDAC, VDD_A_APC_PLL_0P9, VDD_A_EBI_0_0P9, VDD_A_EBI_1_0P9, VDD_A_DSI_0P9, VDD_A_EBI_CC_0P9
2.	VDD_MX_LPI
3.	VDD_CX
4.	VDD_CX_LPI
5.	VDD_CX_WLAN
6.	VDD_PX0, VDD_PX3, VDD_PX7
7.	VREF_MSM
8.	VDD_A_CSI_0_1P2, VDD_A_CSI_1_1P2, VDD_A_DSI_PLL_1P2, VDD_A_DSI_1P2, VDD_A1, VDD_A_PLL_HV_CC_EBI_1P2
9.	VDD_A_USB_SS_0P9, VDD_USB_HS_0P9
10.	VDD_A_EBI_PLL_0P9, VDD_A_QREFS_0P9
11.	VDD_PX1
12.	VDD_IO_EBI_0_CK, VDD_IO_EBI_1_CK, VDD_IO_EBI
13.	VREF_LPDDR3
14.	VDD_QFPROM, VDD_PX11, VDD_A2, VDD_A_USB_SS_1P8, VDD_A_USB_HS_1P8, VDD_A_AUDIO_PLL_1P8, VDD_A_CAMSS_PLL_1P8, VDD_A_WLAN_PLL_1P8, VDD_A_MODEM_PLL_1P8

Sequence	Power domain
15.	VDD_PX2
16.	VDD_A_USB_HS_3P1
17.	VDD_APC

This sequence includes:

- The core voltage (VDD_CX) needs to power up before the pad circuits (VDD_PX), so that the internal circuits can take control of the I/Os and pads.
  - If pad voltages power-up first, the output drivers might be stuck in unknown states and might cause large leakage currents until VDD_CX powers on.
- Any other appropriate supplies can be powered on by software after the sequence is completed.
- Each domain needs to reach its 90% value before the next domain starts ramping up. For example, when VDD_CX reaches 90% of its value, the VDD_CX_LPI supply can start ramping up.

3.6 Digital-logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the QRB2210 device and other ICs within the QTI chipset; therefore, specifications are not required.
- Some are defined by existing standards, such as I^2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications.

Table 3-11 DC specification of 1.8 V GPIOs and WCSS WSI I/Os

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	0.65 × VDDPX	VDDPX + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = low)	-0.3 V	0.35 × VDDPX	V
V_{IH}	High-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	0.7 × VDDPX	VDDPX + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt (HIHYS_EN = high)	-0.3 V	0.3 × VDDPX	V
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN= low)	100	–	mV
V_{SHYS}	Schmitt hysteresis voltage (HIHYS_EN = high)	300	–	mV
I_{IH}	Input high leakage current [a]	–	1.0	µA
I_{IL}	Input low leakage current [a]	-1.0	–	µA
I_{IHPD}	Input high leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{ILPU}	Input low leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)
I_{OZH}	High-level, tri-state leakage current [a]	–	1.0	µA
I_{OZL}	Low-level, tri-state leakage current [a]	-1.0	–	µA
I_{OZHPD}	High-level, tri-state leakage current with pull-down	27.5 (60)	97.5 (20)	µA (kΩ)
I_{OZLPU}	Low-level, tri-state leakage current with pull-up	-97.5 (20)	-27.5 (60)	µA (kΩ)

Table 3-11 DC specification of 1.8 V GPIOs and WCSS WSI I/Os (cont.)

Parameter	Description	Min	Max	Units
I_{OZHKP}	High-level, tri-state leakage current with keeper [b]	-22.5 (20)	-7.5 (60)	µA (kΩ)
I_{OZLKP}	Low-level, tri-state leakage current with keeper [c]	7.5 (60)	22.5 (20)	µA (kΩ)
V_{OH}	High-level output voltage, CMOS	VDDPX - 0.45	VDDPX	V
V_{OL}	Low-level output voltage, CMOS	0.0	0.45	V

[a] I_{IH}, I_{IL}, I_{OZH}, and I_{OZL} values are based on nominal PVT (TT/25°C).
[b] Pin voltage = VDDPX maximum. For keeper pins, pin voltage = VDDPX maximum - 0.45 V.
[c] Pin voltage = GND and supply = VDDPX maximum. For keeper pins, pin voltage = 0.45 V and supply = VDDPX maximum.

Table 3-12 SDC 2.95 V mode DC specifications (VDDPX_2)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.625 × VDDPX	–	VDDPX + 0.3	V
V_{IL}	Low-level input voltage	- 0.3	–	0.25 × VDDPX	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	10	µA
I_{IL}	Input low leakage current	-10	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	0.75 × VDDPX	–	VDDPX	V
V_{OL}	Low-level output voltage	0	–	0.125 × VDDPX	V

Table 3-13 SDC 1.8 V mode DC specifications (VDDPX_2)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	1.27	–	2	V
V_{IL}	Low-level input voltage	-0.3	–	0.58	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	–	–	5	µA
I_{IL}	Input low leakage current	-5	–	–	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ

Table 3-13 SDC 1.8 V mode DC specifications (VDDPX_2) (cont.)

Parameter	Description	Min	Typ	Max	Units
V_{OH}	High-level output voltage	1.4	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45	V

Table 3-14 VDDPX_5 and VDDPX_6 2.95 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.7 × VDDPX	–	VDDPX + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.2 × VDDPX	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	0.8 × VDDPX	–	VDDPX	V
V_{OL}	Low-level output voltage	0	–	0.4	V

Table 3-15 VDDPX_5 and VDDPX_6 1.8 V mode DC specifications

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.7 × VDDPX	–	VDDPX + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.2 × VDDPX	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current	-20	–	20	µA
I_{IL}	Input low leakage current	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10	–	100	kΩ
$R_{PULL-DOWN}$	Pull-down resistance	10	–	100	kΩ
$R_{KEEPER-UP}$	Keeper-up resistance	10	–	100	kΩ
$R_{KEEPER-DOWN}$	Keeper-down resistance	10	–	100	kΩ
V_{OH}	High-level output voltage	0.8 × VDDPX	–	VDDPX	V
V_{OL}	Low-level output voltage	0	–	0.4	V

3.7 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included here.

NOTE All QRB2210 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.7.2.

3.7.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in the figure below.

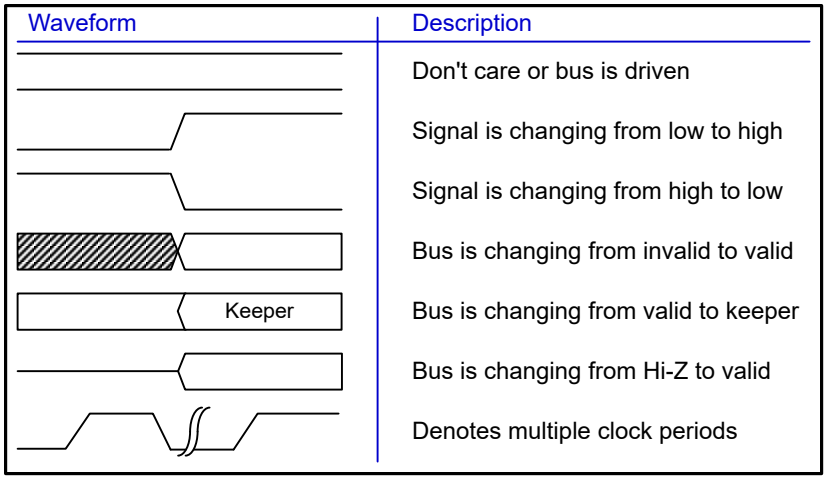


Figure 3-1 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates don't care.

3.7.2 Rise and fall time specifications

The testers that characterize QRB2210 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in the figure below.

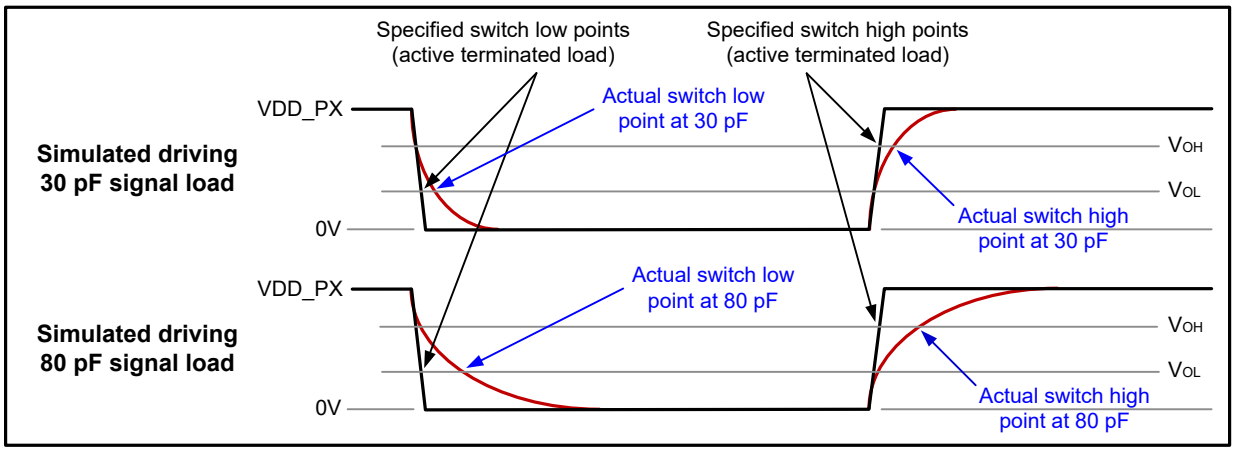


Figure 3-2 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the QRB2210 device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.7.3 Pad design methodology

The QRB2210 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric, with respect to the associated V_{DD_PX} supply (Figure 3-3). The input switch point for pure input-only pads is designed to be $V_{DD_PX}/2$ (or 50% of V_{DD_PX}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DD_PX} for V_IL and 65% of V_{DD_PX} for V_{IH}.

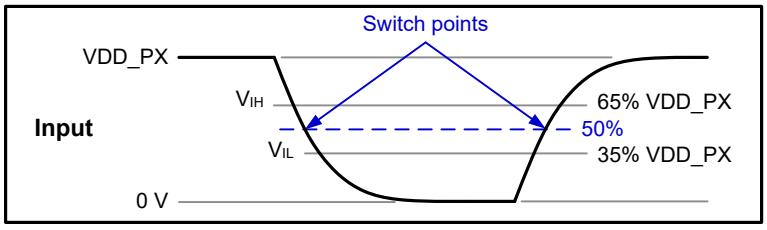


Figure 3-3 Digital input-signal switch points

Outputs (such as addresses, chip selects, and clocks) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL} (max) levels over worst-case process/voltage/temperature. Because the pad output structures (Figure 3-4) are essentially CMOS drivers that possibly have a small

amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected zero DC load outputs are estimated to be:

- V_{OH} ~ V_{DD_PX} - 50 mV or more
- V_{OL} ~ 50 mV or less

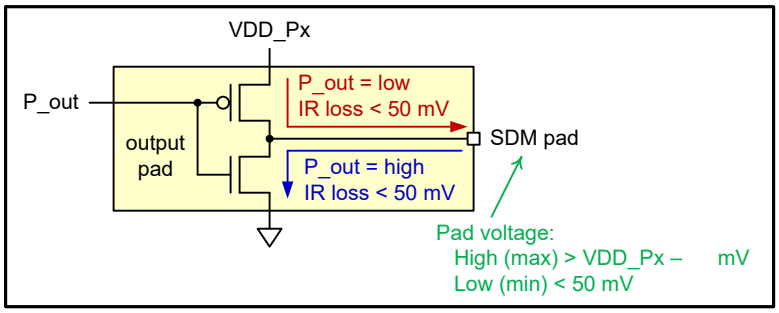


Figure 3-4 Output pad equivalent circuit

The DC output drive strength can be approximated by linear interpolations between V_{OH} (min) and V_{DD_PX} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DD_PX} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of ISC is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to minimize output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (**t**(r)) and fall time (**t**(f)) values are functions of board loading.

Bi-directional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both the input and output behaviors were described above.

3.8 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup time numbers will get worse, and hold time numbers may improve.

3.8.1 EBI0 and EBI1 memory support

EBI0 and EBI1 are dedicated non-PoP type LPDDR4X or LPDDR3 memory. It supports LPDDR4X and LPDDR3 SDRAM memory parts that are compliant with the *JEDEC Standard for Low-Power Double Data Rate 4 SDRAM* (JESD209-4-1) and *JEDEC Standard for Low-Power Double Data Rate 3* (JESD209-3B).

3.8.2 eMMC on SDC1

eMMC NAND flash can be supported via the SDC1 port. See Section 3.10.1 for secure digital interface details.

3.9 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.9.1 Camera interfaces

The QRB2210 device supports three 4-lane DPHY or CPHY camera interfaces.

Table 3-16 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for DPHY v1.2	Supports only unidirectional data receiving
MIPI Alliance Specification for CPHY v1.0	None

3.9.2 Audio support

The QRB2210 supports the PM4125 audio codec IC through SourndWire interface to provide the system's audio functions.

Other audio-related interface options include:

- I^2S – Section 3.10.3
- Digital microphone – Section 3.10.4
- SoundWire – Section 3.10.5
- I^2C – Section 3.10.7

3.9.3 Display support

The QRB2210 device supports one 4-lane MIPI DSI port.

Table 3-17 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for D-PHY v1.2	None

3.10 Connectivity

The connectivity functions supported by the QRB2210 that require electrical specifications include:

- SD, including SD cards and multimedia cards (MMC)
- USB host/slave support with built-in physical layer (PHY)
- Serial low-power interchip media bus (SLIMbus) interface
- Inter-IC sound (I^2S) interfaces
- Touchscreen connections

- Dedicated I^2C interfaces for camera (CCI I2C)
- Through proper configuration of the 10 QUP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports
  - I3C interface for sensor support

Pertinent specifications for these functions are detailed in the following subsections.

NOTE In addition to the following hardware specifications, see the latest software release notes for software-based performance features or limitations.

3.10.1 SD interfaces

Table 3-18 Supported SD standards and exceptions

Applicable standard	Feature exceptions
Multimedia Card Host Specification, version 5.1	None
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

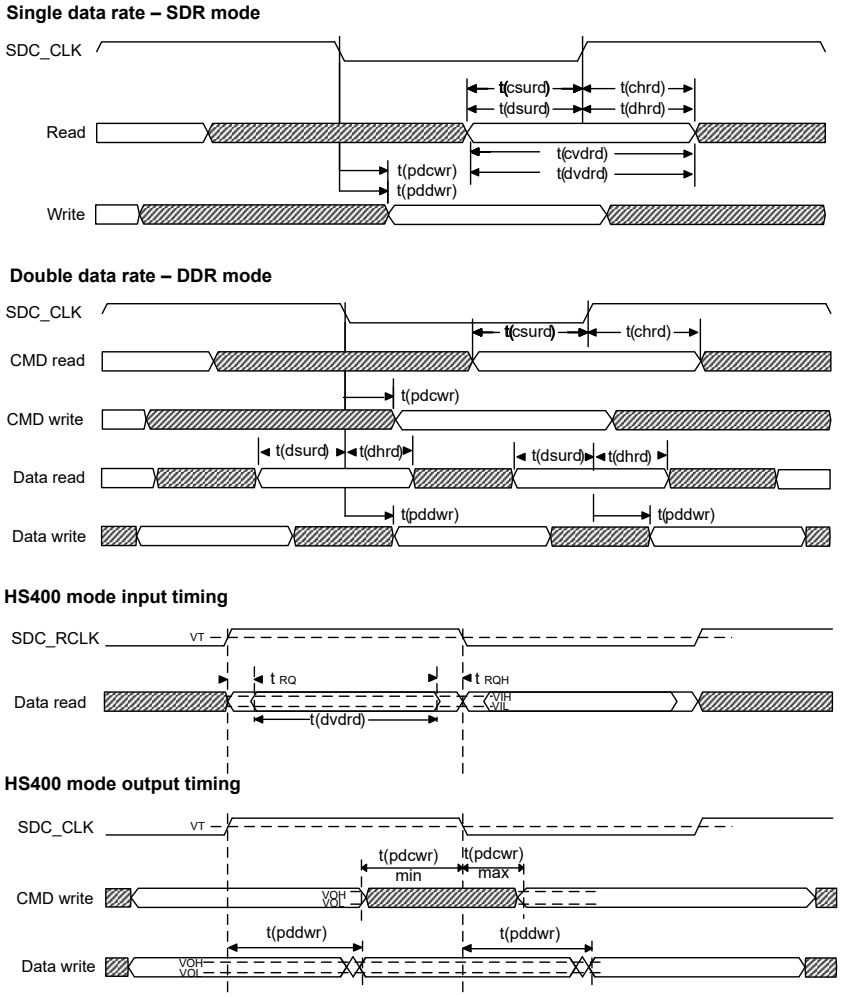


Figure 3-5 SD interface timing

3.10.2 USB interfaces

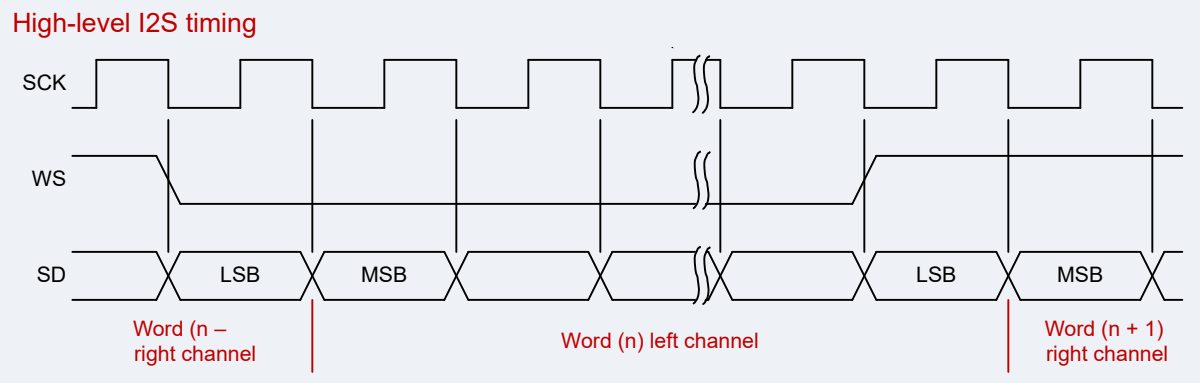
Table 3-19 Supported USB standards and exceptions

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2
Universal Serial Bus Specification, Revision 2.0 (April 27, 2000 or later)	Low speed is not supported in device mode
On-The-Go Supplement to the USB 2.0 Specification (June 24, 2003, Revision 1.0 A or later)	Supports the host mode aspect of OTG only

3.10.3 I²S interfaces

Table 3-20 Supported I²S standards and exceptions

Applicable standards	Feature exceptions
Philips I2S Bus Specifications revised June 5, 1996 (Available for free download.)	None



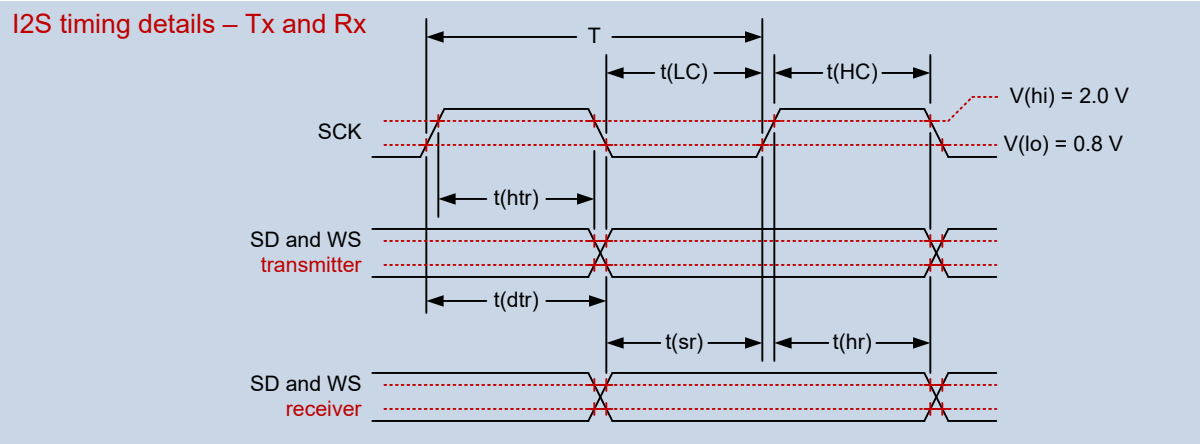


Figure 3-6 I²S timing diagram

Table 3-21 I²S interface timing – MI²S interface 1 and 2 (primary and secondary MI²S)

Parameter		Min	Typ	Max	Unit
Using internal SCK					
	Frequency	–	–	24.576	MHz
T	Clock period	40.69	–	–	ns
t(HC)	Clock high	0.4 × T	–	0.6 × T	ns
t(LC)	Clock low	0.4 × T	–	0.6 × T	ns
t(sr)	SD and WS input setup time	8.14	–	–	ns
t(hr)	SD and WS input hold time	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	6.10	ns
t(htr)	SD and WS output hold time	0	–	–	ns
Using external SCK					
	Frequency	-	–	24.576	MHz

Table 3-21 I²S interface timing – MI²S interface 1 and 2 (primary and secondary MI²S) (cont.)

Parameter		Min	Typ	Max	Unit
T	Clock period	40.69	–	–	ns
t(HC)	Clock high	0.4 × T	–	0.6 × T	ns
t(LC)	Clock low	0.4 × T	–	0.6 × T	ns
t(sr)	SD and WS input setup time	8.14	–	–	ns
t(hr)	SD and WS input hold time	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	6.10	ns
t(htr)	SD and WS output hold time	–	–	–	ns

NOTE I²S slave support of 24.576 MHz is available only with I²S1.

3.10.4 Digital microphone PDM interface

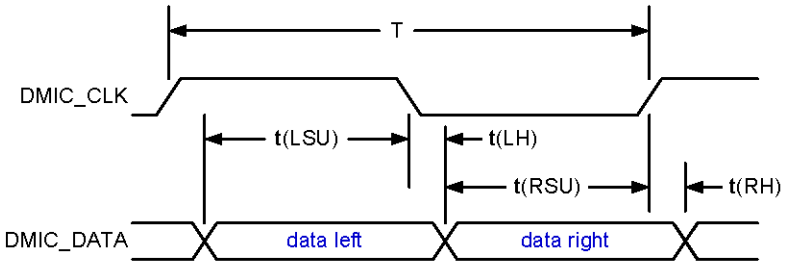


Figure 3-7 Digital microphone PDM interface timing

Table 3-22 Digital microphone timing

Parameter		Comments	Min	Typ	Max	Unit
T	DMIC clock period	–	163	–	1666	ns
t(LSU)	Data left setup time to clock falling edge	–	5	–	–	ns
t(LH)	Data left hold time to clock falling edge	–	0	–	–	ns
t(RSU)	Data right setup time to clock rising edge	–	5	–	–	ns
t(RH)	Data right hold time to clock falling edge	–	0	–	–	ns

3.10.5 SoundWire

QRB2210 SoundWire PHY timing parameters, as specified in the following table, are compliant to clock and data specifications, as specified in the MIPI Alliance Specification for SoundWire Version 0.8, Revision 04. See the following figures.

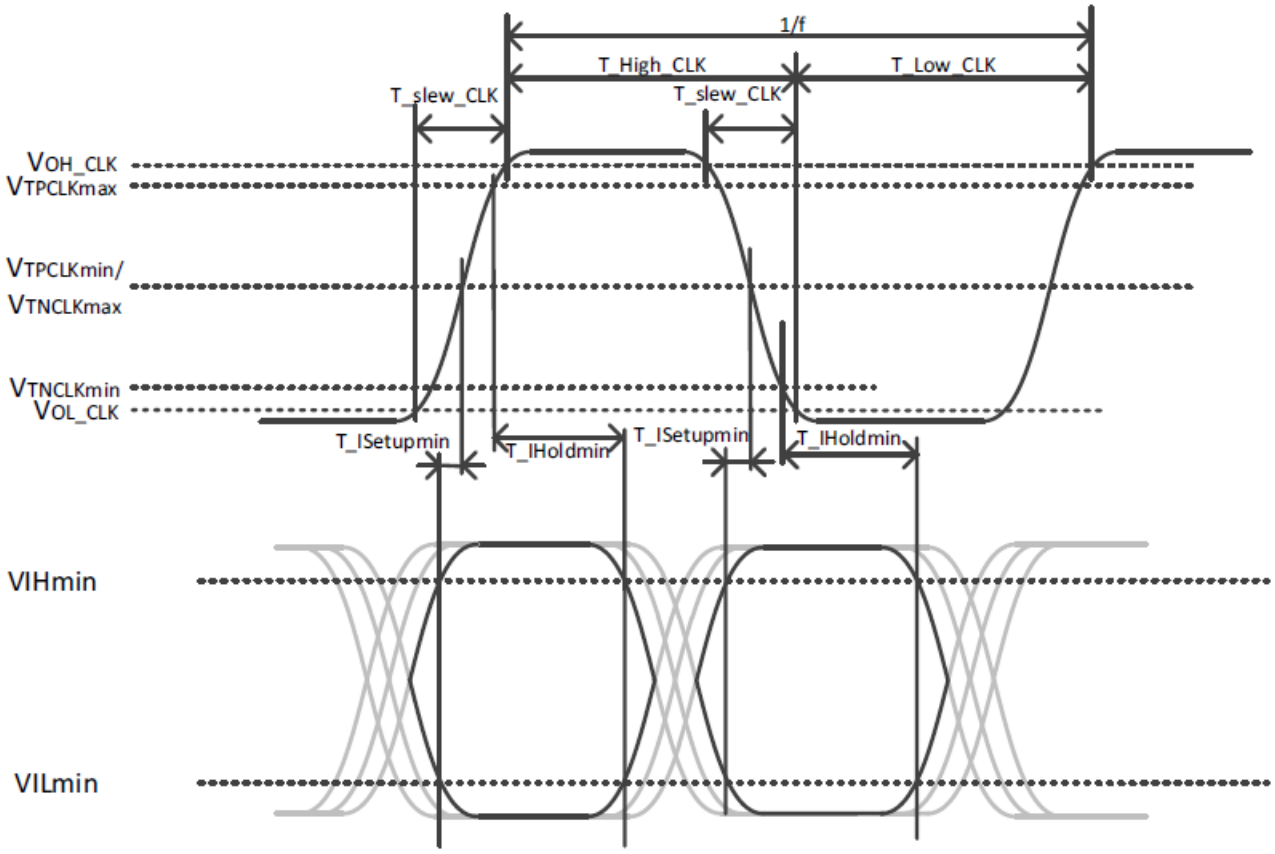


Figure 3-8 PHY timing – clock output/input and data input

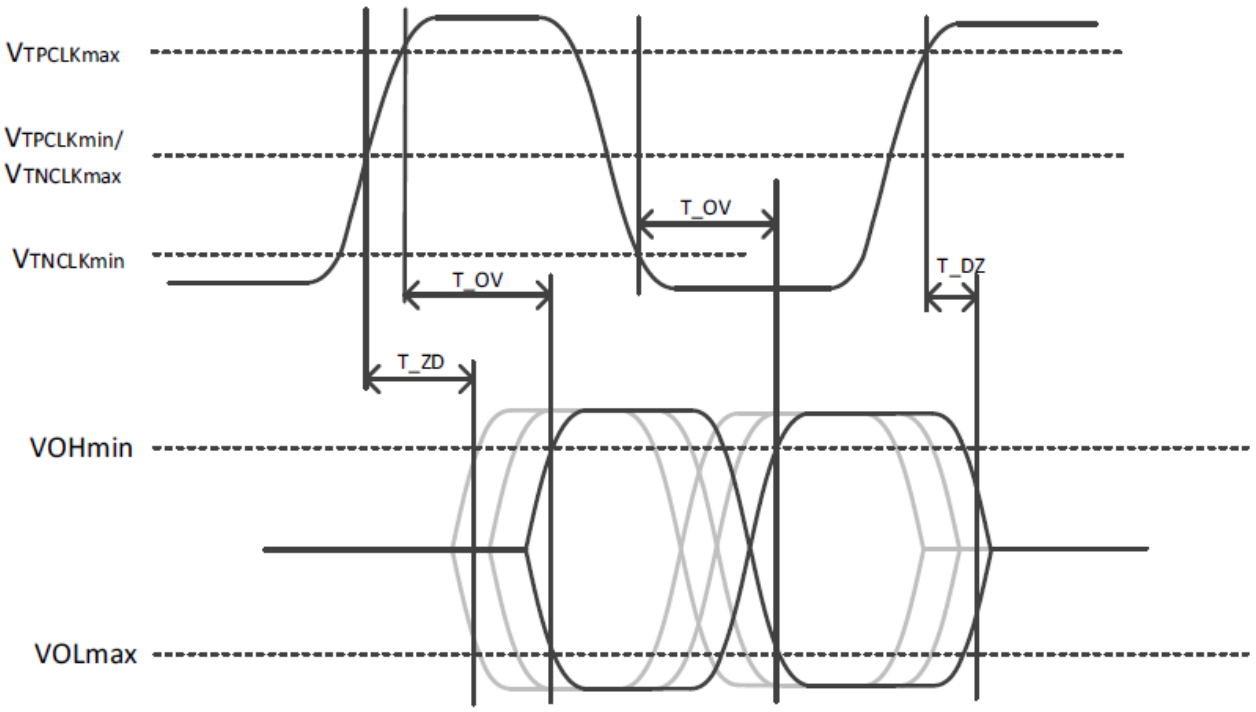


Figure 3-9 PHY timing – clock output and data output

Table 3-23 PHY timing parameters (1.8 V systems)

Name	Description	Min	Max	Unit
f_Clock_small_1V8	Frequency of clock signal in small systems	–	12.288	kHz
t_High_Clock_small_1V8	Duration of high half-period on clock output signal in small systems	35.3	–	ns
t_Low_Clock_small_1V8	Duration of low half-period on clock output signal in small systems	35.3	–	ns
t_DZ_Data_1V8	Time to disable data output signal after positive or negative edge on clock input signal	–	4	ns
t_ZD_Data_1V8	Time to enable data output signal after positive or negative edge on clock input signal	7.9	–	ns
t_OV_Data_small_1V8	Time to valid data output signal after positive or negative edge on clock input signal in small systems	–	27.6	%
t_OH_Data_1V8	Time for data output signal to remain enabled and valid after first becoming valid	6.7	–	ns
t_ISetup_min_Data_1V8	Input setup time	–	0	ns
t_IHold_min_Data_1V8	Input hold time	–	4	ns
DC_Out_Clock	Duty cycle generated at clock output signal calculated from t_Low_Clock/(t_Low_Clock + t_ High_Clock)	46% of the SWR CLK	54% of the SWR CLK	ns

3.10.6 Touchscreen connections

Touchscreen panels are supported using I^2C buses (Section 3.10.7) and GPIOs configured as discrete digital inputs (Section 3.6).

3.10.7 I²C interface

Table 3-24 Supported I²C standards and exceptions

Applicable standard	Feature exceptions
I²C Specification, version 3.0	HS mode, slave mode, and 10-bit addressing are not supported.

3.10.8 I3C interface

Table 3-25 Supported I3C standards and exceptions

Applicable standard	Feature exceptions
I3C Specification, version 1.0	None

3.10.9 Serial peripheral interface

The QRB2210 supports SPI as a master only. Only six out of 10 QUP ports can be configured as an SPI master.

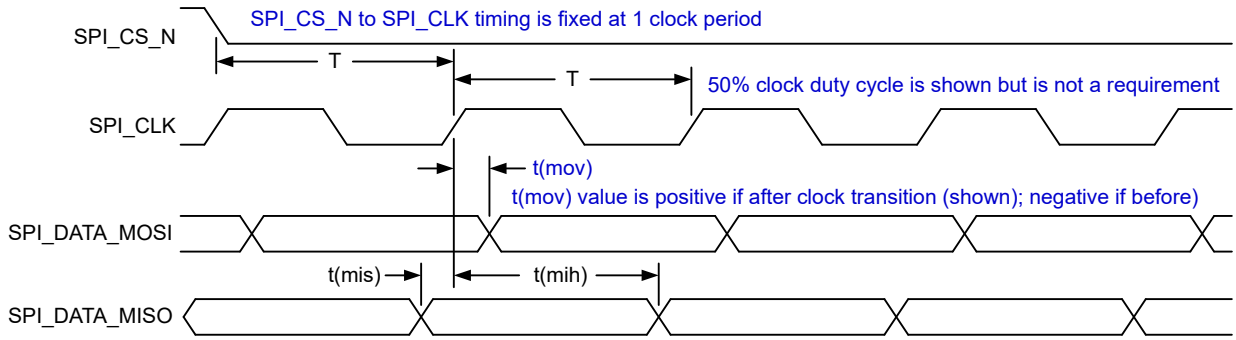


Figure 3-10 SPI master timing diagram

Table 3-26 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [a]	50 MHz maximum	20	–	–	ns
t(ch)	Clock high	9	–	–	ns
t(cl)	Clock low	9	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns

[a] The minimum clock period includes 1% jitter of maximum frequency.

3.11 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.11.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.11.1.1 19.2 MHz CXO input

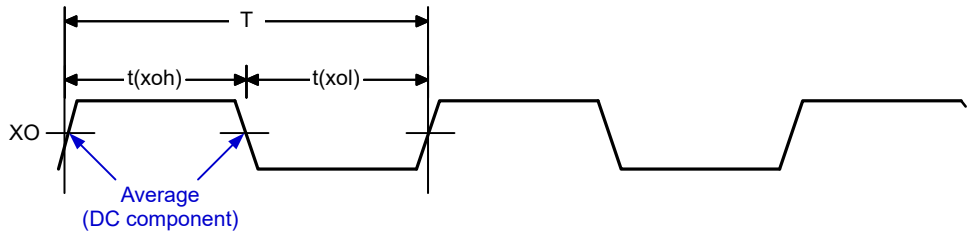


Figure 3-11 XO timing parameters

Table 3-27 XO timing parameters

Parameter		Comments [a]	Min	Typ	Max	Unit
t(xoh)	XO logic high	–	22.6	–	29.5	ns
t(xol)	XO logic low	–	22.6	–	29.5	ns
T	XO clock period	–	–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used	–	19.2	–	MHz

[a] See the *GPS Quality, 19.2 MHz 2520 Package Size, Crystal, and TH + Xtal Mini-Specification (80-V9690-24)* document for more details.

3.11.1.2 Sleep clock

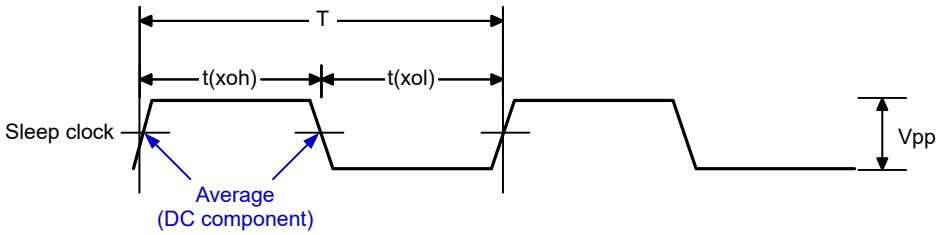


Figure 3-12 Sleep clock timing parameters

Table 3-28 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high	–	4.58	–	25.94	µs
t(xol)	Sleep-clock logic low	–	4.58	–	25.94	µs
T	Sleep-clock period	–	–	30.518	–	µs

Table 3-28 Sleep-clock timing parameters (cont.)

Parameter		Comments	Min	Typ	Max	Unit
F	Sleep-clock frequency	F= 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage	–	–	1.8	–	V

3.11.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.6.

3.11.3 JTAG

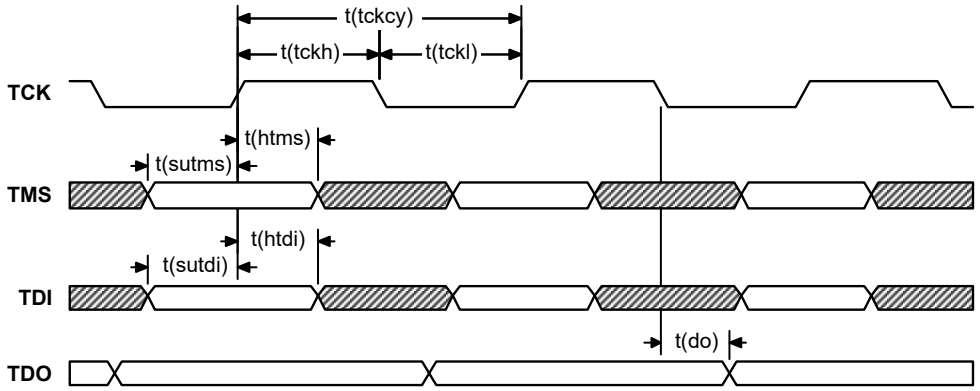


Figure 3-13 JTAG interface timing diagram

Table 3-29 JTAG interface timing characteristics

Parameter		Min	Typ	Max	Unit
t(tckcy)	TCK period	50	–	–	ns
t(tckh)	TCK pulse width high	20	–	–	ns
t(tckl)	TCK pulse width low	20	–	–	ns
t(sutms)	TMS input setup time	5	–	–	ns
t(htms)	TMS input hold time	20	–	–	ns
t(sutdi)	TDI input setup time	5	–	–	ns
t(htdi)	TDI input hold time	20	–	–	ns
t(do)	TDO data output delay	–	–	15	ns

3.12 Power management interfaces

The digital I/Os must meet the logic-level requirements specified in Section 3.6. The Rx and Tx baseband interfaces are proprietary, and therefore are not specified.

3.12.1 System power management interface (SPMI)

Table 3-30 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

4 Mechanical information

This topic provides IC mechanical information including dimensions, markings, ordering information, and thermal characteristics.

4.1 Device physical dimensions

The QRB2210 device is available in the NSP752, a 12 mm × 12.4 mm non-PoP package. The package includes many ground pins for improved electrical grounding, mechanical strength, and thermal continuity. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the package outline drawing is shown in the following figure.

NOTE Click *Package Outline Drawing, NSP752, 12.0 mm × 12.4 mm × 0.91 mm, M530, S143 (NT90-PR195-1)* to download the drawing.

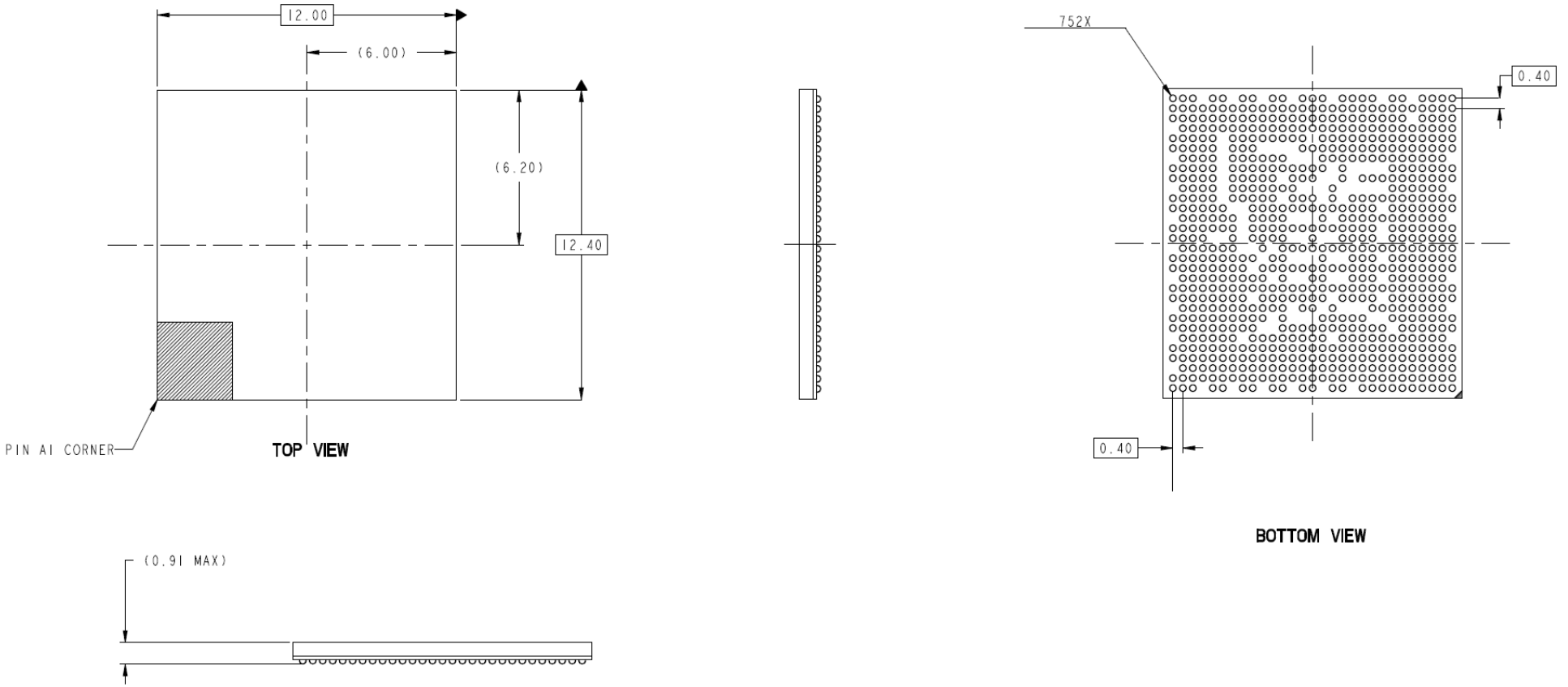


Figure 4-1 NSP752 (12.0 × 12.4 × 0.91 mm) outline drawing

4.2 Part marking

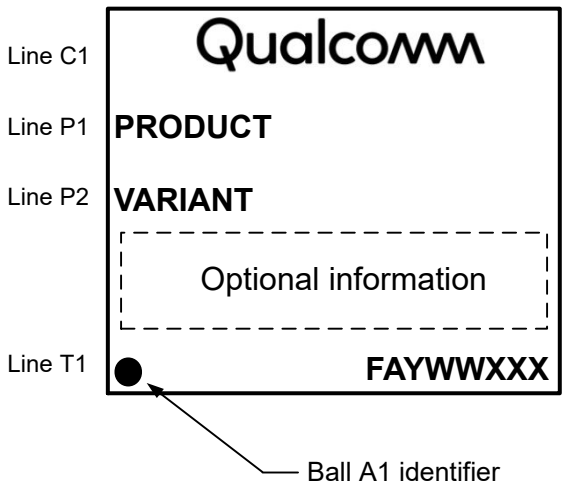


Figure 4-2 QRB2210 device marking (top view, not to scale)

Table 4-1 QRB2210 device marking line definitions

Line	Marking	Description
C1	Qualcomm	Qualcomm name
P1	PRODUCT	QTI product name ▪ QRB2210
P2	VARIANT	Device variant information ▪ See Table 4-3 for the assigned values
	Blank or random	Optional information
T1	FAYWWXXX	F = supply source code ▪ F = H (GLOBALFOUNDRIES) ▪ F = J (Samsung) A = assembly site code ▪ A = E (ASE, Taiwan) ▪ A = U (Amkor, China) ▪ A = K (SPIL, Taiwan) Y = single/last digit of year WW = two-digit work week of year specified by Y XXX = traceability number
	•	Ball A1 indicator

4.3 Device ordering information

The Oracle short description is used to order QTI products, and is present on both the customer label and this document. The short description includes the product name, configuration code, package type, product revision code, source code, and feature code/program ID of the part.

This device can be ordered using the identification code shown in the following table.

Table 4-2 Device identification code

Device ID code	AAA-AAAA	-P	-TTTTTT	NNNN	A	+FF	-EE	-RR	-S	-BB or -PID [a]
Symbol definition	**Product name**	**Configuration code**	**Package type**	**Number of pins**	**Package variable**	**Additional package information**	**Shipping package**	**Product revision**	**Source code**	**Feature code**
Example	QRB-2210	-0	-NSP	752			-TR	-00	-0	

[a] The feature code (BB) and the program ID (PID) are mutually exclusive. A product may have one of them or none of them, but it will never have both. If there is no feature code/program ID, this field is blank, and the Oracle short description ends after the source configuration code (S).

For example: QRB-2210-0-NSP752-TR-00-0

NOTE The shipping package is either TR (tape and reel) or MT (matrix tray).

4.4 Device identification for each sample type

Device identification details for all samples available to date are summarized in the following table.

Table 4-3 Device identification details

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code [a]	Hardware revision number (JTAG_ID - see Table 4-5)	FEATURE_ID (see Table 4-5) [b]	Hardware version	Source configuration code (S) [c]	Comments	Sample date
QRB2210	ES	000	0x0 01C8 0E1	0x0	v1.0	0	NSP752, CPU 2.0, GPU 845, 13 MP + 13 MP, LP4 at 1866 MHz, LP3, NAVIC, SVA, S_CAM, 1080P30 encode/decode, IoT, RB1, Samsung/ GLOBALFOUNDRIES	09/13/2021
QRB2210	CS	000 CS date codes are as follows: ■ ASE = 207 ■ Amkor = 207 ■ SPIL = 207	0x0 01C8 0E1	0x0	v1.0	0	NSP752, CPU 2.0, GPU 845, 13 MP + 13 MP, LP4 at 1866 MHz, LP3, NAVIC, SVA, S_CAM, 1080P30 encode/decode, IoT, RB1, Samsung/ GLOBALFOUNDRIES	05/31/2022

[a] BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the comments column.
[b] The FEATURE_ID combined with the hardware revision number (JTAG_ID) defines unique product variants. This information is shown for situations where other device identification information (such as device marking information) is not easily accessible.
[c] S is the source configuration code that identifies all of the qualified die fabrication-source combinations available when the particular sample type was shipped. The S values are defined in Table 4-4.

Table 4-4 Source configuration code

S value	Die	F value = H	F value = J	A value = E	A value = U	A value = K
0	Digital	GLOBALFOUNDRIES	Samsung	ASE, Taiwan	Amkor, China	SPIL, Taiwan
Other columns and rows will be added in future revisions of this document, if needed.						

The 28-bit QFPROM JTAG register is summarized in the following table:

Table 4-5 QFPROM_CORR_JTAG_ID_LSB register

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants (see Table 4-3).
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the hardware revision number (see Table 4-3).

The device identification register allows the user to determine the device's manufacturer, part number, and version via the test access port (TAP). The 32-bit device identification register is read through the JTAG interface and is summarized in the following table.

Table 4-6 Device identification register

Bit location	Description	Value [a]
bits [31:28]	Version data (may change with sample type)	0x0
bits [27:12]	Part number (changes with sample type)	01C8
bits [11:1]	Manufacturer identity code (administered by JEDEC)	070 (QTI code)
bit [0]	Device identification register start bit	Always = 1

[a] The hardware revision numbers for all sample types are provided in Table 4-3.

4.5 Thermal characteristics

Rather than providing thermal resistance values Θ_{JC} and Θ_{JA}, validated thermal package models are provided through the Qualcomm website. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE Click *QRB2210 Package Thermal Model Icepak (HS11-30843-5HW)* and *QRB2210 Package Thermal Model FloTHERM (HS11-30843-6HW)* to download the package thermal models from the Qualcomm website.

5 Carrier, storage, and handling

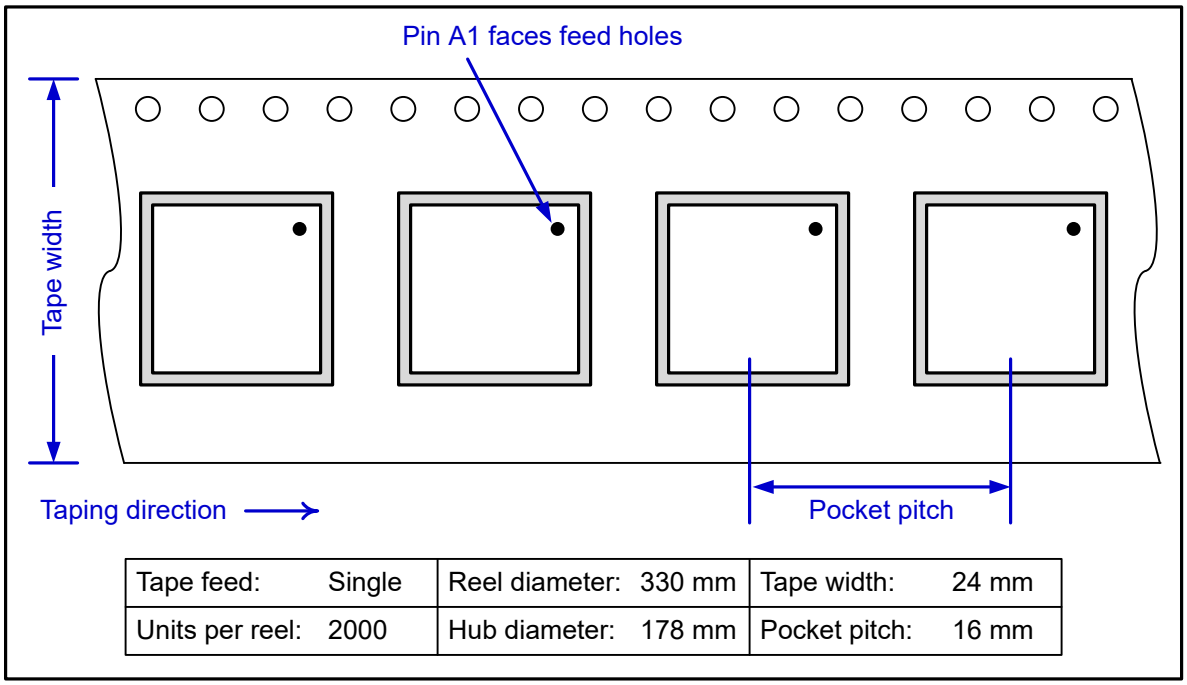
This topic discusses shipping, storage, and handling of this chipset.

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

The following figure shows a simplified sketch of the QRB2210 tape carrier, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	178 mm	Pocket pitch:	16 mm

Figure 5-1 Carrier tape drawing with part orientation

The following figure shows the tape-handling recommendations.

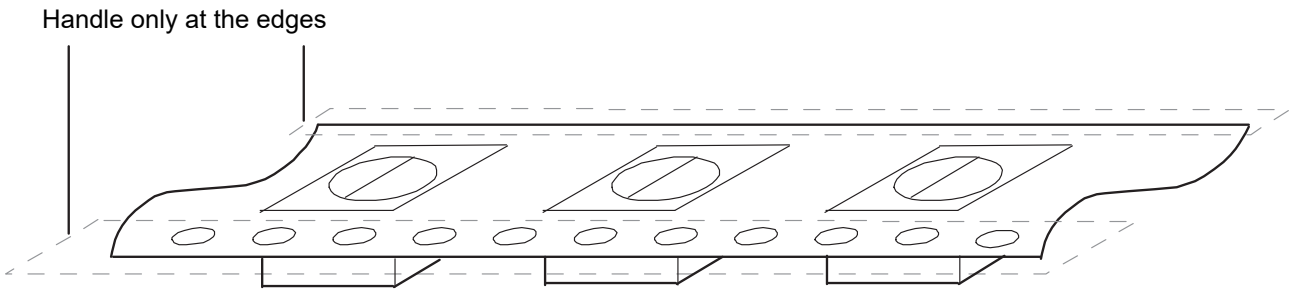


Figure 5-2 Tape handling

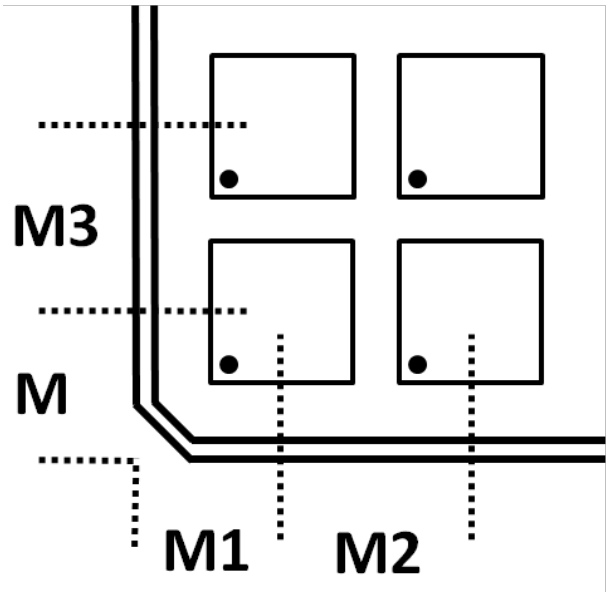
5.1.2 Matrix tray information

All QTI matrix tray carriers confirm to JEDEC standards.

The device pin 1 is oriented to the chamfered corner of the matrix tray.

Each tray of the QRB2210 contains up to 160 devices. Production orders of the QRB2210 that are shipped in matrix tray carriers will be in [10 + 1] tray stacks of [1600] units. The stacking configuration and quantity for sample orders will vary.

The following figure shows the matrix-tray key attributes and dimensions.



Key dimensions	
Array	8 × 20 (160)
M	11.60 mm
M1	11.20 mm
M2	15.40 mm
M3	16.00 mm

Figure 5-3 Matrix-tray key attributes and dimensions

5.2 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in the following table.

Table 5-1 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; **QRB2210 rating**
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The QRB2210 devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

5.3 Storage

5.3.1 Bagged storage conditions

QRB2210 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. See *IC Products Packing Method (80-VK055-1)* for the expected shelf life.

5.3.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB.

5.3.3 Handling

Tape handling was described in Section 5.3.1. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.3.1 Baking

It is not necessary to bake the QRB2210 if the conditions specified in Section 5.3.1 and Section 5.3.2 have **not been exceeded**.

It is necessary to bake the QRB2210 if any condition specified in Section 5.3.1 or Section 5.3.2 has been exceeded. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see the *IC Products Packing Method (80-VK055-1)* document for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.3.4 Bar code label and packing for shipment

See the *IC Products Packing Method (80-VK055-1)* document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

This topic provides specifications for mounting the QRB2210 onto PCBs

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, see the *SMT Assembly Guidelines (SM80-P0982-1)*.

6.3 Daisy chain components

For daisy chain part information, contact the Qualcomm Sales team for support.

7 Part reliability

This topic provides the reliability data, including a definition of the qualification samples and a summary of qualification test results.

7.1 Reliability qualifications summary

The table below lists the QRB2210 reliability evaluation report for NSP752 device where, foundry source is Samsung.

Table 7-1 Silicon reliability results – Samsung

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108-A Total samples from more than three different wafer lots	91	Pass DPPM < 1000 See note below the table
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A Total samples from more than three different wafer lots	91	Pass FIT < 50 See note below the table
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from more than three different wafer lots)	91	> 20 See note below the table
ESD – Human-body model (HBM) rating JESD22-A114-F Target 1000 V Total samples from one wafer lot	24	Pass ± 1000 V
ESD – Charge-device model (CDM) rating JESD22-C101-D Target 250 V Total samples from one wafer lot	3	Pass ± 250 V
Latch-up (I-test): EIA/JESD78C Trigger current: ±100 mA; temperature: 85°C Total samples from one wafer lot	3	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78C Trigger voltage: stress at 1.5 × V_{ddmax} per device specification; temperature: 85°C Total samples from one wafer lot	3	Pass
NOTE Data is leveraged from other previously qualified PSP packages that are similar to this configuration.		

Table 7-2 Package reliability results - Samsung

Tests, standards, and conditions	SPIL, Taiwan Sample size	ASE, Taiwan Sample size	Amkor, China Sample size	Result
Moisture resistance test (MRT): J-STD-020-C Reflow at 260 +0/-5 °C, MSL3 Total samples from three different assembly lots	582	582	582	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** JESD22-A113-F MSL3, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	231	231	231	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hours duration Preconditioning: JESD22-A113-F MSL3, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	231	231	231	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hour duration or 110°C/85% RH and 264-hours duration Preconditioning: JESD22-A113-F MSL3, reflow temperature: 260°C +0/-5°C	120	120	120	Pass
High-Temperature Storage Life: JESD22-A103-C Temperature 150°C, 500 hours, 1000 hours Total samples from three different assembly lots	231	231	231	Pass
Flammability UL-STD-94 Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, if they are mounted on materials rated V-1 or better. Most PWBs onto which our ICs mounted are rated V-0 (better than V-1)	N/A	N/A	N/A	N/A
Physical dimensions: JESD22-B100-B Case outline drawing: QTI internal document Total samples from three different assembly lots	30	30	30	Pass
Solder ball shear JESD22-B117A Total samples from three different assembly lots	15	15	15	Pass
NOTE Data is leveraged from other previously qualified PSP packages that are similar to this configuration.				

The table below lists the QRB2210 reliability evaluation report for NSP752 device where, foundry source is GLOBALFOUNDRIES.

Table 7-3 Silicon reliability results – GLOBALFOUNDRIES

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108-A Total samples from more than three different wafer lots	117	Pass DPPM < 1000 See note below the table
HTOL in FIT (λ) failure in billion device hoursHTOL: JESD22-A108-A Total samples from more than three different wafer lots	117	Pass FIT < 50 See note below the table
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from more than three different wafer lots)	117	> 20 See note below the table
ESD – Human-body model (HBM) rating JESD22-A114-F Target 1000 V (Total samples from one wafer lot)	24	Pass ± 1000 V
ESD – Charge-device model (CDM) rating JESD22-C101-D Target 250 V (Total samples from one wafer lot)	3	Pass ± 250V
Latch-up (I-test): EIA/JESD78C Trigger current: ±100 mA; temperature: 85°C (Total samples from one wafer lot)	3	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78C Trigger voltage: stress at 1.5 × Vdd max per device specification; temperature: 85°C (Total samples from one wafer lot)	3	Pass
NOTE Data is leveraged from other previously qualified PSP packages that are similar to this configuration.		

Table 7-4 Package reliability results – GLOBALFOUNDRIES

Tests, standards, and conditions	SPIL, Taiwan Sample size	ASE, Taiwan Sample size	Amkor, China Sample size	Result
Moisture resistance test (MRT): J-STD-020-C Reflow at 260 +0/-5 °C, MSL3 Total samples from three different assembly lots	582	582	582	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** JESD22-A113-F MSL3, reflow temperature: 260°C+0/-5°C	231	231	231	Pass

Table 7-4 Package reliability results – GLOBALFOUNDRIES (cont.)

Tests, standards, and conditions	SPIL, Taiwan Sample size	ASE, Taiwan Sample size	Amkor, China Sample size	Result
Total samples from three different assembly lots				
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hours duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	231	231	231	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96-hour duration or 110°C/85% RH and 264-hours duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C +0/-5°C	120	120	120	Pass
High-Temperature Storage Life: JESD22-A103-C Temperature 150°C, 500 hours, 1000 hours Total samples from three different assembly lots	231	231	231	Pass
Flammability UL-STD-94 Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, if they are mounted on materials rated V-1 or better. Most PWBs onto which our ICs mounted are rated V-0 (better than V-1)	N/A	N/A	N/A	N/A
Physical dimensions: JESD22-B100-B Case outline drawing: QTI internal document Total samples from three different assembly lots	30	30	30	Pass
Solder ball shear JESD22-B117A Total samples from three different assembly lots	15	15	15	Pass
NOTE Since assembly process is the same for Samsung and GLOBALFOUNDRIES, data provided here is based on the qualification test results from Samsung.				

7.2 Qualification sample description

Table 7-5 Device characteristics

Category	Definition
Device name	QRB2210
Package type	NSP
Package body size	12.0 × 12.4 × 0.91 mm
Ball count	752
Ball composition	SAC125/Ni
Fab process	11 LPP

Table 7-5 Device characteristics (cont.)

Category	Definition
Fab sites	Samsung, GLOBALFOUNDRIES
Assembly sites	■ ASE, Taiwan ■ Amkor, China ■ SPIL, Taiwan
Solder ball pitch	0.4 mm

8 Samples and known issues

This topic discusses the issues, regardless of the sample type (or types) on which they occur.

8.1 Sample testing

See Table 4-3 for device identification details for all available samples.

8.1.1 Engineering samples (ES)

These devices undergo limited testing and sometimes have significant feature limitations. They are suitable to assist with PCB development, to conduct board-level electrical evaluation tests, and to explore manufacturing considerations. Engineering samples should not be used for product-level qualification.

8.1.2 Commercial samples (CS)

These devices undergo full production-level testing, and meet the specifications and features described in the data sheet, except as otherwise noted in this document. They have passed device level qualification. Commercial samples are suitable for performance testing, and also for product-level production and qualification.

8.2 Compatible software releases

Each sample type is for use with a particular QRB2210 software version (or later). Sample types are not expected to be compatible with AMSS software releases that occurred earlier than that particular version. The following table identifies the software compatibility of each sample type.

Table 8-1 Software compatibility for each sample type (PRR value)

Variant	PRR	Compatible software	Comments
QRB2210	000	QRB2210.LE.1.0-00007-STD.PROD-1	ES software release
QRB2210	000	QRB2210.LE.1.0-00016-STD.PROD-3	CS software release

8.3 Known issues

There are no known issues for QRB2210.

9 Revision history

The following table lists the technical content changes for all revisions.

Revision	Date	Description
AE	October 2025	■ Global update: Removed UIM and GNSS support ■ Added the following tables: □ Table 4-5 *QFPROM_CORR_JTAG_ID_LSB register* □ Table 4-6 *Device identification register* ■ Chapter 8 *Samples and known issues*: Added this chapter
AD	August 2022	■ Global update: □ Removed GNSS and WGR7640 □ Updated 752 NSP to NSP752 ■ Cover page: Updated QRB2210 high-level block diagram ■ Figure 1-1 *QRB2210 functional block diagram*: Updated the figure ■ Section 1.2.1 *Air interface features*: Removed table position location and navigation summary ■ Section 2.2.1 *Pin map*: Removed to be released ■ Table 2-2 *Pin descriptions – general pins*: Updated note ■ Table 3-3 *Operating conditions*: Updated footnote
AC	June 2022	■ Table 4-4 *Device identification details*: Updated with CS details ■ Table 4-5 *Source configuration code*: Added Assembly sites ■ Section 4.5 *Thermal characteristics*: Updated this topic
AB	November 2021	Table 4-4 *Device identification details*: Updated the ES sample date
AA	August 2021	Initial release

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