EFR32MG1 Mighty Gecko ZigBee® & Thread SoC Family Data Sheet

The Mighty Gecko ZigBee & Thread family of SoCs is part of the Wireless Gecko portfolio. Mighty Gecko SoCs are ideal for enabling energy-friendly ZigBee & Thread networking for IoT devices.

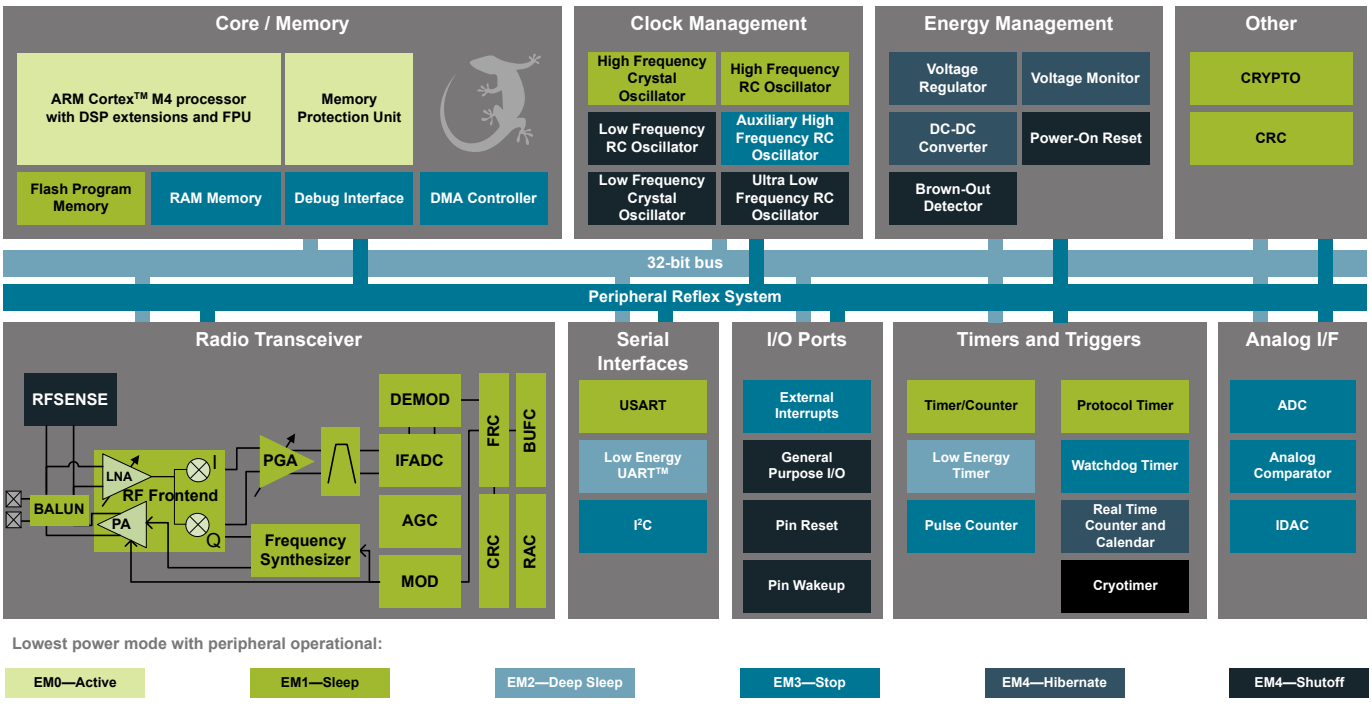
The single-die solution provides industry-leading energy efficiency, ultra-fast wakeup times, a scalable power amplifier, an integrated balun and no-compromise MCU features.

Mighty Gecko applications include:

- Connected Home
- Lighting
- Health and Wellness
- Metering
- Home and Building Automation and Security

KEY FEATURES

- 32-bit ARM® Cortex®-M4 core with 40 MHz maximum operating frequency
- Scalable Memory and Radio configuration options available in several footprint compatible QFN packages
- 12-channel Peripheral Reflex System enabling autonomous interaction of MCU peripherals
- Autonomous Hardware Crypto Accelerator and Random Number Generator
- Integrated 2.4 GHz balun and PA with up to 19.5 dBm transmit power
- Integrated DC-DC with RF noise mitigation



1. Feature List

The EFR32MG1 highlighted features are listed below.

- **Low Power Wireless System-on-Chip**.
  - High Performance 32-bit 40 MHz ARM Cortex®-M4 with DSP instruction and floating-point unit for efficient signal processing
  - Up to 256 kB flash program memory
  - Up to 32 kB RAM data memory
  - 2.4 GHz radio operation
  - TX power up to 19.5 dBm
- **Low Energy Consumption**
  - 8.7 mA RX current at 2.4 GHz (1 Mbps GFSK)
  - 9.8 mA RX current at 2.4 GHz (250 kbps O-QPSK DSSS)
  - 8.8 mA TX current @ 0 dBm output power at 2.4 GHz
  - 63 µA/MHz in Active Mode (EM0)
  - 1.4 µA EM2 DeepSleep current (full RAM retention and RTCC running from LFXO)
  - 1.1 µA EM3 Stop current (State/RAM retention)
  - Wake on Radio with signal strength detection, preamble pattern detection, frame detection and timeout
- **High Receiver Performance**
  - -94 dBm sensitivity @ 1 Mbit/s GFSK
  - -101 dBm sensitivity @ 250 kbps O-QPSK DSSS
- **Supported Modulation Format**
  - 2-FSK / 4-FSK with fully configurable shaping
  - Shaped OQPSK / (G)MSK
- **Supported Protocols:**
  - Bluetooth Smart
  - ZigBee®
  - Thread
  - 2.4 GHz Proprietary Protocols
- **Support for Internet Security**
  - General Purpose CRC
  - Random Number Generator
  - Hardware Cryptographic Acceleration for AES 128/256, SHA-1, SHA-2 (SHA-224 and SHA-256) and ECC
- **Wide selection of MCU peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - 2× Analog Comparator (ACMP)
  - Digital to Analog Current Converter (IDAC)
  - Up to 31 pins connected to analog channels (APORT) shared between Analog Comparators, ADC, and IDAC
  - Up to 31 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 2×16-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels
  - 32-bit Real Time Counter and Calendar
  - 16-bit Low Energy Timer for waveform generation
  - 32-bit Ultra Low Energy Timer/Counter for periodic wake-up from any Energy Mode
  - 16-bit Pulse Counter with asynchronous operation
  - Watchdog Timer with dedicated RC oscillator @ 50nA
  - 2×Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - Low Energy UART (LEUART™)
  - I^2C interface with SMBus support and address recognition in EM3 Stop
- **Wide Operating Range**
  - 1.85 V to 3.8 V single power supply
  - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
  - -40 °C to 85 °C
- **QFN32 5x5 mm Package**
- **QFN48 7x7 mm Package**

2. Ordering Information

Ordering Code	Protocol Stack	Frequency Band	Max TX Power (dBm)	Encryption	Flash (KB)	RAM (KB)	GPIO	Package
EFR32MG1P232F256GM48-B0*	• Bluetooth Smart • ZigBee • Thread • ZigBee RC • Proprietary	2.4 GHz	19.5	Full	256	32	31	QFN48
EFR32MG1P232F256GM32-B0*	• Bluetooth Smart • ZigBee • Thread • ZigBee RC • Proprietary	2.4 GHz	19.5	Full	256	32	16	QFN32
EFR32MG1P132F256GM48-B0*	• Bluetooth Smart • ZigBee • Thread • ZigBee RC • Proprietary	2.4 GHz	16.5	Full	256	32	31	QFN48
EFR32MG1P132F256GM32-B0*	• Bluetooth Smart • ZigBee • Thread • ZigBee RC • Proprietary	2.4 GHz	16.5	Full	256	32	16	QFN32
EFR32MG1B232F256GM48-B0*	• ZigBee • Thread • ZigBee RC	2.4 GHz	19.5	Full	256	32	31	QFN48
EFR32MG1B232F256GM32-B0*	• ZigBee • Thread • ZigBee RC	2.4 GHz	19.5	Full	256	32	16	QFN32
EFR32MG1B132F256GM48-B0*	• ZigBee • Thread • ZigBee RC	2.4 GHz	16.5	Full	256	32	31	QFN48
EFR32MG1B132F256GM32-B0*	• ZigBee • Thread • ZigBee RC	2.4 GHz	16.5	Full	256	32	16	QFN32
EFR32MG1V132F256GM48-B0*	• ZigBee • Thread • ZigBee RC	2.4 GHz	8	AES only	256	32	31	QFN48
EFR32MG1V132F256GM32-B0*	• ZigBee • Thread • ZigBee RC	2.4 GHz	8	AES only	256	32	16	QFN32
* Engineering Samples								

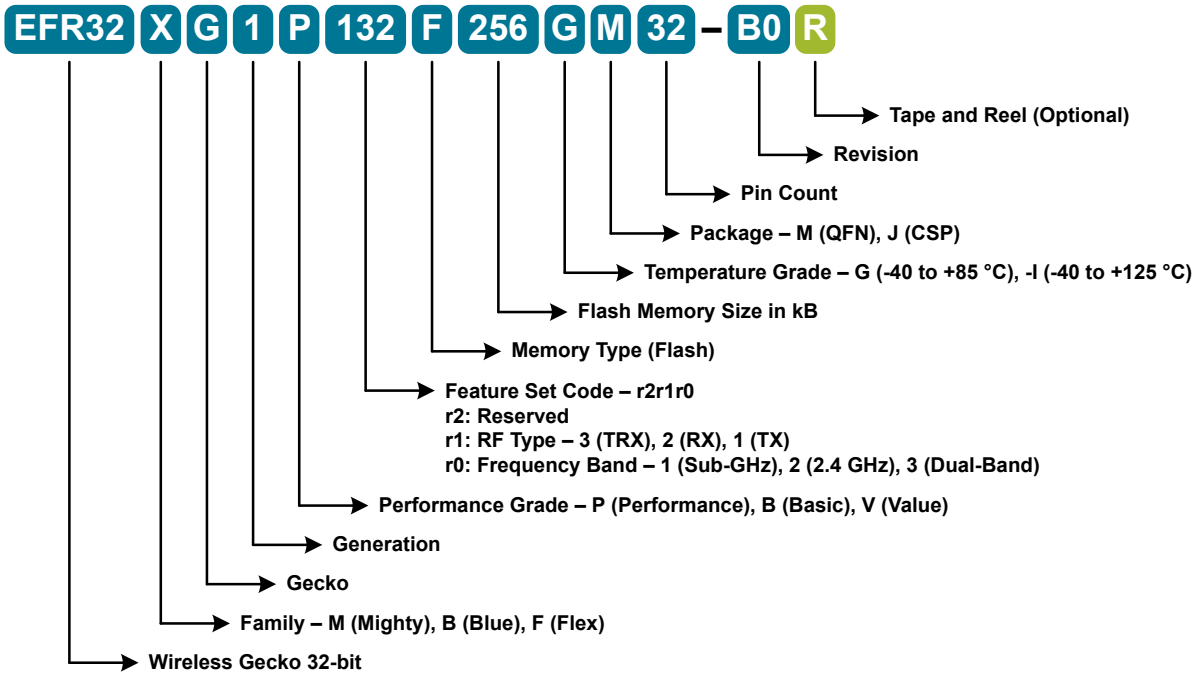


Figure 2.1. OPN Decoder

3. System Overview

3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a highly integrated radio transceiver. The devices are well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the EFR32 Reference Manual.

A block diagram of the EFR32MG1 family is shown in Figure 3.1 Detailed EFR32MG1 Block Diagram on page 4. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

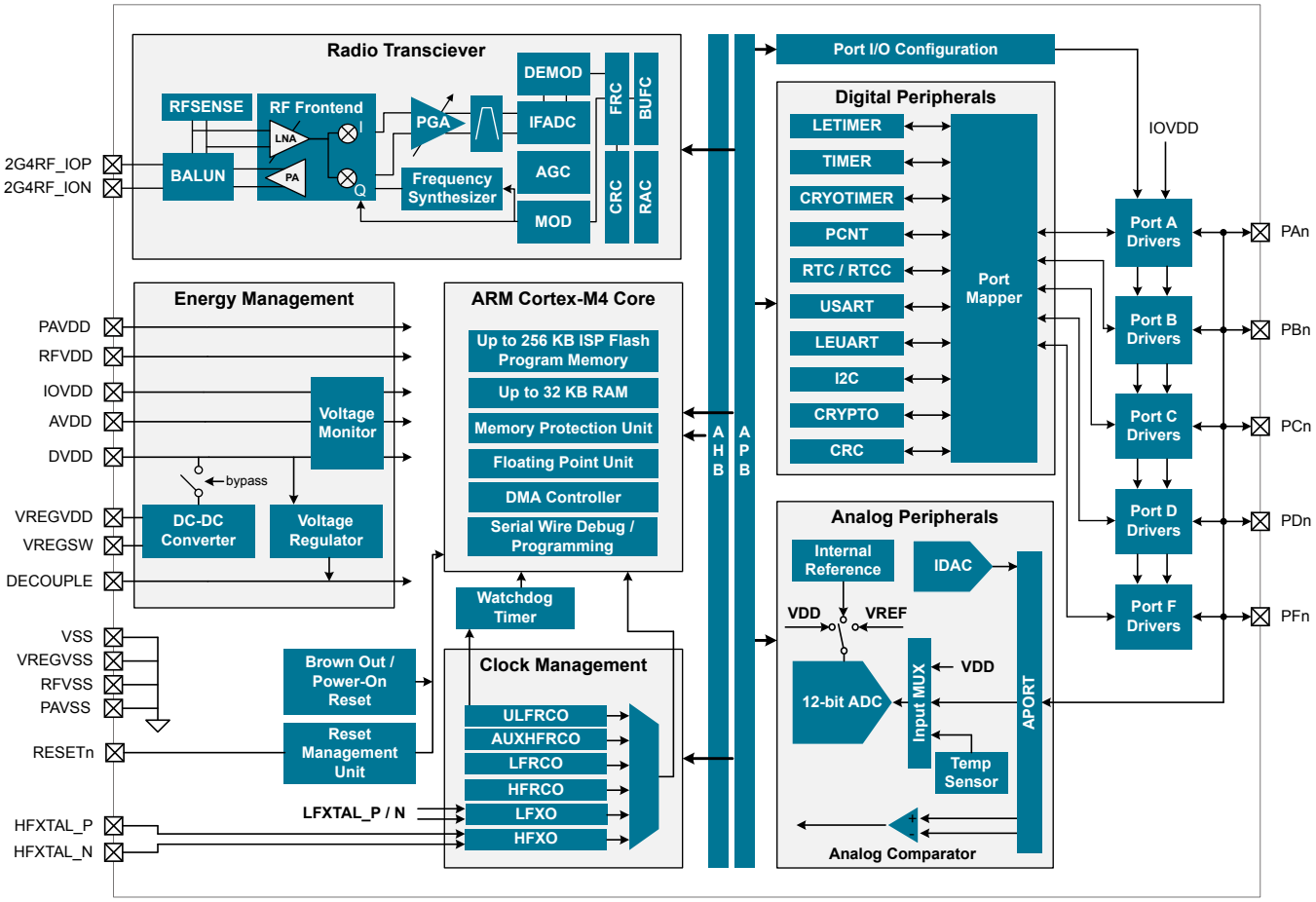


Figure 3.1. Detailed EFR32MG1 Block Diagram

3.2 Radio

The Mighty Gecko family features a highly configurable radio transceiver supporting a wide range of wireless protocols.

3.2.1 Antenna Interface

The 2.4 GHz antenna interface consists of two pins (2G4RF_IOP and 2G4RF_ION) that interface directly to the on-chip BALUN. The 2G4RF_ION pin should be grounded externally.

The external components and power supply connections for the antenna interface typical applications are shown in the RF Matching Networks section.

3.2.2 Fractional-N Frequency Synthesizer

The EFR32MG1 contains a high performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency used by the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance combined with frequency resolution better than 100 Hz, with low energy consumption. The synthesizer has fast frequency settling which allows very short receiver and transmitter wake up times to optimize system energy consumption.

3.2.3 Receiver Architecture

The EFR32MG1 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer, employing a crystal reference. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. Devices are production-calibrated to improve image rejection performance.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

The EFR32MG1 features integrated support for antenna diversity to improve link budget, using complementary control outputs to an external switch. Internal configurable hardware controls automatic switching between antennae during RF receive detection operations.

3.2.4 Transmitter Architecture

The EFR32MG1 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32MG1. These algorithms are typically defined by regulatory standards to improve inter-operability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

3.2.5 Wake on Radio

The Wake on Radio feature allows flexible, autonomous RF sensing, qualification, and demodulation without required MCU activity, using a subsystem of the EFR32MG1 including the Radio Controller (RAC), Peripheral Reflex System (PRS), and Low Energy peripherals.

3.2.6 RFSENSE

The RFSENSE module generates a system wakeup interrupt upon detection of wideband RF energy at the antenna interface, providing true RF wakeup capabilities from low energy modes including EM2, EM3 and EM4.

RFSENSE triggers on a relatively strong RF signal and is available in the lowest energy modes, allowing exceptionally low energy consumption. RFSENSE does not demodulate or otherwise qualify the received signal, but software may respond to the wakeup event by enabling normal RF reception.

Various strategies for optimizing power consumption and system response time in presence of false alarms may be employed using available timer peripherals.

3.2.7 Flexible Frame Handling

EFR32MG1 has an extensive and flexible frame handling support for easy implementation of even complex communication protocols. The Frame Controller (FRC) supports all low level and timing critical tasks together with the Radio Controller and Modulator/Demodulator:

- Highly adjustable preamble length
- Up to 2 simultaneous synchronization words, each up to 32 bits and providing separate interrupts
- Frame disassembly and address matching (filtering) to accept or reject frames
- Automatic ACK frame assembly and transmission
- Fully flexible CRC generation and verification:
  - Multiple CRC values can be embedded in a single frame
  - 8, 16, 24 or 32-bit CRC value
  - Configurable CRC bit and byte ordering
- Selectable bit-ordering (least significant or most significant bit first)
- Optional data whitening
- Optional Forward Error Correction (FEC), including convolutional encoding / decoding and block encoding / decoding
- Half rate convolutional encoder and decoder with constraint lengths from 2 to 7 and optional puncturing
- Optional symbol interleaving, typically used in combination with FEC
- Symbol coding, such as Manchester or DSSS, or biphase space encoding using FEC hardware
- UART encoding over air, with start and stop bit insertion / removal
- Test mode support, such as modulated or unmodulated carrier output
- Received frame timestamping

3.2.8 Packet and State Trace

The EFR32MG1 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.9 Data Buffering

The EFR32MG1 features an advanced Radio Buffer Controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 bytes to 4096 bytes. Each buffer can be used for RX, TX or both. The buffer data is located in RAM, enabling zero-copy operations.

3.2.10 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the EFR32MG1. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter and frequency synthesizer
- Detailed frame transmission timing, including optional LBT or CSMA-CA

3.2.11 Random Number Generator

The Frame Controller (FRC) implements a random number generator that uses entropy gathered from noise in the RF receive chain. The data is suitable for use in cryptographic applications.

Output from the random number generator can be used either directly or as a seed or entropy source for software-based random number generator algorithms such as Fortuna.

3.3 Power

The EFR32MG1 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

AVDD and VREGVDD need to be 1.85 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.3.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the dc-dc regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.3.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Patented RF noise mitigation allows operation of the DC-DC converter without degrading sensitivity of radio components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.4 General Purpose Input/Output (GPIO)

EFR32MG1 has up to 31 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFR32MG1. Individual enabling and disabling of clocks to all peripheral modules is perfomed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal and External Oscillators

The EFR32MG1 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 38 to 40 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire debug port with a wide frequency range.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.6.2 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. When receiving frames, the RTCC value can be used for timestamping. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes.

3.6.3 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.6.4 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.6.5 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.6.6 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.7.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.7.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality can be applied by the PRS. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.8 Security Features

3.8.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.8.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFR32 devices support various levels of hardware-accelerated encryption, depending on the part number. The Ordering Information Table specifies whether this part has **full** or **AES-only** crypto support. AES-only devices support AES encryption and decryption with 128- or 256-bit keys. Full crypto support adds ECC over both GF(P) and GF(2^m), SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO is tightly linked to the Radio Buffer Controller (BUFC) enabling fast and efficient autonomous cipher operations on data buffer content. It allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.9 Analog

3.9.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to analog modules ADC, ACMP, and IDAC on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.9.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 MSamples/s. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.4 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The current is programmable between 0.05 µA and 64 µA with several ranges with various step sizes.

3.10 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32MG1. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Up to 256 KB flash program memory
- Up to 32 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller features 8 channels capable of performing memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The EFR32MG1 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

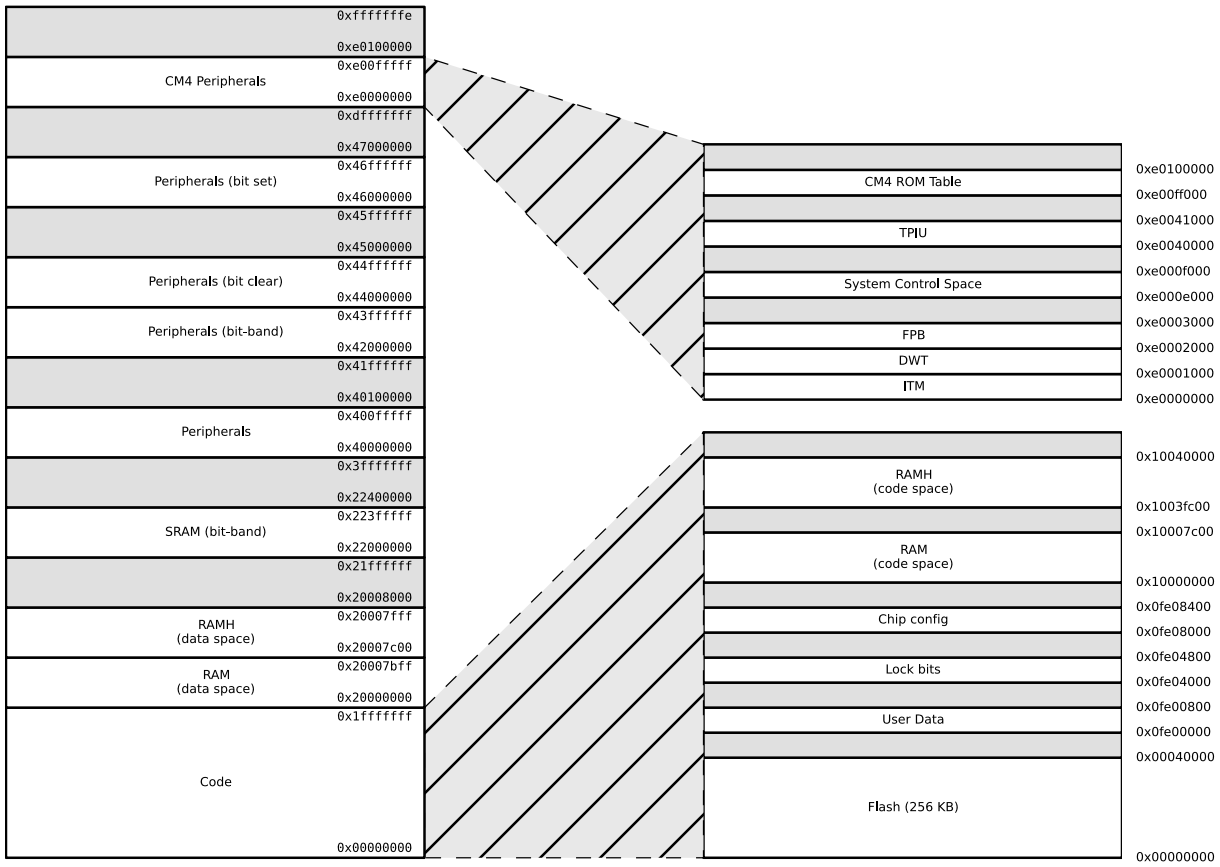


Figure 3.2. EFR32MG1 Memory Map — Core Peripherals and Code Space

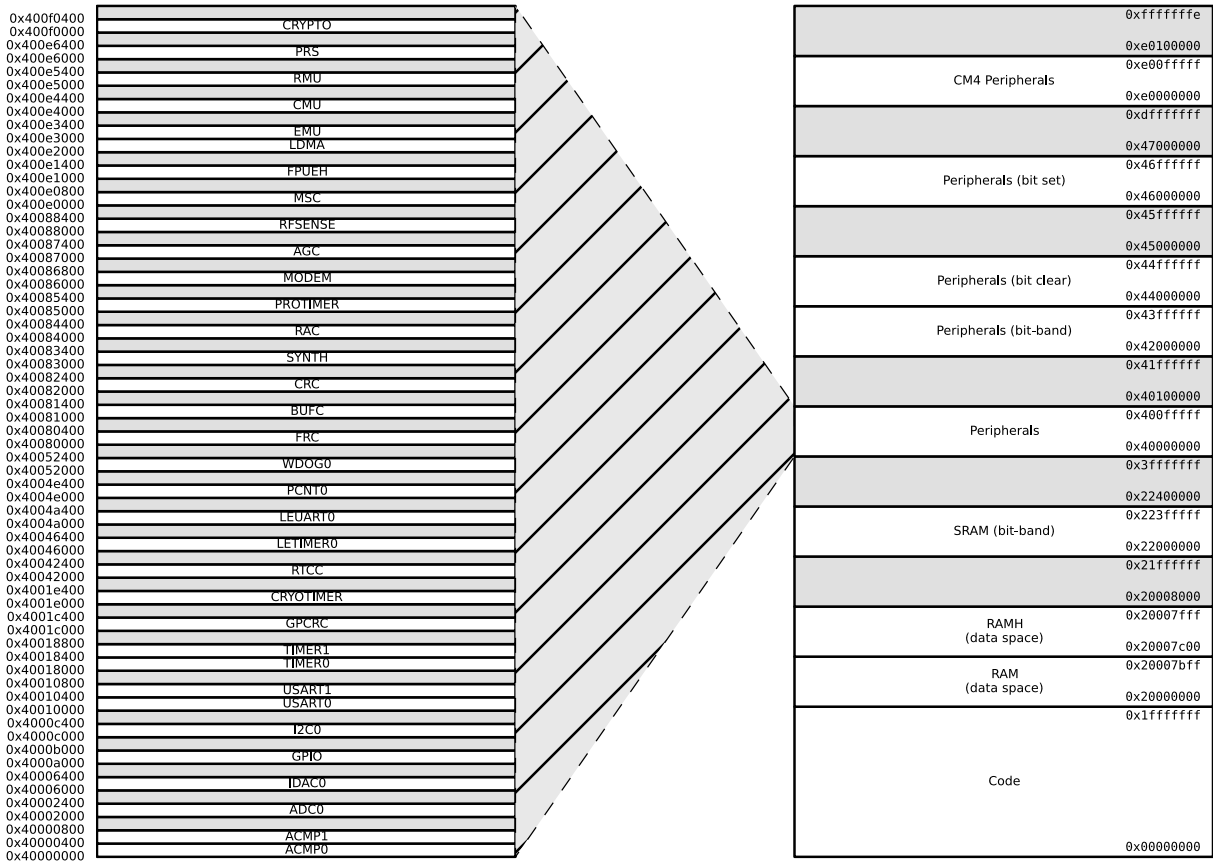


Figure 3.3. EFR32MG1 Memory Map — Peripherals

3.13 Configuration Summary

The features of the EFR32MG1 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.1. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	IrDA I^2S SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1		TIM1_CC[3:0]

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and an operating temperature of -40 to +85 °C, unless stated otherwise.

Refer to Table 4.2 General Operating Conditions on page 15 for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	150	°C
External main supply voltage	V_{DDMAX}		0	—	3.8	V
External main supply voltage ramp rate	$V_{DDRAMPMAX}$		—	—	1	V / µs
Voltage on any 5V tolerant GPIO pin[1]	V_{DIGPIN}		-0.3	—	Min of 5.25 and IOVDD +2	V
Voltage on non-5V tolerant GPIO pins			-0.3	—	IOVDD+0.3	V
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.4	V
Input RF level on pins 2G4RF_IOP and 2G4RF_ION	$P_{RFMAX2G4}$		—	—	10	dBm
Voltage differential between RF pins (2G4RF_IOP - 2G4RF_ION)	V_{MAX2G4}		-50	—	50	mV
Absolute Voltage on RF pins 2G4RF_IOP and 2G4RF_ION	$V_{MAXDIFF2G4}$		-0.3	—	3.3	V
Total current into V_{SS} ground lines (sink)	I_{VSSMAX}		—	—	200	mA
Current per I/O pin (sink)	I_{IOMAX}		—	—	50	mA
Current per I/O pin (source)			—	—	50	mA
Current for all I/O pins (sink)	$I_{IOALLMAX}$		—	—	200	mA
Current for all I/O pins (source)			—	—	200	mA
Voltage difference between AVDD and VREGVDD	ΔV_{DD}		—	—	0.3	V

Note:
1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be the highest voltage in the system
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD
- RFVDD ≤ AVDD
- PAVDD ≤ AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating temperature range	T_{OP}	-G temperature grade	-40	25	85	°C
AVDD Supply voltage[1]	V_{AVDD}		1.85	3.3	3.8	V
VREGVDD Operating supply voltage[12]	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass 50mA load	TBD	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.85	3.3	3.8	V
RFVDD Operating supply voltage	V_{RFVDD}		1.62	—	$V_{VREGVDD}$	V
DVDD Operating supply voltage	V_{DVDD}		1.62	—	$V_{VREGVDD}$	V
PAVDD Operating supply voltage	V_{PAVDD}		1.62	—	$V_{VREGVDD}$	V
IOVDD Operating supply voltage	V_{IOVDD}		1.62	—	$V_{VREGVDD}$	V
Difference between AVDD and VREGVDD, ABS(AVDD-VREGVDD)	dV_{DD}		—	—	0.1	V
HFCLK frequency	f_{CORE}	0 wait-states (MODE = WS0) [3]	—	—	26	MHz
		1 wait-states (MODE = WS1) [3]	—	38.4	40	MHz

Note:

1. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
2. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD_min}+I_{LOAD} * R_{BYP_max}$
3. in MSC_READCTRL register

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance	$THETA_{JA}$	QFN32 Package, 2-Layer PCB, Air velocity = 0 m/s	—	79	—	°C/W
		QFN32 Package, 2-Layer PCB, Air velocity = 1 m/s	—	62.2	—	°C/W
		QFN32 Package, 2-Layer PCB, Air velocity = 2 m/s	—	54.1	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 0 m/s	—	32	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 1 m/s	—	28.1	—	°C/W
		QFN32 Package, 4-Layer PCB, Air velocity = 2 m/s	—	26.9	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 0 m/s	—	64.5	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 1 m/s	—	51.6	—	°C/W
		QFN48 Package, 2-Layer PCB, Air velocity = 2 m/s	—	47.7	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 0 m/s	—	26.2	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 1 m/s	—	23.1	—	°C/W
		QFN48 Package, 4-Layer PCB, Air velocity = 2 m/s	—	22.1	—	°C/W

4.1.4 DC-DC Converter

Test conditions: L_{DCDC}=4.7 µH, C_{DCDC}=1.0 µF (Murata GRM188R71A105KA61D), V_{DCDC_I}=3.3 V, V_{DCDC_O}=1.8 V, I_{DCDC_LOAD}=50 mA, Heavy Drive configuration, F_{DCDC_LN}=8 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, Strong Bypass with PMOS enabled, assumes inductor DCR of 140 mOhms, I_{DCDC_LOAD} = 50 mA	TBD	—	3.8	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	3.8	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	TBD	—	3.8	V
Output voltage programmable range	V_{DCDC_O}	1.8V configuration	TBD	1.8	—	V
Regulation DC Accuracy	ACC_{DC}	Low noise (LN) mode, 1.8 V target output	TBD	—	TBD	mV
		Low power (LP) mode, LPCMPBIAS[1] = 0, 1.8 V target output, I_{DCDC_LOAD} = 200 µA	TBD	—	TBD	mV
		Low power (LP) mode, LPCMPBIAS[1] = 3, 1.8 V target output, I_{DCDC_LOAD} = 10 mA	TBD	—	TBD	mV
Steady-state output ripple	V_R	Radio disabled.	—	3	—	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[1] = 1), Load changes between 0 mA and 100 mA	—	—	150	mV
		DCM Mode (LNFORCECCM[1] = 0), Load changes between 0 mA and 10 mA	—	—	150	mV
DC line regulation	V_{REG}	Input changes between 3.8 V and 2.4 V	—	0.1	—	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%
Max load current	I_{LOAD_MAX}	Low noise (LN) Heavy Drive[2]	—	—	200	mA
		Low noise (LN) mode, Medium Drive[2]	—	—	100	mA
		Low noise (LN) mode, Light Drive[2]	—	—	50	mA
		Low power (LP) mode, LPCMPBIAS[1] = 3	—	—	10	mA
DCDC output capacitor	C_{DCDC}	25% tolerance	TBD	1	TBD	µF
DCDC output inductor	L_{DCDC}	20% tolerance	—	4.7	—	µH

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resistance in Bypass mode	R_{BYP}	BYPPFETEN = 0	TBD	1.2	TBD	Ω
		BYPPFETEN = 1	TBD	0.8	TBD	Ω

Note:

1. In EMU_DCDCMISCCTRL register
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.

4.1.5 Current Consumption

4.1.5.1 Current Consumption 1.85 V without DC-DC Converter

Unless otherwise indicated VREGVDD = AVDD = DVDD = RFVDD = PAVDD= 1.85 V. EMU_PWRCFG_PWRCG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. See Figure 5.1 EFR32MG1 Typical Application Circuit: Direct Supply Configuration without DC-DC converter on page 49.

Table 4.5. Current Consumption 1.85V without DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with radio disabled, All peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash	—	128	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	87	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	103	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	112	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	105	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	235	—	µA/MHz
Current consumption in EM1 Sleep mode with radio disabled. All peripherals disabled	I_{EM1}	38.4 MHz crystal	—	61	—	µA/MHz
		38 MHz HFRCO	—	35	—	µA/MHz
		26 MHz HFRCO	—	37	—	µA/MHz
		1 MHz HFRCO	—	167	—	µA/MHz
Current consumption in EM2 Deep Sleep mode.	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	3.36	—	µA
		4 kB RAM retention and RTCC running from LFRCO	—	3.13	—	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	—	2.84	—	µA
Current consumption in EM4H Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	—	1.08	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.64	—	µA
		128 byte RAM retention, no RTCC	—	0.63	—	µA
Current consumption in EM4S Shutoff mode	I_{EM4S}	No RAM retention, no RTCC	—	0.02	—	µA

4.1.5.2 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated VREGVDD = AVDD = DVDD = RFVDD = PAVDD= 3.3 V. EMU_PWRCFG_PWRCG=NODCDC. EMU_DCDCCTRL_DCDCMODE=BYPASS. See Figure 5.3 EFR32MG1 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDD) on page 50.

Table 4.6. Current Consumption 3.3V without DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with radio disabled, All peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash	—	129	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	87	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	103	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	112	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	105	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	237	—	µA/MHz
Current consumption in EM1 Sleep mode with radio disabled. All peripherals disabled	I_{EM1}	38.4 MHz crystal	—	61	—	µA/MHz
		38 MHz HFRCO	—	35	—	µA/MHz
		26 MHz HFRCO	—	37	—	µA/MHz
		1 MHz HFRCO	—	170	—	µA/MHz
Current consumption in EM2 Deep Sleep mode.	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	3.47	—	µA
		4 kB RAM retention and RTCC running from LFRCO	—	3.35	—	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	—	2.92	—	µA
Current consumption in EM4H Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	—	1.13	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.67	—	µA
		128 byte RAM retention, no RTCC	—	0.66	—	µA
Current consumption in EM4S Shutoff mode	I_{EM4S}	no RAM retention, no RTCC	—	0.04	—	µA

4.1.5.3 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD= 1.8 V DC-DC output. See Figure 5.2 EFR32MG1 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 49.

Table 4.7. Current Consumption 3.3V with DC/DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 Active mode with radio disabled. All peripherals disabled, DCDC in LowNoise mode	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash.	—	87	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	63	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	72	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	78	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	79	—	µA/MHz
Current consumption in EM1 Sleep mode with radio disabled. All peripherals disabled, DCDC in LowPower mode.	I_{EM1}	38.4 MHz crystal	—	39	—	µA/MHz
		38 MHz HFRCO	—	23	—	µA/MHz
		26 MHz HFRCO	—	25	—	µA/MHz
		1 MHz HFRCO	—	142	—	µA/MHz
Current consumption in EM2 Deep Sleep mode.	I_{EM2}	Full RAM retention and RTCC running from LFXO	—	1.4	—	µA
		4 kB RAM retention and RTCC running from LFRCO	—	1.4	—	µA
Current consumption in EM3 Stop mode	I_{EM3}	Full RAM retention and CRYOTIMER running from ULFRCO	—	1.1	—	µA
Current consumption in EM4H Hibernate mode	I_{EM4}	128 byte RAM retention, RTCC running from LFXO	—	0.9	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.6	—	µA
		128 byte RAM retention, no RTCC	—	0.6	—	µA
Current consumption in EM4S Shutoff mode	I_{EM4S}	no RAM retention, no RTCC	—	0.03	—	µA

4.1.5.4 Current Consumption Using Radio

Unless otherwise indicated VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. See Figure 5.2 EFR32MG1 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 49 or Figure 5.3 EFR32MG1 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDD) on page 50.

Table 4.8. Current Consumption Using Radio 3.3 V with DC-DC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)	I_{RX}	1 Mbit/s, 2GFSK, F = 2.4 GHz, Radio clock prescaled by 4	—	8.7	—	mA
		802.15.4 receiving frame, F = 2.4 GHz, Radio clock prescaled by 3	—	9.8	—	mA
Current consumption in transmit mode (MCU in EM1 @ 38.4 MHz, peripheral clocks disabled)	I_{TX}	CW, 0 dBm, F = 2.4 GHz, Radio clock prescaled by 3	—	8.8	—	mA
		CW, 3 dBm, F = 2.4 GHz	—	17.6	—	mA
		CW, 8 dBm, F = 2.4 GHz	—	26.1	—	mA
		CW, 10.5 dBm, F = 2.4 GHz	—	34.1	—	mA
		CW, 16.5 dBm, F = 2.4 GHz, PAVDD connected directly to external 3.3V supply	—	88	—	mA
		CW, 19.5 dBm, F = 2.4 GHz, PAVDD connected directly to external 3.3V supply	—	133	—	mA
RFSENSE current consumption	$I_{RFSENSE}$		—	51	—	nA

4.1.6 Wake up times

Table 4.9. Wake up times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up from EM2 Deep Sleep	t_{EM2_WU}	Code execution from flash	—	10.7	—	µs
		Code execution from RAM	—	3	—	µs
Wakeup time from EM1 Sleep	t_{EM1_WU}	Executing from flash	—	3	—	AHB Clocks
		Executing from RAM	—	3	—	AHB Clocks
Wake up from EM3 Stop	t_{EM3_WU}	Executing from flash	—	10.7	—	µs
		Executing from RAM	—	3	—	µs
Wake up from EM4H Hibernate [1]	t_{EM4H_WU}	Executing from flash	—	60	—	µs
Wake up from EM4S Shutoff[1]	t_{EM4S_WU}		—	290	—	µs

Note:
1. Time from wakeup request until first instruction is executed. Wakeup results in device reset.

4.1.7 Brown Out Detector

Table 4.10. Brown Out Detector

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDDBOD threshold	$V_{DVDDBOD}$	DVDD rising	—	—	TBD	V
		DVDD falling	TBD	—	—	V
DVDD BOD hysteresis	$V_{DVDDBOD_HYST}$		—	24	—	mV
DVDD response time	$t_{DVDDBOD_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	1.85	V
		AVDD falling	TBD	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD_HYST}$		—	21	—	mV
AVDD response time	$t_{AVDDBOD_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	TBD	V
		AVDD falling	TBD	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	46	—	mV
EM4 response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/µs rate	—	300	—	µs

4.1.8 Frequency Synthesizer Characteristics

Table 4.11. Frequency Synthesizer Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF Synthesizer Frequency range	F_{RANGE_2400}	2.4 GHz frequency range	2400	—	2483.5	MHz
LO tuning frequency resolution with 38.4 MHz crystal	F_{RES_2400}	2400 - 2483.5 MHz	—	—	73	Hz
Maximum frequency deviation with 38.4 MHz crystal	ΔF_{MAX_2400}		—	—	1677	kHz

4.1.9 2.4 GHz RF Transceiver Characteristics

4.1.9.1 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated T=25C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.45 GHz. Test circuit according to Figure 5.2 EFR32MG1 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 49 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 50.

Table 4.12. RF Transmitter General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum TX power[1]	$POUT_{MAX}$	19.5 dBm-rated part numbers. PAVDD connected directly to external 3.3V supply	—	19.5	—	dBm
		16.5 dBm-rated part numbers. PAVDD connected directly to external 3.3V supply	—	16.5	—	dBm
		8 dBm-rated part numbers	—	8	—	dBm
Minimum active TX Power	$POUT_{MIN}$	CW		-30	—	dBm
Output power step size	$POUT_{STEP}$	-5 dBm< Output power < 0 dBm	—	1	—	dB
		0 dBm < output power < $POUT_{MAX}$	—	0.5	—	dB
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR_V}$	1.85 V < $V_{VREGVDD}$ < 3.3 V without DC-DC converter, operation at higher than 10.5 dBm.	—	4.5	—	dB
		1.85 V < $V_{VREGVDD}$ < 3.3 V without DC-DC converter, operation at 10.5 dBm.	—	3.8	—	dB
		1.85 V < $V_{VREGVDD}$ < 3.3 V using DC-DC converter	—	2.1	—	dB
Output power variation vs temperature at $POUT_{MAX}$	$POUT_{VAR_T}$	From -40 to +85 °C, PAVDD connected to DCDC output	—	1.4	—	dB
		From -40 to +85 °C, PAVDD connected to external supply	—	1.4	—	dB
Output power variation vs RF frequency at $POUT_{MAX}$	$POUT_{VAR_F}$	Over RF tuning frequency range	—	0.5	—	dB
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of 2. Ordering Information

4.1.9.2 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated T=25C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.440 GHz. Test circuit according to Figure 5.2 EFR32MG1 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 49 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 50.

Table 4.13. RF Receiver General Characteristics for 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	—	-57	—	dBm
		1 GHz to 12 GHz	—	-47	—	dBm
Level above which RFSENSE will trigger	$RFSENSE_{TRIG}$	CW at 2.45 GHz	—	-24	—	dBm
Level below which RFSENSE will not trigger	$RFSENSE_{THRES}$		—	-50	—	dBm
1% PER Sensitivity	$SENS_{2GFSK}$	2 Mbps 2GFSK signal	—	-90.5	—	dBm
0.1% BER Sensitivity		250 kbps 2GFSK signal	—	-99.2	—	dBm

4.1.9.3 RF Transmitter Characteristics for Bluetooth Smart in the 2.4 GHz Band

Unless otherwise indicated T=25C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.44 GHz. Test circuit according to Figure 5.2 EFR32MG1 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 49 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 50.

Table 4.14. RF Transmitter Characteristics for Bluetooth Smart in the 2.4GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6dB bandwidth	TXBW		—	740	—	kHz
Power spectral density limit	PSD_{LIMIT}	Per FCC part 15.247	—	-6.5	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	10	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	99% BW at highest and lowest channels in band	—	1.1	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	At ±2 MHz	—	-39.8	—	dBm
		At ±3 MHz	—	-42.1	—	dBm
Emissions of harmonics out-of-band, per FCC part 15.247	$SPUR_{HRM_FCC}$	2nd,3rd, 5, 6, 8, 9,10 harmonics; continuous transmission of modulated carrier	—	-47.3	—	dBm
Spurious emissions out-of-band, per FCC part 15.247, excluding harmonics captured in $SPUR_{HARM,FCC}$. Restricted Bands	$SPUR_{OOB_FCC}$	Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier[2]	—	-47	—	dBm
Spurious emissions out-of-band, per FCC part 15.247, excluding harmonics captured in $SPUR_{HARM,FCC}$. Non Restricted Bands		Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier	—	-26	—	dBc
Spurious emissions out-of-band; per ETSI 300.328	$SPUR_{ETSI328}$	[2400-BW to 2400] MHz, [2483.5 to 2483.5+BW] MHz	—	-16	—	dBm
		[2400-2BW to 2400-BW] MHz, [2483.5+BW to 2483.5+2BW] MHz per ETSI 300.328	—	-26	—	dBm
Spurious emissions per ETSI EN300.440	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz	—	-60	—	dBm
		25-1000 MHz	—	-42	—	dBm
		1-12 GHz	—	-36	—	dBm

Note:

1. Per Bluetooth Core_4.2, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.
2. For 2480 Mhz, a maximum duty cycle of 20% is used to achieve this value.

4.1.9.4 RF Receiver Characteristics for Bluetooth Smart in the 2.4 GHz Band

Unless otherwise indicated T=25C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4MHz. RF center frequency 2.440 GHz. Test circuit according to Figure 5.2 EFR32MG1 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 49 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 50.

Table 4.15. RF Receiver Characteristics for Bluetooth Smart in the 2.4GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 0.1% BER	SAT	Signal is reference signal[1]. Packet length is 20 bytes.	—	10	—	dBm
Sensitivity, 0.1% BER	SENS	Signal is reference signal[1]. Using DC-DC converter	—	-94	—	dBm
		With dirty transmitter as defined in Core_4.1	—	-91.8	—	dBm
Signal to co-channel interferer, 0.1% BER	C/I_{CC}	Desired signal 3 dB above reference sensitivity	—	8.3	—	dB
N+1 adjacent channel (1 MHz) selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_{1+}	Interferer is reference signal at +1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-3	—	dB
N-1 adjacent channel (1 MHz) selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_{1-}	Interferer is reference signal at -1 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-0.5	—	dB
Alternate (2 MHz) selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_2	Interferer is reference signal at ± 2 MHz offset. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz	—	-43	—	dB
Alternate (3 MHz) selectivity, 0.1% BER, with allowable exceptions. Desired is reference signal at -67 dBm	C/I_3	Interferer is reference signal at ±3 MHz offset. Desired frequency 2404 MHz ≤ Fc ≤ 2480 MHz	—	-46.7	—	dB
Selectivity to image frequency, 0.1% BER. Desired is reference signal at -67 dBm	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision	—	-38.7	—	dB
Selectivity to image frequency +1 MHz, 0.1% BER. Desired is reference signal at -67 dBm	C/I_{IM+1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision	—	-48.2	—	dB
Blocking, 0.1% BER, Desired is reference signal at -67 dBm. Interferer is CW in OOB range.	$BLOCK_{OOB}$	Interferer frequency 30 MHz ≤ f ≤ 2000 MHz	—	-27	—	dBm
		Interferer frequency 2003 MHz ≤ f ≤ 2399 MHz	—	-32	—	dBm
		Interferer frequency 2484 MHz ≤ f ≤ 2997 MHz	—	-32	—	dBm
		Interferer frequency 3 GHz ≤ f ≤ 12.75 GHz	—	-27	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Intermodulation performance per Core_4.1, Vol 6 Section 4.4 (n = 3 alternative), 0.1% BER.	IM	Desired is reference signal at 6dB above reference sensitivity level. Interferer 1 is CW at level IM_{BLE}. Interferer 2 is reference signal at IM_{BLE}.	—	-33	—	dBm
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		4	—	—	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		—	—	-101	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$	—	—	0.5	dB

Note:

1. Reference signal is defined 2GFSK at -67 dBm, Modulation index = 0.5, BT = 0.5, Bit rate = 1 Mbps, desired data = PRBS9; interferer data = PRBS15; frequency accuracy better than 1 ppm

4.1.9.5 RF Transmitter Characteristics for 802.15.4 O-QPSK DSSS in the 2.4 GHz Band

Unless otherwise indicated T=25 °C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Test circuit according to Figure 5.2 EFR32MG1 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 49 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 50

Table 4.16. RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error vector magnitude (offset EVM), per 802.15.4-2011	EVM	Average across frequency. Signal is DSSS-OQPSK reference packet[1]	—	6.1	—	% rms
Power spectral density limit	PSD_{LIMIT}	Relative, at carrier ±3.5 MHz	—	-26	—	dBc
		Absolute, at carrier ±3.5 MHz[2]	—	-36	—	dBm
		Per FCC part 15.247	—	-3.8	—	dBm/ 3kHz
		Output power level which meets 10dBm/MHz ETSI 300.328 specification	—	12	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	99% BW at highest and lowest channels in band	—	2.25	—	MHz
Emissions of harmonics out-of-band, per FCC part 15.247	$SPUR_{HRM_FCC}$	2nd,3rd, 5, 6,8,9,10 harmonics; continuous transmission of modulated carrier	—	-49.7	—	dBm
Spurious emissions out-of-band, per FCC part 15.247, excluding harmonics. Restricted Bands	$SPUR_{OOB_FCC}$	Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier[3]	—	-47	—	dBm
Spurious emissions out-of-band, per FCC part 15.247, excluding harmonics, Non Restricted Bands		Above 2.483 GHz or below 2.4 GHz; continuous transmission of modulated carrier	—	-35.4	—	dBc
Spurious emissions out-of-band; per ETSI 300.328[4]	$SPUR_{ETSI328}$	[2400-BW to 2400], [2483.5 to 2483.5+BW];	—	-36.6	—	dBm
		[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW]; per ETSI 300.328	—	-41.7	—	dBm
Spurious emissions per ETSI EN300.440[4]	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz	—	-60	—	dBm
		25-1000 MHz,	—	-42	—	dBm
		1G-24G	—	-36	—	dBm

Note:

1. Reference packet is defined as 20 octet PSDU, modulated according to 802.15.4-2011 DSSS-OQPSK in the 2.4GHz band, with pseudo-random packet data content
2. For 2415 Mhz, a maximum duty cycle of 50% is used to achieve this value.
3. For 2480 Mhz, a maximum duty cycle of 20% is used to achieve this value.
4. Specified at maximum power output level of 10 dBm

4.1.9.6 RF Receiver Characteristics for 802.15.4 O-QPSK DSSS in the 2.4 GHz Band

Unless otherwise indicated T=25 °C,VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = RFVDD = PAVDD. RFVDD and PAVDD path is filtered using ferrites. Crystal frequency=38.4 MHz. RF center frequency 2.445 GHz. Test circuit according to Figure 5.2 EFR32MG1 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC) on page 49 and Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 50

Table 4.17. RF Receiver Characteristics for 801.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level, 1% PER	SAT	Signal is reference signal[1]. Packet length is 20 octets.	—	10	—	dBm
Sensitivity, 1% PER	SENS	Signal is reference signal. Packet length is 20 octets. Using DC-DC converter.	—	-101	—	dBm
		Signal is reference signal. Packet length is 20 octets. Without DC-DC converter.	—	-101	—	dBm
Co-channel interferer rejection, 1% PER	CCR	Desired signal 10 dB above sensitivity limit	—	-2.6	—	dB
High-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[2]	ACR_{+1}	Interferer is reference signal at +1 channel-spacing.	—	33.75	—	dB
		Interferer is filtered reference signal[3] at +1 channel-spacing.	—	52.2	—	dB
		Interferer is CW at +1 channel-spacing.[4]	—	58.6	—	dB
Low-side adjacent channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[2]	ACR_{-1}	Interferer is reference signal at -1 channel-spacing.	—	35	—	dB
		Interferer is filtered reference signal[3] at -1 channel-spacing.	—	54.7	—	dB
		Interferer is CW at -1 channel-spacing.	—	60.1	—	dB
Alternate channel rejection, 1% PER. Desired is reference signal at 3dB above reference sensitivity level[2]	ACR_2	Interferer is reference signal at ±2 channel-spacing	—	45.9	—	dB
		Interferer is filtered reference signal[3] at ±2 channel-spacing	—	56.8	—	dB
		Interferer is CW at ±2 channel-spacing	—	65.5	—	dB
Image rejection , 1% PER, Desired is reference signal at 3dB above reference sensitivity level[2]	IR	Interferer is CW in image band[4]	—	49.3	—	dB
Blocking rejection of all other channels. 1% PER, Desired is reference signal at 3dB above reference sensitivity level[2]. Interferer is reference signal.	BLOCK	Interferer frequency < Desired frequency - 3 channel-spacing	—	57.2	—	dB
		Interferer frequency > Desired frequency + 3 channel-spacing	—	57.9	—	dB
Blocking rejection of 802.11g signal centered at +12MHz or -13MHz	$BLOCK_{80211G}$	Desired is reference signal at 6dB above reference sensitivity level[2]	—	51.6	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		5	—	—	dBm
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		—	—	-98	dBm
RSSI resolution	$RSSI_{RES}$	over $RSSI_{MIN}$ to $RSSI_{MAX}$	—	0.25	—	dB
RSSI linearity as defined by 802.15.4-2003	$RSSI_{LIN}$		—	0.5	—	dB

Note:

1. Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksymbols/s
2. Reference sensitivity level is -85 dBm
3. Filter is characterized as a symmetric bandpass centered on the adjacent channel having a 3dB bandwidth of 4.6 MHz and stopband rejection better than 26 dB beyond 3.15 MHz from the adjacent carrier.
4. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency ±5 MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.

4.1.10 Modem Features

Table 4.18. Modem Features

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Receive Bandwidth	$RX_{Bandwidth}$	Configurable range with 38.4 MHz crystal	0.1	—	2530	kHz
IF Frequency	IF_{Freq}	Configurable range with 38.4 MHz crystal. Selected steps available.	150	—	1371	kHz
DSSS symbol length	$DSSS_{Range}$	Configurable in steps of 1 chip	2	—	32	chips
DSSS Bits per symbol	$DSSS_{BitPerSym}$	Configurable	1	—	4	bits/symbol

4.1.11 Oscillators

4.1.11.1 LFXO

Table 4.19. LFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	—	70	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}		6	—	18	pF
On-chip tuning cap range [2]	C_{LFXO_T}	On each of LFXTAL_N and LFXTAL_P pins	8	—	40	pF
On-chip tuning cap step size	SS_{LFXO}		—	0.25	—	pF
Current consumption after startup [3]	I_{LFXO}	ESR = 30 kΩ, C_L=12.5 pF, GAIN[4] = 3, AGC[4] = 1	—	273	—	nA
Start- up time	t_{LFXO}	ESR=30 kΩ, C_L=12.5 pF, GAIN[4] =2	—	308	—	ms

Note:

1. Total load capacitance as seen by the crystal
2. The effective load capacitance seen by the crystal will be C_{LFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register
4. In CMU_LFXOCTRL register

4.1.11.2 HFXO

Table 4.20. HFXO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	f_{HFXO}		38	38.4	40	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	Crystal frequency 38.4 MHz	—	—	60	Ω
Supported range of crystal load capacitance [1]	C_{HFXO_CL}		6	—	12	pF
On-chip tuning cap range [2]	C_{HFXO_T}	On each of HFXTAL_N and HFXTAL_P pins	9	20	25	pF
On-chip tuning capacitance step	SS_{HFXO}		—	0.04	—	pF
Startup time	t_{HFXO}	38.4 MHz: ESR=50 Ω, C_L = 10 pF, BOOST[3] = 2	—	300	—	µs
Frequency Tolerance for the crystal	FT_{HFXO}	38.4 MHz, ESR = 50 Ω, CL = 10 pF	-40	—	40	ppm

Note:
1. Total load capacitance as seen by the crystal
2. The effective load capacitance seen by the crystal will be C_{HFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. In CMU_HFXOCTRL register

4.1.11.3 LFRCO

Table 4.21. LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	TBD	32.768	TBD	kHz
		ENVREF = 0 in CMU_LFRCOCTRL	TBD	32.768	TBD	kHz
Startup time	t_{LFRCO}		—	500	—	µs
Current consumption [1]	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	342	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	494	—	nA

Note:
1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register

4.1.11.4 HFRCO and AUXHFRCO

Table 4.22. HFRCO and AUXHFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{HFRCO}	38 MHz frequency band	TBD	38	TBD	MHz
		32 MHz frequency band	TBD	32	TBD	MHz
		26 MHz frequency band	TBD	26	TBD	MHz
		19 MHz frequency band	TBD	19	TBD	MHz
		16 MHz frequency band	TBD	16	TBD	MHz
		13 MHz frequency band	TBD	13	TBD	MHz
		7 MHz frequency band	TBD	7	TBD	MHz
		4 MHz frequency band	TBD	4	TBD	MHz
		2 MHz frequency band	TBD	2	TBD	MHz
		1 MHz frequency band	TBD	1	TBD	MHz
Start-up time	t_{HFRCO}	$f_{HFRCO} \geq 19$ MHz	—	300	—	ns
		$4 < f_{HFRCO} < 19$ MHz	—	1	—	µs
		$f_{HFRCO} \leq 4$ MHz	—	2.5	—	µs
Current consumption on DVDD	$I_{HFRCODIG}$	$f_{HFRCO} = 38$ MHz	—	43	—	µA
		$f_{HFRCO} = 32$ MHz	—	37	—	µA
		$f_{HFRCO} = 26$ MHz	—	31	—	µA
		$f_{HFRCO} = 19$ MHz	—	25	TBD	µA
		$f_{HFRCO} = 16$ MHz	—	22	—	µA
		$f_{HFRCO} = 13$ MHz	—	19	—	µA
		$f_{HFRCO} = 7$ MHz	—	12	—	µA
		$f_{HFRCO} = 4$ MHz	—	10	—	µA
		$f_{HFRCO} = 2$ MHz	—	8	—	µA
		$f_{HFRCO} = 1$ MHz	—	7	—	µA
Current consumption on AVDD [1]	$I_{HFRCOANA}$	$f_{HFRCO} = 38$ MHz	—	161	—	µA
		$f_{HFRCO} = 32$ MHz	—	134	—	µA
		$f_{HFRCO} = 26$ MHz	—	116	—	µA
		$f_{HFRCO} = 19$ MHz	—	101	TBD	µA
		$f_{HFRCO} = 16$ MHz	—	88	—	µA
		$f_{HFRCO} = 13$ MHz	—	81	—	µA
		$f_{HFRCO} = 7$ MHz	—	69	—	µA
		$f_{HFRCO} = 4$ MHz	—	23	—	µA
		$f_{HFRCO} = 2$ MHz	—	23	—	µA
		$f_{HFRCO} = 1$ MHz	—	23	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Step size	SS_{HFRCO}	Coarse (% of period)	—	0.8	—	%
		Fine (% of period)	—	0.1	—	%
Period Jitter	PJ_{HFRCO}		—	0.2	—	% RMS

Note:
1. Current consumption on DVDD instead if ANASW=1 in EMU_PWRCTRL register

4.1.11.5 ULFRCO

Table 4.23. ULFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		TBD	1	TBD	kHz

4.1.12 Flash Memory Characteristics

Table 4.24. Flash Memory Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		10000	—	—	cycles
Flash data retention	RET_{FLASH}	T_{AMB}<85°C	10	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	26	40	µs
Page erase time	t_{PERASE}		20	27	40	ms
Mass erase time	t_{MERASE}		20	27	40	ms
Device erase time[2]	t_{DERASE}		—	60	TBD	ms
Page erase current[3]	I_{ERASE}		—	—	3	mA
Mass or Device erase current[3]			—	—	5	mA
Write current[3]	I_{WRITE}		—	—	3	mA

Note:
1. Flash data retention information is published in the Quarterly Quality and Reliability Report.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW)
3. Measured at 25°C

4.1.13 GPIO

Table 4.25. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	IOVDD*0.3	V
Input high voltage	V_{IOIH}		IOVDD*0.7	—	—	V
Output high voltage relative to IOVDD	V_{IOOH}	Sourcing 3 mA, V_{DD} ≥ 3 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.8	—	—	V
		Sourcing 1.2 mA, V_{DD} ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.6	—	—	V
		Sourcing 20 mA, V_{DD} ≥ 3 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.8	—	—	V
		Sourcing 8 mA, V_{DD} ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.6	—	—	V
Output low voltage relative to IOVDD	V_{IOOL}	Sinking 3 mA, V_{DD} ≥ 3 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.2	V
		Sinking 1.2 mA, V_{DD} ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.4	V
		Sinking 20 mA, V_{DD} ≥ 3 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.2	V
		Sinking 8 mA, V_{DD} ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.4	V
Input leakage current	I_{IOLEAK}	GPIO ≤ IOVDD	—	0.1	TBD	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	IOVDD < GPIO ≤ IOVDD + 2 V	—	3.3	15	µA
I/O pin pull-up resistor	R_{PU}		TBD	43	TBD	kΩ
I/O pin pull-down resistor	R_{PD}		TBD	43	TBD	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		TBD	25	TBD	ns
Output fall time, From 70% to 30% of V_{IO}	t_{IOOF}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE[1] = 0x6	—	1.8	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	4.5	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output rise time, From 30% to 70% of V_{IO}	t_{IOOR}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE = 0x6[1]	—	2.2	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	7.4	—	ns

Note:
1. In GPIO_Pn_CTRL register

4.1.14 VMON

Table 4.26. VMON

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VMON Supply Current	I_{VMON}	In EM0 or EM1, 1 supply monitored	—	5.8	—	µA
		In EM0 or EM1, 4 supplies monitored	—	11.8	—	µA
		In EM2, EM3 or EM4, 1 supply monitored	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored	—	99	—	nA
VMON Loading of Monitored Supply	I_{SENSE}	In EM0 or EM1	—	2	—	µA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V_{VMON_RANGE}		TBD	—	TBD	V
Threshold step size	N_{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t_{VMON_RES}	Supply drops at 1V/µs rate	—	460	—	ns
Hysteresis	V_{VMON_HYST}		—	26	—	mV

4.1.15 ADC

Table 4.27. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	$V_{RESOLUTION}$		6	—	12	Bits
Input voltage range	V_{ADCIN}	Single ended	0	—	2*V_{REF}	V
		Differential	-V_{REF}	—	V_{REF}	V
Input range of external reference voltage, single ended and differential	$V_{ADCREFIN_P}$		1	—	V_{AVDD}	V
Power supply rejection[1]	$PSRR_{ADC}$	At DC	—	80	—	dB
Analog input common mode rejection ratio	$CMRR_{ADC}$	At DC	—	80	—	dB
Current on DVDD, using internal reference buffer. Continous operation. WARMUPMODE[2] = KEEPADCWARM	$I_{ADCDIG_CONTINOUS}$	1 Msps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	40	—	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG[3] = 6	—	15	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG[3] = 15	—	9	—	µA
Current on DVDD, using internal reference buffer. Duty-cycled operation. WARMUPMODE[2] = NORMAL	I_{ADCDIG_NORMAL}	35 ksps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	40	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG[3] = 0	—	5	—	µA
Current on DVDD, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[2] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADCDIG_STANDBY}$	125 ksps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	12	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	6	—	µA
Current on AVDD[4], using internal reference buffer. Continous operation. WARMUPMODE[2] = KEEPADCWARM	$I_{ADCANA_CONTINOUS}$	1 Msps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	286	—	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG[3] = 6	—	155	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG[3] = 15	—	102	—	µA
Current on AVDD[4] , using internal reference buffer. Duty-cycled operation. WARMUPMODE[2] = NORMAL	I_{ADCANA_NORMAL}	35 ksps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	35	—	µA
		5 ksps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	5	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current on AVDD[4], using internal reference buffer. Duty-cycled operation. WARMUPMODE[2] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADCANA_STANDBY}$	125 ksps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	110	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG[3] = 0	—	80	—	µA
ADC Clock Frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	$f_{ADCRATE}$		—	—	1	Msps
Conversion time[5]	$t_{ADCCONV}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core in NORMAL mode	$t_{ADCSTART}$	WARMUPMODE[2] = NORMAL	—	—	5	µs
From standby mode		WARMUPMODE[2] = KEEPINSTANDBY or KEEPINSLOWACC	—	—	1	µs
SNDR at 1Msps and f_{in} = 10kHz	$SNDR_{ADC}$	Internal reference, 2.5 V full-scale, differential (-1.25, 1.25)	TBD	67	—	dB
		vrefp_in = 1.25 V direct mode with 2.5 V full-scale, differential	—	68	—	dB
Spurious-Free Dynamic Range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Input referred ADC noise, rms	V_{REF_NOISE}	Including quantization noise and distortion	—	380	—	µV
Offset Error	$V_{ADCOFFSETERR}$		TBD	1	TBD	LSB
Gain error in ADC	V_{ADC_GAIN}	Using internal reference	—	-0.2	TBD	%
		Using external reference	—	-1	—	%
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution	-1	—	TBD	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	TBD	—	TBD	LSB
Temperature Sensor Slope	V_{TS_SLOPE}		—	-1.84	—	mV/°C

Note:

1. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL
2. In ADCn_CNTL register
3. In ADCn_BIASPROG register
4. Current consumption on DVDD instead if ANASW=1 in EMU_PWRCTRL register
5. Derived from ADCCLK

4.1.16 IDAC

Table 4.28. IDAC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Number of Ranges	N_{IDAC_RANGES}		—	4	—	-
Output Current	I_{IDAC_OUT}	RANGSEL[1] = RANGE0	0.05	—	1.6	µA
		RANGSEL[1] = RANGE1	1.6	—	4.7	µA
		RANGSEL[1] = RANGE2	0.5	—	16	µA
		RANGSEL[1] = RANGE3	2	—	64	µA
Linear steps within each range	N_{IDAC_STEPS}		—	32	—	
Step size	SS_{IDAC}	RANGSEL[1] = RANGE0	—	50	—	nA
		RANGSEL[1] = RANGE1	—	100	—	nA
		RANGSEL[1] = RANGE2	—	500	—	nA
		RANGSEL[1] = RANGE3	—	2	—	µA
Total Accuracy, STEPSEL[1] = 0x10	ACC_{IDAC}	EM0 or EM1, AVDD=3.3 V, T = 25 °C	TBD	—	TBD	%
		EM0 or EM1	TBD	—	TBD	%
		EM2 or EM3	TBD	—	TBD	%
Start up time	t_{IDAC_SU}	Output within 1% of steady state value	—	5	—	µs
Settling time, (output settled within 1% of steady state value)	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	µs
		Step value is changed	—	1	—	µs
Current consumption in EM0 or EM1 [2]	I_{IDAC}	Source mode, excluding output current	—	8.9	—	µA
		Sink mode, excluding output current	—	12	—	µA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mv)	—	0.16	—	%
		RANGESEL1=1, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mV)	—	0.08	—	%
		RANGESEL1=2, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-150 mV)	—	0.03	—	%
		RANGESEL1=3, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-250 mV)	—	0.03	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.82	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.65	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.4	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.25	—	%

Note:

1. In IDAC_CURPROG register
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.17 Analog Comparator (ACMP)

Table 4.29. ACMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}	CMPVDD = ACMPn_CTRL_PWRSEL [1]	0	—	CMPVDD	V
Active current not including voltage reference	I_{ACMP}	BIASPROG[2] = 1, FULLBIAS[2] = 0	—	50	—	nA
		BIASPROG[2] = 0x10, FULLBIAS[2] = 0	—	306	—	nA
		BIASPROG[2] = 0x20, FULLBIAS[2] = 1	—	74	TBD	µA
Current consumption of internal voltage reference,	$I_{ACMPREF}$	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	µA
		VADIV selected as input using VDD/1	—	2.4	—	µA
Hysteresis	$V_{ACMPHYST}$	HYSTSEL[3] = HYST0	—	0	TBD	mV
		HYSTSEL[3] = HYST1	—	12	—	mV
		HYSTSEL[3] = HYST2	—	22	—	mV
		HYSTSEL[3] = HYST3	—	30	—	mV
		HYSTSEL[3] = HYST4	—	36	—	mV
		HYSTSEL[3] = HYST5	—	41	—	mV
		HYSTSEL[3] = HYST6	—	47	—	mV
		HYSTSEL[3] = HYST7	—	52	—	mV
Comparator delay	$t_{ACMPDELAY}$	BIASPROG[2] = 1, FULLBIAS[2] = 0 [4]	—	30	—	µs
		BIASPROG[2] = 0x10, FULLBIAS[2] = 0 [4]	—	3.7	—	µs
		BIASPROG[2] = 0x20, FULLBIAS[2] = 1 [4]	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[2] =0x20, FULLBIAS[2] = 1 [4]	—	—	TBD	mV
Reference Voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Capacitive Sense Internal Resistance	R_{CSRES}	CSRESSEL[5] = 0	—	inf	—	kΩ
		CSRESSEL[5] = 1	—	15	—	kΩ
		CSRESSEL[5] = 2	—	27	—	kΩ
		CSRESSEL[5] = 3	—	39	—	kΩ
		CSRESSEL[5] = 4	—	51	—	kΩ
		CSRESSEL[5] = 5	—	102	—	kΩ
		CSRESSEL[5] = 6	—	164	—	kΩ
		CSRESSEL[5] = 7	—	239	—	kΩ

Note:

1. CMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD
2. In ACMPn_CTRL register
3. In ACMPn_HYSTERESIS register
4. ± 100 mV differential
5. In ACMPn_INPUTSEL register

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given as:

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$$

$I_{ACMPREF}$ is zero if an external voltage reference is used.

4.1.18 I2C

I2C Standard-mode (Sm)

Table 4.30. I2C Standard-mode (Sm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	$t_{SU,DAT}$		250	—	—	ns
SDA hold time[3]	$t_{HD,DAT}$		100	—	3450	ns
Repeated START condition set-up time	$t_{SU,STA}$		4.7	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$		4	—	—	µs
STOP condition set-up time	$t_{SU,STO}$		4	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW})

I2C Fast-mode (Fm)

Table 4.31. I2C Fast-mode (Fm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	$t_{SU,DAT}$		100	—	—	ns
SDA hold time[3]	$t_{HD,DAT}$		100	—	900	ns
Repeated START condition set-up time	$t_{SU,STA}$		0.6	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$		0.6	—	—	µs
STOP condition set-up time	$t_{SU,STO}$		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:
1. For CLHR set to 1 in the I2Cn_CTRL register
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW})

I2C Fast-mode Plus (Fm+)

Table 4.32. I2C Fast-mode Plus (Fm+)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	$t_{SU,DAT}$		50	—	—	ns
SDA hold time	$t_{HD,DAT}$		100	—	—	ns
Repeated START condition set-up time	$t_{SU,STA}$		0.26	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$		0.26	—	—	µs
STOP condition set-up time	$t_{SU,STO}$		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:
1. For CLHR set to 0 or 1 in the I2Cn_CTRL register
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual

4.1.19 USART SPI

SPI Master Timing

Table 4.33. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [2]	t_{SCLK}		2 * $t_{HFPERCLK}$	—	—	ns
CS to MOSI [1] [2]	t_{CS_MO}		0	—	8	ns
SCLK to MOSI [1] [2]	t_{SCLK_MO}		3	—	20	ns
MISO setup time [1] [2]	t_{SU_MI}	IOVDD = 1.98 V	56	—	—	ns
		IOVDD = 3.0 V	37	—	—	ns
MISO hold time [1] [2]	t_{H_MI}		6	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

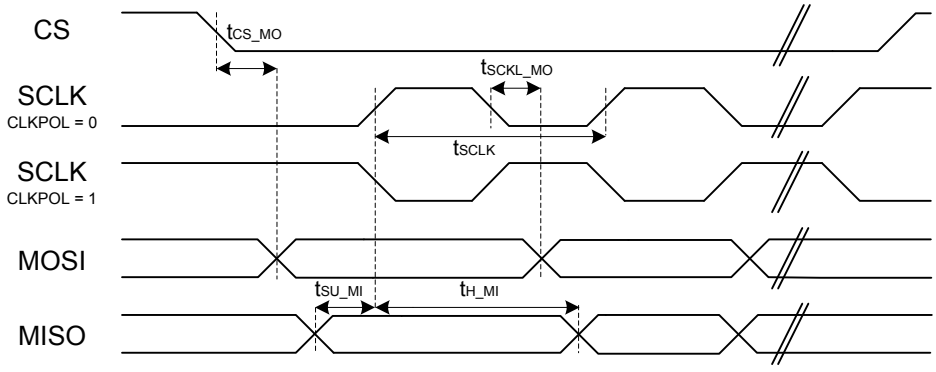


Figure 4.1. SPI Master Timing Diagram

SPI Slave Timing

Table 4.34. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCKL period [1] [2]	t_{SCLK_sl}		2 * $t_{HFPERCLK}$	—	—	ns
SCLK high period[1] [2]	t_{SCLK_hi}		3 * $t_{HFPERCLK}$	—	—	ns
SCLK low period [1] [2]	t_{SCLK_lo}		3 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1] [2]	$t_{CS_ACT_MI}$		4	—	50	ns
CS disable to MISO [1] [2]	$t_{CS_DIS_MI}$		4	—	50	ns
MOSI setup time [1] [2]	t_{SU_MO}		4	—	—	ns
MOSI hold time [1] [2]	t_{H_MO}		3 + 2 * $t_{HFPERCLK}$	—	—	ns
SCLK to MISO [1] [2]	t_{SCLK_MI}		16 + $t_{HFPERCLK}$	—	66 + 2 * $t_{HFPERCLK}$	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

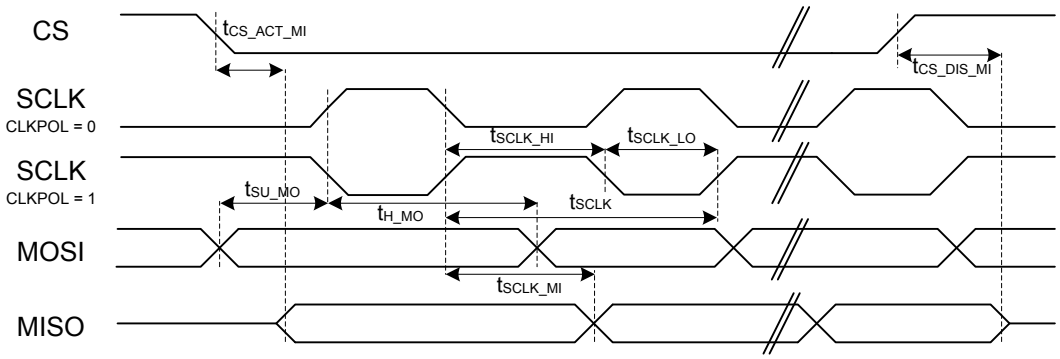


Figure 4.2. SPI Slave Timing Diagram

4.2 Typical Performance Curves

Default test conditions: CCM mode, LDCDC = 4.7 µH, CDCDC = 1.0 µF, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 8 MHz

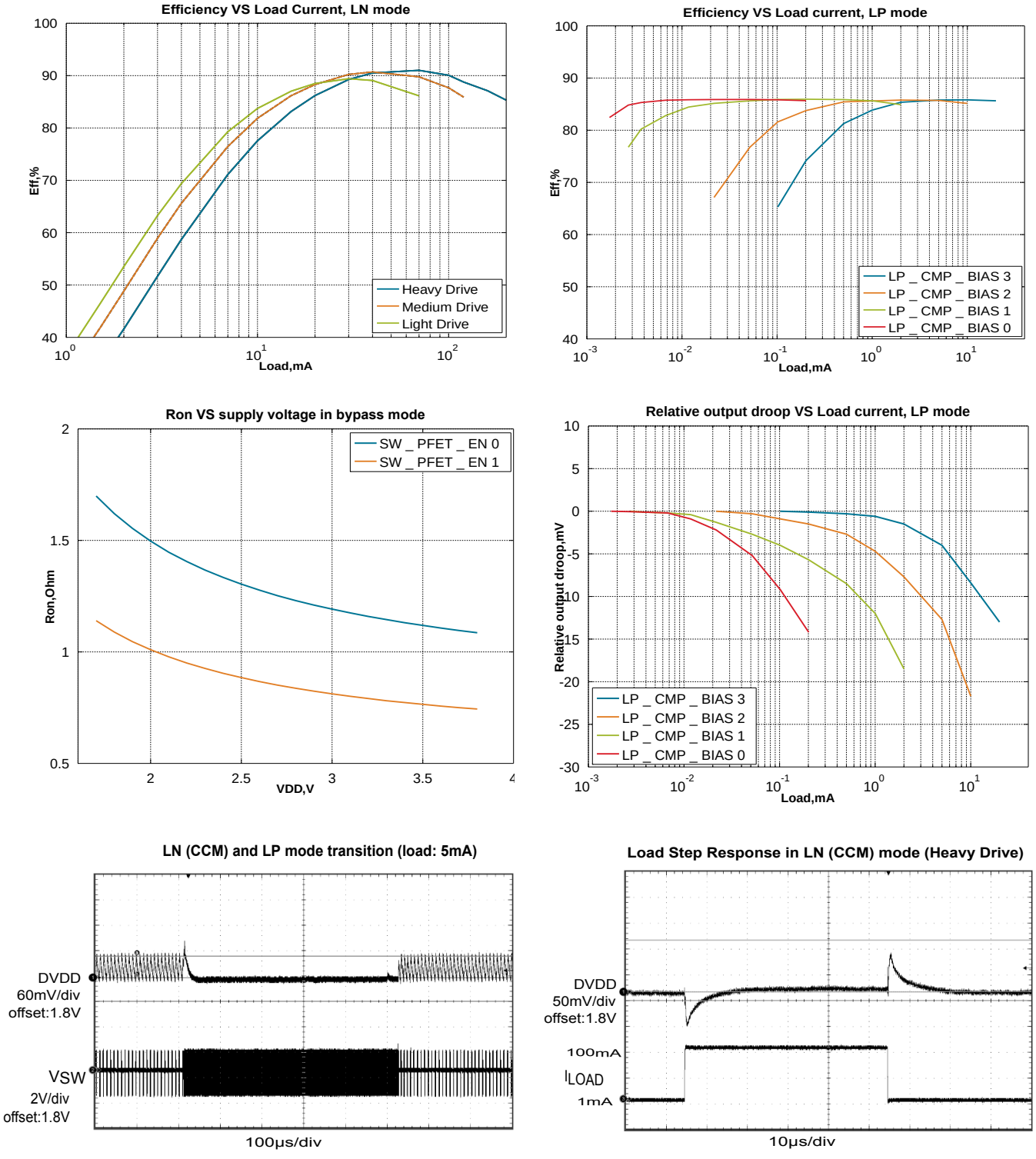


Figure 4.3. DC-DC Converter Typical Performance Characteristics

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections for direct supply, without using the internal DC-DC converter, are shown in the following figure.

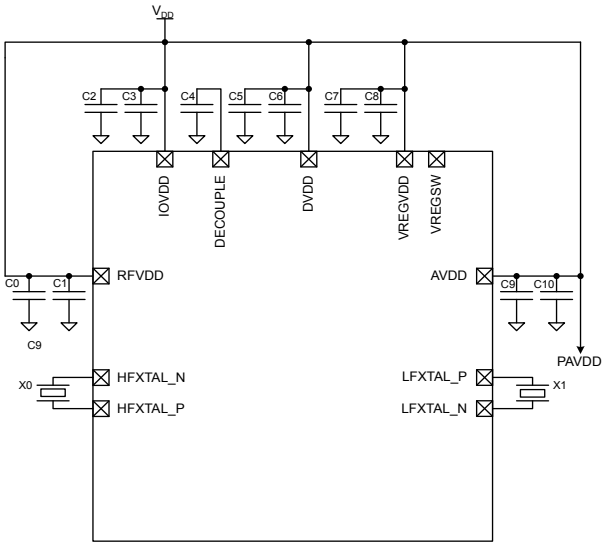


Figure 5.1. EFR32MG1 Typical Application Circuit: Direct Supply Configuration without DC-DC converter

Typical power supply circuits using the internal DC-DC converter are shown below. The MCU operates from the DC-DC converter supply. For low RF transmit power applications less than 13dBm, the RF PA may be supplied by the DC-DC converter. For OPNs supporting high power RF transmission, the RF PA must be directly supplied by VDD for RF transmit power greater than 13 dBm.

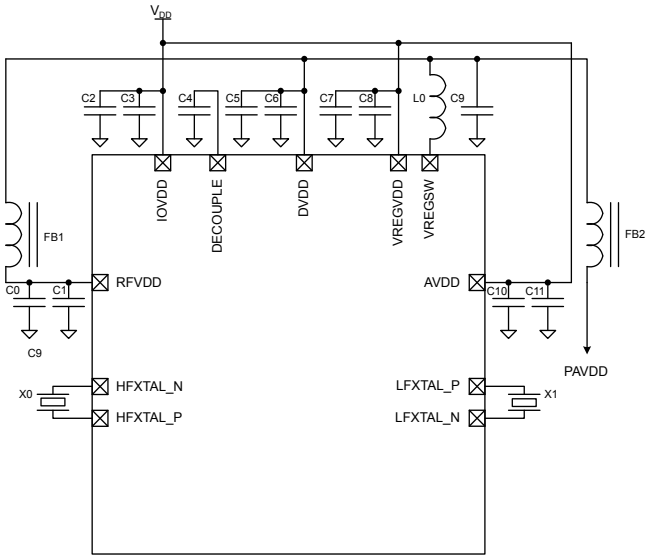


Figure 5.2. EFR32MG1 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDCDC)

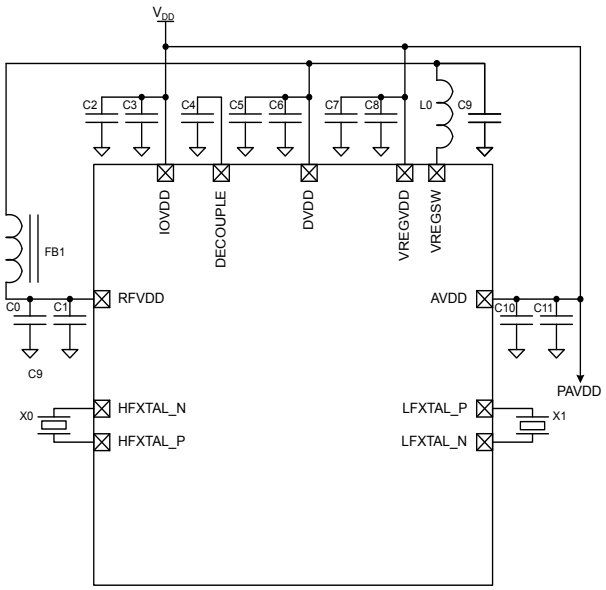


Figure 5.3. EFR32MG1 Typical Application Circuit: Configuration with DC-DC Coverter (PAVDD from VDD)

5.2 RF Matching Networks

Typical RF matching network circuit diagrams are shown in Figure 5.4 Typical 2.4 GHz RF impedance-matching network circuits on page 50 for applications in the 2.4GHz band. Application-specific component values can be found in the EFR32 Reference Manual. For low RF transmit power applications less than 13dBm, the two-element match is recommended. For OPNs supporting high power RF transmission, the four-element match is recommended for high RF transmit power (> 13dBm).

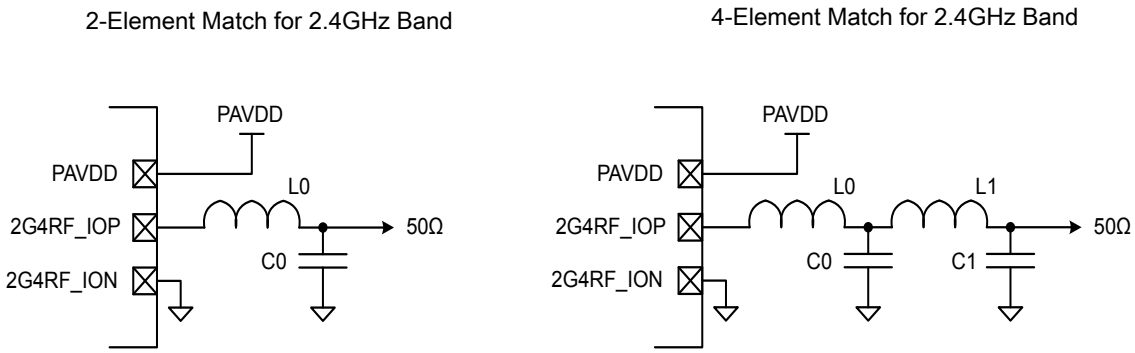


Figure 5.4. Typical 2.4 GHz RF impedance-matching network circuits

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002: "Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 EFR32MG1 QFN48 2.4 GHz Definition

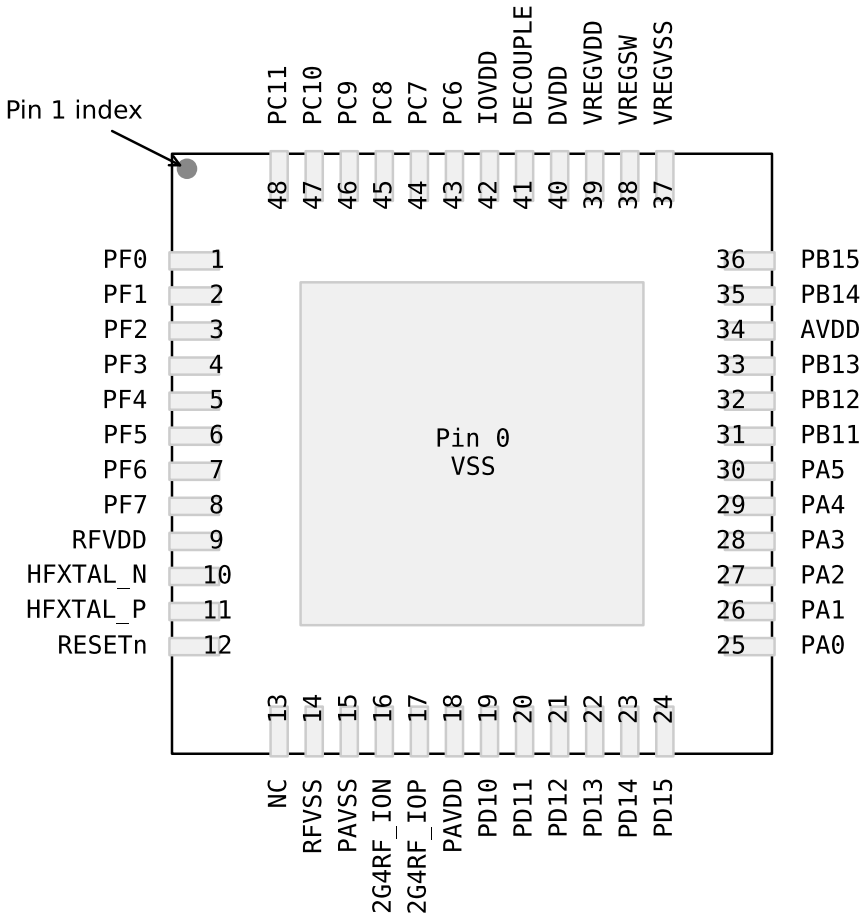


Figure 6.1. EFR32MG1 QFN48 2.4 GHz Pinout

Table 6.1. Device Pinout

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
0	VSS	Ground				
1	PF0	BUSAX [ADC0: APORT1XCH16 ACMP0: APORT1XCH16 ACMP1: APORT1XCH16] BUSBY [ADC0: APORT2YCH16 ACMP0: APORT2YCH16 ACMP1: APORT2YCH16]	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE-TIM0_OUT0 #24 LETIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	FRC_DCLK #24 FRC_DOUT #23 FRC_DFRAME #22 MODEM_DCLK #24 MODEM_DIN #23 MODEM_DOUT #22 MODEM_ANT0 #21 MODEM_ANT1 #20	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0
2	PF1	BUSAY [ADC0: APORT1YCH17 ACMP0: APORT1YCH17 ACMP1: APORT1YCH17] BUSBX [ADC0: APORT2XCH17 ACMP0: APORT2XCH17 ACMP1: APORT2XCH17]	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE-TIM0_OUT0 #25 LETIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	FRC_DCLK #25 FRC_DOUT #24 FRC_DFRAME #23 MODEM_DCLK #25 MODEM_DIN #24 MODEM_DOUT #23 MODEM_ANT0 #22 MODEM_ANT1 #21	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0
3	PF2	BUSAX [ADC0: APORT1XCH18 ACMP0: APORT1XCH18 ACMP1: APORT1XCH18] BUSBY [ADC0: APORT2YCH18 ACMP0: APORT2YCH18 ACMP1: APORT2YCH18]	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE-TIM0_OUT0 #26 LETIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	FRC_DCLK #26 FRC_DOUT #25 FRC_DFRAME #24 MODEM_DCLK #26 MODEM_DIN #25 MODEM_DOUT #24 MODEM_ANT0 #23 MODEM_ANT1 #22	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
4	PF3	BUSAY [ADC0: APORT1YCH19 ACMP0: APORT1YCH19 ACMP1: APORT1YCH19] BUSBX [ADC0: APORT2XCH19 ACMP0: APORT2XCH19 ACMP1: APORT2XCH19]	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LE-TIM0_OUT0 #27 LETIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	FRC_DCLK #27 FRC_DOUT #26 FRC_DFRAME #25 MODEM_DCLK #27 MODEM_DIN #26 MODEM_DOUT #25 MODEM_ANT0 #24 MODEM_ANT1 #23	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI #0
5	PF4	BUSAX [ADC0: APORT1XCH20 ACMP0: APORT1XCH20 ACMP1: APORT1XCH20] BUSBY [ADC0: APORT2YCH20 ACMP0: APORT2YCH20 ACMP1: APORT2YCH20]	TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDTI0 #25 TIM0_CDTI1 #24 TIM0_CDTI2 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 LE-TIM0_OUT0 #28 LETIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27	US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27	FRC_DCLK #28 FRC_DOUT #27 FRC_DFRAME #26 MODEM_DCLK #28 MODEM_DIN #27 MODEM_DOUT #26 MODEM_ANT0 #25 MODEM_ANT1 #24	PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28
6	PF5	BUSAY [ADC0: APORT1YCH21 ACMP0: APORT1YCH21 ACMP1: APORT1YCH21] BUSBX [ADC0: APORT2XCH21 ACMP0: APORT2XCH21 ACMP1: APORT2XCH21]	TIM0_CC0 #29 TIM0_CC1 #28 TIM0_CC2 #27 TIM0_CDTI0 #26 TIM0_CDTI1 #25 TIM0_CDTI2 #24 TIM1_CC0 #29 TIM1_CC1 #28 TIM1_CC2 #27 TIM1_CC3 #26 LE-TIM0_OUT0 #29 LETIM0_OUT1 #28 PCNT0_S0IN #29 PCNT0_S1IN #28	US0_TX #29 US0_RX #28 US0_CLK #27 US0_CS #26 US0_CTS #25 US0_RTS #24 US1_TX #29 US1_RX #28 US1_CLK #27 US1_CS #26 US1_CTS #25 US1_RTS #24 LEU0_TX #29 LEU0_RX #28 I2C0_SDA #29 I2C0_SCL #28	FRC_DCLK #29 FRC_DOUT #28 FRC_DFRAME #27 MODEM_DCLK #29 MODEM_DIN #28 MODEM_DOUT #27 MODEM_ANT0 #26 MODEM_ANT1 #25	PRS_CH0 #5 PRS_CH1 #4 PRS_CH2 #3 PRS_CH3 #2 ACMP0_O #29 ACMP1_O #29

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
7	PF6	BUSAX [ADC0: APORT1XCH22 ACMP0: APORT1XCH22 ACMP1: APORT1XCH22] BUSBY [ADC0: APORT2YCH22 ACMP0: APORT2YCH22 ACMP1: APORT2YCH22]	TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 LE-TIM0_OUT0 #30 LETIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29	US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29	FRC_DCLK #30 FRC_DOUT #29 FRC_DFRAME #28 MODEM_DCLK #30 MODEM_DIN #29 MODEM_DOUT #28 MODEM_ANT0 #27 MODEM_ANT1 #26	CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30
8	PF7	BUSAY [ADC0: APORT1YCH23 ACMP0: APORT1YCH23 ACMP1: APORT1YCH23] BUSBX [ADC0: APORT2XCH23 ACMP0: APORT2XCH23 ACMP1: APORT2XCH23]	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 LE-TIM0_OUT0 #31 LETIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	FRC_DCLK #31 FRC_DOUT #30 FRC_DFRAME #29 MODEM_DCLK #31 MODEM_DIN #30 MODEM_DOUT #29 MODEM_ANT0 #28 MODEM_ANT1 #27	CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1
9	RFVDD	Radio power supply				
10	HFXTAL_N	High Frequency Crystal input pin.				
11	HFXTAL_P	High Frequency Crystal output pin.				
12	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
13	NC	No Connect.				
14	RFVSS	Radio Ground				
15	PAVSS	Power Amplifier (PA) voltage regulator VSS				
16	2G4RF_ION	2.4 GHz Differential RF input/output, negative path.				
17	2G4RF_IOP	2.4 GHz Differential RF input/output, positive path.				
18	PAVDD	Power Amplifier (PA) voltage regulator VDD input				

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
19	PD10	BUSCX [ADC0: APORT3XCH2 ACMP0: APORT3XCH2 ACMP1: APORT3XCH2 IDAC0: APORT1XCH2] BUSDY [ADC0: APORT4YCH2 ACMP0: APORT4YCH2 ACMP1: APORT4YCH2]	TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 LE-TIM0_OUT0 #18 LETIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17	US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17	FRC_DCLK #18 FRC_DOUT #17 FRC_DFRAME #16 MODEM_DCLK #18 MODEM_DIN #17 MODEM_DOUT #16 MODEM_ANT0 #15 MODEM_ANT1 #14	CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18
20	PD11	BUSCY [ADC0: APORT3YCH3 ACMP0: APORT3YCH3 ACMP1: APORT3YCH3 IDAC0: APORT1YCH3] BUSDX [ADC0: APORT4XCH3 ACMP0: APORT4XCH3 ACMP1: APORT4XCH3]	TIM0_CC0 #19 TIM0_CC1 #18 TIM0_CC2 #17 TIM0_CDTI0 #16 TIM0_CDTI1 #15 TIM0_CDTI2 #14 TIM1_CC0 #19 TIM1_CC1 #18 TIM1_CC2 #17 TIM1_CC3 #16 LE-TIM0_OUT0 #19 LETIM0_OUT1 #18 PCNT0_S0IN #19 PCNT0_S1IN #18	US0_TX #19 US0_RX #18 US0_CLK #17 US0_CS #16 US0_CTS #15 US0_RTS #14 US1_TX #19 US1_RX #18 US1_CLK #17 US1_CS #16 US1_CTS #15 US1_RTS #14 LEU0_TX #19 LEU0_RX #18 I2C0_SDA #19 I2C0_SCL #18	FRC_DCLK #19 FRC_DOUT #18 FRC_DFRAME #17 MODEM_DCLK #19 MODEM_DIN #18 MODEM_DOUT #17 MODEM_ANT0 #16 MODEM_ANT1 #15	PRS_CH3 #10 PRS_CH4 #2 PRS_CH5 #1 PRS_CH6 #13 ACMP0_O #19 ACMP1_O #19
21	PD12	BUSCX [ADC0: APORT3XCH4 ACMP0: APORT3XCH4 ACMP1: APORT3XCH4 IDAC0: APORT1XCH4] BUSDY [ADC0: APORT4YCH4 ACMP0: APORT4YCH4 ACMP1: APORT4YCH4]	TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 LE-TIM0_OUT0 #20 LETIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19	US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19	FRC_DCLK #20 FRC_DOUT #19 FRC_DFRAME #18 MODEM_DCLK #20 MODEM_DIN #19 MODEM_DOUT #18 MODEM_ANT0 #17 MODEM_ANT1 #16	PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
22	PD13	BUSCY [ADC0: APORT3YCH5 ACMP0: APORT3YCH5 ACMP1: APORT3YCH5 IDAC0: APORT1YCH5] BUSDX [ADC0: APORT4XCH5 ACMP0: APORT4XCH5 ACMP1: APORT4XCH5]	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 LE-TIM0_OUT0 #21 LETIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	FRC_DCLK #21 FRC_DOUT #20 FRC_DFRAME #19 MODEM_DCLK #21 MODEM_DIN #20 MODEM_DOUT #19 MODEM_ANT0 #18 MODEM_ANT1 #17	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21
23	PD14	BUSCX [ADC0: APORT3XCH6 ACMP0: APORT3XCH6 ACMP1: APORT3XCH6 IDAC0: APORT1XCH6] BUSDY [ADC0: APORT4YCH6 ACMP0: APORT4YCH6 ACMP1: APORT4YCH6]	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 LE-TIM0_OUT0 #22 LETIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	FRC_DCLK #22 FRC_DOUT #21 FRC_DFRAME #20 MODEM_DCLK #22 MODEM_DIN #21 MODEM_DOUT #20 MODEM_ANT0 #19 MODEM_ANT1 #18	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 GPIO_EM4WU4
24	PD15	BUSCY [ADC0: APORT3YCH7 ACMP0: APORT3YCH7 ACMP1: APORT3YCH7 IDAC0: APORT1YCH7] BUSDX [ADC0: APORT4XCH7 ACMP0: APORT4XCH7 ACMP1: APORT4XCH7]	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 LE-TIM0_OUT0 #23 LETIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	FRC_DCLK #23 FRC_DOUT #22 FRC_DFRAME #21 MODEM_DCLK #23 MODEM_DIN #22 MODEM_DOUT #21 MODEM_ANT0 #20 MODEM_ANT1 #19	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 DBG_SWO #2

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
25	PA0	ADC0_EXTN BUSCX [ADC0: APORT3XCH8 ACMP0: APORT3XCH8 ACMP1: APORT3XCH8 IDAC0: APORT1XCH8] BUSDY [ADC0: APORT4YCH8 ACMP0: APORT4YCH8 ACMP1: APORT4YCH8]	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 LE-TIM0_OUT0 #0 LE-TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	FRC_DCLK #0 FRC_DOUT #31 FRC_DFRAME #30 MODEM_DCLK #0 MODEM_DIN #31 MODEM_DOUT #30 MODEM_ANT0 #29 MODEM_ANT1 #28	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0
26	PA1	ADC0_EXTP BUSCY [ADC0: APORT3YCH9 ACMP0: APORT3YCH9 ACMP1: APORT3YCH9 IDAC0: APORT1YCH9] BUSDX [ADC0: APORT4XCH9 ACMP0: APORT4XCH9 ACMP1: APORT4XCH9]	TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 LE-TIM0_OUT0 #1 LE-TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0	US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0	FRC_DCLK #1 FRC_DOUT #0 FRC_DFRAME #31 MODEM_DCLK #1 MODEM_DIN #0 MODEM_DOUT #31 MODEM_ANT0 #30 MODEM_ANT1 #29	CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1
27	PA2	BUSCX [ADC0: APORT3XCH10 ACMP0: APORT3XCH10 ACMP1: APORT3XCH10 IDAC0: APORT1XCH10] BUSDY [ADC0: APORT4YCH10 ACMP0: APORT4YCH10 ACMP1: APORT4YCH10]	TIM0_CC0 #2 TIM0_CC1 #1 TIM0_CC2 #0 TIM0_CDTI0 #31 TIM0_CDTI1 #30 TIM0_CDTI2 #29 TIM1_CC0 #2 TIM1_CC1 #1 TIM1_CC2 #0 TIM1_CC3 #31 LE-TIM0_OUT0 #2 LE-TIM0_OUT1 #1 PCNT0_S0IN #2 PCNT0_S1IN #1	US0_TX #2 US0_RX #1 US0_CLK #0 US0_CS #31 US0_CTS #30 US0_RTS #29 US1_TX #2 US1_RX #1 US1_CLK #0 US1_CS #31 US1_CTS #30 US1_RTS #29 LEU0_TX #2 LEU0_RX #1 I2C0_SDA #2 I2C0_SCL #1	FRC_DCLK #2 FRC_DOUT #1 FRC_DFRAME #0 MODEM_DCLK #2 MODEM_DIN #1 MODEM_DOUT #0 MODEM_ANT0 #31 MODEM_ANT1 #30	PRS_CH6 #2 PRS_CH7 #1 PRS_CH8 #0 PRS_CH9 #10 ACMP0_O #2 ACMP1_O #2

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
28	PA3	BUSCY [ADC0: APORT3YCH11 ACMP0: APORT3YCH11 ACMP1: APORT3YCH11 IDAC0: APORT1YCH11] BUSDX [ADC0: APORT4XCH11 ACMP0: APORT4XCH11 ACMP1: APORT4XCH11]	TIM0_CC0 #3 TIM0_CC1 #2 TIM0_CC2 #1 TIM0_CDTI0 #0 TIM0_CDTI1 #31 TIM0_CDTI2 #30 TIM1_CC0 #3 TIM1_CC1 #2 TIM1_CC2 #1 TIM1_CC3 #0 LE-TIM0_OUT0 #3 LE-TIM0_OUT1 #2 PCNT0_S0IN #3 PCNT0_S1IN #2	US0_TX #3 US0_RX #2 US0_CLK #1 US0_CS #0 US0_CTS #31 US0_RTS #30 US1_TX #3 US1_RX #2 US1_CLK #1 US1_CS #0 US1_CTS #31 US1_RTS #30 LEU0_TX #3 LEU0_RX #2 I2C0_SDA #3 I2C0_SCL #2	FRC_DCLK #3 FRC_DOUT #2 FRC_DFRAME #1 MODEM_DCLK #3 MODEM_DIN #2 MODEM_DOUT #1 MODEM_ANT0 #0 MODEM_ANT1 #31	PRS_CH6 #3 PRS_CH7 #2 PRS_CH8 #1 PRS_CH9 #0 ACMP0_O #3 ACMP1_O #3 GPIO_EM4WU8
29	PA4	BUSCX [ADC0: APORT3XCH12 ACMP0: APORT3XCH12 ACMP1: APORT3XCH12 IDAC0: APORT1XCH12] BUSDY [ADC0: APORT4YCH12 ACMP0: APORT4YCH12 ACMP1: APORT4YCH12]	TIM0_CC0 #4 TIM0_CC1 #3 TIM0_CC2 #2 TIM0_CDTI0 #1 TIM0_CDTI1 #0 TIM0_CDTI2 #31 TIM1_CC0 #4 TIM1_CC1 #3 TIM1_CC2 #2 TIM1_CC3 #1 LE-TIM0_OUT0 #4 LE-TIM0_OUT1 #3 PCNT0_S0IN #4 PCNT0_S1IN #3	US0_TX #4 US0_RX #3 US0_CLK #2 US0_CS #1 US0_CTS #0 US0_RTS #31 US1_TX #4 US1_RX #3 US1_CLK #2 US1_CS #1 US1_CTS #0 US1_RTS #31 LEU0_TX #4 LEU0_RX #3 I2C0_SDA #4 I2C0_SCL #3	FRC_DCLK #4 FRC_DOUT #3 FRC_DFRAME #2 MODEM_DCLK #4 MODEM_DIN #3 MODEM_DOUT #2 MODEM_ANT0 #1 MODEM_ANT1 #0	PRS_CH6 #4 PRS_CH7 #3 PRS_CH8 #2 PRS_CH9 #1 ACMP0_O #4 ACMP1_O #4
30	PA5	BUSCY [ADC0: APORT3YCH13 ACMP0: APORT3YCH13 ACMP1: APORT3YCH13 IDAC0: APORT1YCH13] BUSDX [ADC0: APORT4XCH13 ACMP0: APORT4XCH13 ACMP1: APORT4XCH13]	TIM0_CC0 #5 TIM0_CC1 #4 TIM0_CC2 #3 TIM0_CDTI0 #2 TIM0_CDTI1 #1 TIM0_CDTI2 #0 TIM1_CC0 #5 TIM1_CC1 #4 TIM1_CC2 #3 TIM1_CC3 #2 LE-TIM0_OUT0 #5 LE-TIM0_OUT1 #4 PCNT0_S0IN #5 PCNT0_S1IN #4	US0_TX #5 US0_RX #4 US0_CLK #3 US0_CS #2 US0_CTS #1 US0_RTS #0 US1_TX #5 US1_RX #4 US1_CLK #3 US1_CS #2 US1_CTS #1 US1_RTS #0 LEU0_TX #5 LEU0_RX #4 I2C0_SDA #5 I2C0_SCL #4	FRC_DCLK #5 FRC_DOUT #4 FRC_DFRAME #3 MODEM_DCLK #5 MODEM_DIN #4 MODEM_DOUT #3 MODEM_ANT0 #2 MODEM_ANT1 #1	PRS_CH6 #5 PRS_CH7 #4 PRS_CH8 #3 PRS_CH9 #2 ACMP0_O #5 ACMP1_O #5

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
31	PB11	BUSCY [ADC0: APORT3YCH27 ACMP0: APORT3YCH27 ACMP1: APORT3YCH27 IDAC0: APORT1YCH27] BUSDX [ADC0: APORT4XCH27 ACMP0: APORT4XCH27 ACMP1: APORT4XCH27]	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 LE-TIM0_OUT0 #6 LE-TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	FRC_DCLK #6 FRC_DOUT #5 FRC_DFRAME #4 MODEM_DCLK #6 MODEM_DIN #5 MODEM_DOUT #4 MODEM_ANT0 #3 MODEM_ANT1 #2	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6
32	PB12	BUSCX [ADC0: APORT3XCH28 ACMP0: APORT3XCH28 ACMP1: APORT3XCH28 IDAC0: APORT1XCH28] BUSDY [ADC0: APORT4YCH28 ACMP0: APORT4YCH28 ACMP1: APORT4YCH28]	TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 LE-TIM0_OUT0 #7 LE-TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6	US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6	FRC_DCLK #7 FRC_DOUT #6 FRC_DFRAME #5 MODEM_DCLK #7 MODEM_DIN #6 MODEM_DOUT #5 MODEM_ANT0 #4 MODEM_ANT1 #3	PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7
33	PB13	BUSCY [ADC0: APORT3YCH29 ACMP0: APORT3YCH29 ACMP1: APORT3YCH29 IDAC0: APORT1YCH29] BUSDX [ADC0: APORT4XCH29 ACMP0: APORT4XCH29 ACMP1: APORT4XCH29]	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 LE-TIM0_OUT0 #8 LE-TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	FRC_DCLK #8 FRC_DOUT #7 FRC_DFRAME #6 MODEM_DCLK #8 MODEM_DIN #7 MODEM_DOUT #6 MODEM_ANT0 #5 MODEM_ANT1 #4	PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9
34	AVDD	Analog power supply.				

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
35	PB14	LFXTAL_N BUSCX [ADC0: APORT3XCH30 ACMP0: APORT3XCH30 ACMP1: APORT3XCH30 IDAC0: APORT1XCH30] BUSDY [ADC0: APORT4YCH30 ACMP0: APORT4YCH30 ACMP1: APORT4YCH30]	TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 LE-TIM0_OUT0 #9 LE-TIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8	US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8	FRC_DCLK #9 FRC_DOUT #8 FRC_DFRAME #7 MODEM_DCLK #9 MODEM_DIN #8 MODEM_DOUT #7 MODEM_ANT0 #6 MODEM_ANT1 #5	CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9
36	PB15	LFXTAL_P BUSCY [ADC0: APORT3YCH31 ACMP0: APORT3YCH31 ACMP1: APORT3YCH31 IDAC0: APORT1YCH31] BUSDX [ADC0: APORT4XCH31 ACMP0: APORT4XCH31 ACMP1: APORT4XCH31]	TIM0_CC0 #10 TIM0_CC1 #9 TIM0_CC2 #8 TIM0_CDTI0 #7 TIM0_CDTI1 #6 TIM0_CDTI2 #5 TIM1_CC0 #10 TIM1_CC1 #9 TIM1_CC2 #8 TIM1_CC3 #7 LE-TIM0_OUT0 #10 LETIM0_OUT1 #9 PCNT0_S0IN #10 PCNT0_S1IN #9	US0_TX #10 US0_RX #9 US0_CLK #8 US0_CS #7 US0_CTS #6 US0_RTS #5 US1_TX #10 US1_RX #9 US1_CLK #8 US1_CS #7 US1_CTS #6 US1_RTS #5 LEU0_TX #10 LEU0_RX #9 I2C0_SDA #10 I2C0_SCL #9	FRC_DCLK #10 FRC_DOUT #9 FRC_DFRAME #8 MODEM_DCLK #10 MODEM_DIN #9 MODEM_DOUT #8 MODEM_ANT0 #7 MODEM_ANT1 #6	CMU_CLK0 #1 PRS_CH6 #10 PRS_CH7 #9 PRS_CH8 #8 PRS_CH9 #7 ACMP0_O #10 ACMP1_O #10
37	VREGVSS	Voltage regulator VSS				
38	VREGSW	DCDC regulator switching node				
39	VREGVDD	Voltage regulator VDD input				
40	DVDD	Digital power supply.				
41	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
42	IOVDD	Digital IO power supply.				

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
43	PC6	BUSAX [ADC0: APORT1XCH6 ACMP0: APORT1XCH6 ACMP1: APORT1XCH6] BUSBY [ADC0: APORT2YCH6 ACMP0: APORT2YCH6 ACMP1: APORT2YCH6]	TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 LE-TIM0_OUT0 #11 LETIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10	US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10	FRC_DCLK #11 FRC_DOUT #10 FRC_DFRAME #9 MODEM_DCLK #11 MODEM_DIN #10 MODEM_DOUT #9 MODEM_ANT0 #8 MODEM_ANT1 #7	CMU_CLK0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11
44	PC7	BUSAY [ADC0: APORT1YCH7 ACMP0: APORT1YCH7 ACMP1: APORT1YCH7] BUSBX [ADC0: APORT2XCH7 ACMP0: APORT2XCH7 ACMP1: APORT2XCH7]	TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 LE-TIM0_OUT0 #12 LETIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11	US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11	FRC_DCLK #12 FRC_DOUT #11 FRC_DFRAME #10 MODEM_DCLK #12 MODEM_DIN #11 MODEM_DOUT #10 MODEM_ANT0 #9 MODEM_ANT1 #8	CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12
45	PC8	BUSAX [ADC0: APORT1XCH8 ACMP0: APORT1XCH8 ACMP1: APORT1XCH8] BUSBY [ADC0: APORT2YCH8 ACMP0: APORT2YCH8 ACMP1: APORT2YCH8]	TIM0_CC0 #13 TIM0_CC1 #12 TIM0_CC2 #11 TIM0_CDTI0 #10 TIM0_CDTI1 #9 TIM0_CDTI2 #8 TIM1_CC0 #13 TIM1_CC1 #12 TIM1_CC2 #11 TIM1_CC3 #10 LE-TIM0_OUT0 #13 LETIM0_OUT1 #12 PCNT0_S0IN #13 PCNT0_S1IN #12	US0_TX #13 US0_RX #12 US0_CLK #11 US0_CS #10 US0_CTS #9 US0_RTS #8 US1_TX #13 US1_RX #12 US1_CLK #11 US1_CS #10 US1_CTS #9 US1_RTS #8 LEU0_TX #13 LEU0_RX #12 I2C0_SDA #13 I2C0_SCL #12	FRC_DCLK #13 FRC_DOUT #12 FRC_DFRAME #11 MODEM_DCLK #13 MODEM_DIN #12 MODEM_DOUT #11 MODEM_ANT0 #10 MODEM_ANT1 #9	PRS_CH0 #10 PRS_CH9 #13 PRS_CH10 #2 PRS_CH11 #1 ACMP0_O #13 ACMP1_O #13

QFN48 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
46	PC9	BUSAY [ADC0: APORT1YCH9 ACMP0: APORT1YCH9 ACMP1: APORT1YCH9] BUSBX [ADC0: APORT2XCH9 ACMP0: APORT2XCH9 ACMP1: APORT2XCH9]	TIM0_CC0 #14 TIM0_CC1 #13 TIM0_CC2 #12 TIM0_CDTI0 #11 TIM0_CDTI1 #10 TIM0_CDTI2 #9 TIM1_CC0 #14 TIM1_CC1 #13 TIM1_CC2 #12 TIM1_CC3 #11 LE-TIM0_OUT0 #14 LETIM0_OUT1 #13 PCNT0_S0IN #14 PCNT0_S1IN #13	US0_TX #14 US0_RX #13 US0_CLK #12 US0_CS #11 US0_CTS #10 US0_RTS #9 US1_TX #14 US1_RX #13 US1_CLK #12 US1_CS #11 US1_CTS #10 US1_RTS #9 LEU0_TX #14 LEU0_RX #13 I2C0_SDA #14 I2C0_SCL #13	FRC_DCLK #14 FRC_DOUT #13 FRC_DFRAME #12 MODEM_DCLK #14 MODEM_DIN #13 MODEM_DOUT #12 MODEM_ANT0 #11 MODEM_ANT1 #10	PRS_CH0 #11 PRS_CH9 #14 PRS_CH10 #3 PRS_CH11 #2 ACMP0_O #14 ACMP1_O #14
47	PC10	BUSAX [ADC0: APORT1XCH10 ACMP0: APORT1XCH10 ACMP1: APORT1XCH10] BUSBY [ADC0: APORT2YCH10 ACMP0: APORT2YCH10 ACMP1: APORT2YCH10]	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE-TIM0_OUT0 #15 LETIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14	FRC_DCLK #15 FRC_DOUT #14 FRC_DFRAME #13 MODEM_DCLK #15 MODEM_DIN #14 MODEM_DOUT #13 MODEM_ANT0 #12 MODEM_ANT1 #11	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12
48	PC11	BUSAY [ADC0: APORT1YCH11 ACMP0: APORT1YCH11 ACMP1: APORT1YCH11] BUSBX [ADC0: APORT2XCH11 ACMP0: APORT2XCH11 ACMP1: APORT2XCH11]	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE-TIM0_OUT0 #16 LETIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15	FRC_DCLK #16 FRC_DOUT #15 FRC_DFRAME #14 MODEM_DCLK #16 MODEM_DIN #15 MODEM_DOUT #14 MODEM_ANT0 #13 MODEM_ANT1 #12	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3

6.1.1 EFR32MG1 QFN48 2.4 GHz GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters A through F, and the individual pins on each port are indicated by a number from 15 down to 0.

Table 6.2. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	PA5 (5V)	PA4 (5V)	PA3 (5V)	PA2 (5V)	PA1	PA0
Port B	PB15	PB14	PB13 (5V)	PB12 (5V)	PB11 (5V)	-	-	-	-	-	-	-	-	-	-	-
Port C	-	-	-	-	PC11 (5V)	PC10 (5V)	PC9 (5V)	PC8 (5V)	PC7 (5V)	PC6 (5V)	-	-	-	-	-	-
Port D	PD15 (5V)	PD14 (5V)	PD13 (5V)	PD12 (5V)	PD11 (5V)	PD10 (5V)	-	-	-	-	-	-	-	-	-	-
Port E	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	PF7 (5V)	PF6 (5V)	PF5 (5V)	PF4 (5V)	PF3 (5V)	PF2 (5V)	PF1 (5V)	PF0 (5V)

6.2 EFR32MG1 QFN32 2.4 GHz Definition

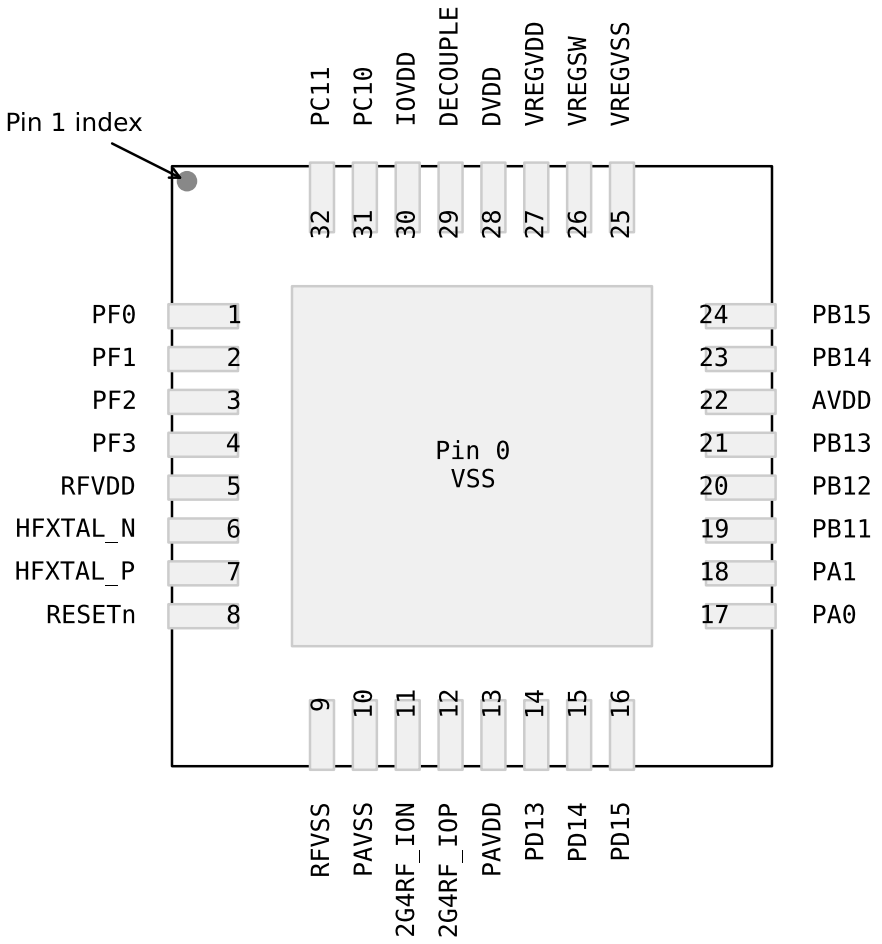


Figure 6.2. EFR32MG1 QFN32 2.4 GHz Pinout

Table 6.3. Device Pinout

QFN32 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
0	VSS	Ground				
1	PF0	BUSAX [ADC0: APORT1XCH16 ACMP0: APORT1XCH16 ACMP1: APORT1XCH16] BUSBY [ADC0: APORT2YCH16 ACMP0: APORT2YCH16 ACMP1: APORT2YCH16]	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 LE-TIM0_OUT0 #24 LETIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	FRC_DCLK #24 FRC_DOUT #23 FRC_DFRAME #22 MODEM_DCLK #24 MODEM_DIN #23 MODEM_DOUT #22 MODEM_ANT0 #21 MODEM_ANT1 #20	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK #0
2	PF1	BUSAY [ADC0: APORT1YCH17 ACMP0: APORT1YCH17 ACMP1: APORT1YCH17] BUSBX [ADC0: APORT2XCH17 ACMP0: APORT2XCH17 ACMP1: APORT2XCH17]	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 LE-TIM0_OUT0 #25 LETIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	FRC_DCLK #25 FRC_DOUT #24 FRC_DFRAME #23 MODEM_DCLK #25 MODEM_DIN #24 MODEM_DOUT #23 MODEM_ANT0 #22 MODEM_ANT1 #21	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS #0
3	PF2	BUSAX [ADC0: APORT1XCH18 ACMP0: APORT1XCH18 ACMP1: APORT1XCH18] BUSBY [ADC0: APORT2YCH18 ACMP0: APORT2YCH18 ACMP1: APORT2YCH18]	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 LE-TIM0_OUT0 #26 LETIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	FRC_DCLK #26 FRC_DOUT #25 FRC_DFRAME #24 MODEM_DCLK #26 MODEM_DIN #25 MODEM_DOUT #24 MODEM_ANT0 #23 MODEM_ANT1 #22	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO #0 DBG_SWO #0 GPIO_EM4WU0

QFN32 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
4	PF3	BUSAY [ADC0: APORT1YCH19 ACMP0: APORT1YCH19 ACMP1: APORT1YCH19] BUSBX [ADC0: APORT2XCH19 ACMP0: APORT2XCH19 ACMP1: APORT2XCH19]	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 LE-TIM0_OUT0 #27 LETIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	FRC_DCLK #27 FRC_DOUT #26 FRC_DFRAME #25 MODEM_DCLK #27 MODEM_DIN #26 MODEM_DOUT #25 MODEM_ANT0 #24 MODEM_ANT1 #23	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI #0
5	RFVDD	Radio power supply				
6	HFXTAL_N	High Frequency Crystal input pin.				
7	HFXTAL_P	High Frequency Crystal output pin.				
8	RESETn	Reset input, active low.To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
9	RFVSS	Radio Ground				
10	PAVSS	Power Amplifier (PA) voltage regulator VSS				
11	2G4RF_ION	2.4 GHz Differential RF input/output, negative path.				
12	2G4RF_IOP	2.4 GHz Differential RF input/output, positive path.				
13	PAVDD	Power Amplifier (PA) voltage regulator VDD input				
14	PD13	BUSCY [ADC0: APORT3YCH5 ACMP0: APORT3YCH5 ACMP1: APORT3YCH5 IDAC0: APORT1YCH5] BUSDX [ADC0: APORT4XCH5 ACMP0: APORT4XCH5 ACMP1: APORT4XCH5]	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 LE-TIM0_OUT0 #21 LETIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	FRC_DCLK #21 FRC_DOUT #20 FRC_DFRAME #19 MODEM_DCLK #21 MODEM_DIN #20 MODEM_DOUT #19 MODEM_ANT0 #18 MODEM_ANT1 #17	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21

QFN32 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
15	PD14	BUSCX [ADC0: APORT3XCH6 ACMP0: APORT3XCH6 ACMP1: APORT3XCH6 IDAC0: APORT1XCH6] BUSDY [ADC0: APORT4YCH6 ACMP0: APORT4YCH6 ACMP1: APORT4YCH6]	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 LE-TIM0_OUT0 #22 LETIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	FRC_DCLK #22 FRC_DOUT #21 FRC_DFRAME #20 MODEM_DCLK #22 MODEM_DIN #21 MODEM_DOUT #20 MODEM_ANT0 #19 MODEM_ANT1 #18	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 GPIO_EM4WU4
16	PD15	BUSCY [ADC0: APORT3YCH7 ACMP0: APORT3YCH7 ACMP1: APORT3YCH7 IDAC0: APORT1YCH7] BUSDX [ADC0: APORT4XCH7 ACMP0: APORT4XCH7 ACMP1: APORT4XCH7]	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 LE-TIM0_OUT0 #23 LETIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	FRC_DCLK #23 FRC_DOUT #22 FRC_DFRAME #21 MODEM_DCLK #23 MODEM_DIN #22 MODEM_DOUT #21 MODEM_ANT0 #20 MODEM_ANT1 #19	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 DBG_SWO #2
17	PA0	ADC0_EXTN BUSCX [ADC0: APORT3XCH8 ACMP0: APORT3XCH8 ACMP1: APORT3XCH8 IDAC0: APORT1XCH8] BUSDY [ADC0: APORT4YCH8 ACMP0: APORT4YCH8 ACMP1: APORT4YCH8]	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 LE-TIM0_OUT0 #0 LE-TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	FRC_DCLK #0 FRC_DOUT #31 FRC_DFRAME #30 MODEM_DCLK #0 MODEM_DIN #31 MODEM_DOUT #30 MODEM_ANT0 #29 MODEM_ANT1 #28	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0

QFN32 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
18	PA1	ADC0_EXTP BUSCY [ADC0: APORT3YCH9 ACMP0: APORT3YCH9 ACMP1: APORT3YCH9 IDAC0: APORT1YCH9] BUSDX [ADC0: APORT4XCH9 ACMP0: APORT4XCH9 ACMP1: APORT4XCH9]	TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDTI0 #30 TIM0_CDTI1 #29 TIM0_CDTI2 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 LE-TIM0_OUT0 #1 LE-TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0	US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0	FRC_DCLK #1 FRC_DOUT #0 FRC_DFRAME #31 MODEM_DCLK #1 MODEM_DIN #0 MODEM_DOUT #31 MODEM_ANT0 #30 MODEM_ANT1 #29	CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1
19	PB11	BUSCY [ADC0: APORT3YCH27 ACMP0: APORT3YCH27 ACMP1: APORT3YCH27 IDAC0: APORT1YCH27] BUSDX [ADC0: APORT4XCH27 ACMP0: APORT4XCH27 ACMP1: APORT4XCH27]	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 LE-TIM0_OUT0 #6 LE-TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	FRC_DCLK #6 FRC_DOUT #5 FRC_DFRAME #4 MODEM_DCLK #6 MODEM_DIN #5 MODEM_DOUT #4 MODEM_ANT0 #3 MODEM_ANT1 #2	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6
20	PB12	BUSCX [ADC0: APORT3XCH28 ACMP0: APORT3XCH28 ACMP1: APORT3XCH28 IDAC0: APORT1XCH28] BUSDY [ADC0: APORT4YCH28 ACMP0: APORT4YCH28 ACMP1: APORT4YCH28]	TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 LE-TIM0_OUT0 #7 LE-TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6	US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6	FRC_DCLK #7 FRC_DOUT #6 FRC_DFRAME #5 MODEM_DCLK #7 MODEM_DIN #6 MODEM_DOUT #5 MODEM_ANT0 #4 MODEM_ANT1 #3	PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7

QFN32 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
21	PB13	BUSCY [ADC0: APORT3YCH29 ACMP0: APORT3YCH29 ACMP1: APORT3YCH29 IDAC0: APORT1YCH29] BUSDX [ADC0: APORT4XCH29 ACMP0: APORT4XCH29 ACMP1: APORT4XCH29]	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 LE-TIM0_OUT0 #8 LE-TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	FRC_DCLK #8 FRC_DOUT #7 FRC_DFRAME #6 MODEM_DCLK #8 MODEM_DIN #7 MODEM_DOUT #6 MODEM_ANT0 #5 MODEM_ANT1 #4	PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9
22	AVDD	Analog power supply.				
23	PB14	LFXTAL_N BUSCX [ADC0: APORT3XCH30 ACMP0: APORT3XCH30 ACMP1: APORT3XCH30 IDAC0: APORT1XCH30] BUSDY [ADC0: APORT4YCH30 ACMP0: APORT4YCH30 ACMP1: APORT4YCH30]	TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 LE-TIM0_OUT0 #9 LE-TIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8	US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8	FRC_DCLK #9 FRC_DOUT #8 FRC_DFRAME #7 MODEM_DCLK #9 MODEM_DIN #8 MODEM_DOUT #7 MODEM_ANT0 #6 MODEM_ANT1 #5	CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9
24	PB15	LFXTAL_P BUSCY [ADC0: APORT3YCH31 ACMP0: APORT3YCH31 ACMP1: APORT3YCH31 IDAC0: APORT1YCH31] BUSDX [ADC0: APORT4XCH31 ACMP0: APORT4XCH31 ACMP1: APORT4XCH31]	TIM0_CC0 #10 TIM0_CC1 #9 TIM0_CC2 #8 TIM0_CDTI0 #7 TIM0_CDTI1 #6 TIM0_CDTI2 #5 TIM1_CC0 #10 TIM1_CC1 #9 TIM1_CC2 #8 TIM1_CC3 #7 LE-TIM0_OUT0 #10 LETIM0_OUT1 #9 PCNT0_S0IN #10 PCNT0_S1IN #9	US0_TX #10 US0_RX #9 US0_CLK #8 US0_CS #7 US0_CTS #6 US0_RTS #5 US1_TX #10 US1_RX #9 US1_CLK #8 US1_CS #7 US1_CTS #6 US1_RTS #5 LEU0_TX #10 LEU0_RX #9 I2C0_SDA #10 I2C0_SCL #9	FRC_DCLK #10 FRC_DOUT #9 FRC_DFRAME #8 MODEM_DCLK #10 MODEM_DIN #9 MODEM_DOUT #8 MODEM_ANT0 #7 MODEM_ANT1 #6	CMU_CLK0 #1 PRS_CH6 #10 PRS_CH7 #9 PRS_CH8 #8 PRS_CH9 #7 ACMP0_O #10 ACMP1_O #10
25	VREGVSS	Voltage regulator VSS				
26	VREGSW	DCDC regulator switching node				
27	VREGVDD	Voltage regulator VDD input				
28	DVDD	Digital power supply.				

QFN32 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	Timers	Communication	Radio	Other
29	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.				
30	IOVDD	Digital IO power supply.				
31	PC10	BUSAX [ADC0: APORT1XCH10 ACMP0: APORT1XCH10 ACMP1: APORT1XCH10] BUSBY [ADC0: APORT2YCH10 ACMP0: APORT2YCH10 ACMP1: APORT2YCH10]	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 LE-TIM0_OUT0 #15 LETIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14	FRC_DCLK #15 FRC_DOUT #14 FRC_DFRAME #13 MODEM_DCLK #15 MODEM_DIN #14 MODEM_DOUT #13 MODEM_ANT0 #12 MODEM_ANT1 #11	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 GPIO_EM4WU12
32	PC11	BUSAY [ADC0: APORT1YCH11 ACMP0: APORT1YCH11 ACMP1: APORT1YCH11] BUSBX [ADC0: APORT2XCH11 ACMP0: APORT2XCH11 ACMP1: APORT2XCH11]	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 LE-TIM0_OUT0 #16 LETIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15	FRC_DCLK #16 FRC_DOUT #15 FRC_DFRAME #14 MODEM_DCLK #16 MODEM_DIN #15 MODEM_DOUT #14 MODEM_ANT0 #13 MODEM_ANT1 #12	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3

6.2.1 EFR32MG1 QFN32 2.4 GHz GPIO Overview

The GPIO pins are organized as 16-bit ports indicated by letters A through F, and the individual pins on each port are indicated by a number from 15 down to 0.

Table 6.4. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PA1	PA0
Port B	PB15	PB14	PB13 (5V)	PB12 (5V)	PB11 (5V)	-	-	-	-	-	-	-	-	-	-	-
Port C	-	-	-	-	PC11 (5V)	PC10 (5V)	-	-	-	-	-	-	-	-	-	-
Port D	PD15 (5V)	PD14 (5V)	PD13 (5V)	-	-	-	-	-	-	-	-	-	-	-	-	-
Port E	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port F	-	-	-	-	-	-	-	-	-	-	-	-	PF3 (5V)	PF2 (5V)	PF1 (5V)	PF0 (5V)

6.3 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.
Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 6.5. Alternate functionality overview

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
ACMP0_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP0, digital output.
ACMP1_O	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Analog comparator ACMP1, digital output.
ADC0_EXTN	0: PA0								Analog to digital converter ADC0 external reference input negative pin
ADC0_EXTP	0: PA1								Analog to digital converter ADC0 external reference input positive pin
CMU_CLK0	0: PA1 1: PB15 2: PC6 3: PC11	5: PD14 6: PF2 7: PF7							Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA0 1: PB14 2: PC7 3: PC10	4: PD10 5: PD15 6: PF3 7: PF6							Clock Management Unit, clock output number 1.
DBG_SWCLKTCK	0: PF0								Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1								Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
DBG_SWO	0: PF2 1: PB13 2: PD15 3: PC11								Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
DBG_TDI	0: PF3								Debug-interface JTAG Test Data In. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_TDO	0: PF2								Debug-interface JTAG Test Data Out. Note that this function is enabled to pin out of reset.
FRC_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Frame Controller, Data Sniffer Clock.
FRC_DFRAME	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Frame Controller, Data Sniffer Frame active
FRC_DOUT	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Frame Controller, Data Sniffer Output.
GPIO_EM4WU0	0: PF2								Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PF7								Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PD14								Pin can be used to wake the system up from EM4
GPIO_EM4WU8	0: PA3								Pin can be used to wake the system up from EM4

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
GPIO_EM4WU9	0: PB13								Pin can be used to wake the system up from EM4
GPIO_EM4WU12	0: PC10								Pin can be used to wake the system up from EM4
I2C0_SCL	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	I2C0 Serial Clock Line input / output.
I2C0_SDA	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	I2C0 Serial Data input / output.
LETIM0_OUT0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Low Energy Timer LETIM0, output channel 1.
LEU0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	LEUART0 Receive input.
LEU0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	0: PB14								Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	0: PB15								Low Frequency Crystal (typically 32.768 kHz) positive pin.
MODEM_ANT0	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	MODEM antenna control output 0, used for antenna diversity.
MODEM_ANT1	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	MODEM antenna control output 1, used for antenna diversity.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
MODEM_DCLK	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	MODEM data clock out.
MODEM_DIN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	MODEM data in.
MODEM_DOUT	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	MODEM data out.
PCNT0_S0IN	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Pulse Counter PCNT0 input number 1.
PRS_CH0	0: PF0 1: PF1 2: PF2 3: PF3	4: PF4 5: PF5 6: PF6 7: PF7	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11					Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PF1 1: PF2 2: PF3 3: PF4	4: PF5 5: PF6 6: PF7 7: PF0							Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PF2 1: PF3 2: PF4 3: PF5	4: PF6 5: PF7 6: PF0 7: PF1							Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PF3 1: PF4 2: PF5 3: PF6	4: PF7 5: PF0 6: PF1 7: PF2	9: PD10 10: PD11 11: PD12	12: PD13 13: PD14 14: PD15					Peripheral Reflex System PRS, channel 3.
PRS_CH4	1: PD10 2: PD11 3: PD12	4: PD13 5: PD14 6: PD15							Peripheral Reflex System PRS, channel 4.
PRS_CH5	0: PD10 1: PD11 2: PD12 3: PD13	4: PD14 5: PD15							Peripheral Reflex System PRS, channel 5.
PRS_CH6	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15	12: PD10 13: PD11 14: PD12 15: PD13	16: PD14 17: PD15				Peripheral Reflex System PRS, channel 6.
PRS_CH7	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PA0						Peripheral Reflex System PRS, channel 7.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PRS_CH8	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PA0 10: PA1						Peripheral Reflex System PRS, channel 8.
PRS_CH9	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PA0 9: PA1 10: PA2 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11				Peripheral Reflex System PRS, channel 9.
PRS_CH10	0: PC6 1: PC7 2: PC8 3: PC9	4: PC10 5: PC11							Peripheral Reflex System PRS, channel 10.
PRS_CH11	0: PC7 1: PC8 2: PC9 3: PC10	4: PC11 5: PC6							Peripheral Reflex System PRS, channel 11.
TIM0_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDTI2	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 1 Capture Compare input / output channel 2.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
TIM1_CC3	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 1 Capture Compare input / output channel 3.
US0_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART0 clock input / output.
US0_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART0 chip select input / output.
US0_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART0 Request To Send hardware flow control output.
US0_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	USART1 clock input / output.
US1_CS	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	USART1 chip select input / output.
US1_CTS	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	USART1 Clear To Send hardware flow control input.
US1_RTS	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART1 Request To Send hardware flow control output.

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US1_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).

6.4 Analog Port (APORT)

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, and DACs. The APORT consists of wires, switches, and control needed to configurably implement the routes. Please see the device Reference Manual for a complete description.

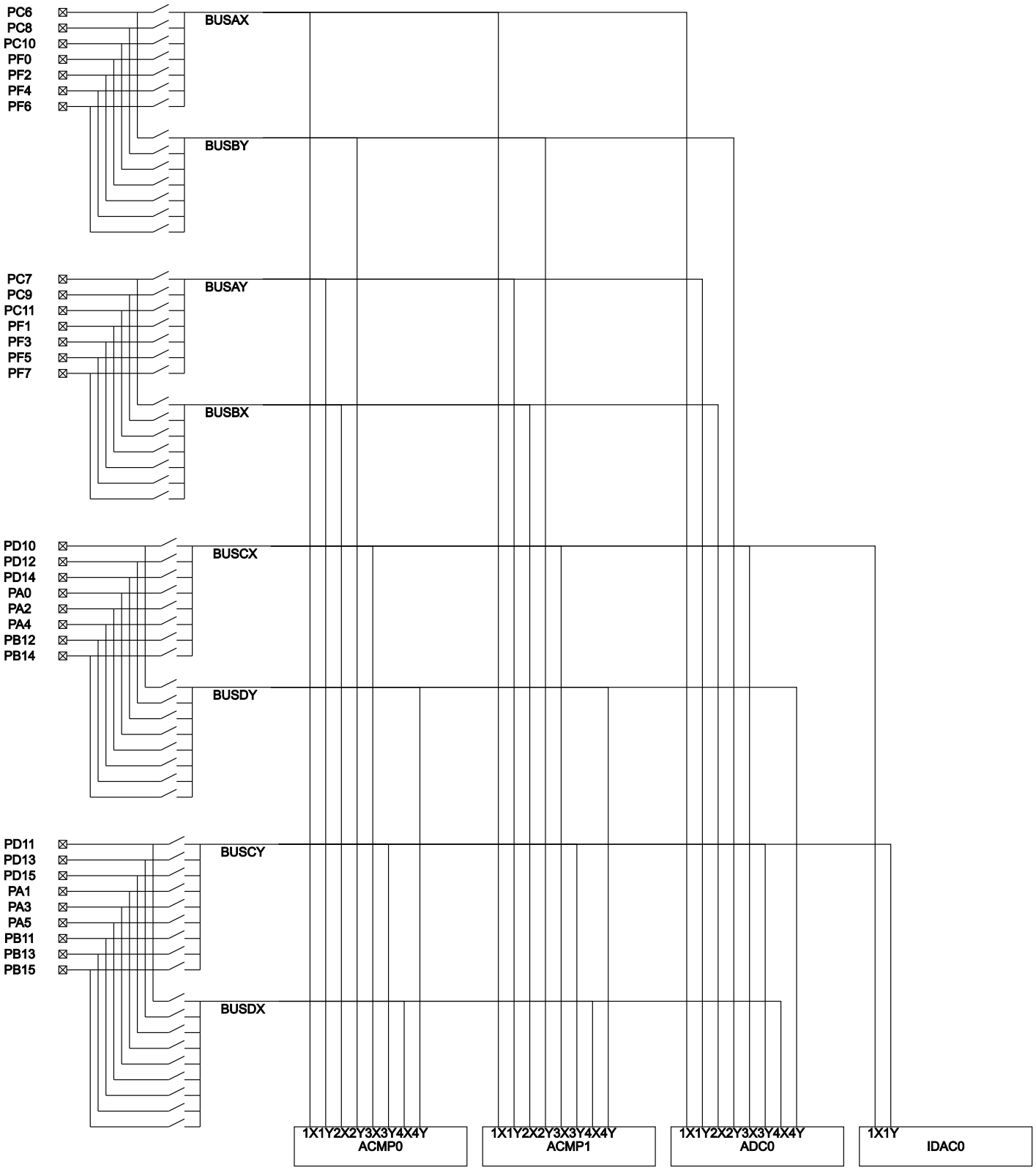


Figure 6.3. EFR32MG1 APORT

Table 6.6. APORT Client Map

Analog Module	Analog Module Channel	Shared Bus	Pin
ACMP0	APORT1XCH6	BUSAX	PC6
	APORT1XCH8		PC8
	APORT1XCH10		PC10
	APORT1XCH16		PF0
	APORT1XCH18		PF2
	APORT1XCH20		PF4
	APORT1XCH22		PF6
ACMP0	APORT1YCH7	BUSAY	PC7
	APORT1YCH9		PC9
	APORT1YCH11		PC11
	APORT1YCH17		PF1
	APORT1YCH19		PF3
	APORT1YCH21		PF5
	APORT1YCH23		PF7
ACMP0	APORT2XCH7	BUSBX	PC7
	APORT2XCH9		PC9
	APORT2XCH11		PC11
	APORT2XCH17		PF1
	APORT2XCH19		PF3
	APORT2XCH21		PF5
	APORT2XCH23		PF7
ACMP0	APORT2YCH6	BUSBY	PC6
	APORT2YCH8		PC8
	APORT2YCH10		PC10
	APORT2YCH16		PF0
	APORT2YCH18		PF2
	APORT2YCH20		PF4
	APORT2YCH22		PF6

Analog Module	Analog Module Channel	Shared Bus	Pin
ACMP0	APORT3XCH2	BUSCX	PD10
	APORT3XCH4		PD12
	APORT3XCH6		PD14
	APORT3XCH8		PA0
	APORT3XCH10		PA2
	APORT3XCH12		PA4
	APORT3XCH28		PB12
	APORT3XCH30		PB14
ACMP0	APORT3YCH3	BUSCY	PD11
	APORT3YCH5		PD13
	APORT3YCH7		PD15
	APORT3YCH9		PA1
	APORT3YCH11		PA3
	APORT3YCH13		PA5
	APORT3YCH27		PB11
	APORT3YCH29		PB13
	APORT3YCH31		PB15
ACMP0	APORT4XCH3	BUSDX	PD11
	APORT4XCH5		PD13
	APORT4XCH7		PD15
	APORT4XCH9		PA1
	APORT4XCH11		PA3
	APORT4XCH13		PA5
	APORT4XCH27		PB11
	APORT4XCH29		PB13
	APORT4XCH31		PB15
ACMP0	APORT4YCH2	BUSDY	PD10
	APORT4YCH4		PD12
	APORT4YCH6		PD14
	APORT4YCH8		PA0
	APORT4YCH10		PA2
	APORT4YCH12		PA4
	APORT4YCH28		PB12
	APORT4YCH30		PB14

Analog Module	Analog Module Channel	Shared Bus	Pin
ACMP1	APORT1XCH6	BUSAX	PC6
	APORT1XCH8		PC8
	APORT1XCH10		PC10
	APORT1XCH16		PF0
	APORT1XCH18		PF2
	APORT1XCH20		PF4
	APORT1XCH22		PF6
ACMP1	APORT1YCH7	BUSAY	PC7
	APORT1YCH9		PC9
	APORT1YCH11		PC11
	APORT1YCH17		PF1
	APORT1YCH19		PF3
	APORT1YCH21		PF5
	APORT1YCH23		PF7
ACMP1	APORT2XCH7	BUSBX	PC7
	APORT2XCH9		PC9
	APORT2XCH11		PC11
	APORT2XCH17		PF1
	APORT2XCH19		PF3
	APORT2XCH21		PF5
	APORT2XCH23		PF7
ACMP1	APORT2YCH6	BUSBY	PC6
	APORT2YCH8		PC8
	APORT2YCH10		PC10
	APORT2YCH16		PF0
	APORT2YCH18		PF2
	APORT2YCH20		PF4
	APORT2YCH22		PF6
ACMP1	APORT3XCH2	BUSCX	PD10
	APORT3XCH4		PD12
	APORT3XCH6		PD14
	APORT3XCH8		PA0
	APORT3XCH10		PA2
	APORT3XCH12		PA4
	APORT3XCH28		PB12
	APORT3XCH30		PB14

Analog Module	Analog Module Channel	Shared Bus	Pin
ACMP1	APORT3YCH3	BUSCY	PD11
	APORT3YCH5		PD13
	APORT3YCH7		PD15
	APORT3YCH9		PA1
	APORT3YCH11		PA3
	APORT3YCH13		PA5
	APORT3YCH27		PB11
	APORT3YCH29		PB13
	APORT3YCH31		PB15
ACMP1	APORT4XCH3	BUSDX	PD11
	APORT4XCH5		PD13
	APORT4XCH7		PD15
	APORT4XCH9		PA1
	APORT4XCH11		PA3
	APORT4XCH13		PA5
	APORT4XCH27		PB11
	APORT4XCH29		PB13
	APORT4XCH31		PB15
ACMP1	APORT4YCH2	BUSDY	PD10
	APORT4YCH4		PD12
	APORT4YCH6		PD14
	APORT4YCH8		PA0
	APORT4YCH10		PA2
	APORT4YCH12		PA4
	APORT4YCH28		PB12
	APORT4YCH30		PB14
ADC0	APORT1XCH6	BUSAX	PC6
	APORT1XCH8		PC8
	APORT1XCH10		PC10
	APORT1XCH16		PF0
	APORT1XCH18		PF2
	APORT1XCH20		PF4
	APORT1XCH22		PF6

Analog Module	Analog Module Channel	Shared Bus	Pin
ADC0	APORT1YCH7	BUSAY	PC7
	APORT1YCH9		PC9
	APORT1YCH11		PC11
	APORT1YCH17		PF1
	APORT1YCH19		PF3
	APORT1YCH21		PF5
	APORT1YCH23		PF7
ADC0	APORT2XCH7	BUSBX	PC7
	APORT2XCH9		PC9
	APORT2XCH11		PC11
	APORT2XCH17		PF1
	APORT2XCH19		PF3
	APORT2XCH21		PF5
	APORT2XCH23		PF7
ADC0	APORT2YCH6	BUSBY	PC6
	APORT2YCH8		PC8
	APORT2YCH10		PC10
	APORT2YCH16		PF0
	APORT2YCH18		PF2
	APORT2YCH20		PF4
	APORT2YCH22		PF6
ADC0	APORT3XCH2	BUSCX	PD10
	APORT3XCH4		PD12
	APORT3XCH6		PD14
	APORT3XCH8		PA0
	APORT3XCH10		PA2
	APORT3XCH12		PA4
	APORT3XCH28		PB12
	APORT3XCH30		PB14

Analog Module	Analog Module Channel	Shared Bus	Pin
ADC0	APORT3YCH3	BUSCY	PD11
	APORT3YCH5		PD13
	APORT3YCH7		PD15
	APORT3YCH9		PA1
	APORT3YCH11		PA3
	APORT3YCH13		PA5
	APORT3YCH27		PB11
	APORT3YCH29		PB13
	APORT3YCH31		PB15
ADC0	APORT4XCH3	BUSDX	PD11
	APORT4XCH5		PD13
	APORT4XCH7		PD15
	APORT4XCH9		PA1
	APORT4XCH11		PA3
	APORT4XCH13		PA5
	APORT4XCH27		PB11
	APORT4XCH29		PB13
	APORT4XCH31		PB15
ADC0	APORT4YCH2	BUSDY	PD10
	APORT4YCH4		PD12
	APORT4YCH6		PD14
	APORT4YCH8		PA0
	APORT4YCH10		PA2
	APORT4YCH12		PA4
	APORT4YCH28		PB12
	APORT4YCH30		PB14
IDAC0	APORT1XCH2	BUSCX	PD10
	APORT1XCH4		PD12
	APORT1XCH6		PD14
	APORT1XCH8		PA0
	APORT1XCH10		PA2
	APORT1XCH12		PA4
	APORT1XCH28		PB12
	APORT1XCH30		PB14

Analog Module	Analog Module Channel	Shared Bus	Pin
IDAC0	APORT1YCH3	BUSCY	PD11
	APORT1YCH5		PD13
	APORT1YCH7		PD15
	APORT1YCH9		PA1
	APORT1YCH11		PA3
	APORT1YCH13		PA5
	APORT1YCH27		PB11
	APORT1YCH29		PB13
	APORT1YCH31		PB15

7. QFN48 Package Specifications

7.1 QFN48 Package Dimensions

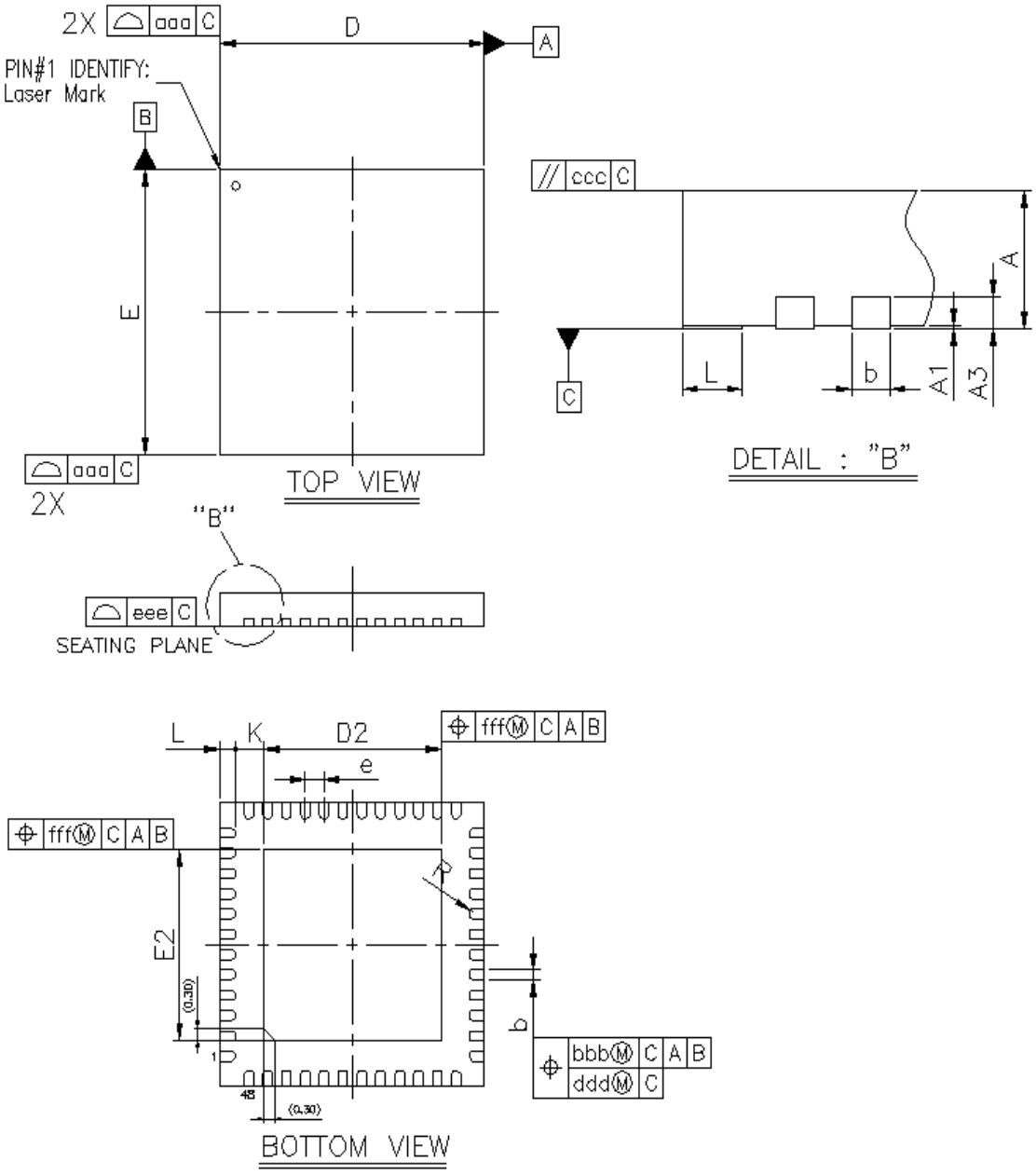


Figure 7.1. QFN48 Package Drawing

Table 7.1. QFN48 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	4.60	4.70	4.80
E2	4.60	4.70	4.80
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
R	0.09	—	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 QFN48 PCB Land Pattern

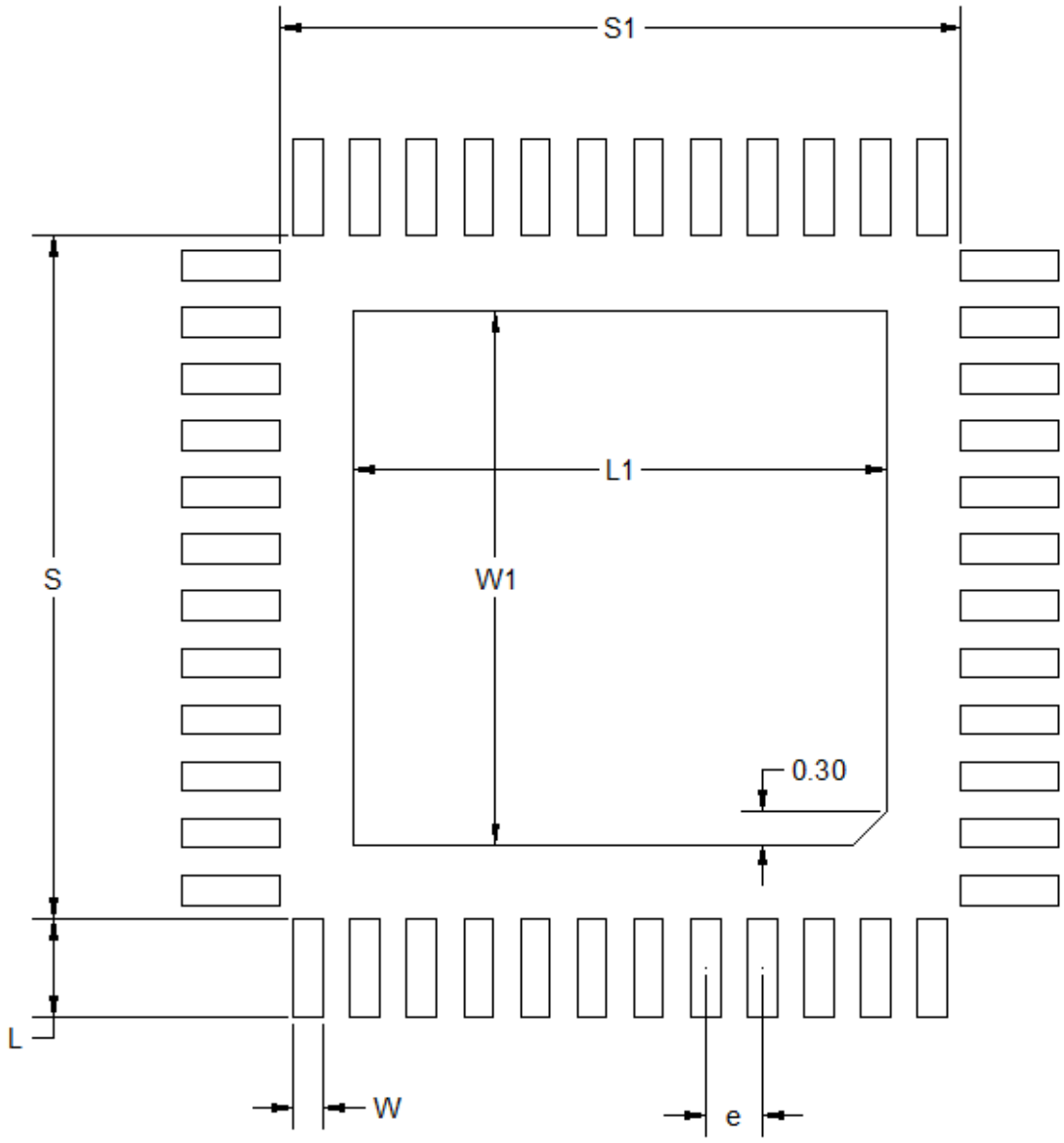


Figure 7.2. QFN48 PCB Land Pattern Drawing

Table 7.2. QFN48 PCB Land Pattern Dimensions

Dimension	Typ
S1	6.01
S	6.01
L1	4.70
W1	4.70
e	0.50
W	0.26
L	0.86

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 4x4 array of 0.75 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 QFN48 Package Marking

Figure 7.3. QFN48 Package Marking

The package marking consists of:

- PPPPPPPPP – The part number designation.
  1. Family Code (B | M | F)
  2. G (Gecko)
  3. Generation (1)
  4. Feature Code (3 | 2 | 1)
  5. TRX Code (3 = TXRX | 2= RX | 1 = TX)
  6. Band (1 = Sub-GHz | 2 = 2.4 GHz | 3 = Dual-band)
  7. Flash (G = 256K | F = 128K | E = 64K | D = 32K)
  8. Temperature Grade (G = -40 to 85 | I = -40 to 125)
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- # – Bootloader revision number.

8. QFN32 Package Specifications

8.1 QFN32 Package Dimensions

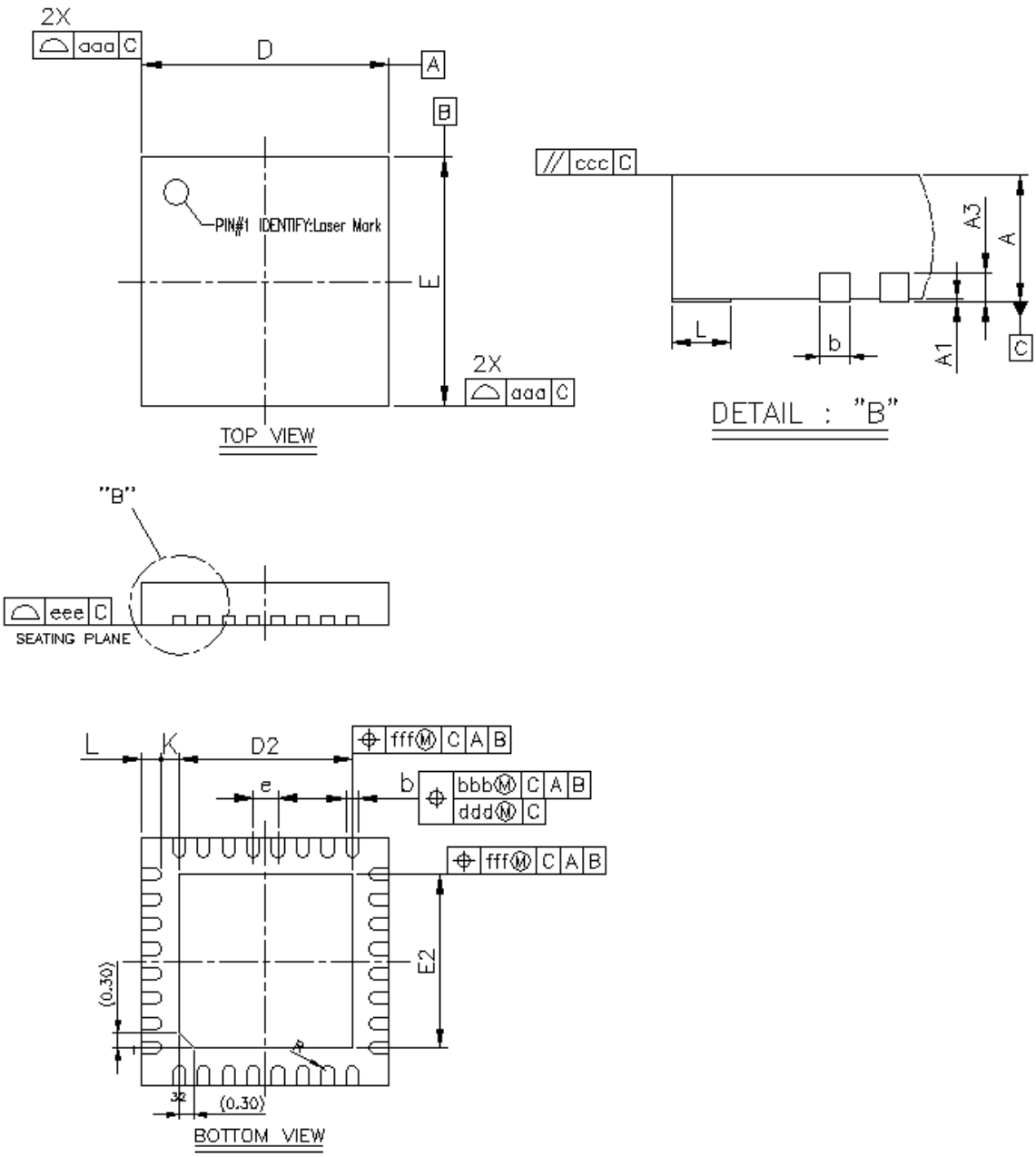


Figure 8.1. QFN32 Package Drawing

Table 8.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D/E	4.90	5.00	5.10
D2/E2	3.40	3.50	3.60
E		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
R	0.09	—	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QFN32 PCB Land Pattern

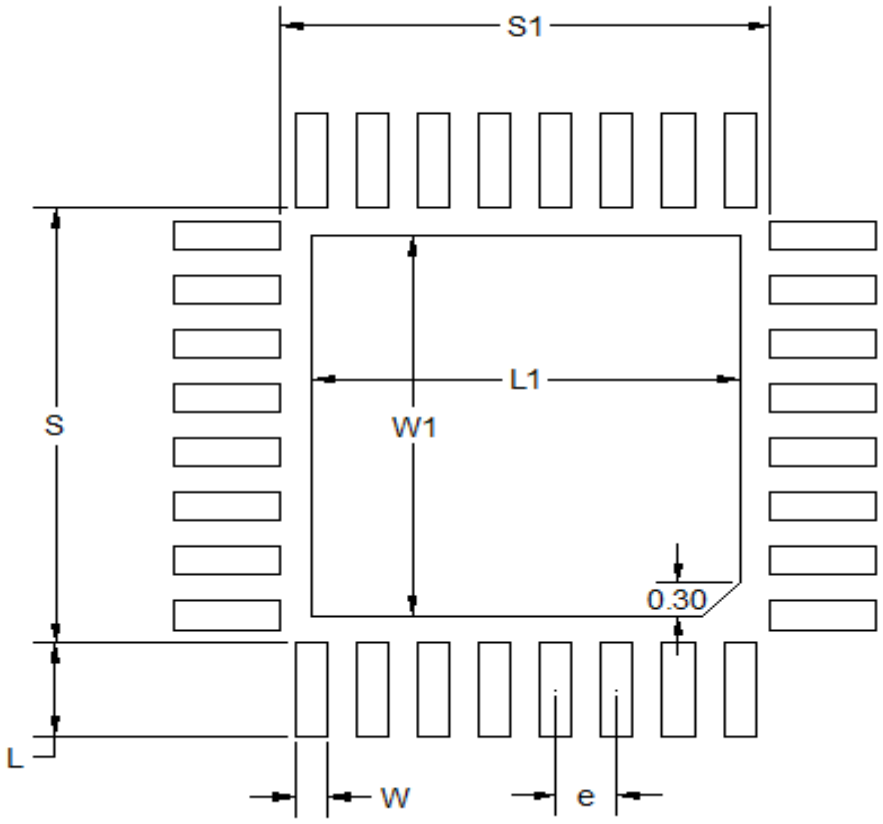


Figure 8.2. QFN32 PCB Land Pattern Drawing

Table 8.2. QFN32 PCB Land Pattern Dimensions

Dimension	Typ
S1	4.01
S	4.01
L1	3.50
W1	3.50
e	0.50
W	0.26
L	0.86

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 3x3 array of 0.85 mm square openings on a 1.00 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3 QFN32 Package Marking

Figure 8.3. QFN32 Package Marking

The package marking consists of:

- PPPPPPPPP – The part number designation.
  1. Family Code (B | M | F)
  2. G (Gecko)
  3. Generation (1)
  4. Feature Code (3 | 2 | 1)
  5. TRX Code (3 = TXRX | 2= RX | 1 = TX)
  6. Band (1 = Sub-GHz | 2 = 2.4 GHz | 3 = Dual-band)
  7. Flash (G = 256K | F = 128K | E = 64K | D = 32K)
  8. Temperature Grade (G = -40 to 85 | I = -40 to 125)
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.

9. Revision History

9.1 Revision 0.9

2016-01-12

- Updated electrical specifications with latest characterization data.
- Added thermal characteristics table.
- Updated OPN decoder figure to include extended family options.

9.2 Revision 0.8

2015-12-01

- Engineering samples note added to ordering information table.
- Updated electrcal specifications with latest available data.

9.3 Revision 0.75

2015-11-3

- Consolidated individual device datasheets into single-family document.
- Re-formatted ordering information table and OPN decoder.
- Updated block diagrams for front page and system overview.
- Removed extraneous sections from DC-DC and wake-on-radio from system overview.
- Updated table formatting for electrical specifications to tech pubs standards.
- Updated electrcal specifications with latest available data.
- Added I2C and USART SPI timing tables.
- Moved DC-DC graph to typical performance curves.
- Updated APORT tables and APORT references to correct nomenclature.

9.4 Revision 0.7

2015-08-31

Outcome of comprehensive review cycle of EFR32BG Datasheets. Major changes span the following sections

- Section 2: Ordering Information
- Section 3.3.4: Receiver Architecture
- Section 3.3.5: Transmitter Architecture
- Section 4: Electrical Characteristics
- Section 4.3.1: General Operating Conditions
- Section 4.4: DC-DC Converter
- Section 4.5: Current Consumption
- Section 4.9.1: RF Transmitter Characteristics for 2.4 GHz Band
- Section 4.9.2: RF Receiver General Characteristics for 2.4 GHz Band
- Section 4.9.3: RF Transmitter Characteristics for Bluetooth Smart in 2.4 GHz Band
- Section 4.9.4: RF Receiver Characteristics for Bluetooth Smart in 2.4 GHz Band
- Section 4.11.1: LFXO
- Section 4.11.2: HFXO
- Section 4.12: GPIO
- Section 4.13: VMON
- Section 4.14: ADC
- Section 4.15: IDAC
- Section 4.16: Analog Comparator
- Section 5: Application Circuits
- Section 6.5: QFNxx Package
- Section 6.7: QFNxx Package Marking

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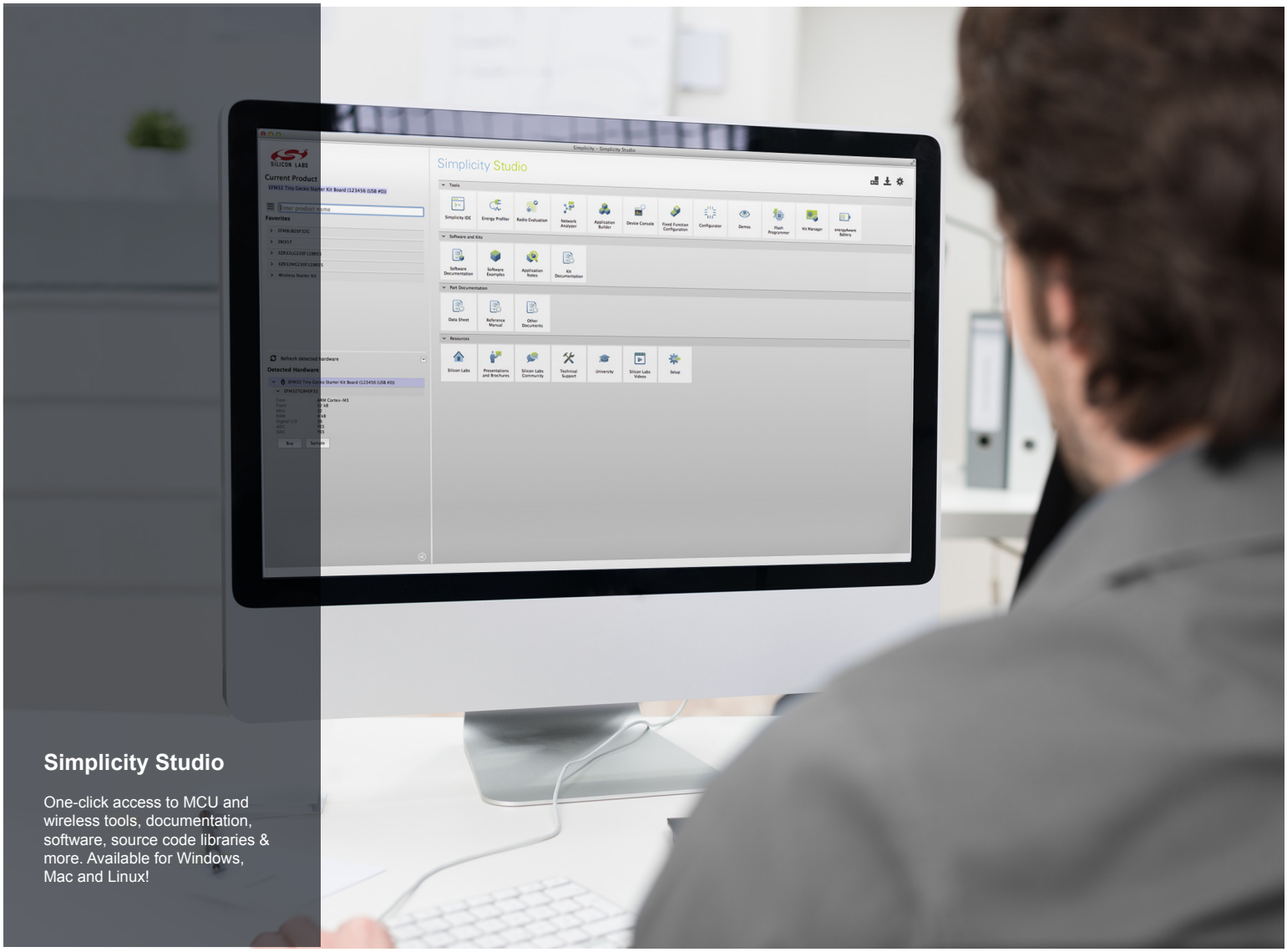

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