

# CC1311P3 SimpleLink™ High-Performance Sub-1GHz Wireless MCU with Integrated Power Amplifier

## 1 Features

### Wireless microcontroller

- Powerful 48MHz Arm® Cortex®-M4 processor
- 352KB flash program memory
- 32KB of ultra-low leakage SRAM
- 8KB of Cache SRAM (Alternatively available as general-purpose RAM)
- Programmable radio includes support for 2-(G)FSK, 4-(G)FSK, MSK, OOK, IEEE 802.15.4 PHY and MAC
- Supports over-the-air upgrade (OTA)

### Low power consumption

- MCU consumption:
  - 2.63mA active mode, CoreMark®
  - 55µA/MHz running CoreMark
  - 0.7µA standby mode, RTC, 32KB RAM
  - 0.1µA shutdown mode, wake-up on pin
- Radio Consumption:
  - 5.4mA RX at 868MHz
  - 24.9mA TX at +14dBm at 868MHz
  - 65mA TX at +20dBm at 915MHz

### Wireless protocol support

- [Mioty](#)
- [Wireless M-Bus](#)
- [SimpleLink™ TI 15.4-stack](#)
- 6LoWPAN
- [Proprietary systems](#)

### High-performance radio

- -121dBm for 2.5kbps long-range mode
- -120dBm at 4.8kbps narrowband mode, 433MHz
- -118dBm at 9.6kbps narrowband mode, 868MHz
- -110dBm at 50kbps, 802.15.4, 868MHz
- Output power up to +20dBm with temperature compensation
- Down to 4kHz receiver filter bandwidth

### Regulatory compliance

- Designed for systems targeting compliance with these standards:
  - ETSI EN 300 220 Receiver Cat. 1.5 and 2, EN 303 131, EN 303 204
  - FCC CFR47 Part 15
  - ARIB STD-T108

### MCU peripherals

- Digital peripherals can be routed to any GPIO
- Four 32-bit or eight 16-bit general-purpose timers
- 12-bit ADC, 200 kSamples/s, 8 channels
- 8-bit DAC
- Analog Comparator
- UART, SSI, I²C, I²S
- Real-time clock (RTC)
- Integrated temperature and battery monitor

### Security enablers

- AES 128-bit cryptographic accelerator
- True random number generator (TRNG)
- Additional cryptography drivers available in Software Development Kit (SDK)

### Development tools and software

- [LP-CC1311P3 Development Kit](#)
- [SimpleLink™ CC13xx and CC26xx Software Development Kit \(SDK\)](#)
- [SmartRF™ Studio](#) for simple radio configuration
- [SysConfig](#) system configuration tool

### Operating range

- On-chip buck DC/DC converter
- 1.8V to 3.8V single supply voltage
- -40 to +105°C

### Package

- 7mm × 7mm RGZ VQFN48 (26 GPIOs)
- RoHS-compliant package



## 2 Applications

- **Grid infrastructure**
  - Smart Meters—[electricity meter](#), [water meter](#), [gas meter](#), and [heat cost allocator](#)
  - Grid communications—[wireless communications](#)
  - EV charging infrastructure—[AC charging \(pile\) station](#)
  - Other alternative energy—[energy harvesting](#)
- **Building automation**
  - Building security systems—[motion detector](#), [door and window sensor](#), [glass break detector](#), [panic button](#), [electronic smart lock](#), and [IP network camera](#)
  - HVAC systems—[thermostat](#), [environmental sensor](#), and [HVAC controller](#)
- Fire safety—[smoke and head detector](#), [gas detector](#), and [fire alarm control panel](#)
- **Retail Automation**
  - Retail automation and payment applications—[electronic shelf labels](#) and [portable POS terminal](#)
- **Personal Electronics**
  - [RF remote controls](#)
  - [Smart Speakers](#) and [smart displays](#)
  - [Gaming](#) and [electronic and robotic toys](#)
  - [Wearables \(non-medical\)](#) and [smart trackers](#)
- **Wireless Modules**
  - [Wireless third-party modules](#)
  - [Wireless communications modules](#)

## 3 Description

The SimpleLink™ CC1311P3 device is a multiprotocol Sub-1GHz wireless microcontroller (MCU) supporting IEEE 802.15.4g, IPv6-enabled smart objects (6LoWPAN), [mioty](#), proprietary systems, including the [TI 15.4-Stack](#) (Sub-1GHz). The CC1311P3 is based on an Arm® Cortex® M4 main processor and optimized for low-power wireless communication and advanced sensing in [grid infrastructure](#), [building automation](#), [retail automation](#), [personal electronics](#), and [medical applications](#).

The CC1311P3 has a software-defined radio powered by an Arm® Cortex® M0, which allows support for multiple physical layers and RF standards. The device supports operation in 143MHz to 176MHz, 287MHz to 351MHz, 359MHz to 527-MHz, 861MHz to 1054MHz, and 1076MHz to 1315MHz frequency bands. The CC1311P3 has an efficient built-in PA that supports +14dBm TX at 24.9mA and +20dBm TX at 65mA. In RX, it has -121dBm sensitivity and 88dB blocking  $\pm 10$ MHz in SimpleLink™ long-range mode with 2.5kbps data rate.

The CC1311P3 has a low sleep current of 0.7 $\mu$ A with RTC and 32KB RAM retention.

Consistent with many customers' 10 to 15 years or longer life cycle requirements, TI has a [product life cycle policy](#) with a commitment to product longevity and continuity of supply.

The CC1311P3 device is part of the SimpleLink™ MCU platform, which consists of Wi-Fi®, [Bluetooth®](#) Low Energy, Thread, Zigbee, Wi-SUN®, Amazon Sidewalk, [mioty](#), Sub-1GHz MCUs, and host MCUs. CC1311P3 is part of a scalable portfolio with flash sizes from 32KB to 704KB with pin-to-pin compatible package options. The common [SimpleLink™CC13xx and CC26xx Software Development Kit \(SDK\)](#) and [SysConfig](#) system configuration tool support migration between devices in the portfolio. A comprehensive number of software stacks, application examples, and SimpleLink™ Academy training sessions are included in the SDK. For more information, visit [wireless connectivity](#).

### Device Information

| PART NUMBER <sup>(1)</sup> | PACKAGE   | PACKAGE SIZE    |
|----------------------------|-----------|-----------------|
| CC1311P31T0RGZR            | VQFN (48) | 7.00mm × 7.00mm |

(1) For more information, see [Section 12](#).

## 4 Functional Block Diagram

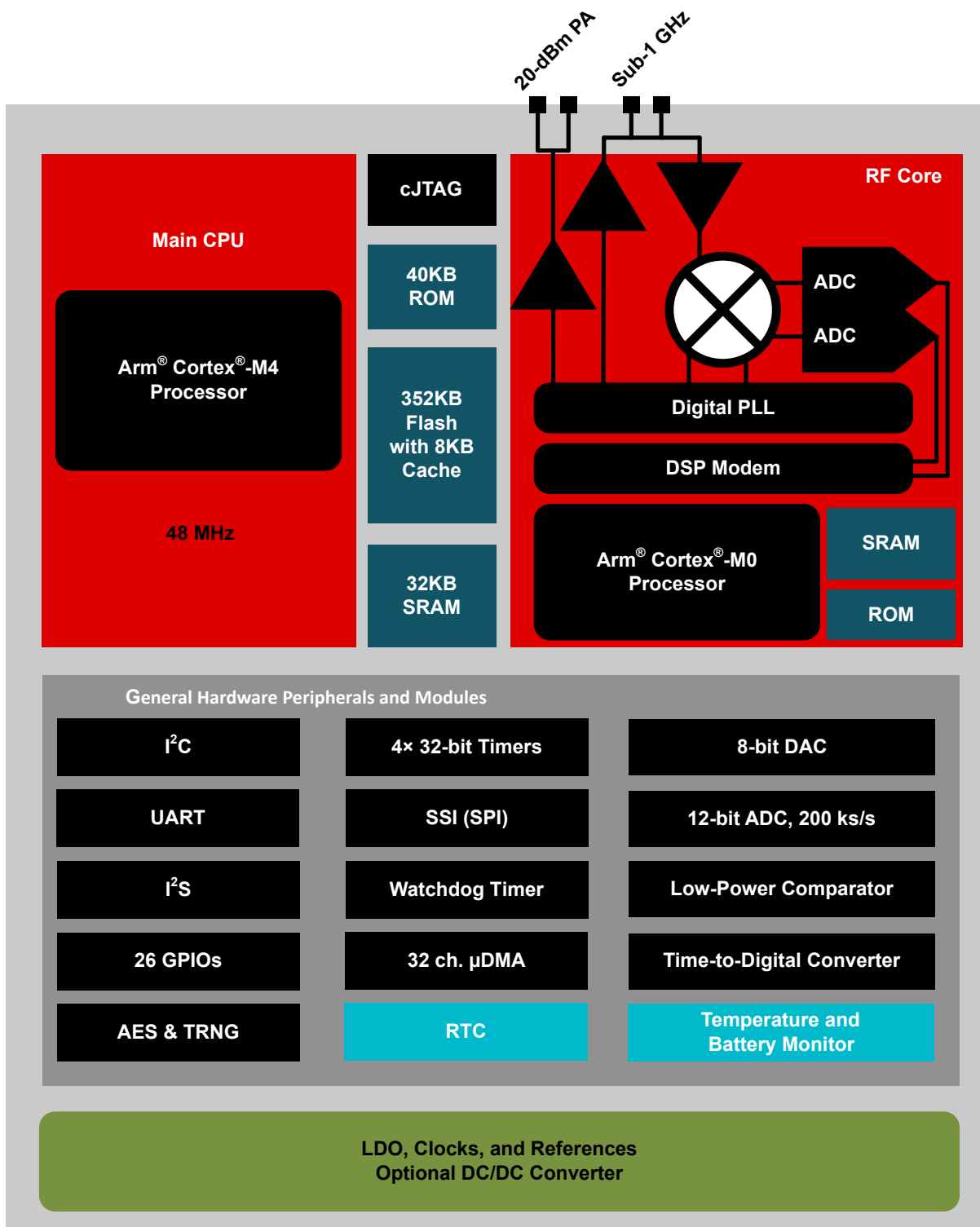


Figure 4-1. CC1311P3 Functional Block Diagram

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## 5 Device Comparison

| DEVICE                  | RADIO SUPPORT  |              |                |       |         |          |               |        |        |               |           | FLASH<br>(kB) | RAM +<br>CACHE<br>(kB) | GPIO  | PACKAGE SIZE      |                   |                   |                   |                   |                   |
|-------------------------|----------------|--------------|----------------|-------|---------|----------|---------------|--------|--------|---------------|-----------|---------------|------------------------|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
|                         | Sub-1GHz Prop. | 2.4GHz Prop. | Wireless M-Bus | mioty | Wi-SUN® | Sidewalk | Bluetooth® LE | Zigbee | Thread | Multiprotocol | +20dBm PA |               |                        |       | 4 × 4mm VQFN (24) | 4 × 4mm VQFN (32) | 5 × 5mm VQFN (32) | 5 × 5mm VQFN (40) | 7 × 7mm VQFN (48) | 8 × 8mm VQFN (64) |
| CC1310                  | √              |              | √              | √     |         |          |               |        |        |               |           | 32-128        | 16-20 + 8              | 10–30 |                   | √                 | √                 |                   | √                 |                   |
| CC1311R3                | √              |              | √              | √     |         |          |               |        |        |               |           | 352           | 32 + 8                 | 22–30 |                   |                   |                   | √                 | √                 |                   |
| CC1311P3                | √              |              | √              | √     |         |          |               |        |        |               | √         | 352           | 32 + 8                 | 26    |                   |                   |                   |                   | √                 |                   |
| CC1312R                 | √              |              | √              | √     | √       |          |               |        |        |               |           | 352           | 80 + 8                 | 30    |                   |                   |                   |                   | √                 |                   |
| CC1312R7                | √              |              | √              | √     | √       | √        |               |        |        | √             |           | 704           | 144 + 8                | 30    |                   |                   |                   |                   | √                 |                   |
| CC1314R10               | √              |              | √              | √     | √       | √        |               |        |        | √             |           | 1024          | 256 + 8                | 30-46 |                   |                   |                   |                   | √                 | √                 |
| CC1352R                 | √              | √            | √              | √     | √       |          | √             | √      | √      | √             |           | 352           | 80 + 8                 | 28    |                   |                   |                   |                   | √                 |                   |
| CC1354R10               | √              | √            | √              | √     | √       |          | √             | √      | √      | √             |           | 1024          | 256 + 8                | 28-42 |                   |                   |                   |                   | √                 | √                 |
| CC1352P                 | √              | √            | √              | √     | √       |          | √             | √      | √      | √             | √         | 352           | 80 + 8                 | 26    |                   |                   |                   |                   | √                 |                   |
| CC1352P7                | √              | √            | √              | √     | √       | √        | √             | √      | √      | √             | √         | 704           | 144 + 8                | 26    |                   |                   |                   |                   | √                 |                   |
| CC1354P10               | √              | √            | √              | √     | √       | √        | √             | √      | √      | √             | √         | 1024          | 256 + 8                | 26–42 |                   |                   |                   |                   | √                 | √                 |
| CC2340R2                |                | √            |                |       |         |          | √             | √      |        |               |           | 256           | 28                     | 12    | √                 |                   |                   |                   |                   |                   |
| CC2340R5 <sup>(1)</sup> |                | √            |                |       |         |          | √             | √      | √      |               |           | 512           | 36                     | 12–26 | √                 |                   |                   | √                 |                   |                   |
| CC2340R5-Q1             |                |              |                |       |         |          | √             |        |        |               |           | 512           | 36                     | 19    |                   |                   | √                 |                   |                   |                   |
| CC2640R2F               |                |              |                |       |         |          | √             |        |        |               |           | 128           | 20 + 8                 | 10–31 |                   | √                 | √                 |                   | √                 |                   |
| CC2642R                 |                |              |                |       |         |          | √             |        |        |               |           | 352           | 80 + 8                 | 31    |                   |                   |                   |                   | √                 |                   |
| CC2642R-Q1              |                |              |                |       |         |          | √             |        |        |               |           | 352           | 80 + 8                 | 31    |                   |                   |                   |                   | √                 |                   |
| CC2651R3                |                | √            |                |       |         |          | √             | √      |        |               |           | 352           | 32 + 8                 | 23–31 |                   |                   |                   | √                 | √                 |                   |
| CC2651P3                |                | √            |                |       |         |          | √             | √      |        |               | √         | 352           | 32 + 8                 | 22–26 |                   |                   |                   | √                 | √                 |                   |
| CC2652R                 |                | √            |                |       |         |          | √             | √      | √      | √             |           | 352           | 80 + 8                 | 31    |                   |                   |                   |                   | √                 |                   |
| CC2652RB                |                | √            |                |       |         |          | √             | √      | √      | √             |           | 352           | 80 + 8                 | 31    |                   |                   |                   |                   | √                 |                   |
| CC2652R7                |                | √            |                |       |         |          | √             | √      | √      | √             |           | 704           | 144 + 8                | 31    |                   |                   |                   |                   | √                 |                   |
| CC2652P                 |                | √            |                |       |         |          | √             | √      | √      | √             | √         | 352           | 80 + 8                 | 26    |                   |                   |                   |                   | √                 |                   |
| CC2652P7                |                | √            |                |       |         |          | √             | √      | √      | √             | √         | 704           | 144 + 8                | 26    |                   |                   |                   |                   | √                 |                   |
| CC2674R10               |                | √            |                |       |         |          | √             | √      | √      | √             |           | 1024          | 256 + 8                | 31–45 |                   |                   |                   |                   | √                 | √                 |
| CC2674P10               |                | √            |                |       |         |          | √             | √      | √      | √             | √         | 1024          | 256 + 8                | 26–45 |                   |                   |                   |                   | √                 | √                 |

(1) Thread support enabled by a future software update

## 6 Pin Configuration and Functions

### 6.1 Pin Diagram—RGZ Package (Top View)

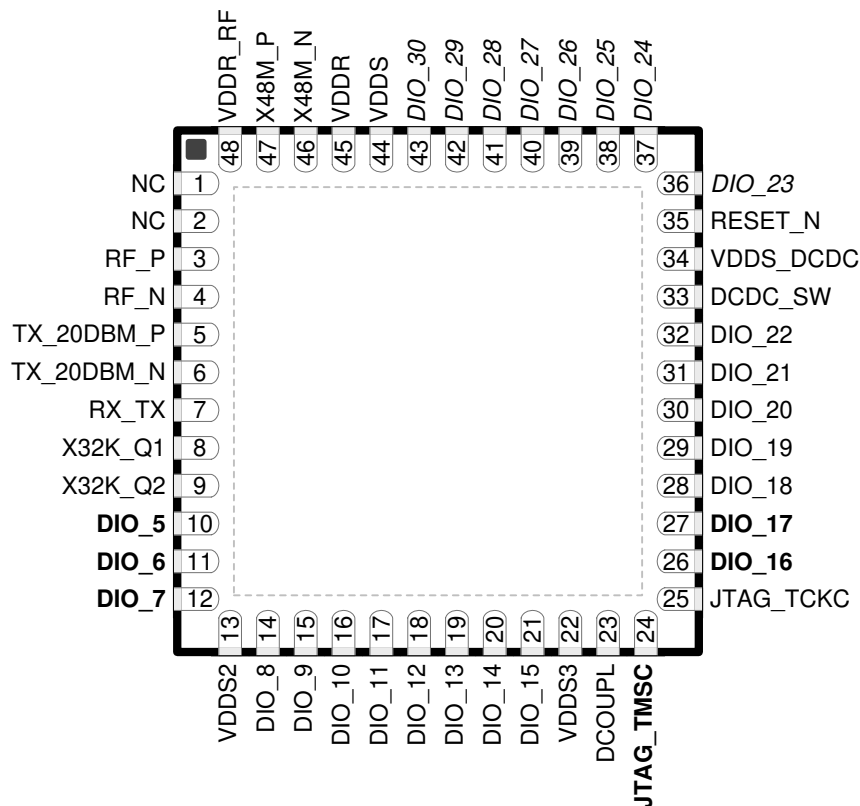


**Figure 6-1. RGZ (7mm × 7mm) Pinout, 0.5mm Pitch (Top View)**

The following I/O pins marked in [Figure 6-1](#) in **bold** have high-drive capabilities:

- Pin 10, **DIO\_5**
- Pin 11, **DIO\_6**
- Pin 12, **DIO\_7**
- Pin 24, **JTAG\_TMSC**
- Pin 26, **DIO\_16**
- Pin 27, **DIO\_17**

The following I/O pins marked in [Figure 6-1](#) in *italics* have analog capabilities:

- Pin 36, *DIO\_23*
- Pin 37, *DIO\_24*
- Pin 38, *DIO\_25*
- Pin 39, *DIO\_26*
- Pin 40, *DIO\_27*
- Pin 41, *DIO\_28*
- Pin 42, *DIO\_29*
- Pin 43, *DIO\_30*

## 6.2 Signal Descriptions—RGZ Package

**Table 6-1. Signal Descriptions—RGZ Package**

| PIN        |     | I/O | TYPE              | DESCRIPTION                                                                                                   |
|------------|-----|-----|-------------------|---------------------------------------------------------------------------------------------------------------|
| NAME       | NO. |     |                   |                                                                                                               |
| DCDC_SW    | 33  | —   | Power             | Output from internal DC/DC converter <sup>(1)</sup>                                                           |
| DCOUPPL    | 23  | —   | Power             | For decoupling of internal 1.27V regulated digital-supply <sup>(2)</sup>                                      |
| DIO_5      | 10  | I/O | Digital           | GPIO, high-drive capability                                                                                   |
| DIO_6      | 11  | I/O | Digital           | GPIO, high-drive capability                                                                                   |
| DIO_7      | 12  | I/O | Digital           | GPIO, high-drive capability                                                                                   |
| DIO_8      | 14  | I/O | Digital           | GPIO                                                                                                          |
| DIO_9      | 15  | I/O | Digital           | GPIO                                                                                                          |
| DIO_10     | 16  | I/O | Digital           | GPIO                                                                                                          |
| DIO_11     | 17  | I/O | Digital           | GPIO                                                                                                          |
| DIO_12     | 18  | I/O | Digital           | GPIO                                                                                                          |
| DIO_13     | 19  | I/O | Digital           | GPIO                                                                                                          |
| DIO_14     | 20  | I/O | Digital           | GPIO                                                                                                          |
| DIO_15     | 21  | I/O | Digital           | GPIO                                                                                                          |
| DIO_16     | 26  | I/O | Digital           | GPIO, JTAG_TDO, high-drive capability                                                                         |
| DIO_17     | 27  | I/O | Digital           | GPIO, JTAG_TDI, high-drive capability                                                                         |
| DIO_18     | 28  | I/O | Digital           | GPIO                                                                                                          |
| DIO_19     | 29  | I/O | Digital           | GPIO                                                                                                          |
| DIO_20     | 30  | I/O | Digital           | GPIO                                                                                                          |
| DIO_21     | 31  | I/O | Digital           | GPIO                                                                                                          |
| DIO_22     | 32  | I/O | Digital           | GPIO                                                                                                          |
| DIO_23     | 36  | I/O | Digital or Analog | GPIO, analog capability                                                                                       |
| DIO_24     | 37  | I/O | Digital or Analog | GPIO, analog capability                                                                                       |
| DIO_25     | 38  | I/O | Digital or Analog | GPIO, analog capability                                                                                       |
| DIO_26     | 39  | I/O | Digital or Analog | GPIO, analog capability                                                                                       |
| DIO_27     | 40  | I/O | Digital or Analog | GPIO, analog capability                                                                                       |
| DIO_28     | 41  | I/O | Digital or Analog | GPIO, analog capability                                                                                       |
| DIO_29     | 42  | I/O | Digital or Analog | GPIO, analog capability                                                                                       |
| DIO_30     | 43  | I/O | Digital or Analog | GPIO, analog capability                                                                                       |
| EGP        | —   | —   | GND               | Ground – exposed ground pad <sup>(3)</sup>                                                                    |
| JTAG_TMSC  | 24  | I/O | Digital           | JTAG TMS, high-drive capability                                                                               |
| JTAG_TCKC  | 25  | I   | Digital           | JTAG TCK                                                                                                      |
| RESET_N    | 35  | I   | Digital           | Reset, active low. No internal pullup resistor                                                                |
| RF_P       | 3   | —   | RF                | Positive RF input signal to LNA during RX<br>Positive RF output signal from PA during TX                      |
| RF_N       | 4   | —   | RF                | Negative RF input signal to LNA during RX<br>Negative RF output signal from PA during TX                      |
| RX_TX      | 7   | —   | RF                | Optional bias pin for the RF LNA                                                                              |
| TX_20DBM_P | 5   | —   | RF                | Positive high-power TX signal                                                                                 |
| TX_20DBM_N | 6   | —   | RF                | Negative high-power TX signal                                                                                 |
| VDDR       | 45  | —   | Power             | Internal supply, must be powered from the internal DC/DC converter or the internal LDO <sup>(2) (4) (6)</sup> |
| VDDR_RF    | 48  | —   | Power             | Internal supply, must be powered from the internal DC/DC converter or the internal LDO <sup>(2) (5) (6)</sup> |
| VDDS       | 44  | —   | Power             | 1.8V to 3.8V main chip supply <sup>(1)</sup>                                                                  |

**Table 6-1. Signal Descriptions—RGZ Package (continued)**

| PIN       |     | I/O | TYPE   | DESCRIPTION                            |
|-----------|-----|-----|--------|----------------------------------------|
| NAME      | NO. |     |        |                                        |
| VDDS2     | 13  | —   | Power  | 1.8V to 3.8V DIO supply <sup>(1)</sup> |
| VDDS3     | 22  | —   | Power  | 1.8V to 3.8V DIO supply <sup>(1)</sup> |
| VDDS_DCDC | 34  | —   | Power  | 1.8V to 3.8V DC/DC converter supply    |
| X48M_N    | 46  | —   | Analog | 48-MHz crystal oscillator pin 1        |
| X48M_P    | 47  | —   | Analog | 48-MHz crystal oscillator pin 2        |
| X32K_Q1   | 8   | —   | Analog | 32kHz crystal oscillator pin 1         |
| X32K_Q2   | 9   | —   | Analog | 32kHz crystal oscillator pin 2         |

- (1) For more details, see the device technical reference manual listed in [Section 10.3](#).  
 (2) Do not supply external circuitry from this pin.  
 (3) EGP is the only ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.  
 (4) If the internal DC/DC converter is not used, this pin is supplied internally from the main LDO.  
 (5) If the internal DC/DC converter is not used, this pin must be connected to VDDR for supply from the main LDO.  
 (6) The output from the internal DC/DC and LDO is trimmed to 1.68V.

## 6.3 Connections for Unused Pins and Modules

**Table 6-2. Connections for Unused Pins—RGZ Package**

| FUNCTION                       | SIGNAL NAME | PIN NUMBER                       | ACCEPTABLE PRACTICE <sup>(1)</sup> | PREFERRED PRACTICE <sup>(1)</sup> |
|--------------------------------|-------------|----------------------------------|------------------------------------|-----------------------------------|
| GPIO                           | DIO_n       | 10–12<br>14–21<br>26–32<br>36–43 | NC or GND                          | NC                                |
| 32.768kHz crystal              | X32K_Q1     | 8                                | NC or GND                          | NC                                |
|                                | X32K_Q2     | 9                                |                                    |                                   |
| No Connects                    | NC          | 1–2                              | NC                                 | NC                                |
| DC/DC converter <sup>(2)</sup> | DCDC_SW     | 33                               | NC                                 | NC                                |
|                                | VDDS_DCDC   | 34                               | VDDS                               | VDDS                              |

- (1) NC = No connect  
 (2) When the DC/DC converter is not used, the inductor between DCDC\_SW and VDDR can be removed. VDDR and VDDR\_RF must still be connected and the 22µF DCDC capacitor must be kept on the VDDR net.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

|                  |                                                                         | MIN                                                      | MAX                               | UNIT |
|------------------|-------------------------------------------------------------------------|----------------------------------------------------------|-----------------------------------|------|
| V <sub>DDS</sub> | Supply voltage                                                          | −0.3                                                     | 4.1                               | V    |
|                  | Voltage on any digital pin <sup>(3) (4) (5)</sup>                       | −0.3                                                     | V <sub>DDSn</sub> + 0.3, max 4.1  | V    |
|                  | Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X48M_N and X48M_P | −0.3                                                     | V <sub>DDDR</sub> + 0.3, max 2.25 | V    |
| V <sub>in</sub>  | Voltage on ADC input                                                    | Voltage scaling enabled                                  | V <sub>DDSn</sub>                 | V    |
|                  |                                                                         | Voltage scaling disabled, internal reference             | 1.49                              |      |
|                  |                                                                         | Voltage scaling disabled, V <sub>DDSn</sub> as reference | V <sub>DDSn</sub> / 2.9           |      |
|                  | Input level, RF pins (RF_P and RF_N)                                    |                                                          | 10                                | dBm  |
| T <sub>stg</sub> | Storage temperature                                                     | −40                                                      | 150                               | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, and performance, and shorten the device's lifetime.
- (2) All voltage values are with respect to ground, unless otherwise noted.
- (3) Including analog capable DIOs
- (4) Injection current is not supported on any GPIO pin.
- (5) V<sub>DDSn</sub>2 and V<sub>DDSn</sub>3 must be lower or equal to V<sub>DDSn</sub>.

### 7.2 ESD Ratings

|                  |                         |                                                                  |          | VALUE | UNIT |
|------------------|-------------------------|------------------------------------------------------------------|----------|-------|------|
| V <sub>ESD</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS001 <sup>(1)</sup> | All pins | ±2000 | V    |
|                  |                         | Charged device model (CDM), per JESD22-C101 <sup>(2)</sup>       | All pins | ±500  | V    |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                                                                                                   |                                                                          | MIN | MAX               | UNIT  |
|---------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|-----|-------------------|-------|
| Operating ambient temperature <sup>(1) (2)</sup>                                                  |                                                                          | −40 | 105               | °C    |
| Operating junction temperature <sup>(1) (2)</sup>                                                 |                                                                          | −40 | 115               | °C    |
| Operating supply voltage (V <sub>DDSn</sub> )                                                     |                                                                          | 1.8 | 3.8               | V     |
| Operating supply voltage (V <sub>DDSn</sub> 2 and V <sub>DDSn</sub> 3) <sup>(4) (5) (6)</sup>     |                                                                          | 1.8 | V <sub>DDSn</sub> |       |
| Operating supply voltage (V <sub>DDSn</sub> ), boost mode                                         | V <sub>DDDR</sub> = 1.95 V<br>+14dBm RF output sub-1 GHz power amplifier | 2.1 | 3.8               | V     |
| Operating supply voltage (V <sub>DDSn</sub> 2 and V <sub>DDSn</sub> 3), boost mode <sup>(4)</sup> | V <sub>DDDR</sub> = 1.95V<br>+14 dBm RF output Sub-1GHz power amplifier  | 1.8 | V <sub>DDSn</sub> | V     |
| Rising supply voltage slew rate                                                                   |                                                                          | 0   | 100               | mV/μs |
| Falling supply voltage slew rate <sup>(3)</sup>                                                   |                                                                          | 0   | 20                | mV/μs |

- (1) Operation at or near maximum operating temperature for extended durations will result in lifetime reduction.
- (2) See the Thermal Resistance Characteristics section for more information.
- (3) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-μF V<sub>DDSn</sub> input capacitor must be used to ensure compliance with this slew rate.
- (4) V<sub>DDSn</sub>2 and V<sub>DDSn</sub>3 must be lower or equal to V<sub>DDSn</sub>. For JTAG operation V<sub>DDSn</sub> should be equal to V<sub>DDSn</sub>3
- (5) All power segments need to be powered all times
- (6) If the IO strength is set to auto, the drive strength is adjusted based on the voltage level for V<sub>DDSn</sub>. In the case of V<sub>DDSn</sub>2 is lower than V<sub>DDSn</sub>, all pins referred to V<sub>DDSn</sub>2 should be manually set (IOCFGn.IOSTR), for example to maximum. In the case of V<sub>DDSn</sub>3 is lower than V<sub>DDSn</sub>, all pins referred to V<sub>DDSn</sub>3 should be manually set (IOCFGn.IOSTR), for example to maximum.

## 7.4 Power Supply and Modules

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                                         |                   | MIN | TYP  | MAX | UNIT |
|-------------------------------------------------------------------|-------------------|-----|------|-----|------|
| VDDS Power-on-Reset (POR) threshold                               |                   | 1.1 | 1.55 |     | V    |
| VDDS Brown-out Detector (BOD) <sup>(1)</sup>                      | Rising threshold  |     | 1.77 |     | V    |
| VDDS Brown-out Detector (BOD), before initial boot <sup>(2)</sup> | Rising threshold  |     | 1.70 |     | V    |
| VDDS Brown-out Detector (BOD) <sup>(1)</sup>                      | Falling threshold |     | 1.75 |     | V    |

(1) For boost mode (VDDR = 1.95 V), TI drivers software initialization will trim VDDS BOD limits to maximum (approximately 2.0 V)

(2) Brown-out Detector is trimmed at initial boot, value is kept until device is reset by a POR reset or the RESET\_N pin

## 7.5 Power Consumption - Power Modes

When measured on the CC1311-P3EM-7XD7793-PA915 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.6\text{ V}$  ( $V_{\text{DDS}}=V_{\text{DDS2}}=V_{\text{DDS3}}$ ) with DC/DC enabled unless otherwise noted.

| PARAMETER                             | TEST CONDITIONS                 | MIN                                                                   | TYP  | MAX | UNIT          |
|---------------------------------------|---------------------------------|-----------------------------------------------------------------------|------|-----|---------------|
| <b>Core Current Consumption</b>       |                                 |                                                                       |      |     |               |
| $I_{\text{core}}$                     | Reset and Shutdown              | Reset. RESET_N pin asserted or VDDS below power-on-reset threshold    | 115  |     | nA            |
|                                       |                                 | Shutdown. No clocks running, no retention                             | 115  |     |               |
|                                       | Standby without cache retention | RTC running, CPU, 32KB RAM and (partial) register retention. RCOSC_LF | 0.7  |     | $\mu\text{A}$ |
|                                       |                                 | RTC running, CPU, 32KB RAM and (partial) register retention. XOSC_LF  | 0.8  |     |               |
|                                       | Standby with cache retention    | RTC running, CPU, 32KB RAM and (partial) register retention. RCOSC_LF | 2.1  |     | $\mu\text{A}$ |
|                                       |                                 | RTC running, CPU, 32KB RAM and (partial) register retention. XOSC_LF  | 2.2  |     |               |
|                                       | Idle                            | Supply Systems and RAM powered. RCOSC_HF                              | 570  |     | $\mu\text{A}$ |
|                                       | Active                          | MCU running CoreMark at 48 MHz. RCOSC_HF                              | 2.50 |     | mA            |
| <b>Peripheral Current Consumption</b> |                                 |                                                                       |      |     |               |
| $I_{\text{peri}}$                     | Peripheral power domain         | Delta current with domain enabled                                     | 47.0 |     | $\mu\text{A}$ |
|                                       | Serial power domain             | Delta current with domain enabled                                     | 3.3  |     |               |
|                                       | RF Core                         | Delta current with power domain enabled, clock enabled, RF core idle  | 122  |     |               |
|                                       | $\mu\text{DMA}$                 | Delta current with clock enabled, module is idle                      | 58.1 |     |               |
|                                       | Timers                          | Delta current with clock enabled, module is idle <sup>(1)</sup>       | 87.0 |     |               |
|                                       | I2C                             | Delta current with clock enabled, module is idle                      | 11.6 |     |               |
|                                       | I2S                             | Delta current with clock enabled, module is idle                      | 25.8 |     |               |
|                                       | SSI                             | Delta current with clock enabled, module is idle                      | 61.3 |     |               |
|                                       | UART                            | Delta current with clock enabled, module is idle                      | 125  |     |               |
|                                       | CRYPTO (AES)                    | Delta current with clock enabled, module is idle                      | 25.2 |     |               |
|                                       | TRNG                            | Delta current with clock enabled, module is idle                      | 23.3 |     |               |

(1) Only one GPTimer running

## 7.6 Power Consumption - Radio Modes

When measured on the CC1311-P3EM-7XD7793-PA915 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DD5}} = 3.6\text{ V}$  with DC/DC enabled unless otherwise noted.

High power PA connected to  $V_{\text{DD5}}$  unless otherwise noted.

Using boost mode (increasing VDDR up to 1.95 V), will increase system current by 15% (does not apply to TX +14 dBm setting where this current is already included).

Relevant  $I_{\text{core}}$  and  $I_{\text{peri}}$  currents are included in below numbers.

| PARAMETER                                        | TEST CONDITIONS                                                                         | MIN | TYP  | MAX | UNIT |
|--------------------------------------------------|-----------------------------------------------------------------------------------------|-----|------|-----|------|
| Radio receive current, 868 MHz                   |                                                                                         |     | 5.4  |     | mA   |
| Radio transmit current<br>Regular PA             | 0 dBm output power setting<br>868 MHz                                                   |     | 7.4  |     | mA   |
|                                                  | +10 dBm output power setting<br>868 MHz                                                 |     | 13.9 |     | mA   |
| Radio transmit current<br>Boost mode, regular PA | +14 dBm output power setting<br>868 MHz                                                 |     | 24.9 |     | mA   |
| Radio transmit current<br>High-power PA          | Transmit (TX), +20 dBm output power setting<br>915 MHz, $V_{\text{DD5}} = 3.3\text{ V}$ |     | 65   |     | mA   |

## 7.7 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and  $V_{\text{DD5}} = 3.0\text{ V}$  (unless otherwise noted)

| PARAMETER                                                                     | TEST CONDITIONS                          | MIN  | TYP  | MAX  | UNIT             |
|-------------------------------------------------------------------------------|------------------------------------------|------|------|------|------------------|
| Flash sector size                                                             |                                          |      | 8    |      | KB               |
| Supported flash erase cycles before failure, full bank <sup>(1) (5)</sup>     |                                          | 30   |      |      | k Cycles         |
| Supported flash erase cycles before failure, single sector <sup>(2)</sup>     |                                          | 60   |      |      | k Cycles         |
| Maximum number of write operations per row before sector erase <sup>(3)</sup> |                                          |      |      | 83   | Write Operations |
| Flash retention                                                               | 105 °C                                   | 11.4 |      |      | Years            |
| Flash sector erase current                                                    | Average delta current                    |      | 9.7  |      | mA               |
| Flash sector erase time <sup>(4)</sup>                                        | Zero cycles                              |      | 10   |      | ms               |
|                                                                               | 30k cycles                               |      |      | 4000 | ms               |
| Flash write current                                                           | Average delta current, 4 bytes at a time |      | 5.3  |      | mA               |
| Flash write time <sup>(4)</sup>                                               | 4 bytes at a time                        |      | 21.6 |      | µs               |

- (1) A full bank erase is counted as a single erase cycle on each sector.
- (2) Up to 4 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles
- (3) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.
- (4) This number is dependent on Flash aging and increases over time and erase cycles
- (5) Aborting flash during erase or program modes is not a safe operation.

## 7.8 Thermal Resistance Characteristics

| THERMAL METRIC <sup>(1)</sup> |                                              | PACKAGE       | UNIT                |
|-------------------------------|----------------------------------------------|---------------|---------------------|
|                               |                                              | RGZ<br>(VQFN) |                     |
|                               |                                              | 48 PINS       |                     |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 25.0          | °C/W <sup>(2)</sup> |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 14.5          | °C/W <sup>(2)</sup> |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 8.7           | °C/W <sup>(2)</sup> |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.2           | °C/W <sup>(2)</sup> |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 8.6           | °C/W <sup>(2)</sup> |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 2.1           | °C/W <sup>(2)</sup> |

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(2) °C/W = degrees Celsius per watt.

## 7.9 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

| PARAMETER       | MIN  | TYP | MAX  | UNIT |
|-----------------|------|-----|------|------|
| Frequency bands | 1076 |     | 1315 | MHz  |
|                 | 861  |     | 1054 |      |
|                 | 431  |     | 527  |      |
|                 | 359  |     | 439  |      |
|                 | 287  |     | 351  |      |
|                 | 143  |     | 176  |      |

### 7.10 861MHz to 1054MHz—Receive (RX)

When measured on CC1311-P3EM-7XD7793-PA915 with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{V}$  with DC/DC enabled and high power PA connected to  $V_{\text{DDS}}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER                                                                   | TEST CONDITIONS                                                      | MIN | TYP   | MAX  | UNIT |
|-----------------------------------------------------------------------------|----------------------------------------------------------------------|-----|-------|------|------|
| <b>General Parameters</b>                                                   |                                                                      |     |       |      |      |
| Digital channel filter programmable receive bandwidth                       |                                                                      | 4   |       | 4000 | kHz  |
| Data rate step size                                                         |                                                                      |     | 1.5   |      | bps  |
| Spurious emissions 25MHz to 1GHz                                            | 868MHz                                                               |     | < -57 |      | dBm  |
| Spurious emissions 1GHz to 13GHz                                            | Conducted emissions measured according to ETSI EN 300 220            |     | < -47 |      | dBm  |
| <b>IEEE 802.15.4, 50kbps, ±25kHz Deviation, 2-GFSK, 100kHz RX Bandwidth</b> |                                                                      |     |       |      |      |
| Sensitivity                                                                 | BER = $10^{-2}$ , 868MHz                                             |     | -110  |      | dBm  |
| Saturation limit                                                            | BER = $10^{-2}$ , 868MHz                                             |     | 10    |      | dBm  |
| Selectivity, ±200kHz                                                        | BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                              |     | 44    |      | dB   |
| Selectivity, ±400kHz                                                        | BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                              |     | 48    |      | dB   |
| Blocking, ±1MHz                                                             | BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                              |     | 58    |      | dB   |
| Blocking, ±2MHz                                                             | BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                              |     | 62    |      | dB   |
| Blocking, ±5MHz                                                             | BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                              |     | 70    |      | dB   |
| Blocking, ±10MHz                                                            | BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                              |     | 77    |      | dB   |
| Image rejection (image compensation enabled)                                | BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                              |     | 41    |      | dB   |
| RSSI dynamic range                                                          | Starting from the sensitivity limit                                  |     | 95    |      | dB   |
| RSSI accuracy                                                               | Starting from the sensitivity limit across the given dynamic range   |     | ±3    |      | dB   |
| <b>100kbps, ±25kHz Deviation, 2-GFSK, 137 kHz RX Bandwidth</b>              |                                                                      |     |       |      |      |
| Sensitivity 100kbps                                                         | 1% PER, 127 byte payload, 868MHz                                     |     | -104  |      | dBm  |
| Selectivity, ±200kHz                                                        | 1% PER, 127 byte payload, 868MHz. Wanted signal at -96dBm            |     | 31    |      | dB   |
| Selectivity, ±400kHz                                                        | 1% PER, 127 byte payload, 868MHz. Wanted signal at -96dBm            |     | 37    |      | dB   |
| Co-channel rejection                                                        | 1% PER, 127 byte payload, 868MHz. Wanted signal at -79dBm            |     | -9    |      | dB   |
| <b>200kbps, ±50kHz Deviation, 2-GFSK, 311 kHz RX Bandwidth</b>              |                                                                      |     |       |      |      |
| Sensitivity                                                                 | BER = $10^{-2}$ , 868MHz                                             |     | -103  |      | dBm  |
| Sensitivity                                                                 | BER = $10^{-2}$ , 915MHz                                             |     | -102  |      | dBm  |
| Selectivity, ±400kHz                                                        | BER = $10^{-2}$ , 915MHz. Wanted signal 3dB above sensitivity limit. |     | 45    |      | dB   |
| Selectivity, ±800kHz                                                        | BER = $10^{-2}$ , 915MHz. Wanted signal 3dB above sensitivity limit. |     | 49    |      | dB   |
| Blocking, ±2MHz                                                             | BER = $10^{-2}$ , 915MHz. Wanted signal 3dB above sensitivity limit. |     | 57    |      | dB   |
| Blocking, ±10MHz                                                            | BER = $10^{-2}$ , 915MHz. Wanted signal 3dB above sensitivity limit. |     | 69    |      | dB   |
| <b>500kbps, ±190kHz Deviation, 2-GFSK, 1150kHz RX Bandwidth</b>             |                                                                      |     |       |      |      |
| Sensitivity 500kbps                                                         | 1% PER, 127 byte payload, 915MHz                                     |     | -94   |      | dBm  |
| Selectivity, ±1MHz                                                          | 1% PER, 127 byte payload, 915MHz. Wanted signal at -88dBm            |     | 14    |      | dB   |

## 7.10 861MHz to 1054MHz—Receive (RX) (continued)

When measured on CC1311-P3EM-7XD7793-PA915 with  $T_c = 25^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{V}$  with DC/DC enabled and high power PA connected to  $V_{DD5}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER                                                                                                                                         | TEST CONDITIONS                                                                                                                                    | MIN | TYP     | MAX | UNIT |
|---------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|-----|---------|-----|------|
| Selectivity, $\pm 2\text{MHz}$                                                                                                                    | 1% PER, 127 byte payload, 915MHz. Wanted signal at -88dBm                                                                                          |     | 42      |     | dB   |
| Co-channel rejection                                                                                                                              | 1% PER, 127 byte payload, 915MHz. Wanted signal at -71dBm                                                                                          |     | -9      |     | dB   |
| <b>1 Mbps, <math>\pm 350\text{kHz}</math> Deviation, 2-GFSK, 1.3MHz RX Bandwidth</b>                                                              |                                                                                                                                                    |     |         |     |      |
| Sensitivity                                                                                                                                       | BER = $10^{-2}$ , 868MHz                                                                                                                           |     | -97     |     | dBm  |
| Sensitivity                                                                                                                                       | BER = $10^{-2}$ , 915MHz                                                                                                                           |     | -96     |     | dBm  |
| Blocking, +2MHz                                                                                                                                   | BER = $10^{-2}$ , 915MHz. Wanted signal 3dB above sensitivity limit.                                                                               |     | 43      |     | dB   |
| Blocking, -2MHz                                                                                                                                   | BER = $10^{-2}$ , 915MHz. Wanted signal 3dB above sensitivity limit.                                                                               |     | 26      |     | dB   |
| Blocking, +10MHz                                                                                                                                  | BER = $10^{-2}$ , 915MHz. Wanted signal 3dB above sensitivity limit.                                                                               |     | 54      |     | dB   |
| Blocking, -10MHz                                                                                                                                  | BER = $10^{-2}$ , 915MHz. Wanted signal 3dB above sensitivity limit.                                                                               |     | 48      |     | dB   |
| <b>SimpleLink™ Long Range, 2.5/5kbps (20ksp/s), <math>\pm 5\text{kHz}</math> Deviation, 2-GFSK, 34kHz RX Bandwidth, FEC = 1:2, DSSS = 1:4/1:2</b> |                                                                                                                                                    |     |         |     |      |
| Sensitivity                                                                                                                                       | 2.5kbps, BER = $10^{-2}$ , 868MHz                                                                                                                  |     | -121    |     | dBm  |
| Sensitivity                                                                                                                                       | 5kbps, BER = $10^{-2}$ , 868MHz                                                                                                                    |     | -119    |     | dBm  |
| Saturation limit                                                                                                                                  | 2.5kbps, BER = $10^{-2}$ , 868MHz                                                                                                                  |     | 10      |     | dBm  |
| Selectivity, $\pm 100\text{kHz}$                                                                                                                  | 2.5kbps, BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                                                                                                   |     | 49      |     | dB   |
| Selectivity, $\pm 200\text{kHz}$                                                                                                                  | 2.5kbps, BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                                                                                                   |     | 50      |     | dB   |
| Selectivity, $\pm 300\text{kHz}$                                                                                                                  | 2.5kbps, BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                                                                                                   |     | 51      |     | dB   |
| Blocking, $\pm 1\text{MHz}$                                                                                                                       | 2.5kbps, BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                                                                                                   |     | 63      |     | dB   |
| Blocking, $\pm 2\text{MHz}$                                                                                                                       | 2.5kbps, BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                                                                                                   |     | 69      |     | dB   |
| Blocking, $\pm 5\text{MHz}$                                                                                                                       | 2.5kbps, BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                                                                                                   |     | 79      |     | dB   |
| Blocking, $\pm 10\text{MHz}$                                                                                                                      | 2.5kbps, BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                                                                                                   |     | 88      |     | dB   |
| Image rejection (image compensation enabled)                                                                                                      | 2.5kbps, BER = $10^{-2}$ , 868MHz <sup>(1)</sup>                                                                                                   |     | 47      |     | dB   |
| RSSI dynamic range                                                                                                                                | Starting from the sensitivity limit                                                                                                                |     | 97      |     | dB   |
| RSSI accuracy                                                                                                                                     | Starting from the sensitivity limit across the given dynamic range                                                                                 |     | $\pm 3$ |     | dB   |
| <b>Narrowband, 9.6kbps, <math>\pm 2.4\text{kHz}</math> Deviation, 2-GFSK, 17.1kHz RX Bandwidth</b>                                                |                                                                                                                                                    |     |         |     |      |
| Sensitivity                                                                                                                                       | BER = $10^{-2}$ , 868MHz                                                                                                                           |     | -117    |     | dBm  |
| Adjacent Channel Rejection                                                                                                                        | BER = $10^{-2}$ , 868MHz. Wanted signal 3dB above the ETSI reference sensitivity limit (-104.6dBm). Interferer $\pm 20\text{kHz}$                  |     | 41      |     | dB   |
| Alternate Channel Rejection                                                                                                                       | BER = $10^{-2}$ , 868MHz. Wanted signal 3dB above the ETSI reference sensitivity limit (-104.6dBm). Interferer $\pm 40\text{kHz}$                  |     | 42      |     | dB   |
| Blocking, $\pm 1\text{MHz}$                                                                                                                       | BER = $10^{-2}$ , 868MHz. Wanted signal 3dB above the ETSI reference sensitivity limit (-104.6dBm).                                                |     | 65      |     | dB   |
| Blocking, $\pm 2\text{MHz}$                                                                                                                       | BER = $10^{-2}$ , 868MHz. Wanted signal 3dB above the ETSI reference sensitivity limit (-104.6dBm).                                                |     | 70      |     | dB   |
| Blocking, $\pm 10\text{MHz}$                                                                                                                      | BER = $10^{-2}$ , 868MHz. Wanted signal 3dB above the ETSI reference sensitivity limit (-104.6dBm).                                                |     | 85      |     | dB   |
| <b>Wi-SUN, 2-GFSK</b>                                                                                                                             |                                                                                                                                                    |     |         |     |      |
| Sensitivity                                                                                                                                       | 50kbps, $\pm 12.5\text{kHz}$ deviation, 2-GFSK, 68kHz RX Bandwidth, 868MHz, 10% PER, 250 byte payload                                              |     | -107    |     | dBm  |
| Selectivity, $\pm 100\text{kHz}$ , 50kbps, $\pm 12.5\text{kHz}$ deviation, 2-GFSK, 868.3MHz                                                       | 50kbps, $\pm 12.5\text{kHz}$ deviation, 2-GFSK, 68kHz RX Bandwidth, 868.3MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level |     | 30      |     | dB   |
| Selectivity, $\pm 200\text{kHz}$ , 50kbps, $\pm 12.5\text{kHz}$ deviation, 2-GFSK, 868.3MHz                                                       | 50kbps, $\pm 12.5\text{kHz}$ deviation, 2-GFSK, 68kHz RX Bandwidth, 868.3MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level |     | 36      |     | dB   |
| Sensitivity                                                                                                                                       | 50kbps, $\pm 25\text{kHz}$ deviation, 2-GFSK, 98kHz RX Bandwidth, 918.2MHz, 10% PER, 250 byte payload                                              |     | -106    |     | dBm  |
| Selectivity, $\pm 200\text{kHz}$ , 50kbps, $\pm 25\text{kHz}$ deviation, 2-GFSK, 918.2MHz                                                         | 50kbps, $\pm 25\text{kHz}$ deviation, 2-GFSK, 98kHz RX Bandwidth, 918.2MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level   |     | 34      |     | dB   |

## 7.10 861MHz to 1054MHz—Receive (RX) (continued)

When measured on CC1311-P3EM-7XD7793-PA915 with  $T_c = 25^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{V}$  with DC/DC enabled and high power PA connected to  $V_{DD5}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER                                                                                    | TEST CONDITIONS                                                                                                                                      | MIN | TYP  | MAX | UNIT |
|----------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|------|
| Selectivity, $\pm 400\text{kHz}$ , 50kbps, $\pm 25\text{kHz}$ deviation, 2-GFSK, 918.2MHz    | 50kbps, $\pm 25\text{kHz}$ deviation, 2-GFSK, 98kHz RX Bandwidth, 918.2MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level     |     | 41   |     | dB   |
| Sensitivity                                                                                  | 100kbps, $\pm 25\text{kHz}$ deviation, 2-GFSK, 135kHz RX Bandwidth, 868MHz, 10% PER, 250 byte payload                                                |     | -104 |     | dBm  |
| Selectivity, $\pm 200\text{kHz}$ , 100kbps, $\pm 25\text{kHz}$ deviation, 2-GFSK, 868.3MHz   | 100kbps, $\pm 25\text{kHz}$ deviation, 2-GFSK, 135kHz RX Bandwidth, 868.3MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level   |     | 37   |     | dB   |
| Selectivity, $\pm 400\text{kHz}$ , 100kbps, $\pm 25\text{kHz}$ deviation, 2-GFSK, 868.3MHz   | 100kbps, $\pm 25\text{kHz}$ deviation, 2-GFSK, 135kHz RX Bandwidth, 868.3MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level   |     | 45   |     | dB   |
| Sensitivity                                                                                  | 100kbps, $\pm 50\text{kHz}$ deviation, 2-GFSK, 196kHz RX Bandwidth, 920.9MHz, 10% PER, 250 byte payload                                              |     | -102 |     | dBm  |
| Selectivity, $\pm 400\text{kHz}$ , 100kbps, $\pm 50\text{kHz}$ deviation, 2-GFSK, 920.9MHz   | 100kbps, $\pm 50\text{kHz}$ deviation, 2-GFSK, 196kHz RX Bandwidth, 920.9MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level   |     | 40   |     | dB   |
| Selectivity, $\pm 800\text{kHz}$ , 100kbps, $\pm 50\text{kHz}$ deviation, 2-GFSK, 920.9MHz   | 100kbps, $\pm 50\text{kHz}$ deviation, 2-GFSK, 196kHz RX Bandwidth, 920.9MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level   |     | 49   |     | dB   |
| Sensitivity                                                                                  | 150kbps, $\pm 37.5\text{kHz}$ deviation, 2-GFSK, 273kHz RX Bandwidth, 920.9MHz, 10% PER, 250 byte payload                                            |     | -99  |     | dBm  |
| Selectivity, $\pm 400\text{kHz}$ , 150kbps, $\pm 37.5\text{kHz}$ deviation, 2-GFSK, 920.9MHz | 150kbps, $\pm 37.5\text{kHz}$ deviation, 2-GFSK, 273kHz RX Bandwidth, 920.9MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level |     | 41   |     | dB   |
| Selectivity, $\pm 800\text{kHz}$ , 150kbps, $\pm 37.5\text{kHz}$ deviation, 2-GFSK, 920.9MHz | 150kbps, $\pm 37.5\text{kHz}$ deviation, 2-GFSK, 273kHz RX Bandwidth, 920.9MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level |     | 47   |     | dB   |
| Sensitivity                                                                                  | 200kbps, $\pm 50\text{kHz}$ deviation, 2-GFSK, 918.4MHz, 273kHz RX BW, 10% PER, 250 byte payload                                                     |     | -99  |     | dBm  |
| Selectivity, $\pm 400\text{kHz}$ , 200kbps, $\pm 50\text{kHz}$ deviation, 2-GFSK, 918.4MHz   | 200kbps, $\pm 50\text{kHz}$ deviation, 2-GFSK, 273kHz RX Bandwidth, 918.4MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level   |     | 42   |     | dB   |
| Selectivity, $\pm 800\text{kHz}$ , 200kbps, $\pm 50\text{kHz}$ deviation, 2-GFSK, 918.4MHz   | 200kbps, $\pm 50\text{kHz}$ deviation, 2-GFSK, 273kHz RX Bandwidth, 918.4MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level   |     | 49   |     | dB   |
| Sensitivity                                                                                  | 200kbps, $\pm 100\text{kHz}$ deviation, 2-GFSK, 273kHz RX Bandwidth, 920.8MHz, 10% PER, 250 byte payload                                             |     | -99  |     | dBm  |
| Selectivity, $\pm 600\text{kHz}$ , 200kbps, $\pm 100\text{kHz}$ deviation, 2-GFSK, 920.8MHz  | 200kbps, $\pm 100\text{kHz}$ deviation, 2-GFSK, 273kHz RX Bandwidth, 920.8MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level  |     | 45   |     | dB   |
| Selectivity, $\pm 1200\text{kHz}$ , 200kbps, $\pm 100\text{kHz}$ deviation, 2-GFSK, 920.8MHz | 200kbps, $\pm 100\text{kHz}$ deviation, 2-GFSK, 273kHz RX Bandwidth, 920.8MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level  |     | 52   |     | dB   |
| Sensitivity                                                                                  | 300kbps, $\pm 75\text{kHz}$ deviation, 2-GFSK, 917.6MHz, 498kHz RX BW, 10% PER, 250 byte payload                                                     |     | -97  |     | dBm  |
| Selectivity, $\pm 600\text{kHz}$ , 300kbps, $\pm 75\text{kHz}$ deviation, 2-GFSK, 917.6MHz   | 300kbps, $\pm 75\text{kHz}$ deviation, 2-GFSK, 498kHz RX Bandwidth, 917.6MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level   |     | 42   |     | dB   |
| Selectivity, $\pm 1200\text{kHz}$ , 300kbps, $\pm 75\text{kHz}$ deviation, 2-GFSK, 917.6MHz  | 300kbps, $\pm 75\text{kHz}$ deviation, 2-GFSK, 498kHz RX Bandwidth, 917.6MHz, 10% PER, 250 byte payload. Wanted signal 3dB above sensitivity level   |     | 47   |     | dB   |

(1) Wanted signal 3dB above the reference sensitivity limit according to ETSI EN 300 220V. 3.1.1

## 7.11 861 MHz to 1054 MHz - Transmit (TX)

Measured on the CC1311-P3EM-7XD7793-PA915 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{ V}$  with DC/DC enabled and high power PA connected to  $V_{\text{DDS}}$  using 2-GFSK, 50 kbps,  $\pm 25\text{ kHz}$  deviation unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted. <sup>(1)</sup>

| PARAMETER                                                                              |                                                                          | TEST CONDITIONS                                                                                | MIN | TYP       | MAX | UNIT |
|----------------------------------------------------------------------------------------|--------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|-----|-----------|-----|------|
| <b>General parameters</b>                                                              |                                                                          |                                                                                                |     |           |     |      |
| Max output power, boost mode<br>Regular PA                                             |                                                                          | VDDR = 1.95 V<br>Minimum supply voltage (VDDS ) for boost mode is 2.1 V<br>868 MHz and 915 MHz |     | 14        |     | dBm  |
| Max output power,<br>Regular PA                                                        |                                                                          | 868 MHz and 915 MHz                                                                            |     | 13        |     | dBm  |
| Max output power,<br>High power PA                                                     |                                                                          | 915 MHz<br>VDDS = 3.3V                                                                         |     | 20        |     | dBm  |
| Output power programmable range<br>Regular PA                                          |                                                                          | 868 MHz and 915 MHz                                                                            |     | 24        |     | dB   |
| Output power programmable range<br>High power PA                                       |                                                                          | 868 MHz and 915 MHz<br>VDDS = 3.3V                                                             |     | 6         |     | dB   |
| Output power variation over temperature<br>Regular PA                                  |                                                                          | +10 dBm setting<br>Over recommended temperature operating range                                |     | $\pm 2$   |     | dB   |
| Output power variation over temperature<br>Boost mode, regular PA                      |                                                                          | +14 dBm setting<br>Over recommended temperature operating range                                |     | $\pm 1.5$ |     | dB   |
| <b>Spurious emissions and harmonics</b>                                                |                                                                          |                                                                                                |     |           |     |      |
| Spurious emissions<br>(excluding harmonics)<br>Regular PA <sup>(2)</sup>               | 30 MHz to 1 GHz                                                          | +14 dBm setting<br>ETSI restricted bands                                                       |     | < -54     |     | dBm  |
|                                                                                        |                                                                          | +14 dBm setting<br>ETSI outside restricted bands                                               |     | < -36     |     | dBm  |
|                                                                                        | 1 GHz to 12.75 GHz<br>(outside ETSI restricted bands)                    | +14 dBm setting<br>measured in 1 MHz bandwidth (ETSI)                                          |     | < -30     |     | dBm  |
| Spurious emissions out-of-band<br>Regular PA, 915 MHz <sup>(2)</sup>                   | 30 MHz to 88 MHz<br>(within FCC restricted bands)                        | +14 dBm setting                                                                                |     | < -56     |     | dBm  |
|                                                                                        | 88 MHz to 216 MHz<br>(within FCC restricted bands)                       | +14 dBm setting                                                                                |     | < -52     |     | dBm  |
|                                                                                        | 216 MHz to 960 MHz<br>(within FCC restricted bands)                      | +14 dBm setting                                                                                |     | < -50     |     | dBm  |
|                                                                                        | 960 MHz to 2390 MHz and above<br>2483.5 MHz (within FCC restricted band) | +14 dBm setting                                                                                |     | < -42     |     | dBm  |
|                                                                                        | 1 GHz to 12.75 GHz<br>(outside FCC restricted bands)                     | +14 dBm setting                                                                                |     | < -40     |     | dBm  |
| Spurious emissions out-of-band<br>High power PA, 915 MHz <sup>(2)</sup> <sup>(3)</sup> | 30 MHz to 88 MHz<br>(within FCC restricted bands)                        | +20 dBm setting, VDDS = 3.3 V                                                                  |     | < -55     |     | dBm  |
|                                                                                        | 88 MHz to 216 MHz<br>(within FCC restricted bands)                       | +20 dBm setting, VDDS = 3.3 V                                                                  |     | < -52     |     | dBm  |
|                                                                                        | 216 MHz to 960 MHz<br>(within FCC restricted bands)                      | +20 dBm setting, VDDS = 3.3 V                                                                  |     | < -49     |     | dBm  |
|                                                                                        | 960 MHz to 2390 MHz and above<br>2483.5 MHz (within FCC restricted band) | +20 dBm setting, VDDS = 3.3 V                                                                  |     | < -41     |     | dBm  |
|                                                                                        | 1 GHz to 12.75 GHz<br>(outside FCC restricted bands)                     | +20 dBm setting, VDDS = 3.3 V                                                                  |     | < -20     |     | dBm  |

## 7.11 861 MHz to 1054 MHz - Transmit (TX) (continued)

Measured on the CC1311-P3EM-7XD7793-PA915 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$  with DC/DC enabled and high power PA connected to  $V_{DD5}$  using 2-GFSK, 50 kbps,  $\pm 25\text{ kHz}$  deviation unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted. <sup>(1)</sup>

| PARAMETER                                                                  |                                                     | TEST CONDITIONS                                     | MIN | TYP   | MAX | UNIT |
|----------------------------------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----|-------|-----|------|
| Spurious emissions out-of-band<br>Regular PA, 920.6/928 MHz <sup>(2)</sup> | Below 710 MHz (ARIB T-108)                          | +14 dBm setting                                     |     | < -36 |     | dBm  |
|                                                                            | 710 MHz to 900 MHz (ARIB T-108)                     | +14 dBm setting                                     |     | < -55 |     | dBm  |
|                                                                            | 900 MHz to 915 MHz (ARIB T-108)                     | +14 dBm setting                                     |     | < -55 |     | dBm  |
|                                                                            | 930 MHz to 1000 MHz (ARIB T-108)                    | +14 dBm setting                                     |     | < -55 |     | dBm  |
|                                                                            | 1000 MHz to 1215 MHz (ARIB T-108)                   | +14 dBm setting                                     |     | < -45 |     | dBm  |
|                                                                            | Above 1215 MHz (ARIB T-108)                         | +14 dBm setting                                     |     | < -30 |     | dBm  |
| Harmonics<br>Regular PA                                                    | Second harmonic                                     | +14 dBm setting, 868 MHz                            |     | < -30 |     | dBm  |
|                                                                            |                                                     | +14 dBm setting, 915 MHz                            |     | < -30 |     |      |
|                                                                            | Third harmonic                                      | +14 dBm setting, 868 MHz                            |     | < -30 |     | dBm  |
|                                                                            |                                                     | +14 dBm setting, 915 MHz                            |     | < -42 |     |      |
|                                                                            | Fourth harmonic                                     | +14 dBm setting, 868 MHz                            |     | < -30 |     | dBm  |
|                                                                            |                                                     | +14 dBm setting, 915 MHz                            |     | < -30 |     |      |
|                                                                            | Fifth harmonic                                      | +14 dBm setting, 868 MHz                            |     | < -30 |     | dBm  |
|                                                                            |                                                     | +14 dBm setting, 915 MHz                            |     | < -42 |     |      |
| Harmonics<br>High power PA                                                 | Second harmonic                                     | +20 dBm setting, $V_{DD5} = 3.3\text{ V}$ , 915 MHz |     | < -30 |     | dBm  |
|                                                                            | Third harmonic                                      | +20 dBm setting, $V_{DD5} = 3.3\text{ V}$ , 915 MHz |     | < -42 |     | dBm  |
|                                                                            | Fourth harmonic                                     | +20 dBm setting, $V_{DD5} = 3.3\text{ V}$ , 915 MHz |     | < -30 |     | dBm  |
|                                                                            | Fifth harmonic                                      | +20 dBm setting, $V_{DD5} = 3.3\text{ V}$ , 915 MHz |     | < -42 |     | dBm  |
| <b>Adjacent Channel Power</b>                                              |                                                     |                                                     |     |       |     |      |
| Adjacent channel power, regular 14 dBm PA                                  | Adjacent channel, 20 kHz offset. 9.6 kbps, $h=0.5$  | 12.5 dBm setting. 868.3 MHz. 14 kHz channel BW      |     | -23   |     | dBm  |
| Alternate channel power, regular 14 dBm PA                                 | Alternate channel, 40 kHz offset. 9.6 kbps, $h=0.5$ | 12.5 dBm setting. 868.3 MHz. 14 kHz channel BW      |     | -30   |     | dBm  |

- (1) Some combinations of frequency, data rate and modulation format requires use of external crystal load capacitors for regulatory compliance. More details can be found in the device errata.
- (2) Suitable for systems targeting compliance with EN 300 220, EN 303 131, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.
- (3) Spurious emissions increase for supply voltages below 2.2 V. As such, care must be taken to ensure regulatory requirements are met when operating at low supply voltage levels. An alternative is to use the Sub-1 GHz PA below 2.2 V.

## 7.12 861 MHz to 1054 MHz - PLL Phase Noise Wideband Mode

When measured on the CC1311-P3EM-7XD7793-PA915 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ .

| PARAMETER                                                              | TEST CONDITIONS               | MIN | TYP  | MAX | UNIT   |
|------------------------------------------------------------------------|-------------------------------|-----|------|-----|--------|
| Phase noise in the 868- and 915-MHz bands<br>20 kHz PLL loop bandwidth | $\pm 10\text{ kHz}$ offset    |     | -76  |     | dBc/Hz |
|                                                                        | $\pm 100\text{ kHz}$ offset   |     | -98  |     | dBc/Hz |
|                                                                        | $\pm 200\text{ kHz}$ offset   |     | -106 |     | dBc/Hz |
|                                                                        | $\pm 400\text{ kHz}$ offset   |     | -113 |     | dBc/Hz |
|                                                                        | $\pm 1000\text{ kHz}$ offset  |     | -122 |     | dBc/Hz |
|                                                                        | $\pm 2000\text{ kHz}$ offset  |     | -130 |     | dBc/Hz |
|                                                                        | $\pm 10000\text{ kHz}$ offset |     | -140 |     | dBc/Hz |

### 7.13 861 MHz to 1054 MHz - PLL Phase Noise Narrowband Mode

When measured on the CC1311-P3EM-7XD7793-PA915 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DD5}} = 3.0\text{ V}$ .

| PARAMETER                                                               | TEST CONDITIONS   | MIN | TYP  | MAX | UNIT   |
|-------------------------------------------------------------------------|-------------------|-----|------|-----|--------|
| Phase noise in the 868- and 915-MHz bands<br>150 kHz PLL loop bandwidth | ±10 kHz offset    |     | -95  |     | dBc/Hz |
|                                                                         | ±100 kHz offset   |     | -94  |     | dBc/Hz |
|                                                                         | ±200 kHz offset   |     | -94  |     | dBc/Hz |
|                                                                         | ±400 kHz offset   |     | -103 |     | dBc/Hz |
|                                                                         | ±1000 kHz offset  |     | -119 |     | dBc/Hz |
|                                                                         | ±2000 kHz offset  |     | -129 |     | dBc/Hz |
|                                                                         | ±10000 kHz offset |     | -138 |     | dBc/Hz |

### 7.14 359MHz to 527MHz—Receive (RX)

When measured on a CC1311-P3EM-7XD7793-PA915 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DD5}} = 3.0\text{V}$  with DC/DC enabled and high power PA connected to  $V_{\text{DD5}}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high-power PA, which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER                                                                                                                  | TEST CONDITIONS                                                    | MIN | TYP   | MAX | UNIT |
|----------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------|-----|-------|-----|------|
| <b>General Parameters</b>                                                                                                  |                                                                    |     |       |     |      |
| Spurious emissions 25MHz to 1GHz                                                                                           | 433.92MHz                                                          |     | < -57 |     | dBm  |
| Spurious emissions 1GHz to 13GHz                                                                                           | Conducted emissions measured according to ETSI EN 300 220          |     | < -47 |     | dBm  |
| <b>IEEE 802.15.4, 50kbps, ±25kHz Deviation, 2-GFSK, 78kHz RX Bandwidth</b>                                                 |                                                                    |     |       |     |      |
| Sensitivity                                                                                                                | BER = $10^{-2}$ , 433.92MHz                                        |     | -110  |     | dBm  |
| Saturation limit                                                                                                           | BER = $10^{-2}$ , 433.92MHz                                        |     | 10    |     | dBm  |
| Selectivity, +200kHz                                                                                                       | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 48    |     | dB   |
| Selectivity, -200kHz                                                                                                       | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 43    |     | dB   |
| Selectivity, +400kHz                                                                                                       | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 53    |     | dB   |
| Selectivity, -400kHz                                                                                                       | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 44    |     | dB   |
| Blocking, +1MHz                                                                                                            | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 60    |     | dB   |
| Blocking, -1MHz                                                                                                            | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 54    |     | dB   |
| Blocking, +2MHz                                                                                                            | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 62    |     | dB   |
| Blocking, -2MHz                                                                                                            | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 61    |     | dB   |
| Blocking, +10MHz                                                                                                           | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 75    |     | dB   |
| Blocking, -10MHz                                                                                                           | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 75    |     | dB   |
| Image rejection (image compensation enabled)                                                                               | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 44    |     | dB   |
| RSSI dynamic range                                                                                                         | Starting from the sensitivity limit                                |     | 95    |     | dB   |
| RSSI accuracy                                                                                                              | Starting from the sensitivity limit across the given dynamic range |     | ±3    |     | dB   |
| <b>200kbps, ±50kHz Deviation, 2-GFSK, 273kHz RX Bandwidth</b>                                                              |                                                                    |     |       |     |      |
| Sensitivity                                                                                                                | BER = $10^{-2}$ , 433.92MHz                                        |     | -104  |     | dBm  |
| Saturation limit                                                                                                           | BER = $10^{-2}$ , 433.92MHz                                        |     | 10    |     | dBm  |
| Selectivity, ±400kHz                                                                                                       | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 48    |     | dB   |
| Blocking, ±1MHz                                                                                                            | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 52    |     | dB   |
| Blocking, ±2MHz                                                                                                            | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 55    |     | dB   |
| Blocking, ±10MHz                                                                                                           | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 68    |     | dB   |
| Image rejection (image compensation enabled)                                                                               | BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                         |     | 45    |     | dB   |
| RSSI dynamic range                                                                                                         | Starting from the sensitivity limit                                |     | 89    |     | dB   |
| RSSI accuracy                                                                                                              | Starting from the sensitivity limit across the given dynamic range |     | ±3    |     | dB   |
| <b>SimpleLink™ Long Range, 2.5/5kbps (20 ksps), ±5kHz Deviation, 2-GFSK, 34kHz RX Bandwidth, FEC = 1:2, DSSS = 1:4/1:2</b> |                                                                    |     |       |     |      |
| Sensitivity                                                                                                                | 2.5kbps, BER = $10^{-2}$ , 433.92MHz                               |     | -121  |     | dBm  |
| Sensitivity                                                                                                                | 5kbps, BER = $10^{-2}$ , 433.92MHz                                 |     | -119  |     | dBm  |

## 7.14 359MHz to 527MHz—Receive (RX) (continued)

When measured on a CC1311-P3EM-7XD7793-PA915 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DD5}} = 3.0\text{V}$  with DC/DC enabled and high power PA connected to  $V_{\text{DD5}}$  unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high-power PA, which is measured at a dedicated antenna connection. All measurements are performed conducted.

| PARAMETER                                    | TEST CONDITIONS                                                    | MIN | TYP | MAX | UNIT |
|----------------------------------------------|--------------------------------------------------------------------|-----|-----|-----|------|
| Saturation limit                             | 5kbps, BER = $10^{-2}$ , 433.92MHz                                 |     | 10  |     | dBm  |
| Selectivity, +100kHz                         | 5kbps, BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                  |     | 55  |     | dB   |
| Selectivity, -100kHz                         | 5kbps, BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                  |     | 53  |     | dB   |
| Blocking, +1MHz                              | 5kbps, BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                  |     | 69  |     | dB   |
| Blocking, -1MHz                              | 5kbps, BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                  |     | 65  |     | dB   |
| Blocking, +2MHz                              | 5kbps, BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                  |     | 71  |     | dB   |
| Blocking, -2MHz                              | 5kbps, BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                  |     | 70  |     | dB   |
| Blocking, +10MHz                             | 5kbps, BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                  |     | 84  |     | dB   |
| Blocking, -10MHz                             | 5kbps, BER = $10^{-2}$ , 433.92MHz <sup>(1)</sup>                  |     | 84  |     | dB   |
| Image rejection (image compensation enabled) | 5kbps, BER = $10^{-2}$ , 433.92MHz                                 |     | 49  |     | dB   |
| RSSI dynamic range                           | Starting from the sensitivity limit                                |     | 101 |     | dB   |
| RSSI accuracy                                | Starting from the sensitivity limit across the given dynamic range |     | ±3  |     | dB   |

(1) Wanted signal 3dB above sensitivity limit

## 7.15 359 MHz to 527 MHz - Transmit (TX)

Measured on the LAUNCHXL-CC1352P-4 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$  with DC/DC enabled unless otherwise noted.

All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted. <sup>(1)</sup>

| PARAMETER                                                          |                                                    | TEST CONDITIONS                                                             | MIN | TYP       | MAX | UNIT |
|--------------------------------------------------------------------|----------------------------------------------------|-----------------------------------------------------------------------------|-----|-----------|-----|------|
| <b>General parameters</b>                                          |                                                    |                                                                             |     |           |     |      |
| Max output power, Regular PA                                       |                                                    | 433.92 MHz, without BOOST ( $V_{DDR} = 1.7\text{ V}$ )                      |     | 13        |     | dBm  |
| Output power programmable range Regular PA                         |                                                    | 433.92 MHz, without BOOST ( $V_{DDR} = 1.7\text{ V}$ )                      |     | 24        |     | dB   |
| Output power variation over temperature, regular PA                |                                                    | +13 dBm setting, 433.92 MHz<br>Over recommended temperature operating range |     | $\pm 1.5$ |     | dB   |
| <b>Spurious emissions and harmonics</b>                            |                                                    |                                                                             |     |           |     |      |
| Spurious emissions (excluding harmonics) Regular PA <sup>(2)</sup> | 30 MHz to 1 GHz                                    | +10 dBm setting<br>ETSI restricted bands                                    |     | < -54     |     | dBm  |
|                                                                    |                                                    | +10 dBm setting<br>ETSI outside restricted bands                            |     | < -36     |     | dBm  |
|                                                                    | 1 GHz to 12.75 GHz (outside ETSI restricted bands) | +10 dBm setting<br>measured in 1 MHz bandwidth (ETSI)                       |     | < -30     |     | dBm  |
| Spurious emissions out-of-band Regular PA, 429 MHz <sup>(2)</sup>  | Outside the necessary frequency band (ARIB T-67)   | +10 dBm setting                                                             |     | < -26     |     | dBm  |
|                                                                    | 710 MHz to 900 MHz (ARIB T-67)                     | +10 dBm setting                                                             |     | < -55     |     | dBm  |
|                                                                    | 900 MHz to 915 MHz (ARIB T-67)                     | +10 dBm setting                                                             |     | < -55     |     | dBm  |
|                                                                    | 930 MHz to 1000 MHz (ARIB T-67)                    | +10 dBm setting                                                             |     | < -55     |     | dBm  |
|                                                                    | 1000 MHz to 1215 MHz (ARIB T-67)                   | +10 dBm setting                                                             |     | < -45     |     | dBm  |
|                                                                    | Above 1215 MHz (ARIB T-67)                         | +10 dBm setting                                                             |     | < -30     |     | dBm  |
| Harmonics Regular PA                                               | Second harmonic                                    | +13 dBm setting, 433 MHz                                                    |     | < -36     |     | dBm  |
| Harmonics Regular PA                                               | Third harmonic                                     | +13 dBm setting, 433 MHz                                                    |     | < -30     |     | dBm  |
| Harmonics Regular PA                                               | Fourth harmonic                                    | +13 dBm setting, 433 MHz                                                    |     | < -30     |     | dBm  |
| Harmonics Regular PA                                               | Fifth harmonic                                     | +13 dBm setting, 433 MHz                                                    |     | < -30     |     | dBm  |

(1) Some combinations of frequency, data rate and modulation format requires use of external crystal load capacitors for regulatory compliance. More details can be found in the device errata.

(2) Suitable for systems targeting compliance with EN 300 220, EN 303 131, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.

## 7.16 359 MHz to 527 MHz - PLL Phase Noise

When measured on the LAUNCHXL-CC1352P-4 reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ .

| PARAMETER                                                    | TEST CONDITIONS               | MIN | TYP  | MAX | UNIT   |
|--------------------------------------------------------------|-------------------------------|-----|------|-----|--------|
| Phase noise in the 433 MHz band<br>20 kHz PLL loop bandwidth | $\pm 10\text{ kHz}$ offset    |     | -82  |     | dBc/Hz |
|                                                              | $\pm 100\text{ kHz}$ offset   |     | -105 |     | dBc/Hz |
|                                                              | $\pm 200\text{ kHz}$ offset   |     | -112 |     | dBc/Hz |
|                                                              | $\pm 400\text{ kHz}$ offset   |     | -119 |     | dBc/Hz |
|                                                              | $\pm 1000\text{ kHz}$ offset  |     | -127 |     | dBc/Hz |
|                                                              | $\pm 2000\text{ kHz}$ offset  |     | -133 |     | dBc/Hz |
|                                                              | $\pm 10000\text{ kHz}$ offset |     | -141 |     | dBc/Hz |

## 7.17 Timing and Switching Characteristics

### 7.17.1 Reset Timing

| PARAMETER            | MIN | TYP | MAX | UNIT |
|----------------------|-----|-----|-----|------|
| RESET_N low duration | 1   |     |     | μs   |

### 7.17.2 Wakeup Timing

Measured over operating free-air temperature with  $V_{DD5} = 3.0\text{ V}$  (unless otherwise noted). The times listed here do not include software overhead.

| PARAMETER               | TEST CONDITIONS | MIN        | TYP | MAX | UNIT |
|-------------------------|-----------------|------------|-----|-----|------|
| MCU, Reset to Active    |                 | 850 - 4000 |     |     | μs   |
| MCU, Shutdown to Active |                 | 850 - 4000 |     |     | μs   |
| MCU, Standby to Active  |                 | 160        |     |     | μs   |
| MCU, Active to Standby  |                 | 36         |     |     | μs   |
| MCU, Idle to Active     |                 | 14         |     |     | μs   |

### 7.17.3 Clock Specifications

#### 7.17.3.1 48 MHz Crystal Oscillator (XOSC\_HF)

Measured on a Texas Instruments reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{ V}$ , unless otherwise noted.<sup>(1)</sup>

|       | PARAMETER                                                                                                           | MIN | TYP                           | MAX | UNIT          |
|-------|---------------------------------------------------------------------------------------------------------------------|-----|-------------------------------|-----|---------------|
|       | Crystal frequency                                                                                                   |     | 48                            |     | MHz           |
| ESR   | Equivalent series resistance<br>$6\text{ pF} < C_L \leq 9\text{ pF}$                                                |     | 20                            | 60  | $\Omega$      |
| ESR   | Equivalent series resistance<br>$5\text{ pF} < C_L \leq 6\text{ pF}$                                                |     |                               | 80  | $\Omega$      |
| $L_M$ | Motional inductance, relates to the load capacitance that is used for the crystal ( $C_L$ in Farads) <sup>(5)</sup> |     | $< 3 \times 10^{-25} / C_L^2$ |     | H             |
| $C_L$ | Crystal load capacitance <sup>(4)</sup>                                                                             | 5   | 7 <sup>(3)</sup>              | 9   | pF            |
|       | Start-up time <sup>(2)</sup>                                                                                        |     | 200                           |     | $\mu\text{s}$ |

- (1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.
- (2) Start-up time using the TI-provided power driver. Start-up time may increase if driver is not used.
- (3) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the Customer Configuration section (CCFG).
- (4) Adjustable load capacitance is integrated into the device. External load capacitors are required for systems targeting compliance with certain regulations. See the device errata for further details.
- (5) The crystal manufacturer's specification must satisfy this requirement for proper operation.

#### 7.17.3.2 48 MHz RC Oscillator (RCOSC\_HF)

Measured on a Texas Instruments reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{ V}$ , unless otherwise noted.

|                                              | MIN | TYP        | MAX | UNIT          |
|----------------------------------------------|-----|------------|-----|---------------|
| Frequency                                    |     | 48         |     | MHz           |
| Uncalibrated frequency accuracy              |     | $\pm 1$    |     | %             |
| Calibrated frequency accuracy <sup>(1)</sup> |     | $\pm 0.25$ |     | %             |
| Start-up time                                |     | 5          |     | $\mu\text{s}$ |

- (1) Accuracy relative to the calibration source (XOSC\_HF)

#### 7.17.3.3 32.768 kHz Crystal Oscillator (XOSC\_LF)

Measured on a Texas Instruments reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{ V}$ , unless otherwise noted.

|                   | MIN | TYP              | MAX | UNIT       |
|-------------------|-----|------------------|-----|------------|
| Crystal frequency |     | 32.768           |     | kHz        |
| ESR               |     | 30               | 100 | k $\Omega$ |
| $C_L$             | 6   | 7 <sup>(1)</sup> | 12  | pF         |

- (1) Default load capacitance using TI reference designs including parasitic capacitance. Crystals with different load capacitance may be used.

#### 7.17.3.4 32 kHz RC Oscillator (RCOSC\_LF)

Measured on a Texas Instruments reference design with  $T_c = 25^\circ\text{C}$ ,  $V_{\text{DDS}} = 3.0\text{ V}$ , unless otherwise noted.

|                                               |                                                        | MIN | TYP                 | MAX | UNIT   |
|-----------------------------------------------|--------------------------------------------------------|-----|---------------------|-----|--------|
| Calibrated frequency                          |                                                        |     | 32.8                |     | kHz    |
| Calibrated<br>RTC<br>variation <sup>(1)</sup> | Calibrated periodically against XOSC_HF <sup>(2)</sup> |     | ±600 <sup>(3)</sup> |     | ppm    |
| Temperature coefficient.                      |                                                        |     | 50                  |     | ppm/°C |

- (1) When using RCOSC\_LF as source for the low frequency system clock (SCLK\_LF), the accuracy of the SCLK\_LF-derived Real Time Clock (RTC) can be improved by measuring RCOSC\_LF relative to XOSC\_HF and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.
- (2) TI driver software calibrates the RTC every time XOSC\_HF is enabled.
- (3) Some device's variation can exceed 1000 ppm. Further calibration will not improve variation.

## 7.17.4 Synchronous Serial Interface (SSI) Characteristics

### 7.17.4.1 Synchronous Serial Interface (SSI) Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER NO.     | PARAMETER              |                   | MIN | TYP | MAX   | UNIT                         |
|-------------------|------------------------|-------------------|-----|-----|-------|------------------------------|
| S1                | $t_{\text{clk\_per}}$  | SSIClk cycle time | 12  |     | 65024 | System Clocks <sup>(2)</sup> |
| S2 <sup>(1)</sup> | $t_{\text{clk\_high}}$ | SSIClk high time  |     | 0.5 |       | $t_{\text{clk\_per}}$        |
| S3 <sup>(1)</sup> | $t_{\text{clk\_low}}$  | SSIClk low time   |     | 0.5 |       | $t_{\text{clk\_per}}$        |

(1) Refer to SSI timing diagrams [Figure 7-1](#), [Figure 7-2](#), and [Figure 7-3](#).

(2) When using the TI-provided Power driver, the SSI system clock is always 48 MHz.

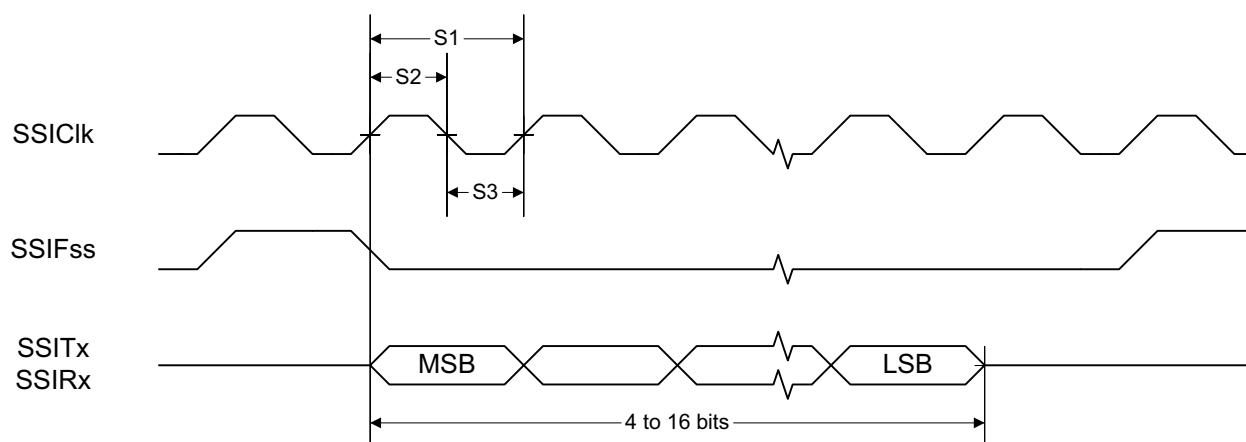


Figure 7-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

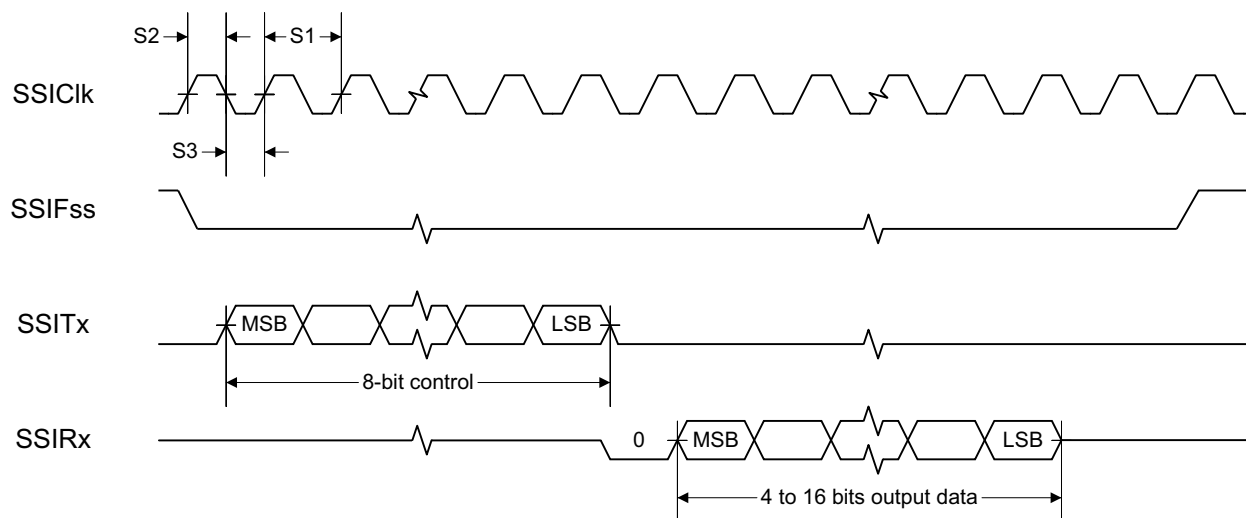


Figure 7-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

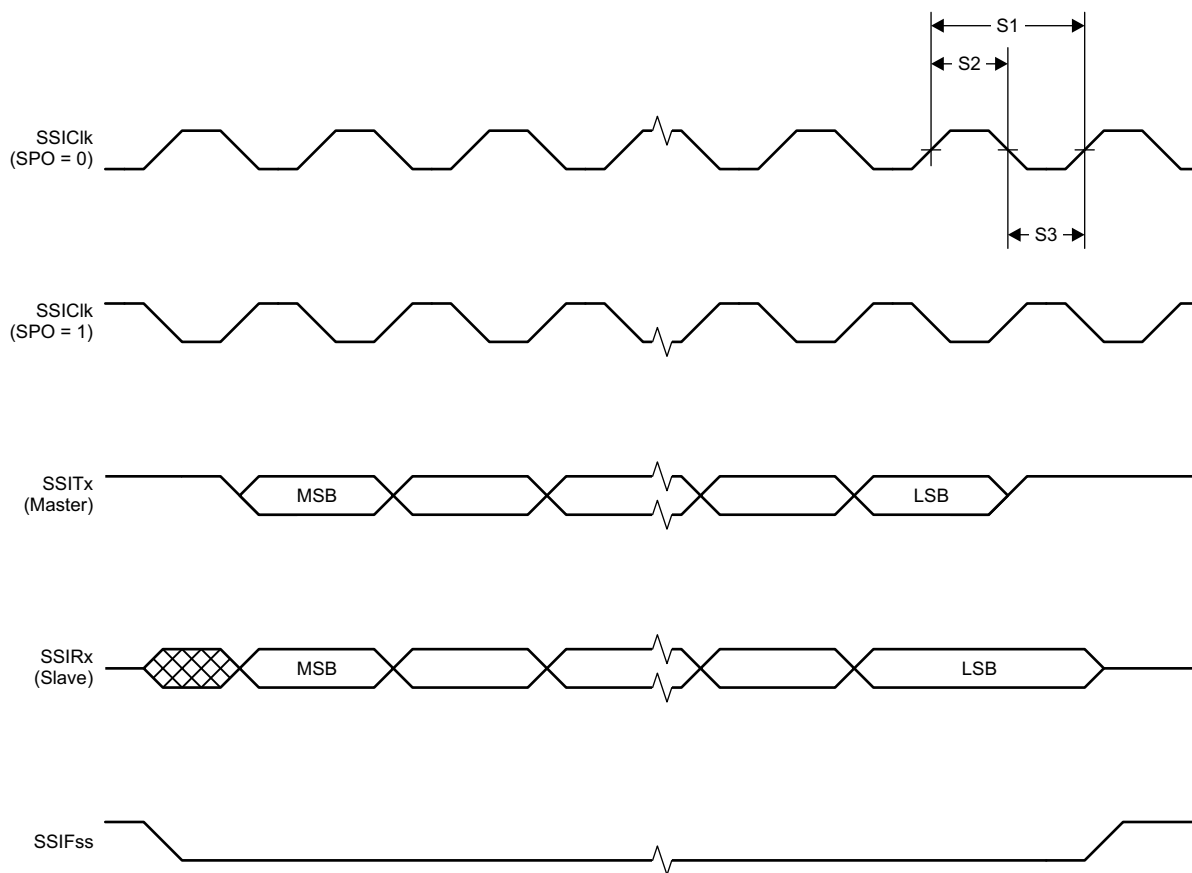


**Figure 7-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1**

## 7.17.5 UART

### 7.17.5.1 UART Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT  |
|-----------|-----|-----|-----|-------|
| UART rate |     |     | 3   | MBaud |

## 7.18 Peripheral Characteristics

### 7.18.1 ADC

#### 7.18.1.1 Analog-to-Digital Converter (ADC) Characteristics

$T_c = 25^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$  and voltage scaling enabled, unless otherwise noted.<sup>(1)</sup>

Performance numbers require use of offset and gain adjustments in software by TI-provided ADC drivers.

| PARAMETER           | TEST CONDITIONS                                    | MIN                                                                                                                                                                                                                             | TYP   | MAX                               | UNIT         |
|---------------------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-----------------------------------|--------------|
| Input voltage range |                                                    | 0                                                                                                                                                                                                                               |       | $V_{DD5}$                         | V            |
| Resolution          |                                                    |                                                                                                                                                                                                                                 | 12    |                                   | Bits         |
| Sample Rate         |                                                    |                                                                                                                                                                                                                                 |       | 200                               | ksps         |
| Offset              | Internal 4.3 V equivalent reference <sup>(2)</sup> |                                                                                                                                                                                                                                 | −0.24 |                                   | LSB          |
| Gain error          | Internal 4.3 V equivalent reference <sup>(2)</sup> |                                                                                                                                                                                                                                 | 7.14  |                                   | LSB          |
| DNL <sup>(4)</sup>  | Differential nonlinearity                          |                                                                                                                                                                                                                                 | >−1   |                                   | LSB          |
| INL                 | Integral nonlinearity                              |                                                                                                                                                                                                                                 | ±4    |                                   | LSB          |
| ENOB                | Effective number of bits                           | Internal 4.3 V equivalent reference <sup>(2)</sup> , 200 kSamples/s, 9.6 kHz input tone                                                                                                                                         |       | 9.8                               | Bits         |
|                     |                                                    | Internal 4.3 V equivalent reference <sup>(2)</sup> , 200 kSamples/s, 9.6 kHz input tone, DC/DC enabled                                                                                                                          |       | 9.8                               |              |
|                     |                                                    | $V_{DD5}$ as reference, 200 kSamples/s, 9.6 kHz input tone                                                                                                                                                                      |       | 10.1                              |              |
|                     |                                                    | Internal reference, voltage scaling disabled, 32 samples average (software), 200 kSamples/s, 300 Hz input tone                                                                                                                  |       | 11.1                              |              |
|                     |                                                    | Internal reference, voltage scaling disabled, 14-bit mode, 200 kSamples/s, 300 Hz input tone <sup>(5)</sup>                                                                                                                     |       | 11.3                              |              |
|                     |                                                    | Internal reference, voltage scaling disabled, 15-bit mode, 200 kSamples/s, 300 Hz input tone <sup>(5)</sup>                                                                                                                     |       | 11.6                              |              |
| THD                 | Total harmonic distortion                          | Internal 4.3 V equivalent reference <sup>(2)</sup> , 200 kSamples/s, 9.6 kHz input tone                                                                                                                                         |       | −65                               | dB           |
|                     |                                                    | $V_{DD5}$ as reference, 200 kSamples/s, 9.6 kHz input tone                                                                                                                                                                      |       | −70                               |              |
|                     |                                                    | Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone                                                                                                                             |       | −72                               |              |
| SINAD, SNDR         | Signal-to-noise and distortion ratio               | Internal 4.3 V equivalent reference <sup>(2)</sup> , 200 kSamples/s, 9.6 kHz input tone                                                                                                                                         |       | 60                                | dB           |
|                     |                                                    | $V_{DD5}$ as reference, 200 kSamples/s, 9.6 kHz input tone                                                                                                                                                                      |       | 63                                |              |
|                     |                                                    | Internal reference, voltage scaling disabled, 32 samples average (software), 200 kSamples/s, 300 Hz input tone                                                                                                                  |       | 68                                |              |
| SFDR                | Spurious-free dynamic range                        | Internal 4.3 V equivalent reference <sup>(2)</sup> , 200 kSamples/s, 9.6 kHz input tone                                                                                                                                         |       | 70                                | dB           |
|                     |                                                    | $V_{DD5}$ as reference, 200 kSamples/s, 9.6 kHz input tone                                                                                                                                                                      |       | 73                                |              |
|                     |                                                    | Internal reference, voltage scaling disabled, 32 samples average (software), 200 kSamples/s, 300 Hz input tone                                                                                                                  |       | 75                                |              |
|                     | Conversion time                                    | Serial conversion, time-to-output, 24 MHz clock                                                                                                                                                                                 |       | 50                                | Clock Cycles |
|                     | Current consumption                                | Internal 4.3 V equivalent reference <sup>(2)</sup>                                                                                                                                                                              |       | 0.39                              | mA           |
|                     | Current consumption                                | $V_{DD5}$ as reference                                                                                                                                                                                                          |       | 0.56                              | mA           |
|                     | Reference voltage                                  | Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1 |       | 4.3 <sup>(2)</sup> <sup>(3)</sup> | V            |

### 7.18.1.1 Analog-to-Digital Converter (ADC) Characteristics (continued)

$T_c = 25^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$  and voltage scaling enabled, unless otherwise noted.<sup>(1)</sup>

Performance numbers require use of offset and gain adjustments in software by TI-provided ADC drivers.

| PARAMETER         | TEST CONDITIONS                                                                                                                                                                                                                                                                                                                       | MIN | TYP                        | MAX | UNIT |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|----------------------------|-----|------|
| Reference voltage | Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows:<br>$V_{ref} = 4.3\text{ V} \times 1408 / 4095$ |     | 1.48                       |     | V    |
| Reference voltage | VDDS as reference, input voltage scaling enabled                                                                                                                                                                                                                                                                                      |     | VDDS                       |     | V    |
| Reference voltage | VDDS as reference, input voltage scaling disabled                                                                                                                                                                                                                                                                                     |     | VDDS / 2.82 <sup>(3)</sup> |     | V    |
| Input impedance   | 200 kSamples/s, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time                                                                                                                                                                                                            |     | >1                         |     | MΩ   |

- (1) Using IEEE Std 1241-2010 for terminology and test methods
- (2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V
- (3) Applied voltage must be within Absolute Maximum Ratings at all times
- (4) No missing codes
- (5)  $\text{ADC\_output} = \Sigma(4^n \text{ samples}) \gg n$ ,  $n$  = desired extra bits

### 7.18.2 DAC

#### 7.18.2.1 Digital-to-Analog Converter (DAC) Characteristics

$T_c = 25^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ , unless otherwise noted.

| PARAMETER                                                                 |                                                                       | TEST CONDITIONS                                                                                                                          | MIN  | TYP | MAX  | UNIT                 |
|---------------------------------------------------------------------------|-----------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|------|-----|------|----------------------|
| General Parameters                                                        |                                                                       |                                                                                                                                          |      |     |      |                      |
|                                                                           | Resolution                                                            |                                                                                                                                          | 8    |     |      | Bits                 |
| V <sub>DDS</sub>                                                          | Supply voltage                                                        | Any load, any V <sub>REF</sub> , pre-charge OFF, DAC charge-pump ON                                                                      | 1.8  |     | 3.8  | V                    |
|                                                                           |                                                                       | External Load <sup>(4)</sup> , any V <sub>REF</sub> , pre-charge OFF, DAC charge-pump OFF                                                | 2.0  |     | 3.8  |                      |
|                                                                           |                                                                       | Any load, V <sub>REF</sub> = DCOUPL, pre-charge ON                                                                                       | 2.6  |     | 3.8  |                      |
| F <sub>DAC</sub>                                                          | Clock frequency                                                       | Buffer ON (recommended for external load)                                                                                                | 16   |     | 250  | kHz                  |
|                                                                           |                                                                       | Buffer OFF (internal load)                                                                                                               | 16   |     | 1000 |                      |
|                                                                           | Voltage output settling time                                          | V <sub>REF</sub> = V <sub>DDS</sub> , buffer OFF, internal load                                                                          | 13   |     |      | 1 / F <sub>DAC</sub> |
|                                                                           |                                                                       | V <sub>REF</sub> = V <sub>DDS</sub> , buffer ON, external capacitive load = 20 pF <sup>(3)</sup>                                         | 13.8 |     |      |                      |
|                                                                           | External capacitive load                                              |                                                                                                                                          | 20   |     | 200  | pF                   |
|                                                                           | External resistive load                                               |                                                                                                                                          | 10   |     |      | MΩ                   |
|                                                                           | Short circuit current                                                 |                                                                                                                                          |      |     | 400  | μA                   |
| Z <sub>MAX</sub>                                                          | Max output impedance Vref = V <sub>DDS</sub> , buffer ON, CLK 250 kHz | V <sub>DDS</sub> = 3.8 V, DAC charge-pump OFF                                                                                            | 50.8 |     |      | kΩ                   |
|                                                                           |                                                                       | V <sub>DDS</sub> = 3.0 V, DAC charge-pump ON                                                                                             | 51.7 |     |      |                      |
|                                                                           |                                                                       | V <sub>DDS</sub> = 3.0 V, DAC charge-pump OFF                                                                                            | 53.2 |     |      |                      |
|                                                                           |                                                                       | V <sub>DDS</sub> = 2.0 V, DAC charge-pump ON                                                                                             | 48.7 |     |      |                      |
|                                                                           |                                                                       | V <sub>DDS</sub> = 2.0 V, DAC charge-pump OFF                                                                                            | 70.2 |     |      |                      |
|                                                                           |                                                                       | V <sub>DDS</sub> = 1.8 V, DAC charge-pump ON                                                                                             | 46.3 |     |      |                      |
|                                                                           |                                                                       | V <sub>DDS</sub> = 1.8 V, DAC charge-pump OFF                                                                                            | 88.9 |     |      |                      |
| Internal Load - Continuous Time Comparator / Low Power Clocked Comparator |                                                                       |                                                                                                                                          |      |     |      |                      |
| DNL                                                                       | Differential nonlinearity                                             | V <sub>REF</sub> = V <sub>DDS</sub> ,<br>load = Continuous Time Comparator or Low Power Clocked Comparator<br>F <sub>DAC</sub> = 250 kHz | ±1   |     |      | LSB <sup>(1)</sup>   |
|                                                                           | Differential nonlinearity                                             | V <sub>REF</sub> = V <sub>DDS</sub> ,<br>load = Continuous Time Comparator or Low Power Clocked Comparator<br>F <sub>DAC</sub> = 16 kHz  | ±1.2 |     |      |                      |

### 7.18.2.1 Digital-to-Analog Converter (DAC) Characteristics (continued)

$T_c = 25^\circ\text{C}$ ,  $V_{DDS} = 3.0\text{ V}$ , unless otherwise noted.

| PARAMETER                                                                               | TEST CONDITIONS                                                   | MIN | TYP   | MAX | UNIT               |
|-----------------------------------------------------------------------------------------|-------------------------------------------------------------------|-----|-------|-----|--------------------|
| Offset error <sup>(2)</sup><br>Load = Continuous Time Comparator                        | $V_{REF} = V_{DDS} = 3.8\text{ V}$                                |     | ±0.64 |     | LSB <sup>(1)</sup> |
|                                                                                         | $V_{REF} = V_{DDS} = 3.0\text{ V}$                                |     | ±0.81 |     |                    |
|                                                                                         | $V_{REF} = V_{DDS} = 1.8\text{ V}$                                |     | ±1.27 |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge ON}$                    |     | ±3.43 |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge OFF}$                   |     | ±2.88 |     |                    |
|                                                                                         | $V_{REF} = \text{ADCREf}$                                         |     | ±2.37 |     |                    |
| Offset error <sup>(2)</sup><br>Load = Low Power Clocked Comparator                      | $V_{REF} = V_{DDS} = 3.8\text{ V}$                                |     | ±0.78 |     | LSB <sup>(1)</sup> |
|                                                                                         | $V_{REF} = V_{DDS} = 3.0\text{ V}$                                |     | ±0.77 |     |                    |
|                                                                                         | $V_{REF} = V_{DDS} = 1.8\text{ V}$                                |     | ±3.46 |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge ON}$                    |     | ±3.44 |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge OFF}$                   |     | ±4.70 |     |                    |
|                                                                                         | $V_{REF} = \text{ADCREf}$                                         |     | ±4.11 |     |                    |
| Max code output voltage variation <sup>(2)</sup><br>Load = Continuous Time Comparator   | $V_{REF} = V_{DDS} = 3.8\text{ V}$                                |     | ±1.53 |     | LSB <sup>(1)</sup> |
|                                                                                         | $V_{REF} = V_{DDS} = 3.0\text{ V}$                                |     | ±1.71 |     |                    |
|                                                                                         | $V_{REF} = V_{DDS} = 1.8\text{ V}$                                |     | ±2.10 |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge ON}$                    |     | ±6.00 |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge OFF}$                   |     | ±3.85 |     |                    |
|                                                                                         | $V_{REF} = \text{ADCREf}$                                         |     | ±5.84 |     |                    |
| Max code output voltage variation <sup>(2)</sup><br>Load = Low Power Clocked Comparator | $V_{REF} = V_{DDS} = 3.8\text{ V}$                                |     | ±2.92 |     | LSB <sup>(1)</sup> |
|                                                                                         | $V_{REF} = V_{DDS} = 3.0\text{ V}$                                |     | ±3.06 |     |                    |
|                                                                                         | $V_{REF} = V_{DDS} = 1.8\text{ V}$                                |     | ±3.91 |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge ON}$                    |     | ±7.84 |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge OFF}$                   |     | ±4.06 |     |                    |
|                                                                                         | $V_{REF} = \text{ADCREf}$                                         |     | ±6.94 |     |                    |
| Output voltage range <sup>(2)</sup><br>Load = Continuous Time Comparator                | $V_{REF} = V_{DDS} = 3.8\text{ V}, \text{code } 1$                |     | 0.03  |     | V                  |
|                                                                                         | $V_{REF} = V_{DDS} = 3.8\text{ V}, \text{code } 255$              |     | 3.62  |     |                    |
|                                                                                         | $V_{REF} = V_{DDS} = 3.0\text{ V}, \text{code } 1$                |     | 0.02  |     |                    |
|                                                                                         | $V_{REF} = V_{DDS} = 3.0\text{ V}, \text{code } 255$              |     | 2.86  |     |                    |
|                                                                                         | $V_{REF} = V_{DDS} = 1.8\text{ V}, \text{code } 1$                |     | 0.01  |     |                    |
|                                                                                         | $V_{REF} = V_{DDS} = 1.8\text{ V}, \text{code } 255$              |     | 1.71  |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge OFF}, \text{code } 1$   |     | 0.01  |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge OFF}, \text{code } 255$ |     | 1.21  |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge ON}, \text{code } 1$    |     | 1.27  |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge ON}, \text{code } 255$  |     | 2.46  |     |                    |
|                                                                                         | $V_{REF} = \text{ADCREf}, \text{code } 1$                         |     | 0.01  |     |                    |
|                                                                                         | $V_{REF} = \text{ADCREf}, \text{code } 255$                       |     | 1.41  |     |                    |
| Output voltage range <sup>(2)</sup><br>Load = Low Power Clocked Comparator              | $V_{REF} = V_{DDS} = 3.8\text{ V}, \text{code } 1$                |     | 0.03  |     | V                  |
|                                                                                         | $V_{REF} = V_{DDS} = 3.8\text{ V}, \text{code } 255$              |     | 3.61  |     |                    |
|                                                                                         | $V_{REF} = V_{DDS} = 3.0\text{ V}, \text{code } 1$                |     | 0.02  |     |                    |
|                                                                                         | $V_{REF} = V_{DDS} = 3.0\text{ V}, \text{code } 255$              |     | 2.85  |     |                    |
|                                                                                         | $V_{REF} = V_{DDS} = 1.8\text{ V}, \text{code } 1$                |     | 0.01  |     |                    |
|                                                                                         | $V_{REF} = V_{DDS} = 1.8\text{ V}, \text{code } 255$              |     | 1.71  |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge OFF}, \text{code } 1$   |     | 0.01  |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge OFF}, \text{code } 255$ |     | 1.21  |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge ON}, \text{code } 1$    |     | 1.27  |     |                    |
|                                                                                         | $V_{REF} = \text{DCOUP}, \text{pre-charge ON}, \text{code } 255$  |     | 2.46  |     |                    |
|                                                                                         | $V_{REF} = \text{ADCREf}, \text{code } 1$                         |     | 0.01  |     |                    |
|                                                                                         | $V_{REF} = \text{ADCREf}, \text{code } 255$                       |     | 1.41  |     |                    |

### 7.18.2.1 Digital-to-Analog Converter (DAC) Characteristics (continued)

$T_c = 25^\circ\text{C}$ ,  $V_{DD5} = 3.0\text{ V}$ , unless otherwise noted.

| PARAMETER                                  |                                                                | TEST CONDITIONS                                  | MIN | TYP        | MAX | UNIT               |
|--------------------------------------------|----------------------------------------------------------------|--------------------------------------------------|-----|------------|-----|--------------------|
| External Load (Keysight 34401A Multimeter) |                                                                |                                                  |     |            |     |                    |
| INL                                        | Integral nonlinearity                                          | $V_{REF} = V_{DD5}$ , $F_{DAC} = 250\text{ kHz}$ |     | $\pm 1$    |     | LSB <sup>(1)</sup> |
|                                            |                                                                | $V_{REF} = DCOUPL$ , $F_{DAC} = 250\text{ kHz}$  |     | $\pm 1$    |     |                    |
|                                            |                                                                | $V_{REF} = ADCREF$ , $F_{DAC} = 250\text{ kHz}$  |     | $\pm 1$    |     |                    |
| DNL                                        | Differential nonlinearity                                      | $V_{REF} = V_{DD5}$ , $F_{DAC} = 250\text{ kHz}$ |     | $\pm 1$    |     | LSB <sup>(1)</sup> |
|                                            | Offset error                                                   | $V_{REF} = V_{DD5} = 3.8\text{ V}$               |     | $\pm 0.20$ |     | LSB <sup>(1)</sup> |
|                                            |                                                                | $V_{REF} = V_{DD5} = 3.0\text{ V}$               |     | $\pm 0.25$ |     |                    |
|                                            |                                                                | $V_{REF} = V_{DD5} = 1.8\text{ V}$               |     | $\pm 0.45$ |     |                    |
|                                            |                                                                | $V_{REF} = DCOUPL$ , pre-charge ON               |     | $\pm 1.55$ |     |                    |
|                                            |                                                                | $V_{REF} = DCOUPL$ , pre-charge OFF              |     | $\pm 1.30$ |     |                    |
|                                            |                                                                | $V_{REF} = ADCREF$                               |     | $\pm 1.10$ |     |                    |
|                                            | Max code output voltage variation                              | $V_{REF} = V_{DD5} = 3.8\text{ V}$               |     | $\pm 0.60$ |     | LSB <sup>(1)</sup> |
|                                            |                                                                | $V_{REF} = V_{DD5} = 3.0\text{ V}$               |     | $\pm 0.55$ |     |                    |
|                                            |                                                                | $V_{REF} = V_{DD5} = 1.8\text{ V}$               |     | $\pm 0.60$ |     |                    |
|                                            |                                                                | $V_{REF} = DCOUPL$ , pre-charge ON               |     | $\pm 3.45$ |     |                    |
|                                            |                                                                | $V_{REF} = DCOUPL$ , pre-charge OFF              |     | $\pm 2.10$ |     |                    |
|                                            |                                                                | $V_{REF} = ADCREF$                               |     | $\pm 1.90$ |     |                    |
|                                            | Output voltage range<br>Load = Low Power Clocked<br>Comparator | $V_{REF} = V_{DD5} = 3.8\text{ V}$ , code 1      |     | 0.03       |     | V                  |
|                                            |                                                                | $V_{REF} = V_{DD5} = 3.8\text{ V}$ , code 255    |     | 3.61       |     |                    |
|                                            |                                                                | $V_{REF} = V_{DD5} = 3.0\text{ V}$ , code 1      |     | 0.02       |     |                    |
|                                            |                                                                | $V_{REF} = V_{DD5} = 3.0\text{ V}$ , code 255    |     | 2.85       |     |                    |
|                                            |                                                                | $V_{REF} = V_{DD5} = 1.8\text{ V}$ , code 1      |     | 0.02       |     |                    |
|                                            |                                                                | $V_{REF} = V_{DD5} = 1.8\text{ V}$ , code 255    |     | 1.71       |     |                    |
|                                            |                                                                | $V_{REF} = DCOUPL$ , pre-charge OFF, code 1      |     | 0.02       |     |                    |
|                                            |                                                                | $V_{REF} = DCOUPL$ , pre-charge OFF, code 255    |     | 1.20       |     |                    |
|                                            |                                                                | $V_{REF} = DCOUPL$ , pre-charge ON, code 1       |     | 1.27       |     |                    |
|                                            |                                                                | $V_{REF} = DCOUPL$ , pre-charge ON, code 255     |     | 2.46       |     |                    |
|                                            |                                                                | $V_{REF} = ADCREF$ , code 1                      |     | 0.02       |     |                    |
|                                            |                                                                | $V_{REF} = ADCREF$ , code 255                    |     | 1.42       |     |                    |

(1) 1 LSB ( $V_{REF} = 3.8\text{ V}/3.0\text{ V}/1.8\text{ V}/DCOUP/ADCREF$ ) = 14.10 mV/11.13 mV/6.68 mV/4.67 mV/5.48 mV

(2) Includes comparator offset

(3) A load > 20 pF will increase the settling time

(4) Keysight 34401A Multimeter

### 7.18.3 Temperature and Battery Monitor

#### 7.18.3.1 Temperature Sensor

Measured on a Texas Instruments reference design with  $T_c = 25\text{ }^{\circ}\text{C}$ ,  $V_{\text{DD}} = 3.0\text{ V}$ , unless otherwise noted.

| PARAMETER                                 | TEST CONDITIONS                                              | MIN | TYP       | MAX | UNIT                        |
|-------------------------------------------|--------------------------------------------------------------|-----|-----------|-----|-----------------------------|
| Resolution                                |                                                              |     | 2         |     | $^{\circ}\text{C}$          |
| Accuracy                                  | $-40\text{ }^{\circ}\text{C}$ to $0\text{ }^{\circ}\text{C}$ |     | $\pm 4.0$ |     | $^{\circ}\text{C}$          |
| Accuracy                                  | $0\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$ |     | $\pm 2.5$ |     | $^{\circ}\text{C}$          |
| Supply voltage coefficient <sup>(1)</sup> |                                                              |     | 3.9       |     | $^{\circ}\text{C}/\text{V}$ |

(1) The temperature sensor is automatically compensated for  $V_{\text{DD}}$  variation when using the TI-provided driver.

#### 7.18.3.2 Battery Monitor

Measured on a Texas Instruments reference design with  $T_c = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted.

| PARAMETER                   | TEST CONDITIONS                | MIN | TYP  | MAX | UNIT |
|-----------------------------|--------------------------------|-----|------|-----|------|
| Resolution                  |                                |     | 25   |     | mV   |
| Range                       |                                | 1.8 |      | 3.8 | V    |
| Integral nonlinearity (max) |                                |     | 23   |     | mV   |
| Accuracy                    | $V_{\text{DD}} = 3.0\text{ V}$ |     | 22.5 |     | mV   |
| Offset error                |                                |     | -32  |     | mV   |
| Gain error                  |                                |     | -1   |     | %    |

### 7.18.4 Comparator

#### 7.18.4.1 Continuous Time Comparator

$T_c = 25\text{ }^{\circ}\text{C}$ ,  $V_{\text{DD}} = 3.0\text{ V}$ , unless otherwise noted.

| PARAMETER                          | TEST CONDITIONS                             | MIN | TYP     | MAX             | UNIT          |
|------------------------------------|---------------------------------------------|-----|---------|-----------------|---------------|
| Input voltage range <sup>(1)</sup> |                                             | 0   |         | $V_{\text{DD}}$ | V             |
| Offset                             | Measured at $V_{\text{DD}} / 2$             |     | $\pm 5$ |                 | mV            |
| Decision time                      | Step from $-10\text{ mV}$ to $10\text{ mV}$ |     | 0.78    |                 | $\mu\text{s}$ |
| Current consumption                | Internal reference                          |     | 9.2     |                 | $\mu\text{A}$ |

(1) The input voltages can be generated externally and connected throughout I/Os or an internal reference voltage can be generated using the DAC

## 7.18.5 GPIO

### 7.18.5.1 GPIO DC Characteristics

| PARAMETER                                             | TEST CONDITIONS                                                 | MIN                  | TYP                  | MAX | UNIT |
|-------------------------------------------------------|-----------------------------------------------------------------|----------------------|----------------------|-----|------|
| <b>T<sub>A</sub> = 25 °C, V<sub>DDs</sub> = 1.8 V</b> |                                                                 |                      |                      |     |      |
| GPIO VOH at 8 mA load                                 | IOCURR = 2, high-drive GPIOs only                               |                      | 1.56                 |     | V    |
| GPIO VOL at 8 mA load                                 | IOCURR = 2, high-drive GPIOs only                               |                      | 0.24                 |     | V    |
| GPIO VOH at 4 mA load                                 | IOCURR = 1                                                      |                      | 1.59                 |     | V    |
| GPIO VOL at 4 mA load                                 | IOCURR = 1                                                      |                      | 0.21                 |     | V    |
| GPIO pullup current                                   | Input mode, pullup enabled, Vpad = 0 V                          |                      | 73                   |     | μA   |
| GPIO pulldown current                                 | Input mode, pulldown enabled, Vpad = VDDs                       |                      | 19                   |     | μA   |
| GPIO low-to-high input transition, with hysteresis    | IH = 1, transition voltage for input read as 0 → 1              |                      | 1.08                 |     | V    |
| GPIO high-to-low input transition, with hysteresis    | IH = 1, transition voltage for input read as 1 → 0              |                      | 0.73                 |     | V    |
| GPIO input hysteresis                                 | IH = 1, difference between 0 → 1 and 1 → 0 points               |                      | 0.35                 |     | V    |
| <b>T<sub>A</sub> = 25 °C, V<sub>DDs</sub> = 3.0 V</b> |                                                                 |                      |                      |     |      |
| GPIO VOH at 8 mA load                                 | IOCURR = 2, high-drive GPIOs only                               |                      | 2.59                 |     | V    |
| GPIO VOL at 8 mA load                                 | IOCURR = 2, high-drive GPIOs only                               |                      | 0.42                 |     | V    |
| GPIO VOH at 4 mA load                                 | IOCURR = 1                                                      |                      | 2.63                 |     | V    |
| GPIO VOL at 4 mA load                                 | IOCURR = 1                                                      |                      | 0.40                 |     | V    |
| <b>T<sub>A</sub> = 25 °C, V<sub>DDs</sub> = 3.8 V</b> |                                                                 |                      |                      |     |      |
| GPIO pullup current                                   | Input mode, pullup enabled, Vpad = 0 V                          |                      | 282                  |     | μA   |
| GPIO pulldown current                                 | Input mode, pulldown enabled, Vpad = VDDs                       |                      | 110                  |     | μA   |
| GPIO low-to-high input transition, with hysteresis    | IH = 1, transition voltage for input read as 0 → 1              |                      | 1.97                 |     | V    |
| GPIO high-to-low input transition, with hysteresis    | IH = 1, transition voltage for input read as 1 → 0              |                      | 1.55                 |     | V    |
| GPIO input hysteresis                                 | IH = 1, difference between 0 → 1 and 1 → 0 points               |                      | 0.42                 |     | V    |
| <b>T<sub>A</sub> = 25 °C</b>                          |                                                                 |                      |                      |     |      |
| VIH                                                   | Lowest GPIO input voltage reliably interpreted as a <i>High</i> | 0.8*V <sub>DDs</sub> |                      |     | V    |
| VIL                                                   | Highest GPIO input voltage reliably interpreted as a <i>Low</i> |                      | 0.2*V <sub>DDs</sub> |     | V    |

## 7.19 Typical Characteristics

All measurements in this section are done with  $T_c = 25^\circ\text{C}$  and  $V_{\text{DD}} = 3.0\text{V}$ , unless otherwise noted. See *Recommended Operating Conditions*, [Section 7.3](#), for device limits. Values exceeding these limits are for reference only.

### 7.19.1 MCU Current

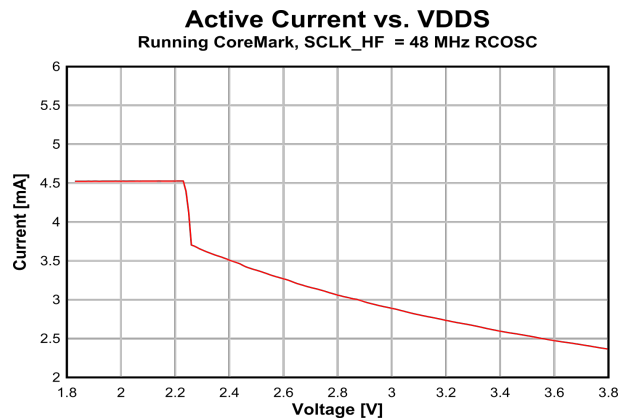


**Figure 7-4. Active Mode (MCU) Current vs Supply Voltage (VDD)**

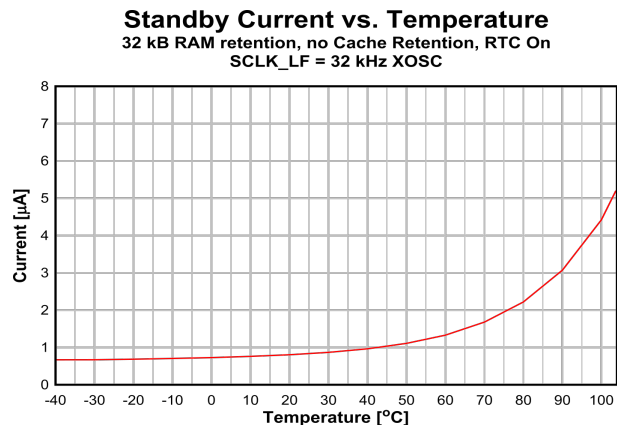


**Figure 7-5. Standby Mode (MCU) Current vs Temperature**

### 7.19.2 RX Current

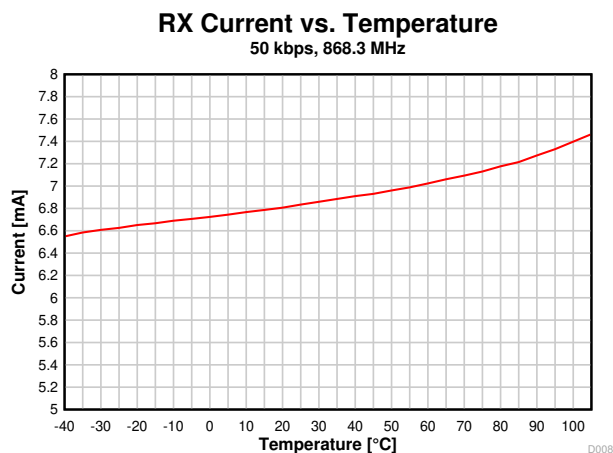


**Figure 7-6. RX Current vs Temperature (50kbps, 868.3MHz)**

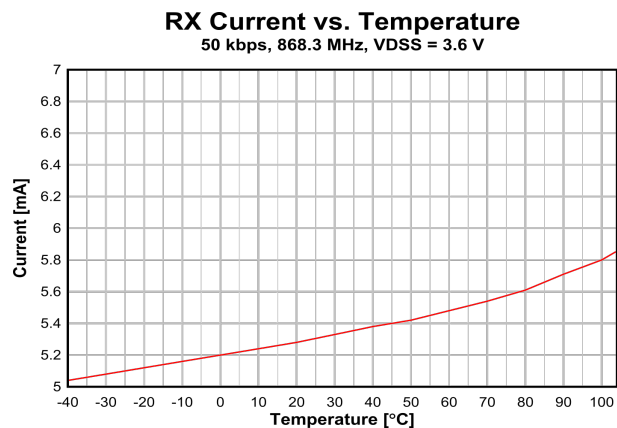


**Figure 7-7. RX Current vs Temperature (50kbps, 868.3MHz, VDD = 3.6)**

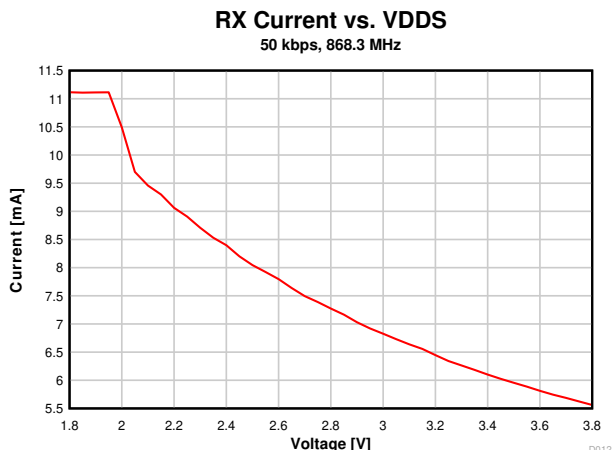


Figure 7-8. RX Current vs Supply Voltage (VDD5) (50kbps, 868.3MHz)

### 7.19.3 TX Current

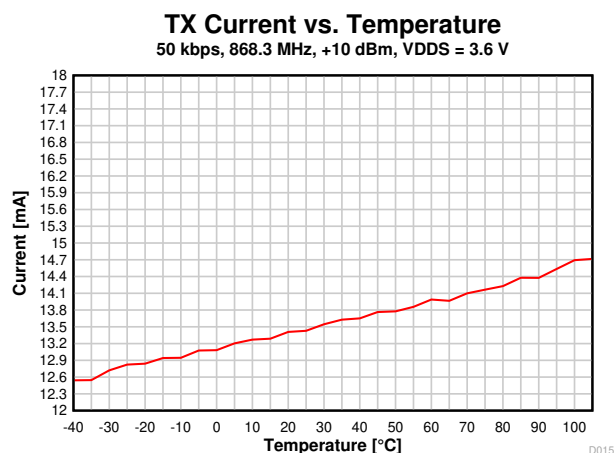


Figure 7-9. TX Current vs Temperature (50kbps, 868.3MHz, VDD5 = 3.6V)

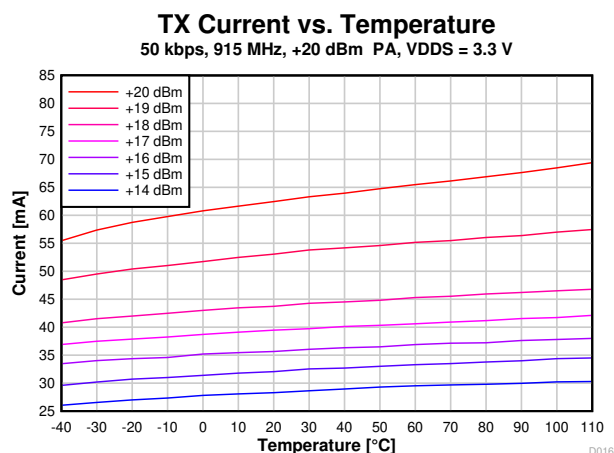


Figure 7-10. TX Current vs Temperature (50kbps, 915MHz, VDD5 = 3.3V)

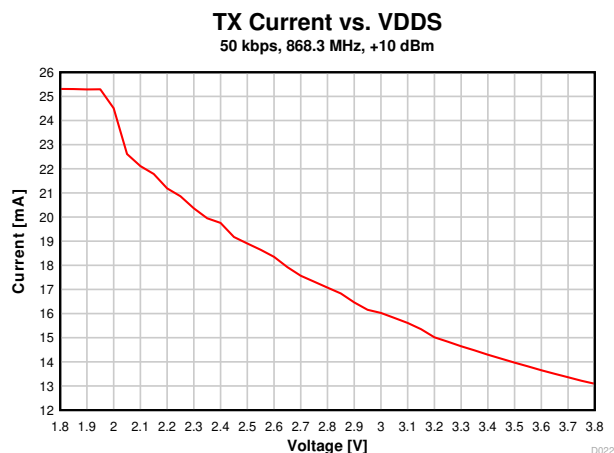


Figure 7-11. TX Current vs Supply Voltage (VDD5) (50 kbps, 868.3MHz)

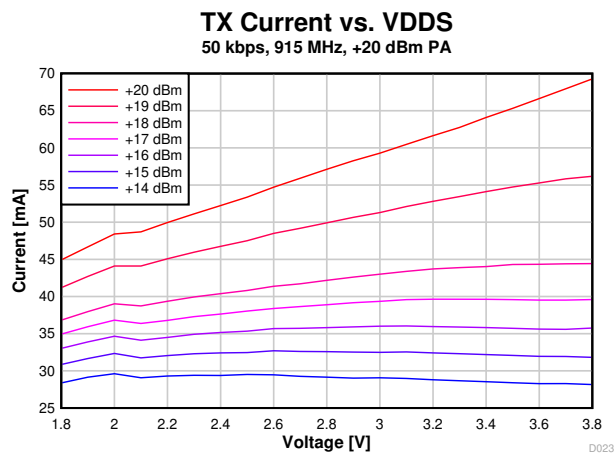


Figure 7-12. TX Current vs Supply Voltage (VDD5) (50 kbps, 915MHz)

Table 7-2 shows typical TX current and output power for different output power settings.

**Table 7-1. Typical TX Current and Output Power, high power PA (915MHz, VDDS = 3.3V)**

| CC1311P3 at 915MHz, VDDS = 3.3V (Measured on CC1311-P3EM-7XD7793-PA915) |                                   |                            |                                  |
|-------------------------------------------------------------------------|-----------------------------------|----------------------------|----------------------------------|
| txPower                                                                 | TX Power Setting (SmartRF Studio) | Typical Output Power [dBm] | Typical Current Consumption [mA] |
| 0x1B8ED2                                                                | 20                                | 20.6                       | 64.9                             |
| 0x448CF                                                                 | 19                                | 19.5                       | 55.4                             |
| 0x48022                                                                 | 18                                | 18.0                       | 46.0                             |
| 0x2661C                                                                 | 17                                | 17.1                       | 41.5                             |
| 0x5618                                                                  | 16                                | 16.2                       | 37.6                             |
| 0x4812                                                                  | 15                                | 15.2                       | 33.9                             |
| 0x380D                                                                  | 14                                | 14.0                       | 30.2                             |

**Table 7-2. Typical TX Current and Output Power (868MHz, VDDS = 3.0V)**

| CC1311P3 at 868MHz, VDDS = 3.0V (Measured on CC1311-P3EM-7XD7793-PA915) |                                   |                            |                                  |
|-------------------------------------------------------------------------|-----------------------------------|----------------------------|----------------------------------|
| txPower                                                                 | TX Power Setting (SmartRF Studio) | Typical Output Power [dBm] | Typical Current Consumption [mA] |
| 0x013F <sup>1</sup>                                                     | 14                                | 13.8                       | 30.0                             |
| 0xB224                                                                  | 12.5                              | 12.2                       | 21.5                             |
| 0x895E                                                                  | 12                                | 11.8                       | 20.3                             |
| 0x669A                                                                  | 11                                | 10.8                       | 18.1                             |
| 0x3E92                                                                  | 10                                | 9.8                        | 16.4                             |
| 0x3EDC                                                                  | 9                                 | 8.9                        | 15.5                             |
| 0x2CD8                                                                  | 8                                 | 8.1                        | 14.5                             |
| 0x26D4                                                                  | 7                                 | 7.0                        | 13.3                             |
| 0x20D1                                                                  | 6                                 | 5.8                        | 12.2                             |
| 0x1CCE                                                                  | 5                                 | 4.4                        | 10.9                             |
| 0x16CD                                                                  | 4                                 | 3.7                        | 10.5                             |
| 0x14CB                                                                  | 3                                 | 2.2                        | 9.7                              |
| 0x12CA                                                                  | 2                                 | 1.5                        | 9.2                              |
| 0x12C9                                                                  | 1                                 | 0.6                        | 8.8                              |
| 0x10C8                                                                  | 0                                 | -0.5                       | 8.3                              |
| 0xAC4                                                                   | -5                                | -7.3                       | 6.5                              |
| 0xAC2                                                                   | -10                               | -13.1                      | 5.6                              |
| 0x6C1                                                                   | -15                               | -18.3                      | 5.2                              |
| 0x4C0                                                                   | -20                               | -22.6                      | 4.9                              |

<sup>1</sup> Boost mode enabled. VDDR regulated to 1.95V.

## 7.19.4 RX Performance

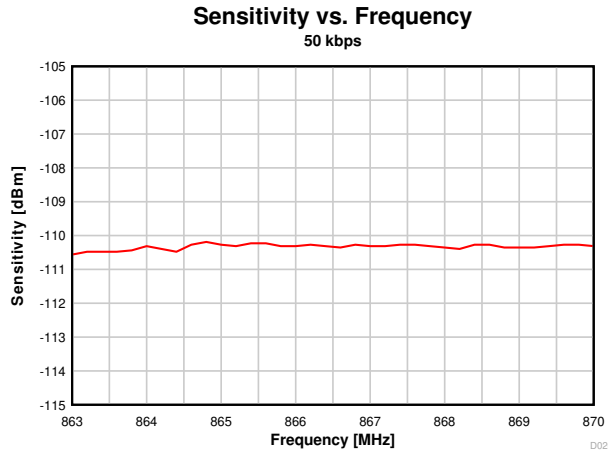


Figure 7-13. Sensitivity vs Frequency (50kbps, 868MHz)

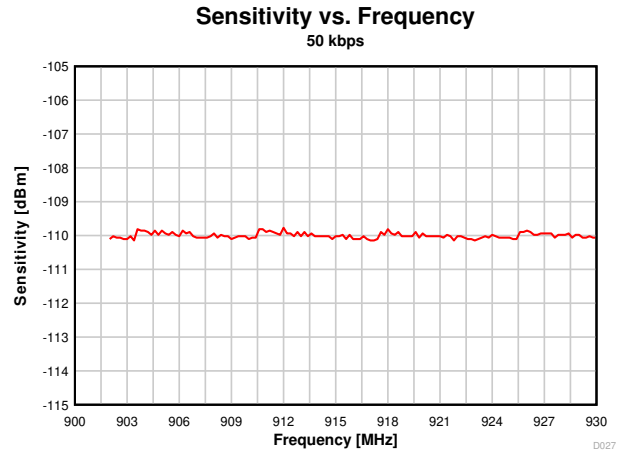


Figure 7-14. Sensitivity vs Frequency (50kbps, 915MHz)

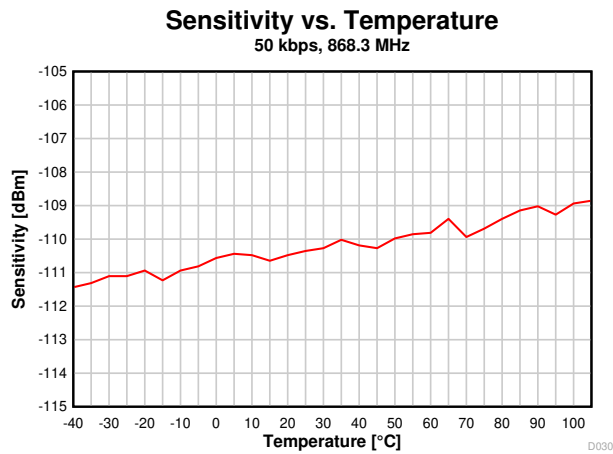


Figure 7-15. Sensitivity vs Temperature (50kbps, 868.3MHz)

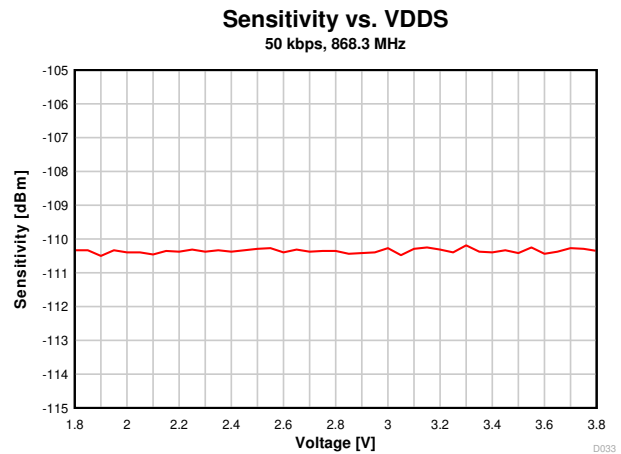


Figure 7-16. Sensitivity vs Supply Voltage (VDDS) (50kbps, 868.3MHz)

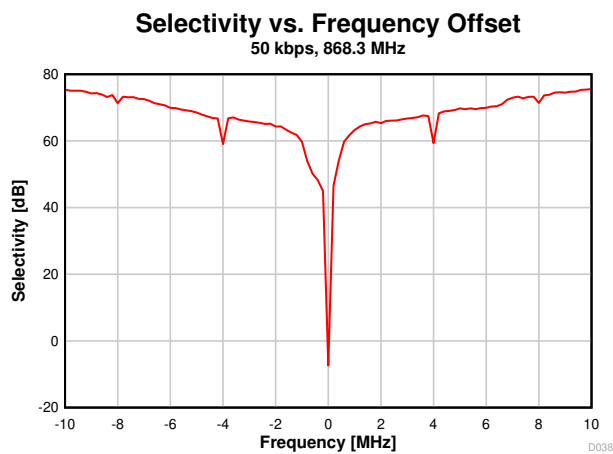


Figure 7-17. Selectivity vs Frequency Offset (50kbps, 868.3MHz)

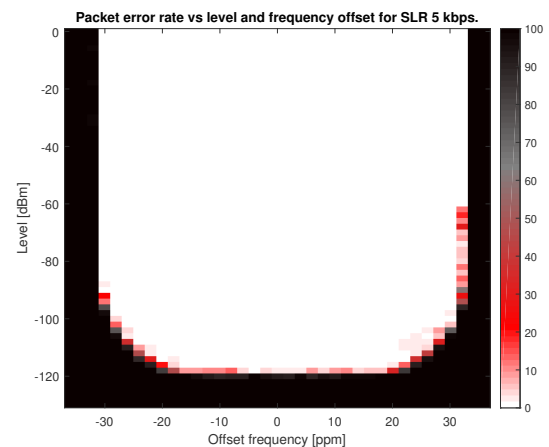


Figure 7-18. PER vs Level vs Frequency (SimpleLink™ Long Range 5kbps, 868MHz)

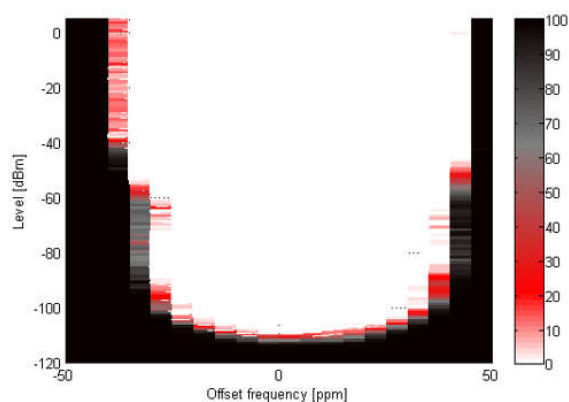


**Figure 7-19. 802.15.4, 50kbps,  $\pm 25$ kHz Deviation, 2-GFSK, 100kHz RX Bandwidth**

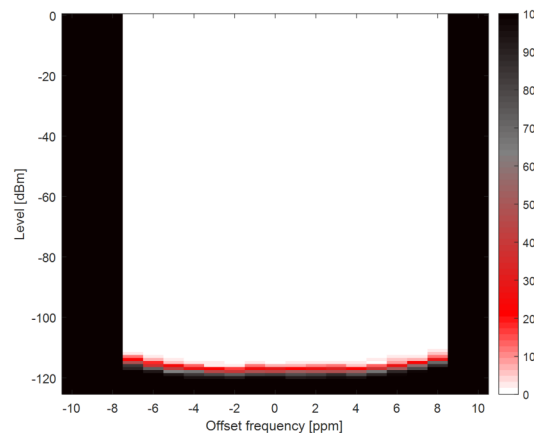


**Figure 7-20. Narrowband, 9.6kbps  $\pm 2.4$ kHz Deviation, 2-GFSK, 868MHz, 17.1kHz RX Bandwidth**

### 7.19.5 TX Performance

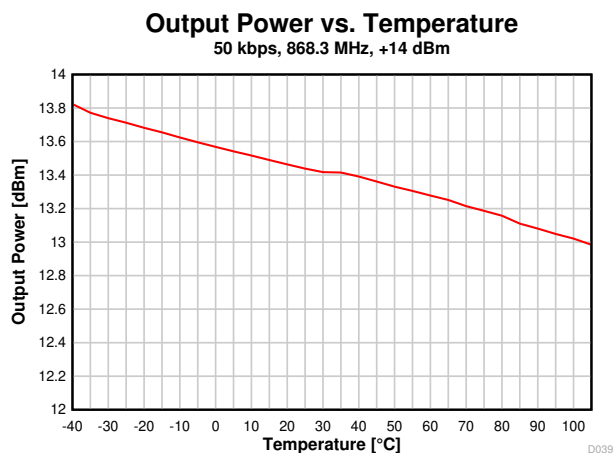


**Figure 7-21. Output Power vs Temperature (50kbps, 868.3MHz)**

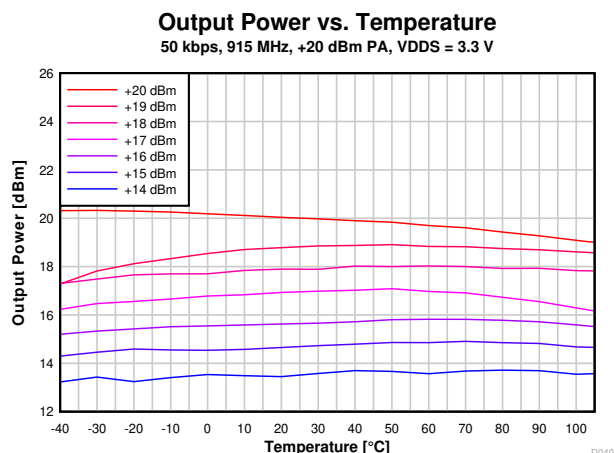


**Figure 7-22. Output Power vs Temperature (50kbps, 915MHz)**

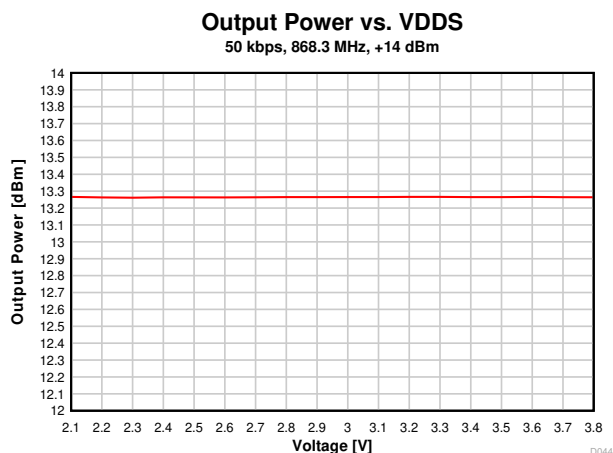


**Figure 7-23. Output Power vs Supply Voltage (VDD5) (50kbps, 868.3MHz)**

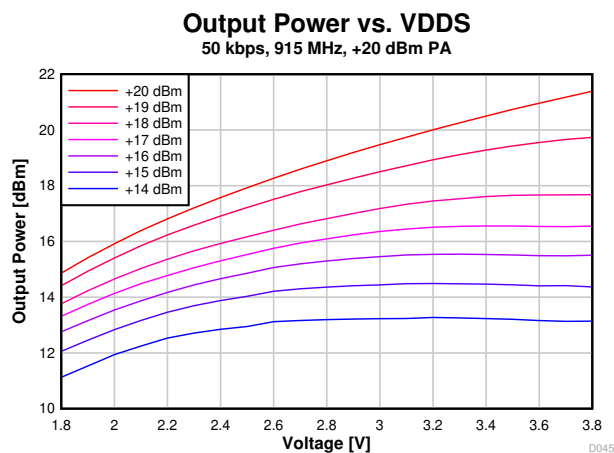


**Figure 7-24. Output Power vs Supply Voltage (VDD5) (50kbps, 915MHz)**

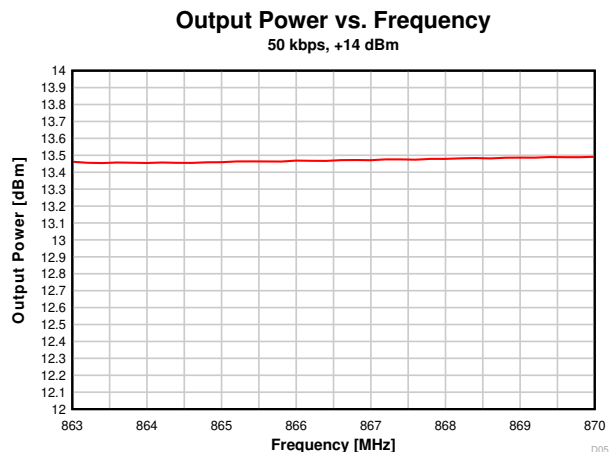


**Figure 7-25. Output Power vs Frequency (50kbps, 868MHz)**

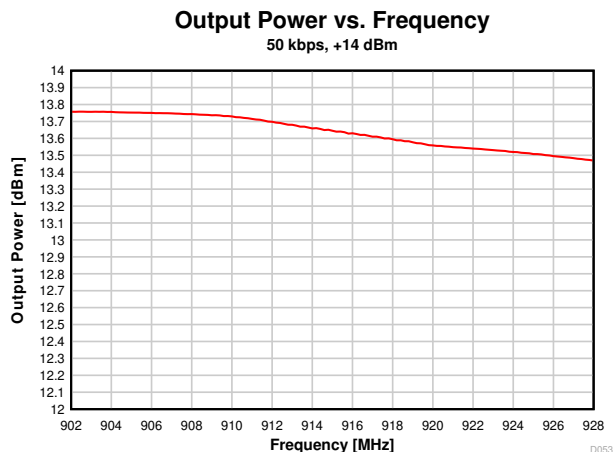


**Figure 7-26. Output Power vs Frequency (50kbps, 915MHz)**

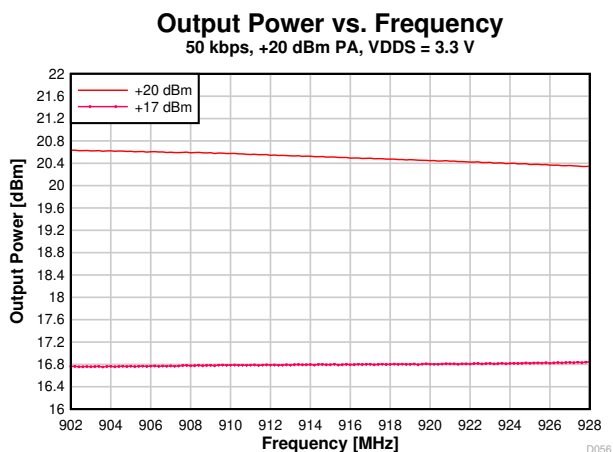


**Figure 7-27. Output Power vs Frequency (50kbps, 915MHz, VDDS = 3.3V)**

## 7.19.6 ADC Performance

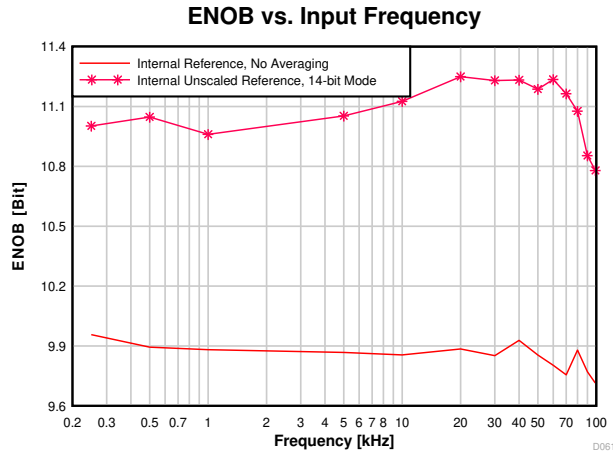


Figure 7-28. ENOB vs Input Frequency

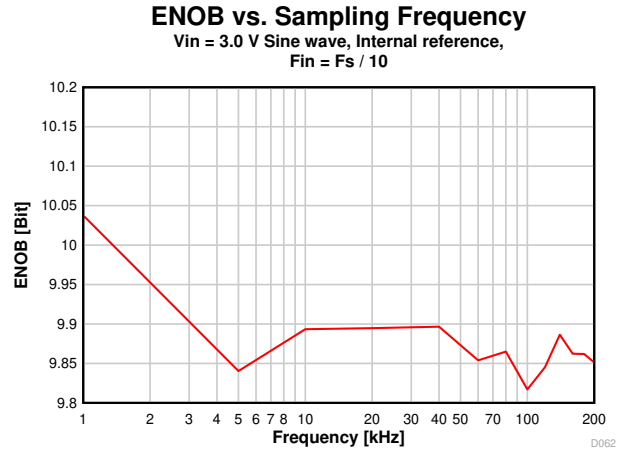


Figure 7-29. ENOB vs Sampling Frequency

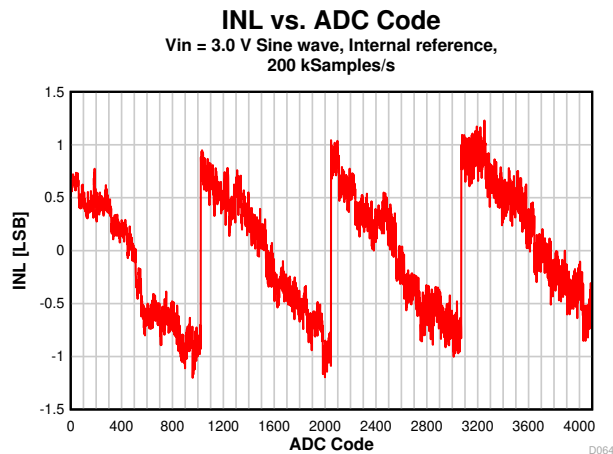


Figure 7-30. INL vs ADC Code

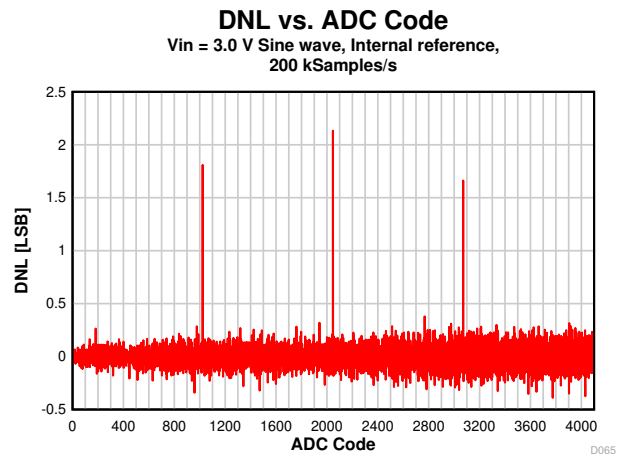


Figure 7-31. DNL vs ADC Code

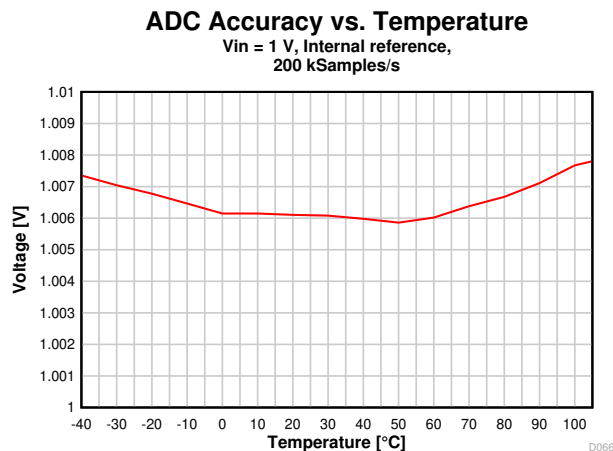


Figure 7-32. ADC Accuracy vs Temperature

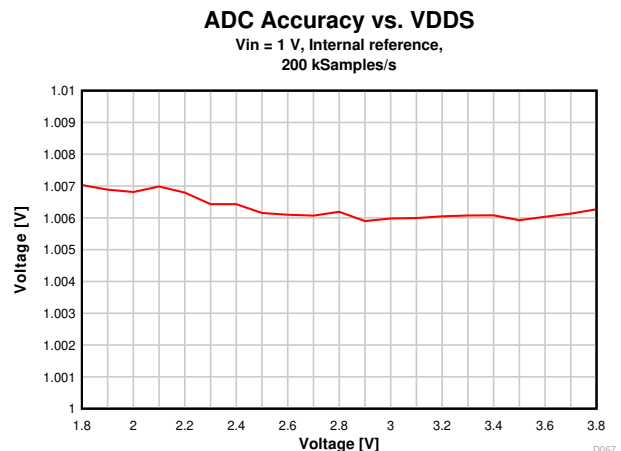


Figure 7-33. ADC Accuracy vs Supply Voltage (VDD)

## 8 Detailed Description

### 8.1 Overview

[Section 4](#) shows the core modules of the CC1311P3 device.

### 8.2 System CPU

The CC1311P3 SimpleLink™ Wireless MCU contains an Arm® Cortex®-M4 system CPU, which runs the application and the higher layers of radio protocol stacks.

The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Its features include the following:

- ARMv7-M architecture optimized for small-footprint embedded applications
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size
- Fast code execution permits increased sleep mode time
- Deterministic, high-performance interrupt handling for time-critical applications
- Single-cycle multiply instruction and hardware divide
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Full debug with data matching for watchpoint generation
  - Data Watchpoint and Trace Unit (DWT)
  - JTAG Debug Access Port (DAP)
  - Flash Patch and Breakpoint Unit (FPB)
- Trace support reduces the number of pins required for debugging and tracing
  - Instrumentation Trace Macrocell Unit (ITM)
  - Trace Port Interface Unit (TPIU) with asynchronous serial wire output (SWO)
- Optimized for single-cycle flash memory access
- Tightly connected to 8KB 4-way random replacement cache for minimal active power consumption and wait states
- Ultra-low-power consumption with integrated sleep modes
- 48MHz operation
- 1.25 DMIPS per MHz

### 8.3 Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

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#### Note

Not all combinations of features, frequencies, data rates, and modulation formats described in this chapter are supported. Over time, TI can enable new physical radio formats (PHYs) for the device and provides performance numbers for selected PHYs in the data sheet. Supported radio formats for a specific device, including optimized settings to use with the TI RF driver, are included in the [SmartRF Studio](#) tool with performance numbers of selected formats found in [Section 7](#).

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### 8.3.1 Proprietary Radio Formats

The CC1311P3 radio can support a wide range of physical radio formats through a set of hardware peripherals combined with firmware available in the device ROM, covering various customer needs for optimizing towards parameters such as speed or sensitivity. This allows great flexibility in tuning the radio both to work with legacy protocols as well as customizing the behavior for specific application needs.

Table 8-1 gives a simplified overview of features of the various radio formats available in ROM. Other radio formats may be available in the form of radio firmware patches or programs through the Software Development Kit (SDK) and may combine features in a different manner, as well as add other features.

**Table 8-1. Feature Support**

| Feature                                     | Main 2-(G)FSK Mode | High Data Rates      | Low Data Rates       | SimpleLink™ Long Range |
|---------------------------------------------|--------------------|----------------------|----------------------|------------------------|
| Programmable preamble, sync word and CRC    | Yes                | Yes                  | Yes                  | No                     |
| Programmable receive bandwidth              | Yes                | Yes                  | Yes (down to 4kHz)   | Yes                    |
| Data / Symbol rate <sup>(3)</sup>           | 20 to 1000 kbps    | ≤ 2 Msps             | ≤ 100 kbps           | ≤ 20 kbps              |
| Modulation format                           | 2-(G)FSK           | 2-(G)FSK<br>4-(G)FSK | 2-(G)FSK<br>4-(G)FSK | 2-(G)FSK               |
| Dual Sync Word                              | Yes                | Yes                  | No                   | No                     |
| Carrier Sense <sup>(1)</sup> <sup>(2)</sup> | Yes                | No                   | No                   | No                     |
| Preamble Detection <sup>(2)</sup>           | Yes                | Yes                  | Yes                  | No                     |
| Data Whitening                              | Yes                | Yes                  | Yes                  | Yes                    |
| Digital RSSI                                | Yes                | Yes                  | Yes                  | Yes                    |
| CRC filtering                               | Yes                | Yes                  | Yes                  | Yes                    |
| Direct-sequence spread spectrum (DSSS)      | No                 | No                   | No                   | 1:2<br>1:4<br>1:8      |
| Forward error correction (FEC)              | No                 | No                   | No                   | Yes                    |
| Link Quality Indicator (LQI)                | Yes                | Yes                  | Yes                  | Yes                    |

- (1) Carrier Sense can be used to implement HW-controlled listen-before-talk (LBT) and Clear Channel Assessment (CCA) for compliance with such requirements in regulatory standards. This is available through the CMD\_PROP\_CS radio API.
- (2) Carrier Sense and Preamble Detection can be used to implement sniff modes where the radio is duty cycled to save power.
- (3) Data rates are only indicative. Data rates outside this range may also be supported. For some specific combinations of settings, a smaller range might be supported.

## 8.4 Memory

The up to 352KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the `ccfg.c` source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is a single 32KB block and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8KB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).

The ROM contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

## 8.5 Cryptography

The CC1311P3 device comes with a wide set of cryptography-related hardware accelerators, reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations run in a background hardware thread.

The hardware accelerator modules are:

- **True Random Number Generator (TRNG)** module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.
- **Advanced Encryption Standard (AES)** with 128 bit key lengths

Together with the hardware accelerator module, a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The TI provided cryptography drivers are:

- **Key Agreement Schemes**
  - Elliptic curve Diffie–Hellman with static or ephemeral keys (ECDH and ECDHE)
- **Signature Generation**
  - Elliptic curve Diffie–Hellman Digital Signature Algorithm (ECDSA)
- **Curve Support**
  - Short Weierstrass form (full hardware support), such as:
    - NIST-P256
  - Montgomery form (hardware support for multiplication), such as:
    - Curve25519
- **Hash**
  - SHA256
- **MACs**
  - HMAC with SHA256
  - AES CBC-MAC
- **Block ciphers**
  - AESECB
  - AESCBC
  - AESCTR
- **Authenticated Encryption**
  - AESCCM
- **Random number generation**
  - True Random Number Generator
  - AES CTR DRBG

## 8.6 Timers

A large selection of timers are available as part of the CC1311P3 device. These timers are:

- **Real-Time Clock (RTC)**

A 70-bit 3-channel timer running on the 32kHz low frequency system clock (SCLK\_LF)

This timer is available in all power modes except Shutdown. The timer can be calibrated to compensate for frequency drift when using the LF RCOSC as the low frequency system clock. If an external LF clock with frequency different from 32.768kHz is used, the RTC tick speed can be adjusted to compensate for this. When using TI-RTOS, the RTC is used as the base timer in the operating system and should thus only be accessed through the kernel APIs such as the Clock module. By default, the RTC halts when a debugger halts the device.

- **General Purpose Timers (GPTIMER)**

The four flexible GPTIMERS can be used as either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48MHz. Each of the 16- or 32-bit timers support a wide range of features such as one-shot or periodic counting, pulse width modulation (PWM), time counting between edges and edge counting. The inputs and outputs of the timer are connected to the device event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. The GPTIMERS are available in Active and Idle power modes.

- **Radio Timer**

A multichannel 32-bit timer running at 4MHz is available as part of the device radio. The radio timer is typically used as the timing base in wireless network communication using the 32-bit timing word as the network time. The radio timer is synchronized with the RTC by using a dedicated radio API when the device radio is turned on or off. This ensures that for a network stack, the radio timer seems to always be running when the radio is enabled. The radio timer is in most cases used indirectly through the trigger time fields in the radio APIs and should only be used when running the accurate 48MHz high frequency crystal is the source of SCLK\_HF.

- **Watchdog timer**

The watchdog timer is used to regain control if the system operates incorrectly due to software errors. It is typically used to generate an interrupt to and reset of the device for the case where periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 1.5MHz clock rate and cannot be stopped once enabled. The watchdog timer pauses to run in Standby power mode and when a debugger halts the device.

## 8.7 Serial Peripherals and I/O

The SSI is a synchronous serial interface that is compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSI support both SPI master and slave up to 4MHz. The SSI module support configurable phase and polarity.

The UART implement universal asynchronous receiver and transmitter functions. It support flexible baud-rate generation up to a maximum of 3Mbps.

The I<sup>2</sup>S interface is used to handle digital audio and can also be used to interface pulse-density modulation microphones (PDM).

The I<sup>2</sup>C interface is also used to communicate with devices compatible with the I<sup>2</sup>C standard. The I<sup>2</sup>C interface can handle 100kHz and 400kHz operation, and can serve as both master and slave.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in [Section 6](#). All digital peripherals can be connected to any digital pin on the device.

For more information, see the [CC13x1x3, CC26x1x3 SimpleLink™ Wireless MCU Technical Reference Manual](#).

## 8.8 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC1311P3 device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

## 8.9 Voltage Supply Domains

The CC1311P3 device can interface to two or three different voltage domains depending on the package type. On-chip level converters ensure correct operation as long as the signal voltage on each input/output pin is set with respect to the corresponding supply pin (VDDS, VDDS2, or VDDS3). [Pin Function to VDDS Mapping Table](#) lists the pin-to-VDDS mapping.

**Table 8-2. Pin Function to VDDS Mapping Table**

|                            | Package                             |                                     |
|----------------------------|-------------------------------------|-------------------------------------|
|                            | VQFN 7 × 7 (RGZ)                    | VQFN 5 × 5 (RKP)                    |
| <b>VDDS</b> <sup>(1)</sup> | DIO 23–30<br>Reset_N                | DIO 15–22<br>Reset_N                |
| <b>VDDS2</b>               | DIO 1–11                            | DIO 1–9                             |
| <b>VDDS3</b>               | DIO 12–22<br>JTAG_TCKC<br>JTAG_TMSC | DIO 10–14<br>JTAG_TCKC<br>JTAG_TMSC |

(1) The VDDS\_DCDC pin must always be connected to the same voltage as the VDDS pin.

## 8.10 μDMA

The device includes a direct memory access (μDMA) controller. The μDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The μDMA controller can perform a transfer between memory and peripherals. The μDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the μDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels

- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

### 8.11 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface. The device boots by default into cJTAG mode and must be reconfigured to use 4-pin JTAG.

## 8.12 Power Management

To minimize power consumption, the CC1311P3 supports a number of power modes and power management features (see [Table 8-3](#)).

**Table 8-3. Power Modes**

| MODE                             | SOFTWARE CONFIGURABLE POWER MODES |                     |                     |           | RESET PIN HELD |
|----------------------------------|-----------------------------------|---------------------|---------------------|-----------|----------------|
|                                  | ACTIVE                            | IDLE                | STANDBY             | SHUTDOWN  |                |
| <b>CPU</b>                       | Active                            | Off                 | Off                 | Off       | Off            |
| <b>Flash</b>                     | On                                | Available           | Off                 | Off       | Off            |
| <b>SRAM</b>                      | On                                | On                  | Retention           | Off       | Off            |
| <b>Radio</b>                     | Available                         | Available           | Off                 | Off       | Off            |
| <b>Supply System</b>             | On                                | On                  | Duty Cycled         | Off       | Off            |
| Register and CPU retention       | Full                              | Full                | Partial             | No        | No             |
| SRAM retention                   | Full                              | Full                | Full                | No        | No             |
| 48MHz high-speed clock (SCLK_HF) | XOSC_HF or RCOSC_HF               | XOSC_HF or RCOSC_HF | Off                 | Off       | Off            |
| 32kHz low-speed clock (SCLK_LF)  | XOSC_LF or RCOSC_LF               | XOSC_LF or RCOSC_LF | XOSC_LF or RCOSC_LF | Off       | Off            |
| Peripherals                      | Available                         | Available           | Off                 | Off       | Off            |
| Wake-up on RTC                   | Available                         | Available           | Available           | Off       | Off            |
| Wake-up on pin edge              | Available                         | Available           | Available           | Available | Off            |
| Wake-up on reset pin             | On                                | On                  | On                  | On        | On             |
| Brownout detector (BOD)          | On                                | On                  | Duty Cycled         | Off       | Off            |
| Power-on reset (POR)             | On                                | On                  | On                  | Off       | Off            |
| Watchdog timer (WDT)             | Available                         | Available           | Paused              | Off       | Off            |

In **Active** mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see [Table 8-3](#)).

In **Idle** mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event or RTC event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

### Note

The power, RF and clock management for the CC1311P3 device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC1311P3 software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete [SDK](#) with TI-RTOS (optional), device drivers, and examples are offered free of charge in source code.

## 8.13 Clock Systems

The CC1311P3 device has several internal system clocks.

The 48MHz SCLK\_HF is used as the main system (MCU and peripherals) clock. This can be driven by the internal 48MHz RC Oscillator (RCOSC\_HF) or an external 48MHz crystal (XOSC\_HF). Radio operation requires an external 48MHz crystal.

SCLK\_LF is the 32.768kHz internal low-frequency system clock. It can be used for the RTC and to synchronize the radio timer before or after Standby power mode. SCLK\_LF can be driven by the internal 32.8kHz RC Oscillator (RCOSC\_LF), a 32.768kHz watch-type crystal, or a clock input on any digital IO.

When using a crystal or the internal RC oscillator, the device can output the 32kHz SCLK\_LF signal to other devices, thereby reducing the overall system cost.

## 8.14 Network Processor

Depending on the product configuration, the CC1311P3 device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the system CPU inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

## 9 Application, Implementation, and Layout

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

For general design guidelines and hardware configuration guidelines, refer to [CC13xx/CC26xx Hardware Configuration and PCB Design Considerations Application Note](#).

For optimum RF performance, especially when using the high-power PA, it is important to accurately follow the reference design with respect to component values and layout. Failure to do so may lead to reduced RF performance due to balun mismatch. The amplitude- and phase balance through the balun must be <1 dB and <6 degrees, respectively.

PCB stack-up is also critical for proper operation. The CC1311P3 EVMs and characterization boards use a finished thickness between the top layer (RF signals) and layer 2 (ground plane) of 175µm. It is very important to use the same substrate thickness, or slightly thicker, in an end product implementing the CC1311P3 device.

### 9.1 Reference Designs

The following reference designs should be followed closely when implementing designs using the CC1311P3 device.

Special attention must be paid to RF component placement, decoupling capacitors and DCDC regulator components, as well as ground connections for all of these.

#### [CC1311-P3EM-7XD7793-PA915 Design Files](#)

The CC1311P3EM-XD7793-PA915 reference design provides schematic, layout and production files for the characterization board used for deriving the performance number found in this document. This reference design is intended for operation in the 868MHz and 915MHz bands.

#### [LP-CC1311P3 Design Files](#)

The CC1311P3 LaunchPad Design Files contain detailed schematics and layouts to build application specific boards using the CC1311P3 device. This LaunchPad is intended for operation in the 868MHz and 915MHz bands.

#### [Sub-1GHz and 2.4GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag](#)

The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169MHz to 2.4GHz, including:

- PCB antennas
- Helical antennas
- Chip antennas
- Dual-band antennas for 868MHz and 915MHz combined with 2.4GHz

The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad Development Kits and SensorTags.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

### 10.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, XCC1311P3 is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RGZ).

For orderable part numbers of CC1311P3 devices in the RGZ (7mm x 7mm) package type, see the *Package Option Addendum* of this document, the Device Information in [Section 3](#), the TI website ([www.ti.com](http://www.ti.com)), or contact your TI sales representative.

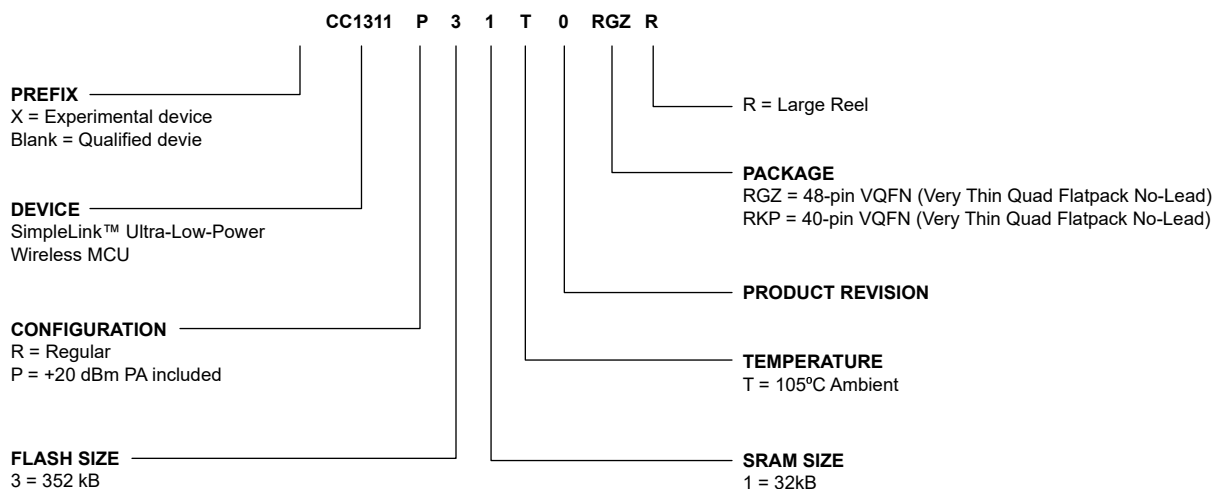


**Figure 10-1. Device Nomenclature**

## 10.2 Tools and Software

The CC1311P3 device is supported by a variety of software and hardware development tools.

### Development Kit

#### Software

##### SimpleLink™ CC13XX- CC26XX SDK

The SimpleLink CC13xx and CC26xx Software Development Kit (SDK) provides a complete package for the development of wireless applications on the CC13XX / CC26XX family of devices. The SDK includes a comprehensive software package for the CC1311P3 device, including the following protocol stacks:

- Bluetooth Low Energy 4 and 5.2
- Thread (based on OpenThread)
- Zigbee 3.0
- Wi-SUN®
- TI 15.4-Stack - an IEEE 802.15.4-based star networking solution for Sub-1GHz and 2.4 GHz
- Proprietary RF - a large set of building blocks for building proprietary RF software
- Multiprotocol support - concurrent operation between stacks using the Dynamic Multiprotocol Manager (DMM)

The SimpleLink CC13XX-CC26XX SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit <http://www.ti.com/simplelink>.

## Development Tools

### Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

### Code Composer Studio™ Cloud IDE

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

### IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32 KB size-limited version is available through [iar.com](http://iar.com).

### SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests - send and receive packets between nodes
- Antenna and radiation tests - set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

### CCS UniFlash

CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

### 10.2.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on [ti.com/simplelink](https://ti.com/simplelink).

### 10.3 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder on [ti.com/product/CC1311P3](https://ti.com/product/CC1311P3). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

#### TI Resource Explorer

##### TI Resource Explorer

Software examples, libraries, executables, and documentation are available for your device and development board.

#### Errata

##### CC1311P3 Silicon Errata

The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

#### Application Notes

All application notes for the CC1311P3 device are found on the device product folder at: [ti.com/product/CC1311P3/#tech-docs](https://ti.com/product/CC1311P3/#tech-docs).

#### Technical Reference Manual (TRM)

##### CC13x1x, CC26x1x SimpleLink™ Wireless MCU TRM

The TRM provides a detailed description of all modules and peripherals available in the device family.

### 10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.5 Trademarks

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IAR Embedded Workbench® is a registered trademark of IAR Systems AB.

Windows® is a registered trademark of Microsoft Corporation.

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## 10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from March 1, 2022 to April 1, 2025 (from Revision \* (March 2022) to Revision A (April 2025))

|                                                                                     | Page |
|-------------------------------------------------------------------------------------|------|
| • Updated the document per the latest Texas Instruments data sheet standards.....   | 2    |
| • Updated <a href="#">Device Comparison</a> .....                                   | 5    |
| • Added RKP data.....                                                               | 9    |
| • Split Rail functionality added to Absolute Maximum Ratings table.....             | 9    |
| • Split Rail functionality added to the Recommended Operating Conditions table..... | 9    |
| • Clarified that current consumption is measured with VDDS=VDDS2=VDDS3.....         | 10   |
| • Added <a href="#">Voltage Supply Domains</a> .....                                | 43   |

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">CC1311P31T0RGZR</a> | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 105   | CC1311<br>P31       |
| CC1311P31T0RGZR.A               | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 105   | CC1311<br>P31       |
| CC1311P31T0RGZR.B               | Active        | Production           | VQFN (RGZ)   48 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 105   | CC1311<br>P31       |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

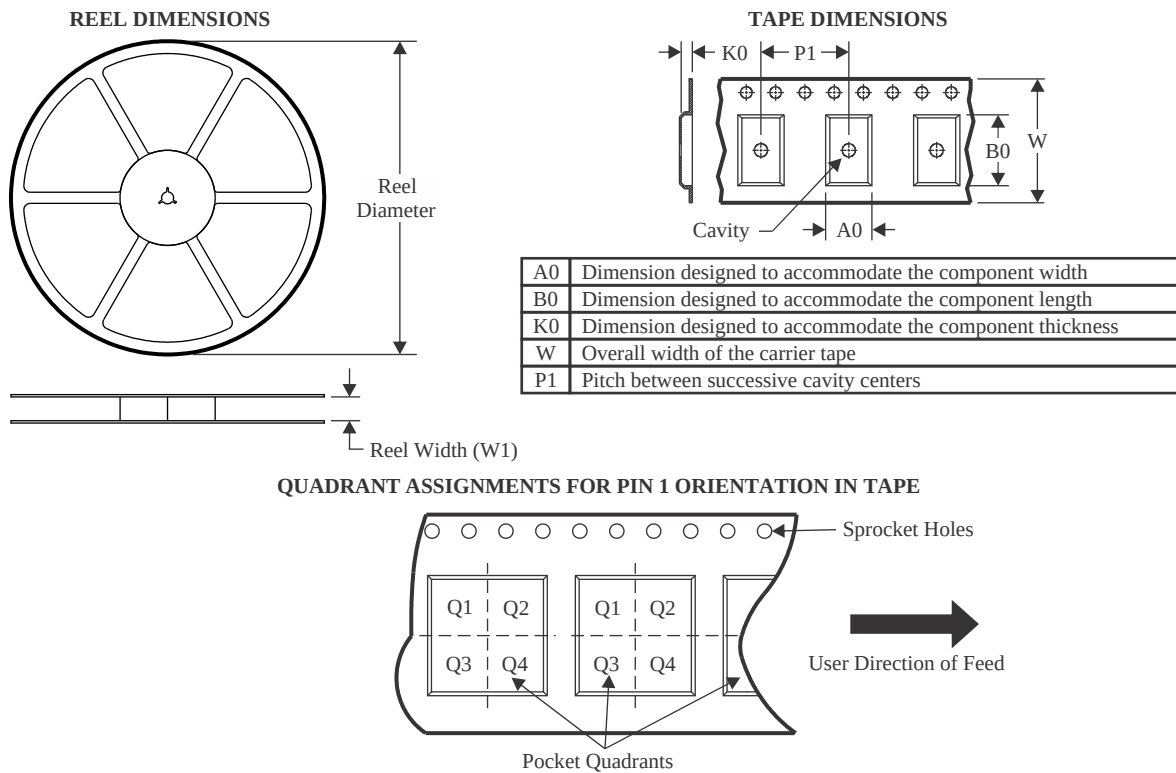
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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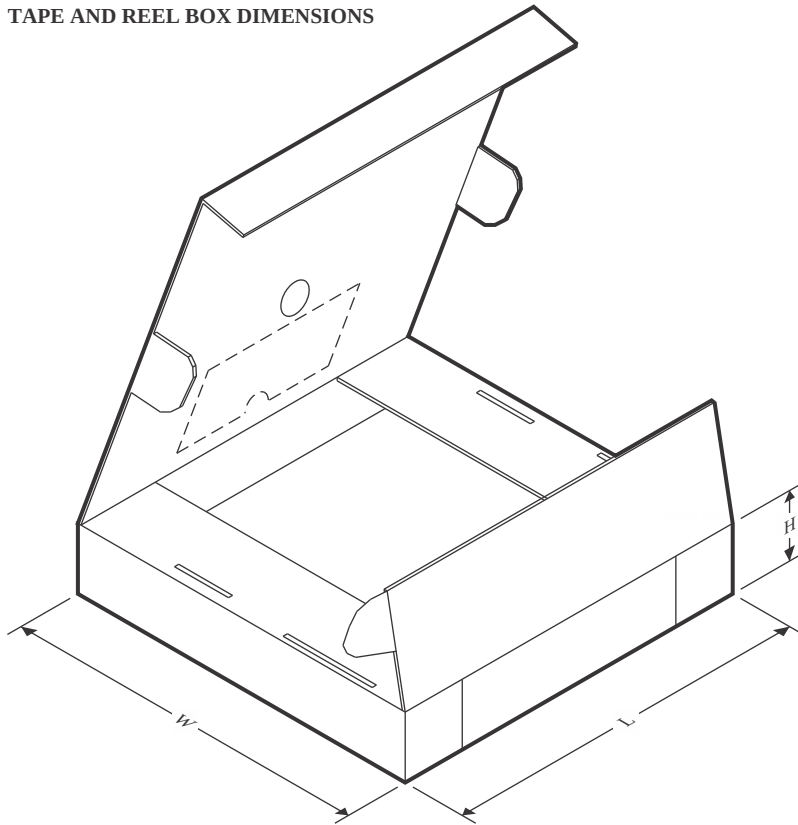
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CC1311P31T0RGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| CC1311P31T0RGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CC1311P31T0RGZR | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 35.0        |
| CC1311P31T0RGZR | VQFN         | RGZ             | 48   | 2500 | 360.0       | 360.0      | 36.0        |

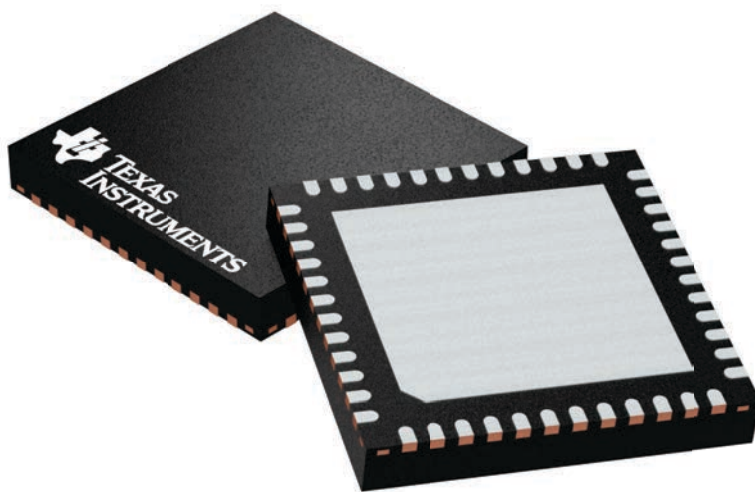
## GENERIC PACKAGE VIEW

**RGZ 48**

**VQFN - 1 mm max height**

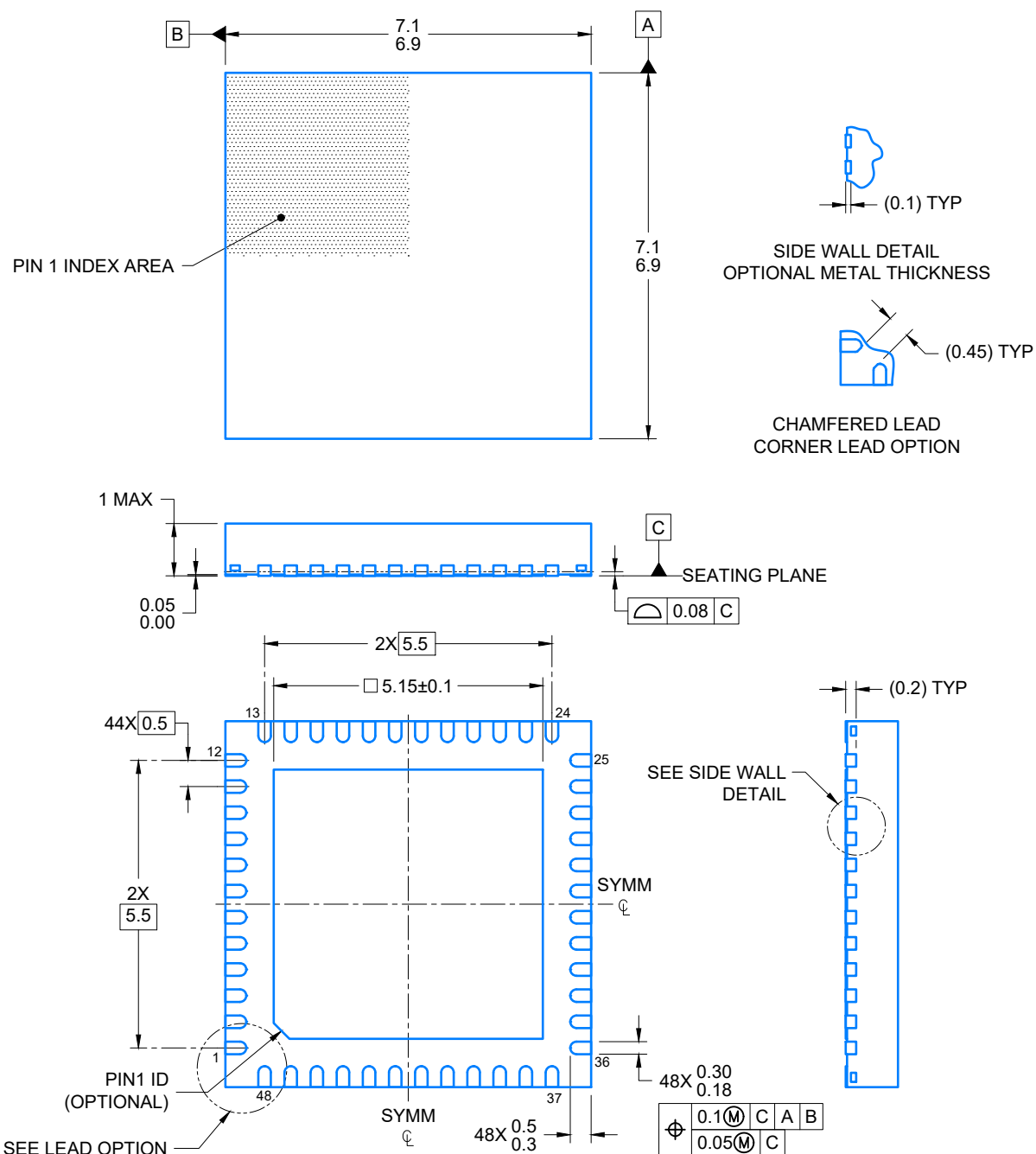
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

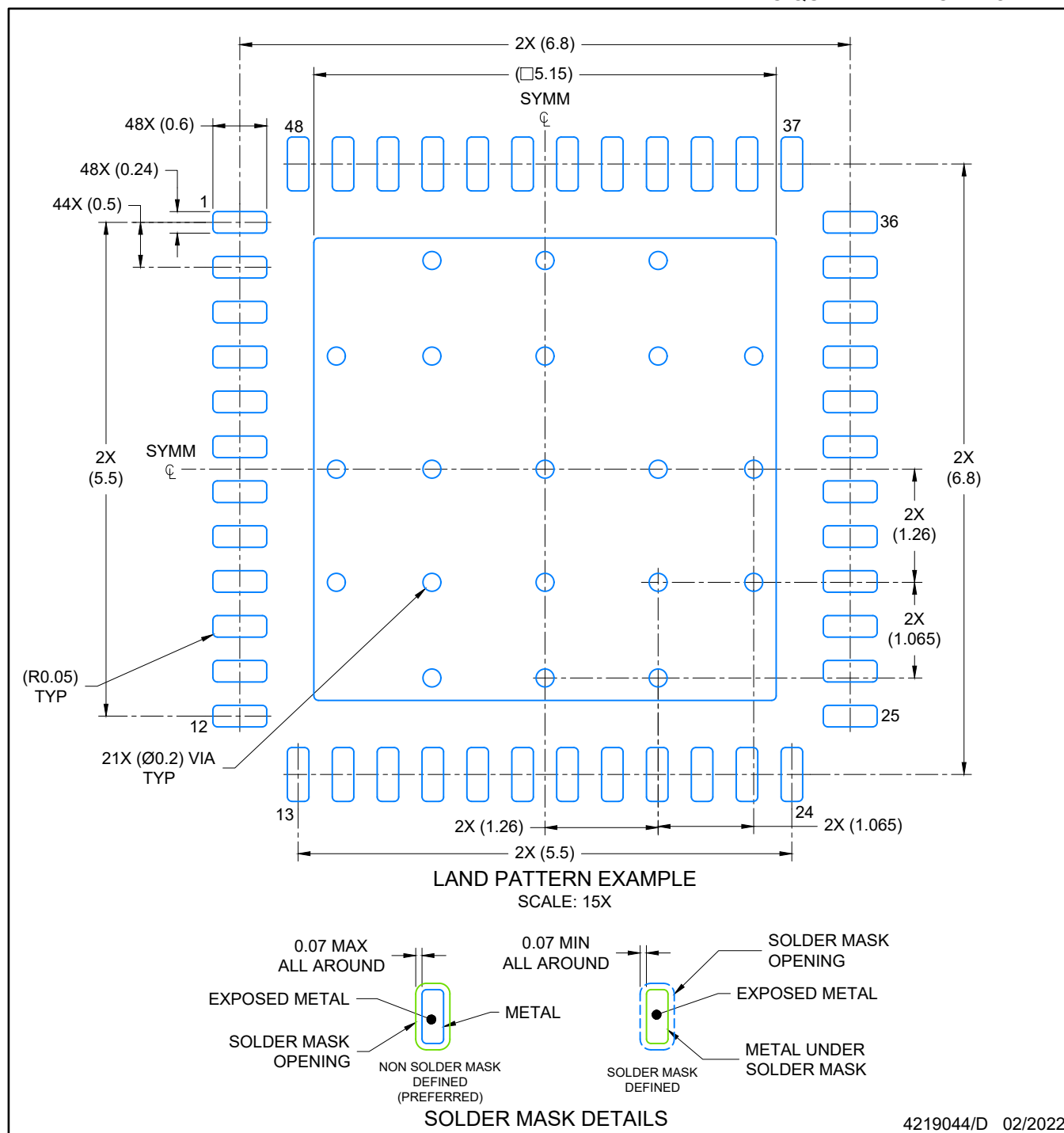
4224671/A



4219044/D 02/2022

## NOTES:

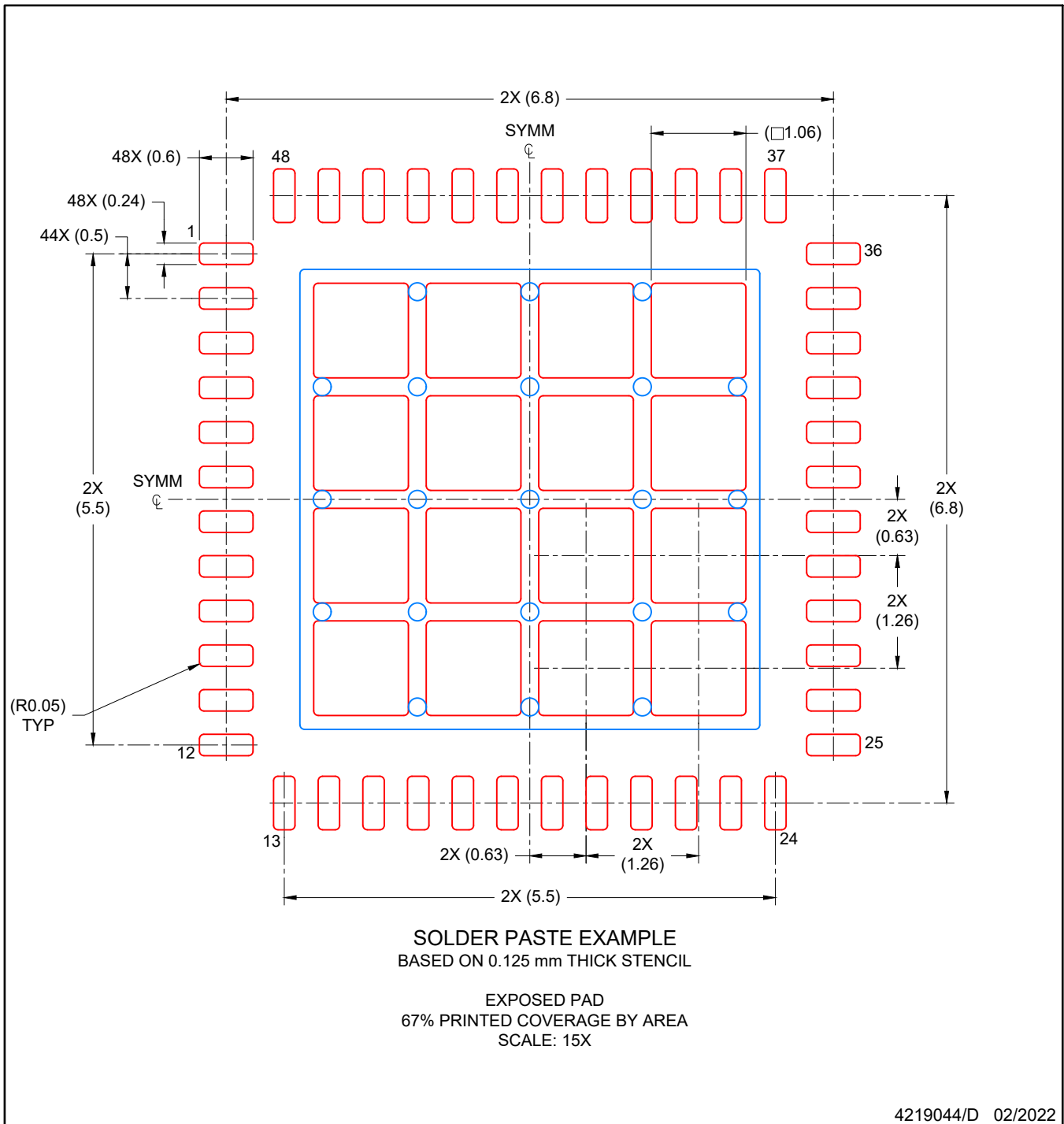
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



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NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025

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