CC3230S and CC3230SF SimpleLink™ Wi-Fi® 2.4GHz Wireless MCU with Coexistence

1 Features

- Multiple-core architecture, system-on-chip (SoC)
- Multilayered security features, help developers protect identities, data, and software IP
- Low-power modes for battery powered application
- Coexistence with BLE radios (CC13x2/CC26x2)
- Network-assisted roaming
- Industrial temperature: –40°C to +85°C
- Wi-Fi CERTIFIED® by the Wi-Fi Alliance®
- Application microcontroller subsystem:
  - Arm® Cortex®-M4 core at 80MHz
  - User-dedicated memory
    - 256KB of RAM
    - Optional 1MB of executable flash
  - Rich set of peripherals and timers
  - 27 I/O pins with flexible multiplexing options
    - UART, I2S, I^{2}C, SPI, SD, ADC, 8-bit parallel interface
    - Timers and PWM
- Wi-Fi network processor subsystem:
  - Wi-Fi® core:
    - 802.11b/g/n 2.4GHz
    - Modes:
      - Access Point (AP)
      - Station (STA)
      - Wi-Fi Direct®
    - Security:
      - WEP
      - WPA™/ WPA2™ PSK
      - WPA2 Enterprise
      - WPA3™ Personal
      - WPA3™ Enterprise
  - Internet and application protocols:
    - HTTPs server, mDNS, DNS-SD, DHCP
    - IPv4 and IPv6 TCP/IP stack
    - 16BSD sockets (fully secured TLS v1.2 and SSL 3.0)
  - Built-in power management subsystem:
    - Configurable low-power profiles (always, intermittent, tag)
    - Advanced low-power modes
    - Integrated DC/DC regulators
- Multilayered security features:
  - Separate execution environments
  - Networking security
  - Device identity and key
  - Hardware accelerator cryptographic engines (AES, DES, SHA/MD5, CRC)
  - Application-level security (encryption, authentication, access control)
  - Initial secure programming
  - Software tamper detection
  - Secure boot
  - Certificate signing request (CSR)
  - Unique per device key pair
- Application throughput:
  - UDP: 16Mbps, TCP: 13Mbps
  - Peak: 72Mbps
- Power-Management Subsystem:
  - Integrated DC/DC converters support a wide range of supply voltage:
    - VBAT wide-voltage mode: 2.1V to 3.6V
    - VIO is always tied with VBAT
  - Advanced low-power modes:
    - Shutdown: 1µA, hibernate: 4.5µA
    - Low-power deep sleep (LPDS): 120µA
    - Idle connected (MCU in LPDS): 710µA
    - RX traffic (MCU active): 59mA
    - TX traffic (MCU active): 223mA
- Wi-Fi TX power:
  - 18.0dBm at 1 DSSS
  - 14.5dBm at 54OFDM
- Wi-Fi RX sensitivity:
  - –96dBm at 1 DSSS
  - –74.5dBm at 54 OFDM
- Clock source:
  - 40.0MHz crystal with internal oscillator
  - 32.768kHz crystal or external RTC
- RGK package
  - 64-pin, 9mm × 9mm very thin quad flat nonleaded (VQFN) package, 0.5mm pitch
- Device supports SimpleLink™ MCU Platform developer's ecosystem

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

2 Applications

- For Internet of Things applications, such as:
  - Building and home automation:
    - HVAc systems and thermostat
    - Video surveillance, video doorbells, and low-power camera
    - Building security systems and e-locks
    - Smoke detector
    - Water leak detector
  - Appliances
    - Smart home remote control
  - Asset tracking
  - Factory automation
  - Medical and healthcare
    - CPAP
  - Grid infrastructure

3 Description

The SimpleLink™ Wi-Fi® CC3230x wireless MCU comes in two variants: CC3230S and C3230SF.

- The *CC3230S* includes 256KB of RAM, IoT networking security, device identity/keys, as well as, MCU level security features such as file system encryption, user IP (MCU image) encryption, secure boot and debug security.
- The *CC3230SF* builds on the CC3230S and integrates a user-dedicated 1MB of executable flash in addition to the 256KB of RAM.

Simplify your IoT design with a Wi-Fi CERTIFIED™ wireless microcontroller (MCU). The *SimpleLink™ Wi-Fi®* CC3230x device family is a system-on-chip (SoC) solution that integrates two processors within a single chip, including:

- Application processor: Arm® Cortex®-M4 MCU with a user-dedicated 256KB of RAM and an optional 1MB of executable flash
- Network processor to run all Wi-Fi and internet logical layers. This ROM-based subsystem completely offloads the host MCU and includes an 802.11b/g/n 2.4GHz radio, baseband, and MAC with a powerful hardware cryptography engine

These devices introduce new capabilities that further simplify the connectivity of things to the internet. The main new features include the following:

- Bluetooth® Low Energy and Wi-Fi 2.4GHz radio coexistence (CC13x2/CC26x2)
- Antenna selection
- Up to 16 concurrent secure sockets
- Certificate sign request (CSR)
- Online certificate status protocol (OCSP)
- Wi-Fi Alliance® certified IoT power-saving features (such as BSS max idle, DMS, and proxy ARP)
- Hostless mode for offloading template packet transmissions
- Network-assisted roaming

The CC3230x device family is part of the SimpleLink™ MCU platform—a common, easy-to-use development environment based on a single-core software development kit (SDK) with a rich tool set and reference designs. The E2E™ community supports Wi-Fi, Bluetooth® low energy, Sub-1GHz, and host MCUs. For more information, visit www.ti.com/simplelink or www.ti.com/simplelinkwifi.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE
CC3230SM2RGKR	VQFN (64)	9.00mm × 9.00mm
CC3230SF12RGKR	VQFN (64)	9.00mm × 9.00mm

(1) For more information, see Section 12.

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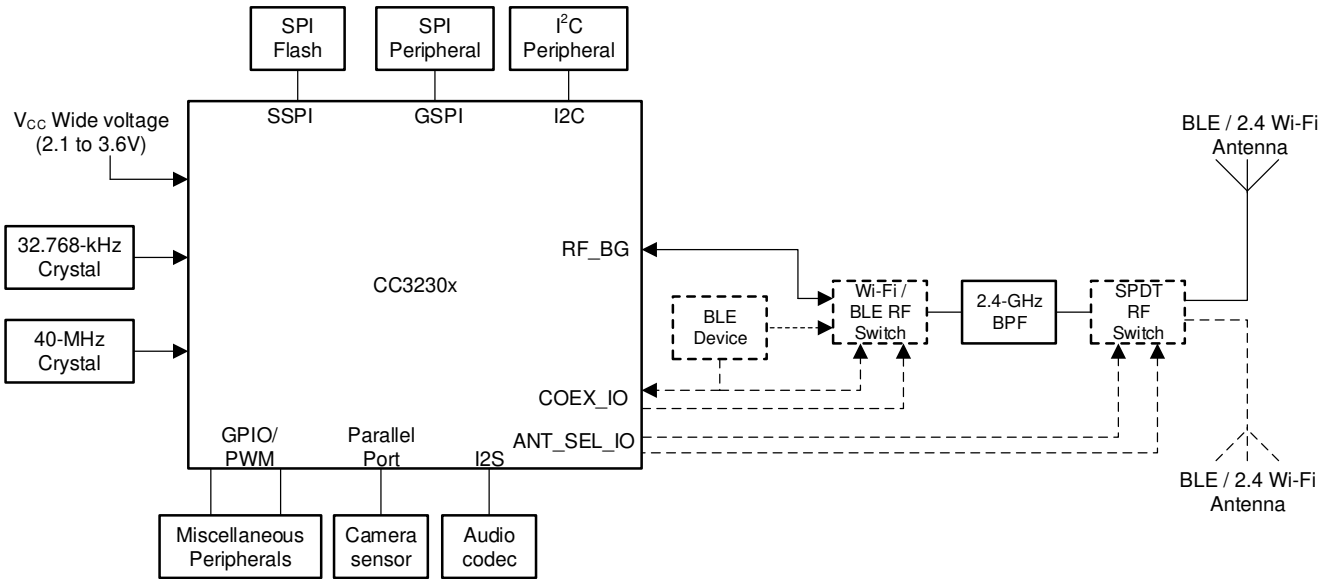
4 Functional Block Diagrams

Figure 4-1 shows the functional block diagram of the CC3230x SimpleLink Wi-Fi solution.



When using the antenna selection feature (dual antenna), an SPDT switch and two GPIO lines are required.

Figure 4-1. CC3230x Functional Block Diagram

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Figure 4-1 shows the hardware overview for the CC3230x device.

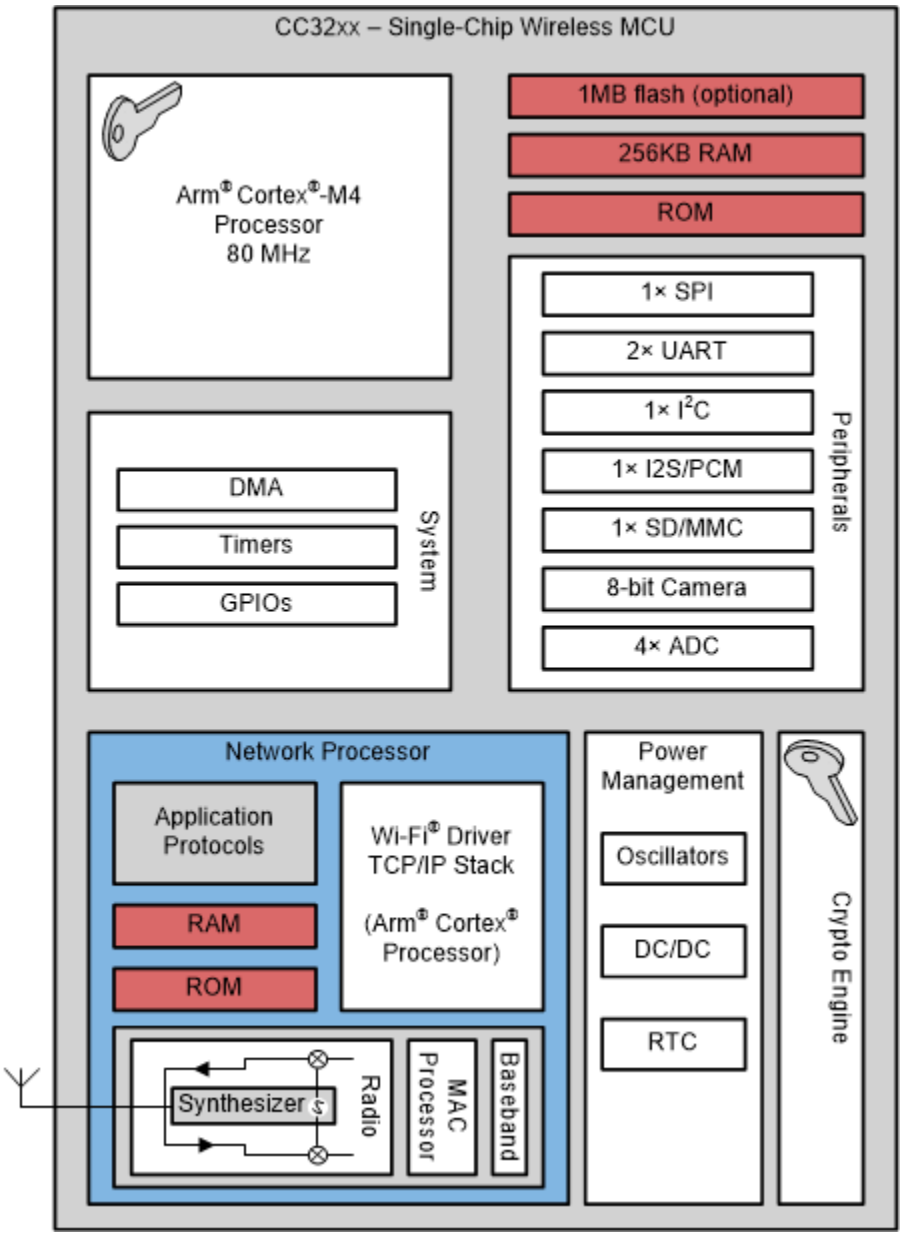

Figure 4-2. CC320x Hardware Overview

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Figure 4-3 shows an overview of the embedded software in the CC3230x device.

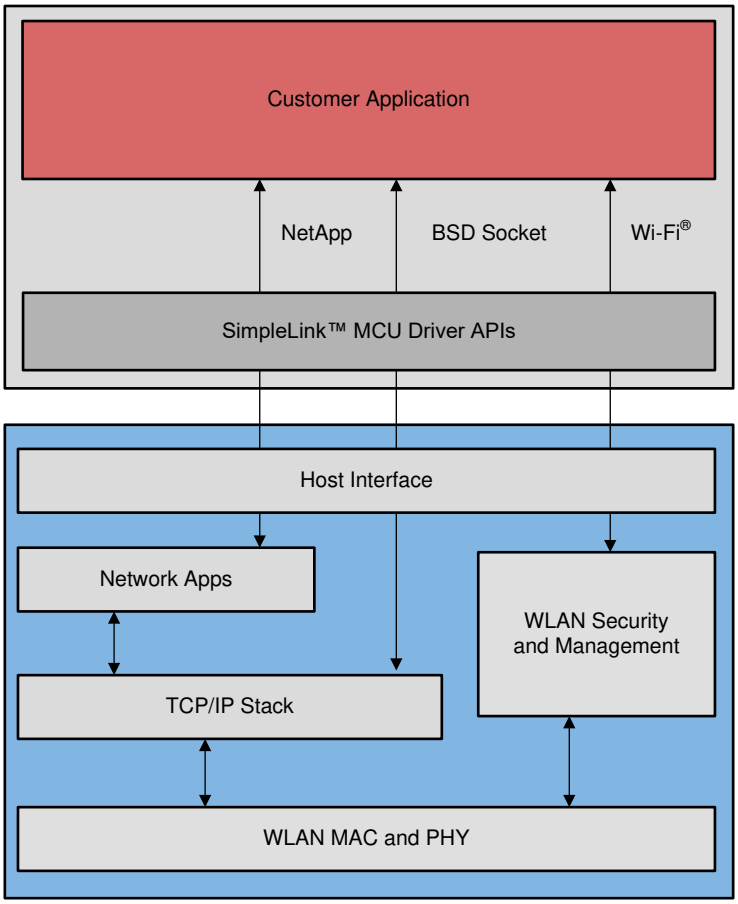

Figure 4-3. CC3230x Embedded Software Overview

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5 Device Comparison

Table 5-1 lists the features supported across different CC3x3x devices.

Table 5-1. Comparison of Device Features

FEATURE	DEVICE					
	CC3130	CC3135	CC3230S	CC3230SF	CC3235S	CC3235SF
Classification	Network Processor	Network Processor	Wireless microcontroller	Wireless microcontroller	Wireless microcontroller	Wireless microcontroller
Standard	802.11b/g/n	802.11a/b/g/n	802.11b/g/n	802.11b/g/n	802.11a/b/g/n	802.11a/b/g/n
TCP/IP stack	IPv4, IPv6	IPv4, IPv6	IPv4, IPv6	IPv4, IPv6	IPv4, IPv6	IPv4, IPv6
Sockets	16	16	16	16	16	16
Package	9mm × 9mm VQFN	9mm × 9mm VQFN	9mm × 9mm VQFN	9mm × 9mm VQFN	9mm × 9mm VQFN	9mm × 9mm VQFN
ON-CHIP APPLICATION MEMORY						
Flash	—	—	—	1MB	—	1MB
RAM	—	—	256KB	256KB	256KB	256KB
RF FEATURES						
Frequency	2.4GHz	2.4GHz, 5GHz	2.4GHz	2.4GHz	2.4GHz, 5GHz	2.4GHz, 5GHz
Coexistence with BLE Radio	Yes	Yes	Yes	Yes	Yes	Yes
SECURITY FEATURES						
Secure boot	—	—	Yes	Yes	Yes	Yes
FIPS 140-2 Level 1 Certification(1)	No	Yes	No	No	Yes	Yes
Enhanced application level security	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming	File system security Secure key storage Software tamper detection Cloning protection Initial secure programming
Wi-Fi level of security (1)	WEP, WPS, WPA / WPA2 PSK, WPA2 (802.1x), WPA3 personal and enterprise					
Additional networking security	Unique device identity Trusted root-certificate catalog TI Root-of-trust public key Online certificate status protocol (OCSP) Certificate signing request (CSR) Unique per-device key pair					
Hardware acceleration	Hardware crypto engines					

(1) For exact status of FIPS certification for a specific part number, please refer to https://csrc.nist.gov/publications/fips.

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5.1 Related Products

For information about other devices in this family of products or related products, see the links that follow.

The SimpleLink™ MCU Portfolio	This portfolio offers a single development environment that delivers flexible hardware, software, and tool options for customers developing wired and wireless applications. With 100 percent code reuse across host MCUs, Wi-Fi®, Bluetooth® low energy, Sub-1 GHz devices and more, choose the MCU or connectivity standard that fits your design. A one-time investment with the SimpleLink™ software development kit (SDK) allows you to reuse often, opening the door to create unlimited applications.
SimpleLink™ Wi-Fi® Family	This device platform offers several Internet-on-a chip™ solutions, which address the need of battery-operated, security-enabled products. Texas Instruments offers a single-chip wireless microcontroller and a wireless network processor that can be paired with any MCU, allowing developers to design new Wi-Fi® products or upgrade existing products with Wi-Fi® capabilities.
BoosterPack™ Plug-in Module	Extend the functionality of the TI LaunchPad™ Development Kit with the BoosterPack™ Plug-in Module. The application-specific BoosterPack Plug-in Module allows you to explore a broad range of applications, including capacitive touch, wireless sensing, LED Lighting control, and more. Stack multiple BoosterPack Plug-in Modules onto a single LaunchPad Development Kit to further enhance the functionality of your design.
Reference Designs	Find reference designs leveraging the best in TI technology – from analog and power management to embedded processors.
The SimpleLink™ Wi-Fi® SDK	The SDK contains drivers for the CC3230 programmable MCU, sample applications, and documentation required to start development with CC3230x solutions.

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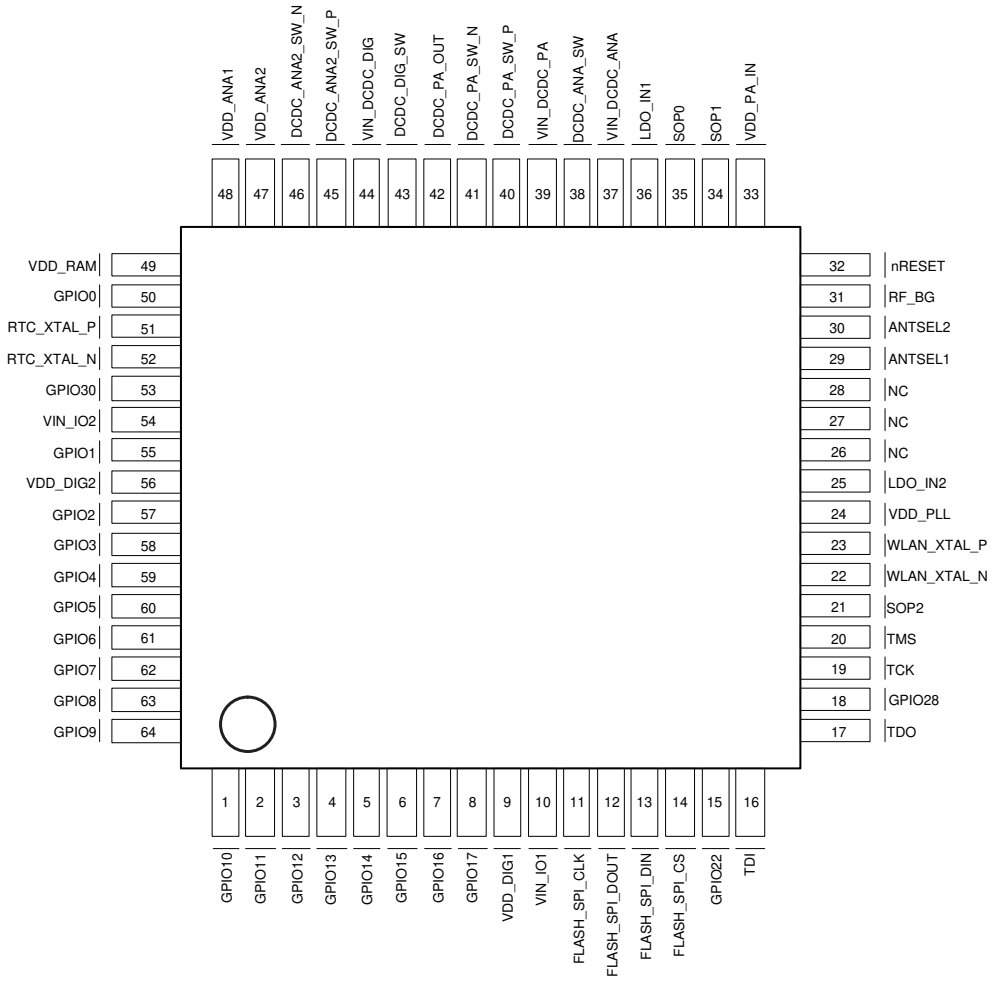
6 Terminal Configuration and Functions

6.1 Pin Diagram

Figure 6-1 shows pin assignments for the 64-pin VQFN package.



NC = No internal connection

Figure 6-1. Top View Pin Assignment for 64-Pin VQFN

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6.2 Pin Attributes

The device makes extensive use of pin multiplexing to accommodate the large number of peripheral functions in the smallest possible package. To achieve this configuration, pin multiplexing is controlled using a combination of hardware configuration (at device reset) and register control.

Note

TI highly recommends using *SysConfig* to obtain the desired pinout. In addition, refer to the user guide within the SimpleLink™ CC32XX Software Development Kit (SDK)

The board and software designers are responsible for the proper pin multiplexing configuration. Hardware does not ensure that the proper pin multiplexing options are selected for the peripherals or interface mode used.

Section 6.2.1 and Table 6-1 list the pin descriptions and attributes. Table 6-2 lists the signal descriptions. Table 6-3 presents an overall view of pin multiplexing. All pin multiplexing options are configurable using the pin mux registers.

The following special considerations apply:

- All I/Os support 2mA, 4mA, and 6mA drive strengths. The drive strength is individually configurable for each pin.
- All I/Os support 10µA pullup and pulldown resistors.
- The V_{IO} and V_{BAT} supplies must be tied together at all times.
- By default, all I/Os float in the Hibernate state. However, the default state can be changed by software.
- All digital I/Os are nonfail-safe.

Note

If an external device drives a positive voltage to the signal pads and the CC3230x device is not powered, DC is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wakeup and boot of the CC3230x device can occur. To prevent current draw, TI recommends any one of the following conditions:

- All devices interfaced to the CC3230x device must be powered from the same power rail as the chip.
- Use level shifters between the device and any external devices fed from other independent rails.
- The nRESET pin of the CC3230x device must be held low until the V_{BAT} supply to the device is driven and stable.
- All GPIO pins default to high impedance unless programmed by the MCU. The bootloader sets the TDI, TDO, TCK, TMS, and Flash_SPI pins to mode 1. All the other pins are left in the Hi-Z state.

The ADC inputs are tolerant up to 1.8V (see Section 7.16.6.6.1 for more details about the usable range of the ADC). On the other hand, the digital pads can tolerate up to 3.6V. Hence, take care to prevent accidental damage to the ADC inputs. TI recommends first disabling the output buffers of the digital I/Os corresponding to the desired ADC channel (that is, converted to Hi-Z state), and thereafter disabling the respective pass switches (S7 [Pin 57], S8 [Pin 58], S9 [Pin 59], and S10 [Pin 60]). For more information, see Section 6.5.

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6.2.1 Pin Descriptions

PINS		TYPE	DESCRIPTION	SELECT AS WAKEUP SOURCE	CONFIGURE ADDITIONAL ANALOG MUX	MUXED WITH JTAG
NO.	NAME					
1	GPIO10	I/O	General-purpose input or output	No	No	No
2	GPIO11	I/O	General-purpose input or output	Yes	No	No
3	GPIO12	I/O	General-purpose input or output	No	No	No
4	GPIO13	I/O	General-purpose input or output	Yes	No	No
5	GPIO14	I/O	General-purpose input or output	No	No	No
6	GPIO15	I/O	General-purpose input or output	No	No	No
7	GPIO16	I/O	General-purpose input or output	No	No	No
8	GPIO17	I/O	General-purpose input or output	Yes	No	No
9	VDD_DIG1	Power	Internal digital core voltage	N/A	N/A	N/A
10	VIN_IO1	Power	I/O power supply (same as battery voltage)	N/A	N/A	N/A
11	FLASH_SPI_CLK	O	Serial flash interface: SPI clock	N/A	N/A	N/A
12	FLASH_SPI_DOUT	O	Serial flash interface: SPI data out	N/A	N/A	N/A
13	FLASH_SPI_DIN	I	Serial flash interface: SPI data in	N/A	N/A	N/A
14	FLASH_SPI_CS	O	Serial flash interface: SPI chip select	N/A	N/A	N/A
15	GPIO22	I/O	General-purpose input or output	No	No	No
16	TDI	I/O	JTAG interface: data input	No	No	Muxed with JTAG TDI
17	TDO	I/O	JTAG interface: data output	Yes	No	Muxed with JTAG TDO
18	GPIO28	I/O	General-purpose input or output	No	No	No
19	TCK	I/O	JTAG / SWD interface: clock	No	No	Muxed with JTAG/ SWD-TCK
20	TMS	I/O	JTAG / SWD interface: mode select or SWDIO	No	No	Muxed with JTAG/ SWD-TMSC
21[(2)]	SOP2	O	Configuration sense-on-power	No	No	No
22	WLAN_XTAL_N	Analog	40MHz XTAL	N/A	N/A	N/A
23	WLAN_XTAL_P	Analog	40MHz XTAL or TCXO clock input	N/A	N/A	N/A
24	VDD_PLL	Power	Internal analog voltage	N/A	N/A	N/A
25	LDO_IN2	Power	Analog RF supply from analog DCDC output	N/A	N/A	N/A
26	NC	—	No Connect	N/A	N/A	N/A
27	NC	—	No Connect	N/A	N/A	N/A
28	NC	—	No Connect	N/A	N/A	N/A
29[(1)]	ANTSEL1	O	Antenna selection control	No	No	No
30[(1)]	ANTSEL2	O	Antenna selection control	No	No	No
31	RF_BG	RF	RF BG band: 2.4GHz TX, RX	N/A	N/A	N/A
32	nRESET	I	Master chip reset input. Active low input.	N/A	N/A	N/A
33	VDD_PA_IN	Power	RF power amplifier (PA) input from PA DC-DC output	N/A	N/A	N/A
34	SOP1	I	Configuration sense-on-power 1	N/A	N/A	N/A
35	SOP0	I	Configuration sense-on-power 0	N/A	N/A	N/A

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PINS		TYPE	DESCRIPTION	SELECT AS WAKEUP SOURCE	CONFIGURE ADDITIONAL ANALOG MUX	MUXED WITH JTAG
NO.	NAME					
36	LDO_IN1	Power	Analog RF supply from analog DCDC output	N/A	N/A	N/A
37	VIN_DCDC_ANA	Power	Analog DC-DC supply input (same as battery voltage)	N/A	N/A	N/A
38	DCDC_ANA_SW	Power	Analog DC/DC converter switching node	N/A	N/A	N/A
39	VIN_DCDC_PA	Power	PA DC/DC converter input supply (same as battery voltage)	N/A	N/A	N/A
40	DCDC_PA_SW_P	Power	PA DC/DC converter +ve switching node	N/A	N/A	N/A
41	DCDC_PA_SW_N	Power	PA DC/DC converter –ve switching node	N/A	N/A	N/A
42	DCDC_PA_OUT	Power	PA DC/DC converter output.	N/A	N/A	N/A
43	DCDC_DIG_SW	Power	Digital DC/DC converter switching node	N/A	N/A	N/A
44	VIN_DCDC_DIG	Power	Digital DC/DC converter supply input (same as battery voltage)	N/A	N/A	N/A
45[4]	DCDC_ANA2_SW_P	I/O	Analog2 DCDC converter +ve switching node	No	User configuration not required [3]	No
46	DCDC_ANA2_SW_N	Power	Analog2 DC-DC converter -ve switching node	N/A	N/A	N/A
47	VDD_ANA2	Power	Analog2 DC-DC output	N/A	N/A	N/A
48	VDD_ANA1	Power	Analog1 power supply fed by ANA2 DC-DC output	N/A	N/A	N/A
49	VDD_RAM	Analog	SRAM LDO output	N/A	N/A	N/A
50	GPIO0	I/O	General-purpose input or output	No	User configuration not required [3]	No
51	RTC_XTAL_P	Analog	32.768kHz XTAL_P or external CMOS level clock input	N/A	N/A	N/A
52[5]	RTC_XTAL_N	Analog	32.768kHz XTAL_N	N/A	User configuration not required [3] [7]	No
53	GPIO30	I/O	General-purpose input or output	No	User configuration not required [3]	No
54	VIN_IO2	Analog	Chip supply voltage (VBAT)	N/A	N/A	N/A
55	GPIO1	I/O	General-purpose input or output	No	No	No
56	VDD_DIG2	Analog	Internal digital core voltage	N/A	N/A	N/A
57[6]	GPIO2	I/O	Analog input (1.5V max) or general-purpose input or output	Wake-up source	See [8]	No
58[6]	GPIO3	I/O	Analog input (1.5V max) or general-purpose input or output	No	See [8]	No
59[6]	GPIO4	I/O	Analog input (1.5V max) or general-purpose input or output	Wake-up source	See [8]	No
60[6]	GPIO5	I/O	Analog input (1.5V max) or general-purpose input or output	No	See [8]	No
61	GPIO6	I/O	General-purpose input or output	No	No	No
62	GPIO7	I/O	General-purpose input or output	No	No	No
63	GPIO8	I/O	General-purpose input or output	No	No	No
64	GPIO9	I/O	General-purpose input or output	No	No	No

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PINS		TYPE	DESCRIPTION	SELECT AS WAKEUP SOURCE	CONFIGURE ADDITIONAL ANALOG MUX	MUXED WITH JTAG
NO.	NAME					
GND_TAB		—	Thermal pad and electrical ground	N/A	N/A	N/A

(1) This pin is reserved for WLAN antenna selection, controlling an external RF switch that multiplexes the RF pin of the CC3230x device between two antennas. These pins must not be used for other functionalities.
(2) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.
(3) Device firmware automatically enables the digital path during ROM boot.
(4) Pin 45 is used by an internal DC/DC converter (ANA2_DCDC). This pin will be available automatically if the serial flash is forced in the CC3230SF device. For the CC3230S devices, pin 45 can be used as GPIO_31 if a supply is provided on pin 47.
(5) Pin 52 is used by the RTC crystal oscillator. These devices use automatic configuration sensing. Therefore, some board-level configuration is required to use pin 52 as a digital pad. Pin 52 is used for the RTC crystal in most applications. However, in some applications, a 32.768kHz square-wave clock might always be available onboard. When a 32.768kHz square-wave clock is available, the crystal can be removed to free pin 52 for digital functions. The external clock must then be applied at pin 51. For the device to automatically detect this configuration, a 100kΩ pullup resistor must be connected between pin 52 and the supply line. To prevent false detection, TI recommends using pin 52 for output-only functions.
(6) This pin is shared by the ADC inputs and digital I/O pad cells.
(7) To use the digital functions, RTC_XTAL_N must be pulled high to the supply voltage using a 100kΩ resistor.
(8) Requires user configuration to enable the analog switch of the ADC channel (the switch is off by default.) The digital I/O is always connected and must be made Hi-Z before enabling the ADC switch.

Table 6-1. Pin Attributes

PIN NO.	SIGNAL NAME(1)	SIGNAL TYPE(2)	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS(3)	Hib(4)	nRESET = 0
1	GPIO10 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SCL		1	I/O (open drain)	Hi-Z, Pull, Drive		
	GT_PWM06		3	O	Hi-Z, Pull, Drive		
	UART1_TX		7	O	1		
	SDCARD_CLK		6	O	0		
	GT_CCP01		12	I	Hi-Z, Pull, Drive		
2	GPIO11 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SDA		1	I/O (open drain)	Hi-Z, Pull, Drive		
	GT_PWM07		3	O	Hi-Z, Pull, Drive		
	pXCLK(XVCLK)		4	O	0		
	SDCARD_CMD		6	I/O (open drain)	Hi-Z, Pull, Drive		
	UART1_RX		7	I	Hi-Z, Pull, Drive		
	GT_CCP02		12	I	Hi-Z, Pull, Drive		
	MCAFSX		13	O	Hi-Z, Pull, Drive		
3	GPIO12 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	McACLK		3	O	Hi-Z, Pull, Drive		
	pVS(VSYNC)		4	I	Hi-Z, Pull, Drive		
	I2C_SCL		5	I/O (open drain)	Hi-Z, Pull, Drive		
	UART0_TX		7	O	1		
	GT_CCP03		12	I	Hi-Z, Pull, Drive		

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Table 6-1. Pin Attributes (continued)

PIN NO.	SIGNAL NAME[1]	SIGNAL TYPE[2]	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS[3]	Hib[4]	nRESET = 0
4	GPIO13 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SDA		5	I/O (open drain)			
	pHS(HSYNC)		4	I			
	UART0_RX		7	I			
	GT_CCP04		12	I			
5	GPIO14 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SCL		5	I/O (open drain)			
	GSPI_CLK		7	I/O			
	pDATA8(CAM_D4)		4	I			
	GT_CCP05		12	I			
6	GPIO15 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SDA		5	I/O (open drain)			
	GSPI_MISO		7	I/O			
	pDATA9(CAM_D5)		4	I			
	GT_CCP06		13	I			
	SDCARD_ DATA0		8	I/O			
7	GPIO16 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GSPI_MOSI		7	I/O	Hi-Z, Pull, Drive		
	pDATA10(CAM_D6)		4	I	Hi-Z, Pull, Drive		
	UART1_TX		5	O	1		
	GT_CCP07		13	I	Hi-Z, Pull, Drive		
	SDCARD_CLK		8	O	0		
8	GPIO17 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART1_RX		5	I			
	GSPI_CS		7	I/O			
	pDATA11 (CAM_D7)		4	I			
	SDCARD_ CMD		8	I/O			
9	VDD_DIG1 (PN)	—	N/A	N/A	N/A	N/A	N/A
10	VIN_IO1	—	N/A	N/A	N/A	N/A	N/A
11	FLASH_SPI_CLK	O	N/A	O	Hi-Z, Pull, Drive[5]	Hi-Z, Pull, Drive	Hi-Z
12	FLASH_SPI_DOUT	O	N/A	O	Hi-Z, Pull, Drive[5]	Hi-Z, Pull, Drive	Hi-Z
13	FLASH_SPI_DIN	I	N/A	I	Hi-Z, Pull, Drive[5]	Hi-Z	Hi-Z
14	FLASH_SPI_CS	O	N/A	O	1	Hi-Z, Pull, Drive	Hi-Z
15	GPIO22 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	McAFSX		7	O			
	GT_CCP04		5	I			
16	TDI (PN)	I/O	1	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO23		0	I/O			
	UART1_TX		2	O	1		
	I2C_SCL		9	I/O (open drain)	Hi-Z, Pull, Drive		

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Table 6-1. Pin Attributes (continued)

PIN NO.	SIGNAL NAME[1]	SIGNAL TYPE[2]	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS[3]	Hib[4]	nRESET = 0
17	TDO (PN)	I/O	1	O	Hi-Z, Pull, Drive	Driven high in SWD; driven low in 4-wire JTAG	Hi-Z
	GPIO24		0	I/O			
	PWM0		5	O			
	UART1_RX		2	I			
	I2C_SDA		9	I/O (open drain)			
	GT_CCP06		4	I			
	McAFSX		6	O			
18	GPIO28 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
19	TCK (PN)	I/O	1	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GT_PWM03		8	O			
20	TMS (PN)	I/O	1	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO29		0	I/O			
21[6]	GPIO25	O	0	O	Hi-Z, Pull, Drive	Driven low	Hi-Z
	GT_PWM02		9	O	Hi-Z, Pull, Drive		
	McAFSX		2	O	Hi-Z, Pull, Drive		
	TCXO_EN		N/A	O	0		
	SOP2 (PN)		See [9]	I	Hi-Z, Pull, Drive		
22	WLAN_XTAL_N	—	N/A	N/A	N/A	N/A	N/A
23	WLAN_XTAL_P	—	N/A	N/A	N/A	N/A	N/A
24	VDD_PLL	—	N/A	N/A	N/A	N/A	N/A
25	LDO_IN2	—	N/A	N/A	N/A	N/A	N/A
26	NC	—	N/A	N/A	N/A	N/A	N/A
27	NC	—	N/A	N/A	N/A	N/A	N/A
28	NC	—	N/A	N/A	N/A	N/A	N/A
29[12]	ANTSEL1	O	0	O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
30[12]	ANTSEL2	O	0	O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
31	RF_BG	—	N/A	N/A	N/A	N/A	N/A
32	nRESET	—	N/A	N/A	N/A	N/A	N/A
33	VDD_PA_IN	—	N/A	N/A	N/A	N/A	N/A
34	SOP1	—	N/A	N/A	N/A	N/A	N/A
35	SOP0	—	N/A	N/A	N/A	N/A	N/A
36	LDO_IN1	—	N/A	N/A	N/A	N/A	N/A
37	VIN_DCDC_ANA	—	N/A	N/A	N/A	N/A	N/A
38	DCDC_ANA_SW	—	N/A	N/A	N/A	N/A	N/A
39	VIN_DCDC_PA	—	N/A	N/A	N/A	N/A	N/A
40	DCDC_PA_SW_P	—	N/A	N/A	N/A	N/A	N/A
41	DCDC_PA_SW_N	—	N/A	N/A	N/A	N/A	N/A
42	DCDC_PA_OUT	—	N/A	N/A	N/A	N/A	N/A
43	DCDC_DIG_SW	—	N/A	N/A	N/A	N/A	N/A
44	VIN_DCDC_DIG	—	N/A	N/A	N/A	N/A	N/A

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Table 6-1. Pin Attributes (continued)

PIN NO.	SIGNAL NAME[1]	SIGNAL TYPE[2]	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS[3]	Hib[4]	nRESET = 0
45[7]	GPIO31	I/O	0	I/O	Hi-Z	Hi-Z	Hi-Z
	UART0_RX		9	I			
	McAFSX		12	O			
	UART1_RX		2	I			
	McAXR0		6	I/O			
	GSPI_CLK		7	I/O			
	DCDC_ANA2_SW_P (PN)	—	See [8]	N/A	N/A	N/A	N/A
46	DCDC_ANA2_SW_N	—	N/A	N/A	N/A	N/A	N/A
47	VDD_ANA2	—	N/A	N/A	N/A	N/A	N/A
48	VDD_ANA1	—	N/A	N/A	N/A	N/A	N/A
49	VDD_RAM	—	N/A	N/A	N/A	N/A	N/A
50	GPIO0 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART0_CTS		12	I	Hi-Z, Pull, Drive		
	McAXR1		6	I/O	Hi-Z, Pull, Drive		
	GT_CCP00		7	I	Hi-Z, Pull, Drive		
	GSPI_CS		9	I/O	Hi-Z, Pull, Drive		
	UART1_RTS		10	O	1		
	UART0_RTS		3	O	1		
	McAXR0		4	I/O	Hi-Z, Pull, Drive		
51	RTC_XTAL_P	—	N/A	N/A	N/A	N/A	N/A
52[10]	RTC_XTAL_N (PN)	O	N/A	N/A	N/A	Hi-Z, Pull, Drive	Hi-Z
	GPIO32		0	O	Hi-Z, Pull, Drive		
	McACLK		2	O			
	McAXR0		4	O			
	UART0_RTS		6	O	1		
	GSPI_MOSI		8	O	Hi-Z, Pull, Drive		
53	GPIO30 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART0_TX		9	O	1		
	McACLK		2	O	Hi-Z, Pull, Drive		
	McAFSX		3	O			
	GT_CCP05		4	I			
	GSPI_MISO		7	I/O			
54	VIN_IO2	—	N/A	N/A	N/A	N/A	N/A
55	GPIO1 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART0_TX		3	O	1		
	pCLK (PIXCLK)		4	I	Hi-Z, Pull, Drive		
	UART1_TX		6	O	1		
	GT_CCP01		7	I	Hi-Z, Pull, Drive		
56	VDD_DIG2	—	N/A	N/A	N/A	N/A	N/A

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Table 6-1. Pin Attributes (continued)

PIN NO.	SIGNAL NAME[1]	SIGNAL TYPE[2]	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS[3]	Hib[4]	nRESET = 0
57[11]	ADC_CH0	Analog input (up to 1.5V) or digital I/O	See [8]	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO2 (PN)		0	I/O			
	UART0_RX		3	I			
	UART1_RX		6	I			
	GT_CCP02		7	I			
58[11]	ADC_CH1	Analog input (up to 1.5V) or digital I/O	See [8]	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO3 (PN)		0	I/O			
	UART1_TX		6	O	1		
	pDATA7 (CAM_D3)		4	I	Hi-Z, Pull, Drive		
59[11]	ADC_CH2	Analog input (up to 1.5V) or digital I/O	See [8]	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO4 (PN)		0	I/O			
	UART1_RX		6	I			
	pDATA6 (CAM_D2)		4	I			
60[11]	ADC_CH3	Analog input (up to 1.5V) or digital I/O	See [8]	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO5 (PN)		0	I/O			
	pDATA5 (CAM_D1)		4	I			
	McAXR1		6	I/O			
	GT_CCP05		7	I			
61	GPIO6 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART0_RTS		5	O	1		
	pDATA4 (CAM_D0)		4	I	Hi-Z, Pull, Drive		
	UART1_CTS		3	I			
	UART0_CTS		6	I			
	GT_CCP06		7	I			
62	GPIO7 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	McACLKX		13	O			
	UART1_RTS		3	O	1		
	UART0_RTS		10	O			
	UART0_TX		11	O			
63	GPIO8 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	SDCARD_IRQ		6	I			
	McAFSX		7	O			
	GT_CCP06		12	I			
64	GPIO9 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GT_PWM05		3	O			
	SDCARD_DATA0		6	I/O			
	McAXR0		7	I/O			
	GT_CCP00		12	I			
GND_TAB		—	N/A	N/A	N/A	N/A	N/A

(1) Signal names with (PN) denote the default pin name.
(2) Signal Types: I = Input, O = Output, I/O = Input or Output.
(3) LPDS state: Unused I/Os are in a Hi-Z state. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.
(4) Hibernate mode: The I/Os are in a Hi-Z state. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.

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(5) To minimize leakage in some serial flash vendors during LPDS, TI recommends that the user application always enables internal weak pulldown resistors on the FLASH_SPI_DIN, FLASH_SPI_DOUT, and FLASH_SPI_CLK pins.
(6) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.
(7) Pin 45 is used by an internal DC/DC (ANA2_DCDC). For the CC3230S device, pin 45 can be used as GPIO_31 if a supply is provided on pin 47.
(8) For details on proper use, see Section 6.5.
(9) This pin is one of three that must have a passive pullup or pulldown resistor onboard to configure the device hardware power-up mode. For this reason, the pin must be output only when used for digital functions.
(10) Pin 52 is used by the RTC crystal oscillator. These devices use automatic configuration sensing. Therefore, some board-level configuration is required to use pin 52 as a digital pad. Pin 52 is used for RTC crystal in most applications. However, in some applications a 32.768kHz square-wave clock might always be available onboard. When a 32.768kHz square-wave clock is available, the crystal can be removed to free pin 52 for digital functions. The external clock must then be applied at pin 51. For the chip to automatically detect this configuration, a 100kΩ pullup resistor must be connected between pin 52 and the supply line. To prevent false detection, TI recommends using pin 52 for output-only functions.
(11) This pin is shared by the ADC inputs and digital I/O pad cells.
(12) This pin is reserved for WLAN antenna selection, controlling an external RF switch that multiplexes the RF pin of the CC3230x device between two antennas. These pins must not be used for other functionalities.

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6.3 Signal Descriptions

Table 6-2. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
ADC	ADC_CH0	57	I/O	I	ADC channel 0 input (maximum of 1.5V)
	ADC_CH1	58	I/O	I	ADC channel 1 input (maximum of 1.5V)
	ADC_CH2	59	I/O	I	ADC channel 2 input (maximum of 1.5V)
	ADC_CH3	60	I	I	ADC channel 3 input (maximum of 1.5V)
Antenna selection	GPIO10	1	I/O	O	Antenna selection control
	GPIO11	2	I/O	O	
	GPIO12	3	I/O	O	
	GPIO13	4	I/O	O	
	GPIO14	5	I/O	O	
	GPIO15	6	I/O	O	
	GPIO16	7	I/O	O	
	GPIO17	8	I/O	O	
	GPIO22	15	I/O	O	
	GPIO28	18(2)	I/O	O	
	GPIO25	21	O	O	
	ANTSEL1	29	O	O	
	ANTSEL2	30	O	O	
	GPIO31	45(2) (1)	I/O	O	
	GPIO0	50	I/O	O	
	GPIO32	52(2)	I/O	O	
	GPIO30	53(2)	I/O	O	
	GPIO3	58	I/O	O	
	GPIO4	59	I/O	O	
	GPIO5	60	I/O	O	
	GPIO6	61	I/O	O	
	GPIO8	63	I/O	O	
	GPIO9	64	I/O	O	

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Table 6-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
BLE/2.4 GHz radio coexistence	GPIO10	1	I/O	I/O	Coexistence inputs and outputs
	GPIO11	2	I/O	O	
	GPIO12	3	I/O	I/O	
	GPIO13	4	I/O	I/O	
	GPIO14	5	I/O	I/O	
	GPIO15	6	I/O	I/O	
	GPIO16	7	I/O	I/O	
	GPIO17	8	I/O	O	
	GPIO22	15	I/O	I/O	
	GPIO28	18(2)	I/O	I/O	
	GPIO25	21	O	O	
	GPIO31	45(2) (1)	I/O	I/O	
	GPIO0	50	I/O	I/O	
	GPIO32	52(2)	I/O	I/O	
	GPIO30	53(2)	I/O	I/O	
	GPIO3	58	I/O	O	
	GPIO4	59	I/O	O	
	GPIO5	60	I/O	I/O	
	GPIO6	61	I/O	I/O	
	GPIO8	63	I/O	I/O	
	GPIO9	64	I/O	I/O	
Clock	WLAN_XTAL_N	22	—	—	40-MHz crystal; pull down if external TCXO is used
	WLAN_XTAL_P	23	—	—	40-MHz crystal or TCXO clock input
	RTC_XTAL_P	51	—	—	Connect 32.768-kHz crystal or force external CMOS level clock
	RTC_XTAL_N	52	—	—	Connect 32.768-kHz crystal or connect 100-kΩ resistor to supply voltage

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Table 6-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Hostless mode	HM_IO	1	I/O	I/O	Hostless mode inputs and outputs
		2	I/O	O	
		3	I/O	I/O	
		4	I/O	I/O	
		5	I/O	I/O	
		6	I/O	I/O	
		7	I/O	I/O	
		8	I/O	O	
		15	I/O	I/O	
		18[2]	I/O	I/O	
		21	O	O	
		45[2] [1]	I/O	I/O	
		50	I/O	I/O	
		52[2]	I/O	I/O	
		53[2]	I/O	I/O	
		58	O	O	
		59	O	O	
		60	I/O	I/O	
		61	I/O	I/O	
		63	I/O	I/O	
		64	I/O	I/O	
JTAG / SWD	TDI	16	I/O	I	JTAG TDI. Reset default pinout.
	TDO	17	I/O	O	JTAG TDO. Reset default pinout.
	TCK	19	I/O	I	JTAG/SWD TCK. Reset default pinout.
	TMS	20	I/O	I/O	JTAG/SWD TMS. Reset default pinout.
I^2C	I2C_SCL	1	I/O	I/O (open drain)	I^2C clock data
		3			
		5			
		16			
	I2C_SDA	2	I/O	I/O (open drain)	I^2C data
		4			
		6			
		17			

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Table 6-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Timers	GT_PWM06	1	I/O	O	Pulse-width modulated O/P
	GT_CCP01	1	I/O	I	Timer capture port
	GT_PWM07	2	I/O	O	Pulse-width modulated O/P
	GT_CCP02	2	I/O	I	Timer capture ports
	GT_CCP03	3	I/O	I	
	GT_CCP04	4	I/O	I	
		15	I/O	I	
	GT_CCP05	5	I/O	I	
	GT_CCP06	6	I/O	I	
		17	I/O	I	
		61	I/O	I	
		63	I/O	I	
	GT_CCP07	7	I/O	I	
	PWM0	17	I/O	O	Pulse-width modulated outputs
	GT_PWM03	19	I/O	O	
	GT_PWM02	21	O	O	
	GT_CCP00	50	I/O	I	Timer capture ports
		64	I/O	I	
	GT_CCP05	53	I/O	I	
	GT_CCP01	55	I/O	I	
	GT_CCP02	57	I/O	I	
	GT_CCP05	60	I	I	Timer capture port Input
	GT_PWM05	64	I/O	O	Pulse-width modulated output

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Table 6-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
GPIO	GPIO10	1	I/O	I/O	General-purpose inputs or outputs
	GPIO11	2	I/O	I/O	
	GPIO12	3	I/O	I/O	
	GPIO13	4	I/O	I/O	
	GPIO14	5	I/O	I/O	
	GPIO15	6	I/O	I/O	
	GPIO16	7	I/O	I/O	
	GPIO17	8	I/O	I/O	
	GPIO22	15	I/O	I/O	
	GPIO23	16	I/O	I/O	
	GPIO24	17	I/O	I/O	
	GPIO28	18	I/O	I/O	
	GPIO29	20	I/O	I/O	
	GPIO25	21	O	O	
	GPIO31	45[1]	I/O	I/O	
	GPIO0	50	I/O	I/O	
	GPIO32	52	I/O	O	
	GPIO30	53	I/O	I/O	
	GPIO1	55	I/O	I/O	
	GPIO2	57	I/O	I/O	
	GPIO3	58	I/O	I/O	
	GPIO4	59	I/O	I/O	
	GPIO5	60	I/O	I/O	
	GPIO6	61	I/O	I/O	
	GPIO7	62	I/O	I/O	
	GPIO8	63	I/O	I/O	
	GPIO9	64	I/O	I/O	

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Table 6-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
McASP I²S or PCM	MCAFSX	2	I/O	O	I²S audio port frame sync
		15			
		17			
		21			
		45(1)			
		53			
		63			
	McACLK	3	I/O	O	I²S audio port clock outputs
		52	O	O	
		53	I/O	O	
	McAXR1	50	I/O	I/O	I²S audio port data 1 (RX/TX)
		60	I	I/O	I²S audio port data 1 (RX and TX)
	McAXR0	45(1)	I/O	I/O	I²S audio port data 0 (RX and TX)
		50	I/O	I/O	
		52	O	O	I²S audio port data (only output mode is supported on pin 52)
		64	I/O	I/O	I²S audio port data (RX and TX)
	McACLKX	62	I/O	O	I²S audio port clock
Multimedia card (MMC or SD)	SDCARD_CLK	1	I/O	O	SD card clock data
		7			
	SDCARD_CMD	2	I/O	I/O (open drain)	SD card command line
		8	I/O	I/O	
	SDCARD_DATA0	6	I/O	I/O	SD card data
		64			
	SDCARD_IRQ	63	I/O	I	Interrupt from SD card(3)
Parallel interface (8-bit π)	pXCLK (XVCLK)	2	I/O	O	Free clock to parallel camera
	pVS (VSYNC)	3	I/O	I	Parallel camera vertical sync
	pHS (HSYNC)	4	I/O	I	Parallel camera horizontal sync
	pDATA8 (CAM_D4)	5	I/O	I	Parallel camera data bit 4
	pDATA9 (CAM_D5)	6	I/O	I	Parallel camera data bit 5
	pDATA10 (CAM_D6)	7	I/O	I	Parallel camera data bit 6
	pDATA11 (CAM_D7)	8	I/O	I	Parallel camera data bit 7
	pCLK (PIXCLK)	55	I/O	I	Pixel clock from parallel camera sensor
	pDATA7 (CAM_D3)	58	I/O	I	Parallel camera data bit 3
	pDATA6 (CAM_D2)	59	I/O	I	Parallel camera data bit 2
	pDATA5 (CAM_D1)	60	I	I	Parallel camera data bit 1
	pDATA4 (CAM_D0)	61	I/O	I	Parallel camera data bit 0

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Table 6-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Power	VDD_DIG1	9	—	—	Internal digital core voltage
	VIN_IO1	10	—	—	Device supply voltage (V_{BAT})
	VDD_PLL	24	—	—	Internal analog voltage
	LDO_IN2	25	—	—	Internal analog RF supply from analog DC/DC output
	VDD_PA_IN	33	—	—	Internal PA supply voltage from PA DC/DC output
	LDO_IN1	36	—	—	Internal analog RF supply from analog DC/DC output
	VIN_DCDC_ANA	37	—	—	Analog DC/DC input (connected to device input supply [V_{BAT}])
	DCDC_ANA_SW	38	—	—	Internal analog DC/DC switching node
	VIN_DCDC_PA	39	—	—	PA DC/DC input (connected to device input supply [V_{BAT}])
	DCDC_PA_SW_P	40	—	—	Internal PA DC/DC switching node
	DCDC_PA_SW_N	41	—	—	Internal PA DC/DC switching node
	DCDC_PA_OUT	42	—	—	Internal PA buck converter output
	DCDC_DIG_SW	43	—	—	Internal digital DC/DC switching node
	VIN_DCDC_DIG	44	—	—	Digital DC/DC input (connected to device input supply [V_{BAT}])
	DCDC_ANA2_SW_P	45(1)	—	—	Analog to DC/DC converter +ve switching node
	DCDC_ANA2_SW_N	46	—	—	Internal analog to DC/DC converter –ve switching node
	VDD_ANA2	47	—	—	Internal analog to DC/DC output
	VDD_ANA1	48	—	—	Internal analog supply fed by ANA2 DC/DC output
	VDD_RAM	49	—	—	Internal SRAM LDO output
	VIN_IO2	54	—	—	Device supply voltage (V_{BAT})
	VDD_DIG2	56	—	—	Internal digital core voltage
Reset	nRESET	32	I	I	Global master device reset (active low)
RF	RF_BG	31	I/O	I/O	WLAN analog RF 802.11 b/g/n bands
SPI	GSPI_CLK	5	I/O	I/O	General SPI clock
		45(1)	I/O	I/O	
	GSPI_MISO	6	I/O	I/O	General SPI MISO
		53	I/O	I/O	
	GSPI_CS	8	I/O	I/O	General SPI device select
		50	I/O	I/O	
	GSPI_MOSI	7	I/O	I/O	General SPI MOSI
		52	O	O	
FLASH SPI	FLASH_SPI_CLK	11	O	O	Clock to SPI serial flash (fixed default)
	FLASH_SPI_DOUT	12	O	O	Data to SPI serial flash (fixed default)
	FLASH_SPI_DIN	13	I	I	Data from SPI serial flash (fixed default)
	FLASH_SPI_CS	14	O	O	Device select to SPI serial flash (fixed default)

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Table 6-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
UART	UART1_TX	1	I/O	O	UART TX data
		7	I/O	O	
		16	I/O	O	
		55	I/O	O	
		58	I/O	O	UART1 TX data
	UART1_RX	2	I/O	I	UART RX data
		8	I/O	I	
		17	I/O	I	
		45(1)	I/O	I	
		57	I/O	I	UART1 RX data
		59	I/O	I	
	UART1_RTS	50	I/O	O	UART1 request-to-send (active low)
		62	I/O	O	
	UART1_CTS	61	I/O	I	UART1 clear-to-send (active low)
	UART0_TX	3	I/O	O	UART0 TX data
		53	I/O	O	
		55	I/O	O	
		62	I/O	O	
	UART0_RX	4	I/O	I	UART0 RX data
		45(1)	I/O	I	
		57	I/O	I	UART0 RX data
	UART0_CTS	50	I/O	I	UART0 clear-to-send input (active low)
		61			
	UART0_RTS	50	I/O	O	UART0 request-to-send (active low)
		52	O	O	
		61	I/O	O	
		62	I/O	O	
Sense-On-Power	SOP2	21(4)	O	I	Sense-on-power 2
	SOP1	34	I	I	Configuration sense-on-power 1
	SOP0	35	I	I	Configuration sense-on-power 0

(1) Pin 45 is used by an internal DC/DC (ANA2_DCDC). For the CC3230S device, pin 45 can be used as GPIO_31 if a supply is provided on pin 47.
(2) LPDS retention unavailable.
(3) Future support.
(4) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.

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6.4 Pin Multiplexing

Table 6-3. Pin Multiplexing

Register Address	Register Name	Pin	ANALOG OR SPECIAL FUNCTION				Digital Function (XXX Field Encoding)[1]												
			JTAG	Hostless Mode	BLE COEX		0	1	2	3	4	5	6	7	8	9	10	11	12	13
					CC_COEX_SW_OUT	CC_COEX_BLE_IN														
0x4402 E0C8	GPIO_PAD_CONFIG_10	1	—	Y	Y	Y	GPIO10	I2C_SCL	—	GT_PWM06	—	—	SDCARD_CLK	UART1_TX	—	—	—	—	GT_CCP01	—
0x4402 E0CC	GPIO_PAD_CONFIG_11	2	—	Y[5]	Y	—	GPIO11	I2C_SDA	—	GT_PWM07	pXCLK (XVCLK)	—	SDCARD_CMD	UART1_RX	—	—	—	—	GT_CCP02	MCAFSX
0x4402 E0D0	GPIO_PAD_CONFIG_12	3	—	Y	Y	Y	GPIO12	—	—	McACLK	pVS (VSYNC)	I2C_SCL	—	UART0_TX	—	—	—	—	GT_CCP03	—
0x4402 E0D4	GPIO_PAD_CONFIG_13	4	—	Y	Y	Y	GPIO13	—	—	—	pHS (HSYNC)	I2C_SDA	—	UART0_RX	—	—	—	—	GT_CCP04	—
0x4402 E0D8	GPIO_PAD_CONFIG_14	5	—	Y	Y	Y	GPIO14	—	—	—	pDATA8 (CAM_D4)	I2C_SCL	—	GSPI_CLK	—	—	—	—	GT_CCP05	—
0x4402 E0DC	GPIO_PAD_CONFIG_15	6	—	Y	Y	Y	GPIO15	—	—	—	pDATA9 (CAM_D5)	I2C_SDA	—	GSPI_MISO	SDCARD_DATA0	—	—	—	—	GT_CCP06
0x4402 E0E0	GPIO_PAD_CONFIG_16	7	—	Y	Y	Y	GPIO16	—	—	—	pDATA10 (CAM_D6)	UART1_TX	—	GSPI_MOSI	SDCARD_CLK	—	—	—	—	GT_CCP07
0x4402 E0E4	GPIO_PAD_CONFIG_17	8	—	Y[5]	Y	—	GPIO17	—	—	—	pDATA11 (CAM_D7)	UART1_RX	—	GSPI_CS	SDCARD_CMD	—	—	—	—	—
0x4402 E0F8	GPIO_PAD_CONFIG_22	15	—	Y	Y	Y	GPIO22	—	—	—	—	GT_CCP04	—	McAFSX	—	—	—	—	—	—
0x4402 E0FC	GPIO_PAD_CONFIG_23	16	Muxed with JTAG	—	—	—	GPIO23	TDI	UART1_TX	—	—	—	—	—	—	I2C_SCL	—	—	—	—
0x4402 E100	GPIO_PAD_CONFIG_24	17	Muxed with JTAG TDO	—	—	—	GPIO24	TDO	UART1_RX	—	GT_CCP06	PWM0	McAFSX	—	—	I2C_SDA	—	—	—	—
0x4402 E140	GPIO_PAD_CONFIG_40	18	—	Y[4]	Y[4]	Y[4]	GPIO28	—	—	—	—	—	—	—	—	—	—	—	—	—
0x4402 E110	GPIO_PAD_CONFIG_28	19	Muxed with JTAG or SWD and TCK	—	—	—	—	TCK	—	—	—	—	—	—	GT_PWM03	—	—	—	—	—
0x4402 E114	GPIO_PAD_CONFIG_29	20	Muxed with JTAG or SWD and TMSC	—	—	—	GPIO29	TMS	—	—	—	—	—	—	—	—	—	—	—	—
0x4402 E104	GPIO_PAD_CONFIG_25	21[2]	—	Y[5]	Y	—	GPIO25	—	McAFSX	—	—	—	—	—	—	GT_PWM02	—	—	—	—
0x4402 E108	GPIO_PAD_CONFIG_26	29	—	—	—	—	ANTSEL 1[3]	—	—	—	—	—	—	—	—	—	—	—	—	—

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Table 6-3. Pin Multiplexing (continued)

Register Address	Register Name	Pin	ANALOG OR SPECIAL FUNCTION				Digital Function (XXX Field Encoding)[1]												
			JTAG	Hostless Mode	BLE COEX		0	1	2	3	4	5	6	7	8	9	10	11	12	13
					CC_COEX_SW_OUT	CC_COEX_BLE_IN														
0x4402 E10C	GPIO_PAD_CONFIG_27	30	—	—	—	—	ANTSEL2[3]	—	—	—	—	—	—	—	—	—	—	—	—	—
0x4402 E11C	GPIO_PAD_CONFIG_31	45[4] [3]	—	Y	Y	Y	GPIO31	—	UART1_RX	—	—	—	McAXR0	GSPI_CLK	—	UART0_RX	—	—	McAFSX	—
0x4402 E0A0	GPIO_PAD_CONFIG_0	50	—	Y	Y	Y	GPIO0	—	—	UART0_RTS	McAXR0	—	McAXR1	GT_CCP00	—	GSPI_CS	UART1_RTS	—	UART0_CTS	—
0x4402 E120	GPIO_PAD_CONFIG_32	52	—	Y[4]	Y[4]	Y[4]	GPIO32	—	McACLK	—	McAXR0	—	UART0_RTS	—	GSPI_MOSI	—	—	—	—	—
0x4402 E118	GPIO_PAD_CONFIG_30	53	—	Y[4]	Y[4]	Y[4]	GPIO30	—	McACLK	McAFSX	GT_CCP05	—	—	GSPI_MISO	—	UART0_TX	—	—	—	—
0x4402 E0A4	GPIO_PAD_CONFIG_1	55	—	—	—	—	GPIO1	—	—	UART0_TX	pCLK (PIXCLK)	—	UART1_TX	GT_CCP01	—	—	—	—	—	—
0x4402 E0A8	GPIO_PAD_CONFIG_2	57	—	—	—	—	GPIO2	—	—	UART0_RX	—	—	UART1_RX	GT_CCP02	—	—	—	—	—	—
0x4402 E0AC	GPIO_PAD_CONFIG_3	58	—	Y[5]	Y	—	GPIO3	—	—	—	pDATA7 (CAM_D3)	—	UART1_TX	—	—	—	—	—	—	—
0x4402 E0B0	GPIO_PAD_CONFIG_4	59	—	Y[5]	Y	—	GPIO4	—	—	—	pDATA6 (CAM_D2)	—	UART1_RX	—	—	—	—	—	—	—
0x4402 E0B4	GPIO_PAD_CONFIG_5	60	—	Y	Y	Y	GPIO5	—	—	—	pDATA5 (CAM_D1)	—	McAXR1	GT_CCP05	—	—	—	—	—	—
0x4402 E0B8	GPIO_PAD_CONFIG_6	61	—	Y	Y	Y	GPIO6	—	—	UART1_CTS	pDATA4 (CAM_D0)	UART0_RTS	UART0_CTS	GT_CCP06	—	—	—	—	—	—
0x4402 E0BC	GPIO_PAD_CONFIG_7	62	—	—	—	—	GPIO7	—	—	UART1_RTS	—	—	—	—	—	—	UART0_RTS	UART0_TX	—	McACLKX
0x4402 E0C0	GPIO_PAD_CONFIG_8	63	—	Y	Y	Y	GPIO8	—	—	—	—	—	SDCARD_IRQ	McAFSX	—	—	—	—	GT_CCP06	—
0x4402 E0C4	GPIO_PAD_CONFIG_9	64	—	Y	Y	Y	GPIO9	—	—	GT_PWM05	—	—	SDCARD_DATA0	McAXR0	—	—	—	—	GT_CCP00	—

(1) Pin mux encodings with (RD) denote the default encoding after reset release.
(2) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.
(3) Pin 45 is used by an internal DC/DC (ANA2_DCDC). For the CC3230S device, pin 45 can be used as GPIO_31 if a supply is provided on pin 47.
(4) LPDS retention unavailable.
(5) Output Only

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6.5 Drive Strength and Reset States for Analog and Digital Multiplexed Pins

Table 6-4 describes the use, drive strength, and default state of analog and digital multiplexed pins at first-time power up and reset (nRESET pulled low).

Table 6-4. Drive Strength and Reset States for Analog and Digital Multiplexed Pins

Pin	Board-Level Configuration and Use	Default State at First Power Up or Forced Reset	State After Configuration of Analog Switches (ACTIVE, LPDS, and HIB Power Modes)	Maximum Effective Drive Strength (mA)
29	Connected to the enable pin of the RF switch (ANTSEL1). Other use is not recommended.	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os	4
30	Connected to the enable pin of the RF switch (ANTSEL2). Other use is not recommended.	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os	4
45	VDD_ANA2 (pin 47) must be shorted to the input supply rail. Otherwise, the pin is driven by the ANA2 DC/DC.	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os	4
50	Generic I/O	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os	4
52	The pin must have an external pullup of 100kΩ to the supply rail and must be used in output signals only.	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os	4
53	Generic I/O	Analog is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os	4
57	Analog signal (1.8V absolute, 1.46V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os	4
58	Analog signal (1.8V absolute, 1.46V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os	4
59	Analog signal (1.8-V absolute, 1.46-V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os	4
60	Analog signal (1.8-V absolute, 1.46-V full scale)	ADC is isolated. The digital I/O cell is also isolated.	Determined by the I/O state, as are other digital I/Os	4

6.6 Pad State After Application of Power to Device, Before Reset Release

When a stable power is applied to the CC3230x device for the first time or when the supply voltage is restored to the proper value following a period with a supply voltage less than 1.5V, the level of each digital pad is undefined in the period starting from the release of nRESET and until DIG_DCDC powers up. This period is less than approximately 10ms. During this period, pads can be internally pulled weakly in either direction. If a certain set of pins is required to have a definite value during this pre-reset period, an appropriate pullup or pulldown resistor must be used at the board level. The recommended value of this external pull is 2.7kΩ.

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6.7 Connections for Unused Pins

All unused pin should be configured as stated in Table 6-5.

Table 6-5. Connections for Unused Pins

FUNCTION	SIGNAL DESCRIPTION	PIN NUMBER	ACCEPTABLE PRACTICE	PREFERRED PRACTICE
GPIO	General-purpose input or output		Wake up I/O source should not be floating during Hibernate. All the I/O pins will float while in Hibernate and Reset states. Ensure pullup and pulldown resistors are available on board to maintain the state of the I/O. Leave unused GPIOs as NC	
No Connect	NC	26, 27, 28	Unused pin, leave as NC.	Unused pin, leave as NC.
SOP	Configuration sense-on-power		Ensure pulldown resistors are available on unused SOP pins	100kΩ pulldown resistor on SOP0 and SOP1. 2.7kΩ pull down on SOP2
Reset	RESET input for the device		Never leave the reset pin floating	
Clock	RTC_XTAL_N		When using an external oscillator, add a 100kΩ pullup resistor to VIO	
	WLAN_XTAL_N		When using an external oscillator, connect to ground if unused	
JTAG	JTAG interface		Leave as NC if unused.	

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7 Specifications

All measurements are referenced at the device pins, unless otherwise indicated. All specifications are over process and voltage, unless otherwise indicated.

7.1 Absolute Maximum Ratings

All measurements are referenced at the device pins unless otherwise indicated. All specifications are over process and overvoltage unless otherwise indicated.
Over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
Supply voltage	V_{BAT} and V_{IO}	Pins: 37, 39, 44	–0.5	3.8	V
	V_{IO} – V_{BAT} (differential)	Pins: 10, 54	V_{BAT} and V_{IO} should be tied together		V
Digital inputs			–0.5	V_{IO} + 0.5	V
RF pins			–0.5	2.1	V
Analog pins, Crystal		Pins: 22, 23, 51, 52	–0.5	2.1	V
Operating temperature, T_A			–40	85	°C
Storage temperature, T_{stg}			–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.3 Power-On Hours (POH)

This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

OPERATING CONDITION	POWER-ON HOURS [POH] (hours)
T_A up to 85°C(1)	87,600

(1) The TX duty cycle (power amplifier ON time) is assumed to be 10% of the device POH. Of the remaining 90% of the time, the device can be in any other state.

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7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2)

				MIN	TYP	MAX	UNIT
Supply voltage	V_{BAT}, V_{IO} (shorted to V_{BAT})	Pins: 10, 37, 39, 44, 54	Direct battery connection(3)	2.1(4)	3.3	3.6	V
Ambient thermal slew				–20		20	°C/minute

(1) Operating temperature is limited by crystal frequency variation.
(2) When operating at an ambient temperature of over 75°C, the transmit duty cycle must remain below 50% to avoid the auto-protect feature of the power amplifier. If the auto-protect feature triggers, the device takes a maximum of 60 seconds to restart the transmission.
(3) To ensure WLAN performance, the ripple on the supply must be less than ±300mV.
(4) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. The brownout condition is also 2.1V, and care must be taken when operating at the minimum specified voltage.

7.5 Current Consumption Summary (CC3230S)

Table 7-1. Current Consumption Summary (CC3230S)

T_A = 25°C, V_{BAT} = 3.6 V

PARAMETER		TEST CONDITIONS(1) (5)			MIN	TYP(6)	MAX	UNIT
MCU ACTIVE	NWP ACTIVE	TX	1 DSSS	TX power level = 0		272		mA
				TX power level = 4		190		
			6 OFDM	TX power level = 0		248		
				TX power level = 4		182		
			54 OFDM	TX power level = 0		223		
				TX power level = 4		160		
		RX	1 DSSS			59		
			54 OFDM			59		
	NWP idle connected(3)					15.3		
MCU SLEEP	NWP ACTIVE	TX	1 DSSS	TX power level = 0		269		mA
				TX power level = 4		187		
			6 OFDM	TX power level = 0		245		
				TX power level = 4		179		
			54 OFDM	TX power level = 0		220		
				TX power level = 4		157		
		RX	1 DSSS			56		
			54 OFDM			56		
	NWP idle connected(3)					12.2		
MCU LPDS	NWP ACTIVE	TX	1 DSSS	TX power level = 0		266		mA
				TX power level = 4		184		
			6 OFDM	TX power level = 0		242		
				TX power level = 4		176		
			54 OFDM	TX power level = 0		217		
				TX power level = 4		154		
		RX	1 DSSS			53		
			54 OFDM			53		
	NWP LPDS(2)		120 µA at 64KB 135 µA at 256KB			135		µA
	NWP idle connected(3)					710		

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Table 7-1. Current Consumption Summary (CC3230S) (continued)

T_A = 25°C, V_{BAT} = 3.6 V

PARAMETER		TEST CONDITIONS(1) (5)		MIN	TYP(6)	MAX	UNIT
MCU SHUTDOWN	MCU shutdown				1		µA
MCU HIBERNATE	MCU hibernate				4.5		µA
Peak calibration current(4)		V_{BAT} = 3.6 V			420		mA
		V_{BAT} = 3.3 V			450		
		V_{BAT} = 2.1 V			670		

(1) TX power level = 0 implies maximum power (see Figure 7-1, Figure 7-2, and Figure 7-3). TX power level = 4 implies output power backed off approximately 4 dB.
(2) LPDS current does not include the external serial flash. The LPDS number of reported is with retention of 256KB of MCU SRAM. The CC3230x device can be configured to retain 0KB, 64KB, 128KB, 192KB, or 256KB of SRAM in LPDS. Each 64-KB block of MCU retained SRAM increases LPDS current by 4 µA.
(3) DTIM = 1
(4) The complete calibration can take up to 17 mJ of energy from the battery over a time of 24 ms. In default mode, calibration is performed sparingly, and typically occurs when re-enabling the NWP and when the temperature has changed by more than 20°C. There are two additional calibration modes that may be used to reduced or completely eliminate the calibration event. For further details, see *CC31xx, CC32xx SimpleLink™ Wi-Fi® and IoT Network Processor Programmer's Guide*.
(5) The CC3230x system is a constant power-source system. The active current numbers scale based on the V_{BAT} voltage supplied.
(6) Typical numbers assume a VSWR of 1.5:1.

7.6 Current Consumption Summary (CC3230SF)

Table 7-2. Current Consumption Summary (CC3230SF)

T_A = 25°C, V_{BAT} = 3.6V

PARAMETER		TEST CONDITIONS(1) (5)			MIN	TYP(5)	MAX	UNIT
MCU ACTIVE	NWP ACTIVE	TX	1 DSSS	TX power level = 0		286		mA
				TX power level = 4		202		
			6 OFDM	TX power level = 0		255		
				TX power level = 4		192		
			54 OFDM	TX power level = 0		232		
				TX power level = 4		174		
		RX	1 DSSS			74		
			54 OFDM			74		
	NWP idle connected(3)					25.2		
MCU SLEEP	NWP ACTIVE	TX	1 DSSS	TX power level = 0		282		mA
				TX power level = 4		198		
			6 OFDM	TX power level = 0		251		
				TX power level = 4		188		
			54 OFDM	TX power level = 0		228		
				TX power level = 4		170		
		RX	1 DSSS			70		
			54 OFDM			70		
	NWP idle connected(3)					21.2		

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Table 7-2. Current Consumption Summary (CC3230SF) (continued)

T_A = 25°C, V_{BAT} = 3.6V

PARAMETER		TEST CONDITIONS(1) (5)			MIN	TYP(5)	MAX	UNIT
MCU LPDS	NWP active	TX	1 DSSS	TX power level = 0		266		mA
				TX power level = 4		184		
			6 OFDM	TX power level = 0		242		
				TX power level = 4		176		
			54 OFDM	TX power level = 0		217		
				TX power level = 4		154		
		RX	1 DSSS			53		
			54 OFDM			53		
	NWP LPDS(2)		120 µA at 64KB 135 µA at 256KB			135		µA
	NWP idle connected(3)					710		
MCU SHUTDOWN	MCU shutdown					1		µA
MCU HIBERNATE	MCU hibernate					4.5		µA
Peak calibration current(4)		V_{BAT} = 3.6 V				420		mA
		V_{BAT} = 3.3 V				450		
		V_{BAT} = 2.1 V				670		

(1) TX power level = 0 implies maximum power (see Figure 7-1, Figure 7-2, and Figure 7-3). TX power level = 4 implies output power backed off approximately 4dB.
(2) LPDS current does not include the external serial flash. The LPDS number of reported is with a retention of 256KB of MCU SRAM. The CC3230x device can be configured to retain 0KB, 64KB, 128KB, 192KB, or 256KB of SRAM in LPDS. Each 64-KB block of MCU retained SRAM increases LPDS current by 4µA.
(3) DTIM = 1
(4) The complete calibration can take up to 17 mJ of energy from the battery over a period of 24 ms. Calibration is performed sparingly, typically when coming out of HIBERNATE and only if the temperature has changed by more than 20°C. The calibration event can be controlled by a configuration file in the serial flash.
(5) Typical numbers assume a VSWR of 1.5:1.

7.7 TX Power Control

The CC3230x has several options for modifying the output power of the device when required. It is possible to lower the overall output power at a global level using the global TX power level setting. In addition, the 2.4GHz band allows the user to enter additional back-offs [1], per channel, region [2]and modulation rates [3], and through Image creator (see the *UniFlash CC3x20, CC3x35 SimpleLink™ Wi-Fi® and Internet-on-a chip™ Solution ImageCreator and Programming Tool User's Guide* for more details).

Figure 7-1, Figure 7-2, and Figure 7-3 show TX power and IBAT versus TX power level settings for the CC3230S device at modulations of 1 DSSS, 6 OFDM, and 54 OFDM, respectively. For the CC3230SF device, the IBAT current has an increase of approximately 10mA to 15mA depending on the transmitted rate. The TX power level will remain the same.

[1] The back-off range is between -6dB to +6dB in 0.25dB increments.
[2] FCC/ISED, ETSI (Europe), and Japan are supported.
[3] Back-off rates are grouped into 11b rates, high modulation rates (MCS7, 54 OFDM and 48 OFDM), and lower modulation rates (all other rates).

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In Figure 7-1, the area enclosed in the circle represents a significant reduction in current during the transition from TX power level 3 to level 4. In the case of lower range requirements (14dBm output power), TI recommends using TX power level 4 to reduce the current.

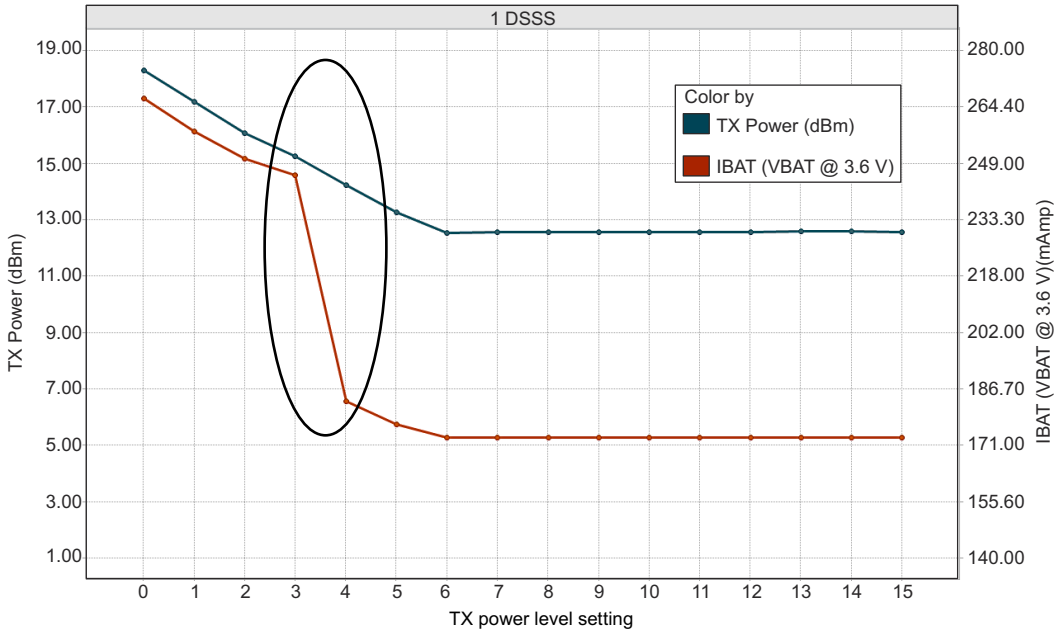

Figure 7-1. TX Power and IBAT vs TX Power Level Settings (1 DSSS)

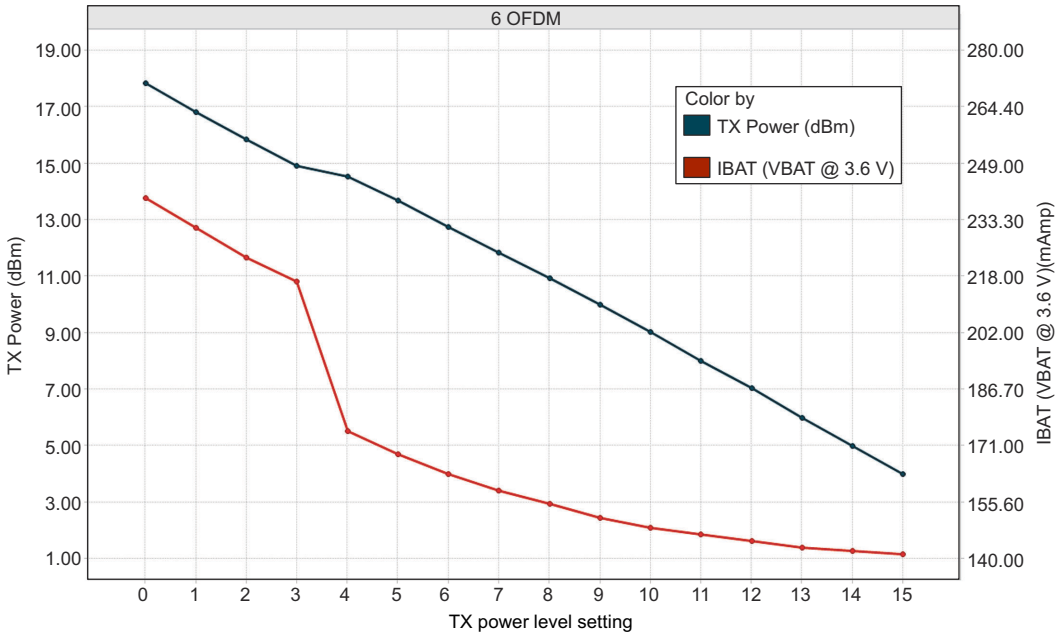

Figure 7-2. TX Power and IBAT vs TX Power Level Settings (6 OFDM)

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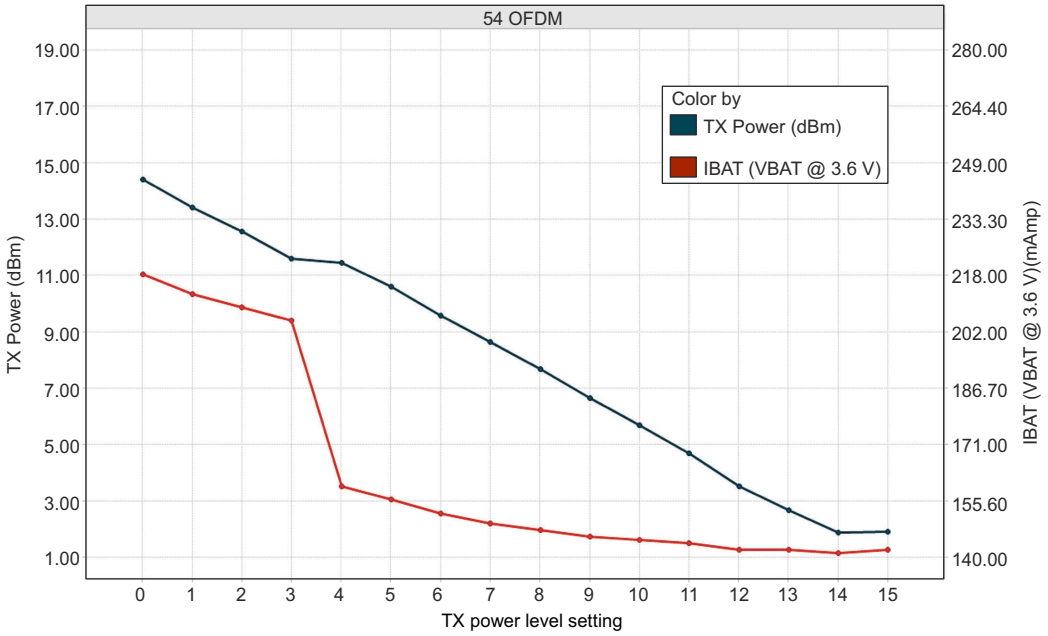

Figure 7-3. TX Power and IBAT vs TX Power Level Settings (54 OFDM)

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7.8 Brownout and Blackout Conditions

The device enters a brownout condition when the input voltage drops below $V_{brownout}$ (see Figure 7-4 and Figure 7-5). This condition must be considered during design of the power supply routing, especially when operating from a battery. High-current operations, such as a TX packet or any external activity (not necessarily related directly to networking) can cause a drop in the supply voltage, potentially triggering a brownout condition. The resistance includes the internal resistance of the battery, the contact resistance of the battery holder (four contacts for 2× AA batteries), and the wiring and PCB routing resistance.

Note

When the device is in HIBERNATE state, brownout is not detected. Only blackout is in effect during HIBERNATE state.

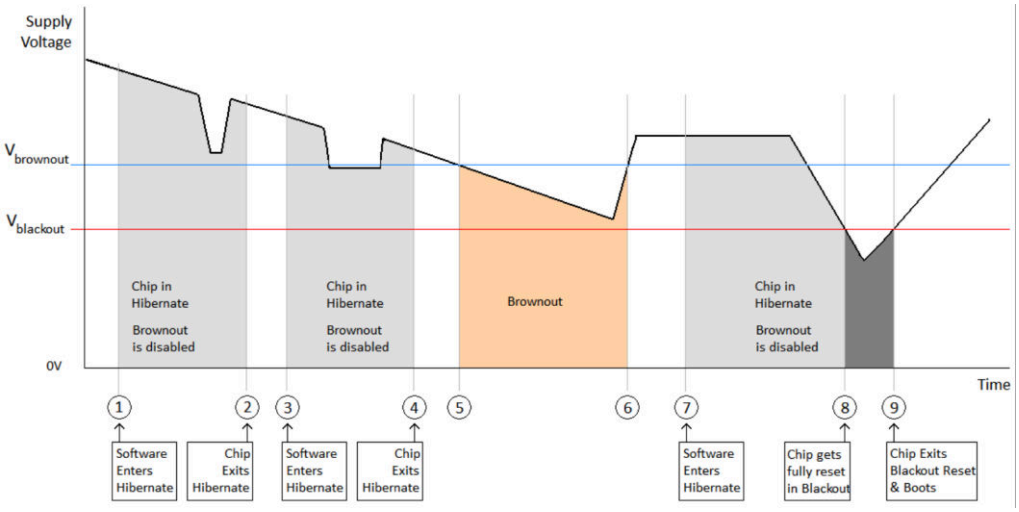

Figure 7-4. Brownout and Blackout Levels (1 of 2)

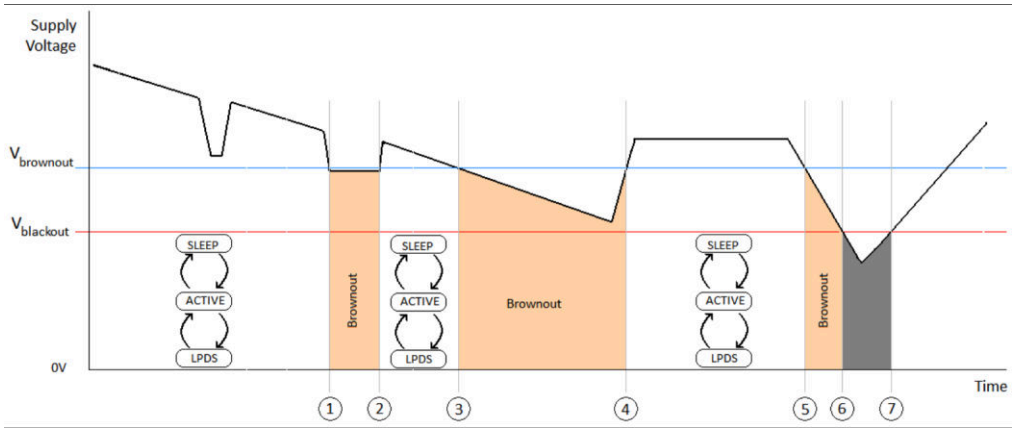

Figure 7-5. Brownout and Blackout Levels (2 of 2)

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In the brownout condition, all sections of the device (including the 32-kHz RTC) shut down except for the Hibernate module, which remains on. The current in this state can reach approximately 400 µA. The blackout condition is equivalent to a hardware reset event in which all states within the device are lost.

Table 7-3 lists the brownout and blackout voltage levels.

Table 7-3. Brownout and Blackout Voltage Levels

CONDITION	VOLTAGE LEVEL	UNIT
$V_{brownout}$	2.1	V
$V_{blackout}$	1.67	V

7.9 Electrical Characteristics for GPIO Pins

7.9.1 Electrical Characteristics: GPIO Pins Except 29, 30, 50, 52, and 53

T_A = 25°C, V_{BAT} = 2.1V to 3.3V(1)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Pin capacitance				4		pF
V_{IH}	High-level input voltage			0.65 × V_{DD}		V_{DD} + 0.5V	V
V_{IL}	Low-level input voltage			–0.5		0.35 × V_{DD}	V
I_{IH}	High-level input current				5		nA
I_{IL}	Low-level input current				5		nA
V_{OH}	High-level output voltage		IL = 2mA; configured I/O drive strength = 2mA; 2.4V ≤ V_{DD} < 3.6V			V_{DD} × 0.8	V
			IL = 4mA; configured I/O drive strength = 4mA; 2.4V ≤ V_{DD} < 3.6V			V_{DD} × 0.7	
			IL = 6mA; configured I/O drive strength = 6mA; 2.4V ≤ V_{DD} < 3.6V			V_{DD} × 0.7	
			IL = 2mA; configured I/O drive strength = 2mA; 2.1V ≤ V_{DD} < 2.4V			V_{DD} × 0.75	
V_{OL}	Low-level output voltage		IL = 2mA; configured I/O drive strength = 2mA; 2.4V ≤ V_{DD} < 3.6V	V_{DD} × 0.2			V
			IL = 4mA; configured I/O drive strength = 4mA; 2.4V ≤ V_{DD} < 3.6V	V_{DD} × 0.2			
			IL = 6mA; configured I/O drive strength = 6mA; 2.4V ≤ V_{DD} < 3.6V	V_{DD} × 0.2			
			IL = 2mA; configured I/O drive strength = 2mA; 2.1V ≤ V_{DD} < 2.4V	V_{DD} × 0.25			
I_{OH}	High-level source current	2mA drive		2			mA
		4mA drive		4			
		6mA drive		6			
I_{OL}	Low-level sink current	2mA drive		2			mA
		4mA drive		4			
		6mA drive		6			

(1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and reduces any potential degradation of RF sensitivity and performance. The default drive strength setting is 6mA.

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7.9.2 Electrical Characteristics: GPIO Pins 29, 30, 50, 52, and 53

T_A = 25°C, V_{BAT} = 2.1V to 3.6V.(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Pin capacitance				7		pF
V_{IH}	High-level input voltage			0.65 × V_{DD}		V_{DD} + 0.5V	V
V_{IL}	Low-level input voltage			–0.5		0.35 × V_{DD}	V
I_{IH}	High-level input current				50		nA
I_{IL}	Low-level input current				50		nA
V_{OH}	High-level output voltage		IL = 2mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6V			V_{DD} × 0.8	V
			IL = 4mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6V			V_{DD} × 0.7	
			IL = 6mA; configured I/O drive strength = 6 mA; 2.4 V ≤ V_{DD} < 3.6V			V_{DD} × 0.7	
			IL = 2mA; configured I/O drive strength = 2 mA; 2.1 V ≤ V_{DD} < 2.4V			V_{DD} × 0.75	
V_{OL}	Low-level output voltage		IL = 2mA; configured I/O drive strength = 2 mA; 2.4 V ≤ V_{DD} < 3.6V	V_{DD} × 0.2			V
			IL = 4mA; configured I/O drive strength = 4 mA; 2.4 V ≤ V_{DD} < 3.6V	V_{DD} × 0.2			
			IL = 6mA; configured I/O drive strength = 6 mA; 2.4 V ≤ V_{DD} < 3.6V	V_{DD} × 0.2			
			IL = 2mA; configured I/O drive strength = 2 mA; 2.1 V ≤ V_{DD} < 2.4V	V_{DD} × 0.25			
I_{OH}	High-level source current, V_{OH} = 2.4	2mA drive		1.5			mA
		4mA drive		2.5			
		6mA drive		3.5			
I_{OL}	Low-level sink current	2mA drive		1.5			mA
		4mA drive		2.5			
		6mA drive		3.5			
V_{IL}	nRESET				0.6		V

(1) TI recommends using the lowest possible drive strength that is adequate for the applications. This recommendation minimizes the risk of interference to the WLAN radio and reduces any potential degradation of RF sensitivity and performance. The default drive strength setting is 6mA.

7.10 Electrical Characteristics for Pin Internal Pullup and Pulldown

Table 7-4. Electrical Characteristics for Pin Internal Pullup and Pulldown

T_A = 25°C, V_{BAT} = 3.0V

I_{OH}	Pullup current, V_{OH} = 2.4 (V_{DD} = 3.0V)		5	10	µA
I_{OL}	Pulldown current, V_{OL} = 0.4 (V_{DD} = 3.0V)		5		µA

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7.11 WLAN Receiver Characteristics

Table 7-5. WLAN Receiver Characteristics

T_A = 25°C, V_{BAT} = 2.1 V to 3.6 V. Parameters are measured at the SoC pin on channel 6 (2437 MHz).

PARAMETER	TEST CONDITIONS (Mbps)	MIN	TYP	MAX	UNIT
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates)(2)	1 DSSS		–96.0		dBm
	2 DSSS		–94.0		
	11 CCK		–88.0		
	6 OFDM		–90.5		
	9 OFDM		–90.0		
	18 OFDM		–86.5		
	36 OFDM		–80.5		
	54 OFDM		–74.5		
	MCS7 (GF)(1)		–71.5		
Maximum input level (10% PER)	802.11b		–4.0		dBm
	802.11g		–10.0		

(1) Sensitivity for mixed mode is 1-dB worse.
(2) Sensitivity is 1-dB worse on channel 13 (2472 MHz).

7.12 WLAN Transmitter Characteristics

Table 7-6. WLAN Transmitter Characteristics

T_A = 25°C, V_{BAT} = 2.1 V to 3.6 V. Parameters measured at SoC pin on channel 6 (2437 MHz).(1) (2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating frequency range(3) (4)		2412		2472	MHz
Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM	1 DSSS		18.0		dBm
	2 DSSS		18.0		
	11 CCK		18.3		
	6 OFDM		17.3		
	9 OFDM		17.3		
	18 OFDM		17.0		
	36 OFDM		16.0		
	54 OFDM		14.5		
	MCS7		13.0		
Transmit center frequency accuracy		–25		25	ppm

(1) The OFDM and MCS7 edge channels (2412 and 2462 MHz) have reduced TX power to meet FCC emission limits.
(2) Power of 802.11b rates are reduced to meet ETSI requirements in Europe.
(3) Channels 1 (2142 MHz) through 11 (2462 MHz) are supported for FCC.
(4) Channels 1 (2142 MHz) through 13 (2472MHz) are supported for Europe and Japan. Note that channel 14 is not supported for Japan.

7.13 WLAN Transmitter Out-of-Band Emissions

The device requires an external band-pass filter to meet the various emission standards, including FCC. Section 7.13.1 presents the minimum attenuation requirements for the band-pass filter. TI recommends using the same filter used in the reference design to ease the process of certification.

7.13.1 WLAN Filter Requirements

PARAMETER	FREQUENCY (MHz)	MIN	TYP	MAX	UNIT
Return loss	2412 to 2484	10			dB
Insertion loss(1)	2412 to 2484		1	1.5	dB

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PARAMETER	FREQUENCY (MHz)	MIN	TYP	MAX	UNIT
Attenuation	804 to 828	30	42		dB
	1608 to 1656	20	23		
	3216 to 3312	30	49		
	4020 to 4140	40	52		
	4824 to 4968	20	30		
	5628 to 5796	20	27		
	6432 to 6624	20	42		
	7200 to 7500	35	44		
	7500 to 10000	20	30		
Reference impendence	2412 to 2484		50		Ω
Filter type	Bandpass				

(1) Insertion loss directly impacts output power and sensitivity. At customer discretion, insertion loss can be relaxed to meet attenuation requirements.

7.14 BLE/2.4 GHz Radio Coexistence and WLAN Coexistence Requirements

For proper BLE/2.4 GHz radio coexistence, the following requirements needs to met:

Table 7-7. COEX Isolation Requirement

PARAMETER	Band	MIN	TYP	MAX	UNIT
Port-to-port isolation	Single antenna	20(1)			dB
	Dual antenna Configuration	20(2)			

(1) WLAN/BLE switch used must provide a minimum of 20 dB isolation between ports.
(2) For dual antenna configuration antenna placement must be such that isolation between the BLE and WLAN ports is at least 20 dB.

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7.15 Thermal Resistance Characteristics for RGK Package

THERMAL METRICS[1]		°C/W[2] [3]	AIR FLOW (m/s)[4]
$R\Theta_{JC}$	Junction-to-case	6.3	0.0051
$R\Theta_{JB}$	Junction-to-board	2.4	0.0051
$R\Theta_{JA}$	Junction-to-free air	23	0.0051
$R\Theta_{JMA}$	Junction-to-moving air	14.6	0.765
		12.4	1.275
		10.8	2.55
Psi_{JT}	Junction-to-package top	0.2	0.0051
		0.2	0.765
		0.3	1.275
		0.1	2.55
Psi_{JB}	Junction-to-board	2.3	0.0051
		2.3	0.765
		2.2	1.275
		2.4	2.55

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.
(3) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 2 W and an ambient temperature of 70°C is assumed.
(4) m/s = meters per second.

7.16 Timing and Switching Characteristics

7.16.1 Power Supply Sequencing

For proper operation of the CC3230x device, perform the recommended power-up sequencing as follows:

1. Tie the following pins together on the board:
   - V_{BAT} (pins 37, 39, and 44)
   - V_{IO} (pins 54 and 10)
2. Hold the RESET pin low while the supplies are ramping up. TI recommends using a simple RC circuit (100 K ||, 0.01 µF, RC = 1 ms).
3. For an external RTC, ensure that the clock is stable before RESET is deasserted (high).

For timing diagrams, see Section 7.16.3.

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7.16.2 Device Reset

When a device restart is required, the user may issue a negative pulse to the nRESET pin. The user must follow one of the following alternatives to ensure the reset is properly applied:

- A negative reset pulse (on pin 32) of at least 200-ms duration
- If the 200-ms pulse duration cannot be ensured, a pulldown resistor of 2 MΩ must be connected to pin 52 (RTC_XTAL_N). If implemented, a shorter pulse of at least 100 µs can be used.

To ensure a proper reset sequence, the user must call the sl_stop function prior to toggling the reset. When a reset is required, it is preferable to use the software reset instead of an external trigger.

7.16.3 Reset Timing

7.16.3.1 nRESET (32-kHz Crystal)

Figure 7-6 shows the reset timing diagram for the 32-kHz crystal first-time power-up and reset removal.

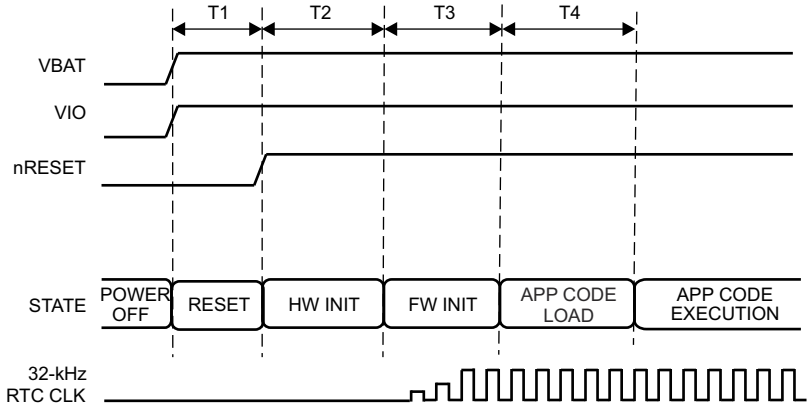

Figure 7-6. First-Time Power-Up and Reset Removal Timing Diagram (32-kHz Crystal)

Section 7.16.3.2 describes the timing requirements for the 32-kHz clock crystal first-time power-up and reset removal.

7.16.3.2 First-Time Power-Up and Reset Removal Timing Requirements (32-kHz Crystal)

ITEM	NAME	DESCRIPTION	MIN	NOM	MAX	UNIT
T1	nReset timing	nReset timing after VBAT and VIO supply are stable		1		ms
T2	Hardware wake-up time			25		ms
T3	Time taken by ROM firmware to initialize hardware	Includes 32.768-kHz XOSC settling time		1.1		s
T4	App code load time for CC3230S	CC3230S		Image size (KB) × 1.7 ms		
	App code integrity check time for CC3230SF	CC3230SF		Image size (KB) × 0.06 ms		

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7.16.3.3 nRESET (External 32-kHz Clock)

Figure 7-7 shows the reset timing diagram for the external 32-kHz clock first-time power-up and reset removal.

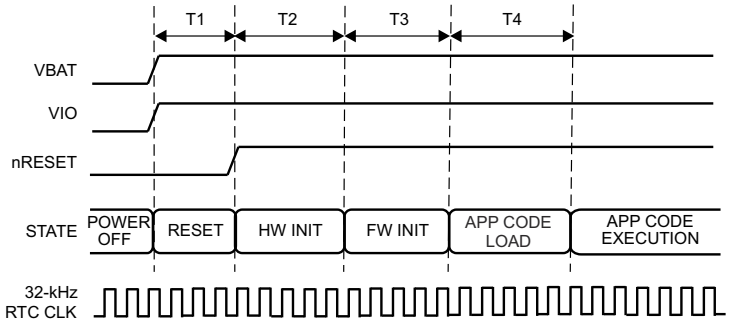

Figure 7-7. First-Time Power-Up and Reset Removal Timing Diagram (External 32-kHz Clock)

Section 7.16.3.3.1 describes the timing requirements for the external 32-kHz clock first-time power-up and reset removal.

7.16.3.3.1 First-Time Power-Up and Reset Removal Timing Requirements (External 32-kHz Clock)

ITEM	NAME	DESCRIPTION	MIN	NOM	MAX	UNIT
T1	nReset time	nReset timing after VBAT and VIO supply are stable		1		ms
T2	Hardware wake-up time			25		ms
T3	Time taken by ROM firmware to initialize hardware	CC3230S		10.3		ms
		CC3230SF		17.3		
T4	App code load time	CC3230S		Image size (KB) × 1.7 ms		
	App code integrity check time	CC3230SF		Image size (KB) × 0.06 ms		

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7.16.4 Wakeup From HIBERNATE Mode

Note

The 32.768-kHz crystal is enabled by default when the chip goes into HIBERNATE mode.

Table 7-8 lists the software hibernate timing requirements.

Table 7-8. Software Hibernate Timing Requirements

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{HIB_MIN}	Minimum hibernate time		10			ms
$T_{wake_from_hib}$ (1)	Hardware wakeup time plus firmware initialization time			50(2)		ms
T_APP_CODE_LOAD	App code load time	CC3230S		Image size (KB) × 1.7 ms		ms
		CC3230SF		Image size (KB) × 0.06 ms		

(1) $T_{wake_from_hib}$ can be 200 ms on rare occasions when calibration is performed. Calibration is performed sparingly, typically when exiting Hibernate and only if temperature has changed by more than 20°C or more than 24 hours have elapsed since a prior calibration.
(2) Wake-up time can extend to 75 ms if a patch is downloaded from the serial Flash.

Figure 7-8 shows the timing diagram for wakeup from HIBERNATE mode.

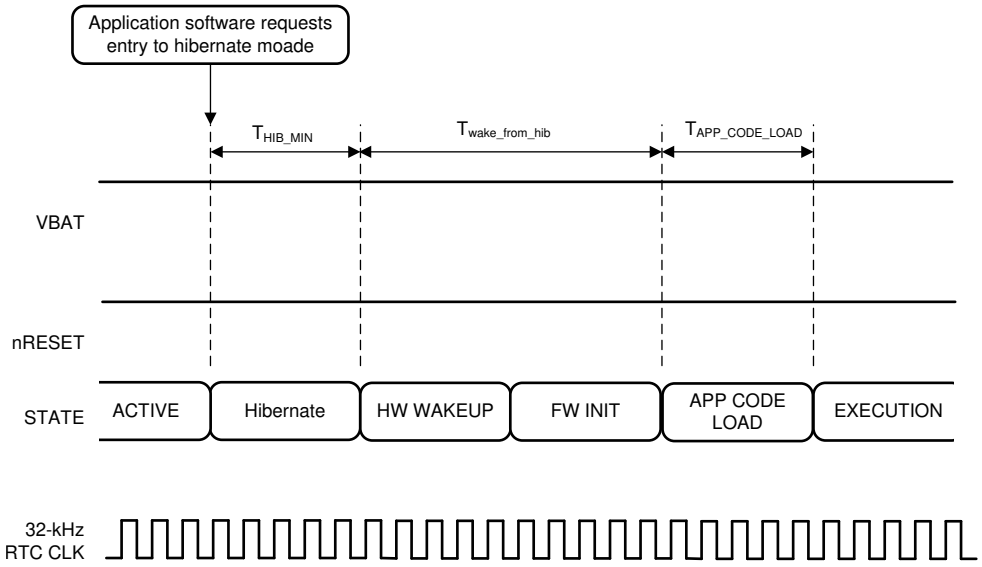

Figure 7-8. Wakeup From HIBERNATE Timing Diagram

7.16.5 Clock Specifications

The CC3230x device requires two separate clocks for operation:

- A slow clock running at 32.768 kHz is used for the RTC.
- A fast clock running at 40 MHz is used by the device for the internal processor and the WLAN subsystem.

The device features internal oscillators that enable the use of less-expensive crystals rather than dedicated TCXOs for these clocks. The RTC can also be fed externally to provide reuse of an existing clock on the system and to reduce overall cost.

7.16.5.1 Slow Clock Using Internal Oscillator

The RTC crystal connected on the device supplies the free-running slow clock. The accuracy of the slow clock frequency must be 32.768 kHz ±150 ppm. In this mode of operation, the crystal is tied between RTC_XTAL_P (pin 51) and RTC_XTAL_N (pin 52) with a suitable load capacitance to meet the ppm requirement.

Figure 7-9 shows the crystal connections for the slow clock.

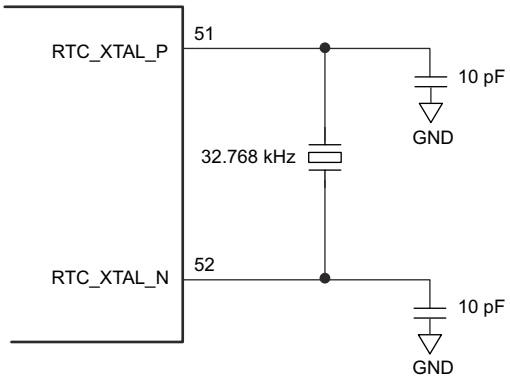

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Figure 7-9. RTC Crystal Connections

Table 7-9 lists the RTC crystal requirements.

Table 7-9. RTC Crystal Requirements

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			32.768		kHz
Frequency accuracy	Initial plus temperature plus aging			±150	ppm
Crystal ESR	32.768 kHz			70	kΩ

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7.16.5.2 Slow Clock Using an External Clock

When an RTC oscillator is present in the system, the CC3230x device can accept this clock directly as an input. The clock is fed on the RTC_XTAL_P line, and the RTC_XTAL_N line is held to V_{IO}. The clock must be a CMOS-level clock compatible with V_{IO} fed to the device.

Figure 7-10 shows the external RTC input connection.

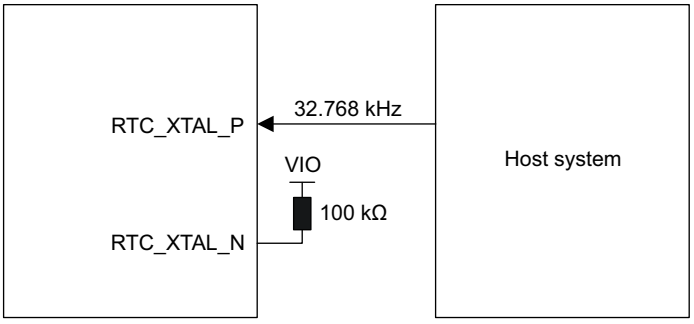

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Figure 7-10. External RTC Input

Section 7.16.5.2.1 lists the external RTC digital clock requirements.

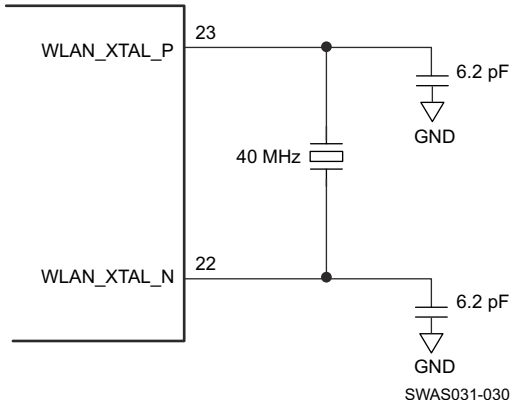
7.16.5.2.1 External RTC Digital Clock Requirements

CHARACTERISTICS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Frequency			32768		Hz
	Frequency accuracy (initial plus temperature plus aging)			±150		ppm
t_r, t_f	Input transition time t_r, t_f (10% to 90%)				100	ns
	Frequency input duty cycle		20%	50%	80%	
V_{ih}	Slow clock input voltage limits	Square wave, DC coupled	0.65 × V_{IO}		V_{IO}	V
V_{il}			0		0.35 × V_{IO}	V_{peak}
	Input impedance		1			MΩ
					5	pF

7.16.5.3 Fast Clock (F_{ref}) Using an External Crystal

The CC3230x device also incorporates an internal crystal oscillator to support a crystal-based fast clock. The crystal is fed directly between WLAN_XTAL_P (pin 23) and WLAN_XTAL_N (pin 22) with suitable loading capacitors.

Figure 7-11 shows the crystal connections for the fast clock.



A. The crystal capacitance must be tuned to ensure that the PPM requirement is met. See *CC31xx & CC32xx Frequency Tuning* for information on frequency tuning.

Figure 7-11. Fast Clock Crystal Connections

Section 7.16.5.3.1 lists the WLAN fast-clock crystal requirements.

7.16.5.3.1 WLAN Fast-Clock Crystal Requirements

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			40		MHz
Frequency accuracy	Initial plus temperature plus aging			±20	ppm
Crystal ESR	40 MHz			60	Ω

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7.16.5.4 Fast Clock (F_{ref}) Using an External Oscillator

The CC3230x device can accept an external TCXO/XO for the 40-MHz clock. In this mode of operation, the clock is connected to WLAN_XTAL_P (pin 23). WLAN_XTAL_N (pin 22) is connected to GND. The external TCXO/XO can be enabled by TCXO_EN (pin 21) from the device to optimize the power consumption of the system.

If the TCXO does not have an enable input, an external LDO with an enable function can be used. Using the LDO improves noise on the TCXO power supply.

Figure 7-12 shows the connection.

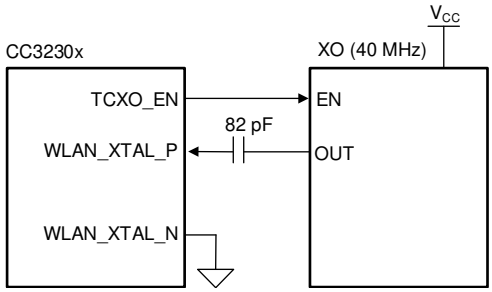

Figure 7-12. External TCXO Input

Section 7.16.5.4.1 lists the external F_{ref} clock requirements.

7.16.5.4.1 External F_{ref} Clock Requirements (–40°C to +85°C)

CHARACTERISTICS			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Frequency				40.00		MHz
	Frequency accuracy (initial plus temperature plus aging)					±20	ppm
	Frequency input duty cycle			45%	50%	55%	
V_{pp}	Clock voltage limits		Sine or clipped sine wave, AC coupled	0.7		1.2	V_{pp}
	Phase noise at 40 MHz		at 1 kHz			–125	dBc/Hz
			at 10 kHz			–138.5	
			at 100 kHz			–143	
	Input impedance	Resistance		12			kΩ
		Capacitance				7	pF

7.16.6 Peripherals Timing

This section describes the peripherals that are supported by the CC3230x device:

- SPI
- I^2S
- GPIOs
- I^2C
- IEEE 1149.1 JTAG
- ADC
- Camera Parallel Port
- UART
- SD Host
- Timers

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7.16.6.1 SPI

7.16.6.1.1 SPI Master

The CC3230x microcontroller includes one SPI module that can be configured as a master or slave device. The SPI includes a serial clock with programmable frequency, polarity, and phase; a programmable timing control between chip select and external clock generation; and a programmable delay before the first SPI word is transmitted. Slave mode does not include a dead cycle between two successive words.

Figure 7-13 shows the timing diagram for the SPI master.

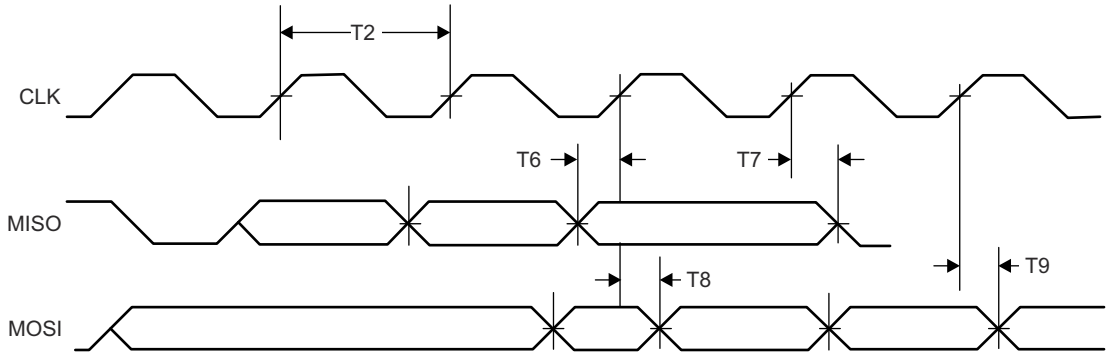

Figure 7-13. SPI Master Timing Diagram

Section 7.16.6.1.1.1 lists the timing parameters for the SPI master.

7.16.6.1.1.1 SPI Master Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
	F(1)	Clock frequency		30	MHz
T2	T_{clk} (1)	Clock period	33.3		ns
	D(1)	Duty cycle	45%	55%	
T6	t_{IS} (1)	RX data setup time	1		ns
T7	t_{IH} (1)	RX data hold time	2		ns
T8	t_{OD} (1)	TX data output delay		8.5	ns
T9	t_{OH} (1)	TX data hold time		8	ns

(1) Timing parameter assumes a maximum load of 20 pF.

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7.16.6.1.2 SPI Slave

Figure 7-14 shows the timing diagram for the SPI slave.

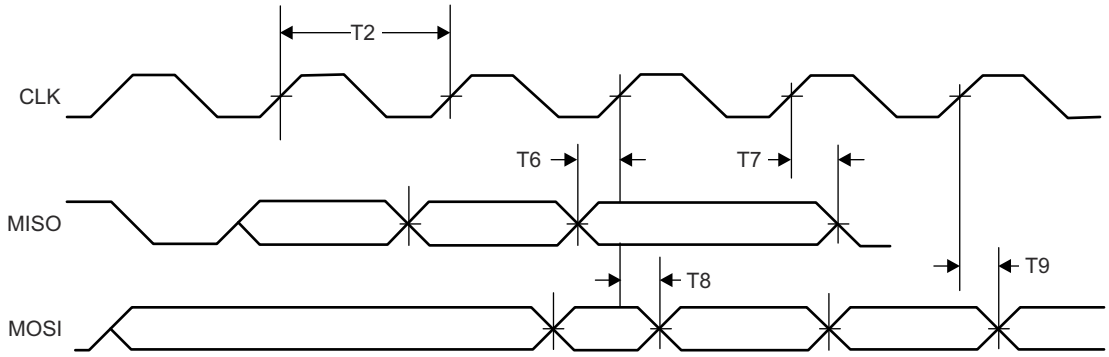

Figure 7-14. SPI Slave Timing Diagram

Section 7.16.6.1.2.1 lists the timing parameters for the SPI slave.

7.16.6.1.2.1 SPI Slave Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
	F(1)	Clock frequency at V_{BAT} = 3.3 V		20	MHz
		Clock frequency at V_{BAT} ≤ 2.1 V		12	
T2	T_{clk} (1)	Clock period	50		ns
	D(1)	Duty cycle	45%	55%	
T6	t_{IS} (1)	RX data setup time	4		ns
T7	t_{IH} (1)	RX data hold time	4		ns
T8	t_{OD} (1)	TX data output delay		20	ns
T9	t_{OH} (1)	TX data hold time		24	ns

(1) Timing parameter assumes a maximum load of 20 pF at 3.3 V.

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7.16.6.2 I²S

The McASP interface functions as a general-purpose audio serial port optimized for multichannel audio applications and supports transfer of two stereo channels over two data pins. The McASP consists of transmit and receive sections that operate synchronously and have programmable clock and frame-sync polarity. A fractional divider is available for bit-clock generation.

7.16.6.2.1 I²S Transmit Mode

Figure 7-15 shows the timing diagram for the I²S transmit mode.

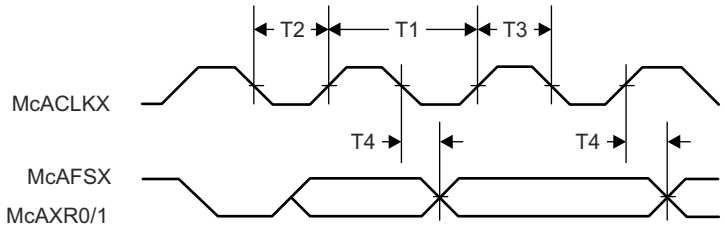

Figure 7-15. I²S Transmit Mode Timing Diagram

Section 7.16.6.2.1.1 lists the timing parameters for the I²S transmit mode.

7.16.6.2.1.1 I²S Transmit Mode Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
T1	f_{clk} (1)	Clock frequency		9.216	MHz
T2	t^{LP} (1)	Clock low period		1/2 fclk	ns
T3	t_{HT} (1)	Clock high period		1/2 fclk	ns
T4	t_{OH} (1)	TX data hold time		22	ns

(1) Timing parameter assumes a maximum load of 20 pF.

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7.16.6.2.2 I²S Receive Mode

Figure 7-16 shows the timing diagram for the I²S receive mode.

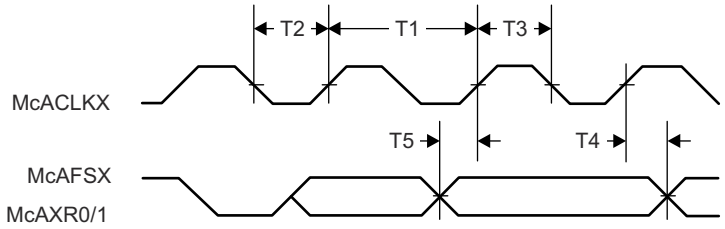

Figure 7-16. I²S Receive Mode Timing Diagram

Section 7.16.6.2.2.1 lists the timing parameters for the I²S receive mode.

7.16.6.2.2.1 I²S Receive Mode Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
T1	f_{clk} (1)	Clock frequency		9.216	MHz
T2	t^{LP} (1)	Clock low period		1/2 f_{clk}	ns
T3	t_{HT} (1)	Clock high period		1/2 f_{clk}	ns
T4	t_{OH} (1)	RX data hold time		0	ns
T5	t_{OS} (1)	RX data setup time		15	ns

(1) Timing parameter assumes a maximum load of 20 pF.

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7.16.6.3 GPIOs

All digital pins of the device can be used as general-purpose input/output (GPIO) pins. The GPIO module consists of four GPIO blocks, each of which provides eight GPIOs. The GPIO module supports 24 programmable GPIO pins, depending on the peripheral used. Each GPIO has configurable pullup and pulldown strength (weak 10 µA), configurable drive strength (2, 4, and 6 mA), and open-drain enable.

Note

Unless otherwise stated, GPIO specifications also applies to pins configured as COEX IOs and network scripter interface

Figure 7-17 shows the GPIO timing diagram.

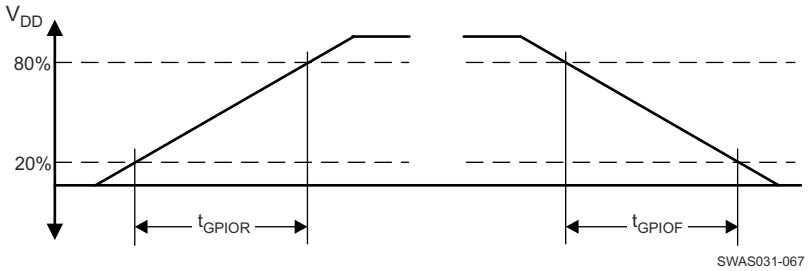

Figure 7-17. GPIO Timing Diagram

7.16.6.3.1 GPIO Output Transition Time Parameters (V_{supply} = 3.3 V)

Section 7.16.6.3.1.1 lists the GPIO output transition times for V_{supply} = 3.3 V.

7.16.6.3.1.1 GPIO Output Transition Times (V_{supply} = 3.3 V) (1) (2)

DRIVE STRENGTH (mA)	DRIVE STRENGTH CONTROL BITS	t_r			t_f			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
2(3)	2MA_EN=1	8.0	9.3	10.7	8.2	9.5	11.0	ns
	4MA_EN=0							
4(3)	2MA_EN=0	6.6	7.1	7.6	4.7	5.2	5.8	ns
	4MA_EN=1							
6	2MA_EN=1	3.2	3.5	3.7	2.3	2.6	2.9	ns
	4MA_EN=1							

(1) V_{supply} = 3.3 V, T = 25°C, total pin load = 30 pF
(2) The transition data applies to the pins except the multiplexed analog-digital pins 29, 30, 45, 50, 52, and 53.
(3) The 2-mA and 4-mA drive strength does not apply to the COEX I/O pins. Pins configured as COEX lines are invariably driven at 6 mA.

7.16.6.3.2 GPIO Input Transition Time Parameters

Section 7.16.6.3.2.1 lists the input transition time parameters.

7.16.6.3.2.1 GPIO Input Transition Time Parameters

		MIN	MAX	UNIT
t_r	Input transition time (t_r, t_f), 10% to 90%	1	3	ns
t_f		1	3	ns

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7.16.6.4 I²C

The CC3230x microcontroller includes one I²C module operating with standard (100 kbps) or fast (400 kbps) transmission speeds.

Figure 7-18 shows the I²C timing diagram.

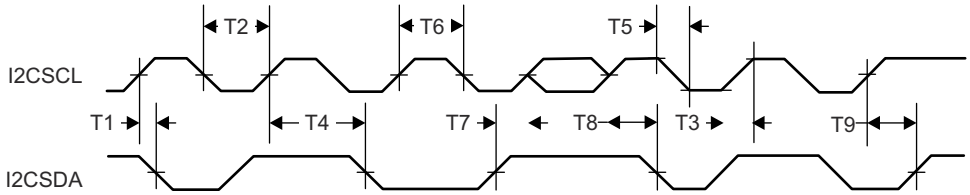

Figure 7-18. I²C Timing Diagram

Section 7.16.6.4.1 lists the I²C timing parameters.

7.16.6.4.1 I²C Timing Parameters (3)

PARAMETER NUMBER			MIN	MAX	UNIT
T2	t_{LP}	Clock low period	See (1)		System clock
T3	t_{SRT}	SCL/SDA rise time		See (2)	ns
T4	t_{DH}	Data hold time	N/A		
T5	t_{SFT}	SCL/SDA fall time	3		ns
T6	t_{HT}	Clock high time	See (1)		System clock
T7	t_{DS}	Data setup time	tLP/2		System clock
T8	t_{SCSR}	Start condition setup time	36		System clock
T9	t_{SCS}	Stop condition setup time	24		System clock

(1) This value depends on the value programmed in the clock period register of I²C. Maximum output frequency is the result of the minimal value programmed in this register.
(2) Because I²C is an open-drain interface, the controller can drive logic 0 only. Logic is the result of an external pullup resistor. Rise time depends on the value of the external signal capacitance and external pullup register.
(3) All timing is with 6-mA drive and 20-pF load.

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7.16.6.5 IEEE 1149.1 JTAG

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a test access port (TAP) and boundary scan architecture for digital integrated circuits and provides a standardized serial interface to control the associated test logic. For detailed information on the operation of the JTAG port and TAP controller, see the IEEE Standard 1149.1,*Test Access Port and Boundary-Scan Architecture*.

Figure 7-19 shows the JTAG timing diagram.

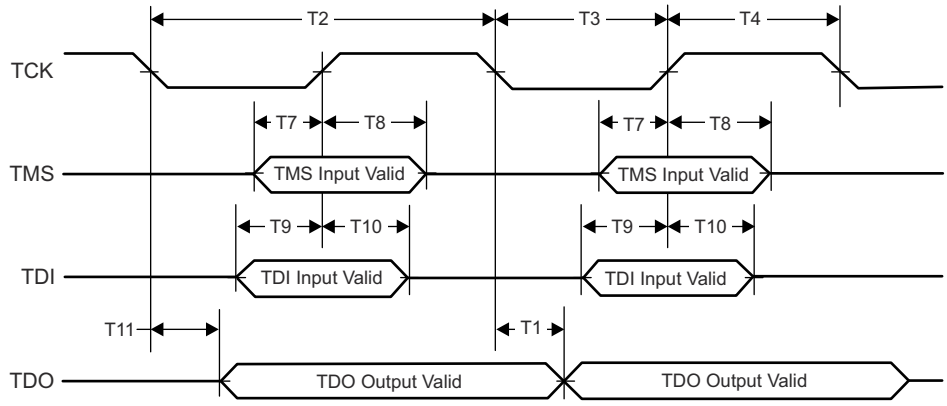

Figure 7-19. JTAG Timing Diagram

Section 7.16.6.5.1 lists the JTAG timing parameters.

7.16.6.5.1 JTAG Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
T1	f_{TCK}	Clock frequency		15	MHz
T2	t_{TCK}	Clock period		$1 / f_{TCK}$	ns
T3	t_{CL}	Clock low period		$t_{TCK} / 2$	ns
T4	t_{CH}	Clock high period		$t_{TCK} / 2$	ns
T7	t_{TMS_SU}	TMS setup time	1		ns
T8	t_{TMS_HO}	TMS hold time	16		ns
T9	t_{TDI_SU}	TDI setup time	1		ns
T10	t_{TDI_HO}	TDI hold time	16		ns
T11	t_{TDO_HO}	TDO hold time		15	ns

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7.16.6.6 ADC

Figure 7-20 shows the ADC clock timing diagram.

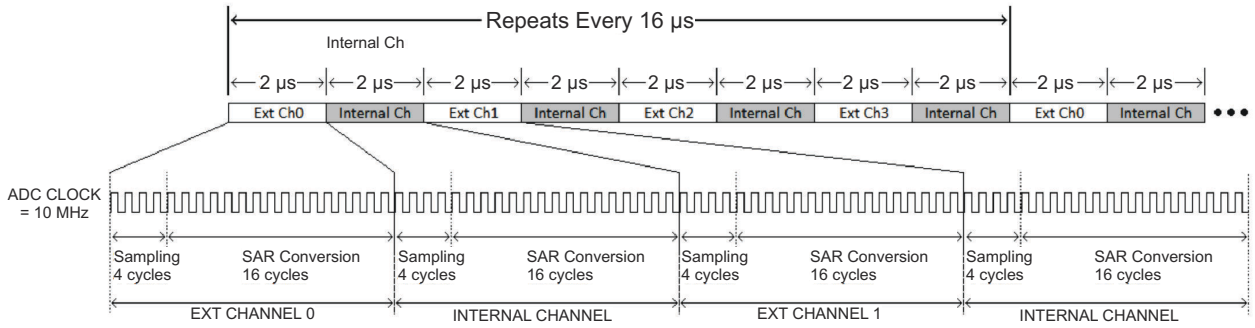

Figure 7-20. ADC Clock Timing Diagram

Section 7.16.6.6.1 lists the ADC electrical specifications. See the CC32xx ADC Appnote wiki for further information on using the ADC and for application-specific examples.

7.16.6.6.1 ADC Electrical Specifications

PARAMETER	DESCRIPTION	TEST CONDITIONS and ASSUMPTIONS	MIN	TYP	MAX	UNIT
Nbits	Number of bits			12		Bits
INL	Integral nonlinearity	Worst-case deviation from histogram method over full scale (not including first and last three LSB levels)	–2.5		2.5	LSB
DNL	Differential nonlinearity	Worst-case deviation of any step from ideal	–1		4	LSB
Input range			0		1.4	V
Driving source impedance					100	Ω
FCLK	Clock rate	Successive approximation input clock rate		10		MHz
Input capacitance				12		pF
Input impedance		ADC Pin 57		2.15		kΩ
		ADC Pin 58		0.7		
		ADC Pin 59		2.12		
		ADC Pin 60		1.17		
Number of channels				4		
F_{sample}	Sampling rate of each pin			62.5		ksps
F_input_max	Maximum input signal frequency				31	kHz
SINAD	Signal-to-noise and distortion	Input frequency DC to 300 Hz and 1.4 V_{pp} sine wave input	55	60		dB
I_active	Active supply current	Average for analog-to-digital during conversion without reference current		1.5		mA
I_PD	Power-down supply current for core supply	Total for analog-to-digital when not active (this must be the SoC level test)		1		µA
Absolute offset error		FCLK = 10 MHz		±2		mV
Gain error				±2%		
V_{ref}	ADC reference voltage			1.467		V

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7.16.6.7 Camera Parallel Port

The fast camera parallel port interfaces with a variety of external image sensors, stores the image data in a FIFO, and generates DMA requests. The camera parallel port supports 8 bits.

Figure 7-21 shows the timing diagram for the camera parallel port.

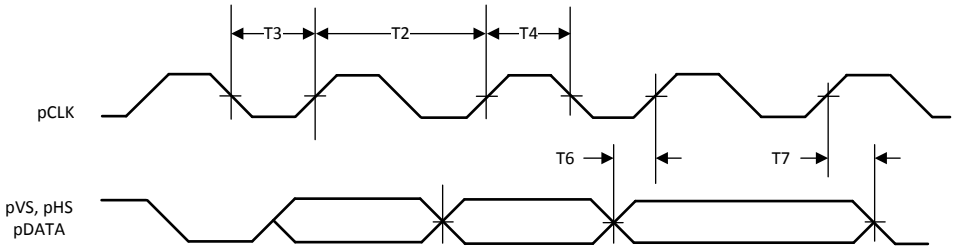

Figure 7-21. Camera Parallel Port Timing Diagram

Section 7.16.6.7.1 lists the timing parameters for the camera parallel port.

7.16.6.7.1 Camera Parallel Port Timing Parameters

PARAMETER NUMBER			MIN	MAX	UNIT
	pCLK	Clock frequency		2	MHz
T2	T_{clk}	Clock period		1/pCLK	ns
T3	t_{LP}	Clock low period		$T_{clk}/2$	ns
T4	t_{HT}	Clock high period		$T_{clk}/2$	ns
T6	t_{IS}	RX data setup time		2	ns
T7	t_{IH}	RX data hold time		2	ns
	D	Duty cycle	45%	55%	

7.16.6.8 UART

The CC3230x device includes two UARTs with the following features:

- Programmable baud-rate generator allows speeds up to 3 Mbps
- Separate 16-bit × 8-bit TX and RX FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including a 1-byte-deep operation providing conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- Generation and detection of line-breaks
- Fully programmable serial interface characteristics:
  - 5, 6, 7, or 8 data bits
  - Generation and detection of even, odd, stick, or no-parity bits
  - Generation of 1 or 2 stop-bits
- RTS and CTS hardware flow support
- Standard FIFO-level and End-of-Transmission interrupts
- Efficient transfers using µDMA:
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
  - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level
- System clock is used to generate the baud clock.

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7.16.6.9 SD Host

The CC3230x device provides an interface between a local host (LH), such as an MCU and an SD memory card, and handles SD transactions with minimal LH intervention.

The SD host does the following:

- Provides SD card access in 1-bit mode
- Deals with SD protocol at the transmission level
- Handles data packing
- Adds cyclic redundancy checks (CRC)
- Start and end bit
- Checks for syntactical correctness

The application interface sends every SD command and either polls for the status of the adapter or waits for an interrupt request. The result is then sent back to the application interface in case of exceptions or to warn of end-of-operation. The controller can be configured to generate DMA requests and work with minimum CPU intervention. Given the nature of integration of this peripheral on the CC3230x platform, TI recommends that developers use peripheral library APIs to control and operate the block. This section emphasizes understanding the SD host APIs provided in the peripheral library of the CC3230x Software Development Kit (SDK).

The SD Host features are as follows:

- Full compliance with SD command and response sets, as defined in the SD memory card
  - Specifications, v2.0
  - Includes high-capacity (size >2GB) HC and SD cards
- Flexible architecture allows support for new command structure
- 1-bit transfer mode specifications for SD cards
- Built-in 1024-byte buffer for read or write
  - 512-byte buffer for both transmit and receive
  - Each buffer is 32-bits wide by 128-words deep
- 32-bit-wide access bus to maximize bus throughput
- Single interrupt line for multiple interrupt source events
- Two slave DMA channels (1 for TX, 1 for RX)
- Programmable clock generation
- Integrates an internal transceiver that allows a direct connection to the SD card without external transceiver
- Supports configurable busy and response timeout
- Support for a wide range of card clock frequency with odd and even clock ratio
- Maximum frequency supported is 24MHz

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7.16.6.10 Timers

Programmable timers can be used to count or time external events that drive the timer input pins. The CC3230x general-purpose timer module (GPTM) contains 16- or 32-bit GPTM blocks. Each 16- or 32-bit GPTM block provides two 16-bit timers or counters (referred to as Timer A and Timer B) that can be configured to operate independently as timers or event counters, or they can be concatenated to operate as one 32-bit timer. Timers can also be used to trigger µDMA transfers.

The GPTM contains four 16- or 32-bit GPTM blocks with the following functional options:

- Operating modes:
  - 16- or 32-bit programmable one-shot timer
  - 16- or 32-bit programmable periodic timer
  - 16-bit general-purpose timer with an 8-bit prescaler
  - 16-bit input-edge count or time-capture modes with an 8-bit prescaler
  - 16-bit PWM mode with an 8-bit prescaler and software-programmable output inversion of the PWM signal
- Counts up or counts down
- Sixteen 16- or 32-bit capture compare pins (CCP)
- User-enabled stalling when the microcontroller asserts CPU Halt flag during debug
- Ability to determine the elapsed time between the assertion of the timer interrupt and entry into the interrupt service routine
- Efficient transfers using micro direct memory access controller (µDMA):
  - Dedicated channel for each timer
  - Burst request generated on timer interrupt
- Runs from system clock (80 MHz)

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8 Detailed Description

8.1 Overview

The CC3230x wireless MCU family has a rich set of peripherals for diverse application requirements. This section briefly highlights the internal details of the CC3230x devices and offers suggestions for application configurations.

8.2 Arm® Cortex®-M4 Processor Core Subsystem

The high-performance Arm® Cortex®-M4 processor provides a cost-conscious platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

- The Arm Cortex-M4 core has low-latency interrupt processing with the following features:
  - A 32-bit Arm® Thumb® instruction set optimized for embedded applications
  - Handler and thread modes
  - Low-latency interrupt handling by automatic processor state saving and restoration during entry and exit
  - Support for Armv6 unaligned accesses
- Nested vectored interrupt controller (NVIC) closely integrated with the processor core to achieve low-latency interrupt processing. The NVIC includes the following features:
  - Bits of priority configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping that enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tail-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts
  - Processor state automatically saved on interrupt entry and restored on interrupt exit with no instruction overhead
  - Wake-up interrupt controller (WIC) providing ultra-low-power sleep mode support
- Bus interfaces:
  - Advanced high-performance bus (AHB-Lite) interfaces: system bus interfaces
  - Bit-band support for memory and select peripheral that includes atomic bit-band write and read operations
- Cost-conscious debug solution featuring:
  - Debug access to all memory and registers in the system, including access to memory-mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted.
  - Serial wire debug port (SW-DP) or serial wire JTAG debug port (SWJ-DP) debug access
  - Flash patch and breakpoint (FPB) unit to implement breakpoints and code patches

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8.3 Wi-Fi® Network Processor Subsystem

The Wi-Fi network processor subsystem includes a dedicated Arm MCU to completely offload the host MCU along with an 802.11b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast, secure WLAN and Internet connections with 256-bit encryption. The CC3230x devices support station, AP, and Wi-Fi Direct modes. The device also supports WPA2 personal and enterprise security, WPS 2.0, and WPA3 personal and enterprise [4]. The Wi-Fi network processor includes an embedded IPv6, IPv4 TCP/IP stack, TLS stack and network applications such as HTTPS server.

8.3.1 WLAN

The WLAN features are as follows:

- 802.11b/g/n integrated radio, modem, and MAC supporting WLAN communication as a BSS station, AP, Wi-Fi Direct client, and group owner with CCK and OFDM rates in the 2.4GHz band (channels 1 through 13).

Note

802.11n is supported only in Wi-Fi® station and Wi-Fi Direct®.

- The automatically calibrated radio with a single-ended 50Ω interface enables easy connection to the antenna without requiring expertise in radio circuit design.
- Advanced connection manager with multiple user-configurable profiles stored in serial flash allows automatic fast connection to an access point without user or host intervention.
- Supports all common Wi-Fi security modes for personal and enterprise networks with on-chip security accelerators, including WEP, WPA/WPA2 PSK, WPA2 Enterprise (802.1x), WPA3 Personal, and WPA3 Enterprise.

Note

When using WPA Enterprise security modes, the TLS socket used to communicate with the Radius server is limited to TLSv1.0.

- Smart provisioning options are deeply integrated within the device providing a comprehensive end-to-end solution. With elaborate events notification to the host, enabling the application to control the provisioning decision flow. The wide variety of Wi-Fi provisioning methods include:
  - Access Point with HTTP server
  - WPS - Wi-Fi Protected Setup, supporting both push button and pin code options.
  - SmartConfig™ Technology: TI proprietary, easy-to-use, one-step, one-time process used to connect a CC3230x-enabled device to the home wireless network.
- 802.11 transceiver mode allows transmitting and receiving of proprietary data through a socket The 802.11 transceiver mode provides the option to select the working channel, rate, and transmitted power. The receiver mode works with the filtering options.
- Antenna selection for best connection
- BLE/2.4GHz radio coexistence mechanism to avoid interference

[4] See CC3230 SDK v3.40 or later for details. Limited to STA mode only.

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8.3.2 Network Stack

The Network Stack features are as follows:

- Integrated IPv4, IPv6 TCP/IP stack with BSD socket APIs for simple Internet connectivity with any MCU, microprocessor, or ASIC

Note

Not all APIs are 100% BSD compliant. Not all BSD APIs are supported.

- Support of 16 simultaneous TCP, UDP, RAW, SSL\TLS sockets
- Built-in network protocols:
  - Static IP, LLA, DHCPv4, DHCPv6 with DAD and stateless autoconfiguration
  - ARP, ICMPv4, IGMP, ICMPv6, MLD, ND
  - DNS client for easy connection to the local network and the Internet
- Built-in network applications and utilities:
  - HTTP/HTTPS
    - Web page content stored on serial flash
    - RESTful APIs for setting and configuring application content
    - Dynamic user callbacks
  - Service discovery: Multicast DNS service discovery lets a client advertise its service without a centralized server. After connecting to the access point, the CC3230x device provides critical information, such as device name, IP, vendor, and port number.
  - DHCP server
  - Ping

Table 8-1 describes the NWP features.

Table 8-1. NWP Features

FEATURE	DESCRIPTION
Wi-Fi standards	802.11b/g/n station 802.11b/g AP supporting up to four stations Wi-Fi Direct client and group owner
Wi-Fi channels	2.4 GHz ISM
Channel Bandwidth	20 MHz
Wi-Fi security	WEP, WPA/WPA2 PSK, WPA2 enterprise (802.1x), WPA3 personal and enterprise (1)
Wi-Fi provisioning	SmartConfig technology, Wi-Fi protected setup (WPS2), AP mode with internal HTTP web server
IP protocols	IPv4/IPv6
IP addressing	Static IP, LLA, DHCPv4, DHCPv6 with DAD
Cross layer	ARP, ICMPv4, IGMP, ICMPv6, MLD, NDP
Transport	UDP, TCP SSLv3.0/TLSv1.0/TLSv1.1/TLSv1.2 RAW
Network applications and utilities	Ping HTTP/HTTPS web server mDNS DNS-SD DHCP server
Host interface	UART/SPI

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Table 8-1. NWP Features (continued)

FEATURE	DESCRIPTION
Security	Device identity Trusted root-certificate catalog TI root-of-trust public key The CC3230S and CC3230SF variants also support: • Secure key storage • Online certificate status protocol (OCSP) • Certificate signing request (CSR) • Unique per device Key-Pair • File system security • Software tamper detection • Cloning protection • Secure boot • Validate the integrity and authenticity of the run-time binary during boot • Initial secure programming • Debug security • JTAG and debug
Power management	Enhanced power policy management uses 802.11 power save and deep-sleep power modes
Other	Transceiver Programmable RX filters with event-trigger mechanism Rx Metrics for tracking the surrounding RF environment

(1) See CC3230 SDK v3.40 or newer for details. Limited to STA mode only.

8.4 Security

The SimpleLink™ Wi-Fi® CC3230x Internet-on-a chip device enhances the security capabilities available for development of IoT devices, while completely offloading these activities from the MCU to the networking subsystem. The security capabilities include the following key features:

Wi-Fi and Internet Security:

- Personal and enterprise Wi-Fi security
  - Personal standards
    - AES (WPA2-PSK)
    - TKIP (WPA-PSK)
    - WEP
  - Enterprise standards
    - EAP Fast
    - EAP PEAPv0/1
    - EAP PEAPv0 TLS
    - EAP PEAPv1 TLS EAP LS
    - EAP TLS
    - EAP TTLS TLS
    - EAP TTLS MSCHAPv2
- Secure sockets
  - Protocol versions: OCSP, SSL v3, TLS 1.0, TLS 1.1, TLS 1.2
  - Powerful crypto engine for fast, secure Wi-Fi and internet connections with 256-bit AES encryption for TLS and SSL connections

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  - Ciphers suites
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_SSL_RSA_WITH_RC4_128_MD5
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_RC4_128_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_CBC_SHA
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_CBC_SHA
    - SL_SEC_MASK_TLS_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_128_GCM_SHA256
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_AES_256_GCM_SHA384
    - SL_SEC_MASK_TLS_ECDHE_ECDSA_WITH_CHACHA20_POLY1305_SHA256
    - SL_SEC_MASK_TLS_ECDHE_RSA_WITH_CHACHA20_POLY1305_SHA256
    - SL_SEC_MASK_TLS_DHE_RSA_WITH_CHACHA20_POLY1305_SHA256
  - Server authentication
  - Client authentication
  - Domain name verification
  - Runtime socket upgrade to secure socket – STARTTLS
- Secure HTTP server (HTTPS)
- Trusted root-certificate catalog – Verifies that the CA used by the application is trusted and known secure content delivery
- TI root-of-trust public key – Hardware-based mechanism that allows authenticating TI as the genuine origin of a given content using asymmetric keys
- Secure content delivery – Allows encrypted file transfer to the system using asymmetric keys created by the device

Code and Data Security:

- Network passwords and certificates are encrypted and signed.
- Cloning protection – Application and data files are encrypted by a unique key per device.
- Access control – Access to application and data files only by using a token provided in file creation time. If an unauthorized access is detected, a tamper protection lock down mechanism takes effect.
- Secured boot – Authentication of the application image on every boot
- Code and data encryption – User application and data files can be encrypted in the serial flash
- Code and data authentication – User Application and data files are authenticated with a public key certificate
- Offloaded crypto library for asymmetric keys, including the ability to create key-pair, sign and verify data buffer
- Recovery mechanism

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Device Security:

- Separate execution environments – Application processor and network processor run on separate Arm cores
- Initial secure programming – Allows for keeping the content confidential on the production line
- Debug security
  - JTAG lock
  - Debug ports lock
- True random number generator

Figure 8-1 shows the high-level structure of the CC3230S and CC3230SF devices. The application image, user data, and network information files (passwords, certificates) are encrypted using a device-specific key.

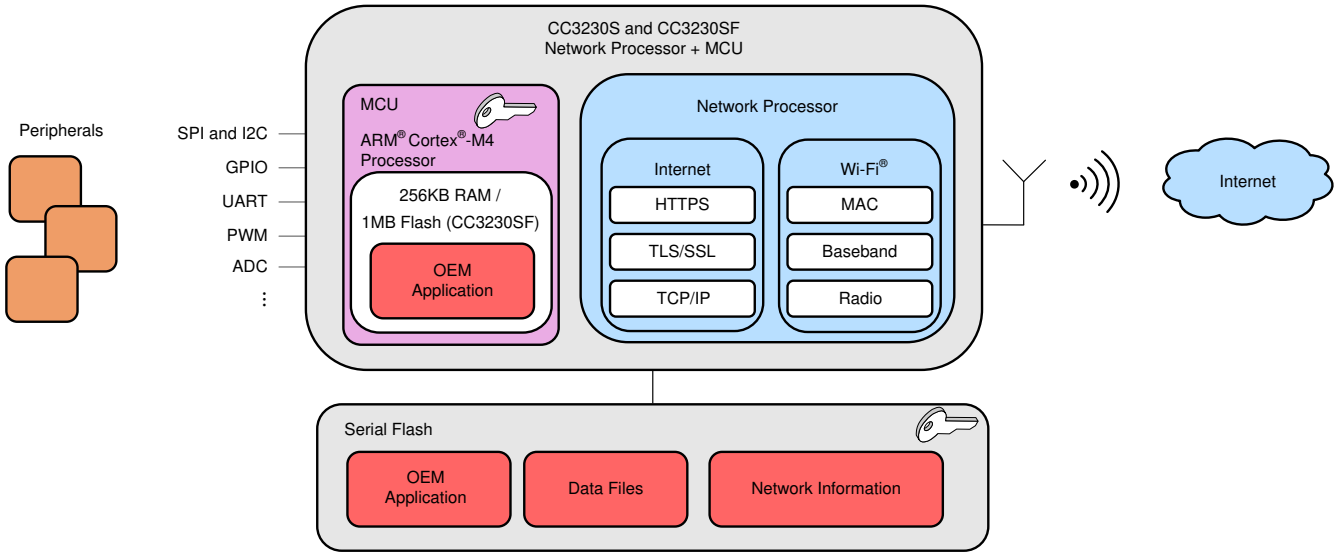

Figure 8-1. CC3230S and CC3230SF High-Level Structure

8.5 Power-Management Subsystem

The CC3230x power-management subsystem contains DC/DC converters to accommodate the different voltage or current requirements of the system.

- Digital DC/DC (Pin 44)
  - Input: V_{BAT} wide voltage (2.1V to 3.6V)
- ANA1 DC/DC (Pin 37)
  - Input: V_{BAT} wide voltage (2.1V to 3.6V)
- PA DC/DC (Pin 39)
  - Input: V_{BAT} wide voltage (2.1V to 3.6V)
- ANA2 DC/DC (Pin 47, CC3230SF only)
  - Input: V_{BAT} wide voltage (2.1V to 3.6V)

The CC3230x device is a single-chip WLAN radio solution used on an embedded system with a wide-voltage supply range. The internal power management, including DC/DC converters and LDOs, generates all of the voltages required for the device to operate from a wide variety of input sources.

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8.6 Low-Power Operating Mode

From a power-management perspective, the CC3230x device comprises the following two independent subsystems:

- Arm® Cortex®-M4 application processor subsystem
- Networking subsystem

Each subsystem operates in one of several power states.

The Arm® Cortex®-M4 application processor runs the user application loaded from an external serial flash, or internal flash (in CC3230SF). The networking subsystem runs preprogrammed TCP/IP and Wi-Fi data link layer functions.

The user program controls the power state of the application processor subsystem. The application processor can be in one of the five modes described in User Program Modes.

Table 8-2. User Program Modes

APPLICATION PROCESSOR (MCU) MODE(1)	DESCRIPTION
MCU active mode	MCU executing code at a state rate of 80MHz
MCU sleep mode	The MCU clocks are gated off in sleep mode and the entire state of the device is retained. Sleep mode offers instant wakeup. The MCU can be configured to wake up by an internal fast timer or by activity from any GPIO line or peripheral.
MCU LPDS mode	State information is lost and only certain MCU-specific register configurations are retained. The MCU can wake up from external events or by using an internal timer. (The wake-up time is less than 3ms.) Certain parts of memory can be retained while the MCU is in LPDS mode. The amount of memory retained is configurable. Users can choose to preserve code and the MCU-specific setting. The MCU can be configured to wake up using the RTC timer or by an external event on specific GPIOs as the wake-up source.
MCU hibernate mode	The lowest power mode in which all digital logic is power-gated. Only a small section of the logic directly powered by the input supply is retained. The RTC continues running and the MCU supports wakeup from an external event or from an RTC timer expiry. Wake-up time is longer than LPDS mode at about 15ms plus the time to load the application from serial flash, which varies according to code size. In this mode, the MCU can be configured to wake up using the RTC timer or external event on a GPIO.
MCU shutdown mode	The lowest power mode system-wise. All device logics are off, including the RTC. The wake-up time in this mode is longer than Hibernate at about 1.1s. To enter or exit the shutdown mode, the state of the nRESET line is changed (low to shut down, high to turn on).

(1) Modes are listed in order of power consumption, with the highest power modes listed first.

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The NWP can be active or in LPDS mode and takes care of its own mode transitions. When there is no network activity, the NWP sleeps most of the time and wakes up only for beacon reception (see Table 8-3).

Table 8-3. Networking Subsystem Modes

NETWORK PROCESSOR MODE	DESCRIPTION
Network active mode (processing layer 3, 2, and 1)	Transmitting or receiving IP protocol packets
Network active mode (processing layer 2 and 1)	Transmitting or receiving MAC management frames; IP processing is not required.
Network active listen mode	Special power-optimized active mode for receiving beacon frames (no other frames are supported)
Network connected Idle	A composite mode that implements 802.11 infrastructure power-save operation. The CC3230x NWP automatically enters LPDS mode between beacons and then wakes into active Listen mode to receive a beacon and determine if there is pending traffic at the AP. If not, the NWP returns to LPDS mode and the cycle repeats. Advanced features of long sleep intervals and IoT low power for extending LPDS time for up to 22 seconds while maintaining Wi-Fi connection are supported in this mode.
Network LPDS mode	Low-power state between beacons in which the state is retained by the NWP, allowing for a rapid wake-up
Network disabled	The network is disabled.

The operation of the application and network processor ensures that the device remains in the lowest power mode most of the time to preserve battery life.

The following examples show the use of the power modes in applications:

- A product that is continuously connected to the network in the 802.11 infrastructure power-save mode but sends and receives little data spends most of the time in connected idle, which is a composite of receiving a beacon frame and waiting for the next beacon.
- A product that is not continuously connected to the network but instead wakes up periodically (for example, every 10 minutes) to send data, spends most of the time in hibernate mode, jumping briefly to active mode to transmit data.

8.7 Memory

8.7.1 External Memory Requirements

The CC3230x device maintains a proprietary file system on the serial flash. The CC3230x file system stores the MCU binary, service pack file, system files, configuration files, certificate files, web page files, and user files. By using a format command through the API, users can provide the total size allocated for the file system. The starting address of the file system cannot be set and is always at the beginning of the serial flash. The applications microcontroller must access the serial flash memory area allocated to the file system directly through the CC3230x file system. The applications microcontroller must not access the serial flash memory area directly.

The file system manages the allocation of serial flash blocks for stored files according to download order, which means that the location of a specific file is not fixed in all systems. Files are stored on serial flash using human-readable filenames rather than file IDs. The file system API works using plain text, and file encryption and decryption is invisible to the user. Encrypted files can be accessed only through the file system.

All file types can have a maximum of 100 supported files in the file system. All files are stored in 4-KB blocks and thus use a minimum of 4KB of flash space. Fail-safe files require twice the original size and use a minimum of 8KB. Encrypted files are counted as fail-safe in terms of space. The maximum file size is 1MB.

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Table 8-4 lists the minimum required memory consumption under the following assumptions:

- System files in use consume 64 blocks (256KB).
- Vendor files are not taken into account.
- MCU code is taken as the maximal possible size for the CC3230 with fail-safe enabled to account for future updates, such as through OTA.
- Gang image:
  - Storage for the gang image is rounded up to 32 blocks (meaning 128KB resolution).
  - Gang image size depends on the actual content size of all components. Additionally, the image should be 128KB aligned so unaligned memory is considered lost. Service pack, system files, and the 128KB aligned memory are assumed to occupy 256KB.
- All calculations consider that the restore-to-default is enabled.

Table 8-4. Recommended Flash Size

ITEM	CC3230S (KB)	CC3230SF (KB)
File system allocation table	20	20
System and configuration files(1)	256	256
Service pack(1)	264	264
MCU Code(1)	512	2048
Gang image size	256 + MCU	256 + MCU
Total	1308 + MCU	2844 + MCU
Minimal flash size(2)	16MBit	32MBit
Recommended flash size(2)	16MBit	32MBit

(1) Including fail-safe
(2) For maximum MCU size

Note

The maximum supported serial flash size is 32MB (256Mb) (see the *Using Serial Flash on CC3135 and CC3235x SimpleLink™ Wi-Fi® and Internet-of-Things Devices application report*).

8.7.2 Internal Memory

The CC3230x device includes on-chip SRAM to which application programs are downloaded and executed. The application developer must share the SRAM for code and data. The micro direct memory access (µDMA) controller can transfer data to and from SRAM and various peripherals. The CC3230x ROM holds the rich set of peripheral drivers, which saves SRAM space. For more information on drivers, see the CC3230x API list.

8.7.2.1 SRAM

The CC3230x family provides 256KB of on-chip SRAM. Internal RAM is capable of selective retention during LPDS mode. This internal SRAM is at offset 0x2000 0000 of the device memory map.

Use the µDMA controller to transfer data to and from the SRAM.

When the device enters low-power mode, the application developer can choose to retain a section of memory based on need. Retaining the memory during low-power mode provides a faster wakeup. The application developer can choose the amount of memory to retain in multiples of 64KB. For more information, see the API guide.

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8.7.2.2 ROM

The internal zero-wait-state ROM of the CC3230x device is at address 0x0000 0000 of the device memory and is programmed with the following components:

- Bootloader
- Peripheral driver library (DriverLib) release for product-specific peripherals and interfaces

The bootloader is used as an initial program loader (when the serial flash memory is empty). The CC3230x DriverLib software library controls on-chip peripherals with a bootloader capability. The library performs peripheral initialization and control functions, with a choice of polled or interrupt-driven peripheral support. The DriverLib APIs in ROM can be called by applications to reduce flash memory requirements and free the flash memory for other purposes.

8.7.2.3 Flash Memory

The CC3230SF device comes with an on-chip flash memory of 1MB that allows application code to execute in place while freeing SRAM exclusively for read-write data. The flash memory is used for code and constant data sections and is directly attached to the icode/dcode bus of the Arm Cortex-M4 core. A 128-bit-wide instruction prefetch buffer allows maintenance of maximum performance for linear code or loops that fit inside the buffer.

The flash memory is organized as 2KB sectors that can be independently erased. Reads and writes can be performed at word (32-bit) level.

8.7.2.4 Memory Map

Table 8-5 describes the various MCU peripherals and how they are mapped to the processor memory. For more information on peripherals, see the API document.

Table 8-5. Memory Map

START ADDRESS	END ADDRESS	DESCRIPTION	COMMENT
0x0000 0000	0x0007 FFFF	On-chip ROM (bootloader + DriverLib)	
0x0100 0000	0x010F FFFF	On-chip flash (for user application code)	CC3230SF device only
0x2000 0000	0x2003 FFFF	Bit-banded on-chip SRAM	
0x2200 0000	0x23FF FFFF	Bit-band alias of 0x2000 0000 to 0x200F FFFF	
0x4000 0000	0x4000 0FFF	Watchdog timer A0	
0x4000 4000	0x4000 4FFF	GPIO port A0	
0x4000 5000	0x4000 5FFF	GPIO port A1	
0x4000 6000	0x4000 6FFF	GPIO port A2	
0x4000 7000	0x4000 7FFF	GPIO port A3	
0x4000 C000	0x4000 CFFF	UART A0	
0x4000 D000	0x4000 DFFF	UART A1	
0x4002 0000	0x4000 07FF	I^2C A0 (master)	
0x4002 0800	0x4002 0FFF	I^2C A0 (slave)	
0x4002 4000	0x4002 4FFF	GPIO group 4	
0x4003 0000	0x4003 0FFF	General-purpose timer A0	
0x4003 1000	0x4003 1FFF	General-purpose timer A1	
0x4003 2000	0x4003 2FFF	General-purpose timer A2	
0x4003 3000	0x4003 3FFF	General-purpose timer A3	
0x400F 7000	0x400F 7FFF	Configuration registers	
0x400F E000	0x400F EFFF	System control	
0x400F F000	0x400F FFFF	µDMA	
0x4200 0000	0x43FF FFFF	Bit band alias of 0x4000 0000 to 0x400F FFFF	
0x4401 0000	0x4401 0FFF	SDIO master	
0x4401 8000	0x4401 8FFF	Camera Interface	

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Table 8-5. Memory Map (continued)

START ADDRESS	END ADDRESS	DESCRIPTION	COMMENT
0x4401 C000	0x4401 DFFF	McASP	
0x4402 0000	0x4402 1FFF	SSPI	Used for external serial flash
0x4402 1000	0x4402 2FFF	GSPI	Used by application processor
0x4402 5000	0x4402 5FFF	MCU reset clock manager	
0x4402 6000	0x4402 6FFF	MCU configuration space	
0x4402 D000	0x4402 DFFF	Global power, reset, and clock manager (GPRCM)	
0x4402 E000	0x4402 EFFF	MCU shared configuration	
0x4402 F000	0x4402 FFFF	Hibernate configuration	
0x4403 0000	0x4403 FFFF	Crypto range (includes apertures for all crypto-related blocks as follows)	
0x4403 0000	0x4403 0FFF	DTHE registers and TCP checksum	
0x4403 5000	0x4403 5FFF	MD5/SHA	
0x4403 7000	0x4403 7FFF	AES	
0x4403 9000	0x4403 9FFF	DES	
0xE000 0000	0xE000 0FFF	Instrumentation trace Macrocell™	
0xE000 1000	0xE000 1FFF	Data watchpoint and trace (DWT)	
0xE000 2000	0xE000 2FFF	Flash patch and breakpoint (FPB)	
0xE000 E000	0xE000 EFFF	NVIC	
0xE004 0000	0xE004 0FFF	Trace port interface unit (TPIU)	
0xE004 1000	0xE004 1FFF	Reserved for embedded trace macrocell (ETM)	
0xE004 2000	0xE00F FFFF	Reserved	

8.8 Restoring Factory Default Configuration

The device has an internal recovery mechanism that allows rolling back the file system to its predefined factory image or restoring the factory default parameters of the device. The factory image is kept in a separate sector on the serial flash in a secure manner and cannot be accessed from the host processor. The following restore modes are supported:

- None – no factory restore settings
- Enable restore of factory default parameters
- Enable restore of factory image and factory default parameters

The restore process is performed by calling software APIs, or by pulling or forcing SOP[2:0] = 110 pins and toggling the nRESET pin from low to high.

The process is fail-safe and resumes operation if a power failure occurs before the restore is finished. The restore process typically takes about 8 seconds, depending on the attributes of the serial flash vendor.

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8.9 Boot Modes

8.9.1 Boot Mode List

The CC3230x device implements a sense-on-power (SOP) scheme to determine the device operation mode.

SOP values are sensed from the device pin during power-up. This encoding determines the boot flow. Before the device is taken out of reset, the SOP values are copied to a register and used to determine the device operation mode while powering up. These values determine the boot flow as well as the default mapping (to JTAG, SWD, UART0) for some of the pins. Table 8-6 lists the pull configurations.

Table 8-6. CC3230x Functional Configurations

BOOT MODE NAME	SOP[2]	SOP[1]	SOP[0]	SOP MODE	COMMENT
UARTLOAD	Pullup	Pulldown	Pulldown	LDfrUART	Factory, lab flash, and SRAM loads through the UART. The device waits indefinitely for the UART to load the code. The SOP bits then must be toggled to configure the device in functional mode. Also puts JTAG in 4-wire mode.
FUNCTIONAL_2WJ	Pulldown	Pulldown	Pullup	Fn2WJ	Functional development mode. In this mode, a 2-pin SWD is available to the developer. TMS and TCK are available for debugger connection.
FUNCTIONAL_4WJ	Pulldown	Pulldown	Pulldown	Fn4WJ	Functional development mode. In this mode, a 4-pin JTAG is available to the developer. TDI, TMS, TCK, and TDO are available for debugger connection.
UARTLOAD_FUNCTIONAL_4WJ	Pulldown	Pullup	Pulldown	LDfrUART_Fn4WJ	Supports flash and SRAM load through UART and functional mode. The MCU bootloader tries to detect a UART break on the UART receive line. If the break signal is present, the device enters the UARTLOAD mode, otherwise, the device enters the functional mode. TDI, TMS, TCK, and TDO are available for debugger connection.
RET_FACTORY_IMAGE	Pulldown	Pullup	Pullup	RetFactDef	When the device reset is toggled, the MCU bootloader kick-starts the procedure to restore factory default images.

The recommended values of pulldown resistors are 100kΩ for SOP0 and SOP1 and 2.7kΩ for SOP2. The application can use SOP2 for other functions after the device has powered up. However, to avoid spurious SOP values from being sensed at power up, TI strongly recommends using the SOP2 pin only for output signals. The SOP0 and SOP1 pins are multiplexed with the WLAN analog test pins and are not available for other functions.

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8.10 Hostless Mode

The SimpleLink Wi-Fi CC3230 device incorporates a scripting ability that enables offloading of simple tasks from the host processor. Using simple and conditional scripts, repetitive tasks can be handled internally, which allows the host processor to remain in a low-power state. In some cases where the scripter is being used to send packets, it reduces code footprint and memory consumption. The *if-this-then-that* style of conditioning can include anything from GPIO toggling to transmitting packets.

The conditional scripting abilities can be divided into conditions and actions. The conditions define when to trigger actions. Only one action can be defined per condition, but multiple instances of the same condition may be used, so in effect, multiple actions can be defined for a single condition. In total, 16 condition and action pairs can be defined. The conditions can be simple, or complex using sub-conditions (using a combinatorial AND condition between them). The actions are divided into two types, those that can occur during runtime and those that can occur only during the initialization phase.

The following actions can only be performed when triggered by the pre-initialization condition:

- Set roles AP, station, P2P, and Tag modes
- Delete all stored profiles
- Set connection policy
- Hardware GPIO indication allows an I/O to be driven directly from the WLAN core hardware to indicate internal signaling

The following actions may be activated during runtime:

- Send transceiver packet
- Send UDP packet
- Send TCP packet
- Increment counter increments one of the user counters by 1
- Set counter allows setting a specific value to a counter
- Timer control
- Set GPIO allows GPIO output from the device using the internal networking core
- Enter Hibernate state

Note

Consider the following limitations:

- Timing cannot be ensured when using the network scripter because some variable latency will apply depending on the utilization of the networking core.
- The scripter is limited to 16 pairs of conditions and reactions.
- Both timers and counters are limited to 8 instances each. Timers are limited to a resolution of 1 second. Counters are 32 bits wide.
- Packet length is limited to the size of one packet and the number of possible packet tokens is limited to 8.

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9 Applications, Implementation, and Layout

Note

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 BLE/2.4 GHz Radio Coexistence

The CC3230x device is designed to support BLE/2.4GHz radio coexistence. Because WLAN is inherently more tolerant to time-domain disturbances, the coexistence mechanism gives priority to the Bluetooth® low energy entity over the WLAN.

The following coexistence modes can be configured by the user:

- Off mode or intrinsic mode
  - No BLE/2.4 GHz radio coexistence, or no synchronization between WLAN and Bluetooth® low energy—in case Bluetooth® low energy exists in this mode, collisions can randomly occur.
- Time division multiplexing (TDM, single antenna)
  - In this mode, (see Figure 9-1) the two entities share the antenna through an RF switch using two GPIOs (one input and one output from the WLAN perspective).
- Time division multiplexing (TDM, dual antenna)
  - In this mode, (see Figure 9-2) the two entities have separate antennas, no RF switch is required, and only a single GPIO (on input from the WLAN perspective).

Figure 9-1 shows the single antenna implementation of a complete Bluetooth® low energy and WLAN coexistence network. The Coex switch is controlled by a GPIO signal from the BLE device and a GPIO signal from the CC3230x device.

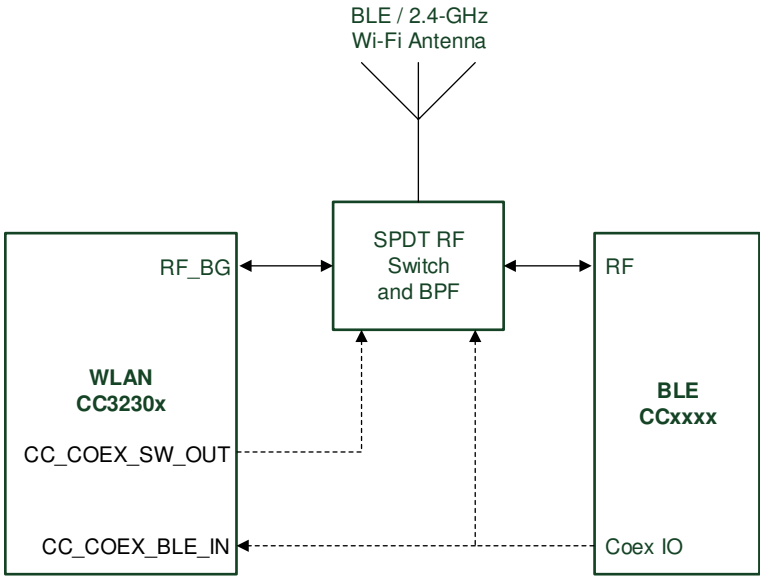

Figure 9-1. Single-Antenna Coexistence Mode Block Diagram

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Figure 9-2 shows the dual antenna implementation of a complete Bluetooth low energy and WLAN coexistence network. Note in this implementation no Coex switch is required and only a single GPIO from the BLE device to the CC3230x device is required.

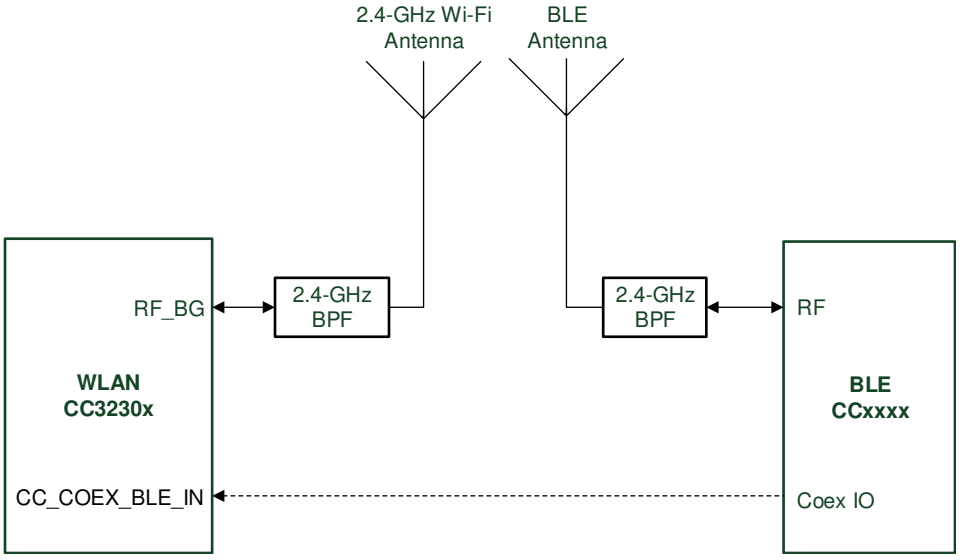

Figure 9-2. Dual-Antenna Coexistence Mode Block Diagram

9.1.2 Antenna Selection

The CC3230x device is designed to also support antenna selection and is controlled from Image Creator. When enabled, there are 3 options possible options:

- ANT 1: When selected, the GPIOs that are defined for antenna selection with set the RF path for antenna 1.
- ANT 2: When selected, the GPIOs that are defined for antenna selection will set the RF path for antenna 2.
- Autoselect: When selected, during a scan and prior to connecting to an AP, CC3230x device will determine the best RF path and select the appropriate antenna [5] [6]. The result is the saved as port of the profile.

Figure 9-3 shows the implementation of a complete Bluetooth® low energy and WLAN coexistence network with WLAN and antenna selection. The Coex switch is controlled by a GPIO signal from the BLE device and a GPIO signal from the CC3230x device. The antenna switch is controlled by 2 GPIO lines from the CC3230x device.

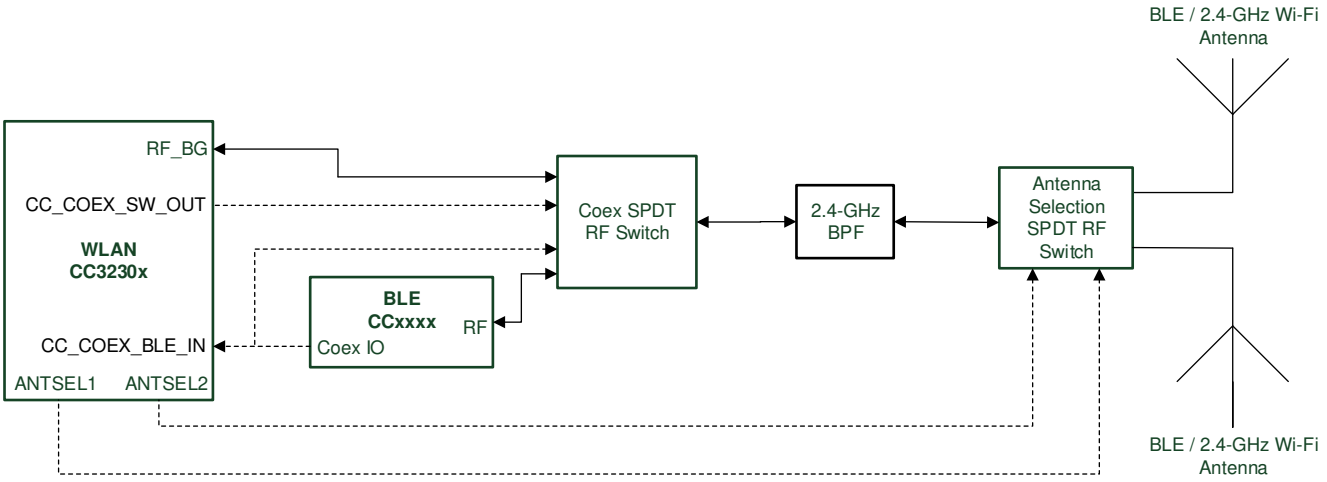

Figure 9-3. Antenna Selection Solution with Coexistence

[5] When selecting Autoselect via the API, a reset is required in order for the CC3230x device to determine the best antenna for use.
[6] Refer to the *UniFlash CC3x20, CC3x35 SimpleLink™ Wi-Fi® and Internet-on-a chip™ Solution ImageCreator and Programming Tool User's Guide* for more information.

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Figure 9-4 shows the antenna selection implementation for Wi-Fi, with BLE operating on it's own antenna. Note in this implementation no Coex switch is required and only a single GPIO from the BLE device to the CC3230x device is required. The antenna switch is controlled by 2 GPIO lines from the CC3230x device.

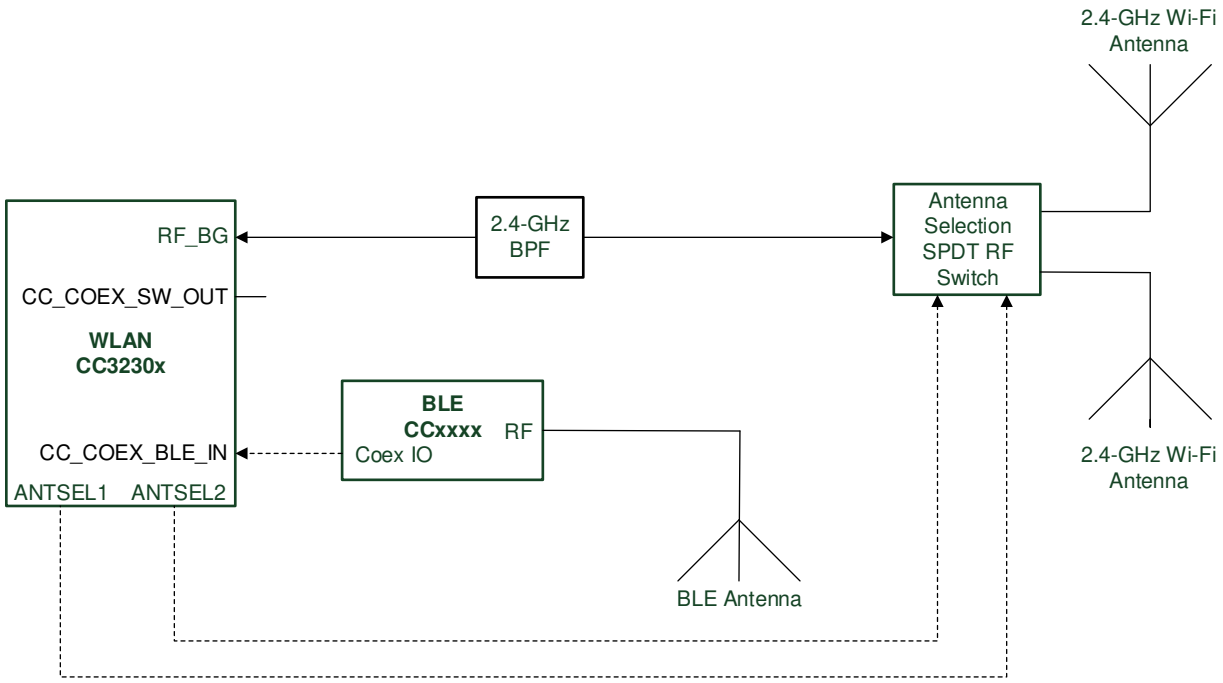

Figure 9-4. Coexistence Solution with Wi-Fi Antenna Selection and Dedicated BLE Antenna

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9.1.3 Typical Application

Figure 9-5 shows the schematic of the engine area for the CC3230x device in the wide-voltage mode of operation, and the optional RF implementations with BLE/2.4GHz coexistence. The corresponding bill-of-materials show in Table 9-1. For a full operation reference design, see the *CC3235x SimpleLink™ and Internet of Things Hardware Design Files*.

Note

The Following guidelines are recommended for implementation of the RF design:

- Ensure an RF path is designed with an impedance of 50Ω

  .
- Tuning of the antenna impedance π matching network is recommended after manufacturing of the PCB to account for PCB parasitics.
- π or L matching and tuning may be required between cascaded passive components on the RF path.

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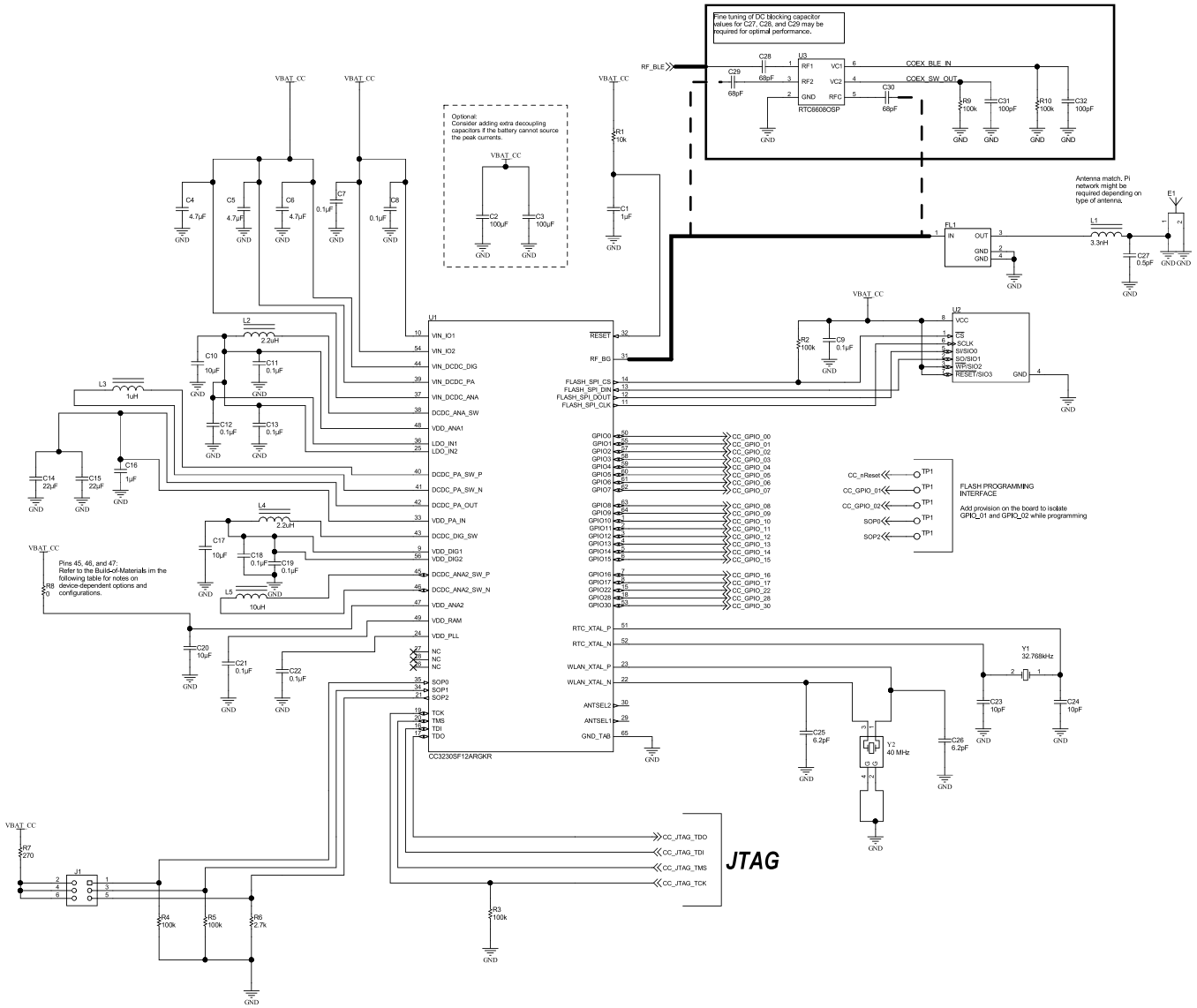

Figure 9-5. CC3230x Engine Area and Optional BLE Coexistence

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Table 9-1. Bill-of-Materials for CC3230x Engine Area and Optional Coexistence

QUANTITY	DESIGNATOR	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
1	C1	1 µF	MuRata	GRM155R61A105KE15D	Capacitor, Ceramic, 1 µF, 10 V, ±10%, X5R, 0402
2	C2, C3	100 µF	Taiyo Yuden	LMK325ABJ107MMHT	Capacitor, Ceramic, 100 µF, 10 V, ±20%, X5R, 1210
3	C4, C5, C6	4.7 µF	TDK	C1005X5R0J475M050BC	Capacitor, Ceramic, 4.7 µF, 6.3 V, ±20%, X5R, 0402
10	C7, C8, C9, C11, C12, C13, C18, C19, C21, C22	0.1 µF	TDK	C1005X5R1A104K050BA	Capacitor, Ceramic, 0.1 µF, 10 V, ±10%, X5R, 0402
3	C10, C17, C20	10 µF	MuRata	GRM188R60J106ME47D	Capacitor, Ceramic, 10 µF, 6.3 V, ±20%, X5R, 0603
2	C14, C15	22 µF	TDK	C1608X5R0G226M080AA	Capacitor, Ceramic, 22 µF, 4 V, ±20%, X5R, 0603
1	C16	1 µF	TDK	C1005X5R1A105K050BB	Capacitor, Ceramic, 1 µF, 10 V, ±10%, X5R, 0402
2	C23, C24	10 pF	MuRata	GRM1555C1H100JA01D	Capacitor, Ceramic, 10 pF, 50 V, ±5%, C0G/NP0, 0402
2	C25, C26	6.2 pF	MuRata	GRM1555C1H6R2CA01D	Capacitor, Ceramic, 6.2 pF, 50 V, ±5%, C0G/NP0, 0402
1	C27	0.5 pF	MuRata	GRM1555C1HR50BA01D	Capacitor, Ceramic, 0.5 pF, 50 V, ±20%, C0G/NP0, 0402
3	C28(3), C29(3), C30(3)	68 pF	MuRata	GRM0335C1H680JA1D	CAP, CERM, 68 pF, 50 V, +/- 5%, C0G/NP0, 0201
2	C31(3), C32(3)	100 pF	Yageo	CC0201JRNPO8BN101	CAP, CERM, 100 pF, 25 V, +/- 5%, C0G/NP0, 0201
1	E1	2.45-GHz Antenna	Taiyo Yuden	AH316M245001-T	ANT Bluetooth W-LAN Zigbee®, SMD
1	FL1	1.02 dB	TDK	DEA202450BT-1294C1-H	Multilayer Chip Band Pass Filter For 2.4 GHz W-LAN/Bluetooth, SMD
1	L1	3.3 nH	MuRata	LQG15HS3N3S02D	Inductor, Multilayer, Air Core, 3.3 nH, 0.3 A, 0.17 ohm, SMD
2	L2, L4	2.2 µH	MuRata	LQM2HPN2R2MG0L	Inductor, Multilayer, Ferrite, 2.2 µH, 1.3 A, 0.08 ohm, SMD
1	L3	1 µH	MuRata	LQM2HPN1R0MG0L	Inductor, Multilayer, Ferrite, 1 µH, 1.6 A, 0.055 ohm, SMD
1	L5(1)	10 µH	Taiyo Yuden	CBC2518T100M	Inductor, Wirewound, Ceramic, 10 µH, 0.48 A, 0.36 ohm, SMD
1	R1	10 k	Vishay-Dale	CRCW040210K0JNED	Resistor, 10 k, 5%, 0.063 W, 0402

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Table 9-1. Bill-of-Materials for CC3230x Engine Area and Optional Coexistence (continued)

QUANTITY	DESIGNATOR	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
6	R2, R3, R4, R5, R9(3), R10(3)	100 k	Vishay-Dale	CRCW0402100KJNED	Resistor, 100 k, 5%, 0.063 W, 0402
1	R6	2.7 k	Vishay-Dale	CRCW04022K70JNED	Resistor, 2.7 k, 5%, 0.063 W, 0402
1	R7	270	Vishay-Dale	CRCW0402270RJNED	Resistor, 270, 5%, 0.063 W, 0402
1	R8(2)	0	Panasonic	ERJ-2GE0R00X	Resistor, 0, 5% 0.063W, 0402
1	U1	MX25R	Macronix International Co., LTD	MX25R3235FM1IL0	Ultra-Low Power, 32-Mbit [x 1/x 2/x 4] CMOS MXSMIO (Serial Multi I/O) Flash Memory, SOP-8
1	U2	CC3230	Texas Instruments	CC3230SF12RGK	SimpleLink™ Wi-Fi® and internet-of-things Solution, a Single-Chip Wireless MCU, RGK0064B
1	U3(3)	SPDT Switch	Richwave	RTC6608OSP	0.03 GHz-6 GHz SPDT Switch
1	Y1	Crystal	Abracon Corportation	ABS07-32.768KHZ-9-T	Crystal, 32.768 KHz, 9PF, SMD
1	Y2	Crystal	Epson	Q24FA20H0039600	Crystal, 40 MHz, 8pF, SMD

(1) For the CC3230SF device, L5 is populated. For the CC3230S device, L5 is not populated.
(2) For the CC3230SF device, R8 is not populated. For the CC3230S device if R8 is populated, Pin 45 can be used as GPIO_31.
(3) If the BLE/2.4GHz Coexistence features is not used, these components are not required.

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9.2 PCB Layout Guidelines

This section details the PCB guidelines to speed up the PCB design using the CC3230x VQFN device. Follow these guidelines ensures that the design will minimize the risk with regulatory certifications including FCC, ETSI, and CE. For more information, see *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines*.

9.2.1 General PCB Guidelines

Use the following PCB guidelines:

- Verify the recommended PCB stackup in the PCB design guidelines, as well as the recommended layers for signals and ground.
- Ensure that the VQFN PCB footprint follows the information in .
- Ensure that the VQFN PCB GND and solder paste follow the recommendations provided in *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines*.
- Decoupling capacitors must be as close as possible to the VQFN device.

9.2.2 Power Layout and Routing

Three critical DC/DC converters must be considered for the CC3230x device.

- Analog DC/DC converter
- PA DC/DC converter
- Digital DC/DC converter

Each converter requires an external inductor and capacitor that must be laid out with care. DC current loops are formed when laying out the power components.

9.2.2.1 Design Considerations

The following design guidelines must be followed when laying out the CC3230x device:

- Ground returns of the input decoupling capacitors (C11, C13, and C19) should be routed on Layer 2 using thick traces to isolate the RF ground from the noisy supply ground. This step is also required to meet the IEEE spectral mask specifications.
- Maintain the thickness of power traces to be greater than 12 mils. Take special consideration for power amplifier supply lines (pin 33, 40, 41, and 42), and all input supply pins (pin 37, 39, and 44).
- Ensure the shortest grounding loop for the PLL supply decoupling capacitor (pin 24).
- Place all decoupling capacitors as close to the respective pins as possible.
- Power budget—the CC3230x device can consume up to 450 mA for 3.3 V, 670 mA for 2.1 V, for 24 ms during the calibration cycle.
- Ensure the power supply is designed to source this current without any issues. The complete calibration (TX and RX) can take up to 17 mJ of energy from the battery over a time of 24 ms.
- The CC3230x device contains many high-current input pins. Ensure the trace feeding these pins can handle the following currents:
  - VIN_DCDC_PA input (pin 39) maximum 1 A
  - VIN_DCDC_ANA input (pin 37) maximum 600 mA
  - VIN_DCDC_DIG input (pin 44) maximum 500 mA
  - DCDC_PA_SW_P (pin 40) and DCDC_PA_SW_N (pin 41) switching nodes maximum 1 A
  - DCDC_PA_OUT output node (pin 42) maximum 1 A
  - DCDC_ANA_SW switching node (pin 38) maximum 600 mA
  - DCDC_DIG_SW switching node (pin 43) maximum 500 mA
  - VDD_PA_IN supply (pin 33) maximum 500 mA

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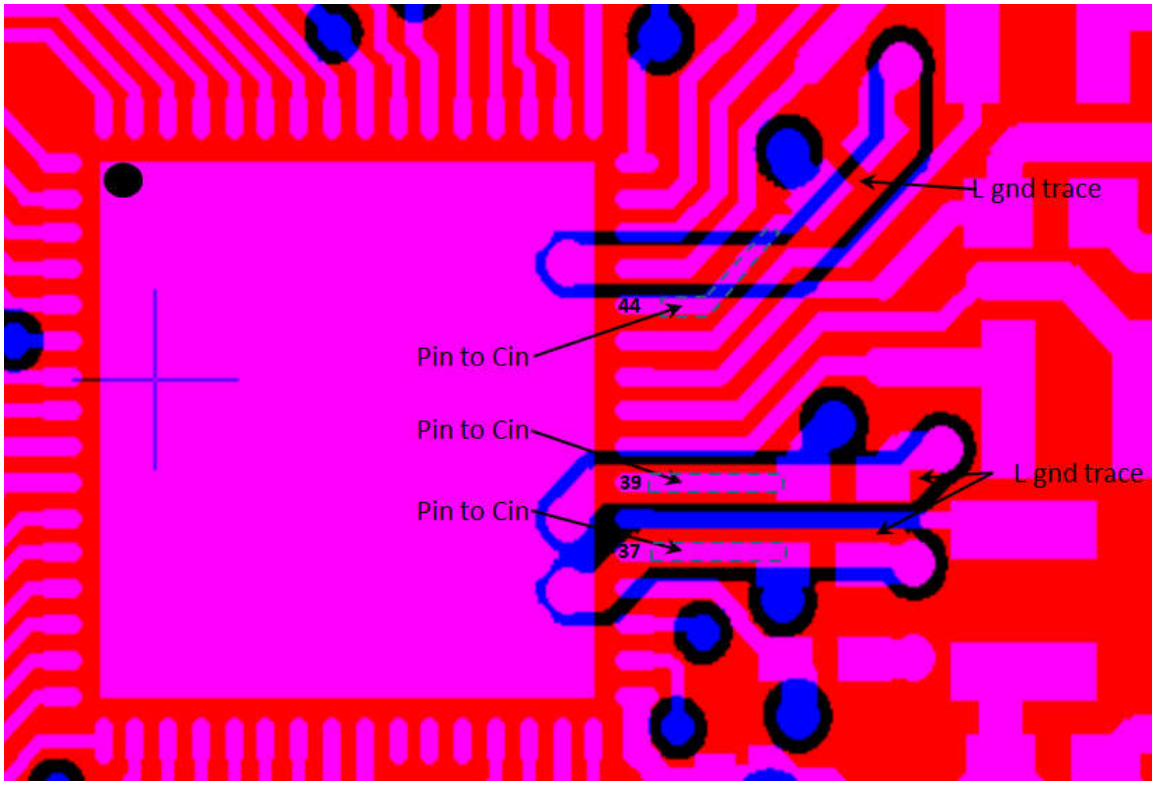

Figure 9-6. Ground Returns for Input Capacitors

9.2.3 Clock Interface Guidelines

The following guidelines are for the slow clock:

- The 32.768kHz crystal must be placed close to the VQFN package.
- Ensure that the load capacitance is tuned according to the board parasitics to the frequency tolerance within ±150ppm.
- The ground plane on layer two is solid below the trace lanes, and there is ground around these traces on the top layer.

The following guidelines are for the fast clock:

- The 40MHz crystal must be placed close to the VQFN package.
- Ensure that the load capacitance is tuned according to the board parasitics to the frequency tolerance within ±10ppm at room temperature. The total frequency across parts, temperature, and with aging must be ±25ppm to meet the WLAN specification.
- To avoid noise degradation, ensure that no high-frequency lines are routed close to the routing of the crystal pins.
- Ensure that crystal tuning capacitors are close to the crystal pads.
- Both traces (XTAL_N and XTAL_P) should be as close as possible to parallel and approximately the same length.
- The ground plane on layer two is solid below the trace lines, and there should be ground around these traces on the top layer.
- For frequency tuning, see *CC31xx & CC32xx Frequency Tuning*.

9.2.4 Digital Input and Output Guidelines

The following guidelines are for the digital I/Os:

- Route SPI and UART lines away from any RF traces.
- Keep the length of the high-speed lines as short as possible to avoid transmission line effects.
- Keep the line lower than 1/10 of the rise time of the signal to ignore transmission line effects (required if the traces cannot be kept short). Place the resistor at the source end closer to the device that is driving the signal.
- Add a series-terminating resistor for each high-speed line (for example, SPI_CLK or SPI_DATA) to match the driver impedance to the line. Typical terminating-resistor values range from 27Ω to 36Ω for a 50Ω line impedance.
- Route high-speed lines with a continuous ground reference plane below it to offer good impedance throughout. This routing also helps shield the trace against EMI.
- Avoid stubs on high-speed lines to minimize the reflections. If the line must be routed to multiple locations, use a separate line driver for each line.
- If the lines are longer compared to the rise time, add series-terminating resistors near the driver for each high-speed line to match the driver impedance to the line. Typical terminating-resistor values range from 27Ω to 36Ω for a 50Ω line impedance.

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9.2.5 RF Interface Guidelines

The following guidelines are for the RF interface. Follow guidelines specified in the vendor-specific antenna design guides (including placement of the antenna). Also see *CC3120 and CC3220 SimpleLink™ Wi-Fi® and IoT Solution Layout Guidelines* for general antenna guidelines.

- Ensure that the antenna is matched for 50Ω. A π-matching network is recommended. Ensure that the π pad is available for tuning the matching network after PCB manufacture.
- Ensure that the area underneath the BPFs pads have a solid plane on layer 2 and that the minimum filter requirements are met.
- Verify that the Wi-Fi RF trace is a 50Ω, impedance-controlled trace with a reference to solid ground.
- The RF trace bends must be made with gradual curves. Avoid 90-degree bends.
- The RF traces must not have sharp corners.
- There must be no traces or ground under the antenna section.
- The RF traces must have via stitching on the ground plane beside the RF trace on both sides.
- For optimal antenna performance, ensure adequate ground plane around the antenna on all layers.
- Ensure RF connectors for conducted testing are isolated from the top layer ground using vias.
- Maintain a controlled pad to trace shapes using filleted edges if necessary to avoid mismatch.

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10 Device and Documentation Support

10.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.2 Tools and Software

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed in this section.

For the most up-to-date list of development tools and software, see the CC3230S Design & development page. Users can also click the "Alert Me" button on the top right corner of the CC3230S Design & development page to stay informed about updates related to the CC3230x device.

Development Tools

Pin Mux Tool	The supported devices are: CC3200, CC3220x, CC3230x, and CC3235x. The Pin Mux Tool is a software tool that provides a graphical user interface (GUI) for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for MPUs from TI. Results are output as C header/code files that can be imported into software development kits (SDKs) or used to configure customers' custom software. Version 3 of the Pin Mux Tool adds the capability of automatically selecting a mux configuration that satisfies the entered requirements.
SimpleLink™ Wi-Fi® Starter Pro	The supported devices are: CC3100, CC3200, CC3120R, CC3220x, CC3130, CC3135, CC3230x and CC3235x. The SimpleLink™ Wi-Fi® Starter Pro mobile App is a new mobile application for SimpleLink™ provisioning. The app goes along with the embedded provisioning library and example that runs on the device side (see *SimpleLink™ Wi-Fi® SDK plugin* and *TI SimpleLink™ CC32XX Software Development Kit (SDK)*). The new provisioning release is a TI recommendation for Wi-Fi® provisioning using SimpleLink™ Wi-Fi® products. The provisioning release implements advanced AP mode and SmartConfig™ technology provisioning with feedback and fallback options to ensure successful process has been accomplished. Customers can use both embedded library and the mobile library for integration to their end products.
SimpleLink™ CC32XX Software Development Kit (SDK)	The CC3230x devices are supported. The SimpleLink™ CC32XX SDK contains drivers for the CC3230 programmable MCU, more than 30 sample applications, and documentation needed to use the solution. It also contains the flash programmer, a command line tool for flashing software, configuring network and software parameters (SSID, access point channel, network profile, BS NIEW), system files, and user files (certificates, web pages, and more). This SDK can be used with TI's SimpleLink™ Wi-Fi® CC3230 LaunchPad™ development kits.
Uniflash Standalone Flash Tool for TI Microcontrollers (MCU), Sitara Processors & SimpleLink Devices	The supported devices are: CC3120R, CC3220x, CC3130, CC3135, CC3230x and CC3235x. CCS Uniflash is a standalone tool used to program on-chip flash memory on TI MCUs and on-board flash memory for Sitara™ processors. Uniflash has a GUI, command line, and scripting interface. CCS Uniflash is available free of charge.

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SimpleLink™ Wi-Fi® Radio Testing Tool	The supported devices are: CC3100, CC3200, CC3120R, CC3220, CC3130, CC3135, CC3230x and CC3235x. The SimpleLink™ Wi-Fi® Radio Testing Tool is a Windows-based software tool for RF evaluation and testing of SimpleLink™ Wi-Fi® CC3x20 and CC3x3x designs during development and certification. The tool enables low-level radio testing capabilities by manually setting the radio into transmit or receive modes. Using the tool requires familiarity and knowledge of radio circuit theory and radio test methods. Created for the internet-of-things (IoT), the SimpleLink™ Wi-Fi® CC31xx and CC32xx family of devices include on-chip Wi-Fi®, Internet, and robust security protocols with no prior Wi-Fi® experience needed for faster development. For more information on these devices, visit SimpleLink™ Wi-Fi® family, Internet-on-a chip™ solutions.
UniFlash Standalone Flash Tool for TI Microcontrollers (MCU), Sitara™ Processors and SimpleLink™ Devices	CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs and on-board flash memory for Sitara™ processors. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

TI Reference Designs

Find reference designs leveraging the best in TI technology – from analog and power management to embedded processors. All designs include a schematic, test data and design files.

10.3 Firmware Updates

TI updates features in the service pack for this module with no published schedule. Due to the ongoing changes, TI recommends that the user has the latest service pack in their module for production.

To stay informed, click the SDK “Alert me” button the top right corner of the product page, or visit *SimpleLink™ CC32XX SDK*.

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10.4 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of the CC3230x device and support tools (see Figure 10-1).

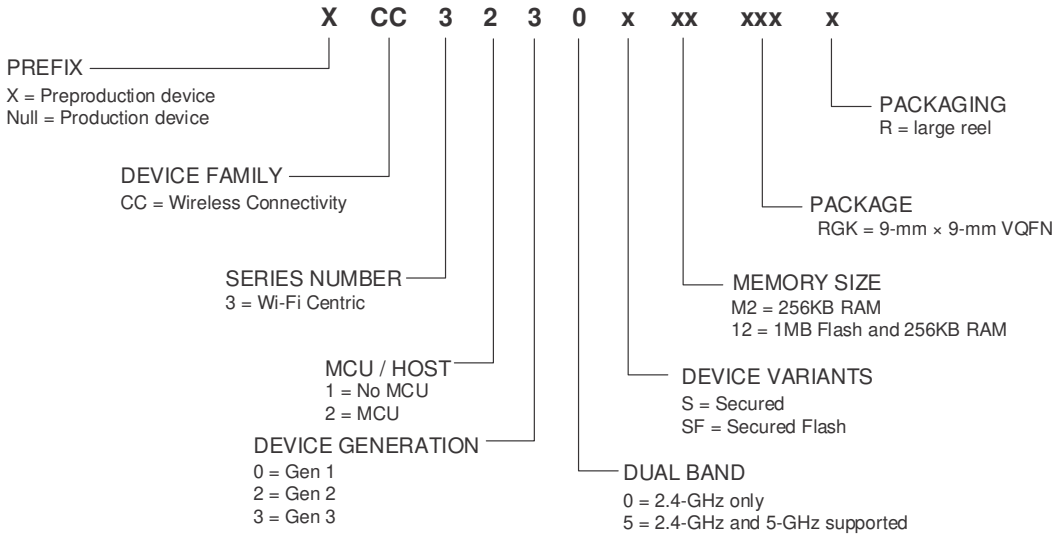

Figure 10-1. CC3230x Device Nomenclature

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10.5 Documentation Support

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for example, CC3230S). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document. The current documentation that describes the processor, related peripherals, and other technical collateral follows.

The following documents provide support for the CC3230 device.

Application Reports

CC3135 and CC3235 SimpleLink™ Wi-Fi® Embedded Programming User Guide	CC3135 and CC3235 SimpleLink Wi-Fi Embedded Programming User Guide
SimpleLink™ CC3135, CC3235 Wi-Fi® Internet-on-a chip™ Networking Sub-System Power Management	This application report describes the best practices for power management and extended battery life for embedded low-power Wi-Fi devices such as the SimpleLink Wi-Fi Internet-on-a chip solution from Texas Instruments.
SimpleLink™ CC31xx, CC32xx Wi-Fi® Internet-on-a chip™ Solution Built-In Security Features	The SimpleLink Wi-Fi CC31xx and CC32xx Internet-on-a chip family of devices from Texas Instruments offer a wide range of built-in security features to help developers address a variety of security needs, which is achieved without any processing burden on the main microcontroller (MCU). This document describes these security-related features and provides recommendations for leveraging each in the context of practical system implementation.
SimpleLink™ CC3135, CC3235 Wi-Fi® and Internet-of-Things Over-the-Air Update	This document describes the OTA library for the SimpleLink Wi-Fi CC3x35 family of devices from Texas Instruments and explains how to prepare a new cloud-ready update to be downloaded by the OTA library.
SimpleLink™ CC3135, CC3235 Wi-Fi® Internet-on-a chip™ Solution Device Provisioning	This guide describes the provisioning process, which provides the SimpleLink Wi-Fi device with the information (network name, password, and so forth) needed to connect to a wireless network.
Transfer of TI's Wi-Fi® Alliance Certifications to Products Based on SimpleLink™	This document explains how to employ the Wi-Fi® Alliance (WFA) derivative certification transfer policy to transfer a WFA certification, already obtained by Texas Instruments, to a system you have developed.
Using Serial Flash on SimpleLink™ CC3135 and CC3235 Wi-Fi® and Internet-of-Things Devices	This application note is divided into two parts. The first part provides important guidelines and best- practice design techniques to consider when choosing and embedding a serial Flash paired with the CC3135 and CC3235 (CC3x35) devices. The second part describes the file system, along with guidelines and considerations for system designers working with the CC3x35 devices.

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User's Guides

SimpleLink™ Wi-Fi® and Internet-of-Things CC31xx and CC32xx Network Processor	This document provides software (SW) programmers with all of the required knowledge for working with the networking subsystem of the SimpleLink Wi-Fi devices. This guide provides basic guidelines for writing robust, optimized networking host applications, and describes the capabilities of the networking subsystem. The guide contains some example code snapshots, to give users an idea of how to work with the host driver. More comprehensive code examples can be found in the formal software development kit (SDK). This guide does not provide a detailed description of the host driver APIs.
SimpleLink™ Wi-Fi® CC3135 and CC3235 and IoT Solution Layout Guidelines	This document provides the design guidelines of the 4-layer PCB used for the CC3135 and CC3235 SimpleLink Wi-Fi family of devices from Texas Instruments. The CC3135 and CC3235 devices are easy to lay out and are available in quad flat no-leads (QFNS) packages. When designing the board, follow the suggestions in this document to optimize performance of the board.
SimpleLink™ CC3235 Wi-Fi® LaunchPad™ Development Kit Hardware	The CC3235 SimpleLink LaunchPad Development Kit (LAUNCHXL-CC3235) is a cost-conscious evaluation platform for Arm Cortex-M4-based MCUs. The LaunchPad design highlights the CC3230 Internet-on-a chip solution and Wi-Fi capabilities. The CC3235 LaunchPad also features temperature and accelerometer sensors, programmable user buttons, three LEDs for custom applications, and onboard emulation for debugging. The stackable headers of the CC3235 LaunchPad XL interface demonstrate how easy it is to expand the functionality of the LaunchPad when interfacing with other peripherals on many existing BoosterPack™ Plug-in Module add-on boards, such as graphical displays, audio codecs, antenna selection, environmental sensing, and more.
SimpleLink™ Wi-Fi® and Internet-on-a chip™ CC3135 and CC3235 Solution Radio Tool	The Radio Tool serves as a control panel for direct access to the radio, and can be used for both the radio frequency (RF) evaluation and for certification purposes. This guide describes how to have the tool work seamlessly on Texas Instruments evaluation platforms such as the BoosterPack™ plus FTDI emulation board for CC3230 devices, and the LaunchPad™ for CC3230 devices.
SimpleLink™ Wi-Fi® CC3135 and CC3235 Provisioning for Mobile Applications	This guide describes TI's SimpleLink Wi-Fi provisioning solution for mobile applications, specifically on the usage of the Android™ and IOS® building blocks for UI requirements, networking, and provisioning APIs required for building the mobile application.

More Literature

CC3235 SimpleLink™ Wi-Fi® and Internet of Things Technical Reference Manual	This technical reference manual details the modules and peripherals of the CC3230 SimpleLink™ Wi-Fi® MCU. Each description presents the module or peripheral in a general sense. Not all features and functions of all modules or peripherals may be present on all devices. Pin functions, internal signal connections, and operational parameters differ from device to device. The user should consult the device-specific data sheet for these details.
CC3x35 SimpleLink™ Wi-Fi® Hardware Design Checklist	
CC3235S/CC3235SF SimpleLink™ Wi-Fi® LaunchPad™ Design Files	

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10.6 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.7 Trademarks

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Zigbee® is a registered trademark of Zigbee Alliance.
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10.8 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.9 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

Changes from Revision B (May 2021) to Revision C (August 2024)	Page
• Added the note on the TLS socket for WPA Enterprise security modes in WLAN	62

Changes from September 28, 2020 to May 13, 2021 (from Revision A (September 2020) to Revision B (May 2021))	Page
• Added "WPA3 Enterprise" to Section 1	1
• Added "WPA3 personal and enterprise" to Table 5-1	7
• Changed footnote in Section 8.3	62
• Added "WPA3 personal and enterprise" to Section 8.3	62
• Added "WPA3 Enterprise" to "WLAN features"	62
• Changed table note for Table 8-1	63
• Added "WPA3 personal and enterprise" to Table 8-1	63
• Added standard sections to Section 10	86

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

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12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking(5) (6)
CC3230SM2RGKR	PREVIEW	VQFN	RGK	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	–40 to 85	CC3230SM2
CC3230SF12RGKR	PREVIEW	VQFN	RGK	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	–40 to 85	CC3230SF12

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD: Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(6) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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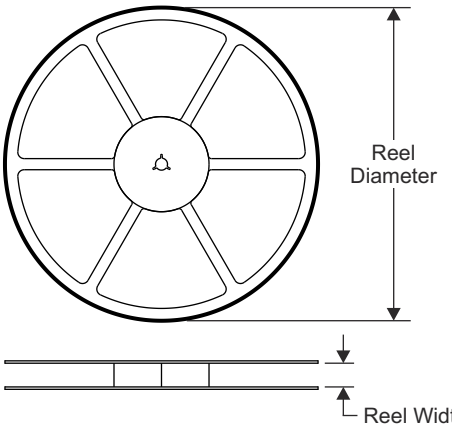
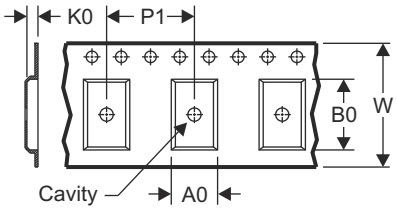
12.1.2 Tape and Reel Information

REEL DIMENSIONS

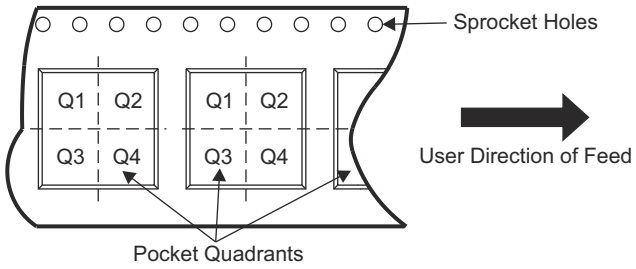


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC3230SM2RGKR	VQFN	RGK	64	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
CC3230SF12RGKR	VQFN	RGK	64	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

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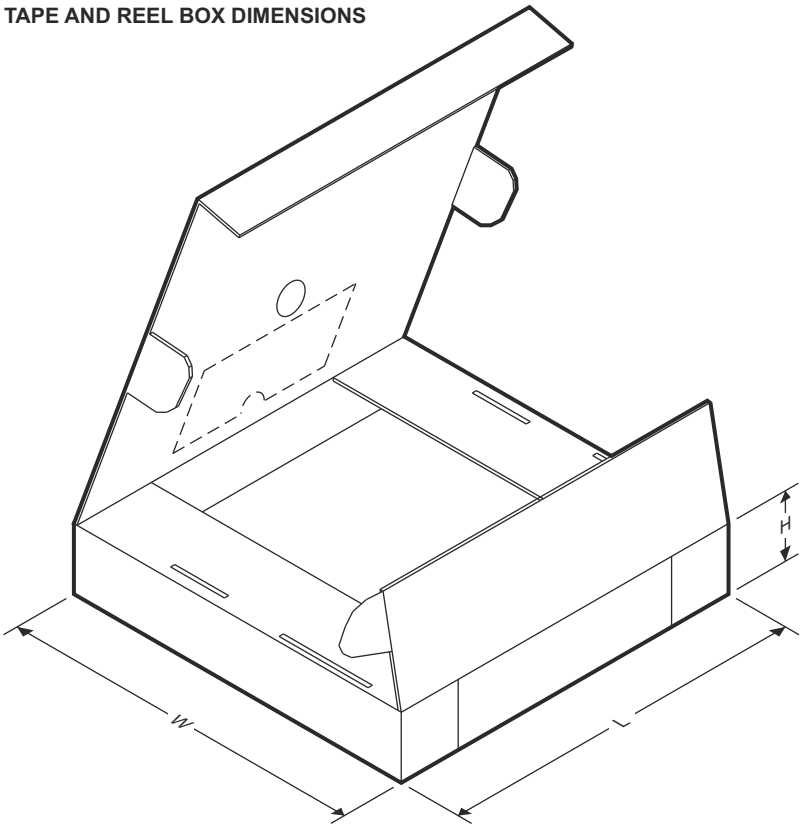
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC3230SM2RGKR	VQFN	RGK	64	2500	367.0	367.0	38.0
CC3230SF12RGKR	VQFN	RGK	64	2500	367.0	367.0	38.0

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CC3230SF12RGKR	Active	Production	VQFN (RGK) | 64	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC3230SF 12
CC3230SM2RGKR	Active	Production	VQFN (RGK) | 64	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC3230S M2
CC3230SM2RGKR.B	Active	Production	VQFN (RGK) | 64	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CC3230S M2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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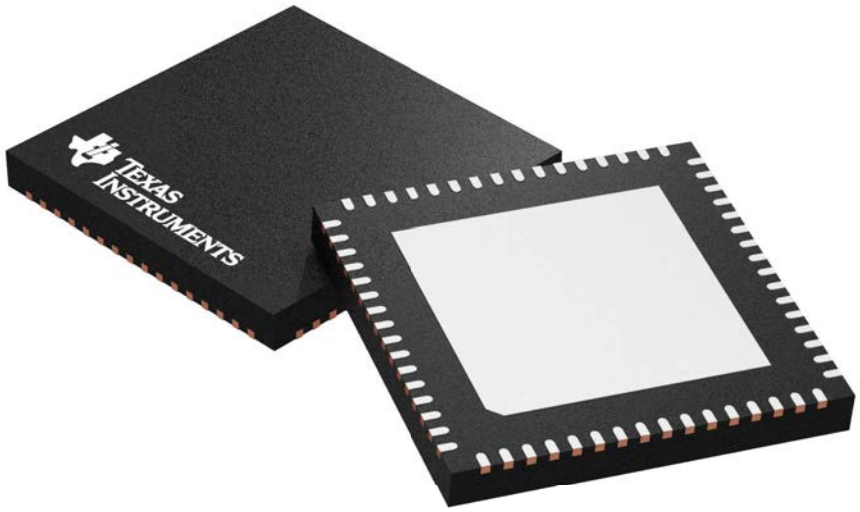
RGK 64

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



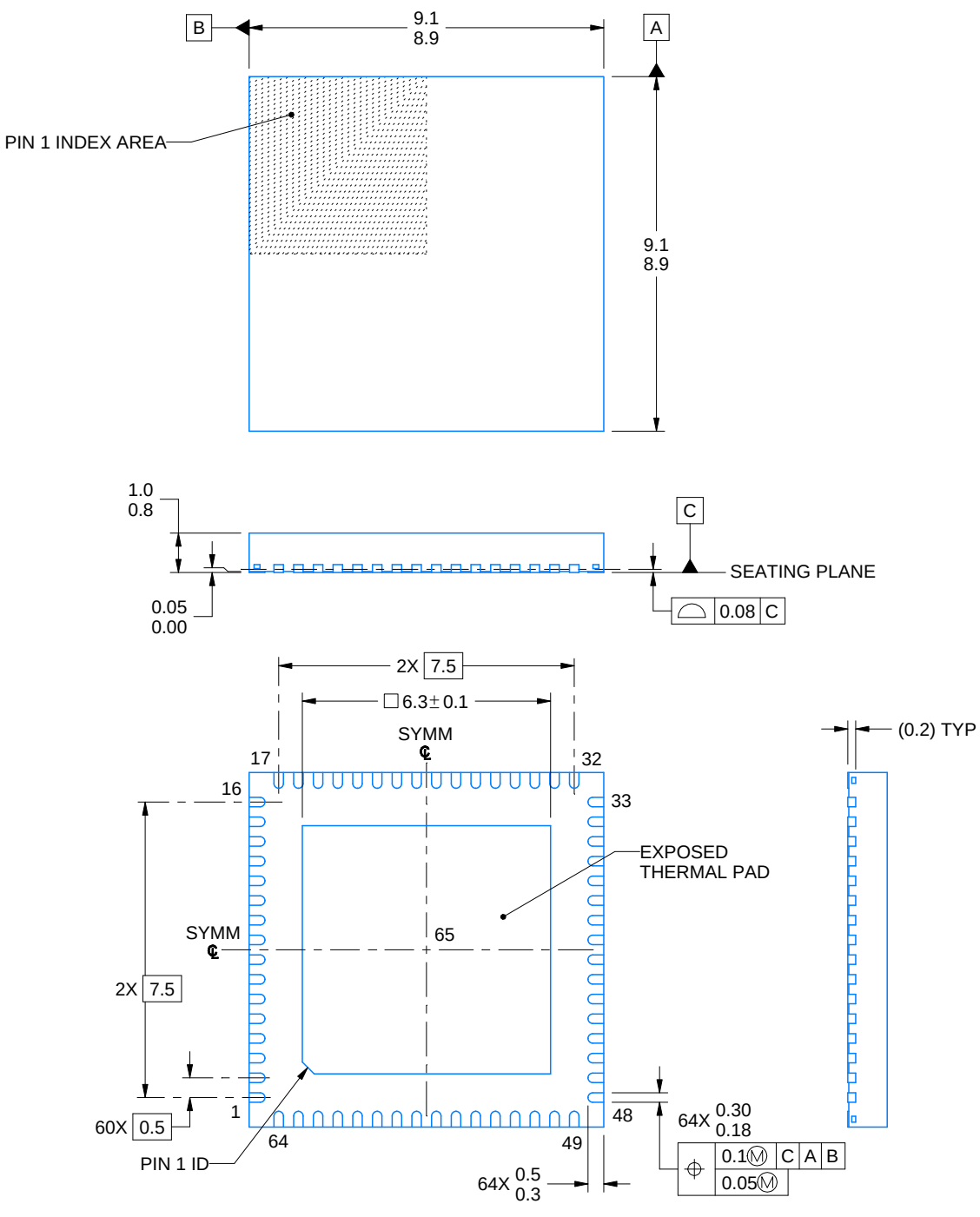
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGK0064B

PACKAGE OUTLINE

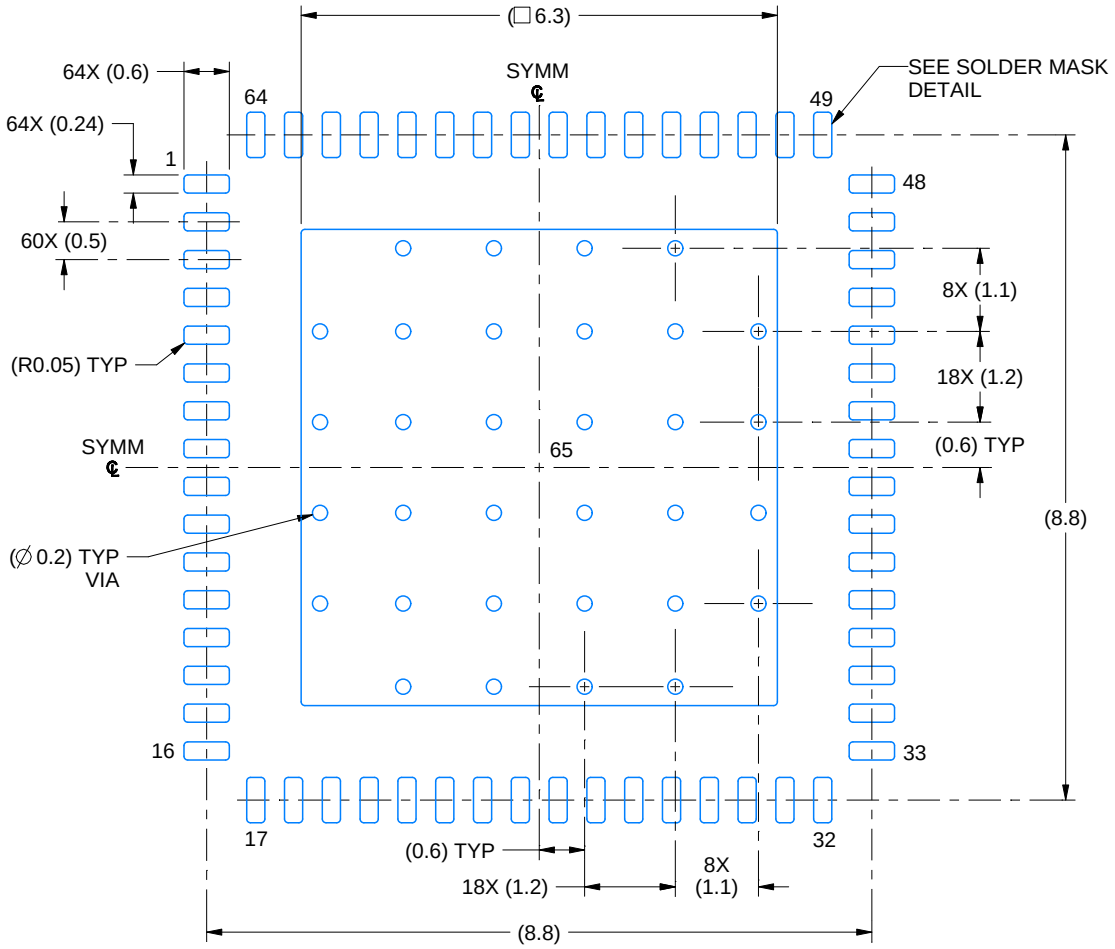
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

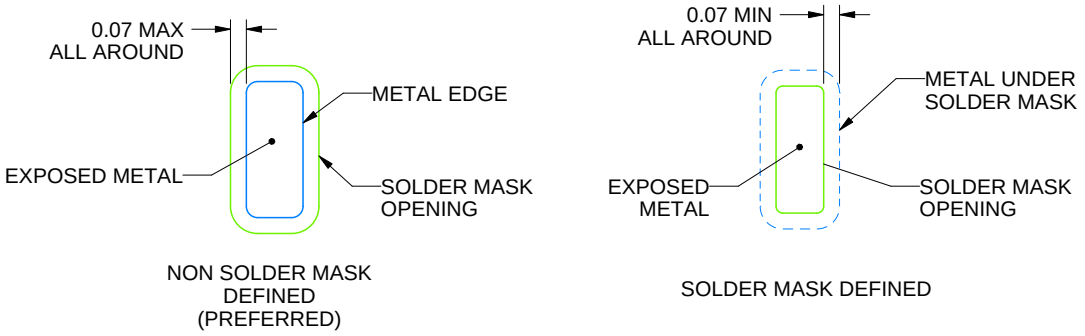


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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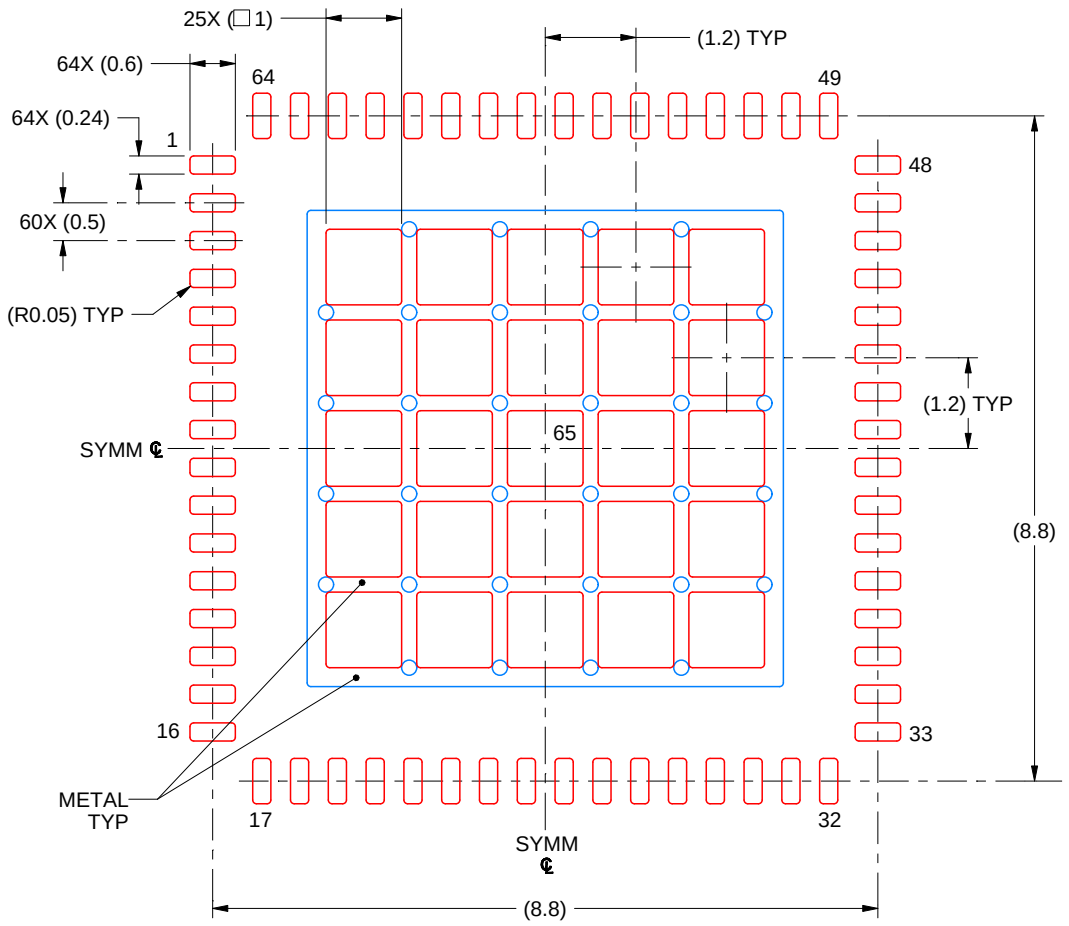
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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