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CYW20735B1

Single-Chip Bluetooth Transceiver for Wireless Input Devices

The Cypress CYW20735B1 is a Bluetooth 5.0-compliant, SoC for IoT applications. Manufactured using the industry's advanced 40 nm CMOS low-power process, the CYW20735B1 employs high levels of integration to minimize external components, reducing the device footprint and the costs associated with implementing Bluetooth solutions.

The CYW20735B1 is the optimal solution for applications in wireless input devices including game controllers, remote controls, keyboards, and joysticks or any Bluetooth connected IoT application that needs 12 dBm transmit power such as lighting.

Features

Bluetooth Subsystem

- Complies with Bluetooth core specification version 5.0 with LE 2-Mbps support
- Supports Basic Rate (BR) and Bluetooth Low Energy (BLE)
- Supports Adaptive Frequency Hopping (AFH)
- Programmable TX power up to 12 dBm
- Rx sensitivity -94.5 dBm (BLE)
- Ultra-low-power radio
  - RX current 8 mA
  - TX current 18 mA @ 12 dBm

Coexistence Support

- Support for Global Coexistence Interface for easy coexistence implementation with select Cypress Wi-Fi devices

MCU Subsystem

- 96-MHz ARM Cortex-M4 microcontroller unit MCU with floating point unit (FPU)
- Supports serial wire debug (SWD)
- Runs Bluetooth stack and application

Memory Subsystem

- 384 KB RAM
- 2 MB ROM that stores Bluetooth stack and drives and offloads flash for user applications

Audio features and interfaces

- 1x I2S with master and slave modes
- 1x PCM
- PDM
- Analog front end for analog microphone

Clocks

- On-chip 32 kHz oscillator
- On-chip 128 kHz oscillator
- 32 kHz crystal oscillator
- 24 MHz crystal oscillator
- 32-bit real time clock (RTC)

Peripherals and Communication

- 6x 16-bit PWMs
- Programmable key-scan matrix interface, up to 8x20 key-scanning matrix
- Quadrature decoder
- Watchdog timer
- 1x peripheral UART, 1x UART for programming and HCI
- 1x SPI (master or salve mode)
- 1x I2C master
- One ADC (10-ENoB for DC measurement and 12-ENOB for Audio measurement)
- Hardware security engine

General Purpose Input Output (GPIO)

- 24 general purpose I/Os
- 2 dedicated pins for analog microphone
- Support 1.7 V to 3.63 V operation
- Four GPIOs support 16 mA and 8 mA source at 3.3 V and 1.8 V respectively

Operating voltage and low-power support

- Wide operating voltage range - 1.625 V to 3.63V
- 4 power modes to implement ultra-low power application - managed by real time operating system
- 1 uA current in HID-Off mode

Packages

- 7 mm x7 mm 60-pin quad flat no-lead (QFN)

Software Support

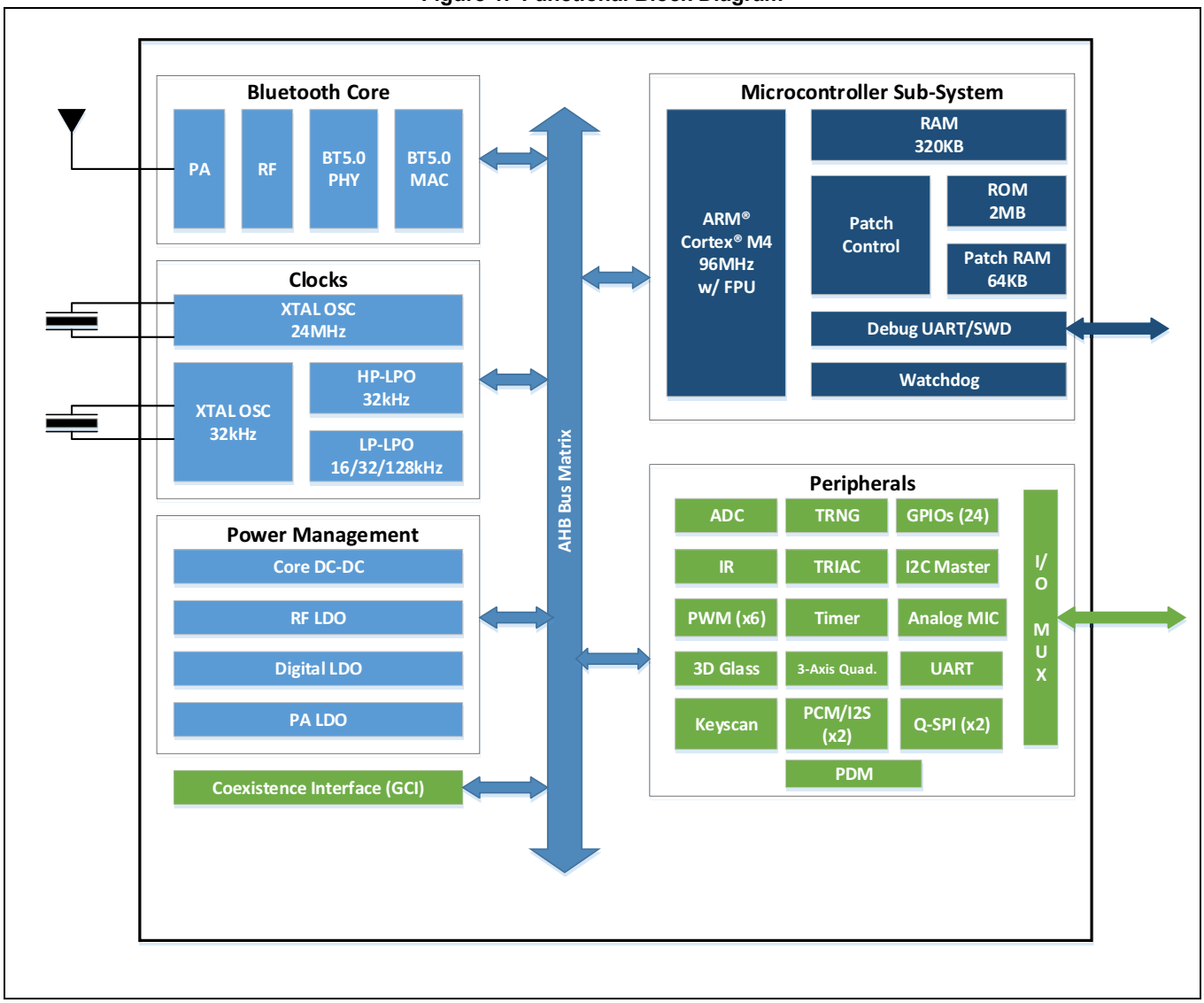
- WICED Studio

Applications

- Game controllers
- Wireless pointing devices (mice)
- Remote controls
- Wireless keyboards
- Joysticks
- Home automation
- Point-of-sale input devices
- 3D glasses
- Blood pressure monitors
- Find-me devices
- Heart-rate monitors
- Proximity sensors
- Thermometers

Functional Block Diagram

Figure 1. Functional Block Diagram



Contents

1. Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules ACL and TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

Table 1. Bluetooth Features

Bluetooth 1.0	Bluetooth 1.2	Bluetooth 2.0
Basic Rate	Interlaced Scans	–
–	Adaptive Frequency Hopping	–
Paging and Inquiry	–	–
Page and Inquiry Scan	–	–
Sniff	–	–
Bluetooth 2.1	**Bluetooth 3.0**	**Bluetooth 4.0**
Secure Simple Pairing	Unicast Connectionless Data	Bluetooth Low Energy
Enhanced Inquiry Response	Enhanced Power Control	–
Sniff Subrating	–	–
Bluetooth 4.1	**Bluetooth 4.2**	
Low Duty Cycle Advertising	Data Packet Length Extension	
Dual Mode	LE Secure Connection	
LE Link Layer Topology	Link Layer Privacy	

1.1 Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task is performed in a different state or substate in the Bluetooth Link Controller.

- BLE states:
  - Advertising
  - Scanning
  - Connection
- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff

1.2 Test Mode Support

The CYW20735B1 fully supports Bluetooth Test mode as described in Part I:1 of the Specification of the Bluetooth System Version 3.0. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the CYW20735B1 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

1.3 Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number based on the link controller state, Bluetooth clock, and device address.

1.4 Microprocessor Unit

The CYW20735B1 microprocessor unit runs software from the link control (LC) layer up to the host controller interface (HCI). The microprocessor is a Cortex-M4 32-bit RISC processor with embedded ICE-RT debug and serial wire debug (SWD) interface units. The microprocessor also includes 2 MB of ROM memory for program storage and 384 KB of RAM for data scratch-pad.

The internal ROM provides flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower-layer protocol stack is executed from internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and feature additions. The device also supports the integration of user applications and profiles.

1.4.1 Floating Point Unit

CYW20735B1 includes the CM4 single precision IEEE-754 compliant floating point unit. For details see the Cortex-M4 manual.

1.4.2 OTP Memory

The CYW20735B1 includes 2 KB of one-time programmable memory that can be used by the factory to store product-specific information.

Note: Use of OTP requires that a 3V supply be present at all times.

1.4.3 NVRAM Configuration Data and Storage

NVRAM contains configuration information about the customer application, including the following:

- Fractional-N information
- BD_ADDR
- UART baud rate
- SDP service record
- File system information used for code, code patches, or data. The CYW20735B1 uses SPI flash for NVRAM storage.

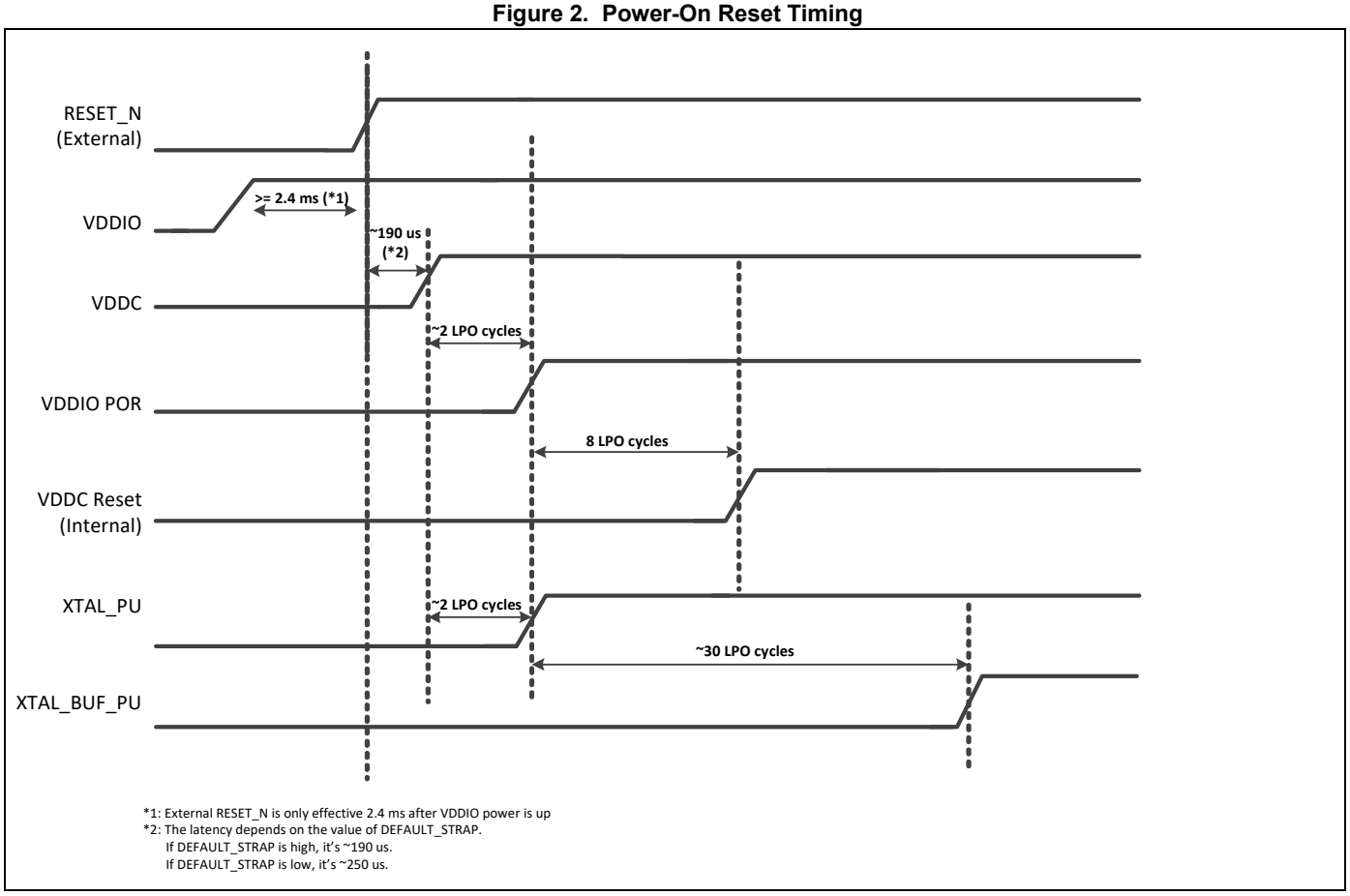
1.4.4 Power-On Reset

The CYW20735B1 includes POR logic to allow the part to initialize correctly when power is applied. Figure 2 shows the sequence used by the CYW20735B1 during initialization. An small external cap may be used on RESET_N to add delay as VDDIO ramps up.

1.4.5 External Reset

An external active-low reset signal, RESET_N, can be used to put the CYW20735B1 in the reset state.

Figure 2. Power-On Reset Timing



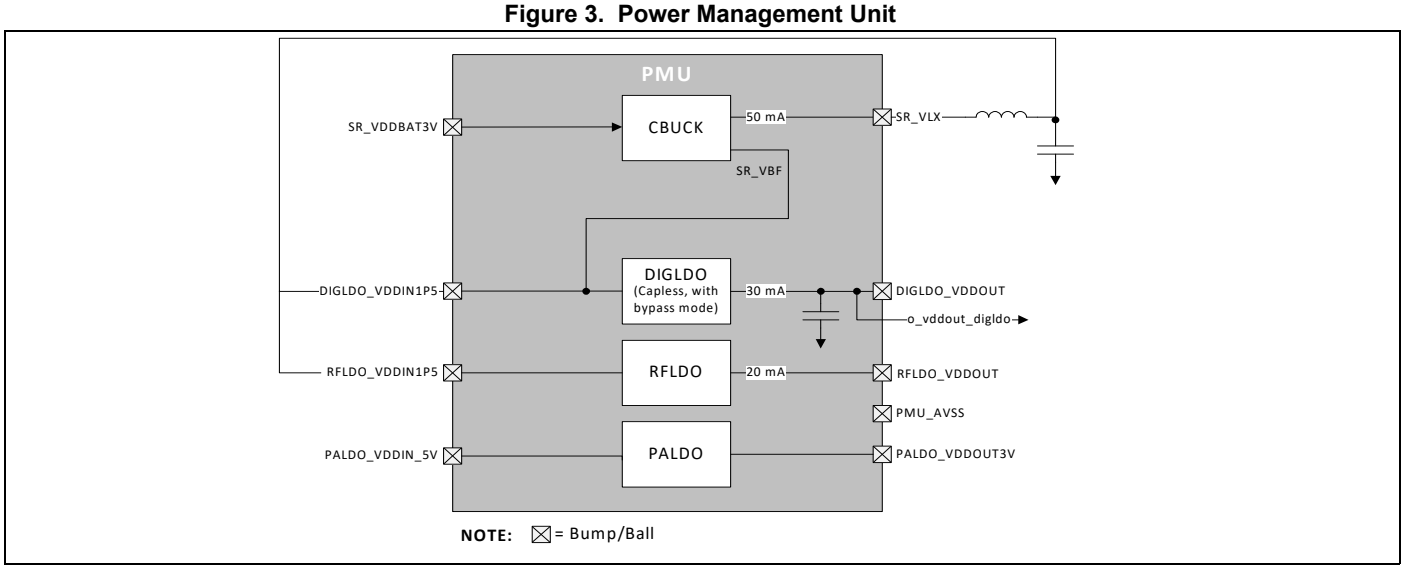
1.4.6 Brownout Detection

An external voltage detector reset IC may be used if brownout detection is required. The reset IC should release RESET_N only after the VDDO supply voltage level has been at or above a minimum operating voltage for
50 ms or longer.

1.5 Power Management Unit

Figure 3 shows the CYW20735B1 power management unit (PMU) block diagram. The CYW20735B1 includes an integrated buck regulator, a capless LDO, PALDO and an additional 1.2V LDO for RF.

Figure 3. Power Management Unit



1.6 Integrated Radio Transceiver

The CYW20735B1 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The CYW20735B1 is fully compliant with the Bluetooth Radio Specification and meets or exceeds the requirements to provide the highest communication link quality of service.

1.6.1 Transmit Path

The CYW20735B1 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4 GHz ISM band.

1.6.2 Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

1.6.3 Power Amplifier

The CYW20735B1 has an integrated power amplifier (PA) that can transmit up to +10 dBm for class 1 operations.

1.6.4 Receiver Path

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the CYW20735B1 to be used in most applications with minimal off-chip filtering.

1.6.5 Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer takes the low-IF received signal and performs an optimal frequency tracking and bit-synchronization algorithm.

1.6.6 Receiver Signal Strength Indicator

The radio portion of the CYW20735B1 provides a receiver signal strength indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

1.6.7 Local Oscillator

A local oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The CYW20735B1 uses an internal loop filter.

1.6.8 Calibration

The CYW20735B1 radio transceiver features a self-contained automated calibration scheme. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration compensates for filter, matching network, and amplifier gain and phase characteristics to yield radio performance within 2% of what is optimal. Calibration takes process and temperature variations into account, and it occurs transparently during normal operation and hop setting times.

1.7 Peripheral Transport Unit

1.7.1 I²C Compatible Master

The CYW20735B1 provides a 2-pin master I²C to communicate with peripherals such as trackball or touch-pad modules, and motion tracking ICs used in mouse devices. The BSC interface is compatible with I²C slave devices. I²C does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported by I²C:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I²C-compatible speed.)
- 1 MHz (Compatibility with high-speed I²C-compatible devices is not guaranteed.)

The following transfer types are supported by BSC:

- Read (Up to 8 bytes can be read.)
- Write (Up to 8 bytes can be written.)
- Read-then-Write (Up to 8 bytes can be read and up to 8 bytes can be written.)
- Write-then-Read (Up to 8 bytes can be written and up to 8 bytes can be read.)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pin (SCL) and data pin (SDA) are both open-drain I/O pins. Pull-up resistors external to the CYW20735B1 are required on both the SCL and SDA pins for proper operation.

1.7.2 HCI UART Interface

The CYW20735B1 includes a UART interface for factory programming and when operating as a BT HCI device in a system with an external host. The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 57600 bps to 6 Mbps. During initial boot, UART speeds may be limited to 750 kbps. The baud rate may be selected via a vendor-specific UART HCI command. The CYW20735B1 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The UART clock default setting is 24 MHz, and can be configured to run as high as 48 MHz to support up to 6 Mbps. The baud rate of the CYW20735B1 UART is controlled by two values. The first is a UART clock divisor (set in the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (set in the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time.

Table 2 on page 10 contains example values to generate common baud rates with a 24 MHz UART clock.

Table 2. Common Baud Rate Examples, 24 MHz Clock

Baud Rate (bps)	Baud Rate Adjustment		Mode	Error (%)
	High Nibble	Low Nibble		
3M	0xFF	0xF8	High rate	0.00
2M	0XFF	0XF4	High rate	0.00
1M	0X44	0XFF	Normal	0.00
921600	0x05	0x05	Normal	0.16
460800	0x02	0x02	Normal	0.16
230400	0x04	0x04	Normal	0.16
115200	0x00	0x00	Normal	0.16
57600	0x00	0x00	Normal	0.16

Table 3 contains example values to generate common baud rates with a 48 MHz UART clock.

Table 3. Common Baud Rate Examples, 48 MHz Clock

Baud Rate (bps)	High Rate	Low Rate	Mode	Error (%)
6M	0xFF	0xF8	High rate	0
4M	0xFF	0xF4	High rate	0
3M	0x0	0xFF	Normal	0
2M	0x44	0xFF	Normal	0
1.5M	0x0	0xFE	Normal	0
1M	0x0	0xFD	Normal	0
921600	0x22	0xFD	Normal	0.16
230400	0x0	0xF3	Normal	0.16
115200	0x1	0xE6	Normal	–0.08
57600	0x1	0xCC	Normal	0.04

Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The CYW20735B1 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±5%.

1.8 Peripheral UART Interface

The CYW20735B1 has a second UART that may be used to interface to peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin. The CYW20735B1 can map the peripheral UART to any LHL GPIO. The peripheral UART clock is fixed at 24 MHz. Both TX and RX have a 256-byte FIFO (see Table 2: “Common Baud Rate Examples, 24 MHz Clock,” on page 11).

1.9 Clock Frequencies

The CYW20735B1 uses a 24 MHz crystal oscillator (XTAL).

1.9.1 Crystal Oscillator

The XTAL must have an accuracy of ±20 ppm as defined by the Bluetooth specification. Two external load capacitors in the range of 5 pF to 30 pF are required to work with the crystal oscillator. The selection of the load capacitors is XTAL-dependent (see Figure 4).

Figure 4. Recommended Oscillator Configuration—12 pF Load Crystal

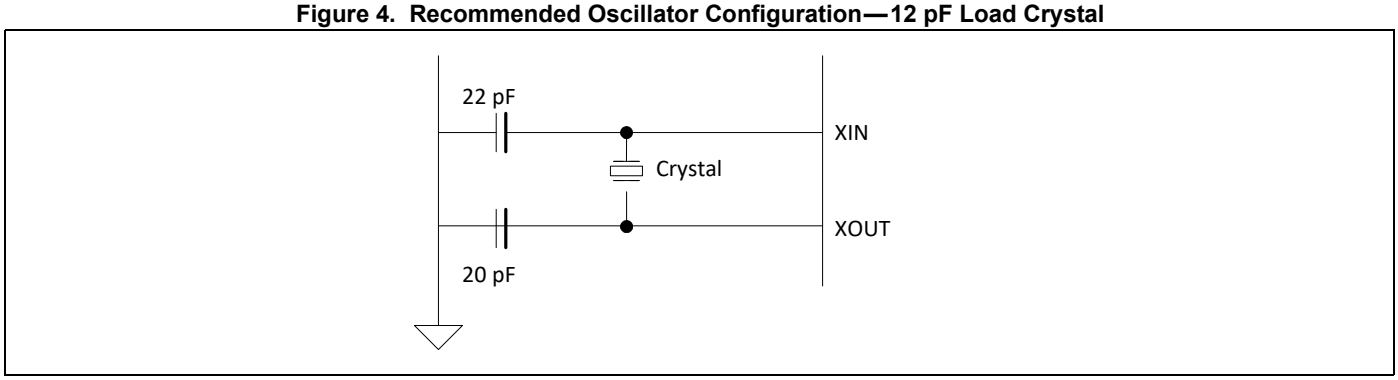


Table 4 shows the recommended crystal specifications.

Table 4. Reference Crystal Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Nominal frequency	–	20	24	40	MHz
Oscillation mode	–		Fundamental		–
Frequency tolerance	@25°C	–	±10	–	ppm
Tolerance stability over temp	@0°C to +70°C	–	±10	–	ppm
Equivalent series resistance	–	–	–	60	Ω
Load capacitance	–	–	12	–	pF
Operating temperature range	–	0	–	+70	°C
Storage temperature range	–	–40	–	+125	°C
Drive level	–	–	–	200	µW
Aging	–	–	±3	±10	ppm/year
Shunt capacitance	–	–	–	2	pF

1.9.2 HID Peripheral Block

The peripheral blocks of the CYW20735B1 all run from a single 128 kHz low-power RC oscillator. The oscillator can be turned on at the request of any of the peripherals. If the peripheral is not enabled, it shall not assert its clock request line.

The keyboard scanner is a special case, in that it may drop its clock request line even when enabled, and then reassert the clock request line if a keypress is detected.

1.9.3 32 kHz Crystal Oscillator

Figure 5 shows the 32 kHz XTAL oscillator with external components and Table on page 13 lists the oscillator's characteristics. It is a standard Pierce oscillator using a comparator with hysteresis on the output to create a single-ended digital output. The hysteresis was added to eliminate any chatter when the input is around the threshold of the comparator and is ~100 mV. This circuit can be operated with a 32 kHz or 32.768 kHz crystal oscillator or be driven with a clock input at a similar frequency. The default component values are: R1 = 10 MΩ and C1 = C2 = ~10 pF. The values of C1 and C2 are used to fine-tune the oscillator.

Figure 5. 32 kHz Oscillator Block Diagram

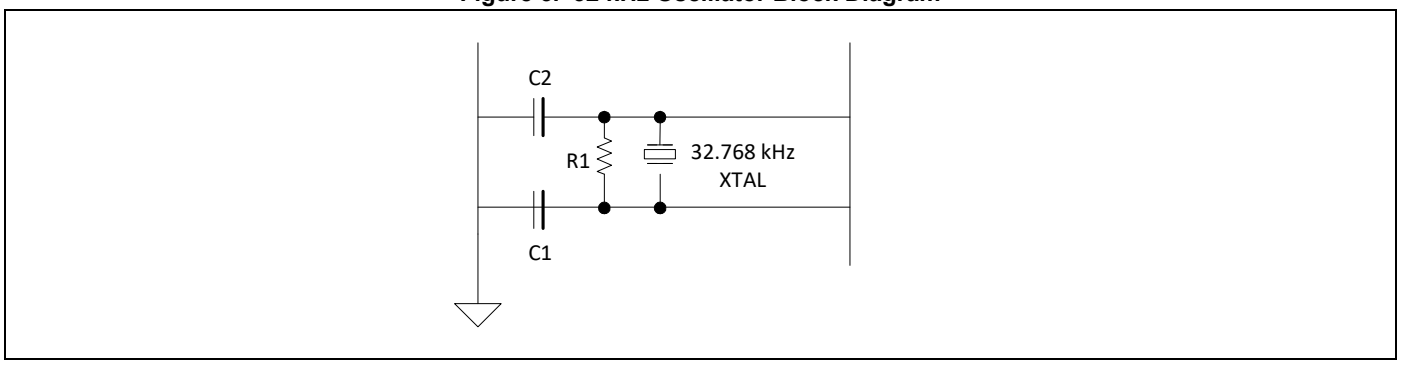


Table 5. XTAL Oscillator Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output frequency	F_{oscout}	–	–	32.768	–	kHz
Frequency tolerance	–	Crystal-dependent	–	100	–	ppm
Start-up time	$T_{startup}$	–	–	–	500	ms
XTAL drive level	P_{drv}	For crystal selection	0.5	–	–	µW
XTAL series resistance	R_{series}	For crystal selection	–	–	70	kΩ
XTAL shunt capacitance	C_{shunt}	For crystal selection	–	–	1.3	pF

1.10 GPIO Ports

GPIO ports for this device is shown in Table 7 on page 21.

The CYW20735B1 uses 40 general-purpose I/Os (GPIOs). All GPIOs support programmable pull-ups and are capable of driving up to 8 mA at 3.3V or 4 mA at 1.8V, except P26, P27, P28, and P29, which are capable of driving up to 16 mA at 3.3V or 8 mA at 1.8V.

P0, P1, P8-P18, P21-23, P28-P38: all of these pins can be programmed as ADC inputs.

Port 26–Port 29: all four of these pins are capable of sinking up to 16 mA for LEDs. These pins also have the PWM function, which can be used for LED dimming.

1.11 Keyboard Scanner

The keyboard scanner is designed to autonomously sample keys and store them into buffer registers without the need for the host microcontroller to intervene. The scanner has the following features:

- Ability to turn off its clock if no keys are pressed.
- Sequential scanning of up to 160 keys in an 8 × 20 matrix.
- Programmable number of columns from 1 to 20.
- Programmable number of rows from 1 to 8.
- 16-byte key code buffer (can be augmented by firmware).
- 128 kHz clock that allows scanning of full 160-key matrix in about 1.2 ms.
- N-key rollover with selective 2-key lockout if ghost is detected.
- Keys are buffered until host microcontroller has a chance to read it, or until overflow occurs.
- Hardware debouncing and noise/glitch filtering.
- Low-power consumption. Single-digit µA-level sleep current.

1.11.1 Theory of Operation

The key scan block is controlled by a state machine with the following states:

1.11.2 Idle

The state machine begins in the idle state. In this state, all column outputs are driven high. If any key is pressed, a transition occurs on one of the row inputs. This transition causes the 128 kHz clock to be enabled (if it is not already enabled by another peripheral) and the state machine to enter the scan state. Also in this state, an
8-bit row-hit register and an 8-bit key-index counter is reset to 0.

1.11.3 Scan

In the scan state, a row counter counts from 0 up to a programmable number of rows minus 1. After the last row is reached, the row counter is reset and the column counter is incremented. This cycle repeats until the row and column counters are both at their respective terminal count values. At that point, the state machine moves into the Scan-End state.

As the keys are being scanned, the key-index counter is incremented. This counter value is compared to the modifier key codes stored in RAM, or in the key code buffer if the key is not a modifier key. It can be used by the microprocessor as an index into a lookup table of usage codes.

Also, as the *n*th row is scanned, the row-hit register is ORed with the current 8-bit row input values if the current column contains two or more row hits. During the scan of any column, if a key is detected at the current row, and the row-hit register indicates that a hit was detected in that same row on a previous column, then a ghost condition may have occurred, and a bit in the status register is set to indicate this.

1.11.4 Scan End

This state determines whether any keys were detected while in the scan state. If yes, the state machine returns to the scan state. If no, the state machine returns to the idle state, and the 128 kHz clock request signal is made inactive.

Note: The microcontroller can poll the key status register.

1.12 Mouse Quadrature Signal Decoder

The mouse signal decoder is designed to autonomously sample two quadrature signals commonly generated by an optomechanical mouse. The decoder has the following features:

- Three pairs of inputs for X, Y, and Z (typical scroll wheel) axis signals. Each axis has two options:
  - For the X axis, choose P2 or P32 as X0 and P3 or P33 as X1.
  - For the Y axis, choose P4 or P34 as Y0 and P5 or P35 as Y1.
  - For the Z axis, choose P6 or P36 as Z0 and P7 or P37 as Z1.
- Control of up to four external high-current GPIOs to power external optoelectronics:
  - Turn-on and turn-off time can be staggered for each HC-GPIO to avoid simultaneous switching of high currents and having multiple high-current devices on at the same time.
  - Sample time can be staggered for each axis.
  - Sense of the control signal can be active high or active low.
  - Control signal can be tristated for off condition or driven high or low, as appropriate.

1.12.1 Theory of Operation

The mouse decoder block has four 10-bit PWMs for controlling external quadrature devices and sampling the quadrature inputs at its core.

The GPIO signals may be used to control such items as LEDs, external ICs that may emulate quadrature signals, photodiodes, and photodetectors.

1.13 ADC Port

The ADC block is a single switched-cap Σ-Δ ADC core for audio and DC measurement. It operates at the 12 MHz clock rate and has 32 DC input channels, including 28 GPIO inputs. The internal bandgap reference has ±5% accuracy without calibration. Different calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in DC mode.

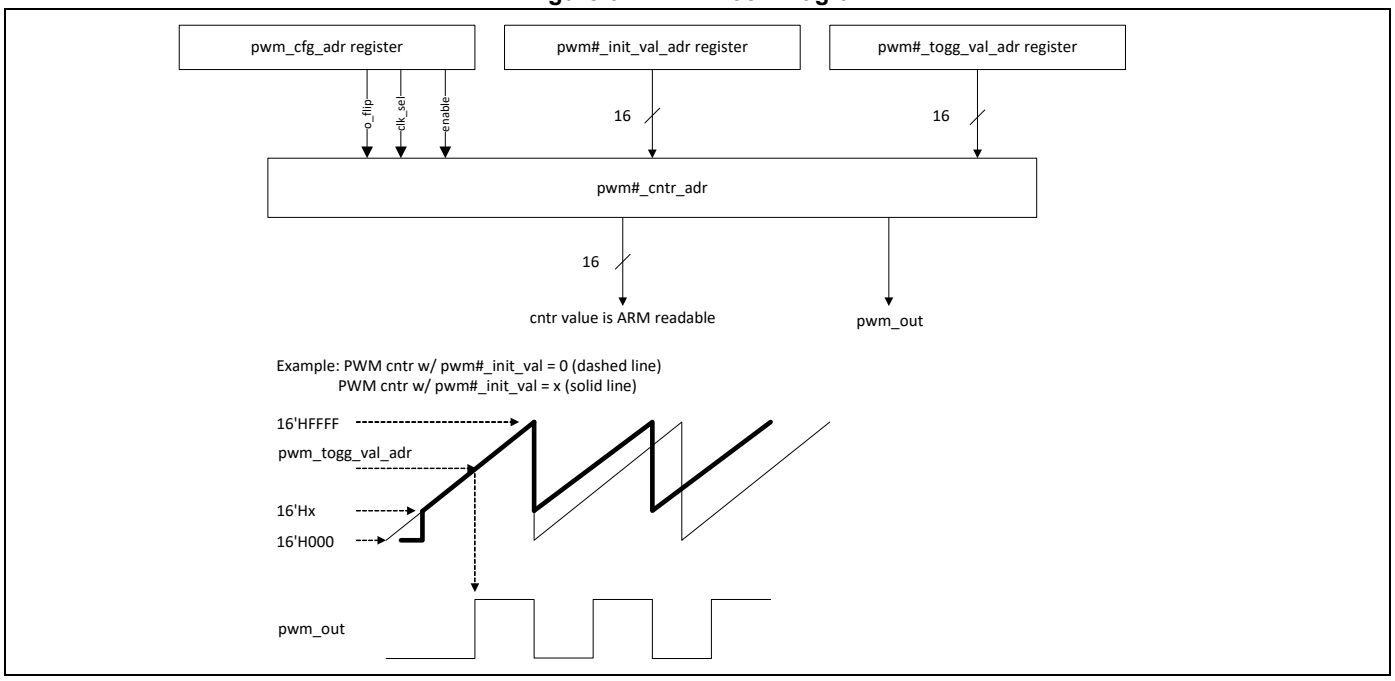
1.14 PWM

The CYW20735B1 has six internal PWMs. The PWM module consists of the following:

- PWM0–5. Each of the six PWM channels contains the following registers:
  - 16-bit initial value register (read/write)
  - 16-bit toggle register (read/write)
  - 16-bit PWM counter value register (read)
- PWM configuration register shared among PWM0–5 (read/write). This 18-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 6 shows the structure of one PWM.

Figure 6. PWM Block Diagram



1.15 Triac Control

The CYW20735B1 includes hardware support for zero-crossing detection and trigger control for up to four triacs. The CYW20735B1 detects zero-crossing on the AC zero detection line and uses that to provide a pulse that is offset from the zero crossing. This allows the CYW20735B1 to be used in dimmer applications, as well as any other applications that require a control signal that is offset from an input event.

The zero-crossing hardware includes an option to suppress glitches.

1.16 Serial Peripheral Interface

The CYW20735B1 has two independent SPI interfaces, both of which support single, dual, and quad mode SPI operations.

Either interface can be a master or a slave. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the CYW20735B1 has optional I/O ports that can be configured individually and separately for each functional pin. The CYW20735B1 acts as an SPI master device that supports 1.8V or 3.3V SPI slaves. The CYW20735B1 can also act as an SPI slave device that supports a 1.8V or 3.3V SPI master.

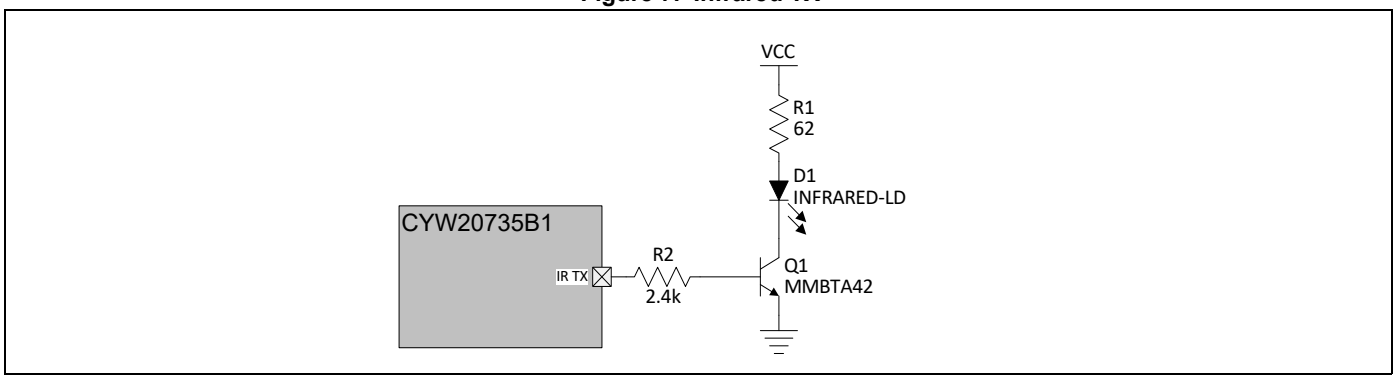
Note: SPI voltage depends on VDDO/VDDM; therefore, it defines the type of devices that can be supported.

1.17 Infrared Modulator

The CYW20735B1 includes hardware support for infrared TX. The hardware can transmit both modulated and unmodulated waveforms. For modulated waveforms, hardware inserts the desired carrier frequency into all IR transmissions. IR TX can be sourced from firmware-supplied descriptors, a programmable bit, or the peripheral UART transmitter.

If descriptors are used, they include IR on/off state and the duration between 1–32767 µsec. The CYW20735B1 IR TX firmware driver inserts this information in a hardware FIFO and makes sure that all descriptors are played out without a glitch due to underrun (see Figure 7).

Figure 7. Infrared TX



1.18 PDM Microphone

The CYW20735B1 accepts a ΣΔ-based one-bit pulse density modulation (PDM) input stream and outputs filtered samples at either 8 kHz or 16 kHz sampling rates. The PDM signal derives from an external kit that can process analog microphone signals and generate digital signals. The digital signal passes through the chip IO and MUX inputs using an auxADC signal. The PDM shares the filter path with the auxADC. Two types of data rates can be supported:

- 8 kHz
- 16 kHz

The external digital microphone accepts a 2.4 MHz clock generated by the CYW20735B1 and outputs a PDM signal which is registered by the PDM interface with either the rising or falling edge of the 2.4 MHz clock selectable through a programmable control bit. The design can accommodate two simultaneous PDM input channels, so stereo voice is possible.

1.19 Security Engine

The CYW20735B1 includes a hardware security accelerator that greatly decreases the time required to perform typical security operations. These functions include:

- Public key acceleration (PKA) cryptography
- AES-CTR/CBC-MAC/CCM acceleration
- SHA2 message hash and HMAC acceleration
- RSA encryption and decryption of modulus sizes up to 2048 bits
- Elliptic curve Diffie-Hellman in prime field GF(p)
- Generic modular math functions

1.20 Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core.

1.20.1 RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver, which then processes the power-down functions accordingly.

1.20.2 Host Controller Power Management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in HIDOFF (deep sleep) mode.

1.20.3 BBC Power Management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth-specified low-power connection mode. While in these low-power connection modes, the CYW20735B1 runs on the Low Power Oscillator and wakes up after a predefined time period.

The CYW20735B1 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

- Active mode
- Idle mode
- Sleep mode
- HIDOFF (deep sleep) mode

The CYW20735B1 transitions to the next lower state after a programmable period of user inactivity. When user activity resumes, the CYW20735B1 immediately enters Active mode.

In HIDOFF mode, the CYW20735B1 baseband and core are powered off by disabling power to VDDC_OUT and PAVDD. The VDDO domain remains powered up and will turn the remainder of the chip on when it detects user events. This mode minimizes chip power consumption and is used for longer periods of inactivity.

2. Pin Assignments and GPIOs

2.1 Pin Assignments

Table 6. Pin Assignments

Pin Name	QFN Pin	I/O	Power Domain	Description
Microphone				
MIC_AVDD	48	I	MIC_AVDD	Microphone supply
MICBIAS	45	I	MIC_AVDD	Microphone bias supply
MICN	47	I	MIC_AVDD	Microphone negative input
MICP	46	I	MIC_AVDD	Microphone positive input
Baseband Supply				
BT_VDDO	36	I	VDDO	I/O pad power supply
BT_VDDC	37	I	VDDC	Baseband core power supply
LHL_VDDO	60	I	VDDO	LHL PAD power supply: can be tied to BT_VDDO
RF Power Supply				
BT_PAVDD2P5	26	I	PAVDD2P5	PA supply
BT_PLLVDD1P2	31	I	PLLVDD1P2	RFPLL and crystal oscillator supply
BT_VCOVDD1P2	29	I	VCOVDD1P2	VCO supply
BT_IFVDD1P2	28	I	IFVDD1P2	IFPLL power supply
Onboard LDOs				
DIGLDO_VDDIN1P5	25	I	–	Internal digital LDO input and feedback pin of switching regulator (CBUCK).
RFLDO_VDDIN1P5	24	I	–	RF LDO input
RFLDO_VDDOUT	23	O	–	RF LDO output
PALDO_VDDIN_5V	19	I	–	PA LDO input
PALDO_VDDOUT3V	20	O	–	PA LDO output
SR_VDDBAT3V	22	I	–	Core buck input
SR_VLX	21	O	–	Core buck output
Ground Pins				
HS-VSS	H	I	VSS	Digital ground
UART				
UART_CTS_N	44	I, PU	VDDO	CTS for HCI UART interface: NC if unused.
UART_RTS_N	43	O, PU	VDDO	RTS for HCI UART interface. NC if unused.
UART_RXD	41	I	VDDO	UART serial input. Serial data input for the HCI UART interface.
UART_TXD	42	O, PU	VDDO	UART serial input. Serial data input for the HCI UART interface.
Serial Peripheral Interface				
SPI_MISO	40	I	VDDO	SPI Master In Slave Out
SPI_MOSI	39	O	VDDO	SPI Master Out Slave In
SPI_CSN	38	O	VDDO	SPI Chip Select
SPI_CLK	35	O	VDDO	SPI Clock
Crystal				
BT_XTALI	32	I	PLLVDD1P2	Crystal oscillator input: see “Crystal Oscillator” on page 12 for options
BT_XTALO	33	O	PLLVDD1P2	Crystal oscillator output

Table 6. Pin Assignments (Cont.)

Pin Name	QFN Pin	I/O	Power Domain	Description
XTALI_32K	50	I	VDDO	Low-power oscillator input
XTALO_32K	49	O	VDDO	Low-power oscillator output
Others				
DEFAULT_STRAP	18	I	VDDO	Connect to VDDO
BT_HOST_WAKE	34	O	VDDO	Host wake-up. This is a signal from the Bluetooth device to the host indicating that the Bluetooth device requires attention. ■ Asserted: Host device must wake up or remain awake. ■ Deasserted: Host device may sleep when sleep criteria is met. The polarity of this signal is software configurable and can be asserted high or low.
BT_RF	27	I/O	PAVDD2P5	RF antenna port
JTAG_SEL	17	–	–	ARM JTAG debug mode control: connect to GND for all applications
RST_N	16	I	VDDO	Active-low system reset with open-drain output and internal pull-up resistor
NC	30			Leave floating

2.2 GPIO Pin Descriptions

Table 7. GPIO Pin Descriptions[ab]

QFN Pin Number	Pin Name	Default Direction	POR State	Power Domain	Default Alternate Function Description
8	P0	Input	Floating	VDDO	■ GPIO: P0 ■ A/D converter input 29 **Note:** Not available during TM1 = 1.
9	P1	Input	Floating	VDDO	■ GPIO: P1 ■ A/D converter input 28
52	P2	Input	Floating	VDDO	■ GPIO: P2
53	P3	Input	Floating	VDDO	■ GPIO: P3
54	P4	Input	Floating	VDDO	■ GPIO: P4
55	P5	Input	Floating	VDDO	■ GPIO: P5
56	P6	Input	Floating	VDDO	■ GPIO: P6
57	P7	Input	Floating	VDDO	■ GPIO: P7
58	P8	Input	Floating	VDDO	■ GPIO: P8 ■ A/D converter input 27
1	P9	Input	Floating	VDDO	■ GPIO: P9 ■ A/D converter input 26
2	P10	Input	Floating	VDDO	■ GPIO: P10 ■ A/D converter input 25
3	P11	Input	Floating	VDDO	■ GPIO: P11 ■ A/D converter input 24
4	P12	Input	Floating	VDDO	■ GPIO: P12 ■ A/D converter input 23
5	P13	Input	Floating	VDDO	■ GPIO: P13 ■ A/D converter input 22
59	P14	Input	Floating	VDDO	■ GPIO: P14 ■ A/D converter input 21
50	P15	Input	Floating	VDDO	■ GPIO: P15 ■ A/D converter input 20
51	P16	Input	Floating	VDDO	■ GPIO: P16 ■ A/D converter input 19
13	P26 PWM0	Input	Floating	VDDO	■ GPIO: P26 ■ Current: 16 mA sink
14	P27 PWM1	Input	Floating	VDDO	■ GPIO: P27 ■ Current: 16 mA sink
6	P28 PWM2	Input	Floating	VDDO	■ GPIO: P28 ■ A/D converter input 11 ■ Current: 16 mA sink

Table 7. GPIO Pin Descriptions[ab] (Cont.)

QFN Pin Number	Pin Name	Default Direction	POR State	Power Domain	Default Alternate Function Description
7	P29 PWM3	Input	Floating	VDDO	■ GPIO: P29 ■ A/D converter input 10 ■ Current: 16 mA sink
15	P32	Input	Floating	VDDO	■ GPIO: P32 ■ A/D converter input 7
10	P34	Input	Floating	VDDO	■ GPIO: P34 ■ A/D converter input 5
11	P38	Input	Floating	VDDO	■ GPIO: P38 ■ A/D converter input 1
12	P39	Input	Floating	VDDO	Reserved for system use. Leave this GPIO unconnected

a. All GPIOs are supermux. All GPIOs can be programmed for any alternative functions. For example, key scan, SPI, I^2C, IR_TX, quadrature, peripheral UART, ADC, etc.

b. During power-on reset, all inputs are disabled.

Table 8. GPIO Supermux Input/Output Function List

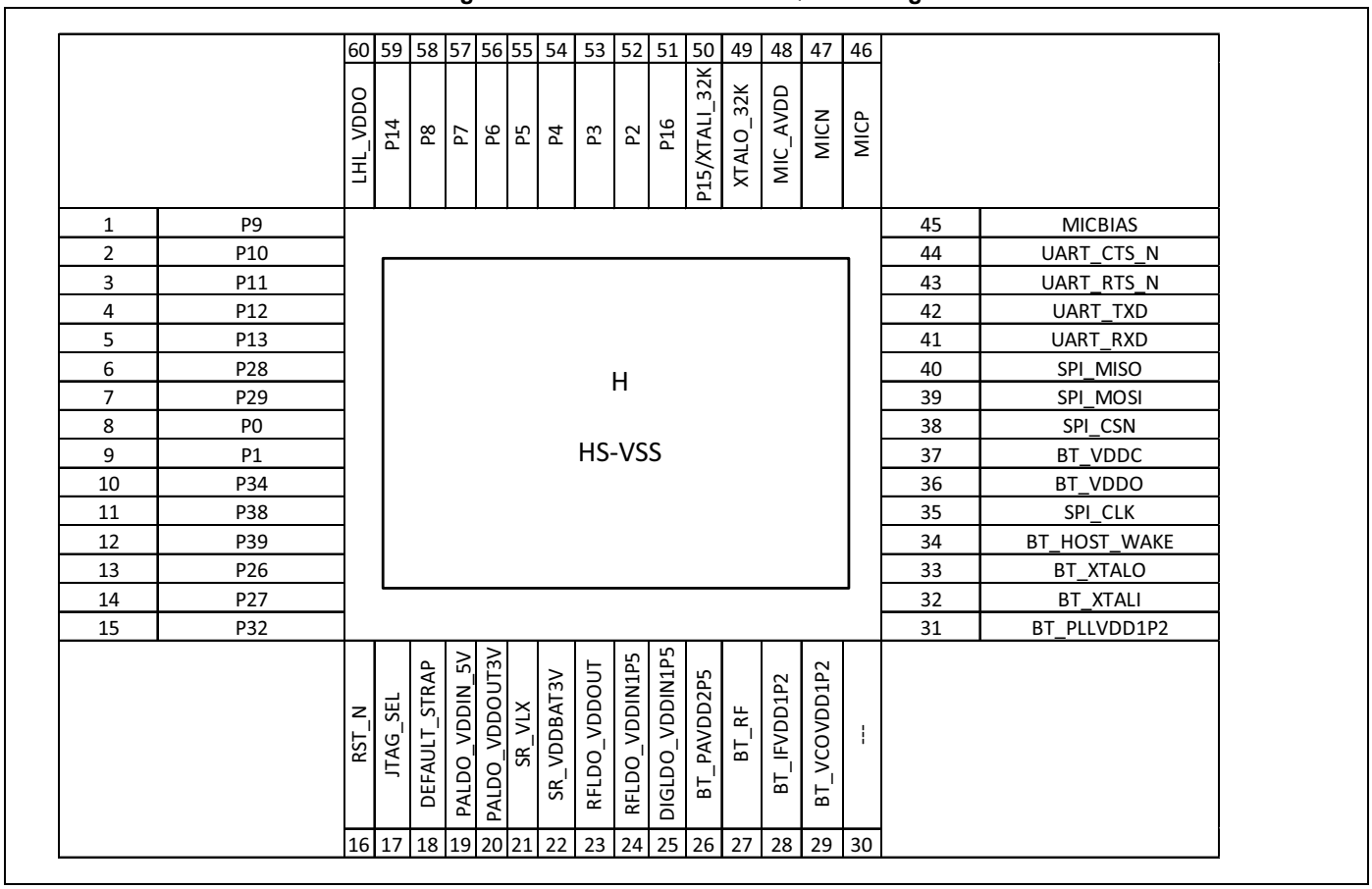
Function	Function	Function	Function
SPI_1: CLK	SPI_1: CS	SPI_1: MOSI	SPI_1: MISO
SPI_1: INT	SPI_2: CLK	SPI_2: CS	SPI_2: MOSI
SPI_2: MISO	SPI_2: INT	SPI_3: CLK	SPI_3: CS
SPI_3: MOSI	SPI_3: MISO	SPI_3: INT	UART_RX
UART_CTS	UART_TX	UART_RTS	PUART_RX
PUART_CTS	PUART_TX	PUART_RTS	SCL
SDA	SCL2	SDA2	PCM_IN
PCM_OUT	PCM_CLK	PCM_SYNC	I2S_DO
I2S_DI	I2S_WS	I2S_CLK	IR_TX
kso0	kso1	kso2	kso3
kso4	kso5	kso6	kso7
kso8	kso9	kso10	kso11
kso12	kso13	kso14	kso15
kso16	kso17	kso18	kso19
PWM0	PWM1	PWM2	PWM3
PWM4	PWM5	aclk0	aclk1
pa_ramp	tx_pd	~tx_pd	–

2.3 Pinouts

2.3.1 60-Pin QFN Package

The 60-pin QFN package is shown in Figure 8.

Figure 8. CYW20735B1 60-Pin QFN Package



Note: Pin H is a ground pin that is used for the signal name HS-VSS.

3. Specifications

3.1 Electrical Characteristics

Caution! The absolute maximum ratings in the following table indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device

Table 9. Absolute Maximum Ratings

Requirement Parameter	Specification			Unit
	Min.	Nom.	Max.	
Maximum Junction Temperature	–	–	125	°C
VDD IO	–0.5	–	3.795	V
VDD RF	–0.5	–	1.38	V
VDDBAT3V	–0.5	–	3.795	V
DIGLDO_VDDIN1P5	–0.5	–	1.65	V
RFLDO_VDDIN1P5	–0.5	–	1.65	V
PALDO_VDDIN_5V	–0.5	–	3.795	V
MIC_AVDD	–0.5	–	3.795	V
OTP_3P3V	–0.5	–	3.795	V

Table 10. ESD/Latchup

Requirement Parameter	Specification			Unit
	Min.	Nom.	Max.	
ESD Tolerance HBM	–2000	–	2000	V
ESD Tolerance CDM	–500	–	500	V
Latch-up	–	200	–	mA

Table 11. Environmental Ratings

Characteristic	Value	Units
Operating Temperature	–30 to +85	°C
Storage Temperature	–40 to +150	°C

Table 12. Recommended Operating Conditions

Parameter	Specification			Unit
	Min.	Typ.	Max.	
VDD IO[a]	V_{SHUT}[b]	3.0	3.63	V
VDDRF	1.14	1.2	1.26	V
VDDBAT3V[a]	V_{SHUT}[b]	3.0	3.63	V
PALDO_VDDIN_5V	2.5	3.3	3.63	
DIGLDO_VDDIN1P5	1.3	1.35	1.5	V
RFLDO_VDDIN1P5	1.3	1.35	1.5	V
MIC_AVDD	V_{SHUT}[b]	3.0	3.63	V
OTP_3P3V	3.0	3.3	3.63	V

a. VDDIO must be greater or equal to V_{BAT}.
b. See Table 13.

The CYW20735B1 uses an onboard low voltage detector to shut down the part when supply voltage (VDDBAT3V) drops below operating range.

Table 13. Shutdown Voltage

Parameter	Specification			Unit
	Min.	Typ.	Max.	
V_{SHUT}	1.625	1.7	1.775	V

3.1.1 Core Buck Regulator

Table 14. Core Buck Regulator

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input supply voltage DC, VBAT	DC voltage range	1.62	3.0	3.63	V
CBUCK output current	–	–	–	65	mA
Output voltage range	Programmable, 30mV/step default = 1.35V (bits = 0000)	1.2	1.35	1.5	V
Output voltage DC accuracy	Includes load and line regulation	–4	–	+4	%
LPOM ripple voltage, static	Measured with 20 MHz bandwidth limit, static load. Max ripple based on VBAT = 3V, Vout = 1.35V Inductor: 0806 inch-size, Tmax = 1 mm, 2.2 µH ±25%, DCR = 114 mΩ ±20%, ACR<1Ω (for frequency <1 MHz) Capacitor: 1 µF ±10%, 6.3V, 0603 inch, X5R, MLCC capacitor + board total-ESR < 20 mΩ	–	–	30	mVpp
Efficiency (high load)	10–50 mA load current, Vout = 1.35V, Vbat = 3V @25°C Inductor: 0806 inch-size, Tmax = 1 mm, 2.2 µH ±25%, DCR = 114 mΩ ±20%, ACR<1Ω (for frequency<1 MHz) Capacitor: 1 µF ±10%, 6.3V, 0603 inch, X5R, MLCC capacitor +board total-ESR < 20 mΩ	–	85	–	%
Efficiency (low load)	1–5 mA load current, Vout = 1.35V, Vbat = 3V @25°C Inductor: 0806 inch-size, Tmax = 1 mm, 2.2 µH ±25%, DCR = 114 mΩ ±20%, ACR<1Ω (for frequency<1 MHz) Capacitor: 1 µF ±10%, 6.3V, 0603 inch, X5R, MLCC capacitor +board total-ESR < 20 mΩ	–	80	–	%
Startup time	See Table 15 on page 27.	–	–	–	–
External inductor L	2.2 µH ±25%, DCR = 114 mΩ ±20%, ACR<1Ω (for frequency<1 MHz)	–	2.2	–	µH
External output capacitor, Cout	1 µF ±10%, 6.3V, 0603 inch, X5R, MLCC capacitor +board total-ESR < 20 mΩ	0.7	1	1.1	µF
External input capacitor, Cin	For SR_VDDBAT 3V pin Ceramic, X5R, 0402, ESR<30 mΩ at 4 MHz, +/-20%, 6.3V, 4.7 µF	0.7	4.7	5.64	µF
Input supply voltage ramp-up time	0 to 3.3V	40	–	–	µs

- Minimum capacitor value refers to residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.
- Maximum capacitor value refers to the total capacitance seen at a node where the capacitor is connected. This also includes any decoupling capacitors connected at the load side, if any.

3.1.2 Digital LDO

Table 15. Digital LDO

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input supply voltage, Vin	Minimum Vin = Vo + 0.12V requirement must be met under maximum load.	1.3	1.35	1.5	V
Nominal output voltage,Vo	Internal default bit setting	–	1.2	–	V
Output voltage programmability	Range Step size Accuracy at any step (including line/load regulation)	0.9 – –4	– 10 –	1.25 – +4	V mV %
Dropout voltage	At maximum load	–	–	120	mV
Output current	DC load	0.2[a]	–	40	mA
Output loading capacitor	Internal, including the decoupling capacitor to be placed next to the load and the equivalent loading capacitor by the core.	4	–	10	nF
Quiescent current	At no load, excluding main bandgap Iq	–	90	120	µA
Line regulation	Vin from (Vo+0.12V) to 1.5V; 40 mA load	–	–	5	mV/V
Load regulation	Load from 1 mA to 25 mA; Vin (Vo+0.12V)	–	0.025	0.045	mV/mA
Leakage current	In full power-down mode or bypass mode: Junction temperature: 25°C Junction temperature: 125°C	 – –	 0.05 1.1	 0.2 5.0	 µA µA
PSRR	@1 kHz, Vin, Vo+0.12V Output cap of 4 nF~10 nF	40	–	–	dB
LDO turn-on time	LDO turn-on time when balance of chip is up	–	–	22	µs
External input capacitor	Only use an external input capacitor at VDD_DIGL-DO1P5 pin if it is not supplied from CBUCK output.	–	1	2.2	µF

a. By default, an internal loading of ~0.2 mA resides inside the LDO. This is to ensure the LDO is stable with zero loading from the core. After the core is up, digital logic can disable this internal loading by setting i_ldo_cntl<8:7> to 00.

3.1.3 PA LDO

Table 16. PA LDO

Specification	Notes	Min.	Typ.	Max.	Units
Input supply voltage	Min = 3.0 + 0.1V = 3.1V Dropout voltage requirement must be met under max load for performance specs	1.8[a]	3.3	3.63	V
Output current	Junction temperature 125°C	–	–	50	mA
Output voltage (Vo)	Default = 3.0V	2.4	3.0	3.4	V
Dropout voltage	At max. load	–	–	100	mV
Output voltage DC accuracy	Include line/load regulation	–5		+5	%
Quiescent current	No load	–	8	–	µA
Line regulation	Vin from (Vo + 0.1V) to 4.8V, max load	–0.2		+0.2	%Vo/V
Load regulation	Load from 1 mA to 50 mA		0.02	0.05	%Vo/mA
Leakage current	In Power-Down mode at 25°C junction temp	–	0.3	–	µA
PSRR	Vbat 3.6V, Vo = 2.5V, Co = l µF, max load, 100 Hz to 100 kHz	20	–		dB
LDO turn-on time	LDO turn-on time when the rest of the chip is up	–	–	100	µs
In-rush current during turn-on	From its output cap in the fully-discharged state	–	–	70	mA
External output capacitor (Co)	Ceramic, X5R, 0402, (ESR: 30m–200 mΩ), ±10%, 6.3V	0.44	1	–	µF
External input capacitor	For PALDO_VDDIN_5V pin Ceramic, X5R, 0402, (ESR: 30m-200 mΩ), ±10%, 6.3V	–	1	–	µF

a. Guaranteed TX power is 4dBm when PALDO input supply voltage is 1.8V.

3.1.4 RF LDO

Table 17. RF LDO

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input supply voltage, Vin	Min Vin = Vo + 0.15V = 1.35V (for Vo = 1.2V) Dropout voltage requirement must be met under maximum load.	1.3	1.35	1.5	V
Nominal output voltage,Vo	Internal default bit setting 000	–	1.2	–	V
Output voltage programmability	Range	1.1	–	1.275	V
	Step size	–	25	–	mV
	Accuracy at any step (including line/load regulation)	–4	–	+4	%
Dropout voltage	At maximum load	–	–	150	mV
Output current	Operating voltage range	0.1	–	25	mA
Quiescent current	No load	–	44	–	µA
Line regulation	Vin from (Vo+0.15V) to 1.5V; 25 mA load	–	–	5.5	mV/V
Load regulation	Load from 1 mA to 25 mA; Vin≥ (Vo+0.15V)	–	0.025	0.045	mV/mA
Load step error	Load step from 1 mA–25 mA in 1 µs and 25 mA–1 mA in 1µs; Vin(Vo+0.15V); Co = 2.2 µF	–	–	35	mV
Leakage current	Power-down junction temperature: 85°C	–	–	10	µA
Output noise	@30 kHz, 25 mA load, Co = 2.2 µF	–	–	60	nV/√Hz
	@100 kHz, 25 mA load, Co = 2.2 µF	–	–	35	nV/√Hz
PSRR	@1kHz, Input > 1.35V, Co = 2.2 µF, Vo = 1.2V	20	–	–	dB
LDO turn-on time	LDO turn-on time when balance of chip is up	–	140	180	µs
In-rush current	Vin = Vo+0.15V to 1.5V, Co = 2.2 µF, no load	–	–	100	mA
External output capacitor, Co	Total ESR (trace/cap): 5 m–240 mΩ	0.5	2.2	4.7	µF
External input capacitor	Only use an external input capacitor at RFLDO_VDDIN1P5 pin if it is not supplied from CBUCK output.	–	1	2.2	µF

Note: Minimum capacitor value refers to residual capacitor value after taking into account part-to-part tolerance, DC-bias, temperature, and aging.

3.1.5 Digital I/O Characteristics

Table 18. Digital I/O Characteristics

Characteristics	Symbol	Minimum	Typical	Maximum	Unit
Input low voltage (VDDO = 3.3V)	V_{IL}	–	–	0.8	V
Input high voltage (VDDO = 3.3V)	V_{IH}	2.0	–	–	V
Input low voltage (VDDO = 1.8V)	V_{IL}	–	–	0.6	V
Input high voltage (VDDO = 1.8V)	V_{IH}	1.1	–	–	V
Output low voltage	V_{OL}	–	–	0.4	V
Output high voltage	V_{OH}	VDDO – 0.4V	–	–	V
Input low current	I_{IL}	–	–	1.0	µA
Input high current	I_{IH}	–	–	1.0	µA
Output low current (VDDO = 3.3V, V_{OL} = 0.4V)	I_{OL}	–	–	2.0	mA
Output high current (VDDO = 3.3V, V_{OH} = 2.9V)	I_{OH}	–	–	4.0	mA
Output high current (VDDO = 1.8V, V_{OH} = 1.4V)	I_{OH}	–	–	2.0	mA
Input capacitance	C_{IN}	–	–	0.4	pF

3.1.6 Current Consumption

In Table 19, current consumption measurements are taken at VBAT with the assumption that VBAT is connected to VDDIO and LDOIN.

Table 19. BLE Current Consumption

Operational Mode	Conditions	Typical	Unit
Receiving	Receiver and baseband are both operating, 100% ON.	8	mA
Transmitting@12 dBm	Transmitter and baseband are both operating, 100% ON.	18	mA
Advertising	1.28s direct advertising in low power idle mode	30	µA
Scanning	TBD	TBD	mA
Connecting	1-second connection interval in low power idle mode	25	µA
HIDOFF (Deep Sleep)	–	1	µA

3.2 ADC Electrical Characteristics

Table 20. ADC Electrical Characteristics

Parameter	Symbol	Conditions/Comments	Min.	Typ.	Max.	Unit
Analog supply voltage	avddBAT	Battery and I/O supply	1.62	–	3.6	V
Analog core supply	AVDDC	±10%	1.08	1.2	1.32	V
Audio supply	Mic_avdd	Only available for audio application	1.8	2.5	3.3	V
Current consumption	I_{TOT}	–	–	2	3	mA
Power down current	–	At room temperature	–	1	–	µA
ADC Core Specification						
ADC reference voltage	VREF	From BG with ±3% accuracy	–	0.85	–	V
ADC sampling clock	–	–	–	12	–	MHz
Absolute error	–	Includes gain error, offset and distortion. Without factory calibration.	–	–	5	%
		Includes gain error, offset and distortion. After factory calibration.	–	–	2	%
ENOB	–	For audio application	12	13	–	Bit
		For static measurement	10	–	–	
ADC input full scale	FS	For audio application	–	1.6	–	
		For static measurement	1.8	–	3.6	
Conversion rate	–	For audio application	8	16	–	kHz
		For static measurement	16	20	–	
Signal bandwidth	–	For audio application	20	–	8K	Hz
		For static measurement	–	DC	–	
Input impedance	R_{IN}	For audio application	10	–	–	KΩ
		For static measurement	500	–	–	
Startup time	–	For audio application	–	10	–	ms
		For static measurement	–	20	–	µs
MIC PGA Specifications						
MIC PGA gain range	–	–	0	–	42	dB
MIC PGA gain step	–	–	–	1	–	dB
MIC PGA gain error	–	Includes part-to-part gain variation	–1	–	1	dB
PGA input referred noise	–	At 42 dB PGA gain A-weighted	–	–	4	µV
Passband gain flatness	–	PGA and ADC, 100 Hz–4 kHz	–0.5	–	0.5	dB
MIC Bias Specifications						
MIC bias output voltage	–	At 2.5V supply	–	2.1	–	V
MIC bias loading current	–	–	–	–	3	mA
MIC bias noise	–	Refers to PGA input 20 Hz to 8 kHz, A-weighted	–	–	3	µV
MIC bias PSRR	–	at 1 kHz	40	–	–	dB
ADC SNR	–	A-weighted 0 dB PGA gain	78	–	–	dB
ADC THD + N	–	–3 dBFS input 0 dB PGA gain	74	–	–	dB
GPIO input voltage		Always lower than avddBAT	–	–	3.6	V
GPIO source impedance[a]	–	Resistance	–	–	1	kΩ
		Capacitance	–	–	10	pF

a. Conditional requirement for the measurement time of 10 µs. Relaxed with longer measurement time for each GPIO input channel.

3.3 RF Specifications

Note: Table 21 and Table 22 on page 42 apply to single-ended industrial temperatures. Unused inputs are left open.

Table 21. Receiver RF Specifications

Parameter	Conditions	Minimum	Typical [a]	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity [b]	–	–	–91.5	–	–
Maximum input	GFSK, 1 Mbps	–	–	–20	dBm
Interference Performance					
TBD					
Out-of-Band Blocking Performance (CW)[c]					
30 MHz–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
Intermodulation Performance[d]					
BT, Df = 4 MHz	–	–39.0	–	–	dBm
Spurious Emissions[e]					
30 MHz to 1 GHz	–	–	–	–62	dBm
1 GHz to 12.75 GHz	–	–	–	–47	dBm
65 MHz to 108 MHz	FM RX	–	–147	–	dBm/Hz
746 MHz to 764 MHz	CDMA	–	–147	–	dBm/Hz
851–894 MHz	CDMA	–	–147	–	dBm/Hz
925–960 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1805–1880 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1930–1990 MHz	PCS	–	–147	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–147	–	dBm/Hz

a. Typical operating conditions are 1.22V operating voltage and 25°C ambient temperature.
b. The receiver sensitivity is measured at BER of 0.1% on the device interface.
c. Meets this specification using front-end band pass filter.
d. f0 = –64 dBm Bluetooth-modulated signal, f1 = –39 dBm sine wave, f2 = –39 dBm Bluetooth-modulated signal, f0 = 2f1 – f2, and |f2 – f1| = n*1 MHz, where n is 3, 4, or 5. For the typical case, n = 4.
e. Includes baseband radiated emissions.

Table 22. Transmitter RF Specifications (TBD)

Parameter	Conditions	Minimum	Typical	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
Class 1: GFSK TX power	–	–	10	–	dBm
Class 2: GFSK TX power	PALDO input supply = 1.8V	–	4	–	dBm
Power control step	–	2	4	8	dB
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0[a]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0[a, b]	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm

a. Maximum value is the value required for Bluetooth qualification.
b. Meets this spec using a front-end band-pass filter.

Table 23. BLE RF Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Frequency range	N/A	2402	–	2480	MHz
RX sense[a]	GFSK, 0.1% BER, 1 Mbps	–	–94.5	–	dBm
TX power	N/A	–	12	–	dBm
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max[b]	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	0.95	–	%

a. Dirty TX is OFF.
b. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

3.4 Timing and AC Characteristics

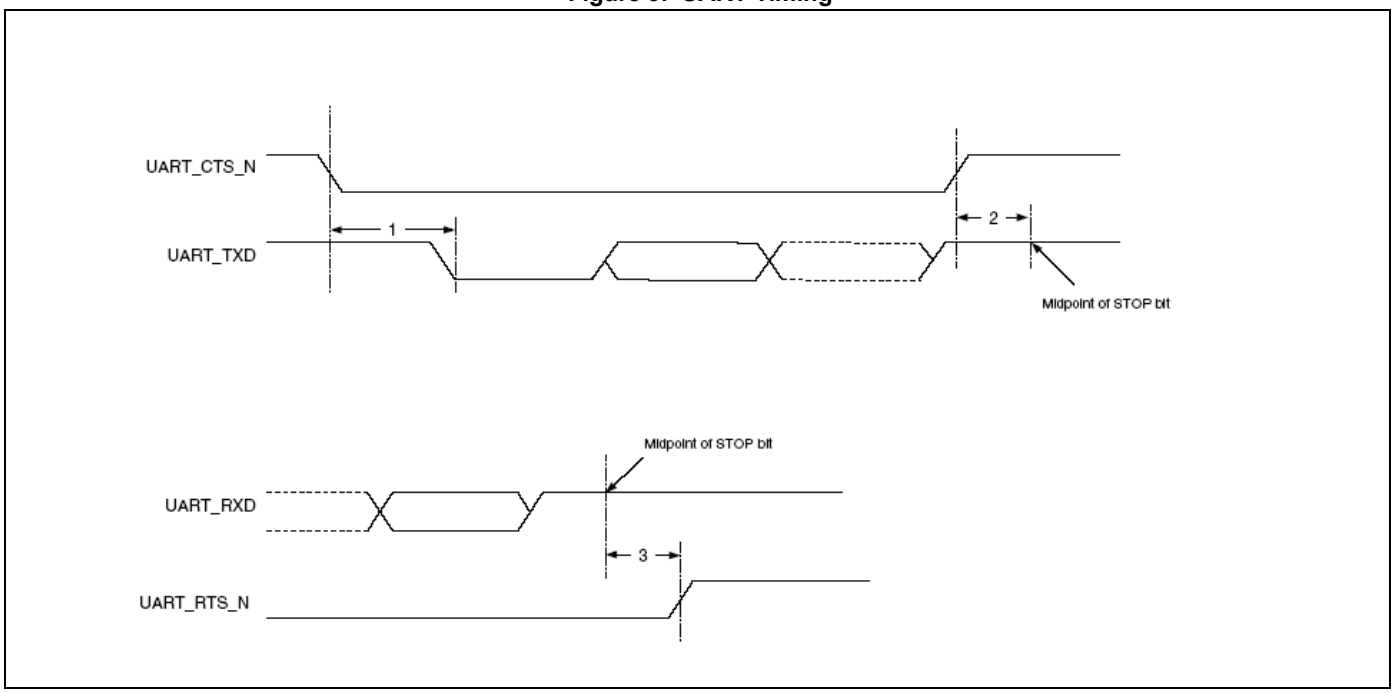
In this section, use the numbers listed in the Reference column of each table to interpret the following timing diagrams.

3.4.1 UART Timing

Table 24. UART Timing Specifications

Reference	Characteristics	Min.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	1.50	Baud periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	0.67	Baud periods
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	1.33	Baud periods

Figure 9. UART Timing



3.4.2 SPI Timing

The SPI interface can be clocked up to 12 MHz.

Table 25 and Figure 10 show the timing requirements when operating in SPI Mode 0 and 2.

Table 25. SPI Mode 0 and 2

Reference	Characteristics	Min.	Max.	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns

Figure 10. SPI Timing, Mode 0 and 2

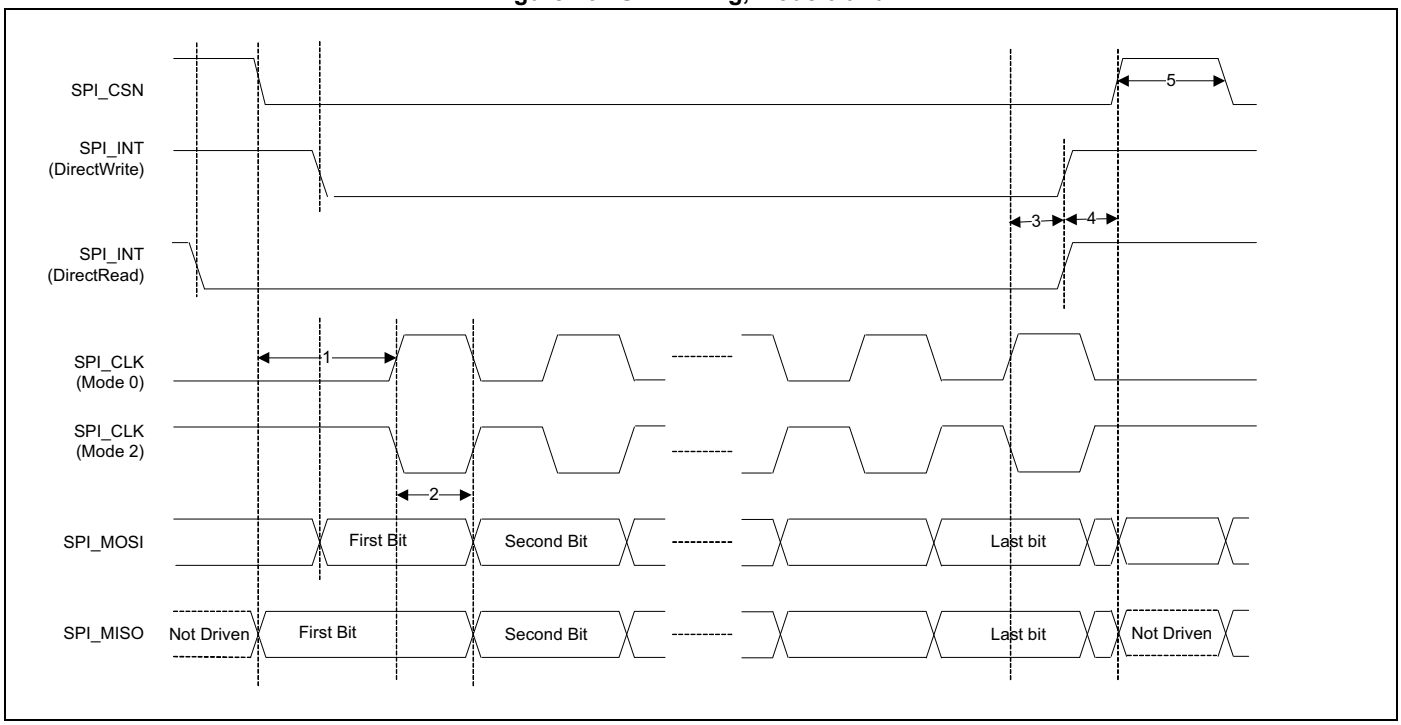
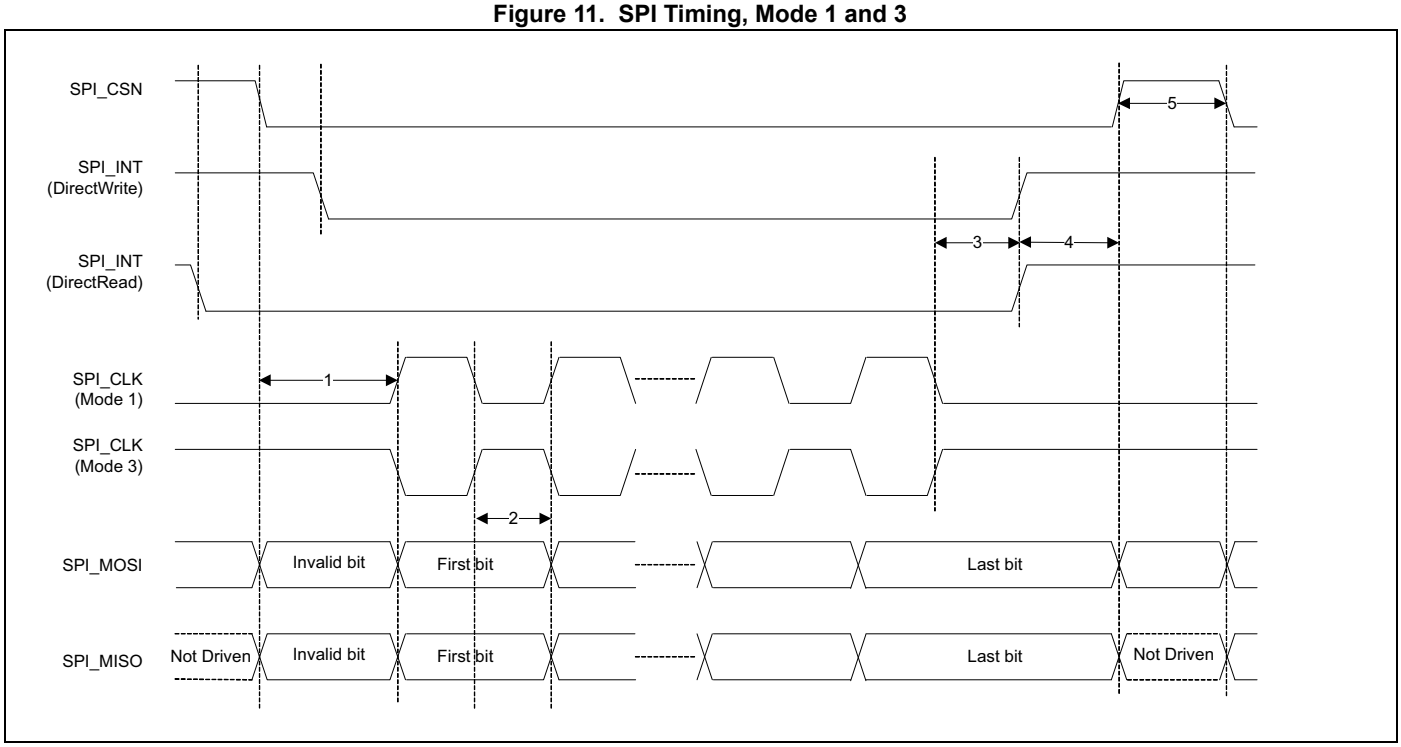


Table 26 and Figure 11 show the timing requirements when operating in SPI Mode 1 and 3.

Table 26. SPI Mode 1 and 3

Reference	Characteristics	Min.	Max.	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	ns
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	ns
5	Idle time between subsequent SPI transactions	1 SCK	–	ns

Figure 11. SPI Timing, Mode 1 and 3



3.4.3 I^2C Interface Timing

The specifications in Table 27 references Figure 12.

Table 27. I^2C Interface Timing Specifications (up to 1 MHz)

Reference	Characteristics	Minimum	Maximum	Unit
1	Clock frequency	–	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	ns
4	Clock low time	650	–	ns
5	Clock high time	280	–	ns
6	Data input hold time[a]	0	–	ns
7	Data input setup time	100	–	ns
8	STOP condition setup time	280	–	ns
9	Output valid from clock	–	400	ns
10	Bus free time[b]	650	–	ns

a. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
b. Time that the CBUS must be free before a new transaction can start.

Figure 12. I^2C Interface Timing Diagram

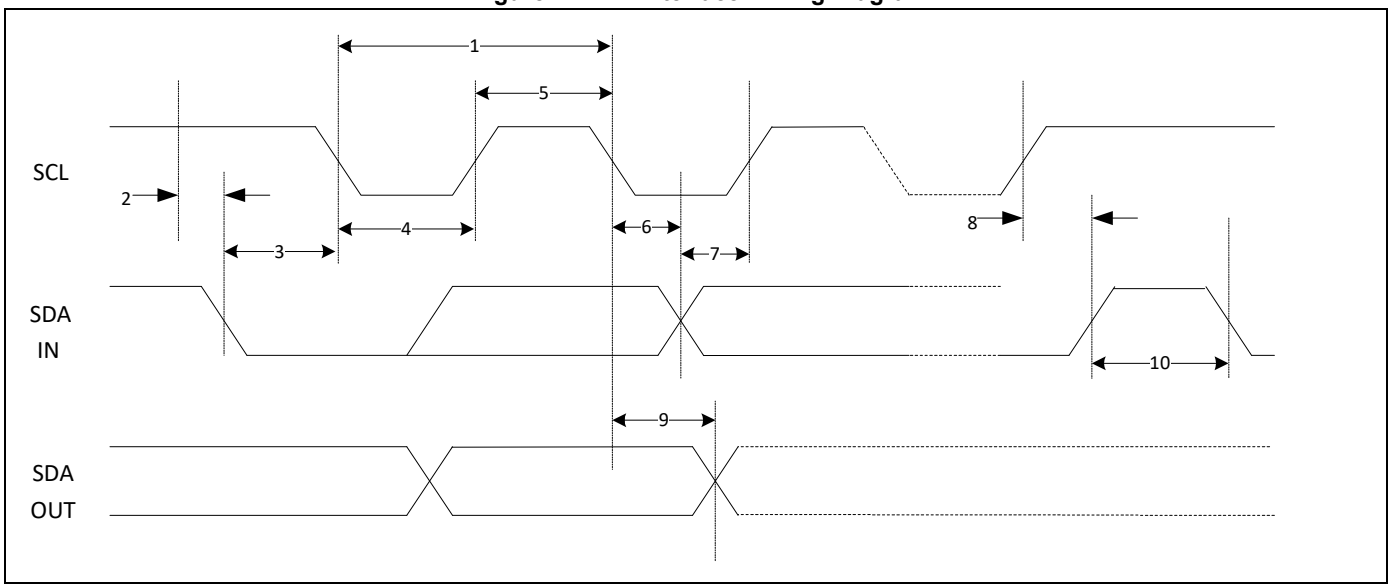
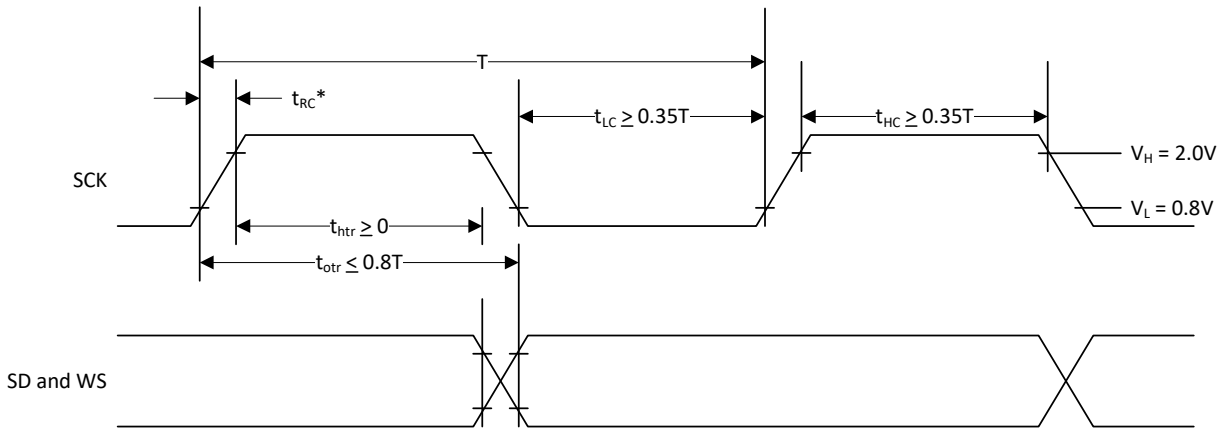


Table 28. Timing for I²S Transmitters and Receivers

	Transmitter				Receiver				Notes
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	a
Master Mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	d
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	e
Hold time t_{htr}	0	–	–	–	–	–	–	–	d
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	f
Hold time t_{hr}	–	–	–	–	–	0	–	–	f

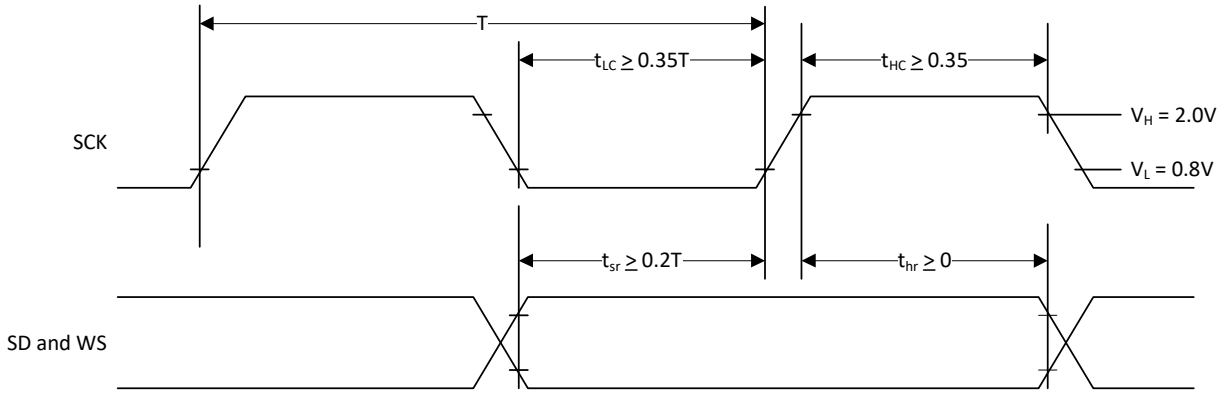
a. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
b. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
c. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
d. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
e. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
f. The data setup and hold time must not be less than the specified receiver setup and hold time.

Figure 13. I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 14. I²S Receiver Timing



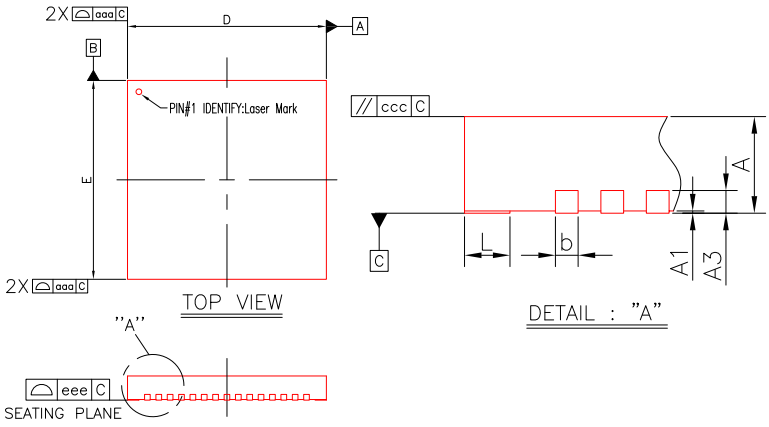
T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

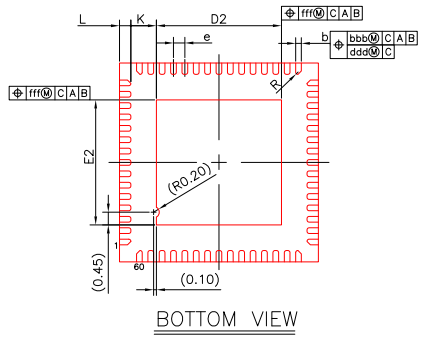
4. Mechanical Information

4.1 Package Diagrams

4.1.1 60-Pin QFN Package

Figure 15. CYW20735B1 7 mm × 7 mm 60-Pin QFN Package





Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.90	7.00	7.10	0.272	0.276	0.280
E	6.90	7.00	7.10	0.272	0.276	0.280
D2	4.30	4.40	4.50	0.169	0.173	0.177
E2	4.30	4.40	4.50	0.169	0.173	0.177
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.60	---	---	0.024	---	---
R	0.075	---	0.125	0.003	---	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

4.2 Tray Packaging Specifications

4.2.1 QFN

The CYW20735B1 QFN package and tray dimensions are annotated in Figure 16 and defined in Table 29 and Table 30 on page 41.

Figure 16. QFN Package and Tray Dimensions

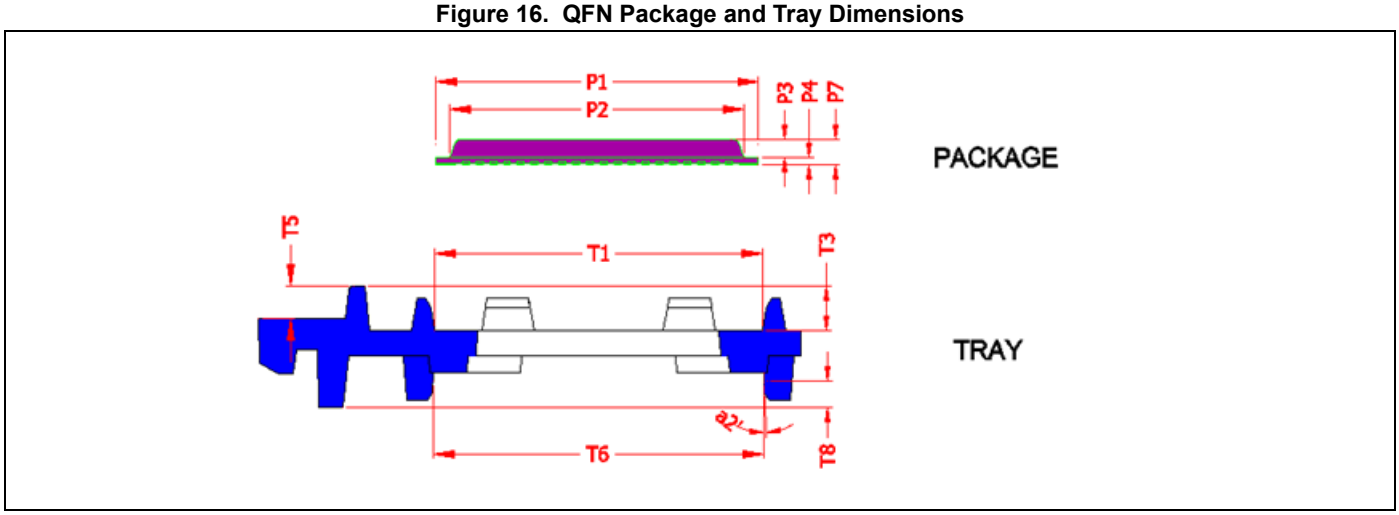


Table 29. QFN Package Dimensions and Tolerances

Parameter	Description	Nom.	Min.	Max.	± Tol.	Unit
P1	Package size	7	6.9	7.1	0.1	mm
P2	Top hat width	0	0	0	–	mm
P3	Top hat height	0	0	0	–	mm
P4	Substrate thickness	0.85	0.8	0.9	0.05	mm
P7	Total thickness (P3 + P4)	0.85	0.8	0.9	0.05	mm

Table 30. QFN Tray Dimensions and Tolerances

Parameter	Description	Nom.	Min.	Max.	± Tol.	Unit
T1	Top pocket size	7.25	7.17	7.33	0.08	mm
T3	Top pocket depth	1.75	1.5	2	0.25	mm
T5	Stacking height	2	1.87	2.13	0.13	mm
T6	Bottom pocket size	7.25	7.17	7.33	0.08	mm
T8	Bottom pocket depth	1.650	1.52	1.78	0.13	mm
a2	Bottom pocket relief wall draft angle	5	5	5	0	Degrees
T10	Packing value between two stacking trays	0.2	0.07	0.33	0.13	mm

5. Ordering Information

Table 31. Ordering Information

Part Number	Package	Ambient Operating Temperature
CYW20735PB1KML1G	60-pin QFN	0°C to 70°C

6. Additional Information

6.1 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (https://community.cypress.com/)

6.2 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

The following list of acronyms and abbreviations may appear in this document.

Term	Description
ADC	analog-to-digital converter
AFH	adaptive frequency hopping
AHB	advanced high-performance bus
APB	advanced peripheral bus
APU	audio processing unit
ARM7TDMI-S™	Acorn RISC Machine 7 Thumb instruction, Debugger, Multiplier, Ice, Synthesizable
BSC	Broadcom Serial Control
BTC	Bluetooth controller
COEX	coexistence
DFU	device firmware update
DMA	direct memory access
EBI	external bus interface
HCI	Host Control Interface
HV	high voltage
IDC	initial digital calibration
IF	intermediate frequency
IRQ	interrupt request
JTAG	Joint Test Action Group
LCU	link control unit
LDO	low drop-out
LHL	lean high land
LPO	low power oscillator

Term	Description
LV	LogicVision™
MIA	multiple interface agent
PDM	pulse density modulation
PLL	phase locked loop
PMU	power management unit
PWM	pulse width modulation
QD	quadrature decoder
RAM	random access memory
RC oscillator	A resistor-capacitor oscillator is a circuit composed of an amplifier, which provides the output signal, and a resistor-capacitor network, which controls the frequency of the signal.
RF	radio frequency
ROM	read -only memory
RX/TX	receive, transmit
SPI	serial peripheral interface
SW	software
SWD	serial wire debug
UART	universal asynchronous receiver/trans-mitter
UPI	µ-processor interface
WD	watchdog

Document History Page

Document Title: CYW20735B1, Single-Chip Bluetooth Transceiver for Wireless Input Devices Document Number: 002-14881			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	–	05/19/2015	20735-DS100-R Initial release.
*A	–	10/13/2015	20735-DS101-R See the release for the applicable change description.
*B	–	11/09/2015	20735-DS102-R Updated: Table 3: “Reference Crystal Electrical Specifications,” on page 21. Section 5: “Ordering Information,” on page 60: updated the part number for the QFN chip.
*C	–	12/04/2015	20735-DS103-R **Updated:** Table 3: “Reference Crystal Electrical Specifications,” on page 22. Table 9: “Core Buck Regulator,” on page 45. Table 10: “Digital LDO,” on page 46. Table 11: “PA LDO,” on page 47. Table 12: “RF LDO,” on page 48. Table 13: “Digital I/O Characteristics,” on page 49. Table 14: “BLE Current Consumption,” on page 49. Table 19: “UART Timing Specifications,” on page 54. **Added:** • “Tray Packaging Specifications” on page 60. **Removed** • Table 15: “BR Current Consumption,” on page 48. • “Tape and Reel Packaging Specifications,” on page 59.
*D	–	03/10/2016	20735-DS104-R **Updated:** Table 14: “BLE Current Consumption,” on page 46.
*E	–	05/26/2016	20735-DS105-R **Updated:** Table8:“Absolute Maximum Ratings,” on page42. Table13:“Core Buck Regulator,” on page44. Table14:“Digital LDO,” on page45. Table15:“PA LDO,” on page46. Table16:“RF LDO,” on page47. Table19:“ADC Microphone Specifications,” on page49. **Added:** “Table 9:“ESD/Latchup,” on page42. Table10:“Environmental Ratings,” on page43. Table11:“Recommended Operating Conditions,” on page43. Table12:“Shutdown Voltage,” on page43. “Power-On Reset” on page14. “Brownout Detection” on page14.
*F	5446946	09/29/2016	Updated to Cypress template.
*G	5688133	05/22/2017	Updated Specifications: Updated Timing and AC Characteristics: Updated UART Timing: Updated Table 24. Updated BSC Interface Timing: Added Table 28. Added Figure 13. Added Figure 14.

Document Title: CYW20735B1, Single-Chip Bluetooth Transceiver for Wireless Input Devices Document Number: 002-14881			
Revision	**ECN**	**Submission Date**	**Description of Change**
*H	6123642	04/18/2018	Replaced “BSC” with “I^2C” in all instances across the document. Removed “111-pin fine pitch ball grid array (FBGA)” package related information in all instances across the document. Updated Cypress Part Numbering Scheme: Updated table “Mapping Table for Part Number between Broadcom and Cypress”. Updated Bluetooth Baseband Core: Added Table 1. Bluetooth Features. Rearranged sections. Removed “Infrared Learning”. Updated Pin Assignments and GPIOs: Updated GPIO Pin Descriptions: Updated Table 7. Updated Functional Block Diagram: Updated Figure 1. Updated Ordering Information: Updated part numbers.
*I	6284060	08/17/2018	Updated document title to read as “CYW20735B1, Single-Chip Bluetooth Transceiver for Wireless Input Devices”. Replaced “CYW20735” with “CYW20735B1” in all instances across the document. Removed “Cypress Part Numbering Scheme”. Updated Features: Updated almost entire section. Updated Functional Block Diagram: Updated Figure 1. Updated Pin Assignments and GPIOs: Updated Pin Assignments: Updated Table 6. Updated GPIO Pin Descriptions: Updated Table 7. Updated Pinouts: Replaced “Ball Maps” with “Pinouts” in heading. Updated Ordering Information: Updated part numbers.
*J	6737859	11/26/2019	Updated Specifications: Updated Electrical Characteristics: Updated PA LDO: Updated Table 16. Updated RF Specifications: Updated Table 22.
*K	6785611	01/28/2020	Updated Features: Updated Peripherals and Communication: Removed “1x MIPI DMI-C interface”.
*L	7218581	08/10/2021	Updated Ordering Information: Updated part numbers. Completing Sunset Review.

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