



**THE DATASHEET OF
TCLAMP2472S.TCT**

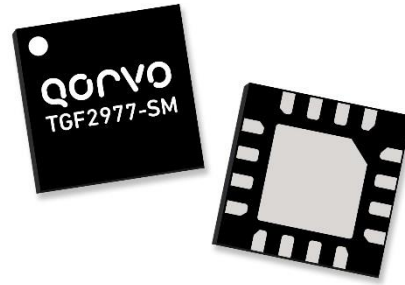


Product Overview

The Qorvo TGF2977-SM is a 5 W (P_{3dB}) discrete GaN on SiC HEMT which operates from DC to 12 GHz and 32 V supply. The device is in an industry standard overmolded package and is ideally suited for avionics, military, marine and weather radar. The device can support pulsed and linear operations.

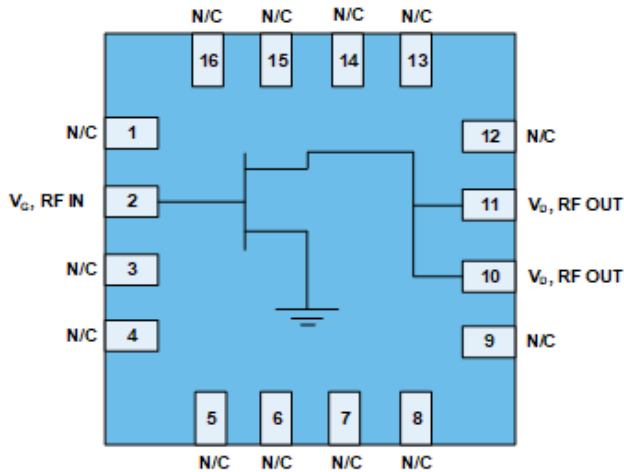
Lead-free and ROHS compliant.

Evaluation boards are available upon request.



3 x 3mm Package

Functional Block Diagram



Key Features

- Frequency: DC to 12 GHz
 - Output Power (P_{3dB})¹: 4.8 W
 - Linear Gain¹: 13 dB
 - Typical PAE_{3dB}¹: 50%
 - Operating Voltage: 32 V
 - CW and Pulse capable
- Note 1: @ 9 GHz Load Pull

Applications

- Military radar
- Commercial radar
 - Avionics
 - Marine
 - Weather

Ordering info

Part No.	Description
TGF2977-SM	QFN Packaged Part
TGF2977-SMEVB01	9 – 10 GHz EVB
TGF2977-SMEVB02	2.6 – 4.2 GHz EVB



Absolute Maximum Ratings¹

Parameter	Rating	Units
Breakdown Voltage, V_{BD}	+100	V
Gate Voltage Range, V_G	-7 to +2	V
Drain Current, $I_{D_{MAX}}$	0.6	A
Power Dissipation, CW (P_{DISS})	9.3 ²	W
RF Input Power, CW, $T_{amb} = 25^\circ\text{C}$	+30	dBm
Mounting Temperature (30 Seconds)	320	$^\circ\text{C}$
Storage Temperature	-65 to +150	$^\circ\text{C}$

Notes:

1. Operation of this device outside the parameter ranges given above may cause permanent damage.
2. Device base temperature = 85°C .

Recommended Operating Conditions¹

Parameter	Min	Typ	Max	Units
Operating Temp. Range	-40	+25	+85	$^\circ\text{C}$
Drain Voltage Range, V_D		+32	+40	V
Drain Bias Current, I_{DQ}		25		mA
Drain Current, I_D^4	-	325	-	mA
Gate Voltage, V_G^3	-	-2.8	-	V
Power Dissipation (P_D) ^{2,4}	-	-	9.2	W
Power Dissipation (P_D), CW ²	-	-	7.4	W

Notes:

1. Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.
2. Package base at 85°C
3. To be adjusted to desired I_{DQ}
4. Pulsed, 100uS PW, 20% DC

Measured Load Pull Performance – Power Tuned¹

Parameter	Typical Values						Units
	5	6	8	9	10	12	
Frequency, F	5	6	8	9	10	12	GHz
Drain Voltage, V_D	32	32	32	32	32	32	V
Drain Bias Current, I_{DQ}	25	25	25	25	25	25	mA
Output Power at 3dB compression, P_{3dB}	37.5	37.2	37.0	36.8	36.8	36.5	dBm
Drain Efficiency at 3dB compression, $DEFF_{3dB}$	53.6	58.6	55.0	51.3	48.9	45.2	%
Gain at 3dB compression, G_{3dB}	15.2	14.4	11.4	9.8	8.3	5.3	dB

Notes:

1. Pulsed, 100 uS Pulse Width, 20% Duty Cycle
2. Characteristic Impedance, $Z_o = 15 \Omega$.

Measured Load Pull Performance – Efficiency Tuned¹

Parameter	Typical Values						Units
	5	6	8	9	10	12	
Frequency, F	5	6	8	9	10	12	GHz
Drain Voltage, V_D	32	32	32	32	32	32	V
Drain Bias Current, I_{DQ}	25	25	25	25	25	25	mA
Output Power at 3dB compression, P_{3dB}	37.2	36.3	35.7	36.0	35.5	36.1	dBm
Drain Efficiency at 3dB compression, $DEFF_{3dB}$	62	64.4	60.4	57.2	54.1	51.8	%
Gain at 3dB compression, G_{3dB}	15.5	14.8	12.0	10.4	8.9	5.8	dB

Notes:

1. Pulsed, 100 uS Pulse Width, 20% Duty Cycle
2. Characteristic Impedance, $Z_o = 15 \Omega$.

9 – 10 GHz EVB 9.4 GHz Performance¹

Parameter	Min	Typ	Max	Units
Linear Gain, G_{LIN}	–	10.1	–	dB
Output Power at 3dB compression point, P3dB	–	3.6	–	W
Drain Efficiency at 3dB compression point, DEFF3dB	–	48.4	–	%
Gain at 3dB compression point, G3dB	–	7.1	–	dB
Gate Leakage, $V_D = 10V$, $V_G = -3.7$	-1.4			mA

Notes:

1. $V_D = +32V$, $I_{DQ} = 35mA$, Temp = +25 °C, Pulse Width = 100 uS, Duty Cycle = 20%

RF Characterization – Mismatch Ruggedness at 9.4 GHz

Symbol	Parameter	dB Compression	Typical
VSWR	Impedance Mismatch Ruggedness	3	10:1

Test conditions unless otherwise noted: $T_A = 25$ and -40 °C, $V_D = 32V$, $I_{DQ} = 35mA$

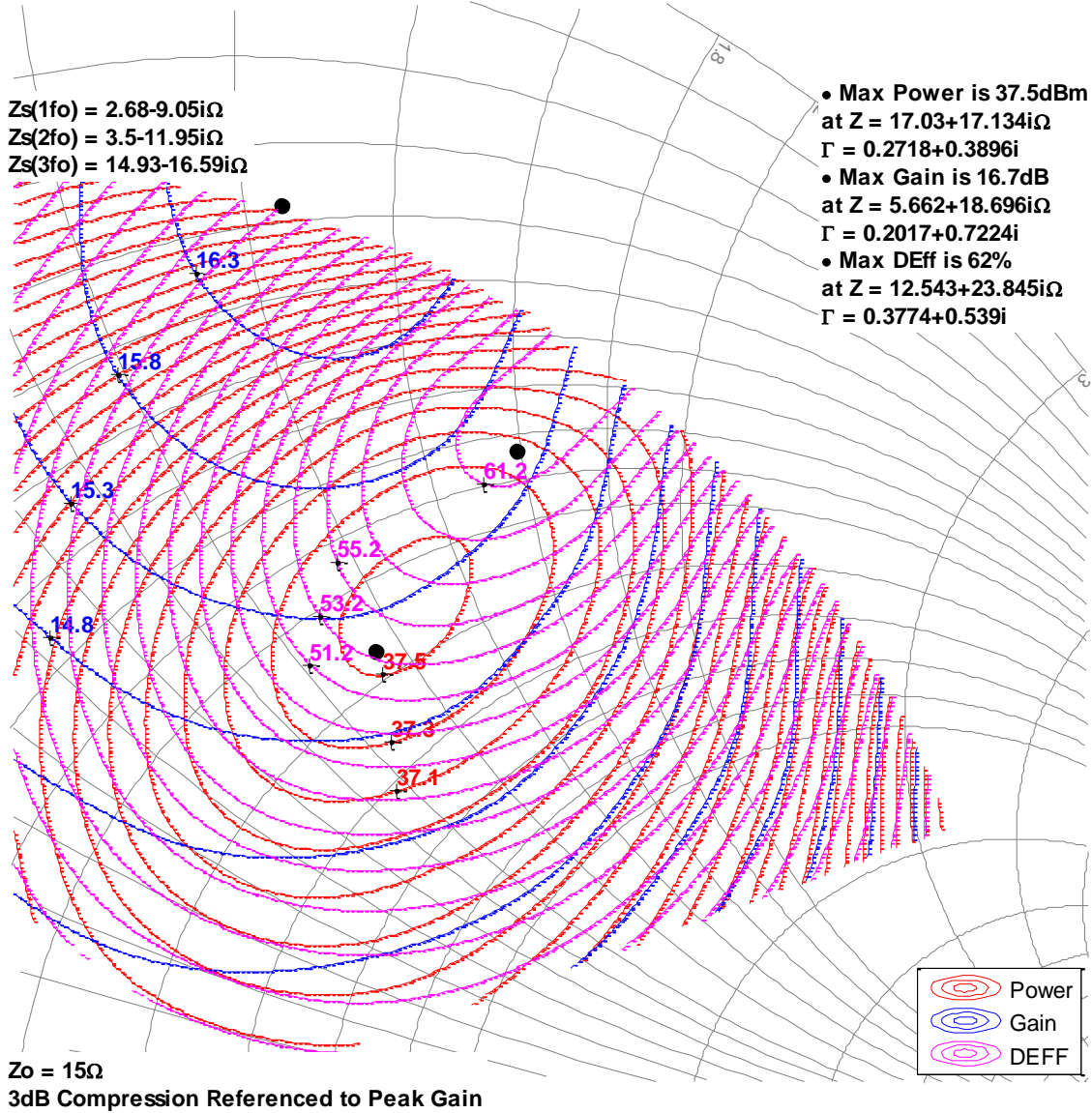
Input drive power is determined at pulsed 3dB compression under matched condition at EVB output connector.

Measured Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$, 100 uS Pulse Width, 20% Duty Cycle
2. See page 20 for load pull reference planes where the performance was measured.

5GHz, Load-pull

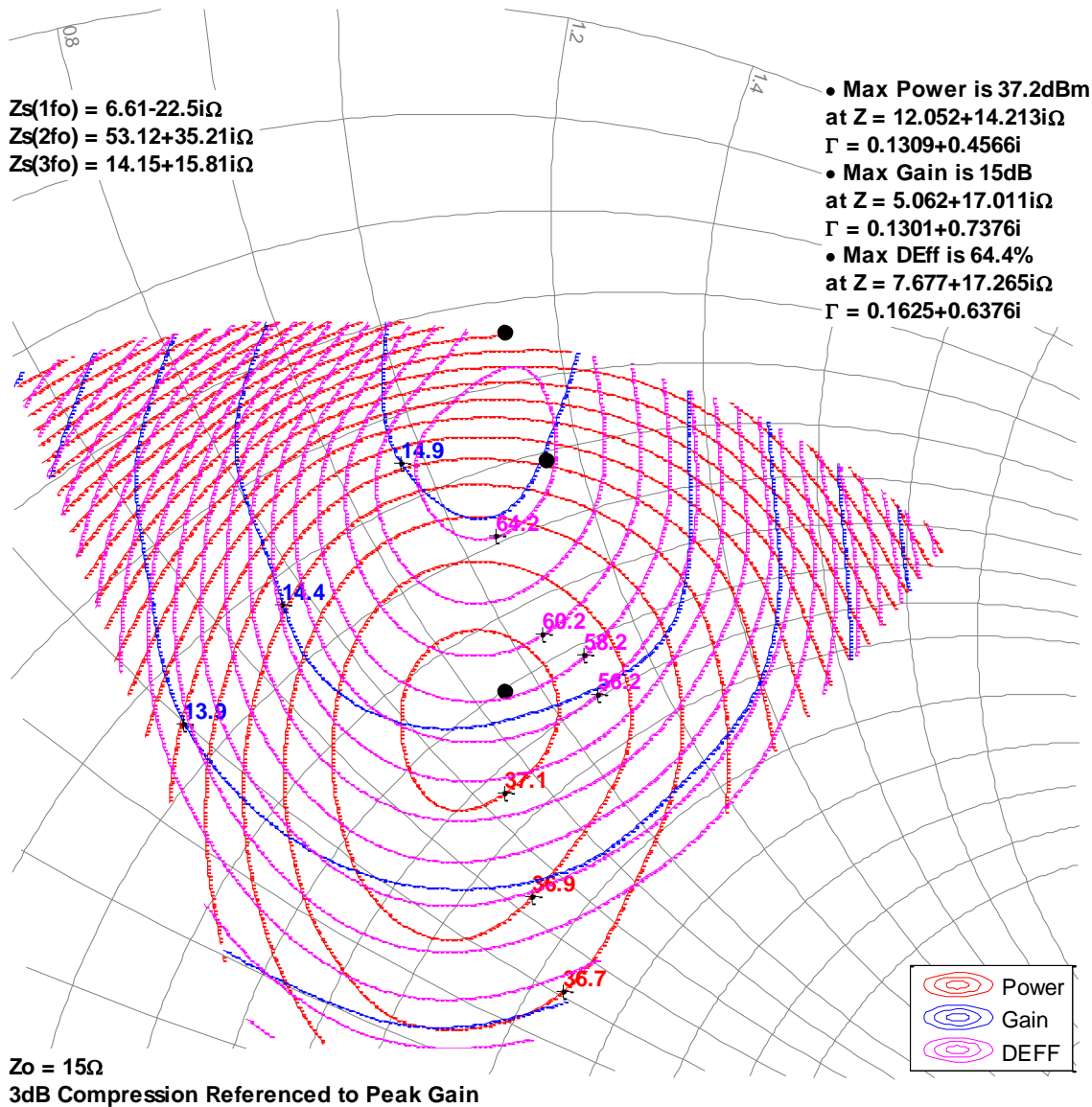


Measured Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$, 100 uS Pulse Width, 20% Duty Cycle
2. See page 20 for load pull reference planes where the performance was measured.

6GHz, Load-pull

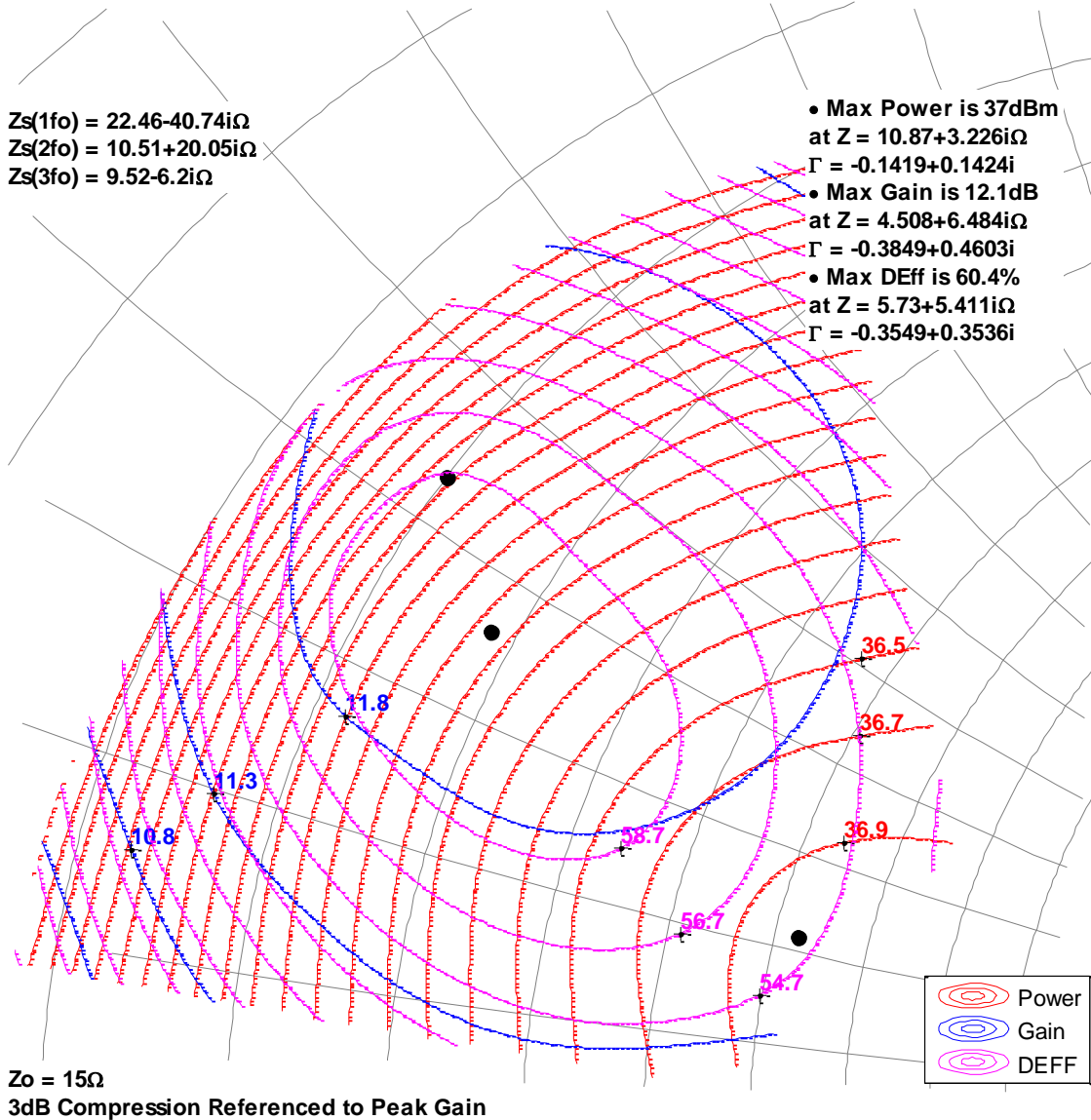


Measured Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$, 100 uS Pulse Width, 20% Duty Cycle
2. See page 20 for load pull reference planes where the performance was measured.

8GHz, Load-pull

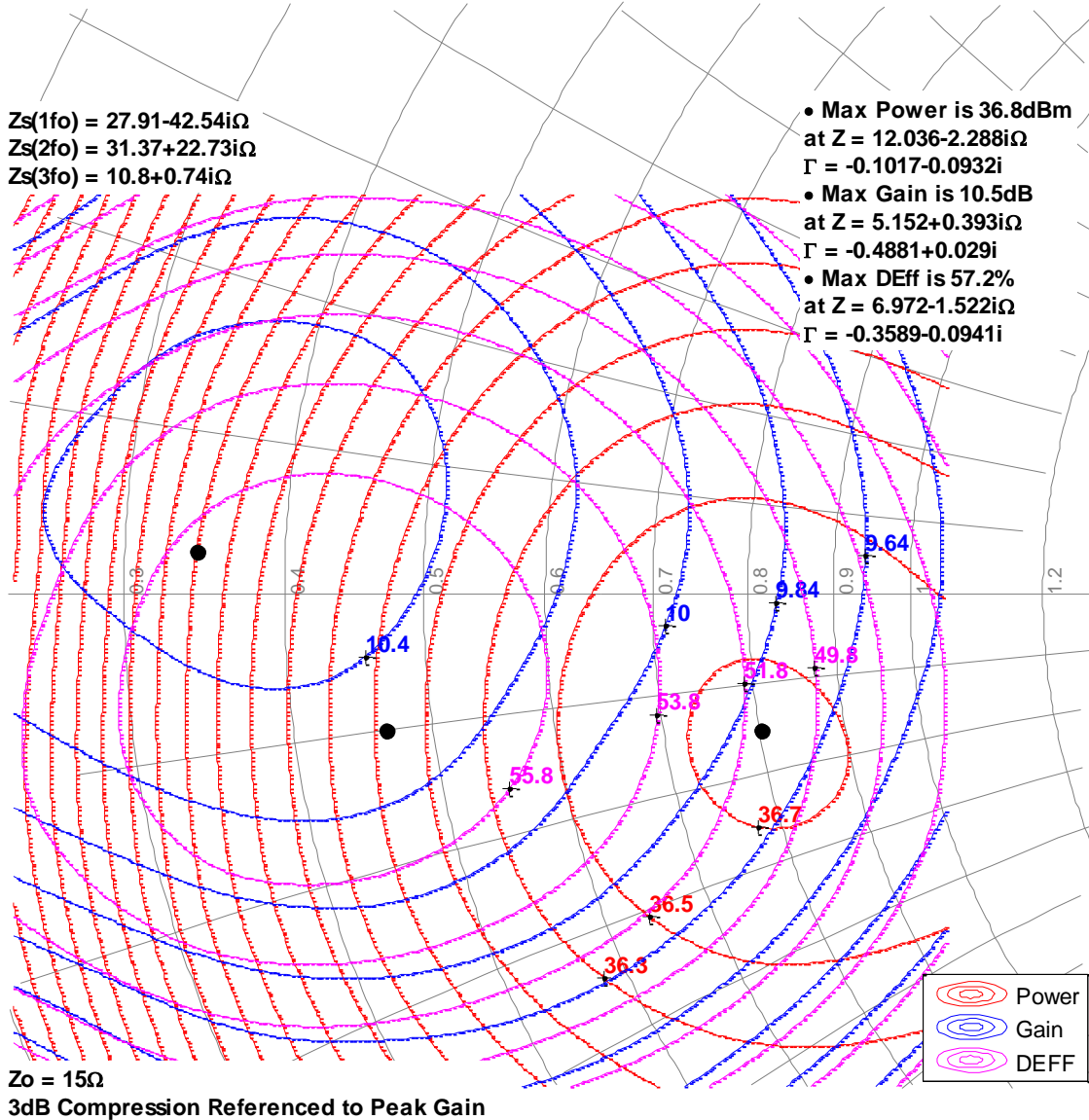


Measured Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$, 100 uS Pulse Width, 20% Duty Cycle
2. See page 20 for load pull reference planes where the performance was measured.

9GHz, Load-pull

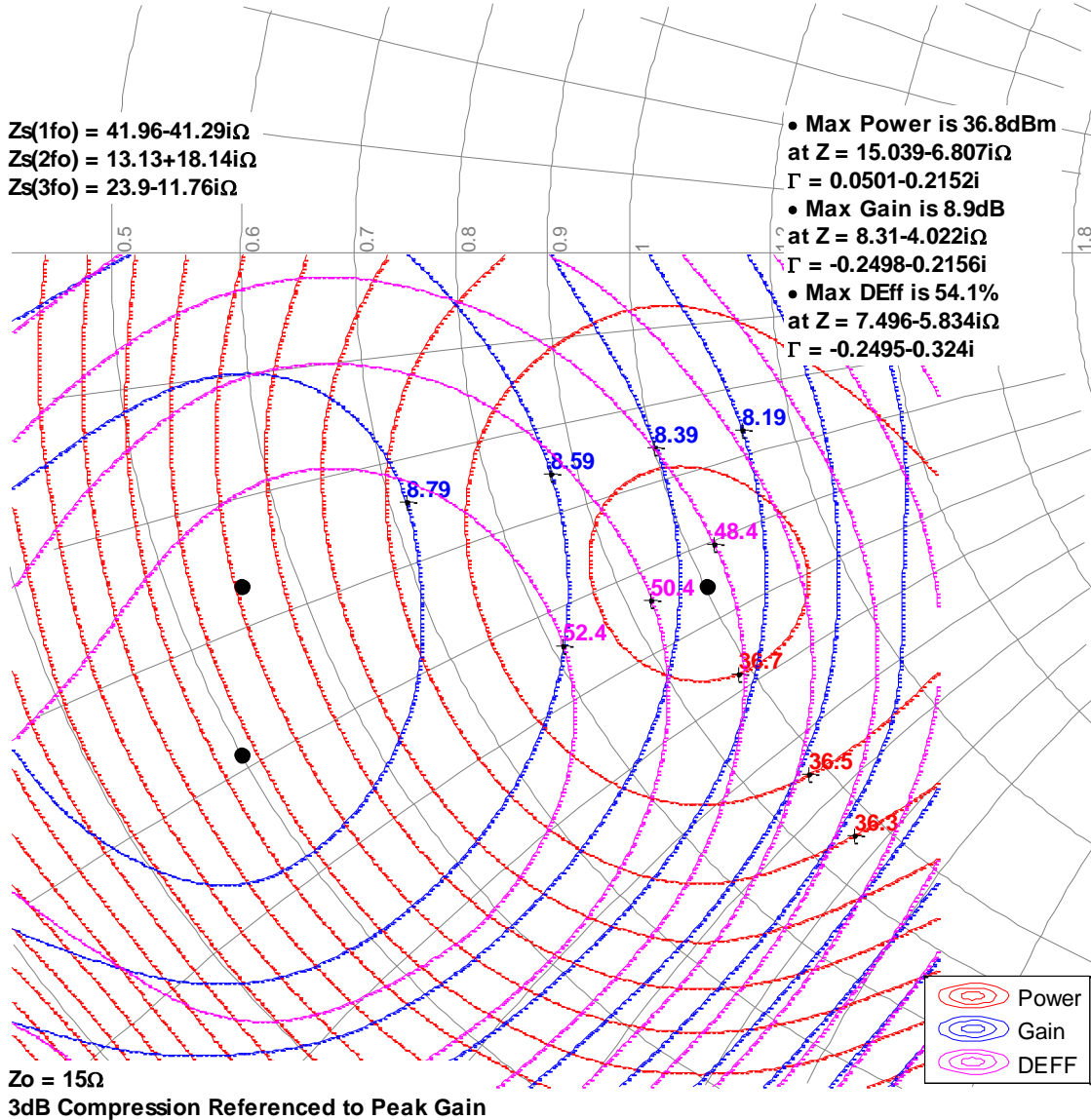


Measured Load-Pull Smith Charts^{1, 2}

Notes:

1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$, 100 μS Pulse Width, 20% Duty Cycle
2. See page 20 for load pull reference planes where the performance was measured.

10GHz, Load-pull

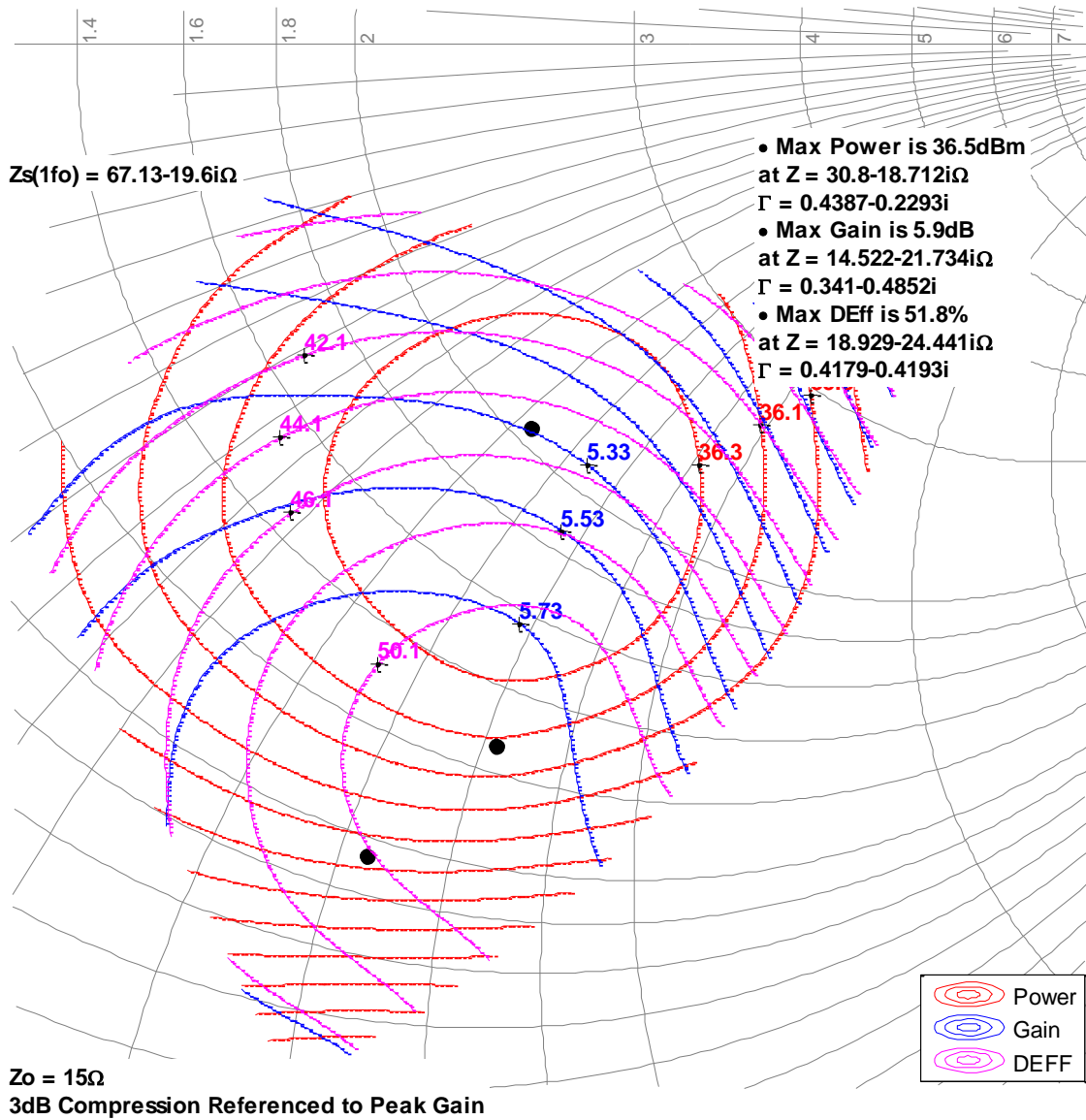


Measured Load-Pull Smith Charts^{1,2}

Notes:

1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$, 100 uS Pulse Width, 20% Duty Cycle
2. See page 20 for load pull reference planes where the performance was measured.

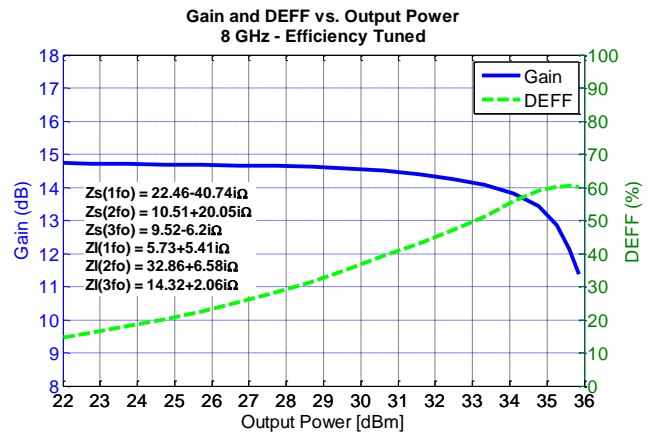
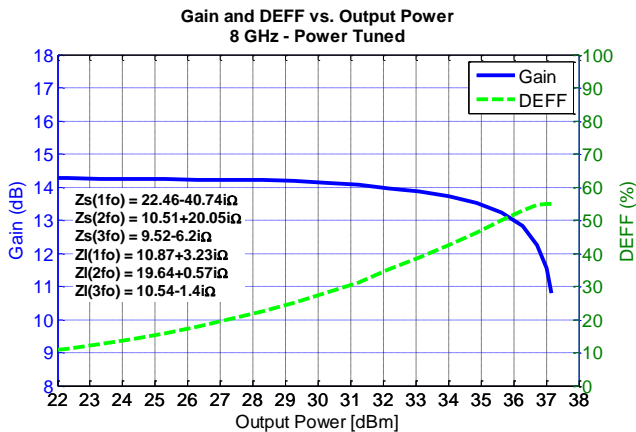
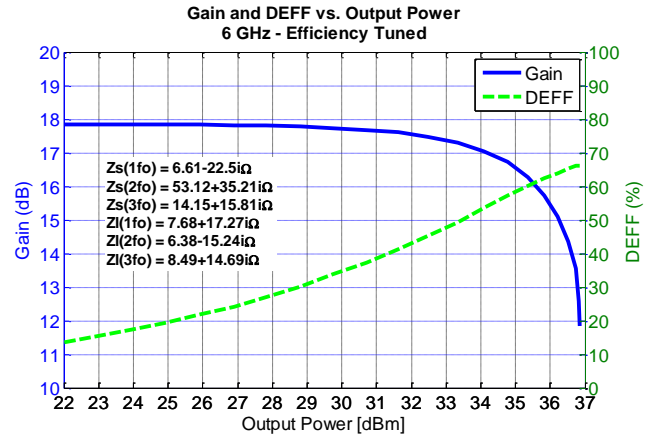
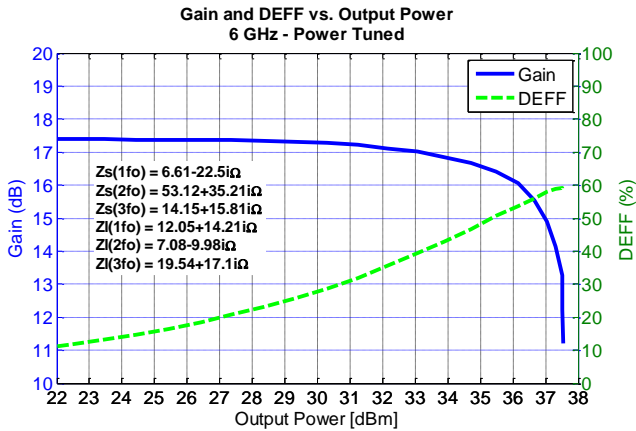
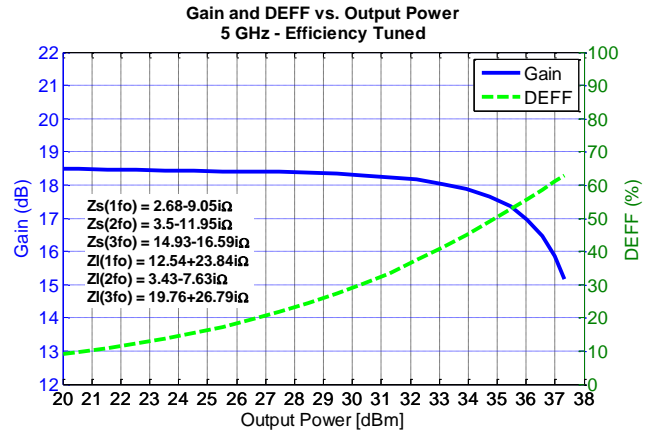
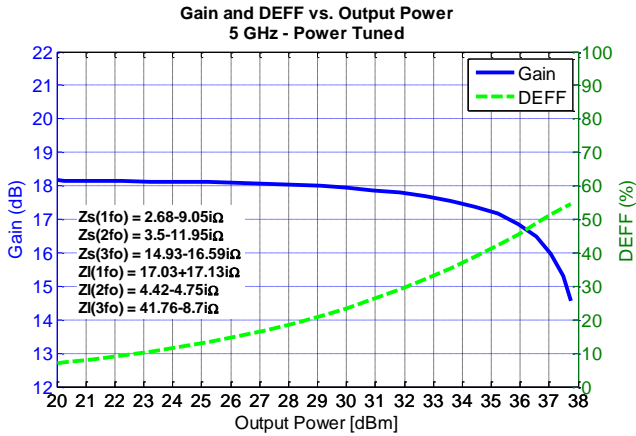
12GHz, Load-pull



Typical Measured Performance – Load-Pull Drive-up^{1, 2}

Notes:

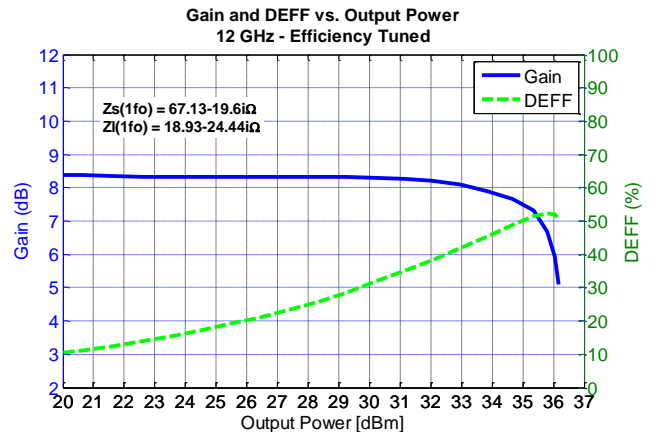
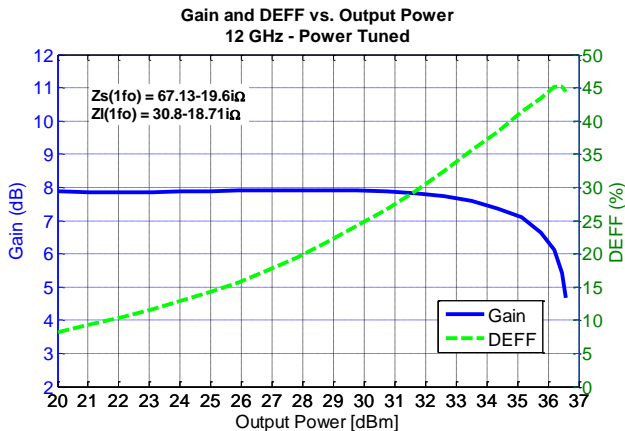
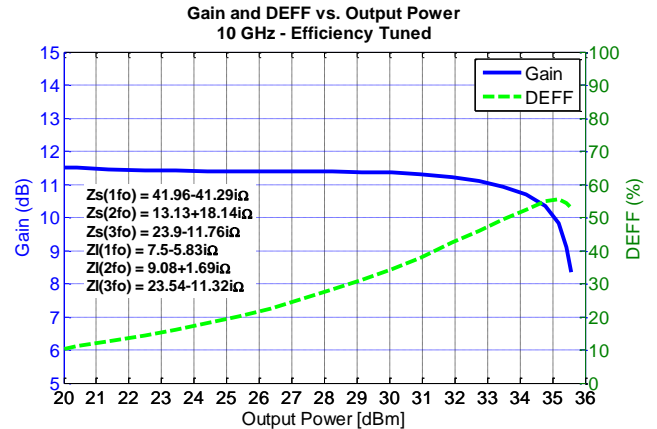
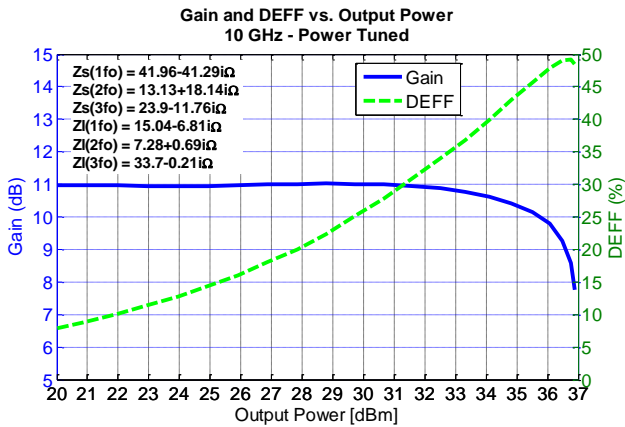
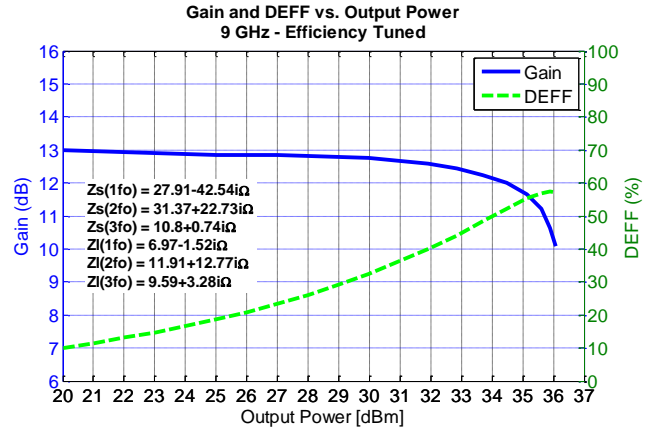
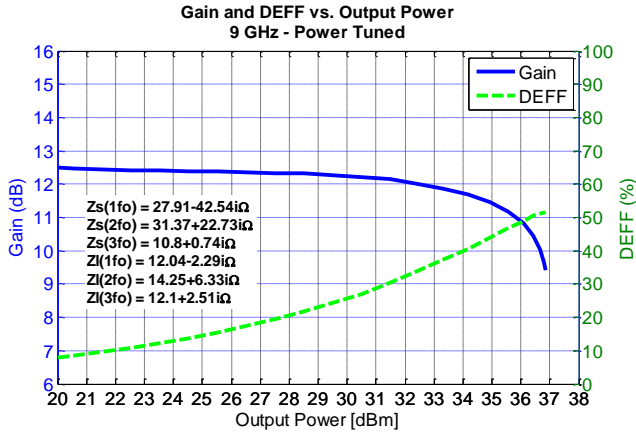
1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$, 100 μs Pulse Width, 20% Duty Cycle
2. See page 20 for load-pull and source-pull reference planes where the performance was measured.



Typical Measured Performance – Load-Pull Drive-up^{1, 2}

Notes:

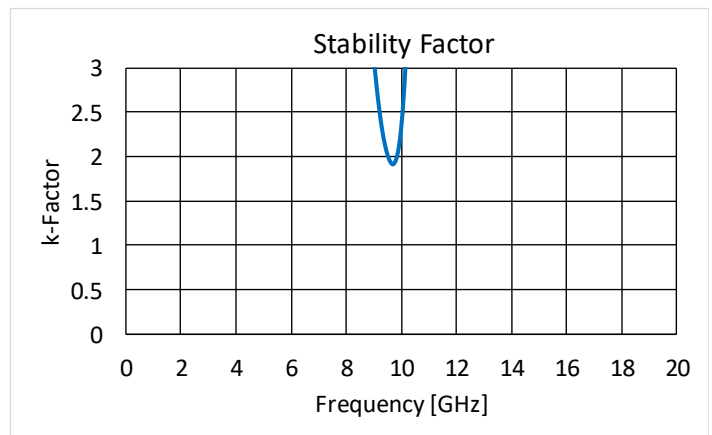
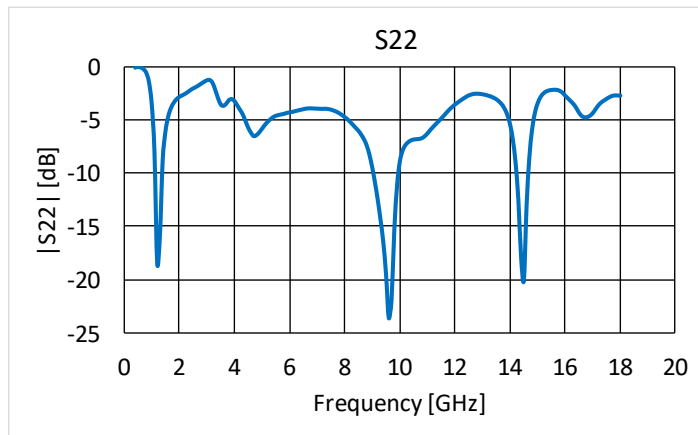
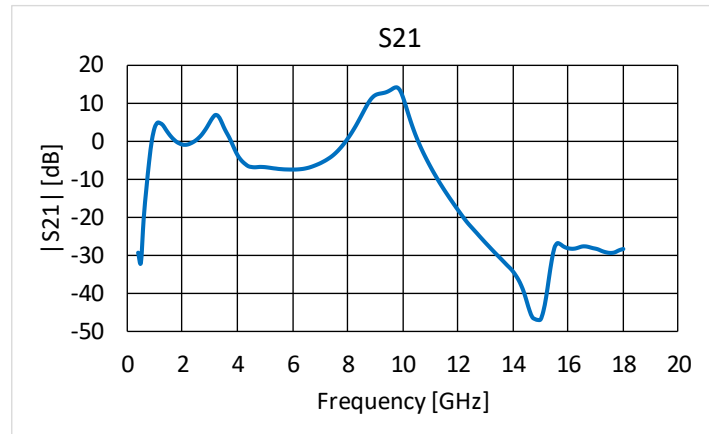
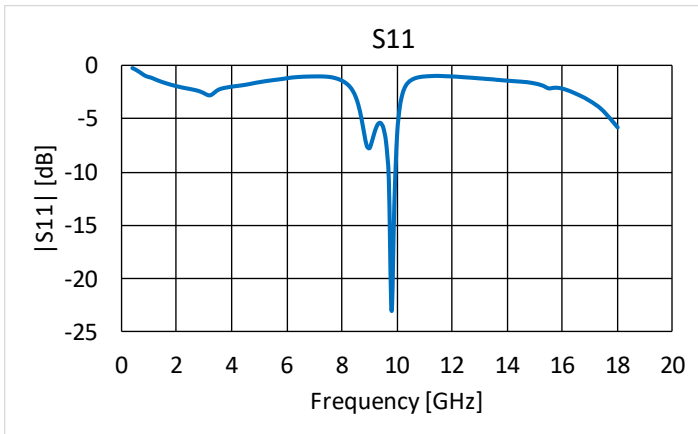
1. C Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$, 100 μs Pulse Width, 20% Duty Cycle
2. See page 20 for load-pull and source-pull reference planes where the performance was measured.



S-Parameters Of 9 – 10 GHz EVB at -40°C¹

Notes:

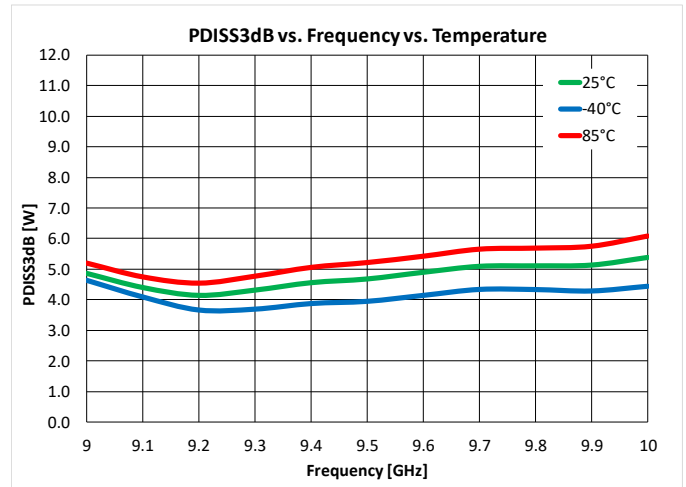
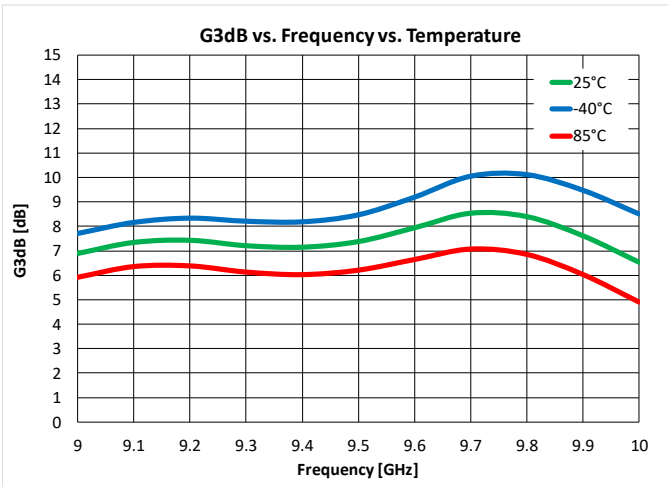
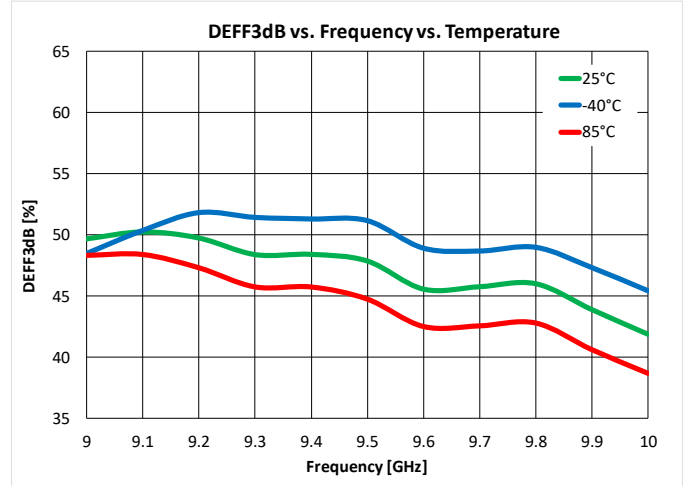
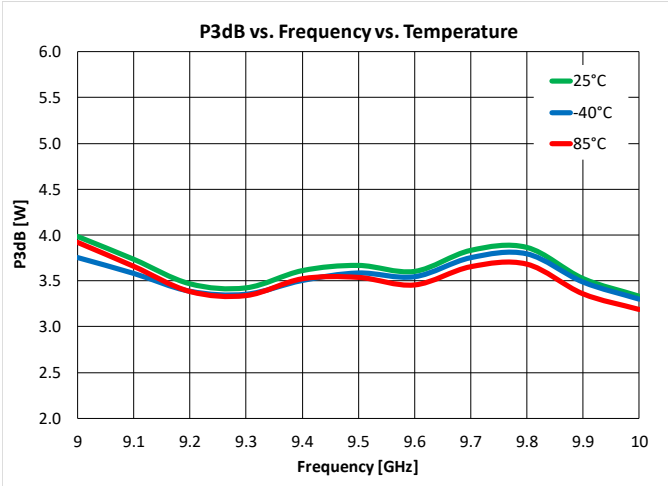
1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 35\text{ mA}$



Power Driveup Performance Over Temperatures Of 9 – 10 GHz EVB¹

Notes:

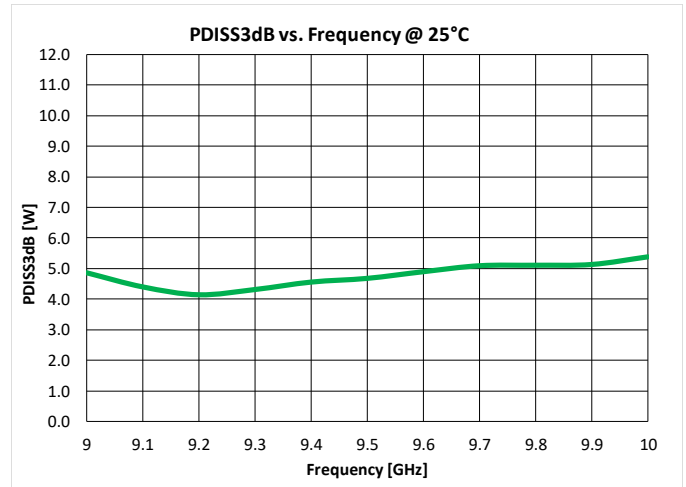
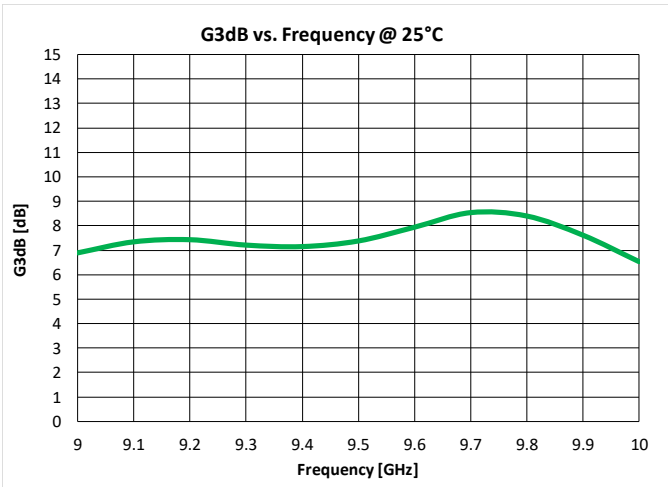
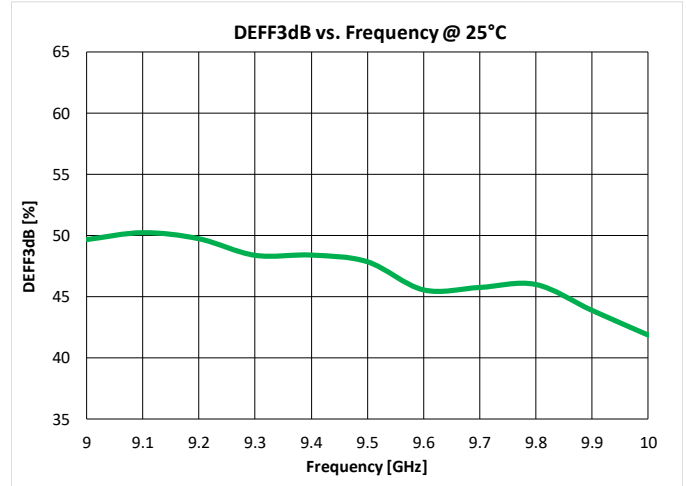
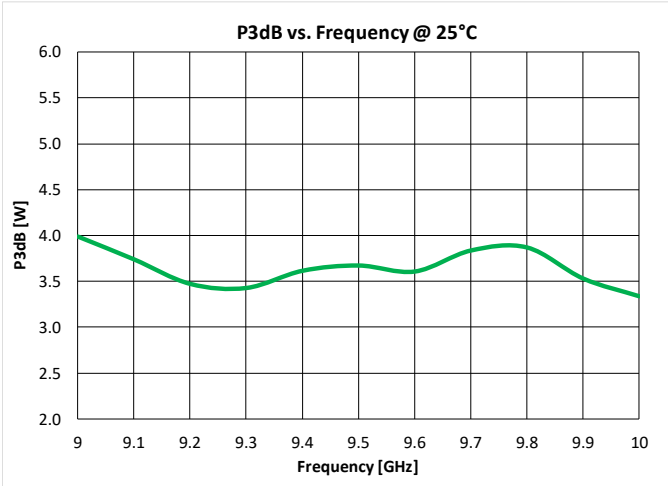
1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 35\text{ mA}$, 100 μs Pulse Width, 20% Duty Cycle



Power Driveup Performance At 25°C Of 9 – 10 GHz EVB^{1,2}

Notes:

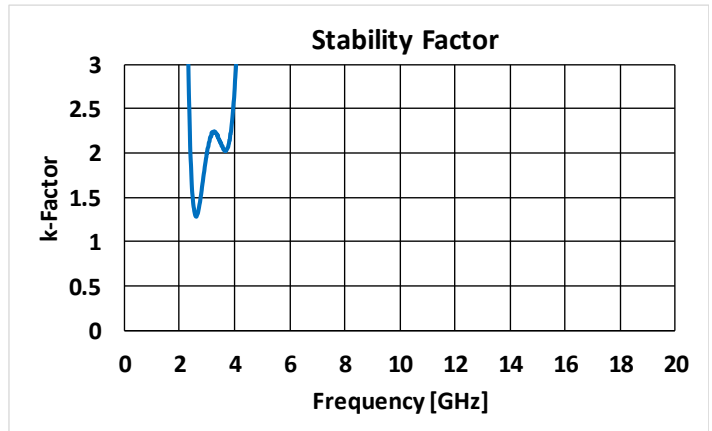
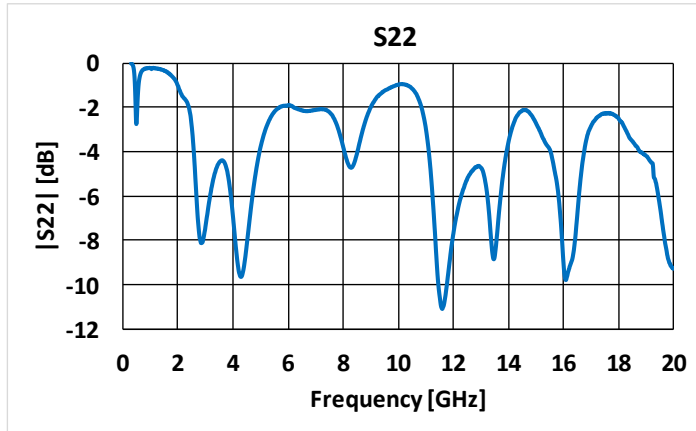
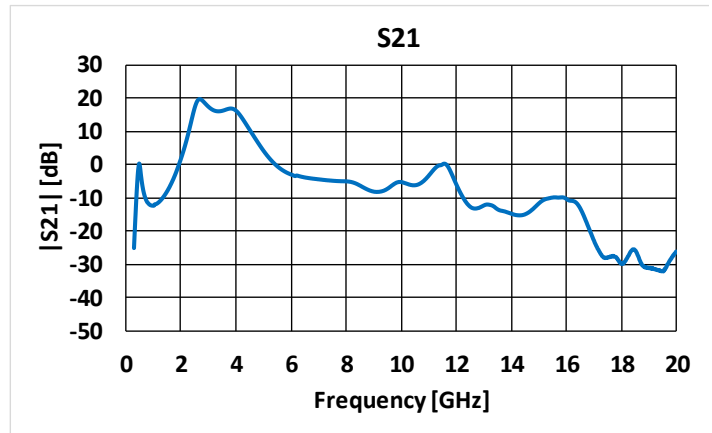
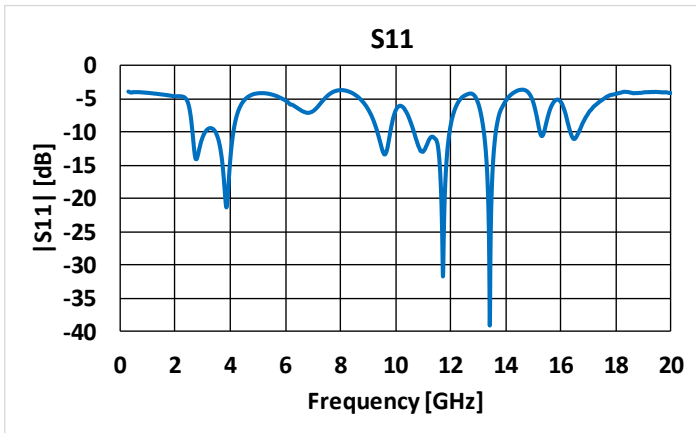
1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 35\text{ mA}$, 100 μs Pulse Width, 20% Duty Cycle



S-Parameters Of 2.6 – 4.2GHz EVB¹

Notes:

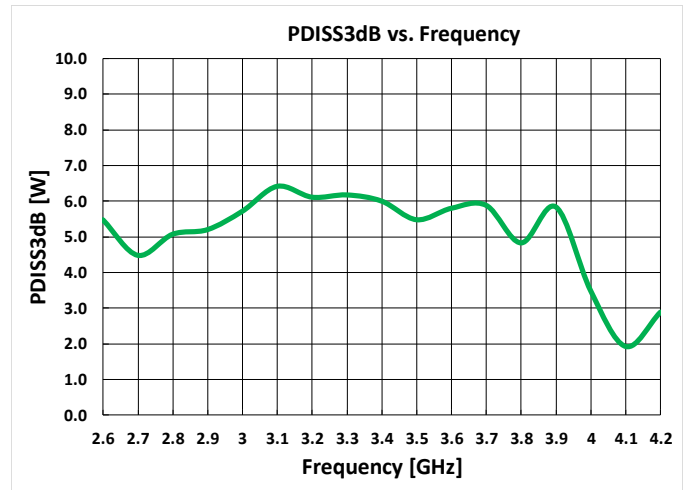
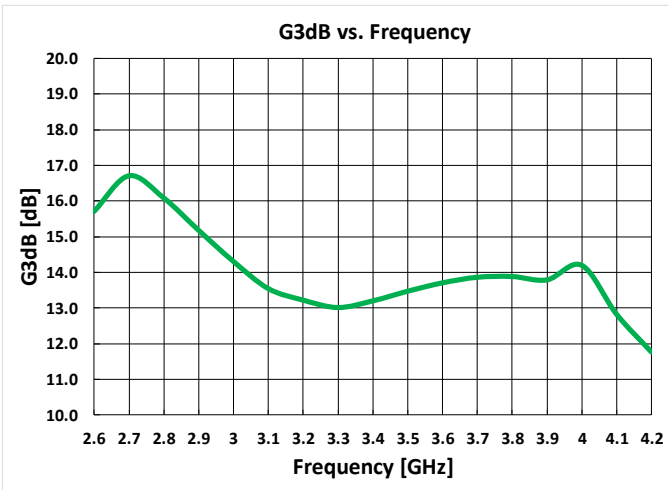
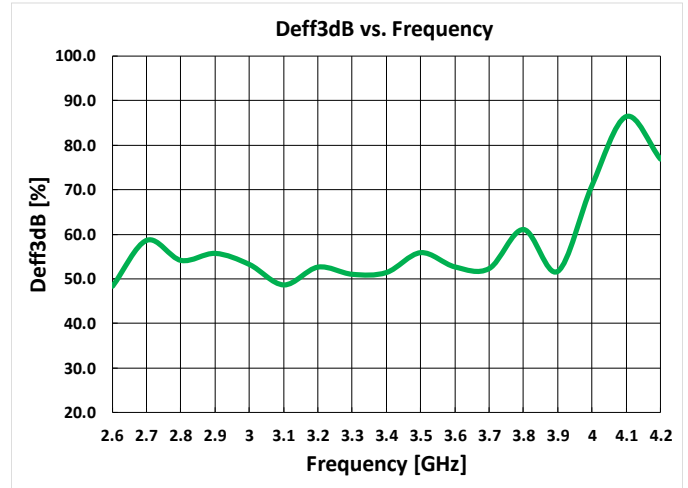
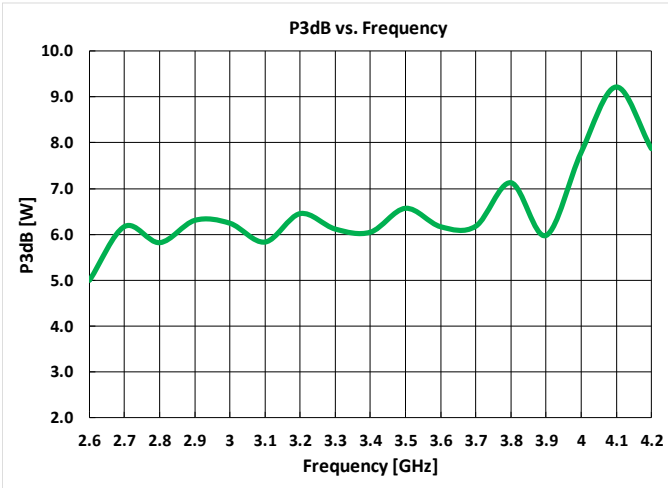
1. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$, $T = 25^\circ\text{C}$

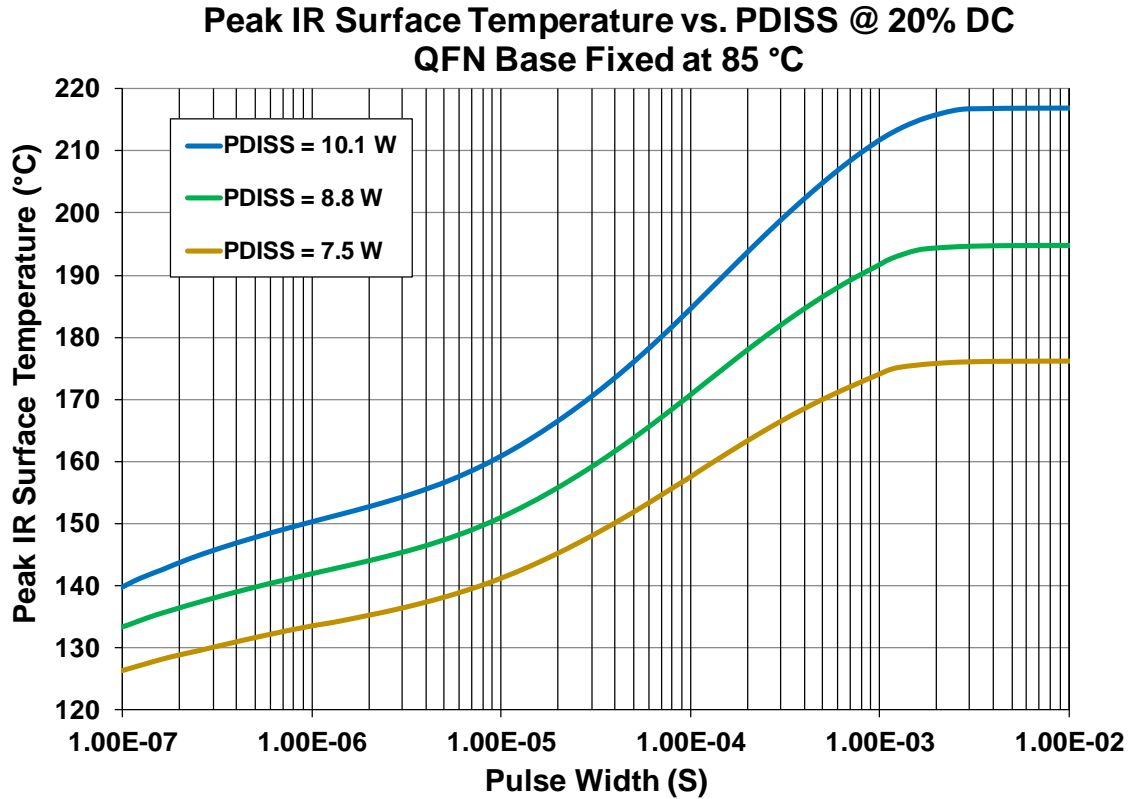


Power Driveup Performance Of 2.6 – 4.2GHz EVB^{1,2}

Notes:

2. Test Conditions: $V_D = 32\text{ V}$, $I_{DQ} = 25\text{ mA}$, 100 uS Pulse Width, 20% Duty Cycle, $T = 25^\circ\text{C}$
3. The dissipation power is conservative because it is specified at DUT only without accounting for the loss of the output matching network..

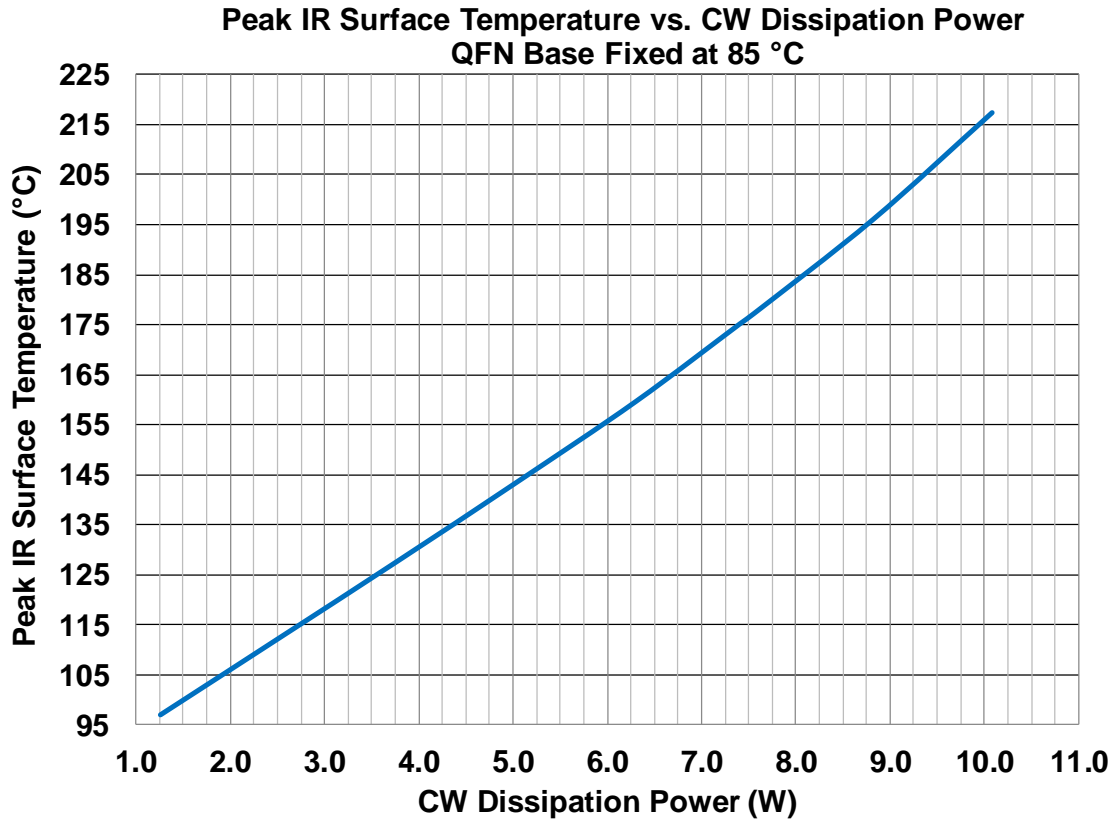


Thermal and Reliability Information – Pulsed¹


Parameter	Conditions	Values	Units
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	9.9	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	10.1 W PDISS, 100uS PW, 20%	185	°C
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	9.8	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	9.2 W PDISS, 100uS PW, 20%	175	°C
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	9.7	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	8.8 W PDISS, 100uS PW, 20%	171	°C

¹Refer to the following document [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

Thermal and Reliability Information – CW^{1, 2, 3}

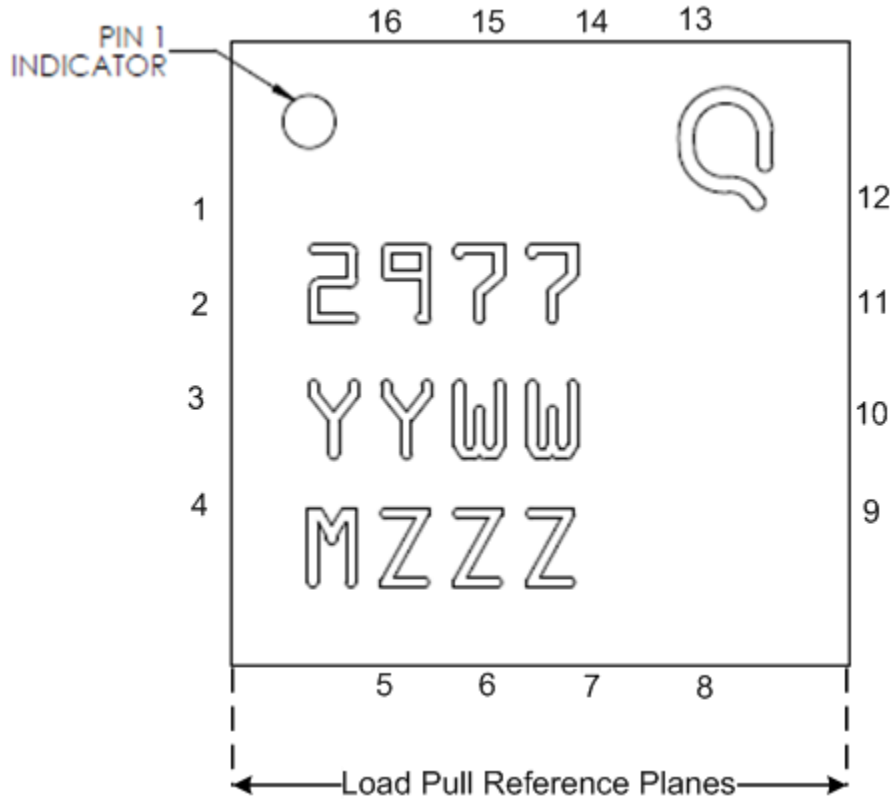


Parameter	Conditions	Values	Units
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	13.1	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	10.1 W Pdiss, CW	217	°C
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	12.6	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	8.8 W Pdiss, CW	196	°C
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	12.2	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	7.4 W Pdiss, CW	175	°C
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	11.9	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	6.3 W Pdiss, CW	160	°C
Thermal Resistance, IR ¹ (θ_{JC})	85 °C Case	11.6	°C/W
Peak IR Surface Temperature ¹ (T_{CH})	5.0 W Pdiss, CW	144	°C

¹Refer to the following document [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

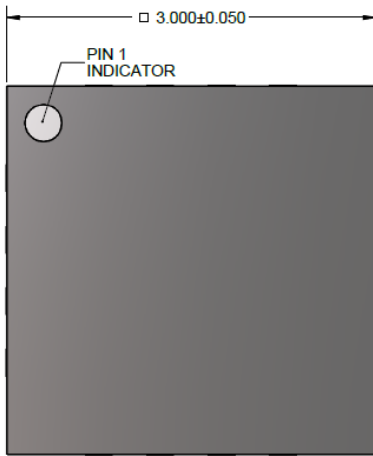
Pin Configuration and Description¹

Note 1: The TGF2977-SM will be marked with the “2977” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the calendar year the part was manufactured, the “WW” is the work week of the assembly lot start, the MZZZ” is the production lot number.

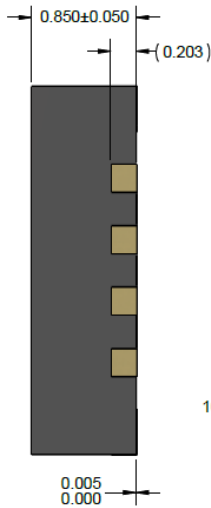


Pin	Symbol	Description
2	RF IN / V_G	Gate
10 - 11	RF OUT / V_D	Drain
1, 3 – 9, 12 - 16	NC	Not Connected
Back side	Source	Source / Ground / Backside of part

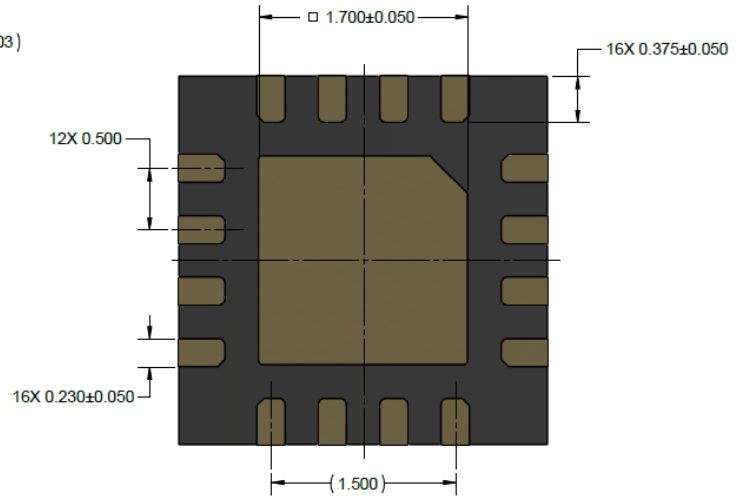
Mechanical Drawing¹



TOP VIEW



SIDE VIEW

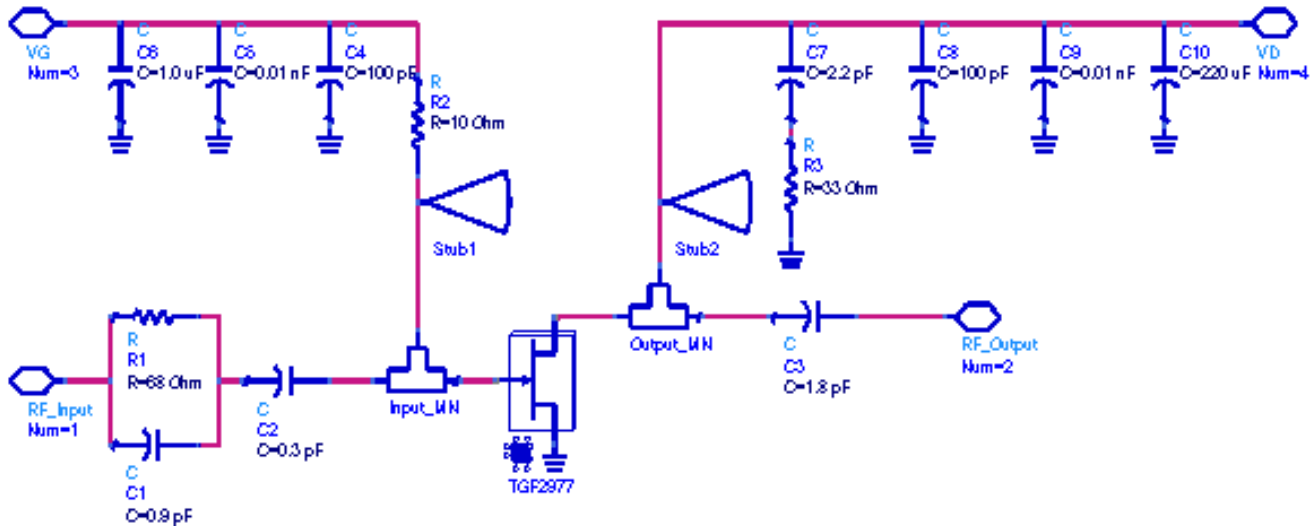


BOTTOM VIEW

Note 1:

1. All dimensions are in inches.
2. Unless otherwise noted, all dimension tolerances are ± 0.100 inches.
3. Package leads are gold plated.
4. Part is mold encapsulated.

9 – 10 GHz Application Circuit - Schematic



Bias-up Procedure

1. Set V_G to -4 V.
2. Set I_D current limit to 30 mA.
3. Apply 32 V V_D .
4. Slowly adjust V_G until I_D is set to 25 mA.
5. Set I_D current limit to 0.4 A (Pulsed operation)
6. Apply RF.

Bias-down Procedure

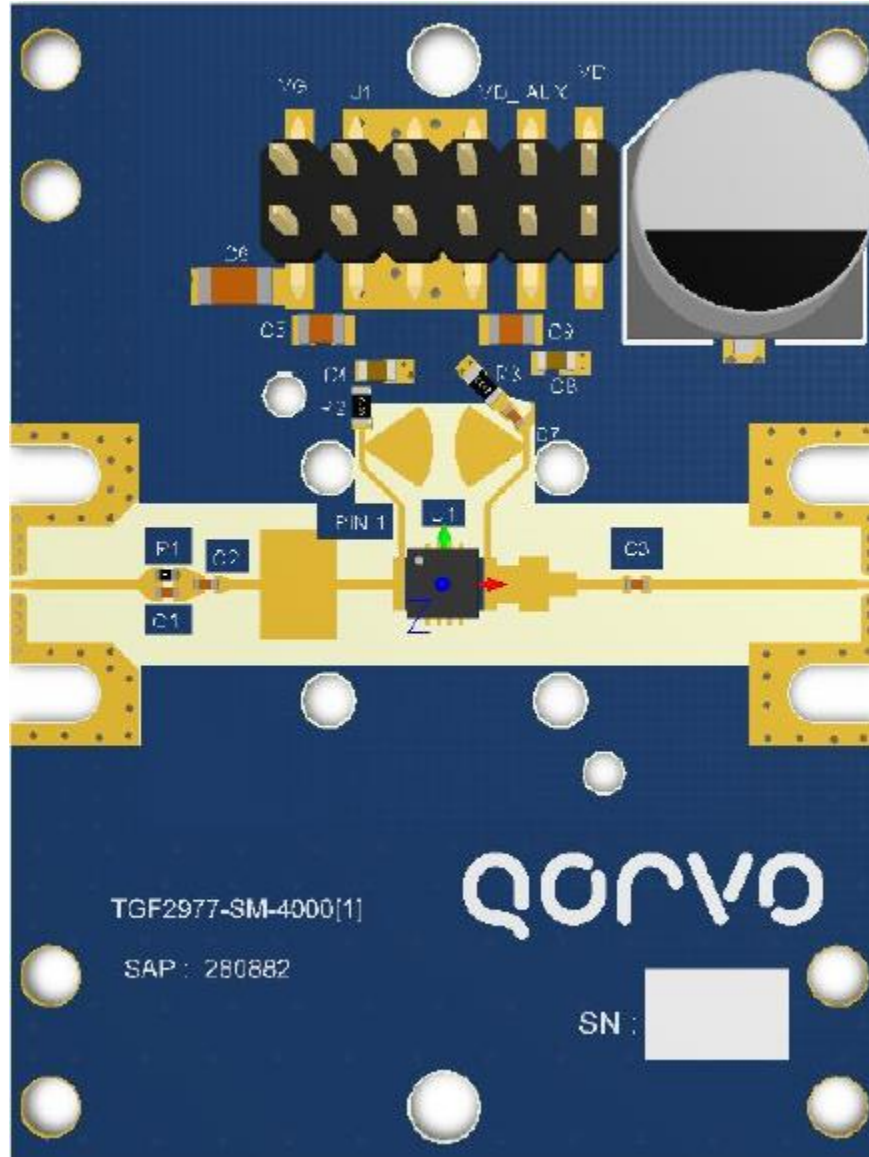
1. Turn off RF signal.
2. Turn off V_D
3. Wait 2 seconds to allow drain capacitor to discharge
4. Turn off V_G

9 – 10 GHz Application Circuit - Bill Of material

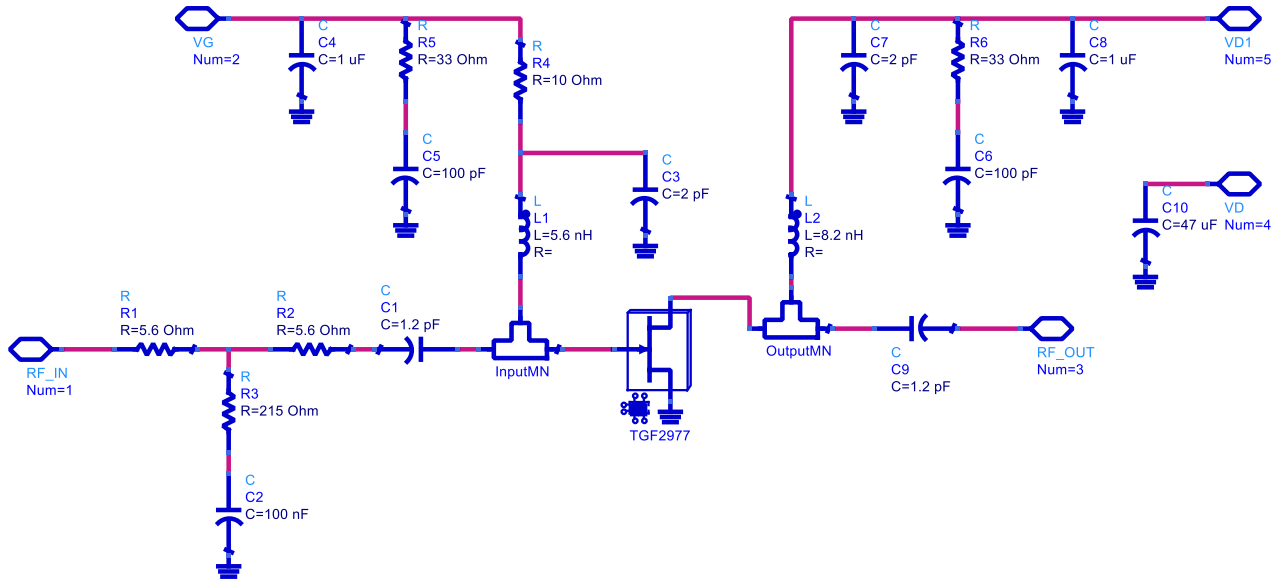
Description	Ref. Des.	Manufacturer	Part Number
Capacitor 0.9pF, 200V, 0402	C1	American Technical Ceramics	600L0R3AT200T
Capacitor 0.3 pF, 200V, 0402	C2	American Technical Ceramics	600L0R3AT200T
Capacitor 1.8 pF, 200V, 0402	C3	American Technical Ceramics	600L1R8AT200T
Capacitor 2.2 pF, 200V, 0402	C7	American Technical Ceramics	600L2R2BT200T
Capacitor 100 pF, 200V, 0603	C4, C8	Carpax Technologies	0603G101J201S
Capacitor 0.1 nF, 200V, 0603	C5, C9	Digi-Key	C0805C103K5RACTU
Capacitor 1 uF, 200V, 1206	C6	Digi-Key	C1206C105K4RACTU
Capacitor, Electrolytic, 47 uF, 50V, 10mm SMD	C16	Panasonic	EEETG1H470P
Resistor, 68 Ohm, 0402	R1	Panasonic	ERJ-2RKF68R0X
Resistor, 10 Ohm, 0603	R2		Generic 0603
Resistor, 33 Ohm, 0603	R3		Generic 0603

9 – 10 GHz Application Circuit - Layout

Board material is RO4003C 0.008" thickness with 1oz copper cladding. Overall EVB size is 1.5" x 2".



2.6 – 4.2 GHz Application Circuit - Schematic



Bias-up Procedure

1. Set V_G to -4 V.
2. Set I_D current limit to 30 mA.
3. Apply 32 V V_D .
4. Slowly adjust V_G until I_D is set to 25 mA.
5. Set I_D current limit to 0.5 A (Pulsed operation)
6. Apply RF.

Bias-down Procedure

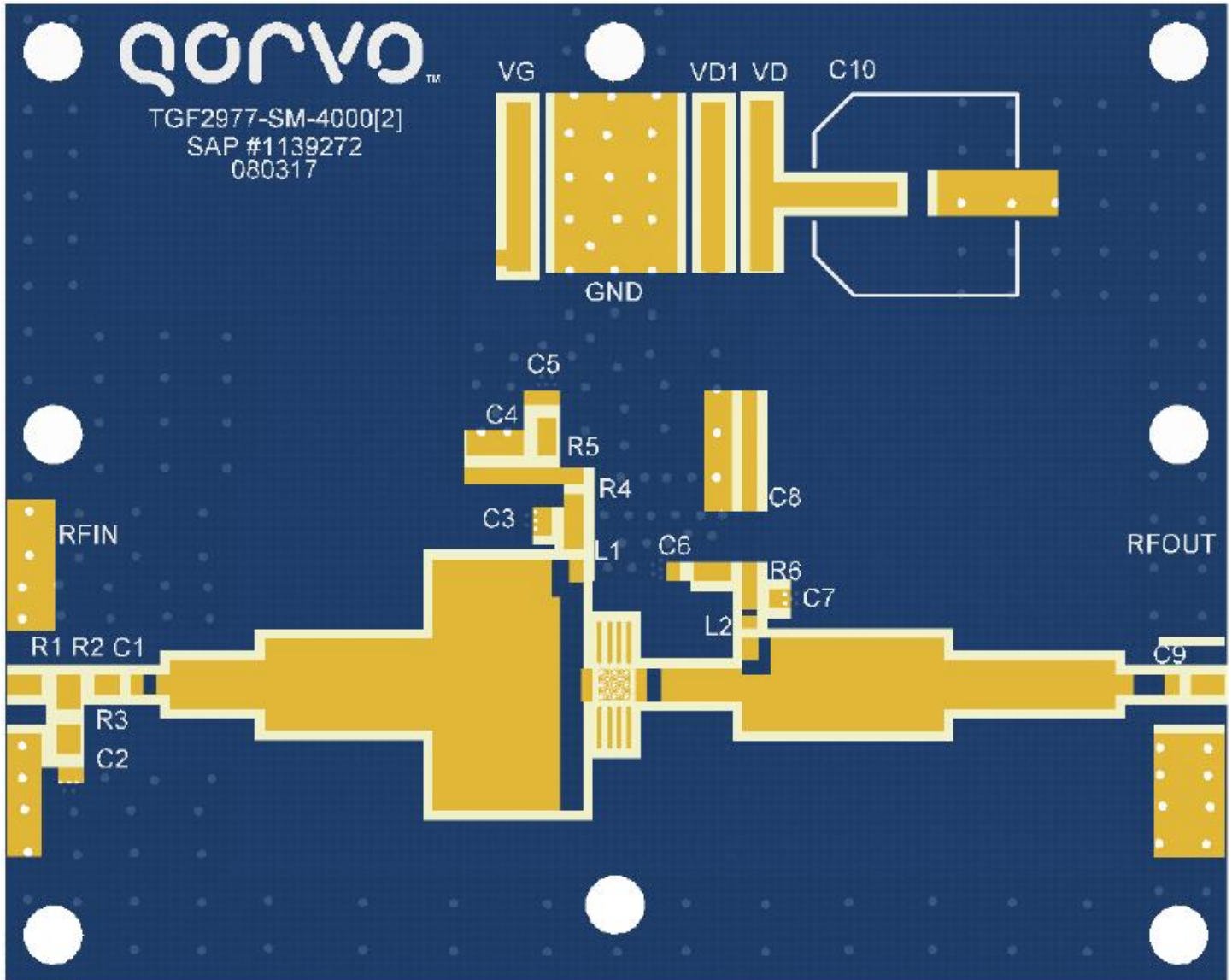
1. Turn off RF signal.
2. Turn off V_D
3. Wait 2 seconds to allow drain capacitor to discharge
4. Turn off V_G

2.6 – 4.2 GHz Application Circuit - Bill Of material

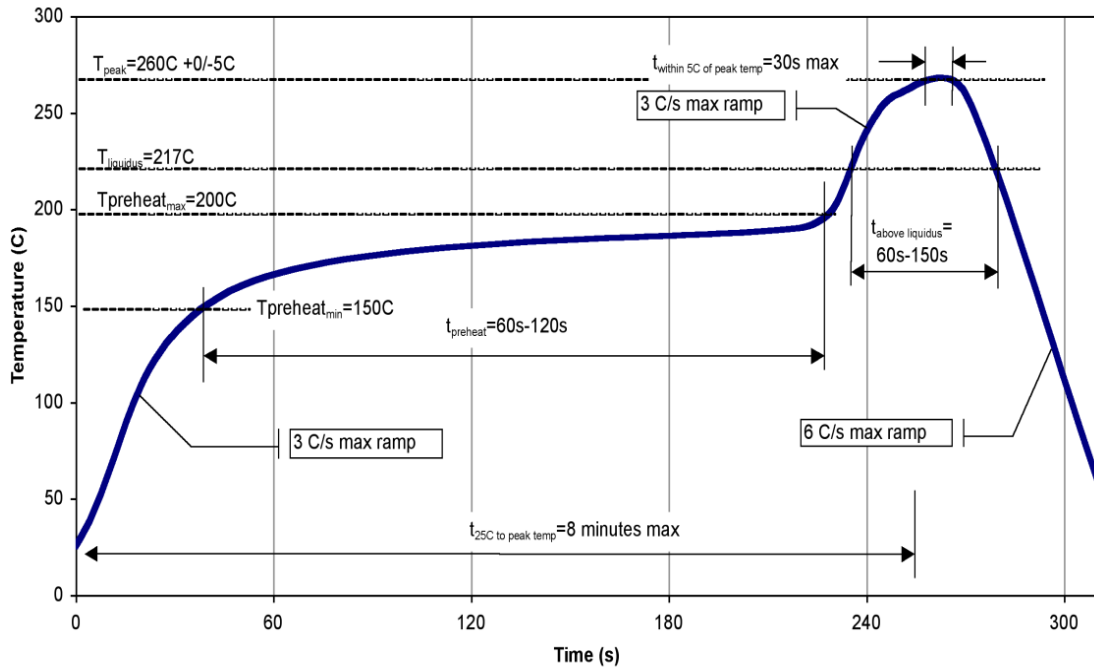
Description	Ref. Des.	Manufacturer	Part Number
Capacitor 1.2pF, 250V, 0603	C1, C9	ATC	600S1R2AT250XT
Capacitor 0.1 uF, 100V, 0603	C2	AVX	0603YC104KAT2A
Capacitor 2.2 pF, 250V, 0603	C3, C7	ATC	600S2R2BT250T
Capacitor 100 pF, 200V, 0603	C5, C6	Capax Technologies	0603G101J201S
Capacitor 1 uF, 200V, 0805	C4, C8	TTI Inc.	C2012X7S2A105M125AB
Capacitor, Electrolytic, 47 uF, 50V	C10	Panasonic	EEETG1H470P
Inductor 5.6 nH, 0603	L1	Coilcraft	0603CS-5N6XJEW
Inductor 8.2 nH, 0603	L2	Coilcraft	0603HP-8N2XJLW
Resistor, 5.6 Ohm, 0603	R1, R2	TTI	CRCW06035R60JNEA
Resistor, 215 Ohm, 0603	R3	Digi-Key	CRCW0603215RFKEA
Resistor, 33.2 Ohm, 0603	R5, R6	TTI	CRCW060333R2FKTA
Resistor, 10 Ohm, 0603	R4	TTI	CRCW060310R0JNTA

2.6 – 4.2 GHz Application Circuit - Layout

Board material is RO4350B 0.020" thickness with 1oz copper cladding. Overall EVB size is 2" x 2.5".



Recommended Solder Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	500 V, 1B	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	1000 V, C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	MSL3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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