THE DATASHEET OF

TX7364ACP

TCAL6416 16-Bit Translating I²C-Bus, SMBus I/O Expander With Interrupt Output, Reset, and Agile I/O Configuration Registers

1 Features

- Operating power-supply voltage range of 1.08V to 3.6V
- Allows bidirectional voltage-level translation and GPIO expansion between 1.2V, 1.8V, 2.5V, and 3.3V I²C bus and p-ports
- Low standby current consumption of 1µA typical at 1.8V
- 1MHz fast mode plus I²C bus
- Hardware address pin allows two devices on the same I²C, SMBus bus
- Active-low reset input ($\overline{\text{RESET}}$)
- Open-drain active-low interrupt output ($\overline{\text{INT}}$)
- Input or output configuration register
- Polarity inversion register
- Configurable I/O drive strength register
- Pull-up and pull-down resistor configuration register
- Internal power-on reset
- Noise filter on SCL or SDA inputs
- Latched outputs with high-current drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22
  - 4000V Human-body model (A114A)
  - 1000V Charged-device model (C101)

2 Applications

- Servers
- Routers (telecom switching equipment)
- Personal computers
- Personal electronics
- Industrial automation
- Gaming consoles
- Products with GPIO-limited processors

3 Description

The TCAL6416 device provides general purpose parallel input/output (I/O) expansion for the two-line bidirectional I²C bus (or SMBus) protocol. The device can operate with a power supply voltage ranging from 1.08V to 3.6V on the I²C bus side (V_{CCI}) and a power supply voltage ranging from 1.08V to 3.6V on the P-port side (V_{CCP}).

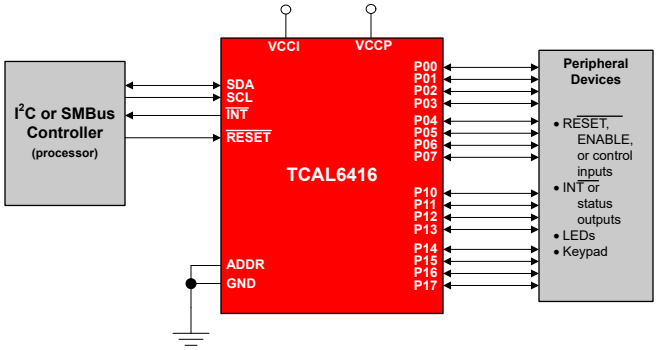
The device supports 100kHz (Standard-mode), 400kHz (Fast-mode), and 1MHz (fast-mode-plus) I²C clock frequencies. I/O expanders such as the TCAL6416 provide a simple solution when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, etc.

The TCAL6416 has Agile I/O ports which include additional features designed to enhance the I/O performance in terms of speed, power consumption and EMI. The additional features are: programmable output drive strength, programmable pull-up and pull-down resistors, latchable inputs, maskable interrupt, interrupt status register, and programmable open-drain or push-pull outputs.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TCAL6416	TSSOP (24)	7.8mm × 6.4mm
	VSSOP (24)	6.1mm x 4.9mm
	WQFN (24)	4mm × 4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

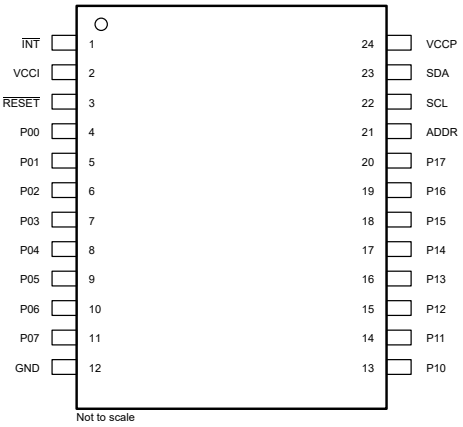


Figure 4-1. PW Package, 24-Pin TSSOP (Top View)

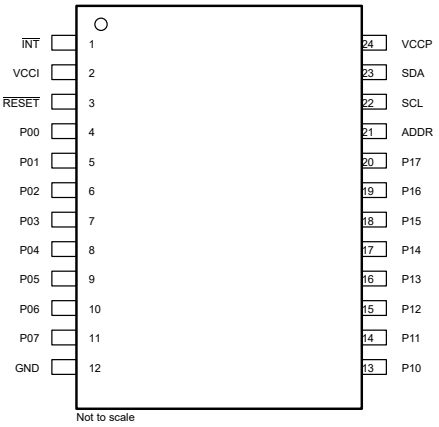
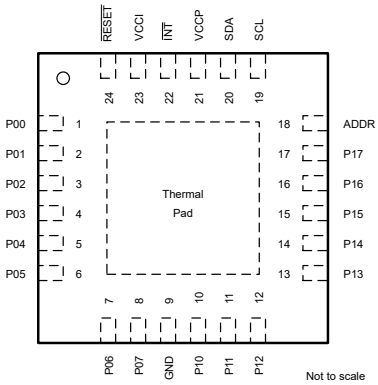


Figure 4-2. DGS Package, 24-Pin VSSOP (Top View)



The exposed center pad must be connected as a secondary ground or left electrically open.

Figure 4-3. RTW Package, 24-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	TSSOP (PW)	VSSOP (DGS)	QFN (RTW)		
$\overline{INT}$	1	1	22	O	Interrupt output. Connect to V_{CCI} or V_{CCP} through a pull-up resistor
VCCI	2	2	23	—	Supply voltage of I^2C bus. Connect directly to the supply voltage of the external I^2C controller
$\overline{RESET}$	3	3	24	I	Active-low reset input. Connect to V_{CCI} through a pull-up resistor, if no active connection is used
P00	4	4	1	I/O	P-port input/output (push-pull design structure). At power on, P00 is configured as an input
P01	5	5	2	I/O	P-port input/output (push-pull design structure). At power on, P01 is configured as an input
P02	6	6	3	I/O	P-port input/output (push-pull design structure). At power on, P02 is configured as an input
P03	7	7	4	I/O	P-port input/output (push-pull design structure). At power on, P03 is configured as an input
P04	8	8	5	I/O	P-port input/output (push-pull design structure). At power on, P04 is configured as an input
P05	9	9	6	I/O	P-port input/output (push-pull design structure). At power on, P05 is configured as an input
P06	10	10	7	I/O	P-port input/output (push-pull design structure). At power on, P06 is configured as an input
P07	11	11	8	I/O	P-port input/output (push-pull design structure). At power on, P07 is configured as an input
GND	12	12	9	—	Ground
P10	13	13	10	I/O	P-port input/output (push-pull design structure). At power on, P10 is configured as an input
P11	14	14	11	I/O	P-port input/output (push-pull design structure). At power on, P11 is configured as an input
P12	15	15	12	I/O	P-port input/output (push-pull design structure). At power on, P12 is configured as an input
P13	16	16	13	I/O	P-port input/output (push-pull design structure). At power on, P13 is configured as an input
P14	17	17	14	I/O	P-port input/output (push-pull design structure). At power on, P14 is configured as an input
P15	18	18	15	I/O	P-port input/output (push-pull design structure). At power on, P15 is configured as an input
P16	19	19	16	I/O	P-port input/output (push-pull design structure). At power on, P16 is configured as an input
P17	20	20	17	I/O	P-port input/output (push-pull design structure). At power on, P17 is configured as an input
ADDR	21	21	18	I	Address input. Connect directly to V_{CCP} or ground
SCL	22	22	19	I	Serial clock bus. Connect to V_{CCI} through a pull-up resistor
SDA	23	23	20	I/O	Serial data bus. Connect to V_{CCI} through a pull-up resistor
VCCP	24	24	21	—	Supply voltage of TCAL6416 for P-ports

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

				MIN	MAX	UNIT
V_{CCI}, V_{CCP}	Supply voltage			–0.5	4	V
V_I	Input voltage(2)			–0.5	4	V
V_O	Output voltage(2)			–0.5	4	V
I_{IK}	Input clamp current		V_I < 0		–20	mA
I_{OK}	Output clamp current		V_O < 0		–20	mA
I_{IOK}	Input-output clamp current	P port	V_O < 0 or V_O > V_{CCP}		±20	mA
		SDA	V_O < 0 or V_O > V_{CCI}		±20	
I_{OL}	Continuous output low current(3)	P port	V_O = 0 to V_{CCP}		50	mA
		SDA	V_O = 0 to V_{CCI}		25	
I_{OH}	Continuous output high current(3)	P port	V_O = 0 to V_{CCP}		–50	mA
I_{CC}	Continuous current through GND				–200	mA
I_{CC}	Continuous current through V_{CCP}				160	mA
	Continuous current through V_{CCI}				10	
T_J	Junction temperature				130	°C
T_{stg}	Storage temperature			–65	150	°C

(1) *Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.*
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Connecting an IO pin directly to GND is not allowed if this pin is set as output, because this will generate >150mA current which could damage the device. We recommend a >10kΩ pull down resistor connected to IO pin if user wants to connect the IO pin to GND.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC specification JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCI}, V_{CCP}	Supply voltage		1.08	3.6	V
V_{IH}	High-level input voltage	SCL, SDA, $\overline{RESET}$	0.7 * V_{CCI}	3.6	V
		P00-P17, ADDR	0.7 * V_{CCP}	3.6	
V_{IL}	Low-level input voltage	SCL, SDA, $\overline{RESET}$	-0.5	0.3 * V_{CCI}	V
		P00-P17, ADDR	-0.5	0.3 * V_{CCP}	V
I_{OH}	High-level output current	P00-P17		–10	mA
I_{OL}	Low-level output current (V_{OL} ≤ 0.3V)	P00-P17		25	mA
T_A	Ambient temperature		–40	125	°C
T_J	Junction temperature			125	°C

5.4 Thermal Information

THERMAL METRIC (1)		Package			UNIT
		DGS (VSSOP)	PW (TSSOP)	RTW (WQFN)	
		PINS	PINS	PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.3	101.4	47.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.6	45.2	41.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.5	56.6	26.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.5	6.9	2.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	47.2	56.2	26.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	NA	15.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCP}	MIN	TYP	MAX	UNIT
V_{IK}	Input diode clamp voltage		I_I = –18mA	1.08V to 3.6V	–1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising		V_I = V_{CC} or GND, I_O = 0			0.85	1.0	V
V_{PORF}	Power-on reset voltage, V_{CC} falling		V_I = V_{CC} or GND, I_O = 0		0.6	0.75		V
V_{OH}	P-port high-level output voltage		I_{OH} = –8mA; CC-XX = 11b	1.08V	0.8			V
				1.65V	1.4			
				2.3V	2.1			
				3V	2.8			
			I_{OH} = –2.5mA & CC-XX = 00b; I_{OH} = –5mA & CC-XX = 01b; I_{OH} = –7.5mA & CC-XX = 10b; I_{OH} = –10mA & CC-XX = 11b;	1.08V	0.75			
				1.65V	1.4			
				2.3V	2.1			
				3V	2.8			
V_{OL}	Low-level output voltage	P ports	I_{OL} = 8mA; CC-XX = 11b	1.08V			0.2	V
				1.65V			0.15	
				2.3V			0.1	
				3.0V			0.1	
		P ports	I_{OL} = 2.5mA and CC-XX = 00b; I_{OL} = 5mA and CC-XX = 01b; I_{OL} = 7.5mA and CC-XX = 10b; I_{OL} = 10mA and CC-XX = 11b;	1.08V			0.25	V
				1.65V			0.15	
				2.3V			0.1	
				3.0V			0.1	
I_{OL}	Low-level output current	SDA	V_{OL} = 0.4V	1.08V to 3.6V	20			mA
		$\overline{INT}$	V_{OL} = 0.4V		4			
I_I	Input leakage current	P ports	V_I = V_{CC} or GND	1.08V to 3.6V			±1	µA
			V_I = 3.6V	0V			±1	
I_I	Input leakage current	SCL, SDA, $\overline{RESET}$	V_I = V_{CC} or GND	1.08V to 3.6V			±1	
I_I	Input leakage current	ADDR	V_I = V_{CC} or GND	1.08V to 3.6V			±1	µA

5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCP}	MIN	TYP	MAX	UNIT
I_{CC} (I_{CCI} + I_{CCP})	Quiescent current	Operating mode (400kHz)	SDA, $\overline{RESET}$ = V_{CCI}, P port, ADDR = V_{CCP} or GND, I/O = inputs, f_{SCL} = 400kHz, –40°C < T_A ≤ 85°C	3.6V		7	15	µA
				2.7V		5	11	
				1.95V		4	8	
				1.32V		2	6	
			SDA, $\overline{RESET}$ = V_{CCI}, P port, ADDR = V_{CCP} or GND, I/O = inputs, f_{SCL} = 400kHz, 85°C < T_A ≤ 125°C	3.6V		7	24	µA
				2.7V		5	18	
				1.95V		4	14	
				1.32V		2	11	
		Operating mode (1MHz)	SDA, $\overline{RESET}$ = V_{CCI}, P port, ADDR = V_{CCP} or GND, I/O = inputs, f_{SCL} = 1MHz, –40°C < T_A ≤ 85°C	3.6V			34	µA
				2.7V			24	
				1.95V			18	
				1.32V			12	
			SDA, $\overline{RESET}$ = V_{CCI}, P port, ADDR = V_{CCP} or GND, I/O = inputs, f_{SCL} = 1MHz, 85°C < T_A ≤ 125°C	3.6V			42	µA
				2.7V			30	
				1.95V			22	
				1.32V			16	
		Standby mode	SCL, SDA, $\overline{RESET}$ = V_{CCI}, P port, ADDR = V_{CCP} or GND, I/O = inputs, I_O = 0, f_{SCL} = 0kHz, –40°C < T_A ≤ 85°C	3.6V		1.5	4	µA
				2.7V		1.2	3	
				1.95V		0.6	3	
				1.32V		0.6	3	
			SCL, SDA, $\overline{RESET}$ = V_{CCI}, P port, ADDR = V_{CCP} or GND, I/O = inputs, I_O = 0, f_{SCL} = 0kHz, 85°C < T_A ≤ 125°C	3.6V			14	µA
				2.7V			10	
				1.95V			8	
				1.32V			6	
$R_{pu(int)}$	internal pull-up resistance	P port			70	100	140	kΩ
$R_{pd(int)}$	internal pull-down resistance							
C_I	Input pin capacitance	SCL	V_I = V_{CC} or GND	1.08V to 3.6V		2.5	5	pF
C_{IO}	Input-output pin capacitance	SDA	V_{IO} = V_{CC} or GND	1.08V to 3.6V		6	8	pF
		P port	V_{IO} = V_{CC} or GND	1.08V to 3.6V		6	8.5	

5.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$\overline{RESET}$				
t_w	Reset pulse duration	80		ns
t_{REC}	Reset recovery time	0		ns
t_{RESET}	Time to reset	400		ns
P-Ports				
t_{PH}	Minimum pulse width on P-Port that causes an interrupt	30		ns

5.7 I²C Bus Timing Requirements

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
I²C Bus - Standard Mode					
f_{scl}	I²C clock frequency		0	100	kHz
t_{sch}	I²C clock high time		4		µs
t_{scl}	I²C clock low time		4.7		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		250		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time			1000	ns
t_{icf}	I²C input fall time			300	ns
t_{ocf}	I²C output fall time	10pF to 400pF bus		300	ns
t_{buf}	I²C bus free time between stop and start		4.7		µs
t_{sts}	I²C start or repeated start condition setup		4.7		µs
t_{sth}	I²C start or repeated start condition hold		4		µs
t_{sps}	I²C stop condition setup		4		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45	µs
C_b	I²C bus capacitive load			400	pF
I²C Bus - Fast Mode					
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		20	300	ns
t_{icf}	I²C input fall time		20 × (V_{CC} / 5.5V)	300	ns
t_{ocf}	I²C output fall time	10pF to 400pF bus	20 × (V_{CC} / 5.5V)	300	ns
t_{buf}	I²C bus free time between stop and start		1.3		µs
t_{sts}	I²C start or repeated start condition setup		0.6		µs
t_{sth}	I²C start or repeated start condition hold		0.6		µs
t_{sps}	I²C stop condition setup		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.9	µs
C_b	I²C bus capacitive load			400	pF
I²C Bus - Fast Mode Plus					
f_{scl}	I²C clock frequency		0	1000	kHz
t_{sch}	I²C clock high time		0.26		µs
t_{scl}	I²C clock low time		0.5		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		50		ns
t_{sdh}	I²C serial-data hold time		0		ns

5.7 I²C Bus Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
t_{icr}	I²C input rise time			120	ns
t_{icf}	I²C input fall time		20 × (V_{CC} / 5.5V)	120	ns
t_{ocf}	I²C output fall time	10pF to 550pF bus	20 × (V_{CC} / 5.5V)	120	ns
t_{buf}	I²C bus free time between stop and start		0.5		µs
t_{sts}	I²C start or repeated start condition setup		0.26		µs
t_{sth}	I²C start or repeated start condition hold		0.26		µs
t_{sps}	I²C stop condition setup		0.26		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		0.45	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.45	µs
C_b	I²C bus capacitive load			550	pF

5.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{INT}$			1	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$			1	µs
t_{pv}	Output data valid time	SCL	P port			400	ns
t_{ps}	Input data setup time	P port	SCL	0			ns
t_{ph}	Input data hold time	P port	SCL	300			ns

5.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

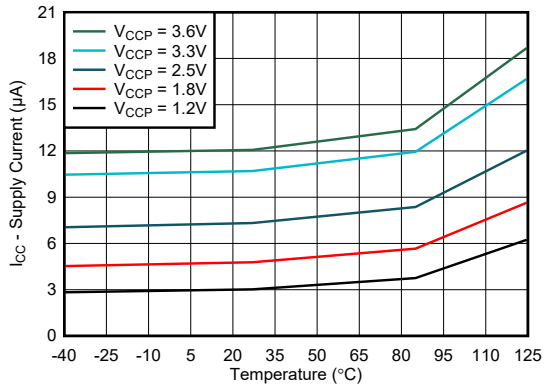


Figure 5-1. Supply Current vs Temperature - FM mode

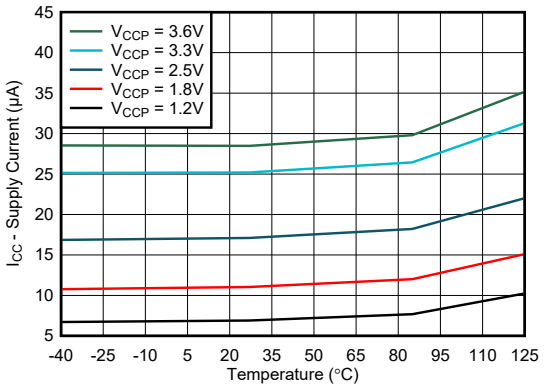


Figure 5-2. Supply Current vs Temperature - FM+ mode

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

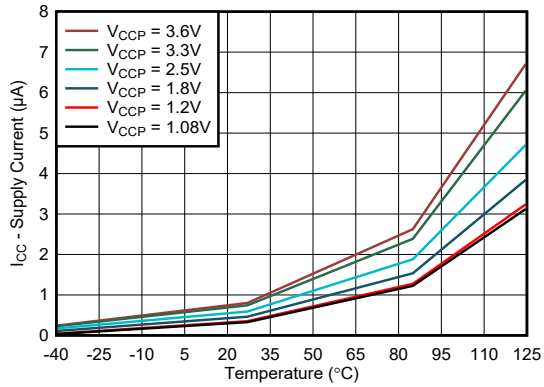


Figure 5-3. Standby Supply Current vs Temperature

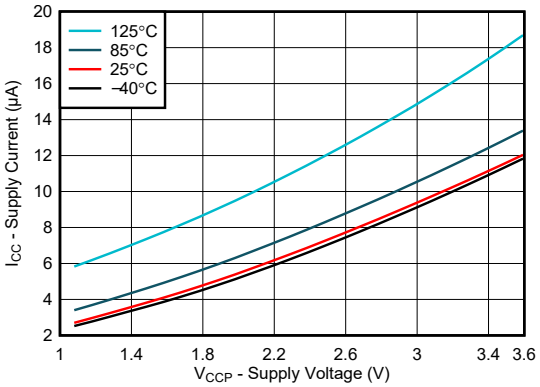


Figure 5-4. Supply Current vs Supply Voltage - FM mode

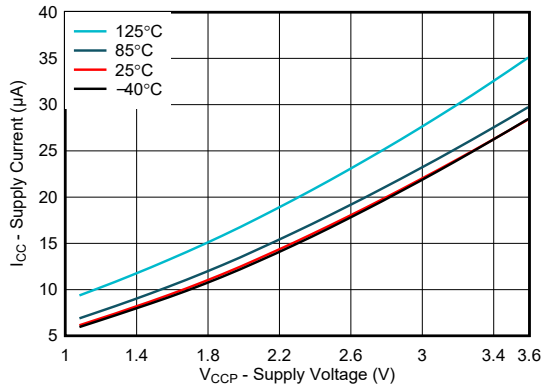


Figure 5-5. Supply Current vs Supply Voltage - FM+ mode

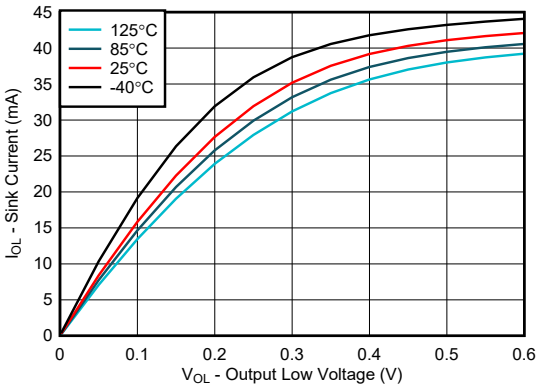


Figure 5-6. I/O Sink Current vs Output Low Voltage, V_{CCP} = 1.08V

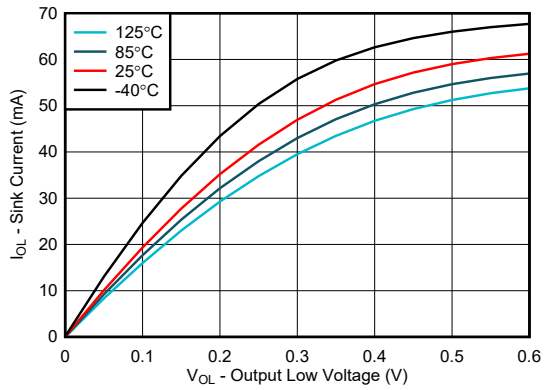


Figure 5-7. I/O Sink Current vs Output Low Voltage, V_{CCP} = 1.2V

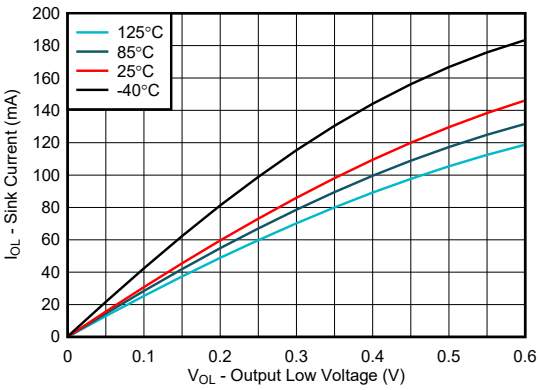


Figure 5-8. I/O Sink Current vs Output Low Voltage, V_{CCP} = 1.8V

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

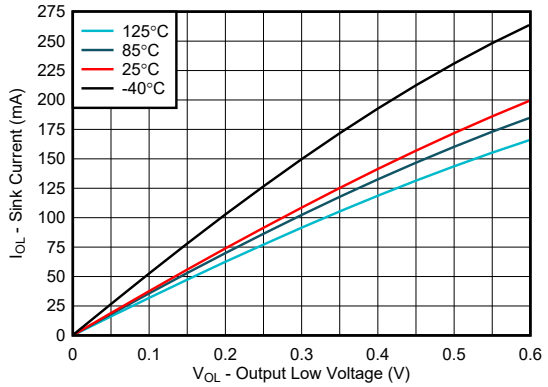


Figure 5-9. I/O Sink Current vs Output Low Voltage, V_{CCP} = 2.5V

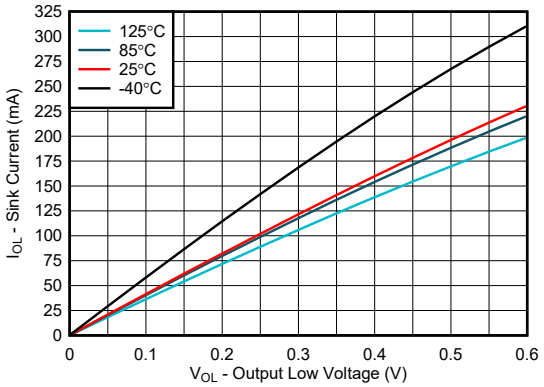


Figure 5-10. I/O Sink Current vs Output Low Voltage, V_{CCP} = 3.3V

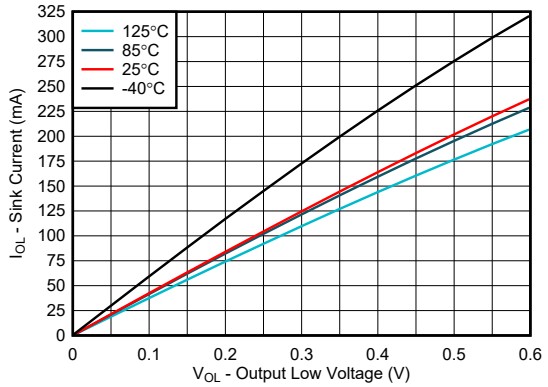


Figure 5-11. I/O Sink Current vs Output Low Voltage, V_{CCP} = 3.6V

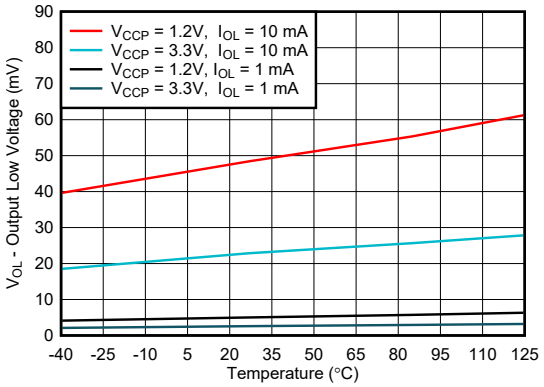


Figure 5-12. I/O Low Voltage vs Temperature

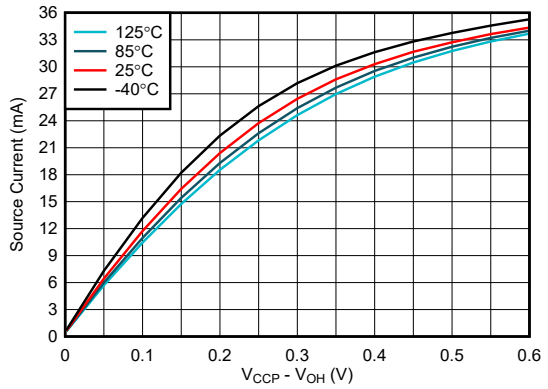


Figure 5-13. I/O Source Current vs Output High Voltage , V_{CCP} = 1.08V

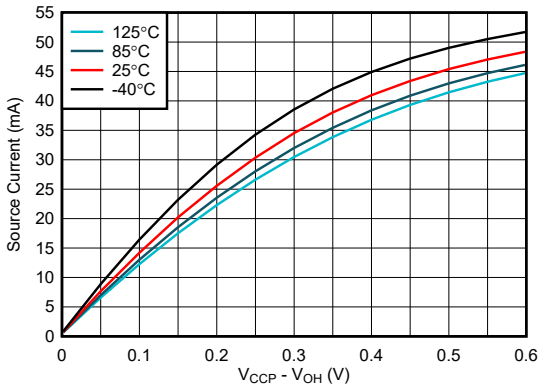


Figure 5-14. I/O Source Current vs Output High Voltage, V_{CCP} = 1.2V

5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

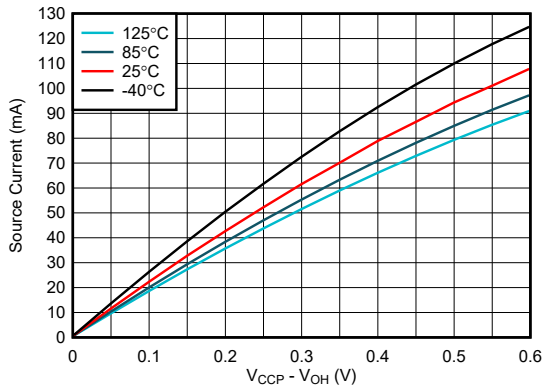


Figure 5-15. I/O Source Current vs Output High Voltage, V_{CCP} = 1.8V

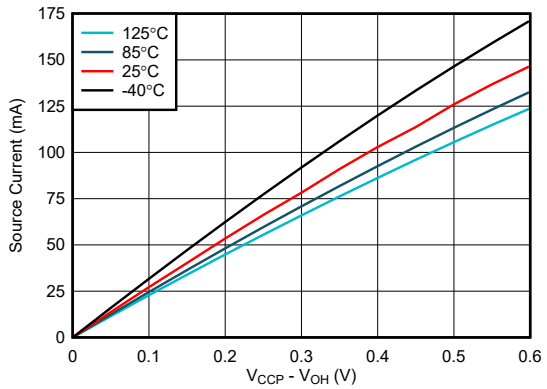


Figure 5-16. I/O Source Current vs Output High Voltage, V_{CCP} = 2.5V

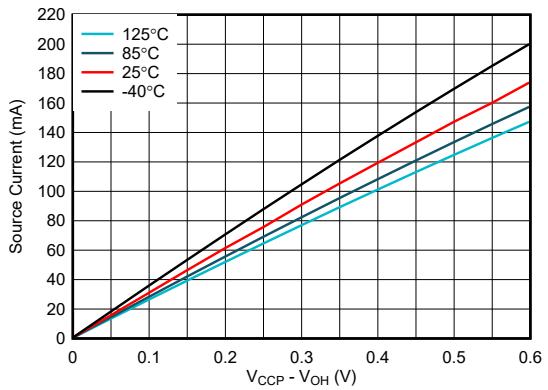


Figure 5-17. I/O Source Current vs Output High Voltage, V_{CCP} = 3.3V

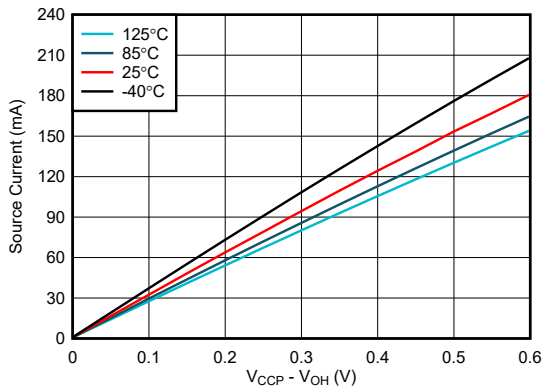


Figure 5-18. I/O Source Current vs Output High Voltage, V_{CCP} = 3.6V

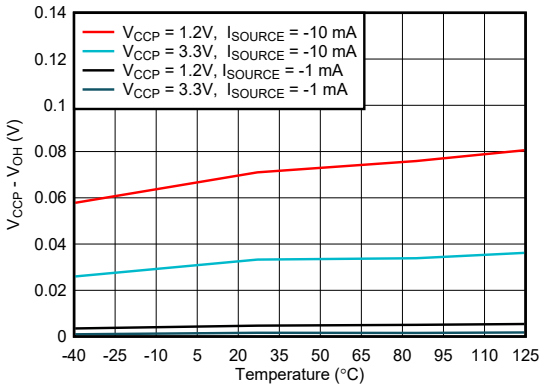
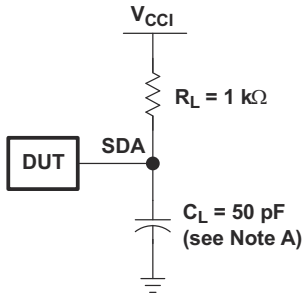
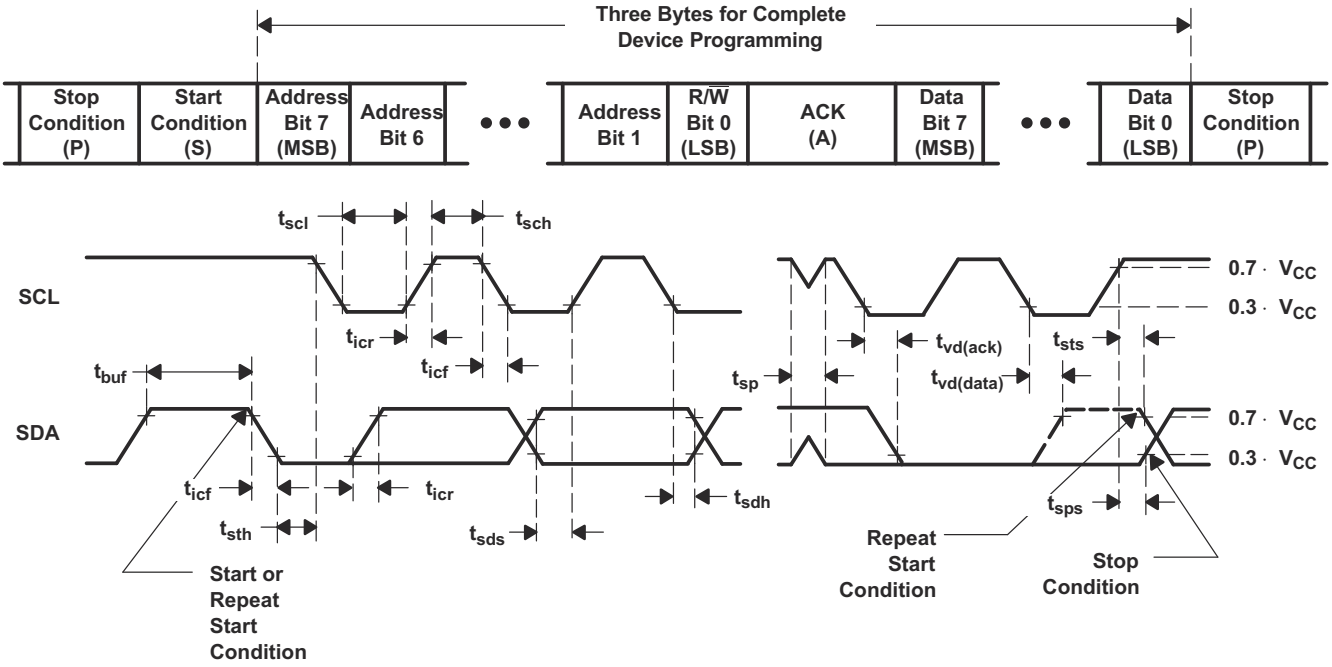


Figure 5-19. I/O High Voltage vs Temperature

6 Parameter Measurement Information



SDA LOAD CONFIGURATION

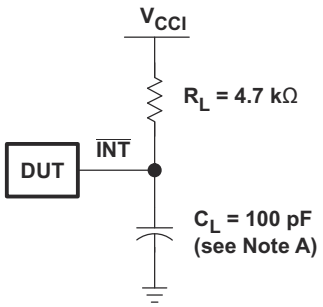


VOLTAGE WAVEFORMS

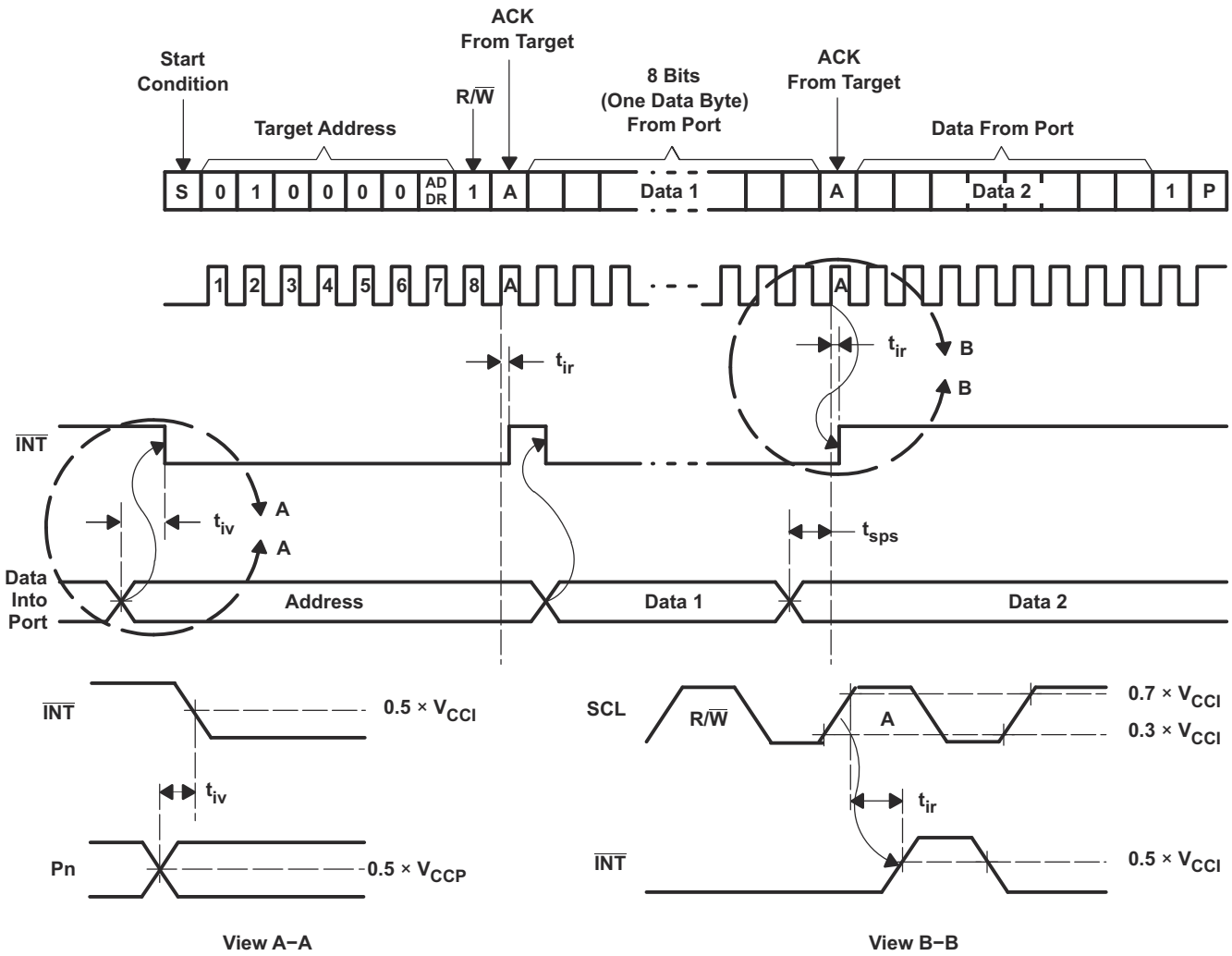
BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

A. C_L includes probe and jig capacitance. tocf is measured with C_L of 10pF or 400pF.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r/t_f ≤ 30ns.
C. All parameters and waveforms are not applicable to all devices.

Figure 6-1. I^2C Interface Load Circuit and Voltage Waveforms



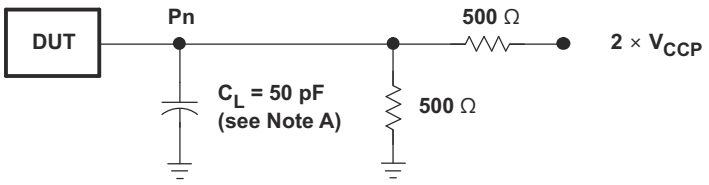
INTERRUPT LOAD CONFIGURATION



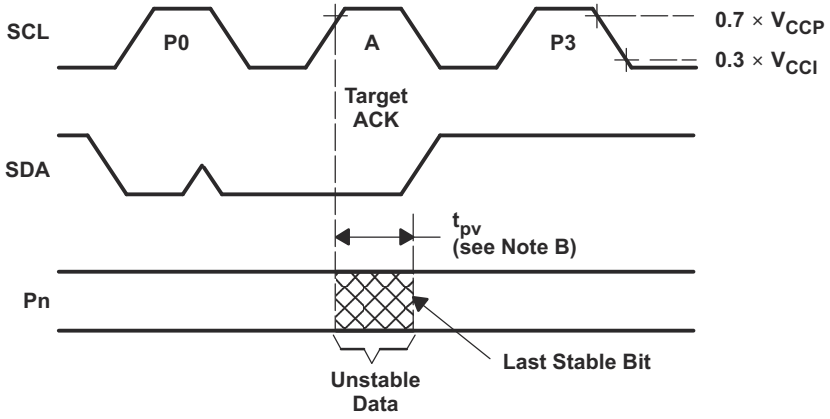
View A–A View B–B

A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r/t_f ≤ 30ns.
C. All parameters and waveforms are not applicable to all devices.

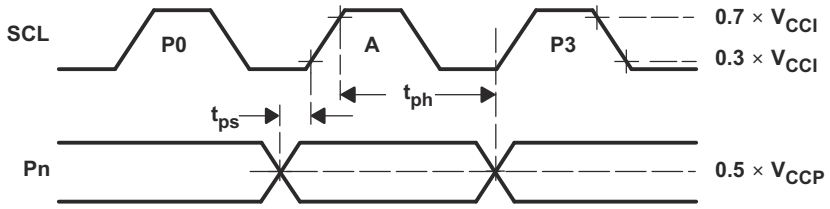
Figure 6-2. Interrupt Load Circuit and Voltage Waveforms



P-PORT LOAD CONFIGURATION



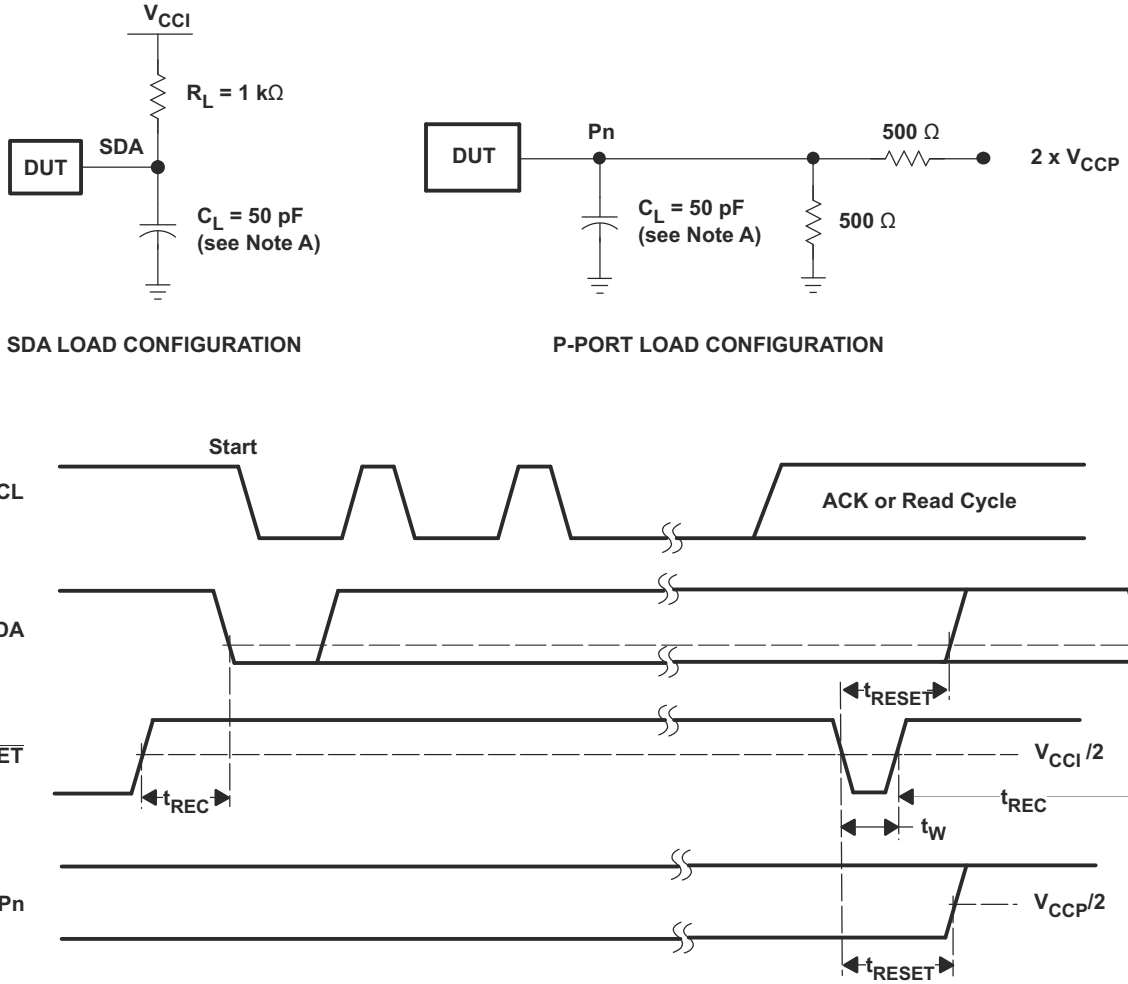
WRITE MODE (R/$\overline{W}$ = 0)



READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r/t_f ≤ 30ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 6-3. P-Port Load Circuit and Timing Waveforms



A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r/t_f ≤ 30ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. I/Os are configured as inputs.
E. All parameters and waveforms are not applicable to all devices.

Figure 6-4. Reset Load Circuits and Voltage Waveforms

7 Detailed Description

7.1 Overview

The TCAL6416 supports voltage translation over a wide supply voltage range. This allows the device to interface with modern processors on the I^2C side, where supply levels are lower to conserve power. In contrast to the dropping power supplies of processors, some PCB components (such as LEDs) still require a higher voltage power supply.

The V_{CCI} pin is the power supply for the I^2C bus, and therefore the pull-up resistors connected to the SCL, SDA, and RESET pins should be terminated at V_{CCI}. The INT output has an open-drain structure and requires an external pull-up resistor to V_{CCP} or V_{CCI} depending on the application. The V_{CCP} pin is the power supply for the P-ports. If the external pull-up resistors are used on any P-port, or if the LEDs are driven by any P-port, then the one or more of the resistors or LEDs connected to P00-P07 and P10-P17 should be terminated at V_{CCP}. The device P-ports configured as outputs have the ability to sink up to 25mA for directly driving LEDs, but the current must be limited externally with an additional resistance.

The TCAL6416 digital core consists of 8-bit data registers, which allow the user to configure the I/O port characteristics. At power-up or after a software reset call, the I/Os are configured as inputs. However, the system controller can configure the I/Os as either inputs or outputs by writing to the Configuration registers. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. The system controller can read all registers. Additionally, the TCAL6416 has Agile I/O functionality, which is specifically targeted to enhance the I/O ports. The Agile I/O features and registers include programmable output drive strength, programmable pull-up and pull-down resistors, latchable inputs, maskable interrupts, interrupt status register, and programmable open-drain or push-pull outputs. These configuration registers improve the I/O by increasing flexibility and allowing the user to optimize their design for power consumption, speed, and EMI.

Other features of the device include an interrupt that is generated on the $\overline{INT}$ pin whenever an input port changes state. The device can be reset to its default state by issuing a software reset command or by cycling power to the device and causing a power-on reset. The ADDR hardware selectable address pin allows two TCAL6416 devices to be connected to the same I^2C bus.

The TCAL6416 open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system controller that an input state has changed. The $\overline{INT}$ pin can be connected to the interrupt input of a processor. By sending an interrupt signal on this line, the device can inform the processor if there is incoming data on the remote I/O ports without having to communicate through the I^2C bus. Thus, the device can remain a simple target device.

The system controller can re-initialize I^2C/SMBus state machine in the event of a timeout or other improper operation by asserting a low on the $\overline{RESET}$ input pin without resetting the sticky registers to default values.

One hardware pin (ADDR) can be used to program and vary the fixed I^2C address, and allow two devices to share the same I^2C bus or SMBus.

7.2 Functional Block Diagrams

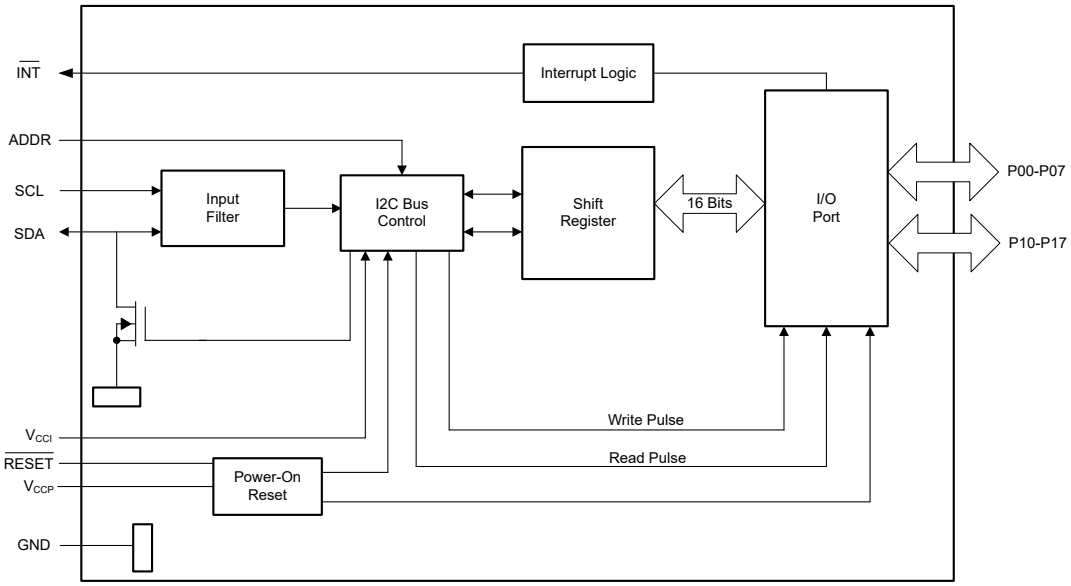
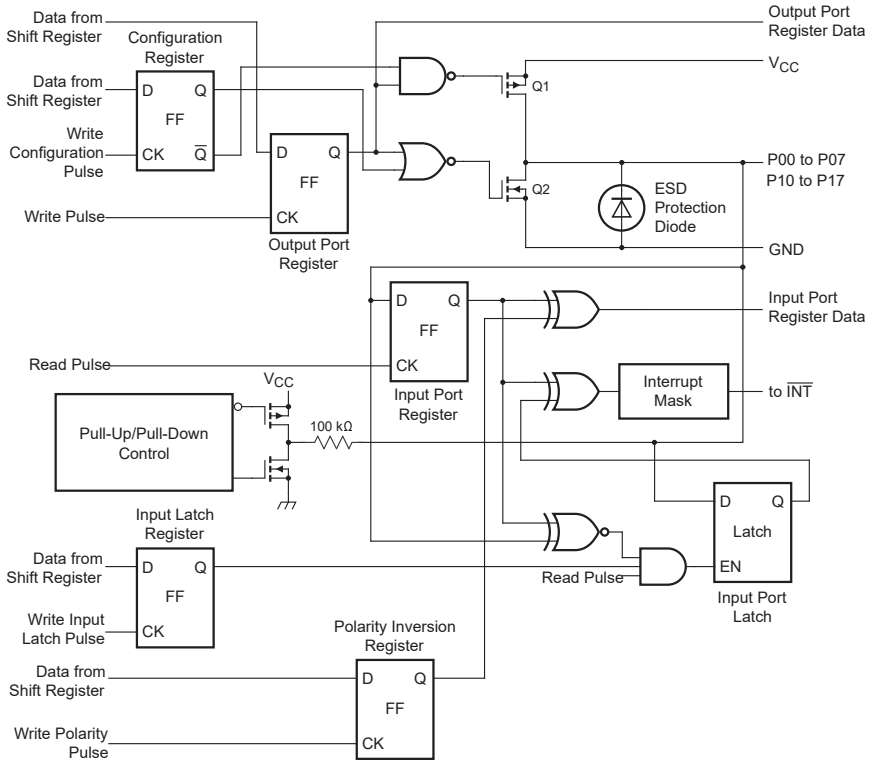


Figure 7-1. Logic Diagram (Positive Logic)



A. On power up or reset, all registers return to default values.

Figure 7-2. Simplified Schematic of P00 to P17

7.3 Feature Description

7.3.1 Voltage Translation

Table 7-1 lists all of the optional voltage supply level combinations for the I^2C bus (V_{CCI}) and the P-ports (V_{CCP}) supported by the TCAL6416.

Table 7-1. Voltage Translation

V_{CCI} (SDA AND SCL OF I^2C Controller) (V)	V_{CCP} (P-PORTS) (V)
1.2	1.2
1.2	1.8
1.2	2.5
1.2	3.3
1.8	1.2
1.8	1.8
1.8	2.5
1.8	3.3
2.5	1.2
2.5	1.8
2.5	2.5
2.5	3.3
3.3	1.2
3.3	1.8
3.3	2.5
3.3	3.3

7.3.2 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off (see Section 7.2), which creates a high-impedance input. The input voltage may be raised above the supply voltage to a maximum of 3.6V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either supply or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

7.3.3 Adjustable Output Drive Strength

The output drive strength registers allow the user to control the drive level of the GPIO. Each GPIO can be configured independently to one of the four possible current levels. By programming these bits the user is changing the number of transistor pairs or 'fingers' that drive the I/O pad. Figure 7-3 shows a simplified output stage. The behavior of the pad is affected by the Configuration register, the output port data, and the output drive strength register. When the output drive strength register bits are programmed to 01b, then only two of the fingers are active, reducing the current drive capability by 50%.

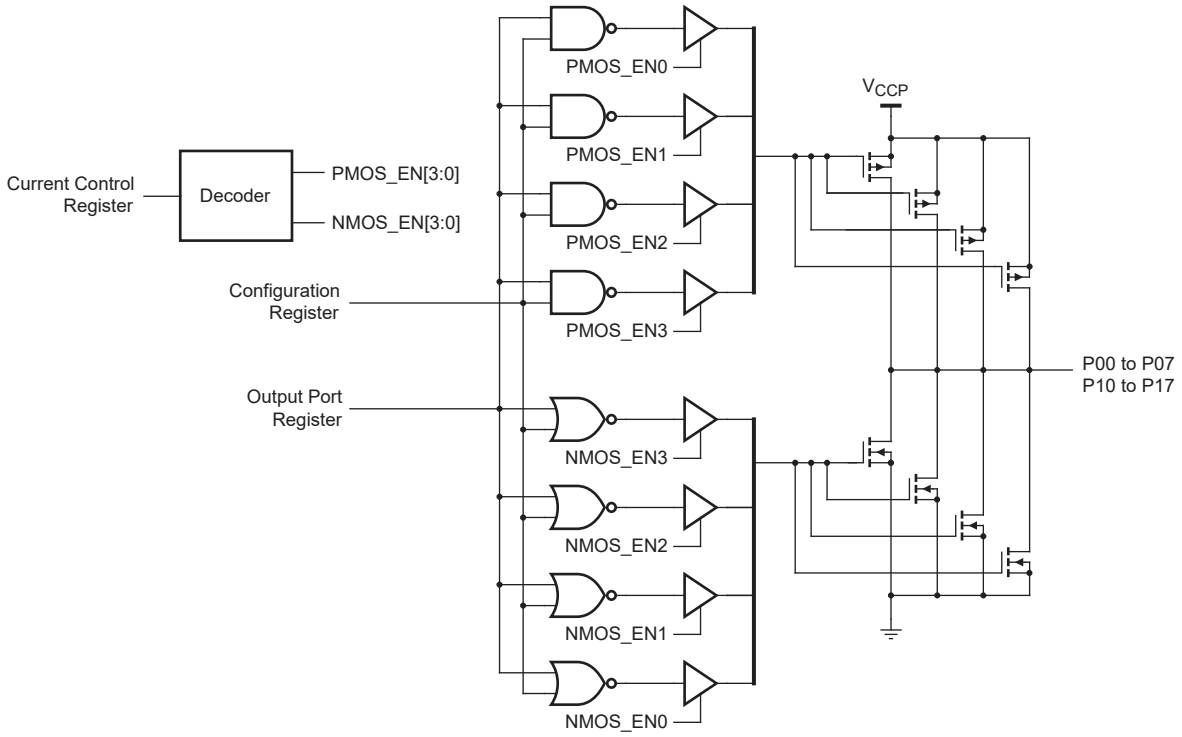


Figure 7-3. Simplified Output Stage

A function of the output drive selection causes a peak current to occur when the output switches. Reducing the current drive capability may reduce the system noise that occurs. This peak current runs through the supply and GND package inductance and creates a noise (some radiated, but more critically Simultaneous Switching Noise (SSN)). In other words, switching many outputs at the same time will create ground and supply noise. The output drive strength control through the Output Drive Strength registers allows the user to mitigate SSN issues without the need of additional external components.

7.3.4 Interrupt Output ($\overline{INT}$)

Any rising or falling edge of the port inputs in the input mode generates an interrupt, provided the interrupt feature is unmasked. After time t_{iv}, the $\overline{INT}$ signal is valid. Resetting the interrupt circuit is achieved when data on the port is changed back to the original setting or when data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the input port register.

The $\overline{INT}$ output has an open-drain structure and requires an external pull-up resistor to V_{CCP} or V_{CCI} depending on the application. The pull-up resistor for $\overline{INT}$ should be connected to the voltage source of the device that requires the interrupt information.

7.3.5 Reset Input ($\overline{RESET}$)

The $\overline{RESET}$ input can be asserted to initialize the system while keeping the V_{CCP} supply at its operating level. A reset can be accomplished by holding the $\overline{RESET}$ pin low for a minimum of t_W. The TCAL6416 registers and I^2C/SMBus state machine are changed to their default state once $\overline{RESET}$ is low (0). When $\overline{RESET}$ is high (1), the I/O levels at the P port can be changed externally or through the controller. This input requires a pull-up resistor to V_{CCI}, if no active connection is used. When $\overline{RESET}$ is toggled the input port register is updated to reflect the state of the GPIO pins.

7.3.6 Software Reset Call

The software reset call is a command sent from the controller on the I^2C bus that instructs all devices that support the command to be reset to the power-up default state. To function as expected, the I^2C bus must be functional, and no devices can be hanging the bus.

The software reset call is defined as the following steps:

1. The I^2C bus controller sends a start condition.
2. The address used is the reserved general call I^2C bus address '0000 0000' with the R/W bit set to 0. The byte sent is 0x00.
3. Any devices supporting the general call functionality will ACK. If the R/W bit is set to 1 (read), then the device will NACK.
4. When the general call address is acknowledged, the controller sends only 1 byte of data equal to 0x06. If the data byte is any other value, then the device does not acknowledge or reset. If more than 1 byte is sent, then no more bytes is acknowledged, and the device ignores the I^2C message considering as invalid.
5. After the 1 byte of data (0x06) is sent, the controller sends a STOP condition to end the Software Reset sequence. The device ignores a repeated START condition and no reset is performed.

When the previous steps are completed successfully, the device performs a reset. This clears all register values back to power-on defaults.

7.4 Device Functional Modes

7.4.1 Power-On Reset

When power (from 0V) is applied to V_{CCP}, an internal power-on reset holds the TCAL6416 in a reset condition until the supply has reached V_{POR}. At that time, the reset condition is released, and the TCAL6416 registers and I^2C/SMBus state machine initializes to their default states. After that, V_{CCP} must be lowered to below V_{PORF} and back up to the operating voltage for a power-reset cycle.

7.5 Programming

7.5.1 I^2C Interface

The bidirectional I^2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer can only be initiated when the bus is not busy.

A controller initiates I^2C communication with this device by sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high (see Figure 7-4). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/ $\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address input of the target device must not be changed between the Start and the Stop conditions.

On the I^2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 7-5).

The controller sends a Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high (see Figure 7-4).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 7-6). When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met for proper operation.

A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target. The controller receiver does this by holding the SDA line high. In this event, the transmitter must release the data line to enable the controller to generate a Stop condition.

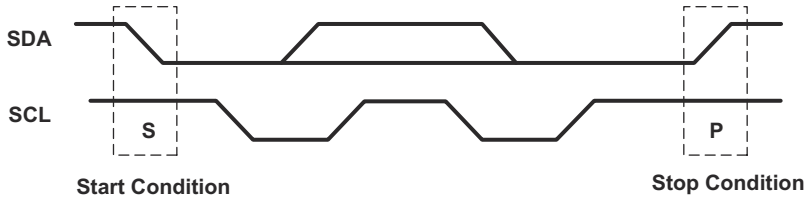


Figure 7-4. Definition of Start and Stop Conditions

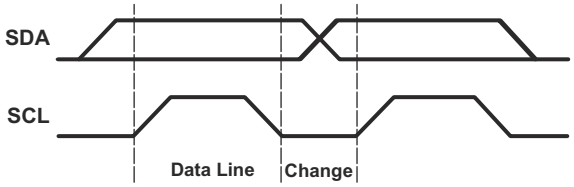


Figure 7-5. Bit Transfer

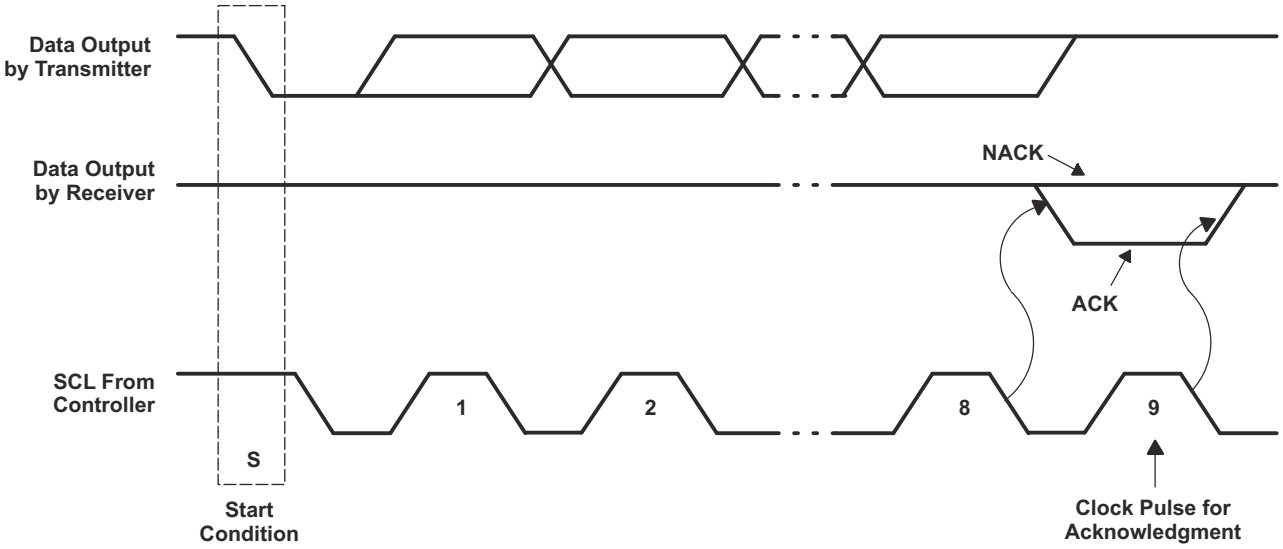


Figure 7-6. Acknowledgment on the I^2C Bus

Table 7-2. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Device I^2C address	L	H	L	L	L	L	ADDR	R/ $\overline{W}$
I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
	P17	P16	P15	P14	P13	P12	P11	P10

7.6 Register Maps

7.6.1 Device Address

Figure 7-7 shows the address of the TCAL6416.

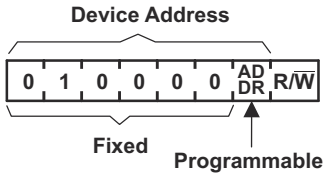


Figure 7-7. TCAL6416 Address

Table 7-3. Address Reference

ADDR	I^2C BUS TARGET ADDRESS
L	32 (decimal), 20 (hexadecimal)
H	33 (decimal), 21 (hexadecimal)

The last bit of the target address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

7.6.2 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus controller sends a command byte, which is stored in the control register in the TCAL6416. The lower bits of this data byte reflect the internal registers (input, output, polarity inversion, or configuration) that are affected. Bit 6 in conjunction with the lower four bits of the Command byte are used to point to the extended features of the device (Agile IO). The command byte is sent only during a write transmission.

Once a new command has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent. Upon power-up, hardware reset, or software reset, the control register defaults to 00h.

B7	B6	B5	B4	B3	B2	B1	B0

Figure 7-8. Control Register Bits

Table 7-4. Command Byte

CONTROL REGISTER BITS								COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00	Input Port 0	Read byte	xxxx xxxx
0	0	0	0	0	0	0	1	01	Input Port 1	Read byte	xxxx xxxx
0	0	0	0	0	0	1	0	02	Output Port 0	Read/write byte	1111 1111
0	0	0	0	0	0	1	1	03	Output Port 1	Read/write byte	1111 1111
0	0	0	0	0	1	0	0	04	Polarity Inversion 0	Read/write byte	0000 0000
0	0	0	0	0	1	0	1	05	Polarity Inversion 1	Read/write byte	0000 0000
0	0	0	0	0	1	1	0	06	Configuration 0	Read/write byte	1111 1111
0	0	0	0	0	1	1	1	07	Configuration 1	Read/write byte	1111 1111
0	1	0	0	0	0	0	0	40	Output Drive Strength 0	Read/write byte	1111 1111
0	1	0	0	0	0	0	1	41	Output Drive Strength 0	Read/write byte	1111 1111
0	1	0	0	0	0	1	0	42	Output Drive Strength 1	Read/write byte	1111 1111
0	1	0	0	0	0	1	1	43	Output Drive Strength 1	Read/write byte	1111 1111
0	1	0	0	0	1	0	0	44	Input latch register 0	Read/write byte	0000 0000
0	1	0	0	0	1	0	1	45	Input latch register 1	Read/write byte	0000 0000
0	1	0	0	0	1	1	0	46	Pull-up/pull-down enable register 0	Read/write byte	0000 0000
0	1	0	0	0	1	1	1	47	pull-up/pull-down enable register 1	Read/write byte	0000 0000
0	1	0	0	1	0	0	0	48	pull-up/pull-down selection register 0	Read/write byte	1111 1111
0	1	0	0	1	0	0	1	49	pull-up/pull-down selection register 1	Read/write byte	1111 1111
0	1	0	0	1	0	1	0	4A	Interrupt mask register 0	Read/write byte	1111 1111
0	1	0	0	1	0	1	1	4B	Interrupt mask register 1	Read/write byte	1111 1111
0	1	0	0	1	1	0	0	4C	Interrupt status register 0	Read byte	0000 0000
0	1	0	0	1	1	0	1	4D	Interrupt status register 1	Read byte	0000 0000
0	1	0	0	1	1	1	1	4F	Output port configuration register	Read/write byte	0000 0000

7.6.3 Register Descriptions

The input port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether Configuration register defines the pin as an input or output. The input port registers are read only. Writes to

these registers have no effect. The externally applied logic level determines the default value (X). Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port register is accessed next.

Table 7-5. Registers 0 and 1 (Input Port Registers) (1)

BIT	I-07	I-06	I-05	I-04	I-03	I-02	I-01	I-00
DEFAULT	X	X	X	X	X	X	X	X
BIT	I-17	I-16	I-15	I-14	I-13	I-12	I-11	I-10
DEFAULT	X	X	X	X	X	X	X	X

The output port registers (registers 2 and 3) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 7-6. Registers 2 and 3 (Output Port Registers)

BIT	O-07	O-06	O-05	O-04	O-03	O-02	O-01	O-00
DEFAULT	1	1	1	1	1	1	1	1
BIT	O-17	O-16	O-15	O-14	O-13	O-12	O-11	O-10
DEFAULT	1	1	1	1	1	1	1	1

The polarity inversion registers (register 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with 1), then the corresponding port pin polarity is inverted. If a bit in these registers is cleared (written with a 0), then the corresponding port pin's original polarity is retained.

Table 7-7. Registers 4 and 5 (Polarity Inversion Registers)

BIT	P-07	P-06	P-05	P-04	P-03	P-02	P-01	P-00
DEFAULT	0	0	0	0	0	0	0	0
BIT	P-17	P-16	P-15	P-14	P-13	P-12	P-11	P-10
DEFAULT	0	0	0	0	0	0	0	0

The configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, then the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in these registers is cleared to 0, then the corresponding port pin is enabled as an output. Changing a port from an input to an output configuration will cause any interrupt associated with that port to be cleared.

Table 7-8. Registers 6 and 7 (Configuration Registers)

BIT	C-07	C-06	C-05	C-04	C-03	C-02	C-01	C-00
DEFAULT	1	1	1	1	1	1	1	1
BIT	C-17	C-16	C-15	C-14	C-13	C-12	C-11	C-10
DEFAULT	1	1	1	1	1	1	1	1

The output drive strength registers control the output drive level of the P port GPIO buffers. Each GPIO can be configured independently to the desired output current level by two register control bits. For example, register 0x41h (bits 7 and 6) controls Port P07, register 0x41h (bits 5 and 4) controls port P06, and so forth. The output drive level of the GPIO is programmed 00b = 0.25x drive strength, 01b = 0.5x drive strength, 10b = 0.75x drive strength, or 11b = 1x for full drive strength capability. For more details, see \.

Table 7-9. Registers 0x40h, 0x41h, 0x42h, and 0x43h (Output Drive Strength Registers)

BIT	CC-03	CC-03	CC-02	CC-02	CC-01	CC-01	CC-00	CC-00
DEFAULT	1	1	1	1	1	1	1	1

Table 7-9. Registers 0x40h, 0x41h, 0x42h, and 0x43h (Output Drive Strength Registers) (continued)

BIT	CC-03	CC-03	CC-02	CC-02	CC-01	CC-01	CC-00	CC-00
BIT	CC-07	CC-07	CC-06	CC-06	CC-05	CC-05	CC-04	CC-04
DEFAULT	1	1	1	1	1	1	1	1
BIT	CC-13	CC-13	CC-12	CC-12	CC-11	CC-11	CC-10	CC-10
DEFAULT	1	1	1	1	1	1	1	1
BIT	CC-17	CC-17	CC-16	CC-16	CC-15	CC-15	CC-14	CC-14
DEFAULT	1	1	1	1	1	1	1	1

The input latch registers enable and disable the input latch feature of the P port GPIO pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is set to 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0 and 1). A read of the input port register clears the interrupt. However, if the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt.

For example, if the P04 input was at a logic 0 state and then transitions to a logic 1 state followed by returning to the logic 0 state, then the input port 0 register captures this change and an interrupt is generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is cleared, assuming there were no additional inputs that have changed, and bit 4 of the input port 0 register reads '1'. The next read of the input port register bit 4 should now read '0'.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. If the input latch register changes from a latched to a non-latched configuration, the interrupt is cleared if the input logic value returns to its original state.

If the input pin is changed from a latched to a non-latched input, then a read from the input port register reflects the current port logic level. If the input pin is changed from a non-latched to a latched input, then the read from the input register reflects the latched logic level.

Table 7-10. Registers 0x44h and 0x45h (Input Latch Registers)

BIT	L-07	L-06	L-05	L-04	L-03	L-02	L-01	L-00
DEFAULT	0	0	0	0	0	0	0	0
BIT	L-17	L-16	L-15	L-14	L-13	L-12	L-11	L-10
DEFAULT	0	0	0	0	0	0	0	0

The pull-up/pull-down enable registers allow the user to enable or disable pull-up/pull-down resistors on the GPIO pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the GPIO pins. The resistors are disabled when the GPIO pins are configured as outputs. Use the pull-up/pull-down selection registers to select either a pull-up or pull-down resistor.

Table 7-11. Registers 0x46h and 0x47h (Pull-Up/Pull-Down Enable Registers)

BIT	PE-07	PE-06	PE-05	PE-04	PE-03	PE-02	PE-01	PE-00
DEFAULT	0	0	0	0	0	0	0	0
BIT	PE-17	PE-16	PE-15	PE-14	PE-13	PE-12	PE-11	PE-10

Table 7-11. Registers 0x46h and 0x47h (Pull-Up/Pull-Down Enable Registers) (continued)

BIT	PE-07	PE-06	PE-05	PE-04	PE-03	PE-02	PE-01	PE-00
DEFAULT	0	0	0	0	0	0	0	0

The pull-up/pull-down selection registers allow the user to configure each GPIO to have a pull-up or pull-down resistor by programming the respective register bit. Setting a bit to a logic 1 selects a 10kΩ pull-up resistor for that GPIO pin. Setting a bit to logic 0 selects a 10kΩ pull-down resistor for that GPIO pin. If the pull-up/pull-down feature is disabled through registers 0x46h and 0x47h, then writing to these registers will have no effect on the GPIO pin.

Table 7-12. Registers 0x48h and 0x49h (Pull-Up/Pull-Down Selection Registers)

BIT	PUD-07	PUD-06	PUD-05	PUD-04	PUD-03	PUD-02	PUD-01	PUD-00
DEFAULT	1	1	1	1	1	1	1	1
BIT	PUD-17	PUD-16	PUD-15	PUD-14	PUD-13	PUD-12	PUD-11	PUD-10
DEFAULT	1	1	1	1	1	1	1	1

The interrupt mask registers are defaulted to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0.

If an input changes state and the corresponding bit in the interrupt mask register is set to 1, the interrupt is masked and the interrupt pin is not asserted. If the corresponding bit in the interrupt mask register is set to 0, the interrupt pin is asserted.

When an input changes state and the resulting interrupt is masked, setting the interrupt mask register bit to 0 causes the interrupt pin to be asserted. If the interrupt mask bit of an input that is already currently the source of an interrupt is set to 1, the interrupt pin is de-asserted.

Table 7-13. Registers 0x4Ah and 0x4Bh (Interrupt Mask Registers)

BIT	M-07	M-06	M-05	M-04	M-03	M-02	M-01	M-00
DEFAULT	1	1	1	1	1	1	1	1
BIT	M-17	M-16	M-15	M-14	M-13	M-12	M-11	M-10
DEFAULT	1	1	1	1	1	1	1	1

The interrupt status registers are read only registers used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt. When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return to logic 0.

Table 7-14. Registers 0x4Ch and 0x4Dh (Interrupt Status Registers)

BIT	S-07	S-06	S-05	S-04	S-03	S-02	S-01	S-00
DEFAULT	0	0	0	0	0	0	0	0
BIT	S-17	S-16	S-15	S-14	S-13	S-12	S-11	S-10
DEFAULT	0	0	0	0	0	0	0	0

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull (Q1 and Q2 are active. A logic 1 configures the I/O as open-drain (Q1 is disabled, Q2 is active) and the recommended command sequence is to program this register (0x4Fh) before the Configuration register (06 and 07) sets the port pins as outputs.

ODEN0 configures Port 0X and ODEN1 configures Port 1X.

Table 7-15. Register 0x4Fh (Output Port Configuration Register)

BIT	Reserved						ODEN-1	ODEN-0
DEFAULT	0	0	0	0	0	0	0	0

7.6.4 Bus Transactions

Data is exchanged between the controller and TCAL6416 through write and read commands.

7.6.4.1 Writes

Data is transmitted to the TCAL6416 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see Figure 7-7 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

Twenty-two registers within the TCAL6416 are configured to operate as eleven register pairs. The eleven pairs are input port, output port, polarity inversion, configuration, output drive strength (two 16-bit registers), input latch, pull-up/pull-down enable, pull-up/pulldown selection, interrupt mask, and interrupt status registers. After sending data to one register, the next data byte is sent to the other register in the pair (see Figure 7-9 and Figure 7-10). For example, if the first byte is sent to Output Port 1 (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register pair may be updated independently of the other registers.

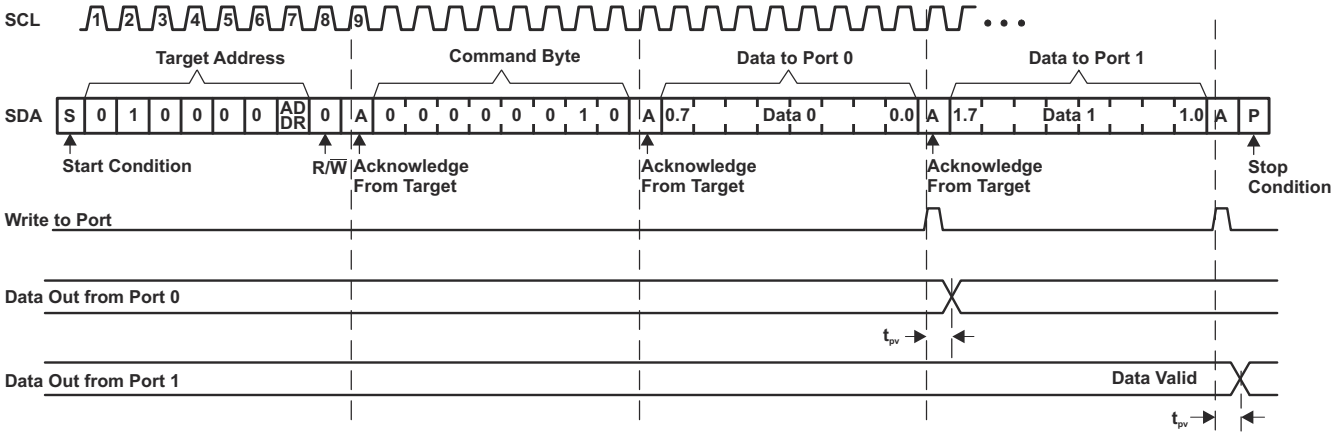


Figure 7-9. Write to Output Port Registers

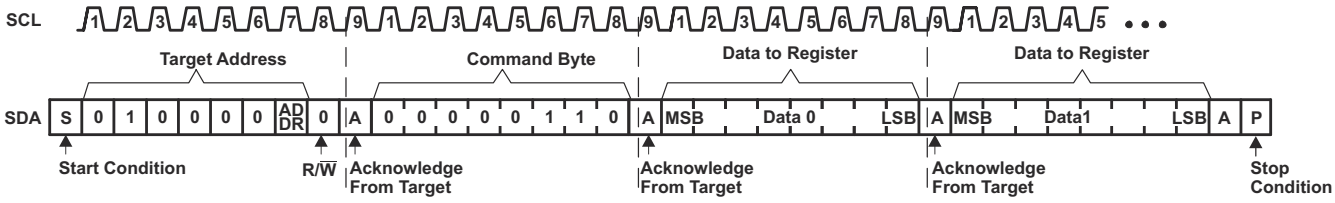


Figure 7-10. Write to Configuration Registers

7.6.4.2 Reads

The bus controller must first send the TCAL6416 address with the LSB set to a logic 0 (see Figure 7-7 for device address). The command byte is sent after the address and determines which register is accessed.

After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte is sent by the TCAL6416 (see Figure 7-11 and Figure 7-12).

Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflects the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0. There is no limit on the number of data bytes received in one read transmission, but on the final byte received, the bus controller must not acknowledge the data. After a subsequent restart, the command byte contains the value of the next register to be read in the pair. For example, if Input Port 1 was read last before the restart, then the register that is read after the restart is the Input Port 0.

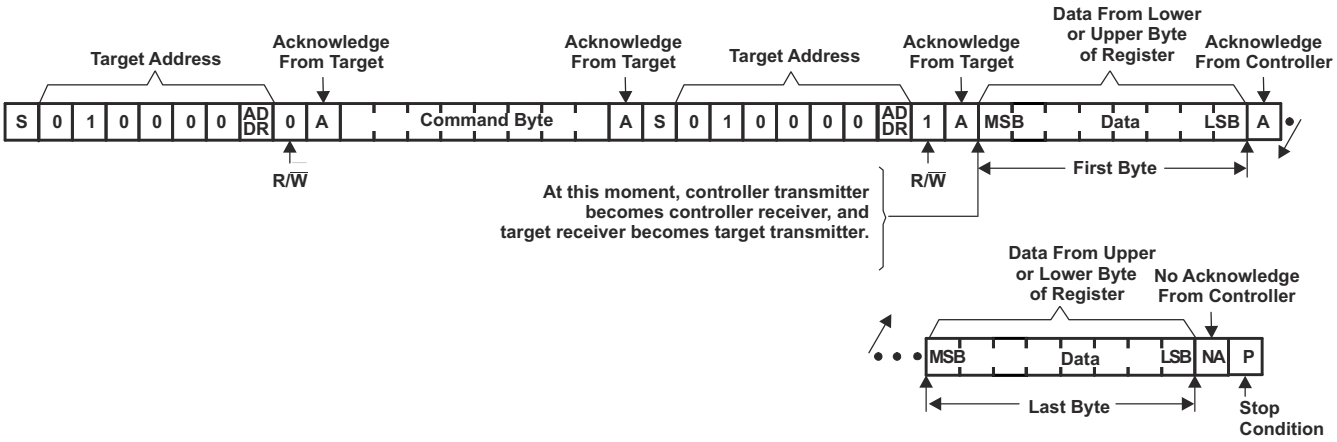
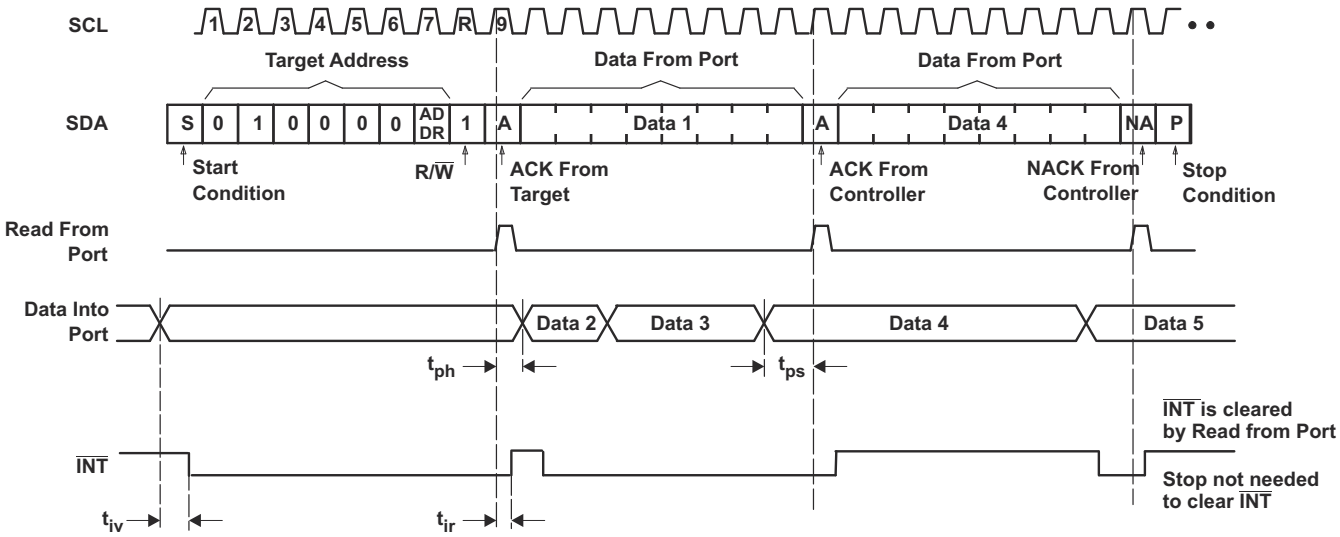


Figure 7-11. Read From Register



A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and target address call between the initial target address call and actual data transfer from P port (see Figure 7-11).

Figure 7-12. Read Input Port Register

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

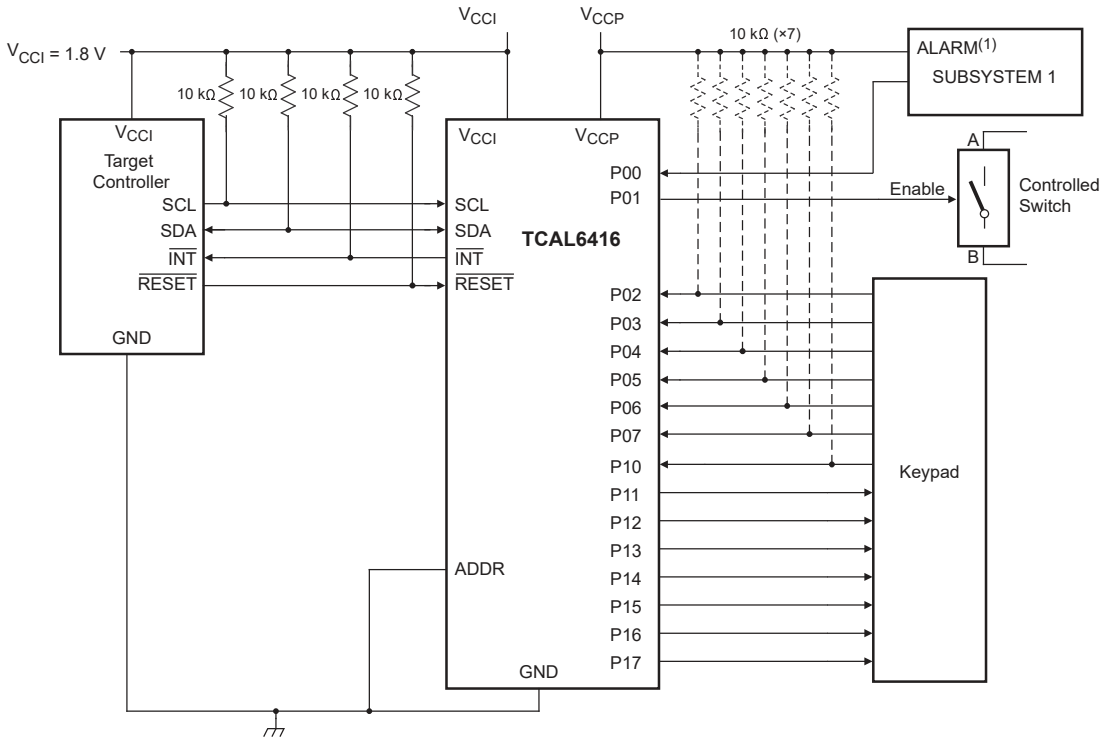
8.1 Application Information

TCAL6416 is used in applications where this device is connected as a target to an I^2C controller (processor); the I^2C bus may contain any number of other target devices. The TCAL6416 is in a remote location from the controller, placed close to the GPIOs to which the controller needs to monitor or control.

A typical application of the TCAL6416 operates with a lower voltage on the controller side (V_{CCI}), and a higher voltage on the P-port side (V_{CCP}). The P-ports can be configured as outputs connected to inputs of devices such as enable, reset, power select, the gate of a switch, and LEDs. The P-ports can also be configured as inputs to receive data from interrupts, alarms, status outputs, or push buttons.

8.2 Typical Application

Figure 8-1 shows an application in which the TCAL6416 can be used.



A. Device address configured as 0100000 for this example.
B. P00 and P02–P10 are configured as inputs.
C. P01 and P11–P17 are configured as outputs.
D. Resistors are required for inputs (on P port) that may float. If a driver to an input will never let the input float, then a resistor is not needed. Outputs (in the P port) do not need pullup resistors.

Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
I^2C input voltage (V_{CCI})	1.8V
P-port input/output voltage (V_{CCP})	3.6V
Output current rating, P-port sinking (I_{OL})	25mA
Output current rating, P-port sourcing (I_{OH})	10mA
I^2C bus clock (SCL) speed	1MHz

8.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all targets on the I^2C bus. The minimum pull-up resistance is a function of V_{CCI}, $V_{OL,(max)}$, and I_{OL}:

$$R_{p(min)} = \frac{V_{CCI} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (120ns for fast-mode-plus operation, f_{SCL} = 1MHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I^2C bus must not exceed 400pF for standard-mode or fast-mode operation, or 550pF for fast-mode-plus. The bus capacitance can be approximated by adding the capacitance of the TCAL6416, C_i for SCL, or C_{io} for SDA. Plus the capacitance of wires, connections, traces, and the capacitance of additional targets on the bus.

8.2.2.1 Minimizing I_{CC} When I/Os Control LEDs

As shown in Figure 8-2, normally I/Os are connected to V_{CCP} through a resistor when the I/Os are used to control LEDs. For a P-port configured as an input, current consumption increases as V_I becomes lower than V_{CCP}. The LEDs are diodes with threshold voltage V_T, and are off when a P-port is configured as an input, but the voltages at the P-port will be equal to V_{CCPCC} minus V_T.

For battery-powered applications, it is essential that the voltage of P-ports controlling the LEDs is greater than or equal to V_{CCP} when the P-ports are configured as input to minimize current consumption. Figure 8-2 shows a high-value resistor in parallel with the LED. Figure 8-3 shows V_{CCP} less than the LED supply voltage by at least V_T. Both of these methods maintain the I/O V_I at or above V_{CCP} and prevent additional supply current consumption when the P-port is configured as an input and the LED is off.

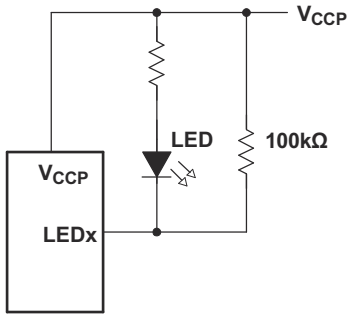


Figure 8-2. High-Value Resistor in Parallel with LED

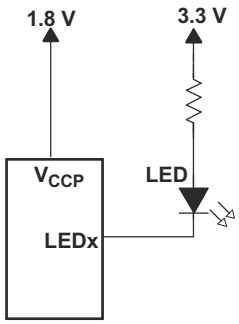
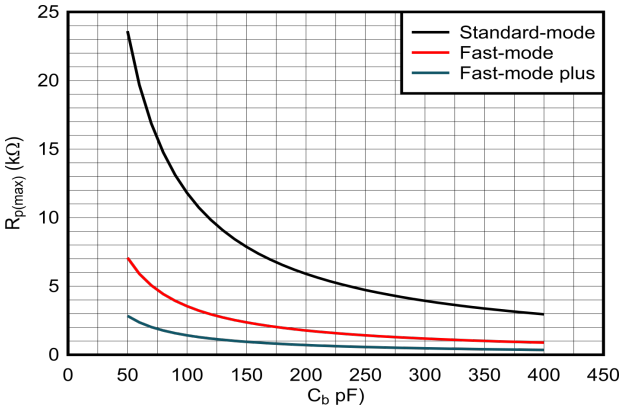


Figure 8-3. Device Supplied by a Lower Voltage

8.2.3 Application Curves



Standard-mode:	f_{SCL} = 100kHz	t_r = 1 µs
Fast-mode:	f_{SCL} = 400kHz	t_r = 300ns
Fast-mode plus:	f_{SCL} = 1MHz	t_r = 120ns

Figure 8-4. Maximum Pullup Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)

8.3 Power Supply Recommendations

8.3.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCAL6416 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

Figure 8-5 and Figure 8-6 shows the two types of power-on reset.

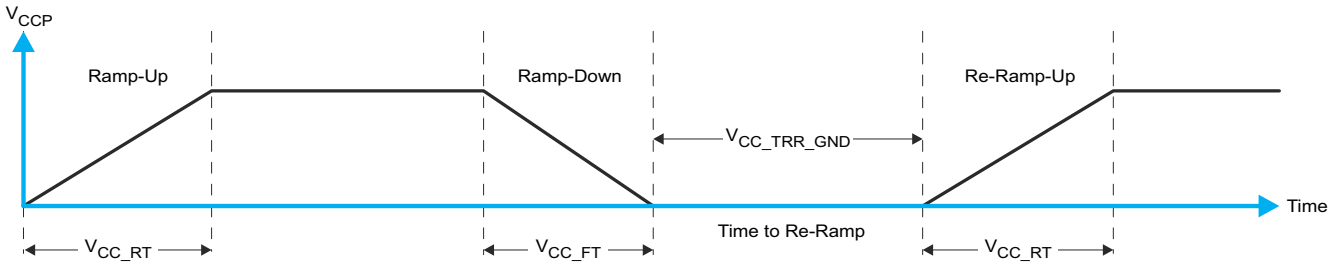


Figure 8-5. V_{CCP} is Lowered Below 0.2V or 0V and Then Ramped Up

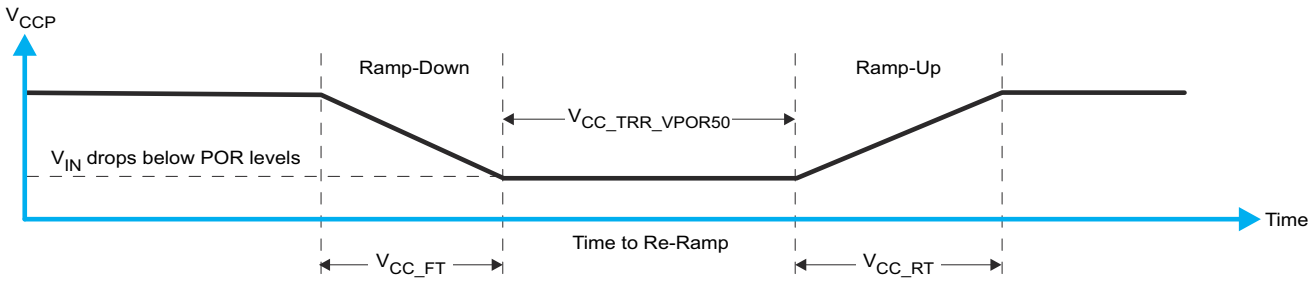


Figure 8-6. V_{CCP} is Lowered Below the POR Threshold, then Ramped Back Up

Table 8-2 lists the performance of the power-on reset feature for both types of power-on reset.

Table 8-2. Recommended Supply Sequencing and Ramp Rates

PARAMETER(1) (2)			MIN	TYP	MAX	UNIT
t_{FT}	Fall rate	See Figure 8-5	0.1		2000	ms
t_{RT}	Rise rate	See Figure 8-5	0.1		2000	ms
t_{TRR_GND}	Time to re-ramp (when V_{CC} drops to GND)	See Figure 8-5	1			µs
t_{TRR_POR50}	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50mV)	See Figure 8-6	1			µs
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCP_GW} = 1µs	See Figure 8-7			1.0	V
t_{GW}	Glitch width that will not cause a functional disruption when V_{CCP_GH} = 0.5 × V_{CCx}	See Figure 8-7			10	µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.6			V
V_{PORR}	Voltage trip point of POR on rising V_{CC}				1.0	V

(1) T_A = 25°C (unless otherwise noted).
(2) Not tested. Specified by design.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. For more information on how to measure these specifications, see Figure 8-7 and Table 8-2.

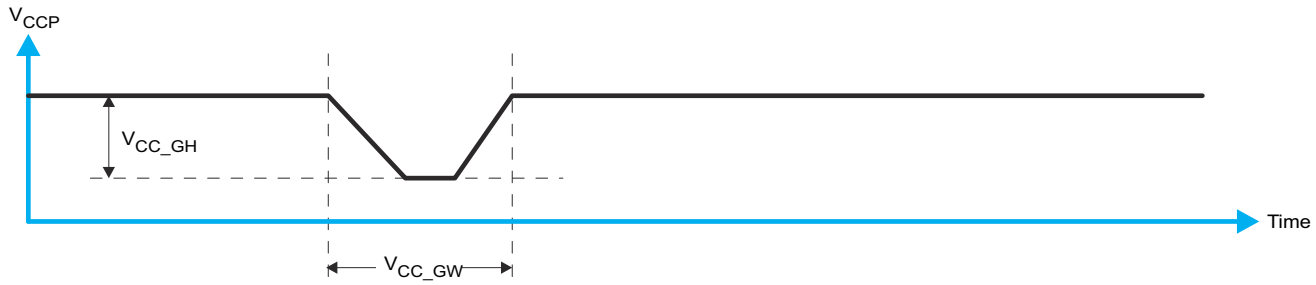


Figure 8-7. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CCP} being lowered to or from 0. For more details on this specification, see Figure 8-8 and Table 8-2.

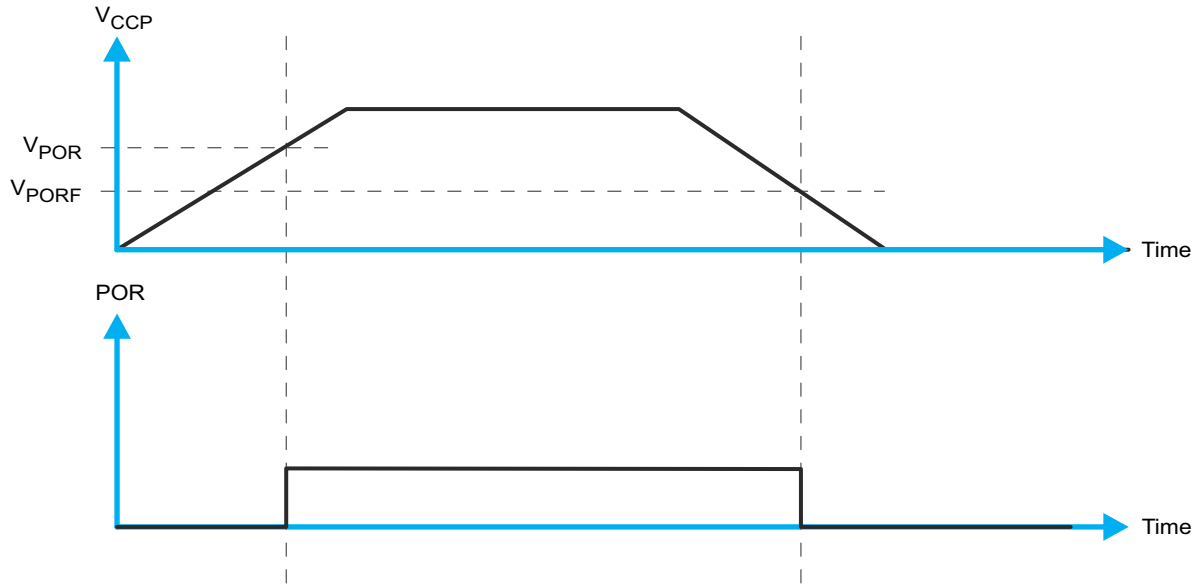


Figure 8-8. V_{POR}

8.4 Layout

8.4.1 Layout Guidelines

For device reliability, follow common printed circuit board (PCB) layout practices. Additional concerns related to high-speed data transfer, such as matched impedance and differential pairs, are not a concern for I^2C signal speeds.

It is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces in all PCB layouts. Bypass and decoupling capacitors are commonly used to control the voltage on the supply pins. Using a larger capacitor provides additional power in the event of a short power supply glitch, and using a smaller capacitor filters out high-frequency ripple. These capacitors should be placed as close to the TCAL6416 as possible. Figure 8-9 shows these best practices.

For the layout example provided in Figure 8-9 , it is possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to power or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 8-9 .

8.4.2 Layout Example

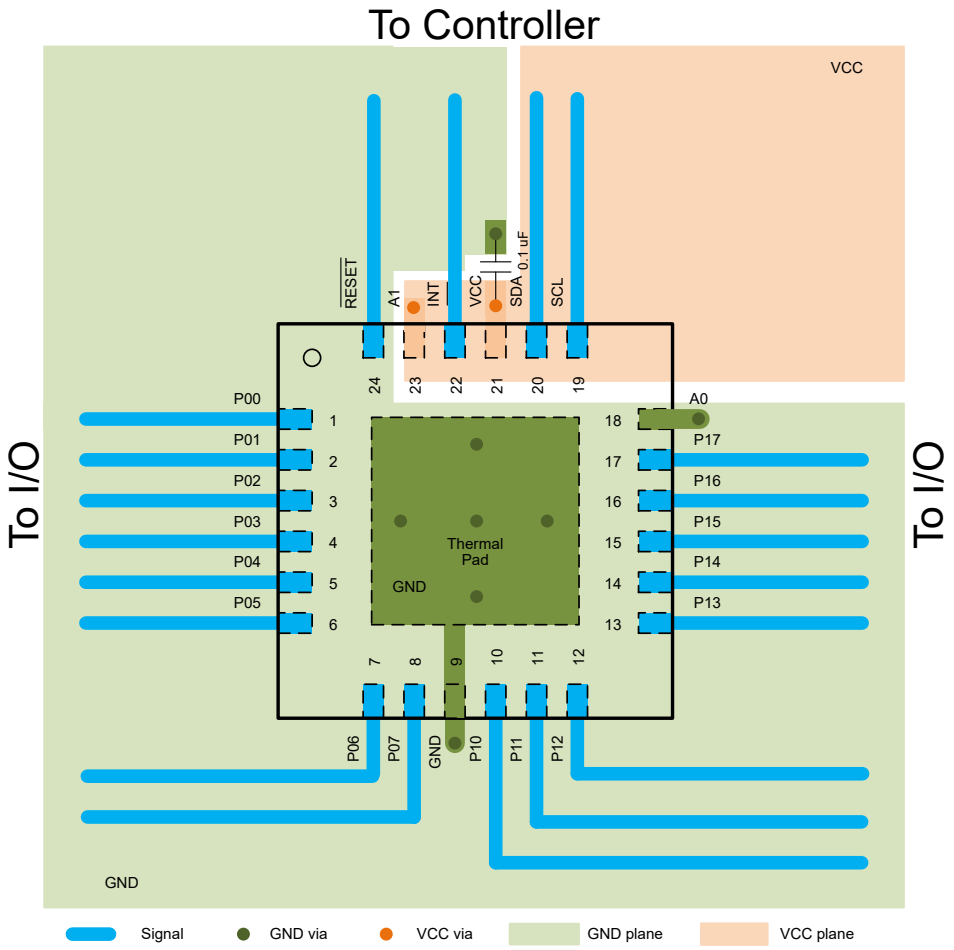


Figure 8-9. TCAL6416 Layout

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

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All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2025) to Revision E (September 2025)	Page
• Deleted the register description for TCAL6416RA/B	25

Changes from Revision C (June 2023) to Revision D (January 2025)	Page
• Added the package 24-pin VSSOP to the Package Information table	1
• Added the package 24-Pin VSSOP	3

Changes from Revision B (April 2023) to Revision C (June 2023)	Page
• Changed the document title from: TCAL6416 16-Bit I2C-Bus to: *TCAL6416 16-Bit Translating I2C-Bus*	1
• Changed the *Package Information* table, included note 2	1

Changes from Revision A (August 2022) to Revision B (April 2023)	Page
• Deleted the Product Preview note from TSSOP in the *Package Information* table	1

Changes from Revision * (June 2022) to Revision A (August 2022)	Page
• Changed the document from: Advanced Information to: *Production* data	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAL6416DGSR	Active	Production	VSSOP (DGS) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L6416
TCAL6416DGSR.A	Active	Production	VSSOP (DGS) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L6416
TCAL6416PWR	Active	Production	TSSOP (PW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TCAL6416
TCAL6416PWR.A	Active	Production	TSSOP (PW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TCAL6416
TCAL6416RTWR	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TCAL 6416
TCAL6416RTWR.A	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TCAL 6416
TCAL6416RTWRG4	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TCAL 6416
TCAL6416RTWRG4.A	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TCAL 6416

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

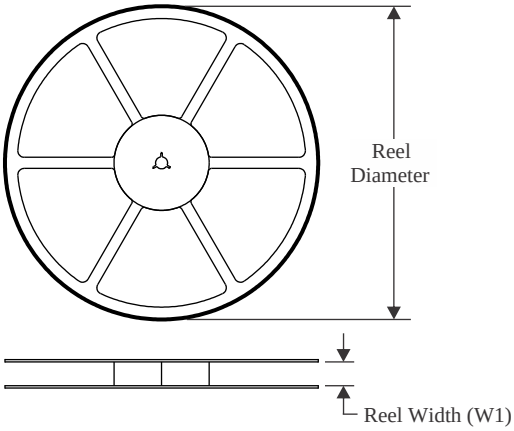
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

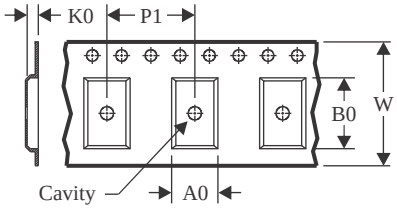
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

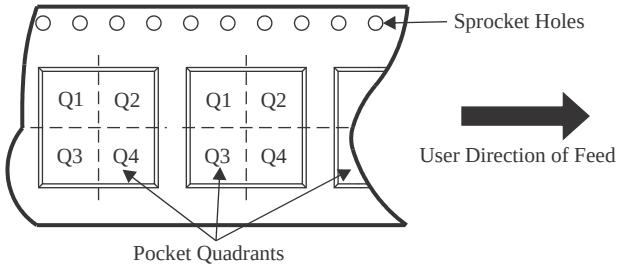


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

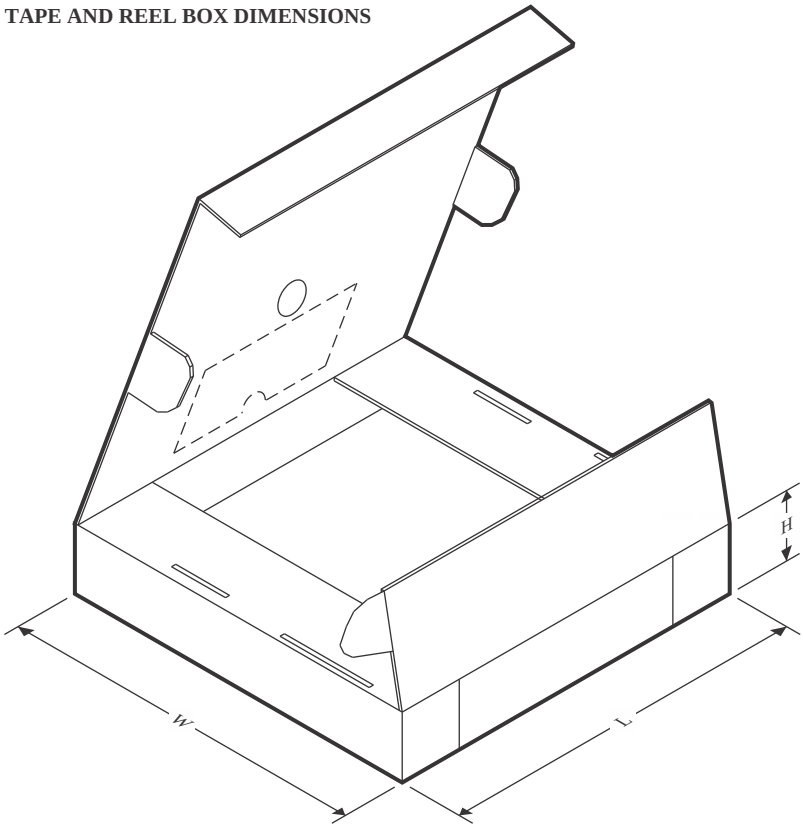
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAL6416DGSR	VSSOP	DGS	24	5000	330.0	16.4	5.44	6.4	1.45	8.0	16.0	Q1
TCAL6416PWR	TSSOP	PW	24	3000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TCAL6416RTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TCAL6416RTWRG4	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAL6416DGSR	VSSOP	DGS	24	5000	353.0	353.0	32.0
TCAL6416PWR	TSSOP	PW	24	3000	353.0	353.0	32.0
TCAL6416RTWR	WQFN	RTW	24	3000	367.0	367.0	35.0
TCAL6416RTWRG4	WQFN	RTW	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

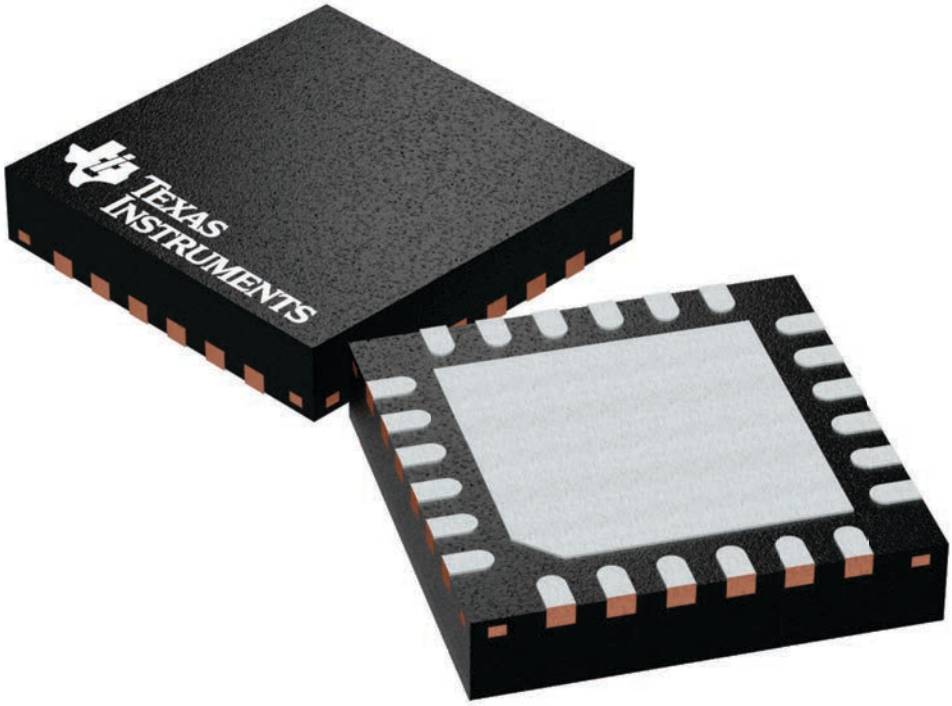
RTW 24

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

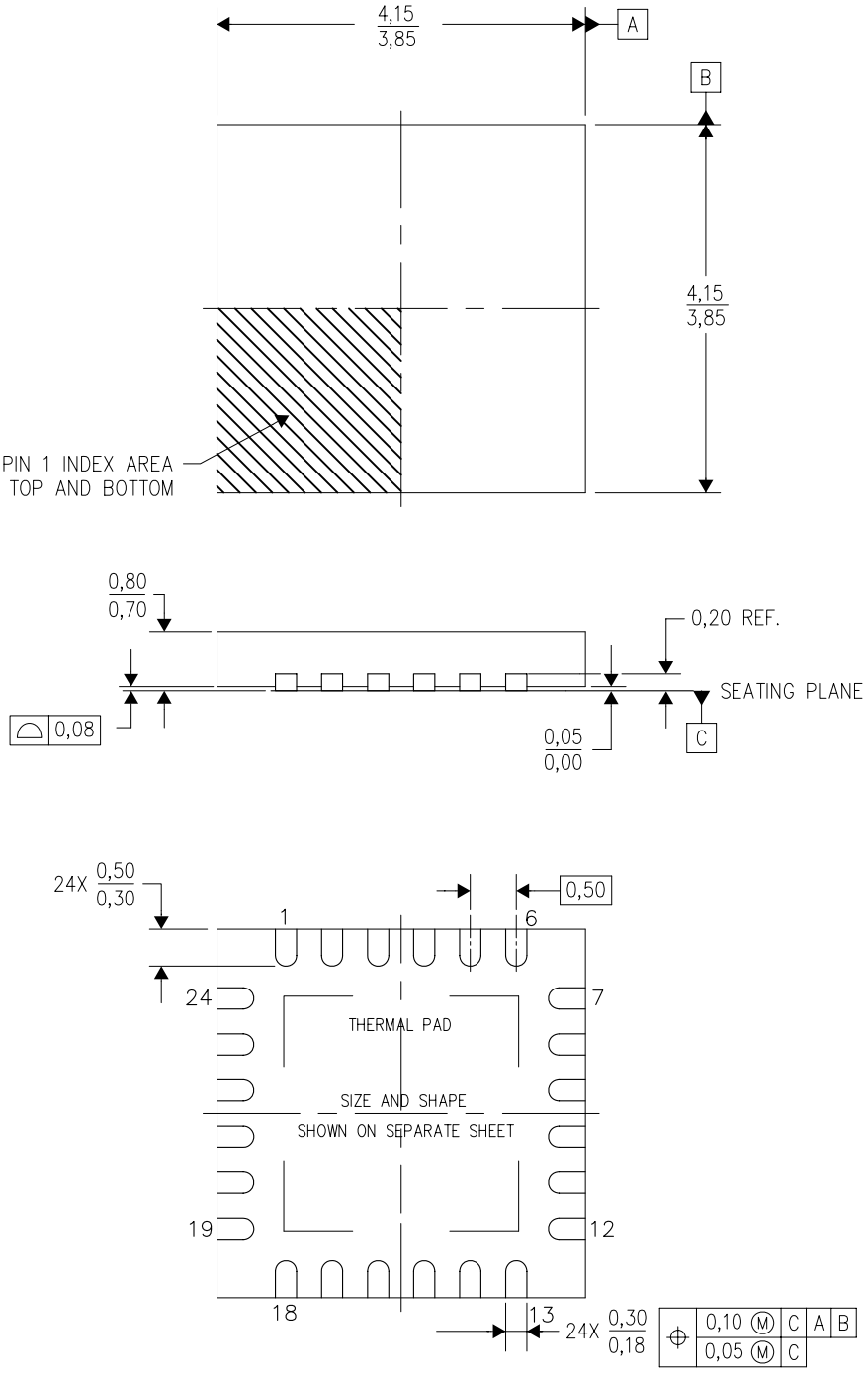
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224801/A

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

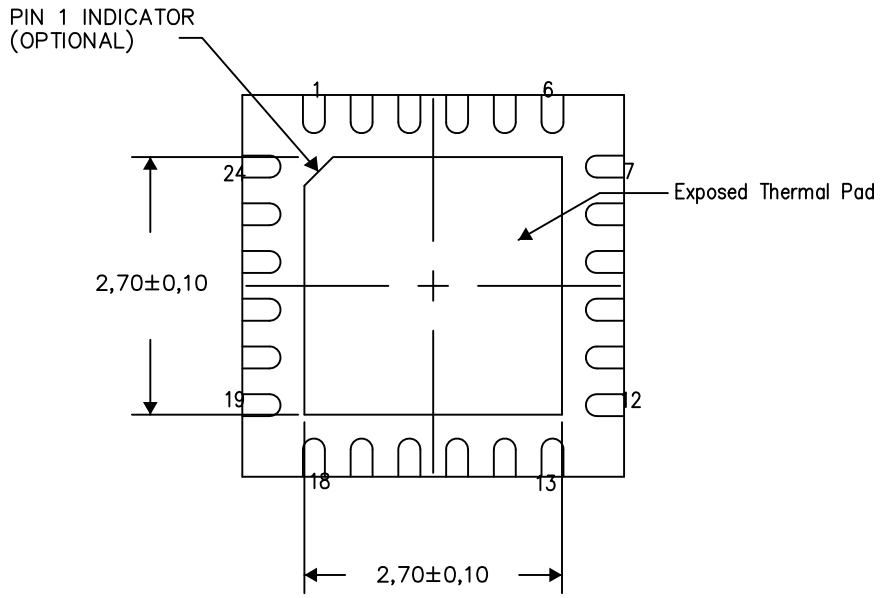
RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



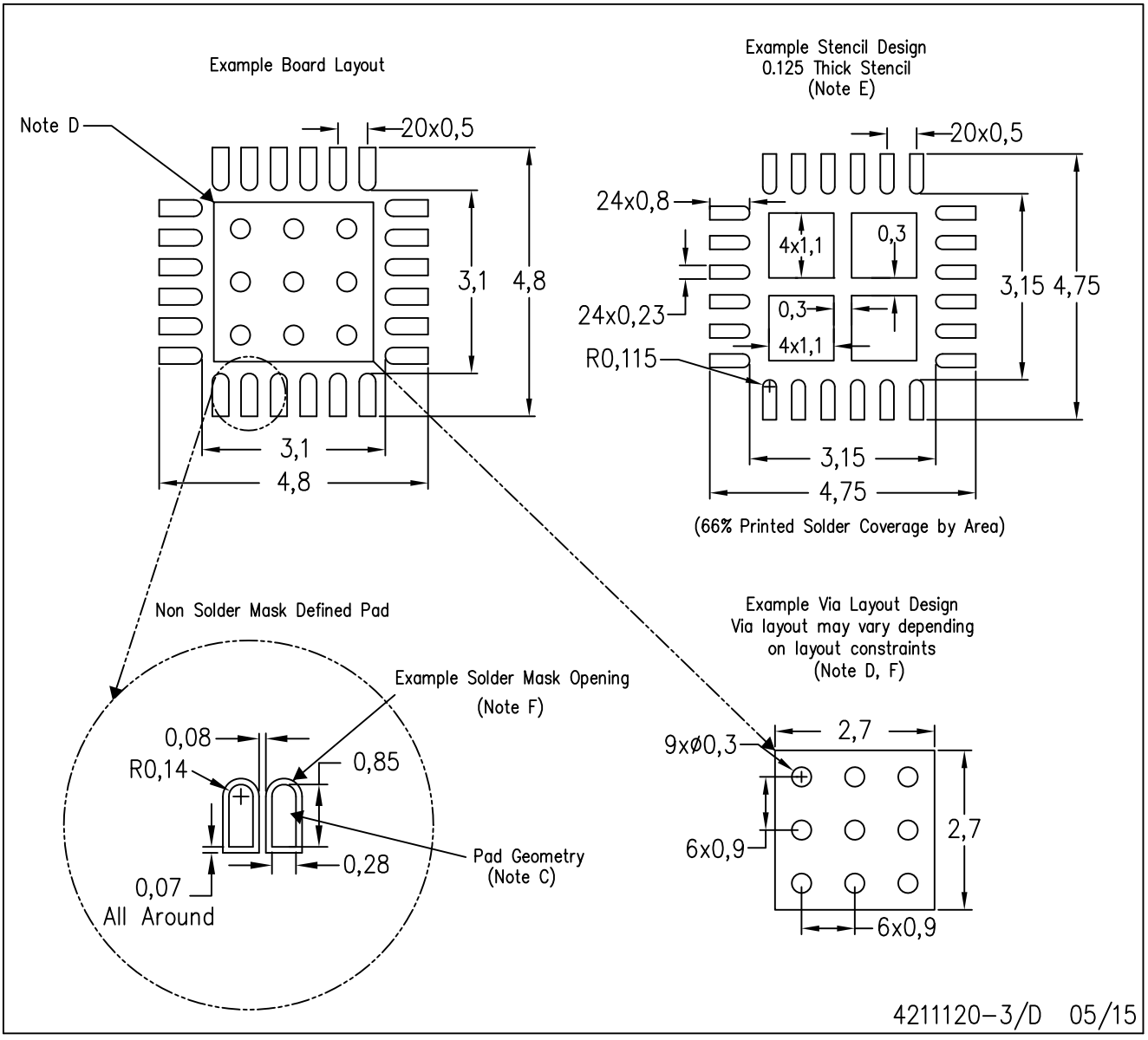
Bottom View

Exposed Thermal Pad Dimensions

4206249–5/P 05/15

NOTES: A. All linear dimensions are in millimeters

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



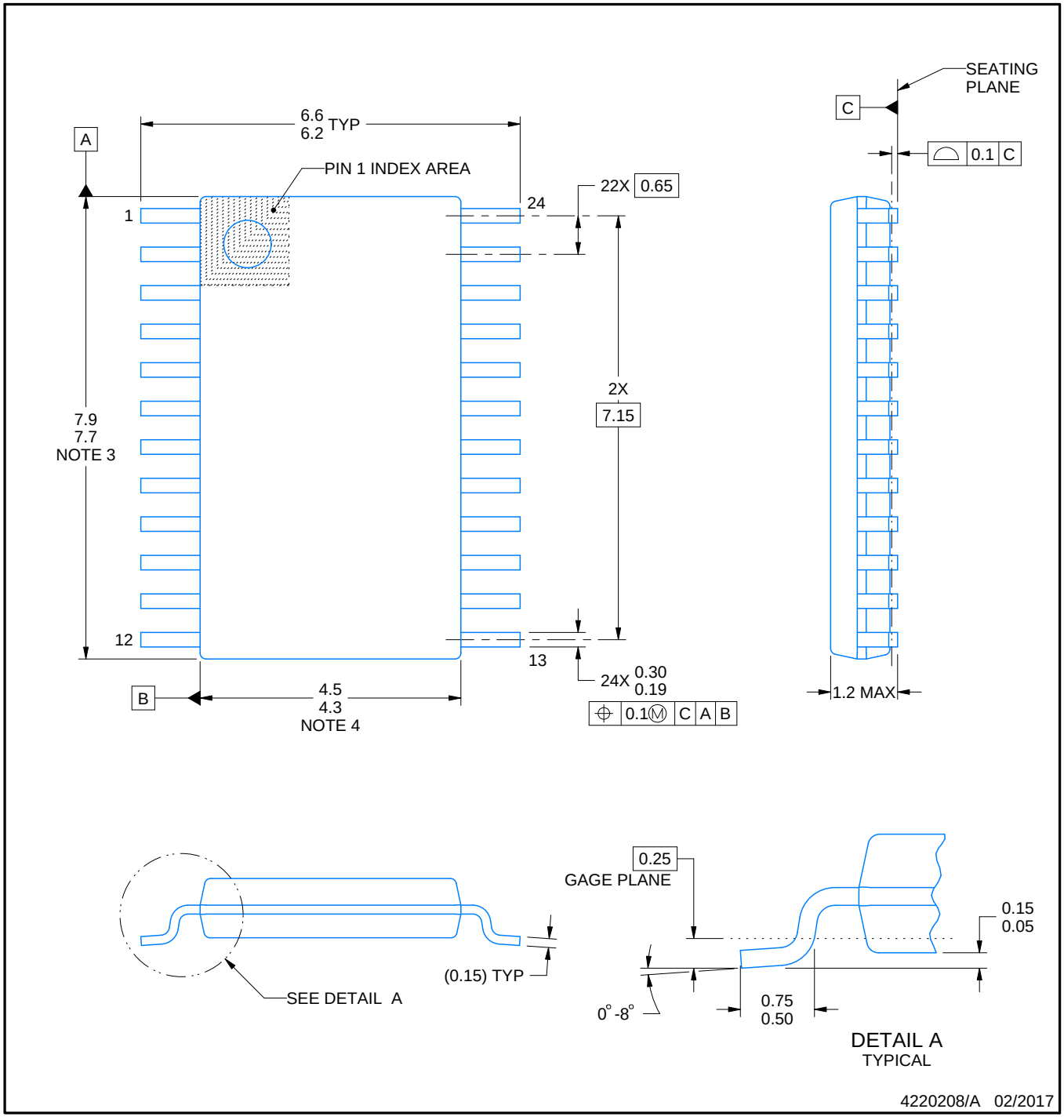
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PACKAGE OUTLINE

PW0024A

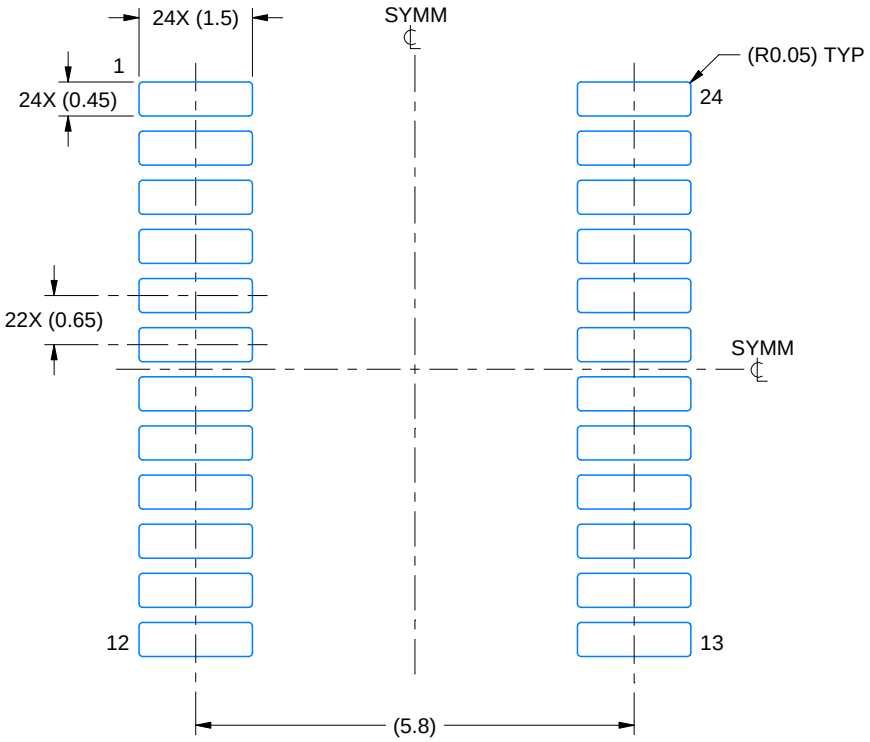
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

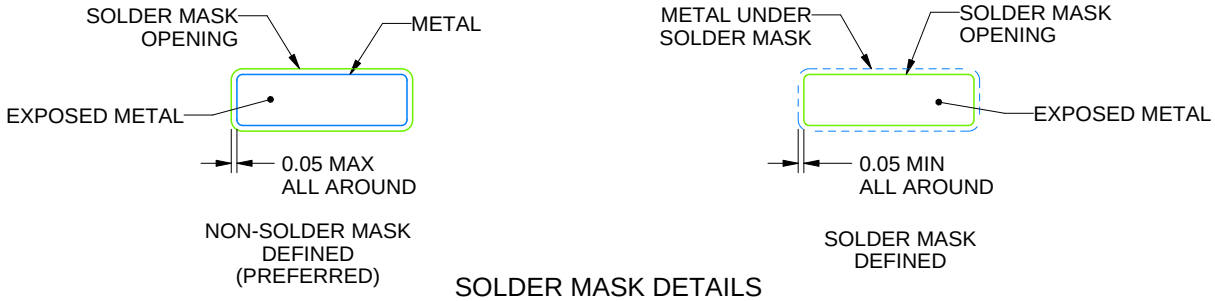


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

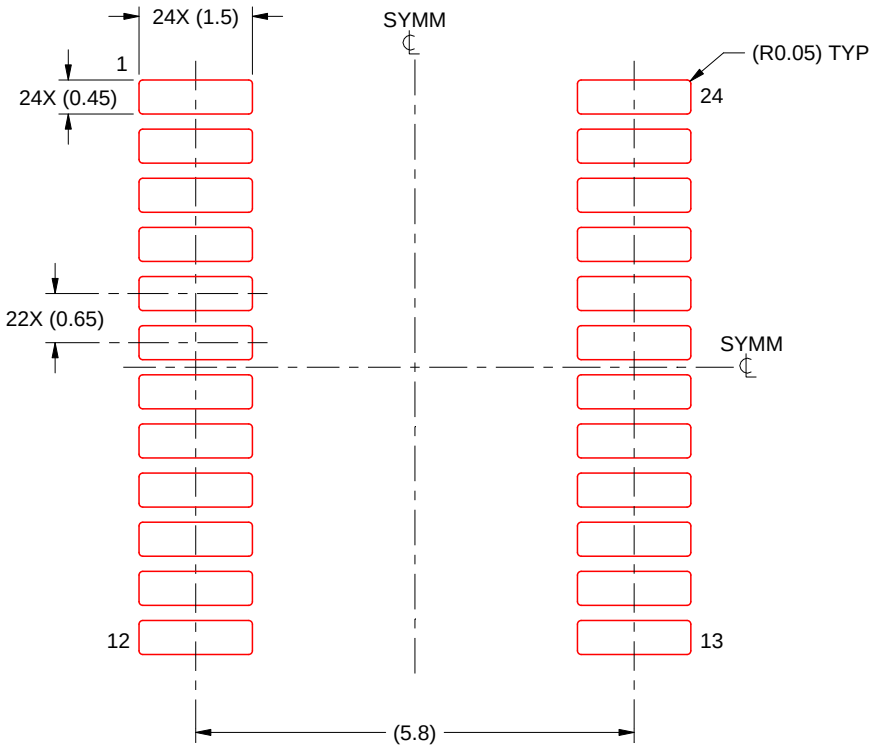


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

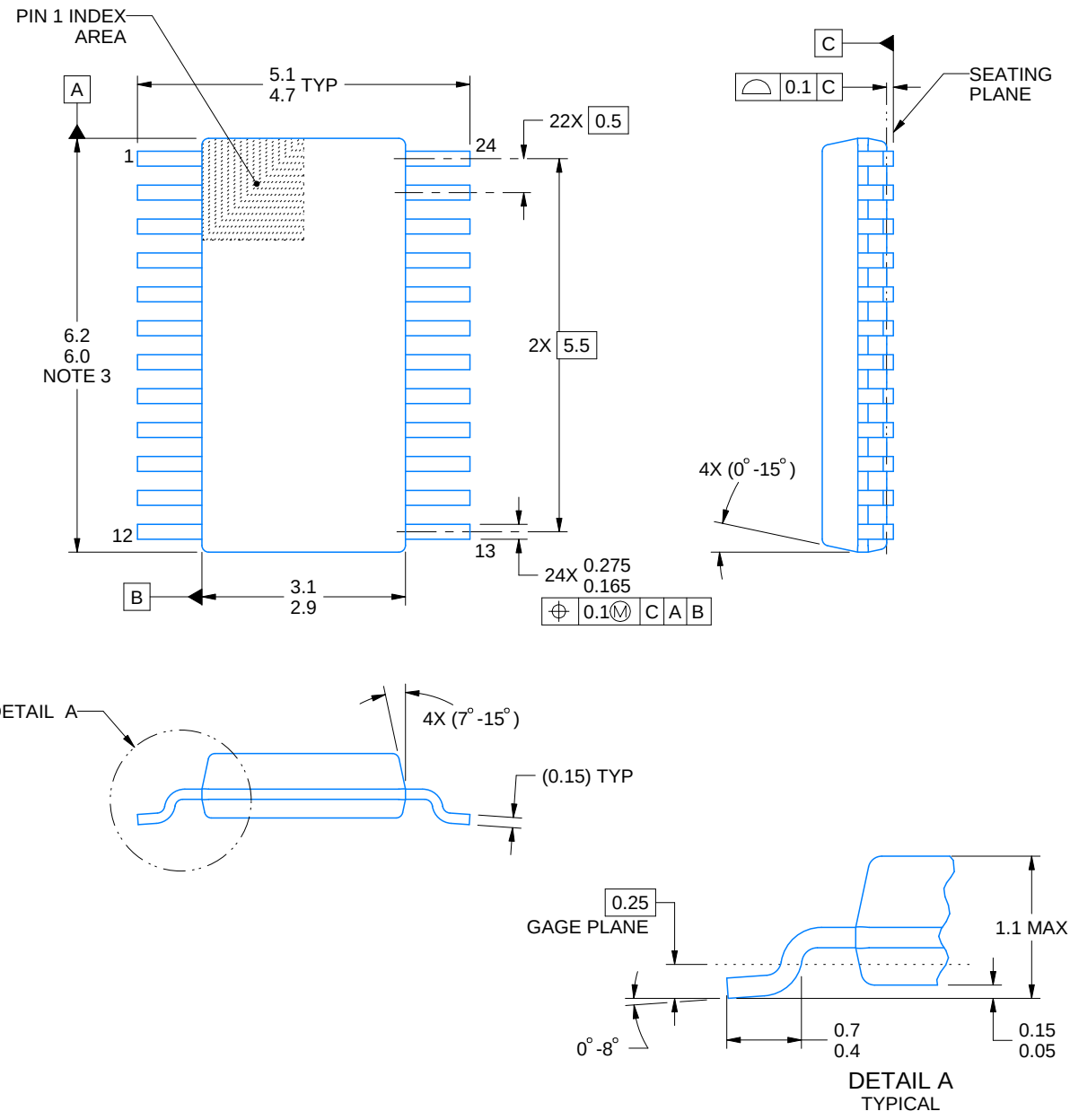
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0024A

VSSOP - 1.1 mm max height

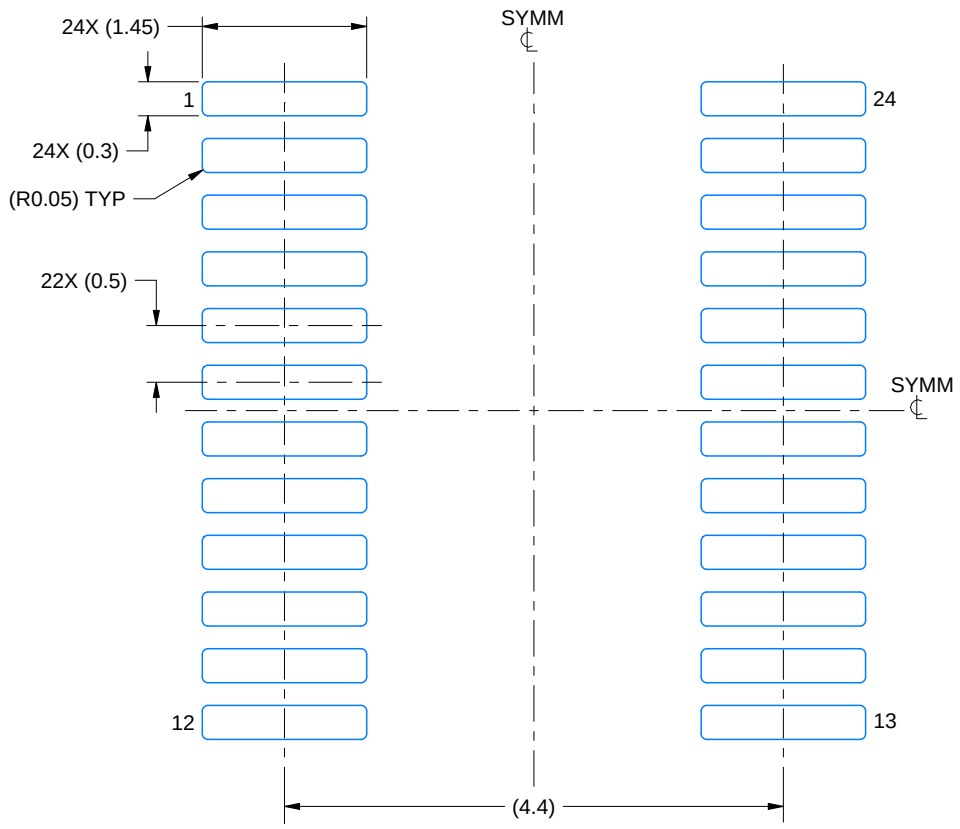
SMALL OUTLINE PACKAGE



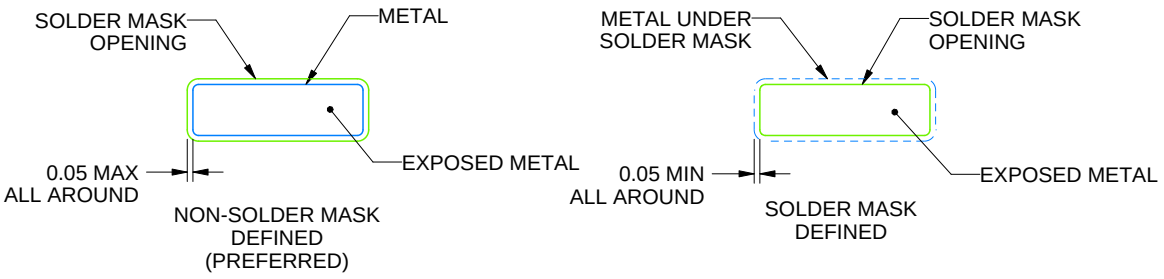
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 15X

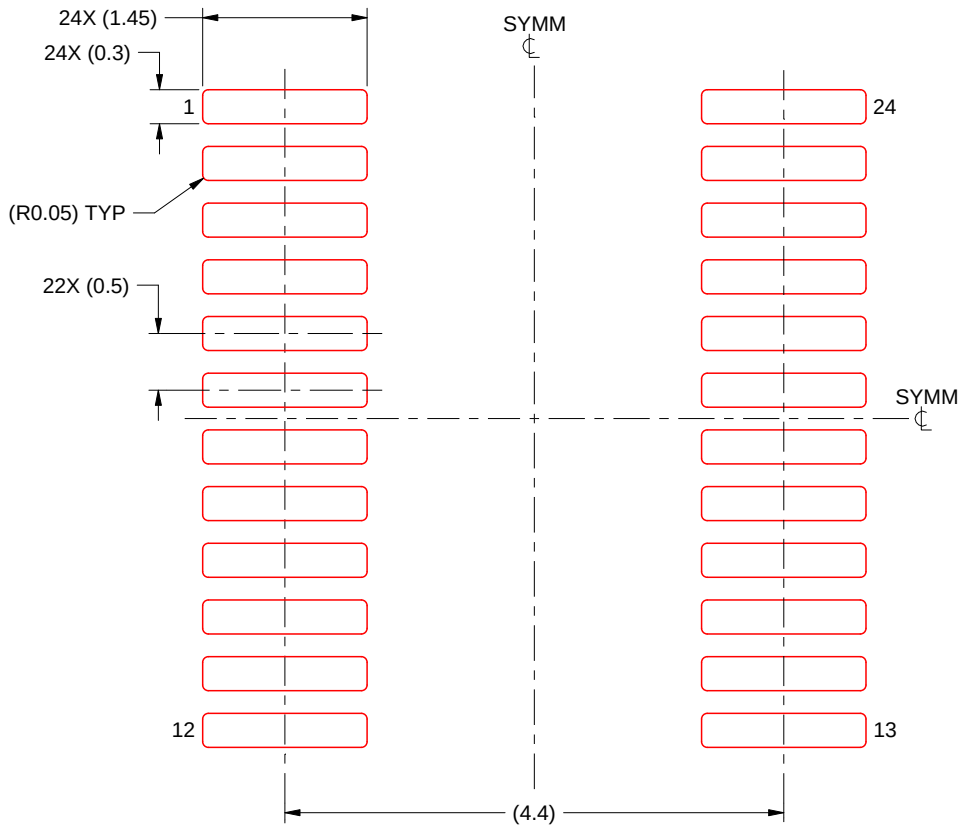


SOLDER MASK DETAILS

4226366/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

4226366/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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