



# THE DATASHEET OF TLV7022DDFR



## RS-232 TRANSCEIVER WITH SPLIT SUPPLY PIN FOR LOGIC SIDE

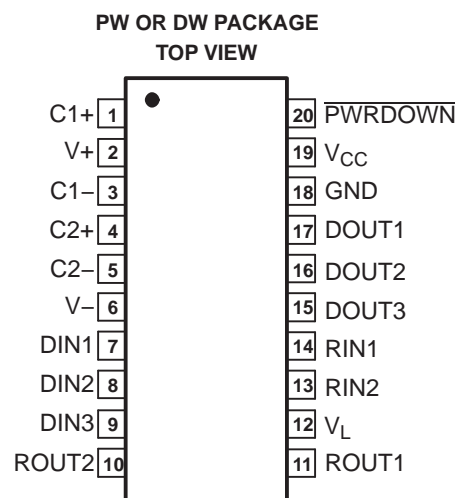
 Check for Samples: [TRS3386E](#)

### FEATURES

- $V_L$  Pin for Compatibility With Mixed-Voltage Systems Down to 2.5 V on Logic Side
- Enhanced ESD Protection on RIN Inputs and DOUT Outputs
  - $\pm 15$ -kV Human-Body Model
  - $\pm 15$ -kV IEC 61000-4-2, Air-Gap Discharge
  - $\pm 8$ -kV IEC 61000-4-2, Contact Discharge
- Low 300- $\mu$ A Supply Current
- Specified 250-kbps Data Rate
- 1- $\mu$ A Low-Power Shutdown
- Meets EIA/TIA-232 Specifications Down to 3 V
- Designed to be Interchangeable With Industry Standard '3386 Devices

### APPLICATIONS

- Hand-Held Equipment
- PDAs
- Cell Phones
- Battery-Powered Equipment
- Data Cables



### DESCRIPTION/ORDERING INFORMATION

The TRS3386E is a three-driver and two-receiver RS-232 interface device, with split supply pins for mixed-signal operations. All RS-232 inputs and outputs are protected to  $\pm 15$  kV using the IEC 61000-4-2 Air-Gap Discharge method,  $\pm 8$  kV using the IEC 61000-4-2 Contact Discharge method, and  $\pm 15$  kV using the Human-Body Model.

The charge pump requires only four small 0.1- $\mu$ F capacitors for operation from a 3.3-V supply. The TRS3386E is capable of running at data rates up to 250 kbps, while maintaining RS-232-compliant output levels.

The TRS3386E has a unique  $V_L$  pin that allows operation in mixed-logic voltage systems. Both driver in (DIN) and receiver out (ROUT) logic levels are pin programmable through the  $V_L$  pin. The TRS3386E is available in a space-saving thin shrink small-outline package (TSSOP).

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1) (2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	TSSOP – PW	TRS3386ECPWR	RV86EC
	SOIC – DW	TRS3386ECDWR	TRS3386EC
–40°C to 85°C	TSSOP – PW	TRS3386EIPWR	RV86EI
	SOIC – DW	TRS3386EIDWR	TRS3386EI

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

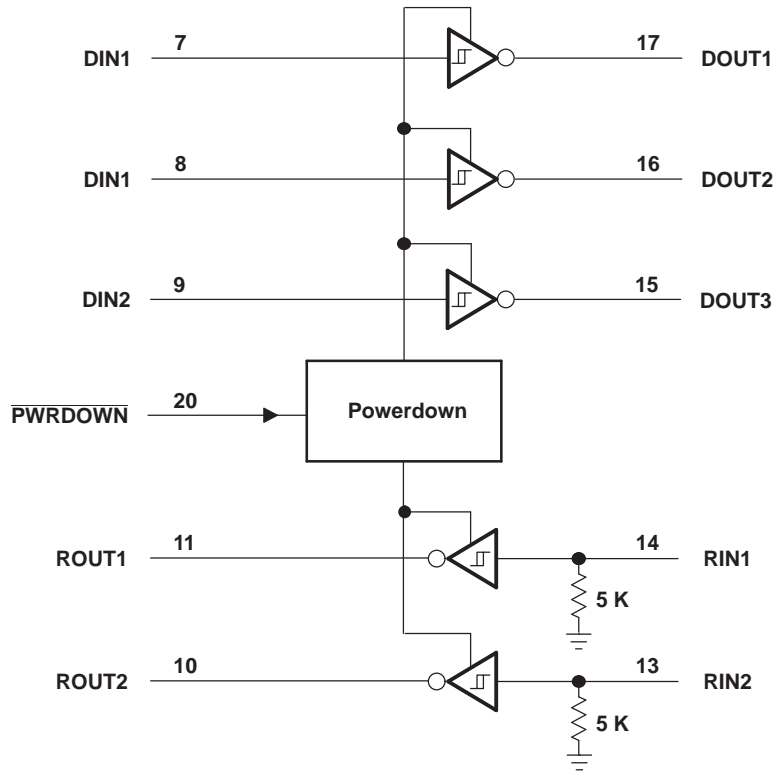


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**Table 1. TRUTH TABLE (SHUTDOWN FUNCTION)**

$\overline{\text{PWRDWN}}$	DRIVER OUTPUTS	RECEIVER OUTPUTS	CHARGE PUMP
L	High-Z	High-Z	Inactive
H	Active	Active	Active

**FUNCTIONAL BLOCK DIAGRAM**



**TERMINAL FUNCTIONS**

TERMINAL		DESCRIPTION
NAME	NO.	
C1+	1	Positive terminal of the voltage-doubler charge-pump capacitor
V+	2	5.5-V supply generated by the charge pump
C1–	3	Negative terminal of the voltage-doubler charge-pump capacitor
C2+	4	Positive terminal of the inverting charge-pump capacitor
C2–	5	Negative terminal of the inverting charge-pump capacitor
V–	6	–5.5-V supply generated by the charge pump
DIN1	7	Driver inputs
DIN2	8	
DIN3	9	
ROUT2	10	Receiver outputs. Swing between 0 and V <sub>L</sub> .
ROUT1	11	
V <sub>L</sub>	12	Logic-level supply. All CMOS inputs and outputs are referenced to this supply.
RIN2	13	RS-232 receiver inputs
RIN1	14	
DOUT3	15	RS-232 driver outputs
DOUT2	16	
DOUT1	17	
GND	18	Ground
V <sub>CC</sub>	19	3-V to 5.5-V supply voltage
$\overline{\text{PWRDWN}}$	20	Powerdown input L = Powerdown H = Normal operation

**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub> to GND		–0.3	6	V
V <sub>L</sub> to GND		–0.3	V <sub>CC</sub> + 0.3	V
V+ to GND		–0.3	7	V
V– to GND		0.3	–7	V
V+ +  V–  <sup>(2)</sup>			13	V
V <sub>I</sub>	Input voltage	DIN, $\overline{\text{PWRDWN}}$ to GND		V
		RIN to GND		
V <sub>O</sub>	Output voltage	DOUT to GND		V
		ROUT		
Short-circuit duration DOUT to GND		Continuous		
Continuous power dissipation		T <sub>A</sub> = 70°C, 20-pin TSSOP (derate 7 mW/°C above 70°C)		mW
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature range	–65	150	°C
	Lead temperature (soldering, 10 s)		300	°C

- Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- V+ and V– can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.

### Recommended Operating Conditions

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		3	5.5	V
V <sub>L</sub>	Supply voltage		2.25	V <sub>CC</sub>	V
Input logic threshold low	DIN, $\overline{\text{PWRDWN}}$	V <sub>L</sub> = 3 V or 5.5 V		0.8	V
		V <sub>L</sub> = 2.3 V		0.6	
Input logic threshold high	DIN, $\overline{\text{PWRDWN}}$	V <sub>L</sub> = 5.5 V	2.4		V
		V <sub>L</sub> = 3 V	2.0		
		V <sub>L</sub> = 2.7 V	1.4		
Operating temperature		TRS3386ECPWR	0	70	°C
		TRS3386EIPWR	-40	85	
Receiver input voltage			-25	25	V

### Electrical Characteristics

over operating free-air temperature range, V<sub>CC</sub> = V<sub>L</sub> = 3 V to 5.5 V, C1–C4 = 0.1 μF (tested at 3.3 V ± 10%), C1 = 0.047 μF, C2–C4 = 0.33 μF (tested at 5 V ± 10%) (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>DC Characteristics (V<sub>CC</sub> = 3.3 V or 5 V, T<sub>A</sub> = 25°C)</b>					
Powerdown supply current	$\overline{\text{PWRDWN}}$ = GND, All inputs at V <sub>CC</sub> or GND		1	10	μA
Supply current	$\overline{\text{PWRDWN}}$ = V <sub>CC</sub> , No load		0.3	1	mA

(1) Typical values are at V<sub>CC</sub> = V<sub>L</sub> = 3.3 V, T<sub>A</sub> = 25°C.

### ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
RIN, DOUT	Human-Body Model	±15	kV
	IEC 61000-4-2 Air-Gap Discharge	±15	
	IEC 61000-4-2 Contact Discharge	±8	

## RECEIVER SECTION

### Electrical Characteristics

over operating free-air temperature range,  $V_{CC} = V_L = 3\text{ V}$  to  $5.5\text{ V}$ ,  $C1\text{--}C4 = 0.1\text{ }\mu\text{F}$  (tested at  $3.3\text{ V} \pm 10\%$ ),  $C1 = 0.047\text{ }\mu\text{F}$ ,  $C2\text{--}C4 = 0.33\text{ }\mu\text{F}$  (tested at  $5\text{ V} \pm 10\%$ ),  $T_A = T_{MIN}$  to  $T_{MAX}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$I_{off}$	Output leakage current	ROUT, receivers disabled			$\pm 0.05$	$\pm 10$	$\mu\text{A}$
$V_{OL}$	Output voltage low	$I_{OUT} = 1.6\text{ mA}$				0.4	V
$V_{OH}$	Output voltage high	$I_{OUT} = -1\text{ mA}$		$V_L - 0.6$	$V_L - 0.1$		V
$V_{IT-}$	Input threshold low	$T_A = 25^\circ\text{C}$	$V_L = 5\text{ V}$	0.8	1.2		V
			$V_L = 3.3\text{ V}$	0.6	1.5		
$V_{IT+}$	Input threshold high	$T_A = 25^\circ\text{C}$	$V_L = 5\text{ V}$		1.8	2.4	V
			$V_L = 3.3\text{ V}$		1.5	2.4	
$V_{hys}$	Input hysteresis				0.5		V
	Input resistance	$T_A = 25^\circ\text{C}$		3	5	7	k $\Omega$

(1) Typical values are at  $V_{CC} = V_L = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$

### Switching Characteristics

over operating free-air temperature range,  $V_{CC} = V_L = 3\text{ V}$  to  $5.5\text{ V}$ ,  $C1\text{--}C4 = 0.1\text{ }\mu\text{F}$  (tested at  $3.3\text{ V} \pm 10\%$ ),  $C1 = 0.047\text{ }\mu\text{F}$ ,  $C2\text{--}C4 = 0.33\text{ }\mu\text{F}$  (tested at  $5\text{ V} \pm 10\%$ ),  $T_A = T_{MIN}$  to  $T_{MAX}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP <sup>(1)</sup>	UNIT
$t_{PHL}$	Receiver propagation delay	Receiver input to receiver output, $C_L = 150\text{ pF}$	0.15	$\mu\text{s}$
$t_{PLH}$			0.15	
$t_{PHL} - t_{PLH}$	Receiver skew		50	ns
$t_{en}$	Receiver output enable time	From $\overline{\text{PWRDWN}}$	200	ns
$t_{dis}$	Receiver output disable time	From $\overline{\text{PWRDWN}}$	200	ns

(1) Typical values are at  $V_{CC} = V_L = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## DRIVER SECTION

### Electrical Characteristics

over operating free-air temperature range,  $V_{CC} = V_L = 3\text{ V to }5.5\text{ V}$ ,  $C1-C4 = 0.1\ \mu\text{F}$  (tested at  $3.3\text{ V} \pm 10\%$ ),  $C1 = 0.047\ \mu\text{F}$ ,  $C2-C4 = 0.33\ \mu\text{F}$  (tested at  $5\text{ V} \pm 10\%$ ),  $T_A = T_{MIN}$  to  $T_{MAX}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{OH}$ Output voltage swing	All driver outputs loaded with $3\text{ k}\Omega$ to ground	$\pm 5$	$\pm 5.4$		V
$r_o$ Output resistance	$V_{CC} = V_+ = V_- = 0$ , Driver output = $\pm 2\text{ V}$	300	10M		$\Omega$
$I_{OS}$ Output short-circuit current	$V_{T\_OUT} = 0$			$\pm 60$	mA
$I_{OZ}$ Output leakage current	$V_{T\_OUT} = \pm 12\text{ V}$ , Driver disabled, $V_{CC} = 0$ or $3\text{ V to }5.5\text{ V}$			$\pm 25$	$\mu\text{A}$
Driver input hysteresis				0.5	V
Input leakage current	DIN, $\overline{\text{PWRDWN}}$		$\pm 0.01$	$\pm 1$	$\mu\text{A}$

(1) Typical values are at  $V_{CC} = V_L = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$

### Timing Requirements

over operating free-air temperature range,  $V_{CC} = V_L = 3\text{ V to }5.5\text{ V}$ ,  $C1-C4 = 0.1\ \mu\text{F}$  (tested at  $3.3\text{ V} \pm 10\%$ ),  $C1 = 0.047\ \mu\text{F}$ ,  $C2-C4 = 0.33\ \mu\text{F}$  (tested at  $5\text{ V} \pm 10\%$ ),  $T_A = T_{MIN}$  to  $T_{MAX}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
Maximum data rate	$R_L = 3\text{ k}\Omega$ , $C_L = 1000\text{ pF}$ , One driver switching	250			kbps
Time-to-exit powerdown	$ V_{T\_OUT}  > 3.7\text{ V}$		100		$\mu\text{s}$
$ t_{PHL} - t_{PLH} $ Driver skew <sup>(2)</sup>			100		ns
Transition-region slew rate	$V_{CC} = 3.3\text{ V}$ , $T_A = 25^\circ\text{C}$ , $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ , Measured from $3\text{ V}$ to $-3\text{ V}$ or $-3\text{ V}$ to $3\text{ V}$				V/ $\mu\text{s}$
	$C_L = 150\text{ pF to }1000\text{ pF}$	6		30	
		4		30	

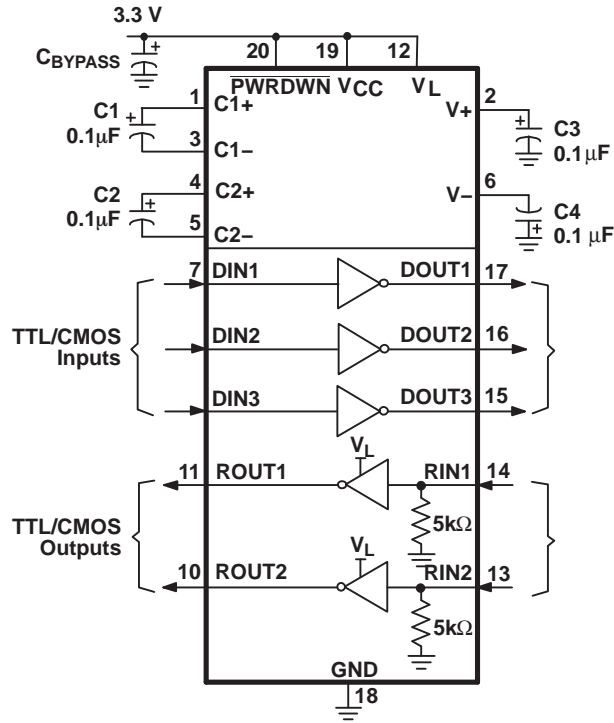
(1) Typical values are at  $V_{CC} = V_L = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) Driver skew is measured at the driver zero crosspoint.

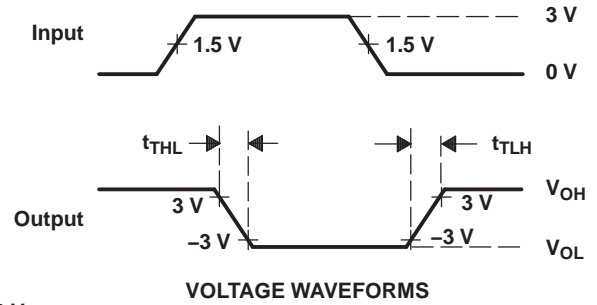
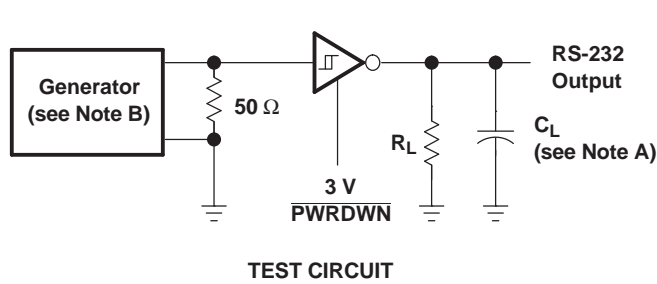
### ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
RIN, DOUT	Human-Body Model	$\pm 15$	kV
	IEC 61000-4-2 Air-Gap Discharge	$\pm 15$	
	IEC 61000-4-2 Contact Discharge	$\pm 8$	

APPLICATION INFORMATION



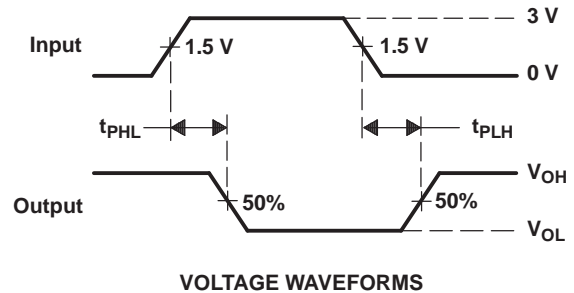
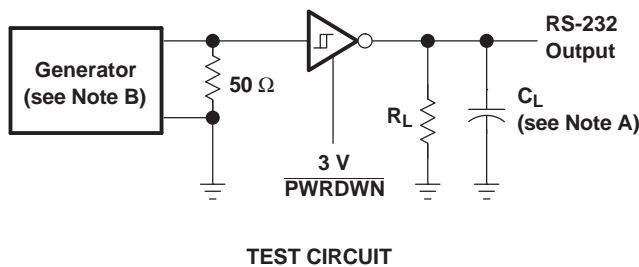
**PARAMETER MEASUREMENT INFORMATION**



$$SR(tr) = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$

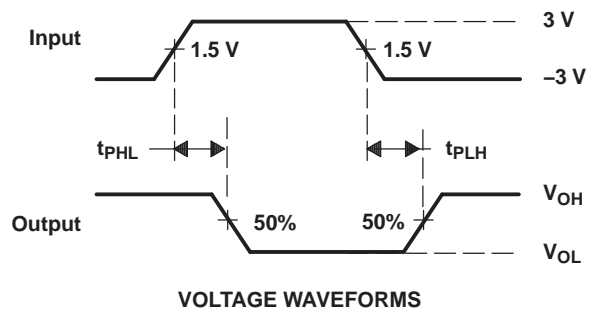
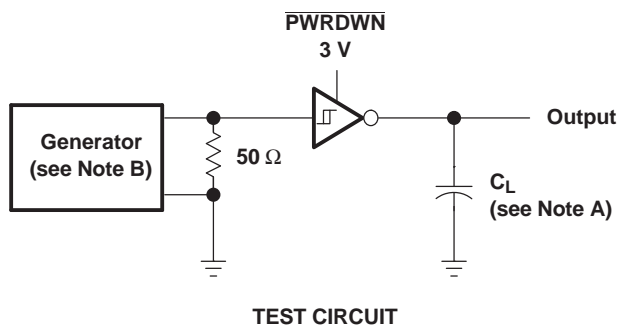
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

**Figure 1. Driver Slew Rate**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

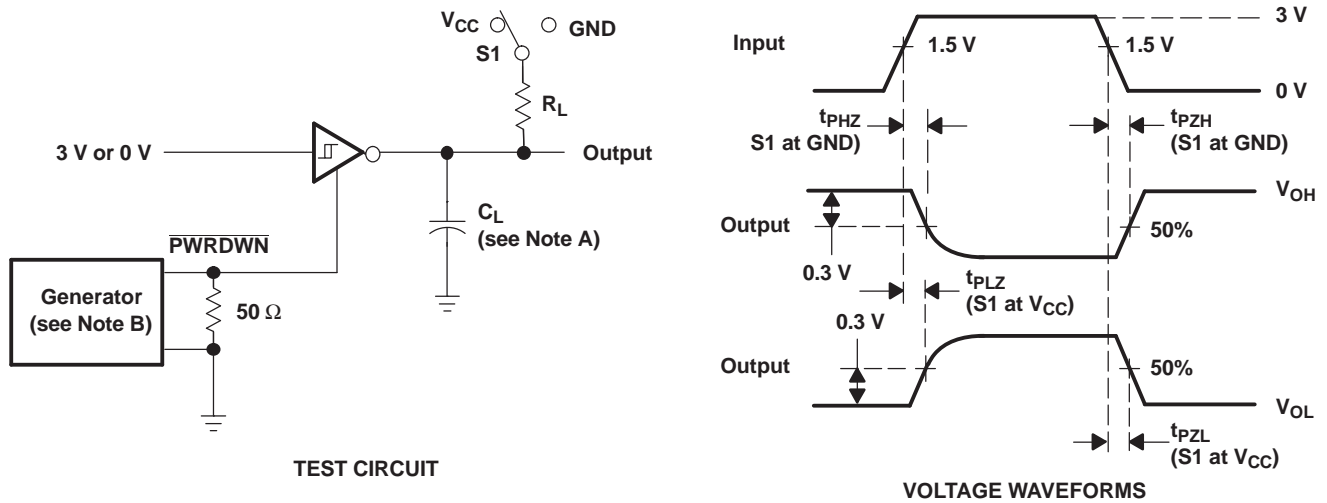
**Figure 2. Driver Pulse Skew**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

**Figure 3. Receiver Propagation Delay Times**

PARAMETER MEASUREMENT INFORMATION (Continued)



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

Figure 4. Receiver Enable and Disable Times

## REVISION HISTORY

Changes from Revision B (April 2009) to Revision C	Page
• Changed $V_L$ Pin for Compatibility With Mixed-Voltage Systems Down to 2.5 V (originally 1.8 V) on the Logic Side. ....	1
• Changed $V_L$ Supply MIN value from 1.65 V to 2.25 V. ....	4
• Deleted $V_L = 1.65V$ parameter from Input logic threshold low. ....	4
• Deleted $V_L = 1.95V$ parameter from Input logic threshold high. ....	4

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TRS3386ECDWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3386EC
TRS3386ECDWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3386EC
<a href="#">TRS3386ECPW</a>	Obsolete	Production	TSSOP (PW)   20	-	-	Call TI	Call TI	0 to 70	RV86EC
<a href="#">TRS3386ECPWR</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RV86EC
TRS3386ECPWR.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RV86EC
TRS3386ECPWRG4	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	RV86EC
<a href="#">TRS3386EIDWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3386EI
TRS3386EIDWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3386EI
<a href="#">TRS3386EIPW</a>	Obsolete	Production	TSSOP (PW)   20	-	-	Call TI	Call TI	-40 to 85	RV86EI
<a href="#">TRS3386EIPWR</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RV86EI
TRS3386EIPWR.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RV86EI

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

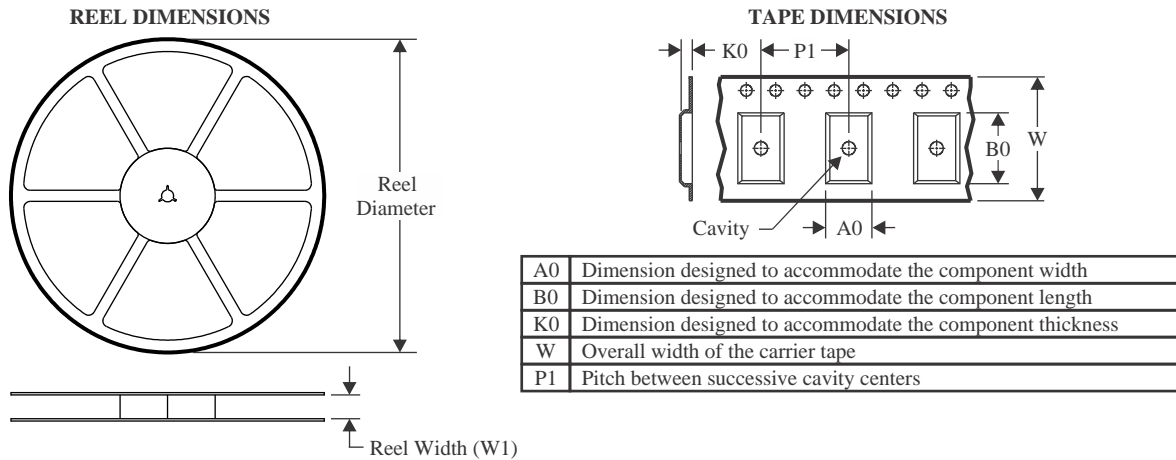
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3386ECDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TRS3386ECPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TRS3386EIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3386ECDWR	SOIC	DW	20	2000	356.0	356.0	45.0
TRS3386ECPWR	TSSOP	PW	20	2000	353.0	353.0	32.0
TRS3386EIPWR	TSSOP	PW	20	2000	353.0	353.0	32.0

# PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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