



**THE DATASHEET OF  
X4-0.6-0-SP**



# TPSI3052-Q1 Automotive Reinforced Isolated Switch Driver With Integrated 15V Gate Supply

## 1 Features

- No isolated secondary supply required
- Drives external power transistors or SCRs
- 5kV<sub>RMS</sub> reinforced isolation
- 15V gate drive with 1.5/3A peak source and sink current
- Up to 50mW supply for external auxiliary circuitry
- Supports AC or DC switching
- Supports two-wire or three-wire modes
- Seven levels of power transfer, resistor selectable
- **Functional Safety-Capable**
  - [Documentation available to aid functional safety system design](#)
- AEC Q-100 qualified for automotive applications:
  - Temperature grade 1: –40 to +125°C, T<sub>A</sub>
- Safety-Related Certifications
  - 7071V<sub>PK</sub> reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 5kV<sub>RMS</sub> isolation for 1 minute per UL 1577
- Long isolation lifetime
  - 30+ years at 1.2kV<sub>RMS</sub> or 1700V<sub>DC</sub>
  - 15+ years at 1.7kV<sub>RMS</sub> or 2400V<sub>DC</sub>

## 2 Applications

- [Solid state relay \(SSR\)](#)
- [Battery management system](#)
- [On-board charger](#)
- [Hybrid, electric, and powertrain system](#)
- [Building automation](#)
- [Factory automation and control](#)

## 3 Description

The TPSI3052-Q1 is a fully integrated, isolated switch driver, which when combined with an external power switch, forms a complete isolated solid state relay (SSR). With a nominal gate drive voltage of 15V with 1.5/3.0A peak source and sink current, select from a large variety of external power switches to meet a wide range of applications. The TPSI3052-Q1 generates its own secondary bias supply from the power received from its primary side, so no isolated secondary supply bias is required. Additionally, the TPSI3052-Q1 can optionally supply power to external supporting circuitry for various application needs.

The TPSI3052-Q1 supports two modes of operation based on the number of input pins required. In two-wire mode, typically found in driving mechanical relays, controlling the switch requires only two pins and supports a wide voltage range of operation from 6.5V to 48V. In three-wire mode, the primary supply from 3V to 5.5V is supplied externally, and the switch is controlled through a separate enable. Available in three-wire mode only, the TPSI3052S-Q1 features a one-shot enable for the switch control. This feature is useful for driving SCRs that typically require only one pulse of current to trigger.

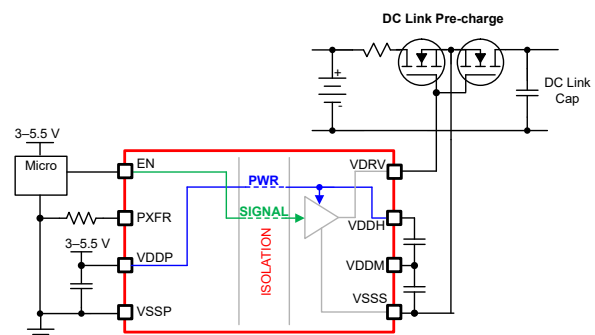
The secondary side provides a regulated, floating supply rail of 15V for driving a large variety of power switches with no need for a secondary bias supply. The application can drive single power switches for DC applications or dual, back-to-back power switches for AC applications, as well as various types of SCR. The TPSI3052-Q1 integrated isolation protection is robust with higher reliability, lower power consumption, and increased temperature ranges than traditional mechanical relays and optocouplers.

Adjust the power transfer of the TPSI3052-Q1 by selecting one of seven power level settings using an external resistor from the PXFR pin to VSSP. This action allows for tradeoffs in power dissipation versus power provided on the secondary depending on the needs of the application.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TPSI3052-Q1	SOIC 8-pin (DWZ)	7.50mm × 5.85mm
TPSI3052S-Q1		

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.

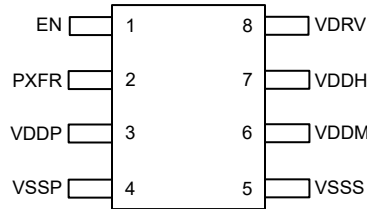


**TPSI3052-Q1 Simplified Schematic**

## Table of Contents

<b>1 Features</b> .....	1	7.1 Overview.....	18
<b>2 Applications</b> .....	1	7.2 Functional Block Diagram.....	18
<b>3 Description</b> .....	1	7.3 Feature Description.....	18
<b>4 Pin Configuration and Functions</b> .....	3	7.4 Device Functional Modes.....	25
<b>5 Specifications</b> .....	4	<b>8 Application and Implementation</b> .....	26
5.1 Absolute Maximum Ratings.....	4	8.1 Application Information.....	26
5.2 ESD Ratings.....	4	8.2 Typical Application.....	26
5.3 Recommended Operating Conditions.....	4	8.3 Power Supply Recommendations.....	34
5.4 Thermal Information.....	5	8.4 Layout.....	34
5.5 Power Ratings.....	5	<b>9 Device and Documentation Support</b> .....	38
5.6 Insulation Specifications.....	5	9.1 Receiving Notification of Documentation Updates... 38	
5.7 Safety-Related Certifications.....	6	9.2 Support Resources.....	38
5.8 Safety Limiting Values.....	7	9.3 Trademarks.....	38
5.9 Electrical Characteristics.....	7	9.4 Electrostatic Discharge Caution.....	38
5.10 Switching Characteristics.....	10	9.5 Glossary.....	38
5.11 Insulation Characteristic Curves.....	12	<b>10 Revision History</b> .....	38
5.12 Typical Characteristics.....	13	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	38
<b>6 Parameter Measurement Information</b> .....	16		
<b>7 Detailed Description</b> .....	18		

## 4 Pin Configuration and Functions



**Figure 4-1. TPSI3052-Q1, TPSI3052S-Q1 8-Pin SOIC Top View**

**Table 4-1. Pin Functions**

PIN		I/O	TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.			
EN	1	I	—	Active high driver enable
PXFR	2	I	—	Power transfer can be adjusted by selecting one of seven power level settings using an external resistor from the PXFR pin to VSSP. In three-wire mode, a given resistor setting sets the duty cycle of the power converter (see <a href="#">Table 7-1</a> ) and hence the amount of power transferred. In two-wire mode, a given resistor setting adjusts the current limit of the EN pin (see <a href="#">Table 7-2</a> ) and hence the amount of power transferred.
VDDH	7	—	P	Generated high supply
VDDM	6	—	P	Generated mid supply
VDDP	3	—	P	Power supply for primary side
VDRV	8	O	—	Active high driver output
VSSP	4	—	GND	Ground supply for primary side
VSSS	5	—	GND	Ground supply for secondary side

(1) P = power, GND = ground, NC = no connect

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER <sup>(1)</sup>		MIN	MAX	UNIT
Primary Side Supply <sup>(2)</sup>	VDDP	-0.3	6	V
Primary Side Supply <sup>(2)</sup>	EN	-0.3	60	V
Primary Side Supply <sup>(2)</sup>	PXFR	-0.3	60	V
Secondary Side Supply <sup>(3)</sup>	VDRV	-0.3	18	V
Secondary Side Supply <sup>(3)</sup>	VDDH	-0.3	18	V
Secondary Side Supply <sup>(3)</sup>	VDDM	-0.3	6	V
Secondary Side Supply <sup>(3)</sup>	VDDH-VDDM	-0.3	12	V
Junction temperature, T <sub>J</sub>	Junction temperature, T <sub>J</sub>	-40	150	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to VSSP.
- (3) All voltage values are with respect to VSSS.

### 5.2 ESD Ratings

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD classification level 2	±2000	V	
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C4B	Corner pins (1, 4, 5, and 8)		±750
			Other pins		±500

- (1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDP	Primary side supply voltage in three-wire mode <sup>(1)</sup>	3.0		5.5	V
EN	Enable in two-wire mode <sup>(1)</sup>	0		48.0	V
	Enable in three-wire mode <sup>(1)</sup>	0		5.5	V
PXFR	Power transfer control <sup>(1)</sup>	0		5.5	V
C <sub>VDDP</sub>	Decoupling capacitance on VDDP and VSSP, two-wire mode <sup>(2)</sup>	220		330	nF
	Decoupling capacitance on VDDP and VSSP, three-wire mode <sup>(2)</sup>	0.22		20	μF
C <sub>DIV1</sub> <sup>(3)</sup>	Decoupling capacitance across VDDH and VDDM <sup>(2)</sup>	0.004		15	μF
C <sub>DIV2</sub> <sup>(3)</sup>	Decoupling capacitances across VDDM and VSSS <sup>(2)</sup>	0.012		40	μF
T <sub>A</sub>	Ambient operating temperature	-40		125	°C

### 5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T <sub>J</sub>	Operating junction temperature	-40		150	°C
ΔV <sub>EN</sub> /Δt	EN rise and fall rates, two-wire mode.	65			V/ms

- (1) All voltage values are with respect to VSSP.
- (2) All capacitance values are absolute. Apply derating where necessary.
- (3) C<sub>DIV1</sub> and C<sub>DIV2</sub> must be of same type and tolerance. C<sub>DIV2</sub> capacitance value must be at least three times the capacitance value of C<sub>DIV1</sub>, for example, C<sub>DIV2</sub> ≥ 3 × C<sub>DIV1</sub>.

### 5.4 Thermal Information

THERMAL METRIC <sup>(1) (2)</sup>		DEVICE	UNIT
		DWZ(SOIC)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	89.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	40.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	45.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	10.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	44.4	°C/W

- (1) Estimate only.
- (2) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

### 5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P <sub>D</sub>	Maximum power dissipation, VDDP.	V <sub>VDDP</sub> = 5V, R <sub>PXFR</sub> = 20kΩ, three-wire mode, C <sub>VDRV</sub> = 100pF, C <sub>DIV1</sub> = 33nF, C <sub>DIV2</sub> = 100nF f <sub>EN</sub> = 1kHz square wave, V <sub>EN</sub> = 5V peak to peak.			250	mW
	Maximum power dissipation, EN.	R <sub>PXFR</sub> = 20kΩ, two-wire mode, C <sub>VDRV</sub> = 100pF, C <sub>DIV1</sub> = 33nF, C <sub>DIV2</sub> = 100nF f <sub>EN</sub> = 1kHz square wave, V <sub>EN</sub> = 48V peak to peak.k.			350	mW

### 5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFIC ACTION	UNIT
<b>CREEPAGE AND TRACKING</b>				
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	≥ 8.5	mm
CPG	External Creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	≥ 8.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	≥ 120	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 1000V <sub>RMS</sub>	I-III	
<b>DIN EN IEC 60747-17 (VDE 0884-17)</b>				

## 5.6 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	SPECIFIC ATION	UNIT
$V_{IORM}$	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	$V_{PK}$
$V_{IOWM}$	Maximum isolation working voltage	AC voltage (sine wave)	1000	$V_{RMS}$
		DC voltage	1414	$V_{DC}$
$V_{IOTM}$	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ ; $t = 60s$ (qualification test)	7070	$V_{PK}$
		$V_{TEST} = 1.2 \times V_{IOTM}$ ; $t = 1s$ (100% production test)	8484	$V_{PK}$
$V_{IMP}$	Maximum impulse voltage <sup>(3)</sup>	Tested in air; 1.2/50 $\mu$ s waveform per IEC 62638-1	9230	$V_{PK}$
$V_{IOSM}$	Maximum surge isolation voltage <sup>(3)</sup>	Tested in oil (qualification test); 1.2/50 $\mu$ s waveform per IEC 62638-1	12000	$V_{PK}$
$q_{pd}$	Apparent charge <sup>(4)</sup>	Method a: After input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60s$ ; $V_{pd(m)} = 1.2 \times V_{IORM}$ , $t_m = 10s$ .	$\leq 5$	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$ , $t_{ini} = 60s$ ; $V_{pd(m)} = 1.6 \times V_{IORM}$ , $t_m = 10s$ .	$\leq 5$	
		Method b1: At routine test (100% production test) and preconditioning (type test), $V_{ini} = V_{IOTM}$ , $t_{ini} = 1s$ ; $V_{pd(m)} = 1.875 \times V_{IORM}$ , $t_m = 1s$ .	$\leq 5$	
$C_{IO}$	Barrier capacitance, input to output <sup>(5)</sup>	$V_{IO} = 0.4 \times \sin(2\pi ft)$ , $f = 1MHz$	3	pF
$R_{IO}$	Insulation resistance, input to output <sup>(5)</sup>	$V_{IO} = 500V$ , $T_A = 25^\circ C$	$> 10^{12}$	$\Omega$
		$V_{IO} = 500V$ , $100^\circ C \leq T_A \leq 125^\circ C$	$> 10^{11}$	
		$V_{IO} = 500V$ at $T_S = 150^\circ C$	$> 10^9$	
	Pollution degree		2	
	Climatic category		40/125/21	
<b>UL 1577</b>				
$V_{ISO}$	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000V_{RMS}$ , $t = 60s$ (qualification test), $V_{TEST} = 1.2 \times V_{ISO} = 6000V_{RMS}$ , $t = 1s$ (100% production test)	5000	$V_{RMS}$

- Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
- Testing is carried out in air to determine the intrinsic surge immunity of the package.
- Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- Apparent charge is electrical discharge caused by a partial discharge (pd).
- All pins on each side of the barrier tied together creating a two-pin device.

## 5.7 Safety-Related Certifications

VDE	UL
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Recognized under UL 1577 Component Recognition Program
Reinforced insulation; Maximum transient isolation voltage, 7071 $V_{PK}$ ; Maximum repetitive peak isolation voltage, 1414 $V_{PK}$ ; Maximum surge isolation voltage, 12000 $V_{PK}$	Single protection, 5000 $V_{RMS}$
Certificate number: 40040142	File number: UL-US-2300613-0

## 5.8 Safety Limiting Values

PARAMETER <sup>(1) (2)</sup>		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Safety input, output, or supply current	R <sub>θJA</sub> = 89.3°C/W, V <sub>VDDP</sub> = 5.5V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, three-wire mode.			254	mA
		R <sub>θJA</sub> = 89.3°C/W, V <sub>EN</sub> = 24V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, two-wire mode.			58	
		R <sub>θJA</sub> = 89.3°C/W, V <sub>EN</sub> = 48V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C, two-wire mode.			29	
P <sub>S</sub>	Safety input, output, or total power	R <sub>θJA</sub> = 89.3°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C.			1.4	W
T <sub>S</sub>	Maximum safety temperature				150	°C

- (1) Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.
- (2) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

## 5.9 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). Typical at T<sub>A</sub> = 25°C. C<sub>VDDP</sub> = 220nF (two-wire mode), C<sub>VDDP</sub> = 1 μF (three-wire mode), C<sub>DIV1</sub> = 5.1nF, C<sub>DIV2</sub> = 15nF, C<sub>VDRV</sub> = 100pF, R<sub>PXFR</sub> = 7.32kΩ ±1%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>COMMON</b>						
V <sub>VDDP_UV_R</sub>	VDDP under-voltage threshold rising	VDDP rising	2.50	2.70	2.90	V
V <sub>VDDP_UV_F</sub>	VDDP under-voltage threshold falling	VDDP falling	2.35	2.55	2.75	V
V <sub>VDDP_UV_HYS</sub>	VDDP under-voltage threshold hysteresis			75		mV
V <sub>VDDH_UV_R</sub>	VDDH under-voltage threshold rising	VDDH rising.	12.5	13	13.4	V
V <sub>VDDH_UV_F</sub>	VDDH under-voltage threshold falling.	VDDH falling.	9.9	10.4	10.9	V
V <sub>VDDH_UV_HYS</sub>	VDDH under-voltage threshold hysteresis.			2.5		V
V <sub>VDDM_UV_R</sub>	VDDM under-voltage threshold rising	VDDM rising.	2.8	3.3	3.7	V
V <sub>VDDM_UV_F</sub>	VDDM under-voltage threshold falling	VDDM falling.	2.6	3	3.5	V
V <sub>VDDM_UV_HYS</sub>	VDDM under-voltage threshold hysteresis.			0.3		V
I <sub>Q_VDDH</sub>	Internal quiescent current of VDDH supply.			45		μA
R <sub>DSON_VDRV</sub>	Driver on resistance in low state.	Force V <sub>VDDH</sub> = 15V, sink I <sub>VDRV</sub> = 50mA.		1.7		Ω
	Driver on resistance in high state.	Force V <sub>VDDH</sub> = 15V, source I <sub>VDRV</sub> = 50mA.		2.5		Ω

## 5.9 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typicals at  $T_A = 25^\circ\text{C}$ .  $C_{VDDP} = 220\text{nF}$  (two-wire mode),  $C_{VDDP} = 1\ \mu\text{F}$  (three-wire mode),  $C_{DIV1} = 5.1\text{nF}$ ,  $C_{DIV2} = 15\text{nF}$ ,  $C_{VDRV} = 100\text{pF}$ ,  $R_{PXFR} = 7.32\text{k}\Omega \pm 1\%$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VDRV\_PEAK}$	VDRV peak output current during rise	$V_{VDDH}$ in steady state, transition EN low to high, measure peak current.		1.5		A
	VDRV peak output current during fall	$V_{VDDH}$ in steady state, transition EN high to low, measure peak current.		3		A
TSD	Temperature shutdown			173		$^\circ\text{C}$
TSDH	Temperature shutdown hysteresis			32		$^\circ\text{C}$
CMTI	Common-mode transient immunity	$ V_{CM}  = 1000\text{V}$	100			V/ns
<b>TWO-WIRE MODE</b>						
$V_{IH\_EN}$	Minimum voltage on EN to be detected as a valid logic high.		6.5			V
$V_{IL\_EN}$	Maximum voltage on EN to be detected as a valid logic low.				2.0	V
$I_{EN\_START}$	Enable current at startup	EN = 0V $\rightarrow$ 6.5V		27		mA
$I_{EN}$	Enable current steady state	EN = 6.5V, $R_{PXFR} = 7.32\text{k}\Omega$ , $R_{PXFR} \geq 100\text{k}\Omega$ or $R_{PXFR} \leq 1\text{k}\Omega$ , $V_{VDDH}$ in steady state.		1.9		mA
		EN = 6.5V, $R_{PXFR} = 20\text{k}\Omega$ , $V_{VDDH}$ in steady state.		6.8		mA
$V_{VDDP\_AVG}$	VDDP average voltage.	EN = 6.5V, $V_{VDDH}$ in steady state, measure average VDDP voltage.		4.5		V
$V_{VDDH}$	VDDH output voltage	EN = 6.5V, $V_{VDDH}$ in steady state.	13.9	15	16.2	V
$V_{VDRV\_H}$	VDRV output voltage driven high	EN = 6.5V, $V_{VDDH}$ in steady state, no DC loading.	13.9	15	16.2	V
$V_{VDRV\_L}$	VDRV output voltage driven low	EN = 6.5V $\rightarrow$ 0V, $V_{VDDH}$ in steady state, sink 10mA load.			0.1	V
$V_{VDDM\_IAUX}$	Average VDDM voltage when sourcing external current.	EN = 6.5V, steady state. $R_{PXFR} = 7.32\text{k}\Omega$ , $R_{PXFR} \geq 100\text{k}\Omega$ or $R_{PXFR} \leq 1\text{k}\Omega$ , $C_{DIV1} = 75\text{nF}$ , $C_{DIV2} = 220\text{nF}$ , source 0.20mA from VDDM, measure VDDM voltage.	4.6		5.5	V
	Average VDDM voltage when sourcing external current.	EN = 6.5V, steady state. $R_{PXFR} = 20\text{k}\Omega$ , $C_{DIV1} = 75\text{nF}$ , $C_{DIV2} = 220\text{nF}$ , source 1.2mA from VDDM, measure VDDM voltage.	4.6		5.5	V
<b>THREE-WIRE MODE</b>						
$V_{IH\_EN}$	Minimum voltage on EN to be detected as a valid logic high. $V_{IH(\min)} = 0.7 \times V_{VDDP}$	$V_{VDDP} = 3\text{V}$	2.1			V
		$V_{VDDP} = 5.5\text{V}$	3.85			V
$V_{IL\_EN}$	Maximum voltage on EN to be detected as a valid logic low.	$V_{VDDP} = 3\text{V}$			0.9	V
		$V_{VDDP} = 5.5\text{V}$			1.65	V

## 5.9 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typicals at  $T_A = 25^\circ\text{C}$ .  $C_{VDDP} = 220\text{nF}$  (two-wire mode),  $C_{VDDP} = 1\ \mu\text{F}$  (three-wire mode),  $C_{DIV1} = 5.1\text{nF}$ ,  $C_{DIV2} = 15\text{nF}$ ,  $C_{VDRV} = 100\text{pF}$ ,  $R_{PXFR} = 7.32\text{k}\Omega \pm 1\%$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VDDP}$	VDDP average current in steady state	EN = 3.3V, $V_{VDDP} = 3.3\text{V}$ , $R_{PXFR} = 7.32\text{k}\Omega$ , $R_{PXFR} \geq 100\text{k}\Omega$ or $R_{PXFR} \leq 1\text{k}\Omega$ , $C_{VDDP} = 10\ \mu\text{F}$ , $V_{VDDH}$ in steady state, measure $I_{VDDP}$ .		3.1		mA
		EN = 3.3V, $V_{VDDP} = 3.3\text{V}$ , $R_{PXFR} = 20\text{k}\Omega$ , $C_{VDDP} = 10\ \mu\text{F}$ , $V_{VDDH}$ in steady state, measure $I_{VDDP}$ .		26		
		EN = 5V, $V_{VDDP} = 5\text{V}$ , $R_{PXFR} = 7.32\text{k}\Omega$ , $R_{PXFR} \geq 100\text{k}\Omega$ or $R_{PXFR} \leq 1\text{k}\Omega$ , $C_{VDDP} = 10\ \mu\text{F}$ , $V_{VDDH}$ in steady state, measure $I_{VDDP}$ .		4.8		mA
		EN = 5V, $V_{VDDP} = 5\text{V}$ , $R_{PXFR} = 20\text{k}\Omega$ , $C_{VDDP} = 10\ \mu\text{F}$ , $V_{VDDH}$ in steady state, measure $I_{VDDP}$ .		37		
$V_{VDDM\_IAUX}$	Average VDDM voltage when sourcing external current.	$V_{VDDP} = 3.3\text{V}$ , EN = 0.0V, steady state. $R_{PXFR} = 7.32\text{k}\Omega$ , $C_{DIV1} = 75\text{nF}$ , $C_{DIV2} = 220\text{nF}$ , Source 0.35mA from VDDM measure $V_{VDDM}$ .	4.6		5.5	V
$V_{VDDM\_IAUX}$	Average VDDM voltage when sourcing external current.	$V_{VDDP} = 5.0\text{V}$ , EN = 0.0V, steady state. $R_{PXFR} = 7.32\text{k}\Omega$ , $C_{DIV1} = 75\text{nF}$ , $C_{DIV2} = 220\text{nF}$ , Source 0.50mA from VDDM measure $V_{VDDM}$ .	4.6		5.5	V
$V_{VDDM\_IAUX}$	Average VDDM voltage when sourcing external current.	$V_{VDDP} = 3.3\text{V}$ , EN = 0.0V, steady state. $R_{PXFR} = 20\text{k}\Omega$ $C_{DIV1} = 75\text{nF}$ , $C_{DIV2} = 220\text{nF}$ , Source 3.0mA from VDDM measure $V_{VDDM}$ .	4.6		5.5	V
$V_{VDDM\_IAUX}$	Average VDDM voltage when sourcing external current.	$V_{VDDP} = 5.0\text{V}$ , EN = 0.0V, steady state. $R_{PXFR} = 20\text{k}\Omega$ $C_{DIV1} = 75\text{nF}$ $C_{DIV2} = 220\text{nF}$ Source 5.0mA from VDDM measure $V_{VDDM}$ .	4.6		5.5	V

## 5.9 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typical at  $T_A = 25^\circ\text{C}$ .  $C_{VDDP} = 220\text{nF}$  (two-wire mode),  $C_{VDDP} = 1\ \mu\text{F}$  (three-wire mode),  $C_{DIV1} = 5.1\text{nF}$ ,  $C_{DIV2} = 15\text{nF}$ ,  $C_{VDRV} = 100\text{pF}$ ,  $R_{PXFER} = 7.32\text{k}\Omega \pm 1\%$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VDDH}$	VDDH output voltage	$V_{VDDP} = 3.0\text{V}$ , $EN = 3.0\text{V}$ , $V_{VDDH}$ in steady state.	13.9	15	16.2	V
$V_{VDRV\_H}$	VDRV output voltage driven high	$V_{VDDP} = 3.0\text{V}$ , $EN = 3.0\text{V}$ , $V_{VDDH}$ in steady state, no DC loading.	13.9	15	16.2	V
$V_{VDRV\_L}$	VDRV output voltage driven low	$V_{VDDP} = 3.0\text{V}$ , $EN = 0\text{V}$ , $V_{VDDH}$ in steady state, VDRV sinking 10mA.			0.1	V

## 5.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). Typical at  $T_A = 25^\circ\text{C}$ .  $C_{VDDP} = 220\text{nF}$  (two-wire mode),  $C_{VDDP} = 1\ \mu\text{F}$  (three-wire mode),  $C_{DIV1} = 5.1\text{nF}$ ,  $C_{DIV2} = 15\text{nF}$ ,  $C_{VDRV} = 100\text{pF}$ ,  $R_{PXFER} = 7.32\text{k}\Omega \pm 1\%$

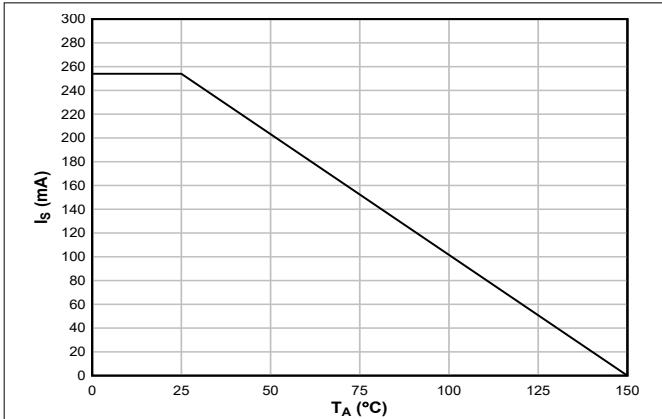
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TWO-WIRE MODE</b>						
$t_{LO\_EN}$	Low time of EN.		5			$\mu\text{s}$
$t_{LH\_VDDH}$	Propagation delay time from EN rising to VDDH at 50% level.	$EN = 0\text{V} \rightarrow 6.5\text{V}$ , $V_{VDDH} = 7.5\text{V}$ .		165		$\mu\text{s}$
$t_{LH\_VDRV}$	Propagation delay time from EN rising to VDRV at 90% level.	$EN = 0\text{V} \rightarrow 6.5\text{V}$ , $V_{VDRV} = 13.5\text{V}$ .		185		$\mu\text{s}$
$t_{HL\_VDRV}$	Propagation delay time from EN falling to VDRV at 10% level.	$EN = 6.5\text{V} \rightarrow 0\text{V}$ , $V_{VDRV} = 1.5\text{V}$ .		2.4	3	$\mu\text{s}$
$t_{R\_VDRV}$	VDRV rise time from EN rising to VDRV from 15% to 85% level.	$EN = 0\text{V} \rightarrow 6.5\text{V}$ , $V_{VDRV} = 2.25\text{V}$ to $12.75\text{V}$ .		6		ns
$t_{F\_VDRV}$	VDRV fall time from EN falling to VDRV from 85% to 15% level.	$EN = 6.5\text{V} \rightarrow 0\text{V}$ , $V_{VDRV} = 12.75\text{V}$ to $2.25\text{V}$ .		5		ns
<b>THREE-WIRE MODE</b>						
$t_{LO\_EN}$	Low time of EN.	$V_{VDDP} = 3.3\text{V}$ , $V_{VDDH} = \text{steady state}$ .	5			$\mu\text{s}$
$t_{HI\_EN}$	High time of EN.	$V_{VDDP} = 3.3\text{V}$ , $V_{VDDH} = \text{steady state}$ .	5			$\mu\text{s}$
$t_{HI\_VDRV}$	High time of VDRV in one-shot enable mode. TPSI3052S-Q1 only. One-shot enable only available in three-wire mode.	$V_{VDDP} = 3.3\text{V}$ , steady state.		2.5		$\mu\text{s}$
$t_{LH\_VDDH}$	Propagation delay time from VDDP rising to VDDH at 50% level.	$EN = 0\text{V}$ , $V_{VDDP} = 0\text{V} \rightarrow 3.3\text{V}$ at $1\text{V}/\mu\text{s}$ , $V_{VDDH} = 7.5\text{V}$ , $C_{DIV1} = 3.3\text{nF}$ , $C_{DIV2} = 220\text{nF}$ .		85		$\mu\text{s}$
$t_{LH\_VDRV}$	Propagation delay time from EN rising to VDRV at 90% level	$V_{VDDP} = 3.3\text{V}$ , $V_{VDDH}$ steady state, $EN = 0\text{V} \rightarrow 3.3\text{V}$ , $V_{VDRV} = 13.5\text{V}$ .		3	4.5	$\mu\text{s}$
$t_{HL\_VDRV}$	Propagation delay time from EN falling to VDRV at 10% level	$V_{VDDP} = 3.3\text{V}$ , $V_{VDDH}$ steady state, $EN = 3.3\text{V} \rightarrow 0\text{V}$ , $V_{VDRV} = 1.5\text{V}$ .		2.5	3	$\mu\text{s}$
$t_{HL\_VDRV\_PD}$	Propagation delay time from VDDP falling to VDRV at 10% level. Timeout mechanism due to loss of power on primary supply.	$EN = 3.3\text{V}$ , $V_{VDDP} = 3.3\text{V} \rightarrow 0\text{V}$ at $-1\text{V}/\mu\text{s}$ , $V_{VDRV} = 1.5\text{V}$ .		300		$\mu\text{s}$

## 5.10 Switching Characteristics (continued)

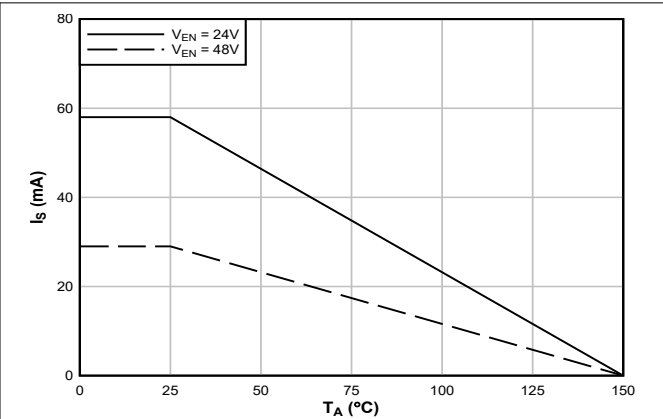
over operating free-air temperature range (unless otherwise noted). Typical at  $T_A = 25^\circ\text{C}$ .  $C_{VDDP} = 220\text{nF}$  (two-wire mode),  $C_{VDDP} = 1\ \mu\text{F}$  (three-wire mode),  $C_{DIV1} = 5.1\text{nF}$ ,  $C_{DIV2} = 15\text{nF}$ ,  $C_{VDRV} = 100\text{pF}$ ,  $R_{PXFER} = 7.32\text{k}\Omega \pm 1\%$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{R\_VDRV}$	VDRV rise time from EN rising to VDRV from 15% to 85% level	$V_{VDDP} = 3.3\text{V}$ , $V_{VDDH}$ steady state, EN = 0V → 3.3V, $V_{VDRV} = 2.25\text{V}$ to 12.75V.		6		ns
$t_{F\_VDRV}$	VDRV fall time from EN falling to VDRV from 85% to 15% level	$V_{VDDP} = 3.3\text{V}$ , $V_{VDDH}$ steady state, EN = 3.3V → 0V, $V_{VDRV} = 12.75\text{V}$ to 2.25V.		5		ns

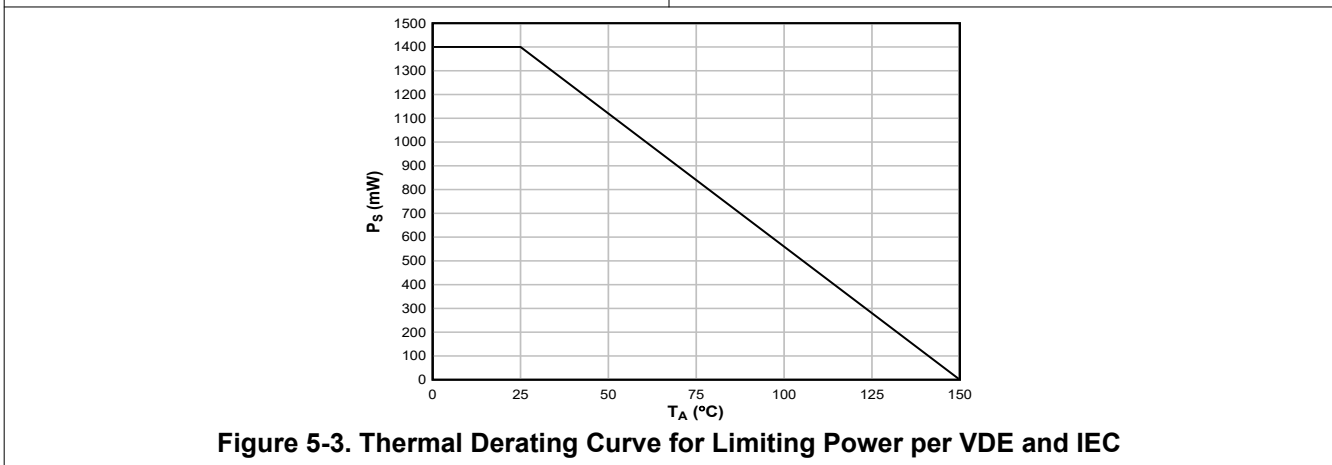
### 5.11 Insulation Characteristic Curves



**Figure 5-1. Thermal Derating Curve for Limiting Current per VDE and IEC, Three-Wire Mode**

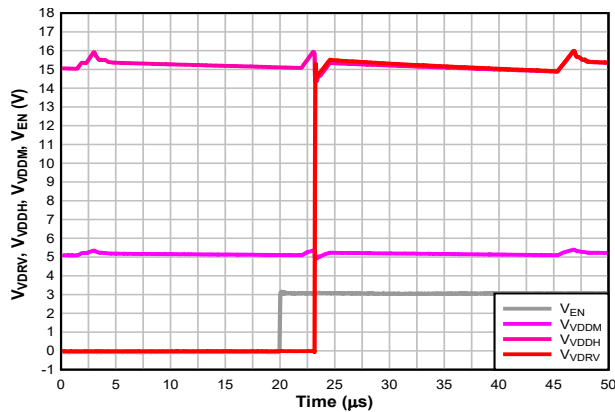


**Figure 5-2. Thermal Derating Curve for Limiting Current per VDE and IEC, Two-Wire Mode**



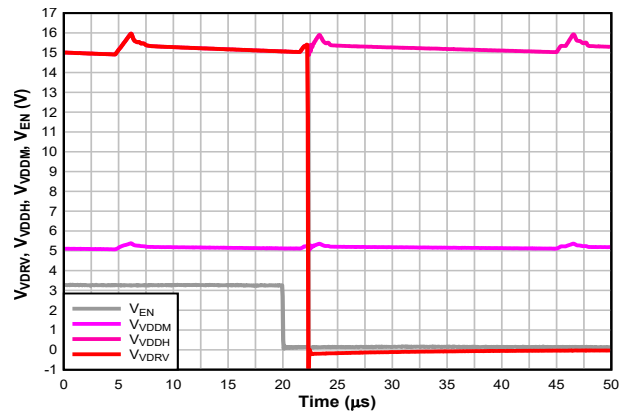
**Figure 5-3. Thermal Derating Curve for Limiting Power per VDE and IEC**

## 5.12 Typical Characteristics



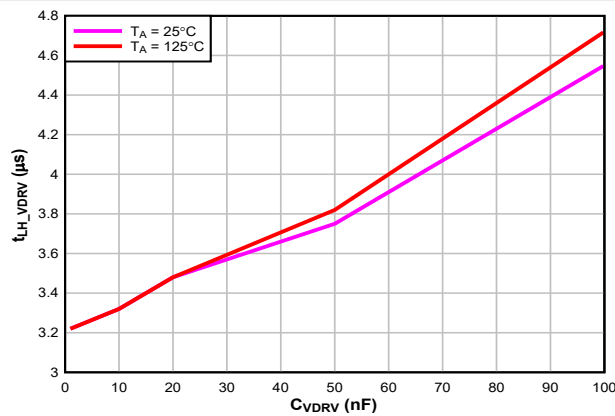
Three-wire mode    VDDP = 5.0V    R<sub>PXFR</sub> = 7.32kΩ  
 C<sub>DIV1</sub> = 5.1nF    C<sub>VDRV</sub> = 100pF    T<sub>A</sub> = 25°C  
 C<sub>DIV2</sub> = 15nF    C<sub>VDDP</sub> = 1µF    I<sub>AUX</sub> = 0mA

**Figure 5-4. t<sub>LH\_VDRV</sub>, Three-Wire Mode**



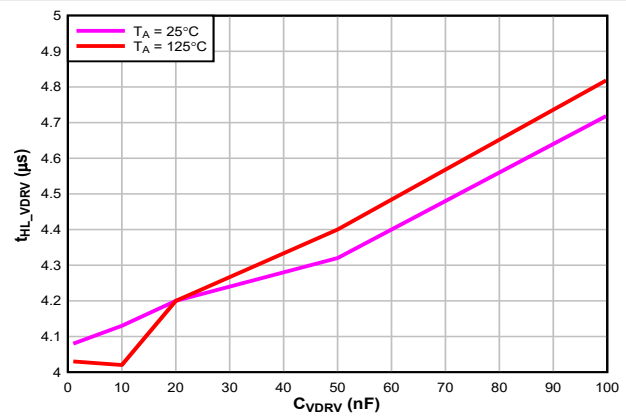
Three-wire mode    VDDP = 5.0V    R<sub>PXFR</sub> = 7.32kΩ  
 C<sub>DIV1</sub> = 5.1nF    C<sub>VDRV</sub> = 100pF    T<sub>A</sub> = 25°C  
 C<sub>DIV2</sub> = 15nF    C<sub>VDDP</sub> = 1µF    I<sub>AUX</sub> = 0mA

**Figure 5-5. t<sub>HL\_VDRV</sub>, Three-Wire Mode**



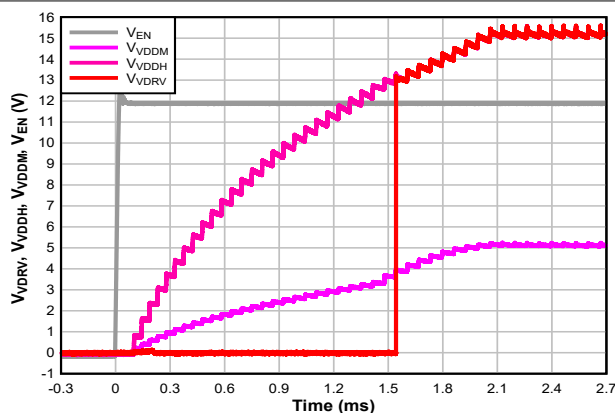
Three-wire mode    VDDP = 3.3V    R<sub>PXFR</sub> = 7.32kΩ  
 C<sub>DIV1</sub> = 2.2µF    C<sub>DIV2</sub> = 2.2µF

**Figure 5-6. t<sub>LH\_VDRV</sub> versus C<sub>VDRV</sub>**



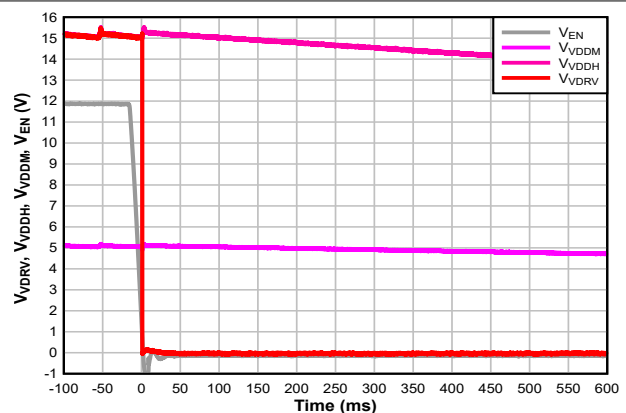
Three-wire mode    VDDP = 3.3V    R<sub>PXFR</sub> = 7.32kΩ  
 C<sub>DIV1</sub> = 2.2µF    C<sub>DIV2</sub> = 2.2µF

**Figure 5-7. t<sub>HL\_VDRV</sub> versus C<sub>VDRV</sub>**



Two-wire mode    EN = 12V    R<sub>PXFR</sub> = 7.32kΩ  
 C<sub>DIV1</sub> = 33nF    C<sub>VDRV</sub> = 100pF    T<sub>A</sub> = 25°C  
 C<sub>DIV2</sub> = 100nF    C<sub>VDDP</sub> = 220nF    I<sub>AUX</sub> = 0mA

**Figure 5-8. t<sub>LH\_VDRV</sub>, Two-Wire Mode**



Two-wire mode    EN = 12V    R<sub>PXFR</sub> = 7.32kΩ  
 C<sub>DIV1</sub> = 33nF    C<sub>VDRV</sub> = 100pF    T<sub>A</sub> = 25°C  
 C<sub>DIV2</sub> = 100nF    C<sub>VDDP</sub> = 220nF    I<sub>AUX</sub> = 0mA

**Figure 5-9. t<sub>HL\_VDRV</sub>, Two-Wire Mode**

### 5.12 Typical Characteristics (continued)

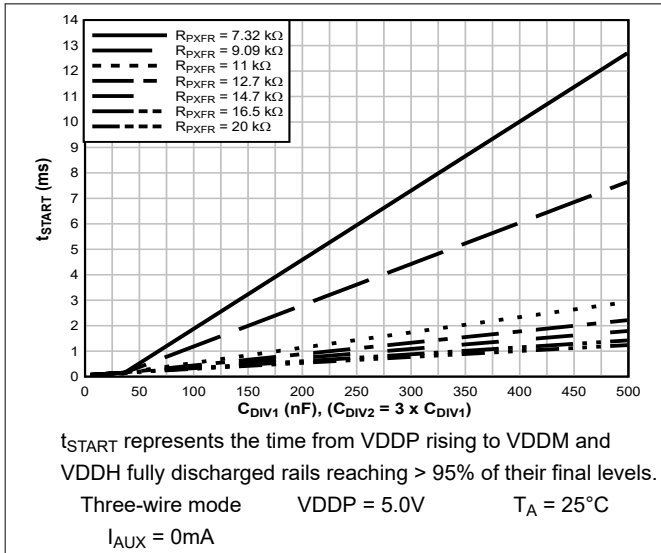


Figure 5-10.  $t_{START}$  versus  $C_{DIV1}$ ,  $C_{DIV2}$

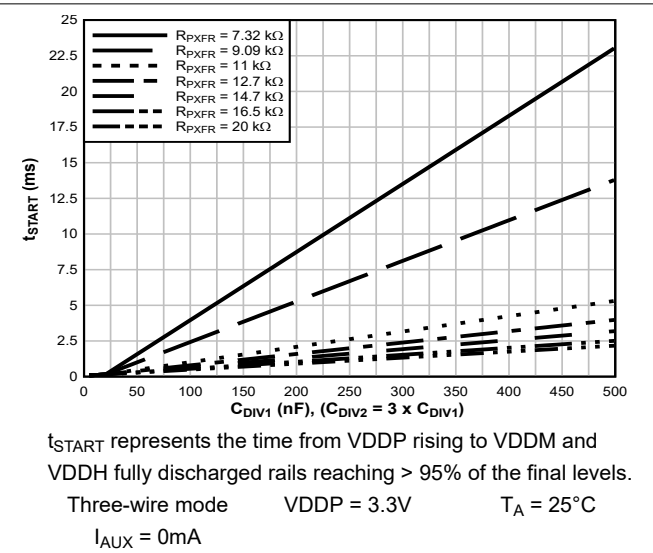


Figure 5-11.  $t_{START}$  versus  $C_{DIV1}$ ,  $C_{DIV2}$

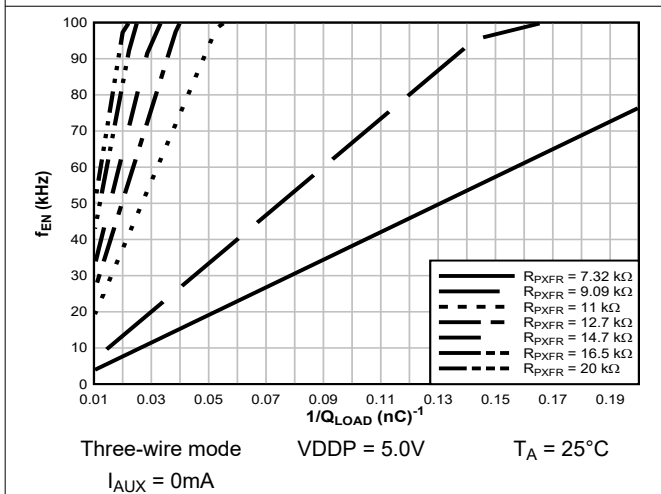


Figure 5-12. Max.  $f_{EN}$  versus  $Q_{LOAD} = 10\text{nC}$  to  $100\text{nC}$

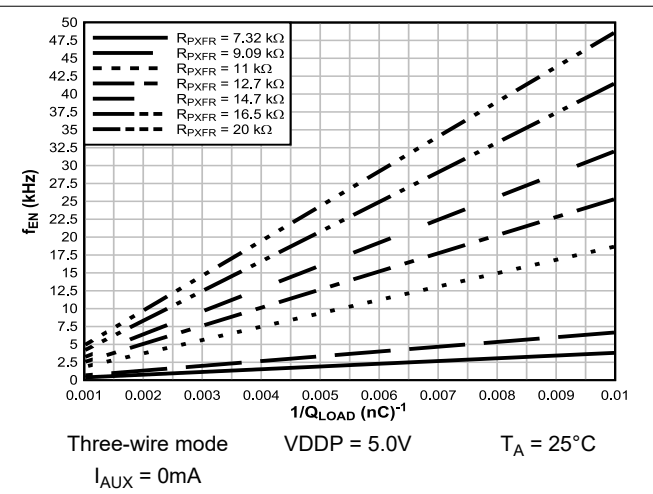
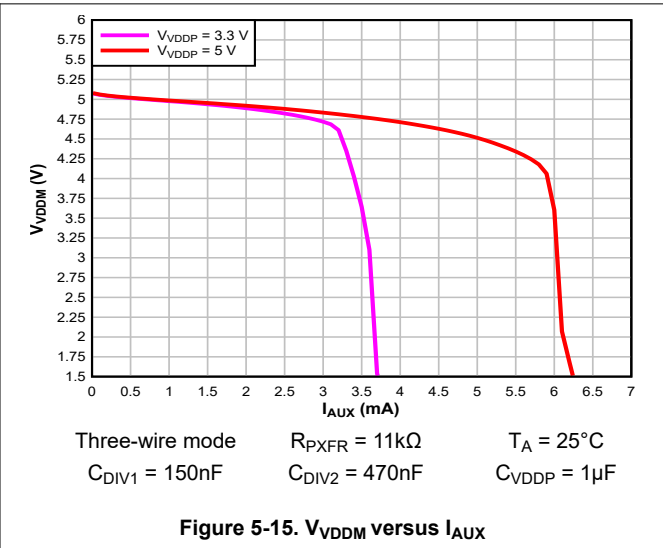
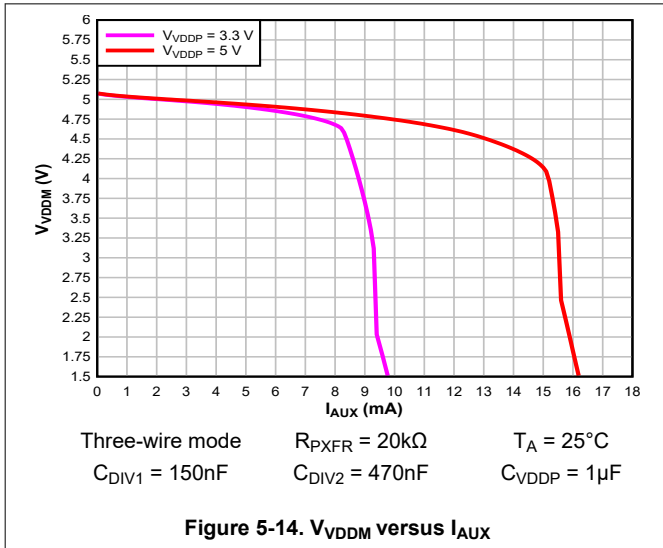


Figure 5-13. Max.  $f_{EN}$  versus  $Q_{LOAD} = 100\text{nC}$  to  $1000\text{nC}$

### 5.12 Typical Characteristics (continued)



## 6 Parameter Measurement Information

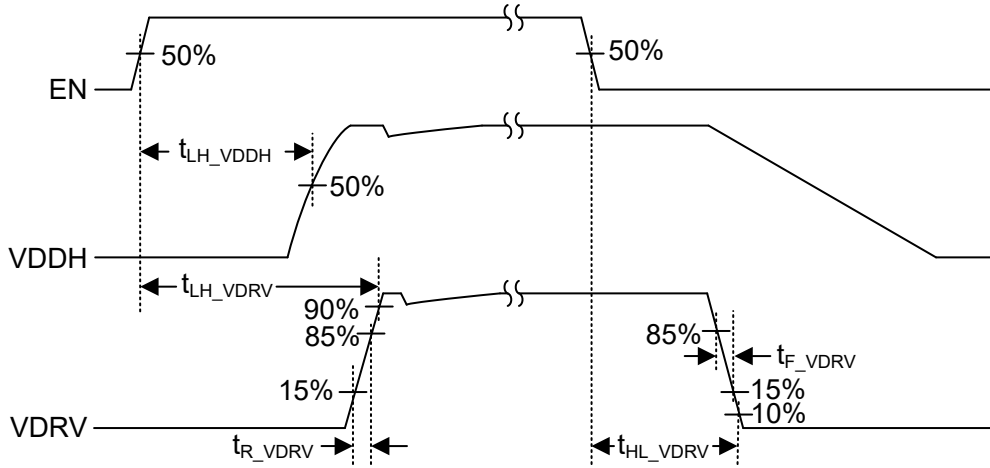


Figure 6-1. Two-Wire Mode Timing, Standard Enable (TPSI3052-Q1 Only)

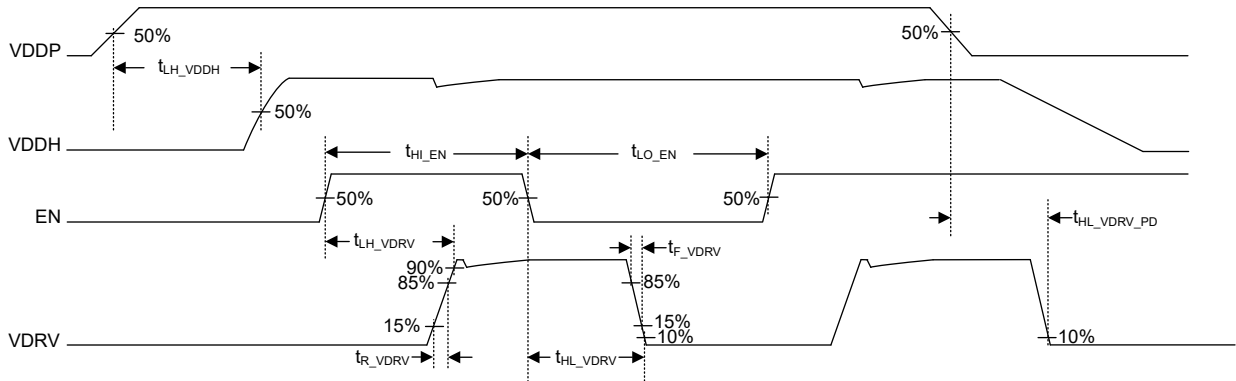


Figure 6-2. Three-Wire Mode Timing, Standard Enable (TPSI3052-Q1 Only)

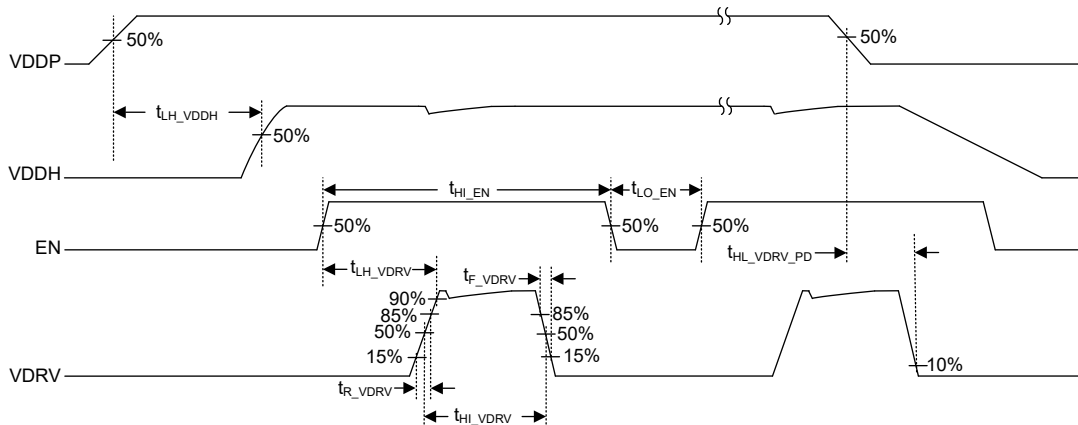
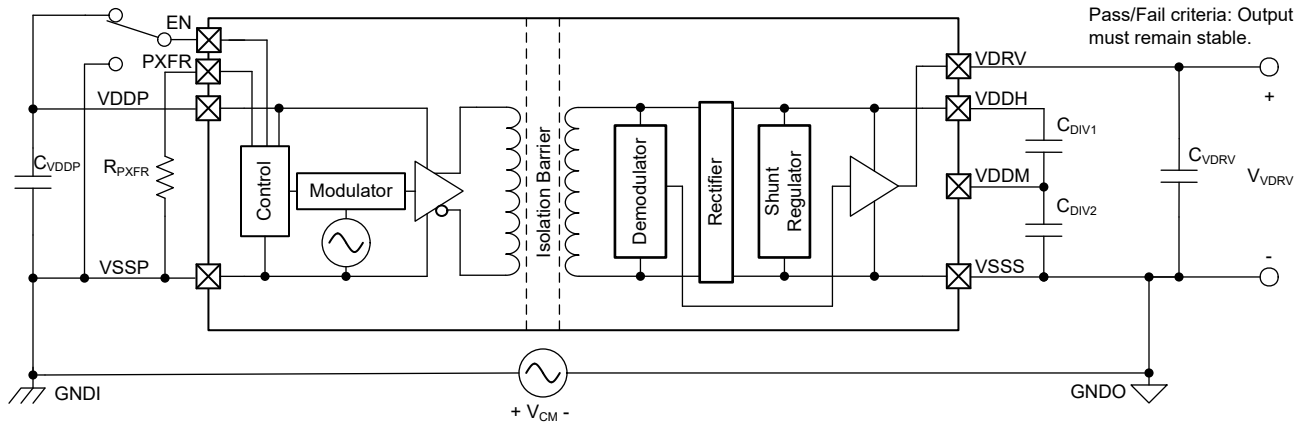


Figure 6-3. Three-Wire Mode Timing, One-Shot Enable (TPSI3052S-Q1 Only)



**Figure 6-4. Common-Mode Transient Immunity Test Circuit**

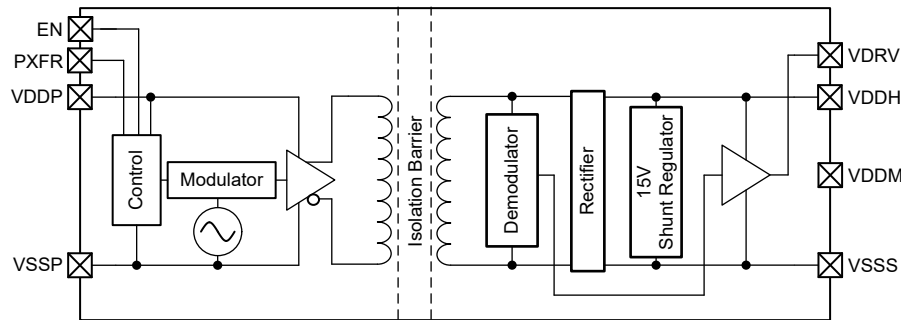
## 7 Detailed Description

### 7.1 Overview

The TPSI3052-Q1 is a fully integrated, reinforced isolated power switch driver, which when combined with an external power switch, forms a complete isolated Solid State Relay (SSR). With a nominal gate drive voltage of 15V and 1.5/3.0A peak source and sink current, select from a large variety of external power switches to meet a wide range of applications. The TPSI3052-Q1 generates its own secondary supply from the power received from its primary side, so no isolated secondary bias supply is required.

The [Functional Block Diagram](#) shows the primary side that includes a transmitter that drives an alternating current into the primary winding of an integrated transformer at a rate determined by the setting of the PXFR pin and the logic state of the EN pin. The transmitter operates at high frequency to drive the transformer to peak efficiency. In addition, the transmitter uses spread spectrum techniques to improve EMI performance, allowing many applications to achieve CISPR 25 - Class 5. During transmission, data information transfers to the secondary side alongside with the power. On the secondary side, the voltage induced on the secondary winding of the transformer is rectified, and the shunt regulator regulates the output voltage level of VDDH. Lastly, the demodulator decodes the received data information and drives VDRV high or low based on the logic state of the EN pin.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 Transmission of the Enable State

The TPSI3052-Q1 and TPSI3052S-Q1 use a modulation scheme to transmit the switch enable state information across the isolation barrier. The transmitter modulates the EN signal with an internally generated, high frequency carrier (89MHz typical), and differentially drives the primary winding of the isolation transformer. The receiver on the secondary side demodulates the received signal and asserts VDRV high or low, based on the data received.

#### 7.3.2 Power Transmission

The TPSI3052-Q1 and TPSI3052S-Q1 do not use an isolated supply for power. The secondary side power is obtained by the transferring of the primary side input power across the isolation transformer. The modulation scheme uses spread spectrum of the high frequency carrier (89MHz typical) to improve EMI performance assisting applications in meeting the CISPR 25 Class 5 standards.

#### 7.3.3 Gate Driver

The TPSI3052-Q1 and TPSI3052S-Q1 have an integrated gate driver that provides a nominal 15V gate voltage with 1.5/3.0A peak source and sink current sufficient for driving many power transistors or silicon-controlled rectifiers (SCR). When driving external power transistors, TI recommends bypass capacitors ( $C_{DIV2} = 3 \times C_{DIV1}$ ) from VDDH to VDDM and VDDM to VSSS of 20 times the equivalent gate capacitance.

The gate driver also includes an active clamp keep off circuit. This feature helps to keep the driver output, VDRV, low. For example, if power is lost on the secondary supply rails, power loss on the VDDP supply prevents power transfer. If power is lost, the active clamp keep off circuit attempts to clamp the voltage of VDRV to under 2V, relative to VSSS.

### 7.3.4 Modes Overview

The TPSI3052-Q1 and TPSI3052S-Q1 have two modes of operation: two-wire mode and three-wire mode.

In two-wire mode, the power on the primary side is provided directly by the EN pin. Setting EN high causes power transfer to the secondary side. As power transfers, the secondary rails, VDDM and VDDH, begin to rise. After sufficient power is available on the secondary side, VDRV is asserted high. Setting EN low causes VDRV to assert low and halts power transfer to the secondary side.

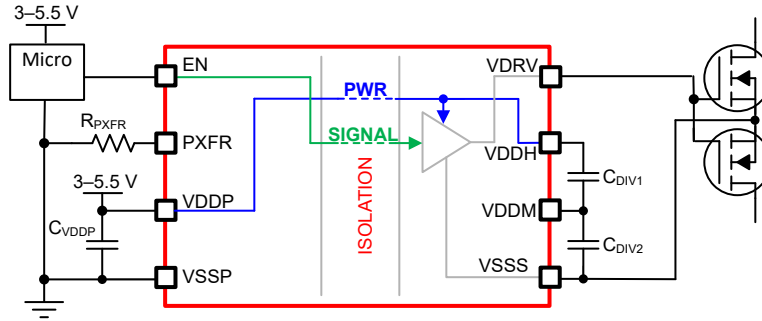
In three-wire mode, the power on the primary side is provided by a dedicated, low output impedance supply connected to VDDP. In this case, power transfer is independent from the enable state. If VDDP power is present, power is transferred from the primary side to the secondary side regardless of the EN state. In steady state conditions, when sufficient power is available on the secondary side, setting EN high causes VDRV to assert high. Setting EN low causes VDRV to assert low.

In standard enable, available only on the TPSI3052-Q1, VDRV follows the state of the EN pin and is used in most load switch applications. In one-shot enable mode, available only on the TPSI3052S-Q1 in three-wire mode, when a rising transition occurs on EN, VDRV is asserted high momentarily and then automatically asserted low, forming a one-shot pulse on VDRV. This event is useful for driving SCR devices that require only one burst of power to trigger. To re-trigger VDRV, EN must first transition low, followed by another rising transition.

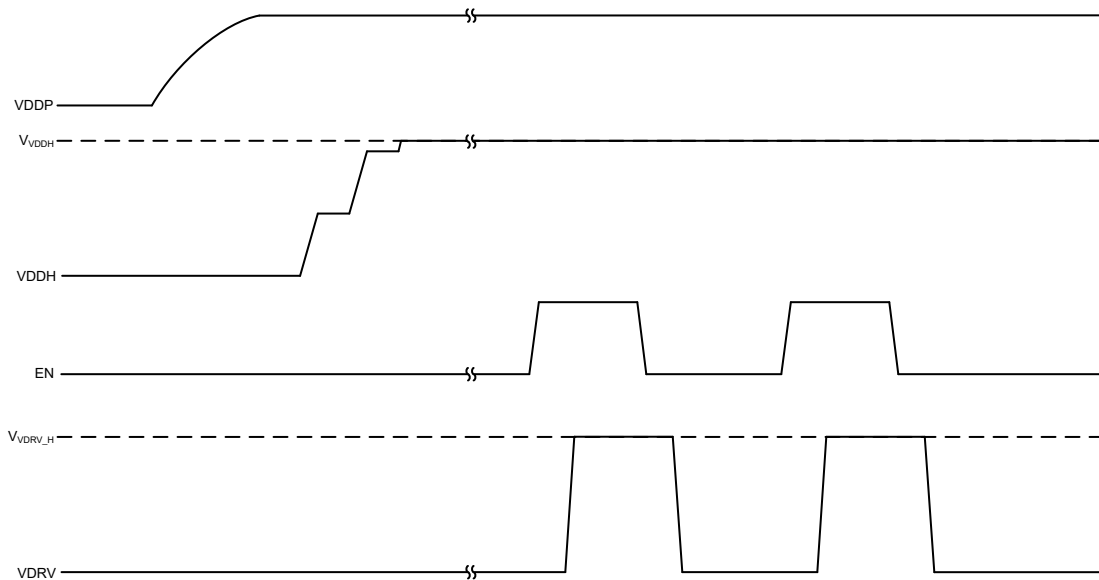
### 7.3.5 Three-Wire Mode

Three-wire mode is used for applications that require higher levels of power transfer or the shortest propagation delay TPSI3052-Q1 can offer. VDDP is supplied independently from the EN pin by a low output impedance external supply that can deliver the required power. In this mode, power from the primary side to the secondary side always occurs regardless of the state of the EN pin. Setting the EN pin logic high or low asserts or de-asserts VDRV, thereby enabling or disabling the external switch, respectively. [Figure 7-1](#) shows the basic setup required for three-wire mode operation which requires EN, VDDP, and VSSP signals. EN can be driven up to 5.5V which is normally driven from the circuitry residing on the same rail as VDDP. In this example, the TPSI3052-Q1 drives back-to-back MOSFETs in a common-source configuration.  $C_{VDDP}$  provides the required decoupling capacitance for the VDDP supply rail of the device.  $C_{DIV1}$  and  $C_{DIV2}$  provide the required decoupling capacitances of the VDDH and VDDM supply rails that provide the peak current to drive the external MOSFETs.

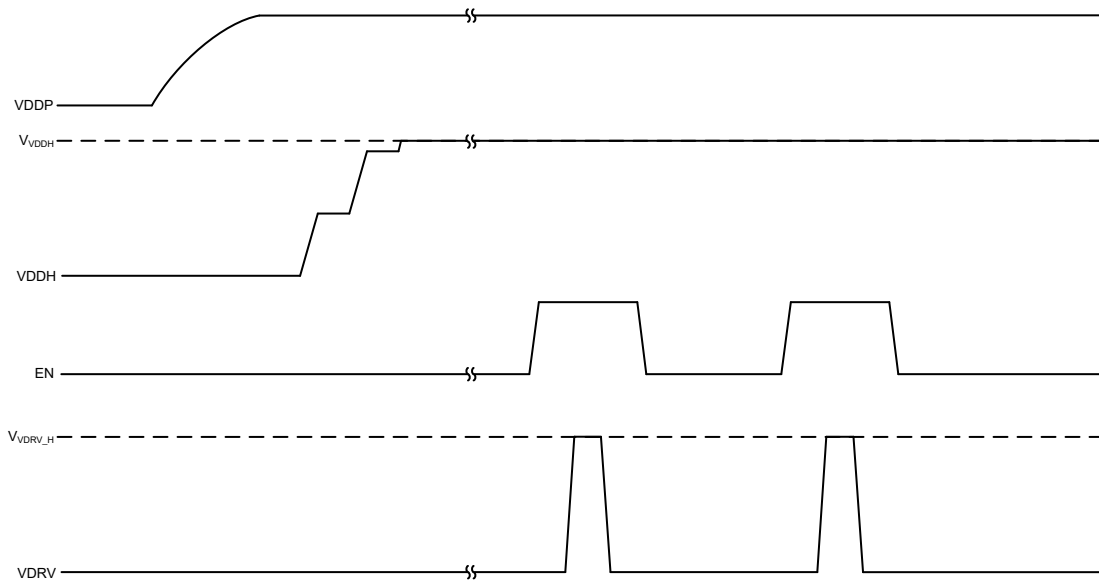
[Figure 7-2](#) and [Figure 7-3](#) show the basic operation from start-up to steady-state conditions. [Figure 7-2](#) shows operation using standard enable of the TPSI3052-Q1. After power up, the TPSI3052-Q1 begins to transfer power from VDDP to the secondary side for a fixed time period (25 $\mu$ s typical) at a duty cycle rate determined by  $R_{PXFER}$ , which begins to charge the VDDH (and VDDM) secondary side rails. Power transfer continues as long as VDDP is present. The time required to fully charge VDDH depends on several factors including the values of VDDP,  $C_{DIV1}$ ,  $C_{DIV2}$ ,  $R_{PXFER}$ , and the overall power transfer efficiency. When the application drives the EN pin to a logic high, the TPSI3052-Q1 signals information from the primary side to the secondary side to assert VDRV and drive it high. Similarly, setting EN pin to a logic low causes VDRV to drive low. [Figure 7-3](#) shows operation using one-shot enable of the TPSI3052S-Q1. The start-up behavior is identical. In one-shot enable, when the application drives the EN pin to a logic high, VDRV is asserted high ( $t_{HI\_VDRV}$ ), then is automatically asserted low by the TPSI3052S-Q1. To assert VDRV high again, the EN pin must transition low first, followed by a transition high.



**Figure 7-1. Three-Wire Mode Simplified Schematic**



**Figure 7-2. Three-Wire Mode with TPSI3052-Q1 (Standard Enable)**



**Figure 7-3. Three-Wire Mode with TPSI3052S-Q1 (One-shot Enable)**

To reduce average power, the TPSI3052-Q1 transfers power from the primary side to the secondary side in a burst fashion. The period of the burst is fixed while the burst on time is programmable by selecting one of seven appropriate resistor values,  $R_{PXFR}$ , from the PXFR to VSSP pins, thereby changing the duty cycle of the power converter. This action provides flexibility in the application, allowing tradeoffs in power consumed versus power delivered. Higher power converter settings increase the burst on time which, in turn, increases average power consumed from the VDDP supply and increases the amount of power transferred to the secondary side VDDH and VDDM supplies. Similarly, lower power converter settings decrease the burst on time which, in turn, decreases average power consumed from the VDDP supply and decreases the amount of power transferred to the secondary side.

Table 7-1 summarizes the three-wire mode power transfer selection.

**Table 7-1. Three-Wire Mode Power Transfer Selection**

$R_{PXFR}$ (1) (2)	Power Converter Duty Cycle (Three-Wire Mode, Nominal)	Description
7.32k $\Omega$	13.3%	The device supports seven, fixed power transfer settings, by selection of a corresponding $R_{PXFR}$ value. Selecting a given power transfer setting adjusts the duty cycle of the power converter and hence the amount of power transferred. Higher power transfer settings leads to an increased duty cycle of the power converter leading to increased power transfer and consumption. During power up, the power transfer setting is determined and remains fixed at that setting until VDDP power cycles.
9.09k $\Omega$	26.7%	
11k $\Omega$	40.0%	
12.7k $\Omega$	53.3%	
14.7k $\Omega$	66.7%	
16.5k $\Omega$	80.0%	
20k $\Omega$	93.3%	

(1) Standard resistor (EIA E96), 1% tolerance, nominal value.

(2)  $R_{PXFR} \geq 100k\Omega$  or  $R_{PXFR} \leq 1k\Omega$  sets the duty cycle of the power converter to 13.3%.

### 7.3.6 Two-Wire Mode

Figure 7-4 shows the basic setup required for two-wire mode operation, which requires the EN signal and VSSP ground signal. EN can be driven up to 48V. No current limiting resistor is required on EN because the TPSI3052-Q1 limits the input current based on the values set by the  $R_{PXFR}$  resistor (see Table 7-2). In this example, the TPSI3052-Q1 drives back-to-back MOSFETs in a common-source configuration.  $C_{VDDP}$  provides the required decoupling capacitance for the VDDP supply rail of the device.  $C_{DIV1}$  and  $C_{DIV2}$  provide the required decoupling capacitance of the VDDH and VDDM supply rails that provide the peak current to drive the external MOSFETs.

Figure 7-5 shows the typical operation in two-wire mode configured for standard enable. The application drives EN to a logic high and the TPSI3052-Q1 begins the power-up sequence. During power up, the current provided by the EN pin,  $I_{EN}$ , begins to charge up the external capacitance,  $C_{VDDP}$ , and the voltage on VDDP begins to rise until it reaches  $V_{VDDP\_H}$ . After VDDP reaches its peak,  $V_{VDDP\_H}$ , the TPSI3052-Q1 transfers stored energy on  $C_{VDDP}$  to the secondary side for a fixed time (3.3 $\mu$ s typical) which begins to charge up the VDDH (and VDDM) secondary side rails thereby discharging the voltage on VDDP. In steady state, this results in an average voltage on VDDP,  $V_{VDDP\_AVG}$ . This cycle repeats until the VDDH (and VDDM) secondary side rails are fully charged. The time required to fully charge VDDH depends on several factors including the values of  $C_{VDDP}$ ,  $C_{DIV1}$ ,  $C_{DIV2}$ ,  $R_{PXFR}$ , and the overall power transfer efficiency. After VDDH is fully charged, VDRV is asserted high and remains high while the EN pin remains at a logic high. When the application drives the EN pin to a logic low, the charge on VDDP begins to discharge. Prior to VDDP reaching its UVLO falling threshold, TPSI3052-Q1 signals information from the primary side to the secondary side to deassert VDRV and drive VDRV low. Because power is no longer being transferred, all rails begin to fully discharge.

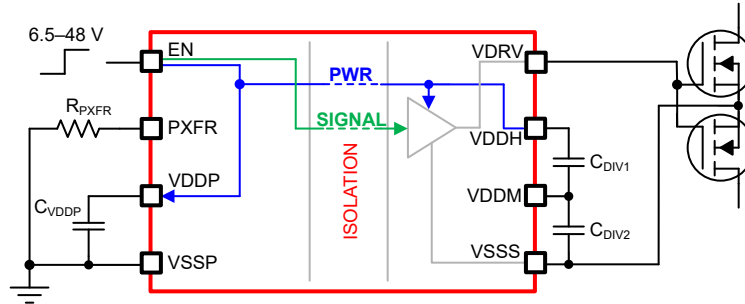


Figure 7-4. Two-Wire Mode Simplified Schematic

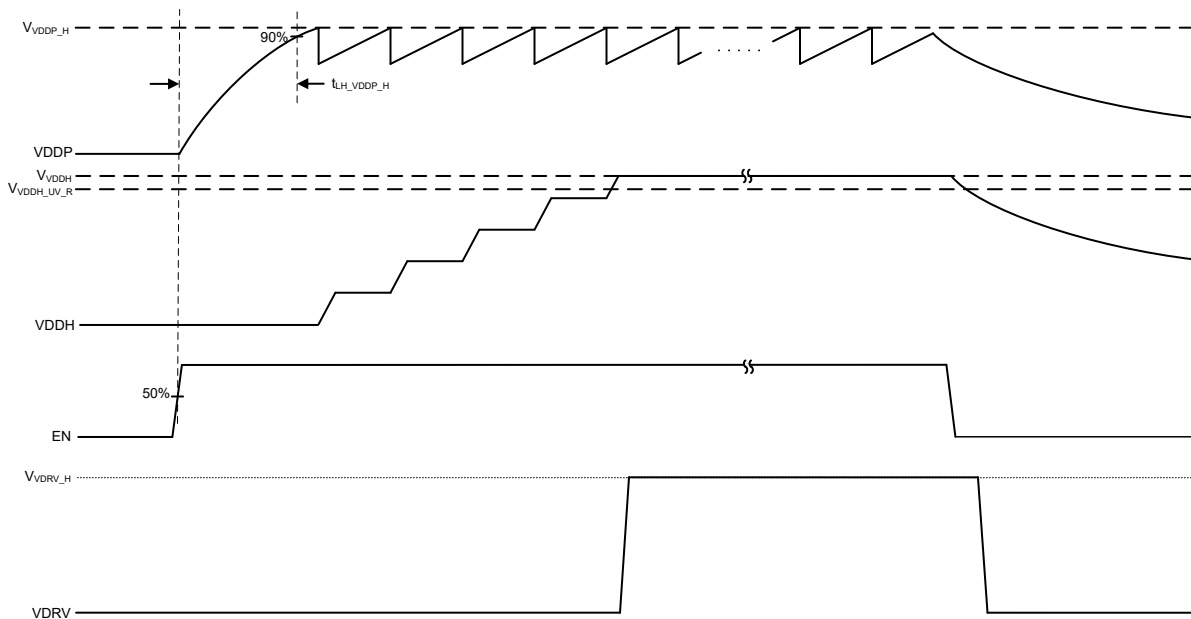


Figure 7-5. Two-Wire Mode with Standard Enable (TPSI3052-Q1 Only)

In two-wire mode, power is supplied directly by the EN pin. When EN is asserted high, the TPSI3052-Q1 transfers power to the secondary side for a fixed time ( $3.3\mu\text{s}$  nominal) while the time period varies. The period varies due to the hysteretic control of the power transfer that verifies the average current supplied through the EN pin is maintained. The amount of average current, and hence the amount of power transferred, is programmable by selecting one of seven appropriate resistor values,  $R_{PXFR}$ , from the PXFR to VSSP pins. Higher settings of  $R_{PXFR}$  increase  $I_{EN}$  which increases the average power consumed from the EN pin and increases the amount of power transferred to the secondary side VDDH supply. Similarly, lower settings of  $R_{PXFR}$  decrease  $I_{EN}$ , which decreases the average power consumed from the EN pin and decreases the amount of power transferred to the secondary side.

Table 7-2 summarizes the two-wire mode power selection.

**Table 7-2. Two-Wire Mode Power Selection**

$R_{PXFR}$ <sup>(1) (2)</sup>	$I_{EN}$ (Two-Wire Mode, Nominal)	Description
7.32k $\Omega$	1.9mA	The device supports seven, fixed EN input current limit options selected by the corresponding $R_{PXFR}$ specified value. Higher current limit selections lead to increased power transfer and consumption. During power up, the EN input current limit is determined and remains fixed at that setting until VDDP power cycles.
9.09k $\Omega$	2.8mA	
11k $\Omega$	3.7mA	
12.7k $\Omega$	4.5mA	
14.7k $\Omega$	5.2mA	
16.5k $\Omega$	6.0mA	
20k $\Omega$	6.7mA	

- (1) Standard resistor (EIA E96), 1% tolerance, nominal value.  
 (2)  $R_{PXFR} \geq 100k\Omega$  or  $R_{PXFR} \leq 1k\Omega$  sets the  $I_{EN}$  to 1.9mA.

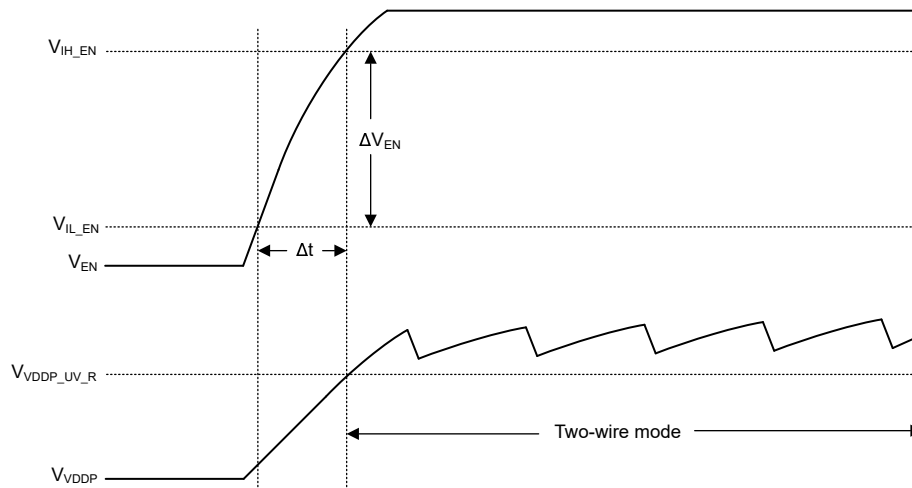
### 7.3.7 VDDP, VDDH, and VDDM Undervoltage Lockout (UVLO)

TPSI3052-Q1 and TPSI3052S-Q1 implement an internal UVLO protection feature for both input and output power supplies, VDDP, VDDH, and VDDM. When VDDP is lower than the UVLO threshold voltage, power ceases transfer to the VDDM and VDDH rails. Over time, the VDDH and VDDM rails begin to discharge. If enough charge is available on VDDP, the device attempts to signal VDRV to assert low. If not enough charge is available on VDDP, a timeout mechanism establishes that VDRV asserts low after reaching the timeout. When either VDDH or VDDM are lower than the respective UVLO thresholds, VDRV asserts low, regardless of the EN state. The UVLO protection blocks feature hysteresis, which helps to improve the noise immunity of the power supply. During turn-on and turn-off, the driver sources and sinks a peak transient current, which can result in voltage drop of the VDDH, VDDM power supplies. The internal UVLO protection block ignores the associated noise during these normal switching transients.

### 7.3.8 Power Supply and EN Sequencing

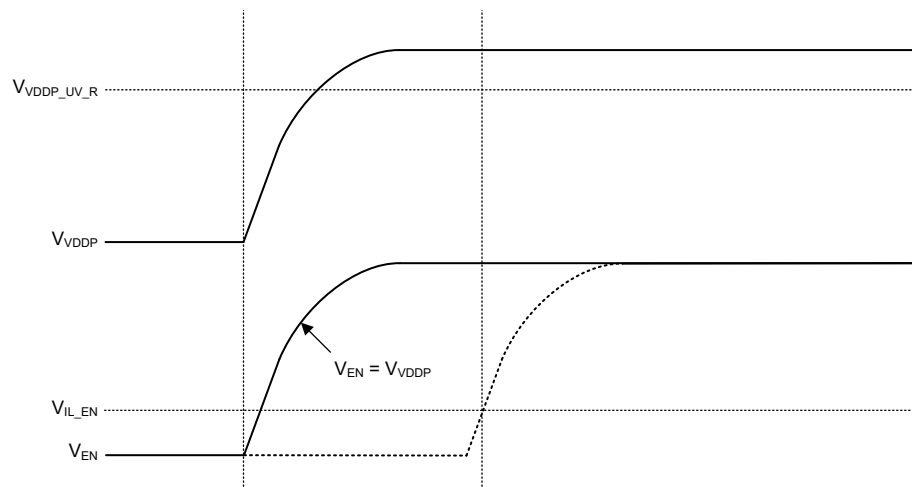
During power up, the device automatically determines whether to enter two-wire or three-wire mode. Once the wire mode is determined, the mode is maintained until another power cycle is performed. Therefore, it is important to understand different scenarios that can affect the device operation.

In two-wire mode, the device is supplied power from a single external voltage source through EN, which charges the  $C_{VDDP}$  capacitance on VDDP. The voltage supply is required to meet the power supply needs at the selected PXFR setting, as well as to meet the recommended minimum ramp time,  $|\Delta V_{EN}/\Delta t|$ . To verify that two-wire mode is entered properly,  $V_{EN}$  must reach  $V_{IH\_EN}$  prior to  $V_{VDDP}$  reaching  $V_{VDDP\_UV\_R}$ . This is summarized in [Figure 7-6](#). Similarly, TI recommends that  $V_{EN}$  meet the minimum recommended ramp down time to  $V_{IL\_EN}$ . Too slow a ramp down time can cause insufficient power to transfer while slowly transitioning between  $V_{IH\_EN}$  and  $V_{IL\_EN}$  leading to intermittent de-assertions and assertions of VDRV. This can continue until the power transfer reduces sufficiently to maintain VDRV low.



**Figure 7-6. Two-Wire Mode Entry**

In most three-wire mode applications, EN and VDDP are supplied by the same voltage rail and source. TI recommends that  $V_{EN}$  remain below  $V_{IL\_EN}$  until  $V_{VDDP}$  reaches  $V_{VDDP\_UV\_R}$ . Some applications can directly connect EN to the VDDP supply. These two scenarios are shown in [Figure 7-7](#).



**Figure 7-7. Three-Wire Mode Power Sequences**

In three-wire mode applications with separate voltage sources supplying EN and VDDP, TI recommends that  $V_{EN}$  remain below  $V_{IL\_EN}$  until  $V_{VDDP}$  reaches  $V_{VDDP\_UV\_R}$ . If  $V_{EN}$  reaches  $V_{IH\_EN}$  prior to  $V_{VDDP}$  reaching  $V_{VDDP\_UV\_R}$ , current from the supply that sources EN attempts to power VDDP. Depending on the impedance residing on the other supply on VDDP and the amount of power available from the EN pin,  $V_{VDDP}$  can begin to rise and eventually exceed  $V_{VDDP\_UV\_R}$ . At that point, the device begins to transfer power to the secondary and start charging the VDDM and VDDH rails. If VDDP remains above  $V_{VDDP\_UV\_R}$ , the device continues to transfer power to the secondary eventually charging the VDDM and VDDH rails and VDRV can assert high.

### 7.3.9 Thermal Shutdown

The device contains an integrated temperature sensor to monitor the local temperature of the device. When the sensor reaches its threshold, it automatically ceases power transfer from the primary side to the secondary side. In addition, if power is still present on VDDP, the driver is automatically asserted low. The power transfer is disabled until the local temperature reduces enough to re-engage.

## 7.4 Device Functional Modes

Table 7-3 summarizes the functional modes for the TPSI3052-Q1 and TPSI3052S-Q1.

**Table 7-3. TPSI3052-Q1, TPSI3052S-Q1 Device Functional Modes**

VDDP <sup>(1)</sup>	VDDH	EN <sup>(1)</sup>	VDRV	COMMENTS
Powered up <sup>(2)</sup>	Powered up <sup>(3)</sup>	L	L	TPSI3052-Q1 normal operation: VDRV output state assumes logic state of EN logic state.
		H	H	
		L	L	TPSI3052S-Q1 normal operation (three-wire mode only): rising edge of EN causes VDRV to be singly pulsed high. EN must be asserted low first to assert another pulse.
		L → H	L → H → L	
Powered down <sup>(6)</sup>	Powered down <sup>(4)</sup>	X <sup>(5)</sup>	L	Disabled operation: VDRV output disabled, keep off circuitry applied.
Powered up <sup>(2)</sup>	Powered down <sup>(4)</sup>	X <sup>(5)</sup>	L	Disabled operation: VDRV output disabled, keep off circuitry applied.
Powered down <sup>(6)</sup>	Powered up <sup>(3)</sup>	X <sup>(5)</sup>	L	Disabled operation: when VDDP is powered down, output driver is disabled automatically after timeout, keep off circuitry applied.

- (1) Refer to [Power Supply and EN Sequencing](#) for additional information.
- (2)  $V_{VDDP} \geq VDDP$  undervoltage lockout rising threshold,  $V_{VDDP\_UV\_R}$ .
- (3)  $V_{VDDH} \geq VDDH$  undervoltage lockout rising threshold,  $V_{VDDH\_UV\_R}$ .
- (4)  $V_{VDDH} < VDDH$  undervoltage lockout falling threshold,  $V_{VDDH\_UV\_F}$ .
- (5) X: do not care.
- (6)  $V_{VDDP} < VDDP$  undervoltage lockout falling threshold,  $V_{VDDP\_UV\_F}$ .

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The TPSI3052-Q1 is a fully integrated, isolated switch driver with integrated bias, which when combined with an external power switch, forms a complete isolated solid state relay solution. With a nominal gate drive voltage of 15V with 1.5/3.0A peak source and sink current, select from a large variety of external power switches, such as MOSFETs, IGBTs, or SCRs, to meet a range of applications. The TPSI3052-Q1 generates its own secondary bias supply from the power received from its primary side, so no isolated secondary supply bias is required.

The TPSI3052-Q1 supports two modes of operation based on the number of input pins required. In two-wire mode, typically found in driving mechanical relays, controlling the switch requires only two pins and supports a wide voltage range of operation from 6.5V to 48V. In three-wire mode, the primary supply from 3V to 5.5V is supplied externally, and the switch is controlled through a separate enable. Available in three-wire mode only, the TPSI3052S-Q1 features a one-shot enable for the switch control. This feature is useful for driving SCRs that typically require only one pulse of current to trigger.

The secondary side provides a regulated, floating supply rail of 15V for driving a large variety of power switches with no need for a secondary bias supply. The TPSI3052-Q1 supports driving single power switch, dual back-to-back, parallel power switches for a variety of AC or DC applications. The TPSI3052-Q1 integrated isolation protection is robust with higher reliability, lower power consumption, and increased temperature ranges than those found using traditional mechanical relays and optocouplers.

Adjust the power dissipation of the TPSI3052-Q1 using an external resistor from the PXFR pin to VSSP. This feature allows for tradeoffs in power dissipation versus power provided on the secondary depending on the needs of the application.

### 8.2 Typical Application

The circuits in [Figure 8-1](#) and [Figure 8-2](#) show a typical application for driving silicon based MOSFETs in three-wire mode and two-wire mode, respectively.

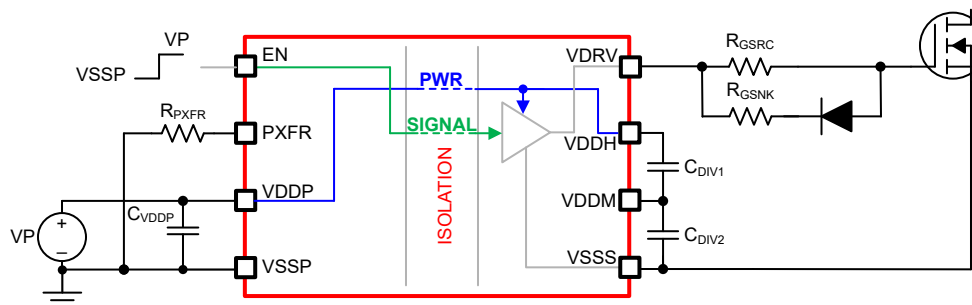


Figure 8-1. TPSI3052-Q1 Three-Wire Mode Driving MOSFETs

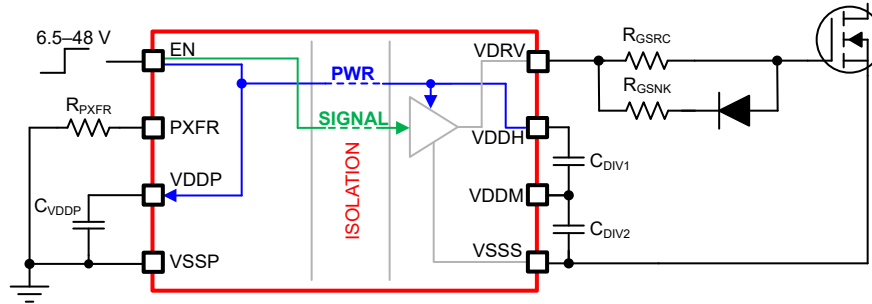


Figure 8-2. TPSI3052-Q1 Two-Wire Mode Driving MOSFETs

### 8.2.1 Design Requirements

Table 8-1 lists the design requirements of the TPSI3052-Q1 gate driver.

Table 8-1. TPSI3052-Q1 Design Requirements

DESIGN PARAMETERS	
Total gate capacitance	100nC
FET turn-on time	1μs
Propagation delay	< 4μs
Switching frequency	10kHz
Supply voltage (VDDP)	5V ± 5%

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Two-Wire or Three-Wire Mode Selection

The first design decision is to determine if two-wire or three-wire mode can be used in the application. For this design, note that the overall propagation delay is less than 4μs and only three-wire mode is able to meet this requirement. In this case, two-wire mode is not applicable. Two-wire mode, due to its limited power transfer, is typically limited to very low frequency applications of less than a few kHz or when enable times are not critical.

#### 8.2.2.2 Standard Enable, One-Shot Enable

Next, based on the application, device if standard enable or one-shot enable mode is required. In this design, assume that after the switch is enabled, it is desired that the switch remain enabled until commanded to be disabled. Therefore, standard enable mode is assumed. In most applications that involve driving FETs, standard enable is appropriate. If driving SCRs or TRIACS, one-shot mode can be beneficial.

#### 8.2.2.3 CDIV1, CDIV2 Capacitance

The CDIV1 and CDIV2 capacitances required depends on the amount of drop that can be tolerated on the VDDH rail during switching of the external load. The charge stored on the CDIV1 and CDIV2 capacitances is used to provide the current to the load during switching. During switching, charge sharing occurs and the voltage on VDDH drops. At a minimum, TI recommends that the total capacitance formed by the series combination of CDIV1 and CDIV2 be sized to be at least 30 times the total gate capacitance to be switched. This sizing results in an approximate 0.5V drop of the VDDH supply rail that is used to supply power to the VDRV signal. Equation 1 and Equation 2 can be used to calculate the amount of capacitance required for a specified voltage drop.

CDIV1 and CDIV2 must be of the same type and tolerance.

$$C_{DIV1} = \left(\frac{n+1}{n}\right) \times \frac{Q_{LOAD}}{\Delta V}, n \geq 3.0 \quad (1)$$

$$C_{DIV2} = n \times C_{DIV1}, n \geq 3.0 \quad (2)$$

where

- n is a real number greater than or equal to 3.0.

- $C_{DIV1}$  is the external capacitance from VDDH to VDDM.
- $C_{DIV2}$  is the external capacitance from VDDM to VSSS.
- $Q_{LOAD}$  is the total charge of the load from VDRV to VSSS.
- $\Delta V$  is the voltage drop on VDDH when switching the load.

#### Note

$C_{DIV1}$  and  $C_{DIV2}$  represent absolute capacitances and components selected must be adjusted for tolerances and any derating necessary to achieve the required capacitances.

Larger values of  $\Delta V$  can be used in the application, but excessive droop can cause the VDDH undervoltage lockout falling threshold ( $V_{VDDH\_UVLO\_F}$ ) to be reached and cause VDRV to assert low. Note that as the series combination of  $C_{DIV1}$  and  $C_{DIV2}$  capacitances increases relative to  $Q_{LOAD}$ , the VDDH supply voltage drop decreases, but the initial charging of the VDDH supply voltage during power up increases.

For this design, assuming  $n = 3$  and  $\Delta V \cong 0.5V$ , then

$$C_{DIV1} = \left(\frac{3+1}{3}\right) \times \frac{120nC}{0.5V} = 320nF \quad (3)$$

$$C_{DIV2} = 3 \times 320nF = 960nF \quad (4)$$

For this design,  $C_{DIV1} = 330nF$  and  $C_{DIV2} = 1\mu F$  standard capacitor values are selected.

#### 8.2.2.4 $R_{PXFR}$ Selection

The selection of  $R_{PXFR}$  allows for a tradeoff between power consumed and power delivered, as described in [Three-wire Mode](#). For this design, select an appropriate  $R_{PXFR}$  that establish that enough power is transferred to support the amount of load being driven at the specified switching frequency.

During switching of the load,  $Q_{LOAD}$  of charge on VDDH is transferred to the load and VDDH supply voltage droops. After each switching cycle, replenish this charge before the next switching cycle occurs. This action ensures that the charge residing on VDDH does not deplete over time due to subsequent switching cycles of the load. The time it takes to recover this charge,  $t_{RECOVER}$ , can be estimated as follows:

$$t_{RECOVER} = \frac{1}{f_{MAX}} \cong \frac{Q_{LOAD}}{I_{OUT}} \quad (5)$$

where

- $Q_{LOAD}$  is the load charge in Coulombs
- $I_{OUT}$  is the average current available from VDDH supply in Amperes (A)
- $f_{MAX}$  is maximum switching frequency in Hertz (Hz)

For this design,  $Q_{LOAD} = 100nC$  and  $f_{MAX} = 10kHz$  are known, so  $I_{OUT}$  required can be estimated as

$$I_{OUT} \cong 100nC \times 10kHz = 1.0mA \quad (6)$$

$I_{OUT}$  represents the minimum average current required to meet the design requirements. Using the TPSI3052-Q1 calculator tool, find the  $R_{PXFR}$  necessary by referring to the  $I_{OUT}$  or  $f_{MAX}$  columns. [Table 8-2](#) shows the results from the tool, assuming  $V_{DDP} = 4.75V$ , to account for the supply tolerance specified in the design requirements. Find the TPSI3052-Q1 Calculator tool at [Design Calculator](#).

**Table 8-2. Results from the TPSI3052-Q1 Calculator Tool,  $T_A = 25^\circ C$ , Three-Wire Mode**

$R_{PXFR}$ , k $\Omega$	Power Converter Duty Cycle, %	$I_{VDDP}$ , mA	$P_{IN}$ , mW	$P_{OUT}$ , mW	$I_{OUT}$ , mA	$t_{START}$ , $\mu s$	$t_{RECOVER}$ , $\mu s$	$f_{EN\_MAX}$ , kHz	$I_{AUX\_MAX}$ , mA
7.32	13.3	5.3	25.0	5.9	0.35	N/A	N/A	N/A	N/A
9.09	21.1	8.3	39.6	10.0	0.62	N/A	N/A	N/A	N/A
11	40.0	15.8	75.1	26.8	1.74	2076	56.3	17.8	2.3
12.7	53.3	21.1	100.1	36.1	2.35	1581	41.8	23.9	4.1

**Table 8-2. Results from the TPSI3052-Q1 Calculator Tool, T<sub>A</sub> = 25°C, Three-Wire Mode (continued)**

R <sub>PXFR</sub> , kΩ	Power Converter Duty Cycle, %	I <sub>VDDP</sub> , mA	P <sub>IN</sub> , mW	P <sub>OUT</sub> , mW	I <sub>OUT</sub> , mA	t <sub>START</sub> , μs	t <sub>RECOVER</sub> , μs	f <sub>EN_MAX</sub> , kHz	I <sub>AUX_MAX</sub> , mA
14.7	66.7	26.4	125.2	45.5	2.98	1287	33.2	30.2	6.0
16.5	80.0	31.6	150.2	58.8	3.86	1032	25.7	39.0	8.6
20	93.3	36.9	175.2	68.8	4.52	905	21.9	45.6	10.0

Table 8-3 summarizes the various output parameters of the calculator tool.

**Table 8-3. TPSI3052-Q1 Calculator Tool Parameter Descriptions**

Parameter	Description
R <sub>PXFR</sub>	External resistor setting that controls the amount of power transferred to the load by adjusting the duty cycle. Higher R <sub>PXFR</sub> settings lead to increased power transfer and power consumption.
Power Converter Duty Cycle	Nominal duty cycle of the power converter. Higher R <sub>PXFR</sub> settings leads to higher duty cycles of the power converter and higher power transfer.
I <sub>VDDP</sub>	Average current consumed from the VDDP supply
P <sub>IN</sub>	Average power consumed from the VDDP supply
P <sub>OUT</sub>	Average power delivered to the VDDH supply
I <sub>OUT</sub>	Average current delivered to the VDDH supply
t <sub>START</sub>	Start-up time from VDDP rising until VDDH supply rail is fully charged. This parameter assumes VDDH and VDDM supply rails are fully discharged initially.
t <sub>RECOVER</sub>	Represents the time for the VDDH rail to recover after switching the load present on VDRV
f <sub>MAX</sub>	Maximum switching frequency possible for a given R <sub>PXFR</sub> setting for the applied loading conditions
I <sub>AUX_MAX</sub>	Maximum auxiliary current available at current user input settings. There is an inverse relationship between f <sub>MAX</sub> and I <sub>AUX_MAX</sub> .

For this design example, configure the R<sub>PXFR</sub> to the 9.09kΩ setting or higher to transfer enough power to support switching the specified load at the required 10kHz frequency.

#### 8.2.2.5 C<sub>VDDP</sub> Capacitance

For two-wire mode, the recommended capacitance C<sub>VDDP</sub> from VDDP to VSSP is 220nF.

For this design, three-wire mode is required to meet the design requirements. For three-wire mode, increasing the amount of capacitance, C<sub>VDDP</sub>, improves the ripple on the VDDP supply. For this design, 1μF in parallel with 100nF is used.

#### 8.2.2.6 Gate Driver Output Resistor

The optional external gate driver resistors, R<sub>GSRC</sub> and R<sub>GSNK</sub>, along with the diode are used to:

1. Limit ringing caused by parasitic inductances and capacitances
2. Limit ringing caused by high voltage switching dv/dt, high current switching di/dt, and body-diode reverse recovery
3. Fine-tune gate drive strength for sourcing and sinking
4. Reduce electromagnetic interference (EMI)

The TPSI3052-Q1 has a pullup structure with a P-channel MOSFET with a peak source current of 1.5A. Therefore, the peak source current can be predicted with:

$$I_{O+} \cong \min\left(1.5A, \frac{V_{VDDH}}{R_{DSON\_VDRV} + R_{GSRC} + R_{GFET\_INT}}\right) \quad (7)$$

where

- R<sub>GSRC</sub>: external turn-on resistance.
- R<sub>DSON\_VDRV</sub>: TPSI3052-Q1 driver on resistance in high state. See *Electrical Characteristics*.



As an example, assume that the auxiliary circuitry requires an average current of 4mA. [Table 8-4](#) summarizes the results from the TPSI3052-Q1 calculator tool. The Calculator tool can be found at [Design Calculator](#).

**Table 8-4. Results from the TPSI3052-Q1 Calculator Tool,  $T_A = 25^\circ\text{C}$ , Three-Wire Mode with  $I_{\text{AUX}} = 4\text{mA}$**

$R_{\text{PXFR}}$ , k $\Omega$	Power Converter Duty Cycle, %	$I_{\text{VDDP}}$ , mA	$P_{\text{IN}}$ , mW	$P_{\text{OUT}}$ , mW	$I_{\text{OUT}}$ , mA	$t_{\text{START}}$ , $\mu\text{s}$	$t_{\text{RECOVER}}$ , $\mu\text{s}$	$f_{\text{EN\_MAX}}$ , kHz	$I_{\text{AUX\_MAX}}$ , mA
7.32	13.3	5.3	25.0	5.9	0.35	N/A	N/A	N/A	N/A
9.09	21.1	8.3	39.6	10.0	0.62	N/A	N/A	N/A	N/A
11	40.0	15.8	75.1	26.8	1.74	N/A	N/A	N/A	N/A
12.7	53.3	21.1	100.1	36.1	2.35	3557	96.0	10.4	4.1
14.7	66.7	26.4	125.2	45.5	2.98	2285	60.1	16.6	6.0
16.5	80.0	31.6	150.2	58.8	3.86	1549	39.3	25.5	8.6
20	93.3	36.9	175.2	68.8	4.52	1262	31.2	32.1	10.0

Based on the results in [Table 8-4](#), several observations can be made:

- With  $R_{\text{PXFR}} = 7.32\text{k}\Omega$ ,  $R_{\text{PXFR}} = 9.09\text{k}\Omega$ , and  $R_{\text{PXFR}} = 11\text{k}\Omega$ , insufficient power is available to meet the application power needs specified in the design requirements in [Table 8-1](#).
- With  $R_{\text{PXFR}} = 12.7\text{k}\Omega$  and higher, sufficient power is transferred to meet the specified design requirements, however, for this design,  $R_{\text{PXFR}} = 14.7\text{k}\Omega$  was selected for additional margin.
- For a given  $R_{\text{PXFR}}$ , because a significant amount of the transferred power is being provided to the auxiliary circuitry,  $t_{\text{START}}$  is longer, and  $f_{\text{MAX}}$  reduced when compared to the results shown in [Table 8-4](#) with  $I_{\text{AUX}} = 0\text{mA}$ .

#### 8.2.2.9 VDDM Ripple Voltage

Note that when supplying power from VDDM, that is when  $I_{\text{AUX}} > 0\text{mA}$ , additional voltage ripple is present on the VDDM rail. For a given  $R_{\text{PXFR}}$  setting, this ripple can be reduced by applying additional capacitance from VDDM to VSSS or increasing the  $R_{\text{PXFR}}$  setting for more power transfer. For this design example, the ripple on VDDM,  $V_{\text{DDM\_ripple}}$ , computed in the calculator tool is 35mV.

### 8.2.3 Application Curves

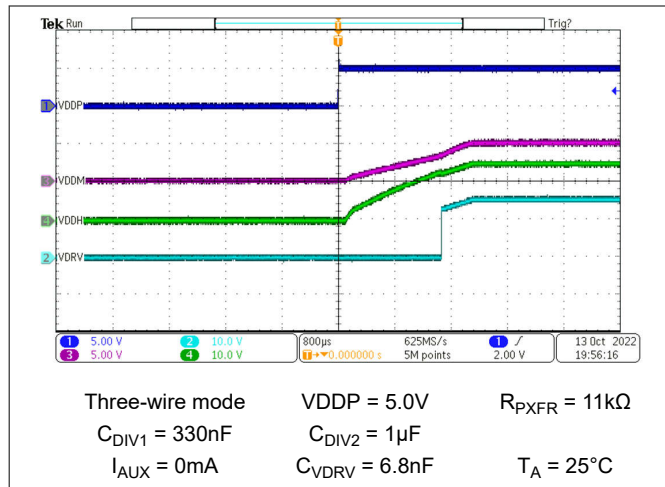


Figure 8-4. Power Up, V<sub>EN</sub> = V<sub>VDDP</sub>, Three-Wire Mode, TPSI3052-Q1

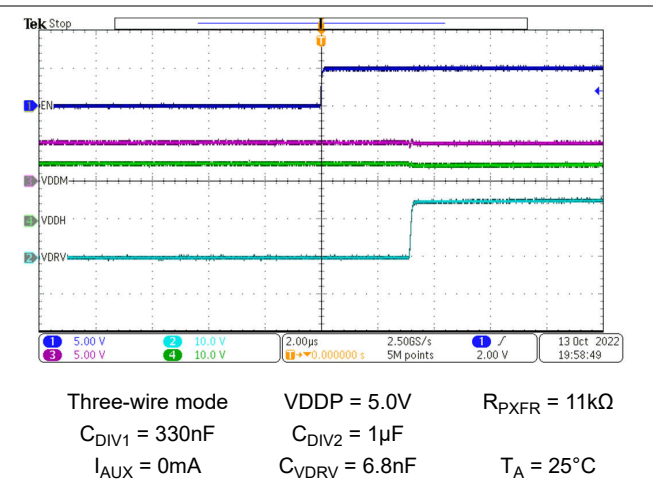


Figure 8-5. t<sub>LH\_VDRV</sub>, Three-Wire Mode, TPSI3052-Q1

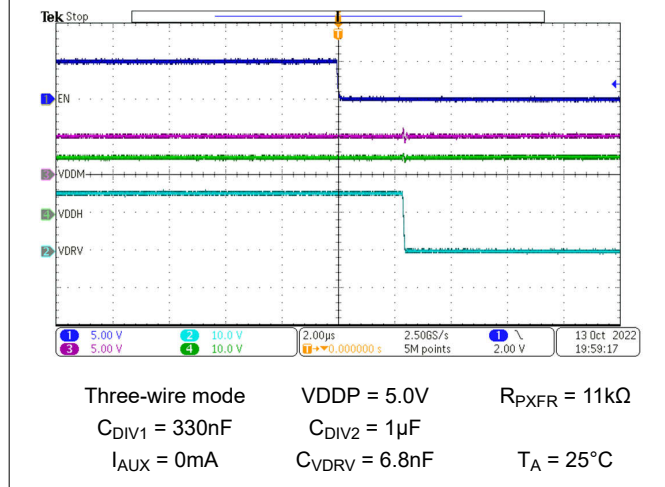


Figure 8-6. t<sub>HL\_VDRV</sub>, Three-Wire Mode, TPSI3052-Q1

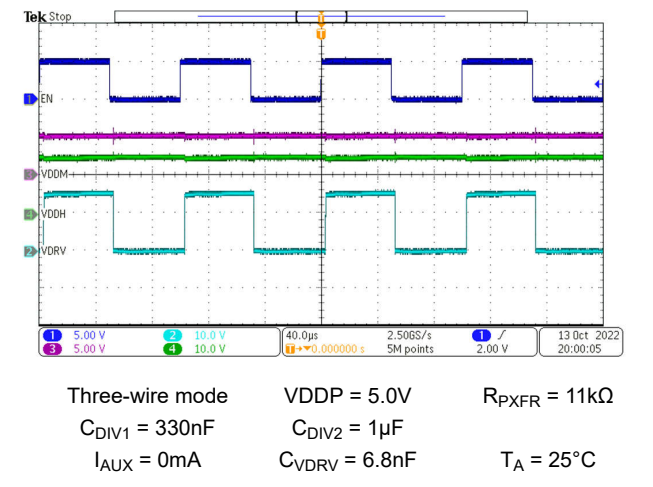


Figure 8-7. Three-Wire Mode, f<sub>EN</sub> = 10kHz, TPSI3052-Q1

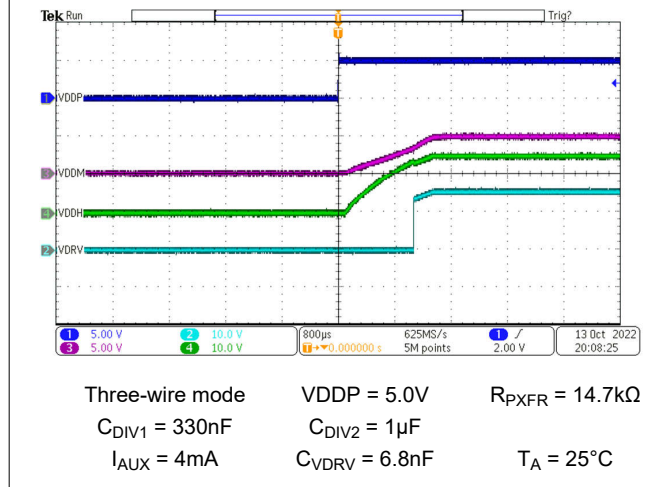


Figure 8-8. Power Up, V<sub>EN</sub> = V<sub>VDDP</sub>, Three-Wire Mode, TPSI3052-Q1

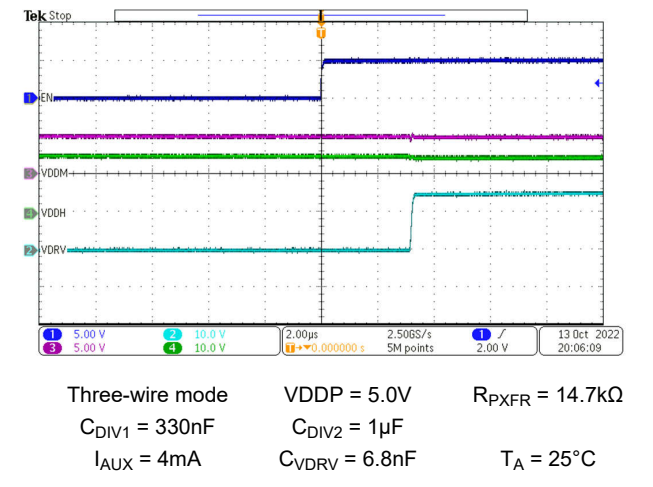
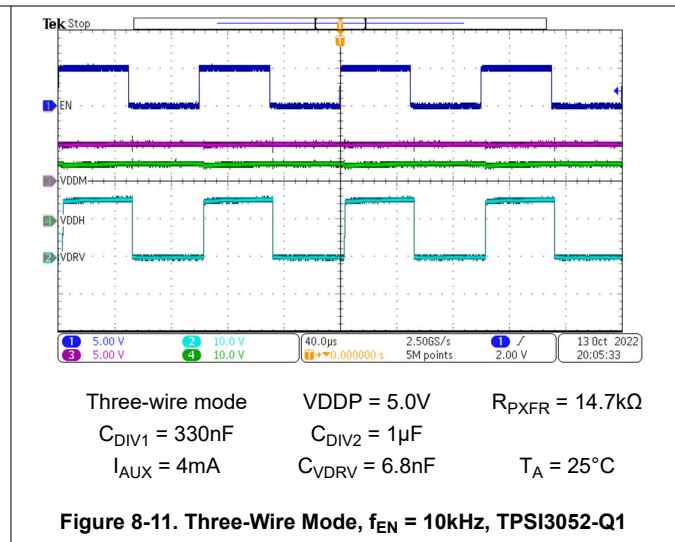
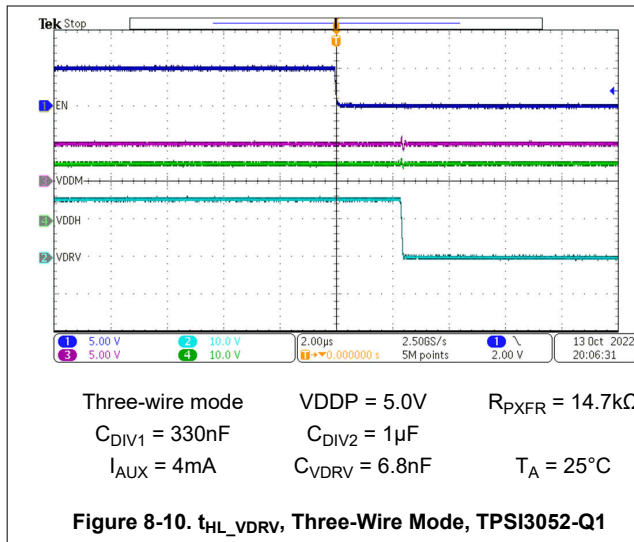


Figure 8-9. t<sub>LH\_VDRV</sub>, Three-Wire Mode, TPSI3052-Q1

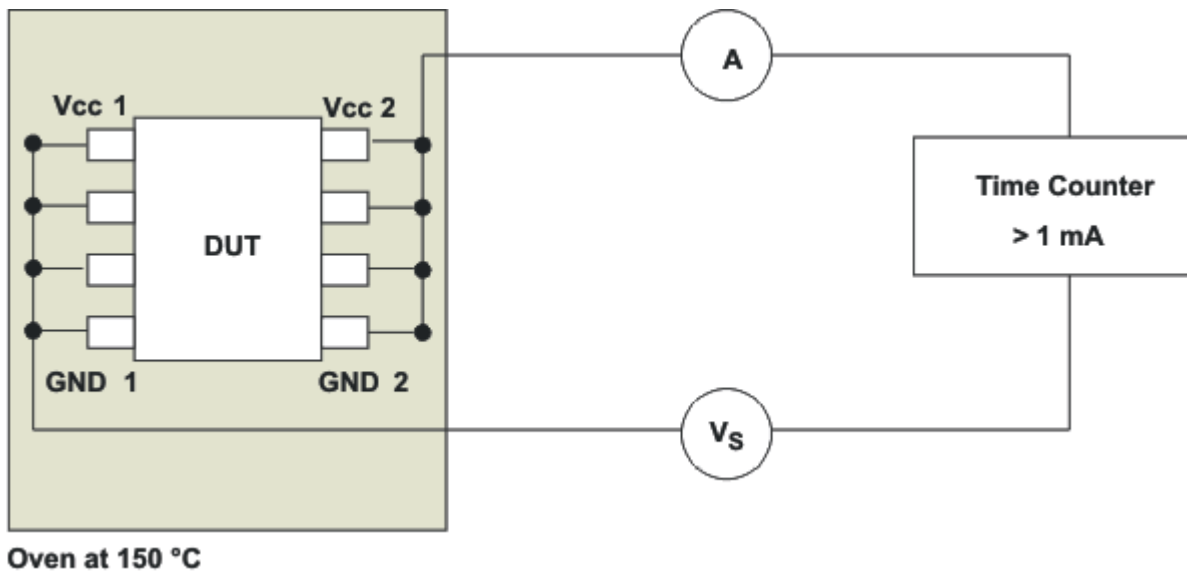
### 8.2.3 Application Curves (continued)



### 8.2.4 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 8-12 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

Figure 8-13 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is  $1000V_{RMS}$  with a lifetime of 1184 years.



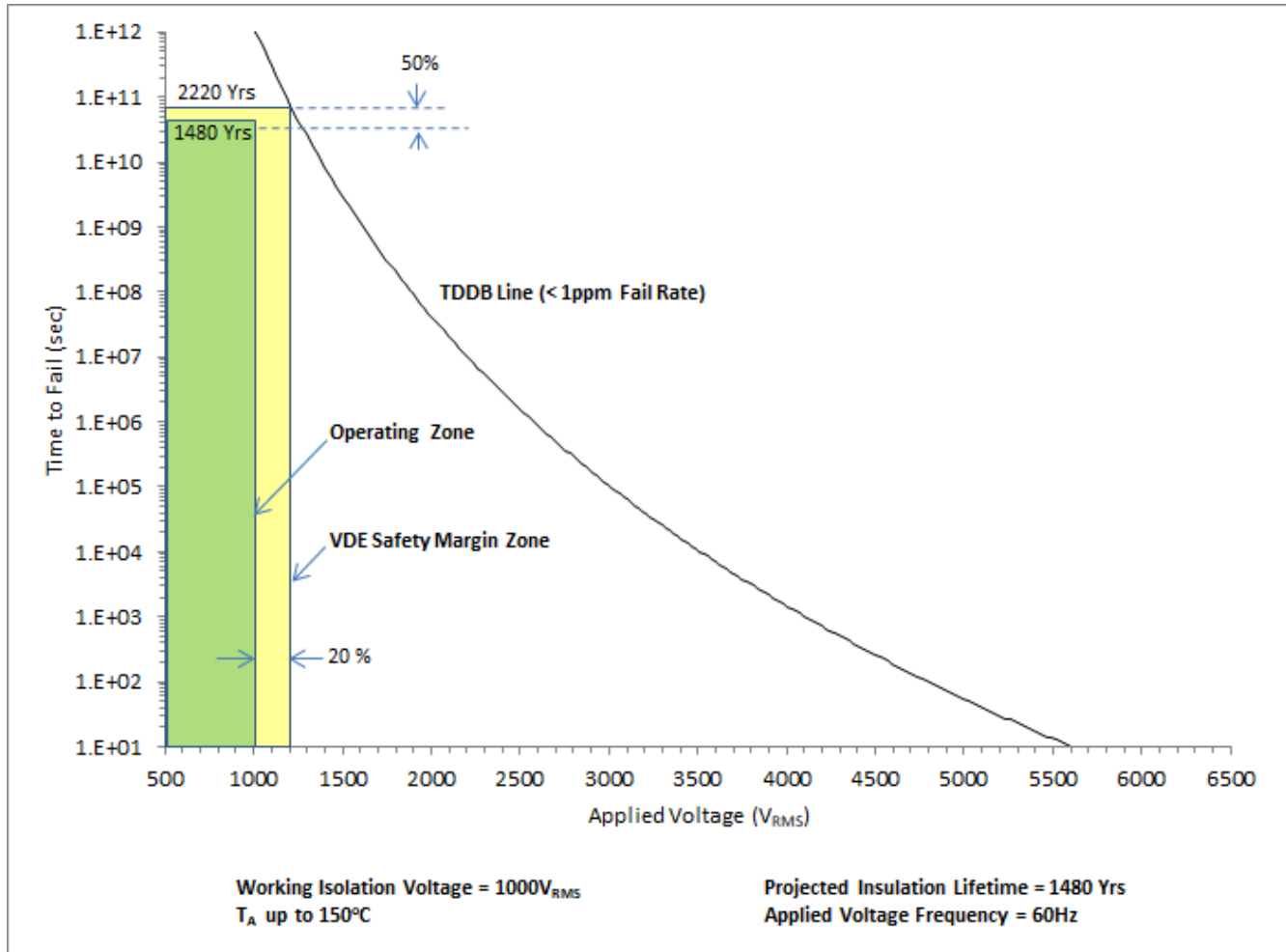


Figure 8-13. Insulation Lifetime Projection Data

### 8.3 Power Supply Recommendations

In three-wire mode, to help ensure a reliable supply voltage, TI recommends that the C<sub>VDDP</sub> capacitance from VDDP to VSSP consists of a 0.1μF bypass capacitor for high frequency decoupling in parallel with a 1μF for low frequency decoupling.

In two-wire mode, TI recommends that the C<sub>VDDP</sub> capacitance placed from VDDP to VSSP consists of a 220nF capacitor connected close to the device between the VDDP and VSSP pins. The recommended absolute capacitance must be 220nF, so if derating is required, a higher component value can be needed.

Low-ESR and low-ESL capacitors must be connected close to the device between the VDDP and VSSP pins.

### 8.4 Layout

#### 8.4.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the TPSI3052-Q1. Some key guidelines are:

- Component placement:
  - Place the driver as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces.
  - Connect low-ESR and low-ESL capacitors close to the device between the VDDH and VDDM pins and the VDDM and VSSS pins to bypass noise and to support high peak currents when turning on the external power transistor.

- Connect low-ESR and low-ESL capacitors close to the device between the VDDP and VSSP pins.
- Minimize parasitic capacitances on the R<sub>PXFR</sub> pin.
- Grounding considerations:
  - Limit the high peak currents that charge and discharge the transistor gates to a minimal physical area. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. Place the gate driver as close as possible to the transistors.
  - Connect the driver VSSS to the Kelvin connection of MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, connect the VSSS pin as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. TI recommends a PCB cutout or groove to prevent contamination that can compromise the isolation performance.
- Thermal considerations:
  - Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance ( $\theta_{JB}$ ).
  - If the system has multiple layers, TI also recommends connecting the VDDH and VSSS pins to internal ground or power planes through multiple vias of adequate size. These vias must be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

### 8.4.2 Layout Example

Figure 8-14 shows a PCB layout example with the signals and key components labeled.

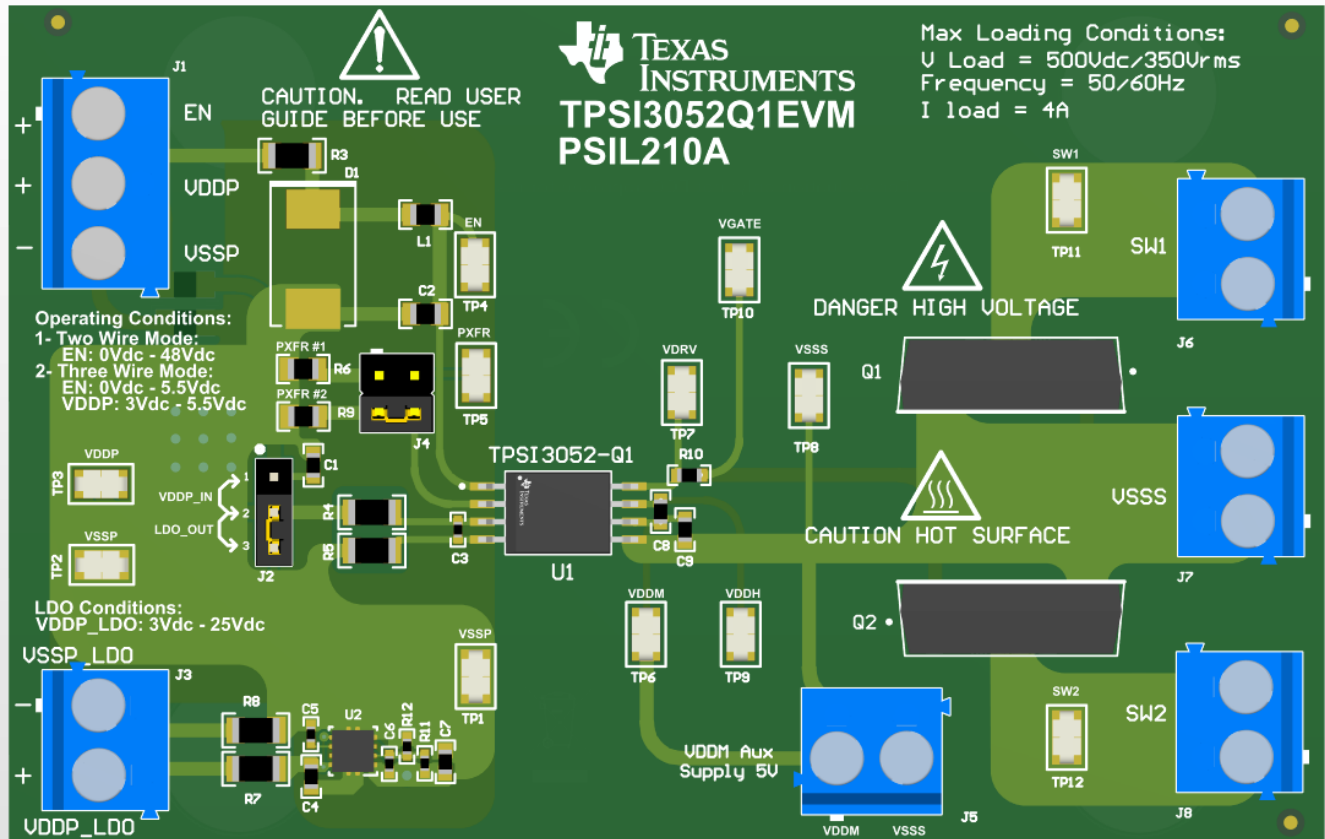


Figure 8-14. 3D PCB View

**TPSI3052-Q1**

SLVSFY5D – APRIL 2022 – REVISED FEBRUARY 2026

Figure 8-15 and Figure 8-16 show the top and bottom layer traces and copper.

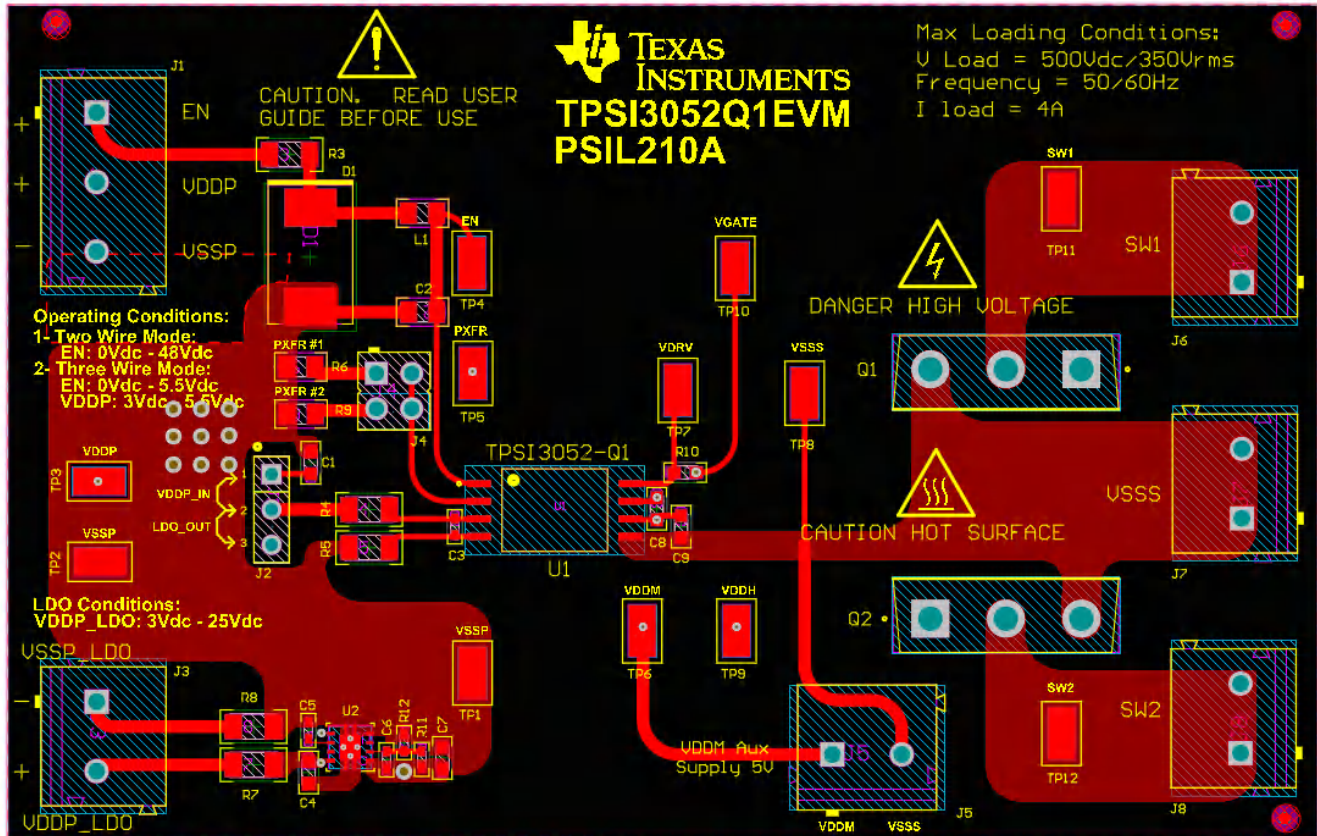


Figure 8-15. Top Layer

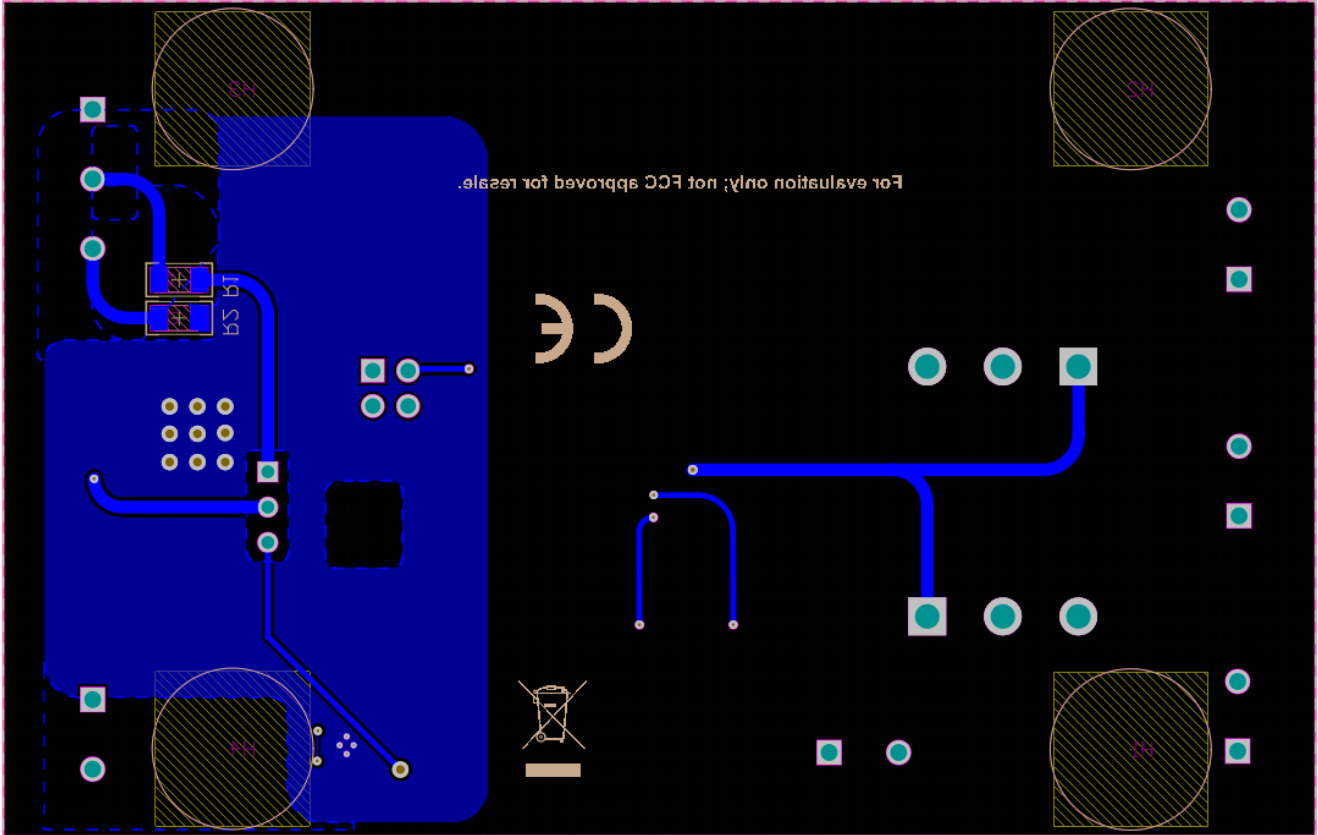


Figure 8-16. Bottom Layer

## 9 Device and Documentation Support

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision C (August 2023) to Revision D (February 2026)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added isolation lifetime data to <i>Features</i> .....	1

<b>Changes from Revision B (April 2023) to Revision C (August 2023)</b>	<b>Page</b>
• Updated Safety-Related Certifications section with associated file and certificate numbers.....	4

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPSI3052QDWZRQ1</a>	Active	Production	SO-MOD (DWZ)   8	1000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	I3052Q1
TPSI3052QDWZRQ1.A	Active	Production	SO-MOD (DWZ)   8	1000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	I3052Q1
<a href="#">TPSI3052SQDWZRQ1</a>	Active	Production	SO-MOD (DWZ)   8	1000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	I3052SQ1
TPSI3052SQDWZRQ1.A	Active	Production	SO-MOD (DWZ)   8	1000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	I3052SQ1

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

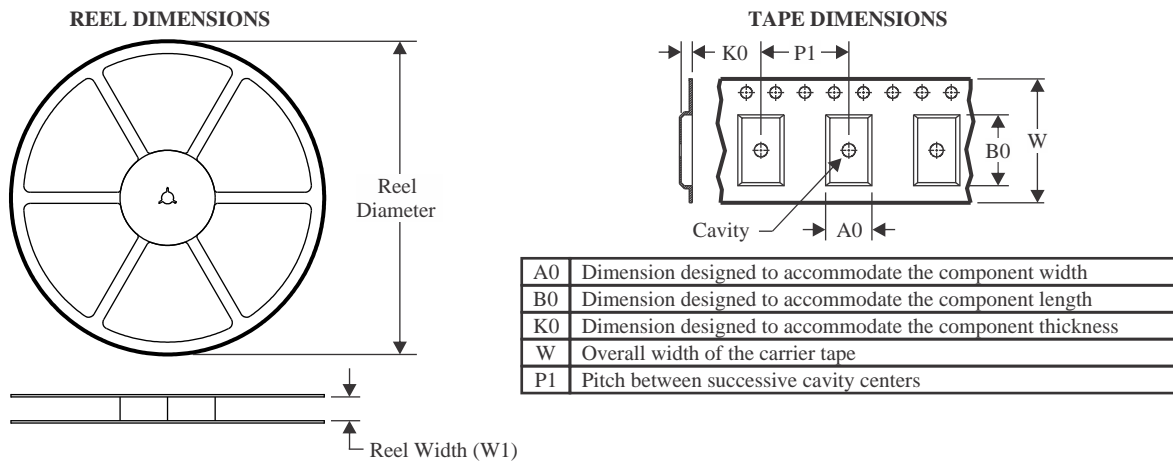
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPSI3052-Q1 :**

- Catalog : [TPSI3052](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSI3052QDWZRQ1	SO-MOD	DWZ	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3052SQDWZRQ1	SO-MOD	DWZ	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

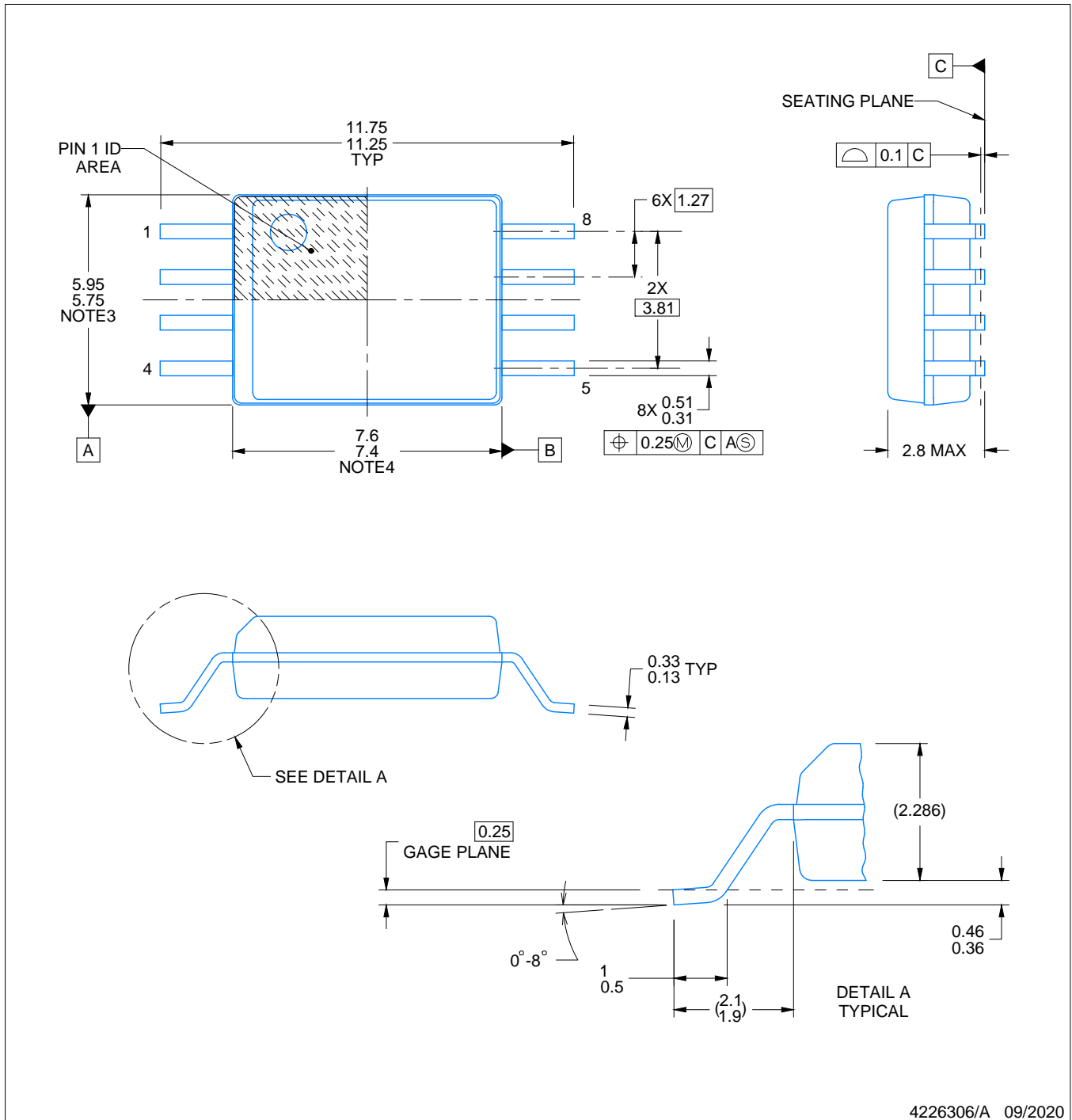
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSI3052QDWZRQ1	SO-MOD	DWZ	8	1000	350.0	350.0	43.0
TPSI3052SQDWZRQ1	SO-MOD	DWZ	8	1000	350.0	350.0	43.0

# PACKAGE OUTLINE

## DWZ0008A

### SOIC - 2.8 mm max height

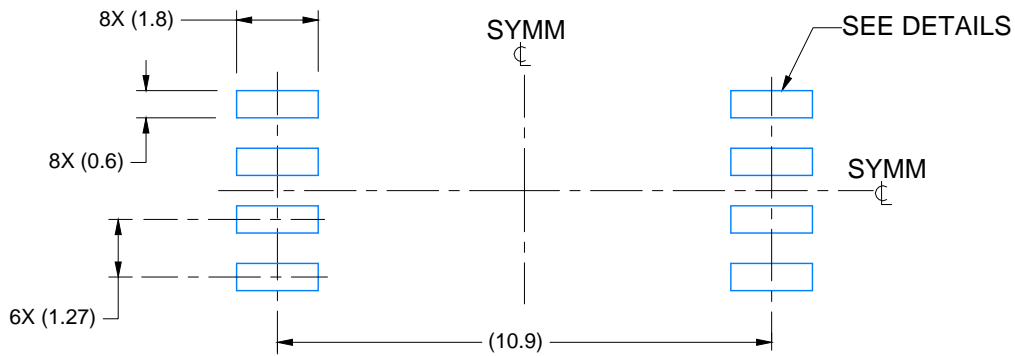
SMALL OUTLINE PACKAGE



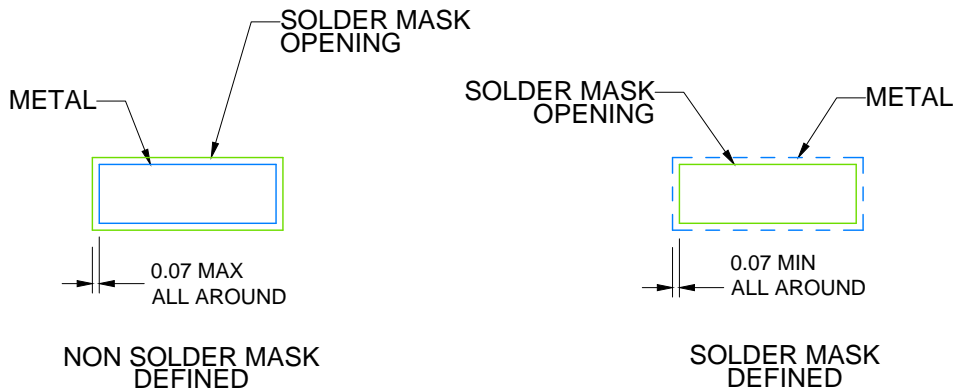
4226306/A 09/2020

#### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Ref. JEDEC registration MS-013



LAND PATTERN EXAMPLE  
9.1 mm NOMINAL CLEARANCE/CREEPAGE  
SCALE: 6X

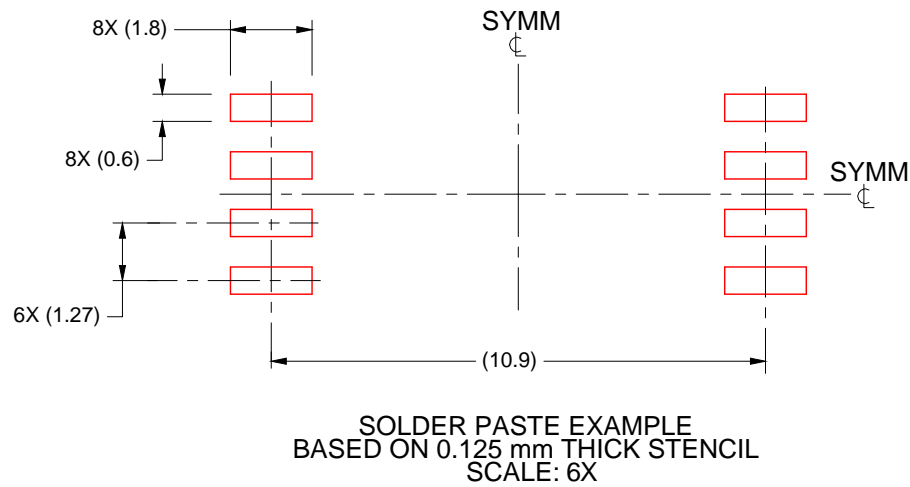


SOLDER MASK DETAILS

4226306/A 09/2020

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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