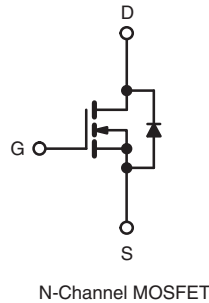
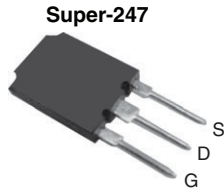


Power MOSFET



FEATURES

- Superfast body diode eliminates the need for External diodes in ZVS applications
- Lower gate charge results in simpler drive requirements
- Enhanced dV/dt capabilities offer improved ruggedness
- Higher gate voltage threshold offers improved noise immunity
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- Zero voltage switching SMPS
- Telecom and server power supplies
- Uninterruptible power supplies
- Motor control applications

PRODUCT SUMMARY	
V_{DS} (V)	500
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.087
Q_g (Max.) (nC)	380
Q_{gs} (nC)	80
Q_{gd} (nC)	190
Configuration	Single

ORDERING INFORMATION	
Package	Super-247
Lead (Pb)-free and halogen free	SiHFPS40N50L-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	500	V	
Gate-source voltage	V_{GS}	± 30		
Continuous drain current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A	
		$T_C = 100\text{ }^\circ\text{C}$		
Pulsed drain current ^a	I_{DM}	180		
Linear derating factor		4.3	W/ $^\circ\text{C}$	
Single pulse avalanche energy ^b	E_{AS}	920	mJ	
Repetitive avalanche current ^a	I_{AR}	46	A	
Repetitive avalanche Energy ^a	E_{AR}	54	mJ	
Maximum power dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	540	W
Peak diode recovery dV/dt ^c		dV/dt	34	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$	
Soldering recommendations (peak temperature)	for 10 s	300 ^d		

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 0.86\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 46\text{ A}$ (see fig. 12)
- $I_{SD} \leq 46\text{ A}$, $dI/dt \leq 550\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case




THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient ^a	R _{thJA}	-	40	°C/W
Case-to-sink, flat, greased surface	R _{thCS}	0.24	-	
Maximum junction-to-case (drain) ^a	R _{thJC}	-	0.23	

Note

a. R_{th} is measured at T_J approximately 90 °C

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	500	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA	-	0.60	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	3.0	-	5.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 30 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V	-	-	50	μA
		V _{DS} = 400 V, V _{GS} = 0 V, T _J = 125 °C	-	-	2.0	mA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 28 A ^b	-	0.087	0.100	Ω
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 46 A	21	-	-	S
Dynamic						
Input capacitance	C _{iSS}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	8110	-	pF
Output capacitance	C _{oSS}		-	960	-	
Reverse transfer capacitance	C _{rSS}		-	130	-	
Output capacitance	C _{oSS}	V _{GS} = 0 V	V _{DS} = 1.0 V, f = 1.0 MHz	-	11200	-
			V _{DS} = 400 V, f = 1.0 MHz	-	240	-
Effective output capacitance	C _{oSS eff.}	V _{GS} = 0 V	V _{DS} = 0 V to 400 V ^c	-	440	-
Effective output capacitance (energy related)	C _{oSS eff. (ER)}			-	310	-
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 46 A, V _{DS} = 400 V, see fig. 7 and 15 ^b	-	-	380
Gate-source charge	Q _{gs}			-	-	80
Gate-drain charge	Q _{gd}			-	-	190
Internal gate resistance	R _g	f = 1 MHz, open drain		-	0.90	-
Turn-on delay time	t _{d(on)}	V _{DD} = 250 V, I _D = 46 A, R _g = 0.85 Ω, V _{GS} = 10 V, see fig. 14a and 14b ^b	-	27	-	ns
Rise time	t _r		-	170	-	
Turn-off delay time	t _{d(off)}		-	50	-	
Fall time	t _f		-	69	-	
Drain-source body diode characteristics						
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	46	A
Pulsed diode forward current ^a	I _{SM}		-	-	180	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 46 A, V _{GS} = 0 V ^b	-	-	1.5	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 46 A	-	170	250	ns
		T _J = 125 °C, dI/dt = 100 A/μs ^b	-	220	330	
Body diode reverse recovery charge	Q _{rr}	T _J = 25 °C, I _S = 46 A, V _{GS} = 0 V ^b	-	705	1060	nC
		T _J = 125 °C, dI/dt = 100 A/μs ^b	-	1.3	2.0	
Reverse recovery current	I _{RRM}	T _J = 25 °C	-	9.0	-	A
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width ≤ 400 μs; duty cycle ≤ 2 %
- c. C_{oSS eff.} is a fixed capacitance that gives the same charging time as C_{oSS} while V_{DS} is rising from 0 % to 80 % V_{DS}
C_{oSS eff. (ER)} is a fixed capacitance that stores the same energy as C_{oSS} while V_{DS} is rising from 0 % to 80 % V_{DS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

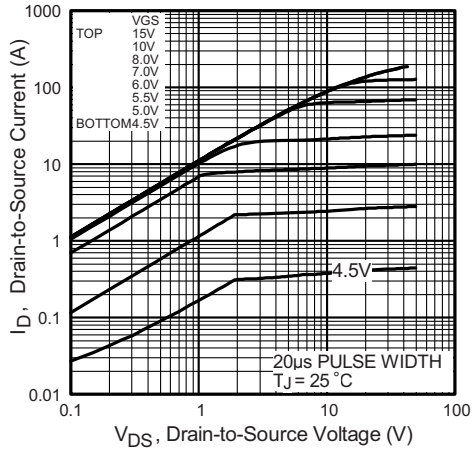


Fig. 1 - Typical Output Characteristics

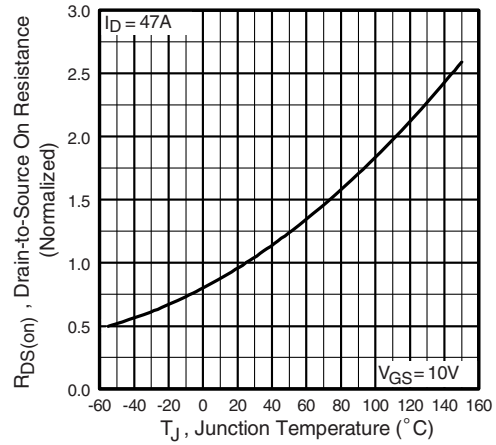


Fig. 4 - Normalized On-Resistance vs. Temperature

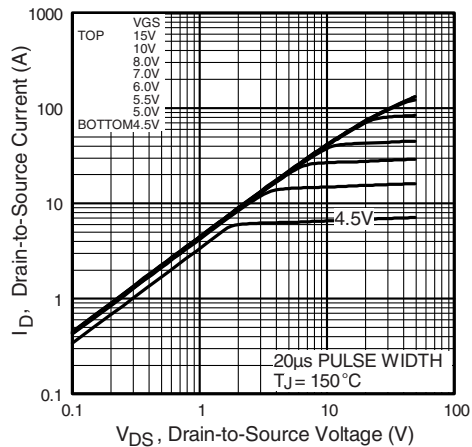


Fig. 2 - Typical Output Characteristics

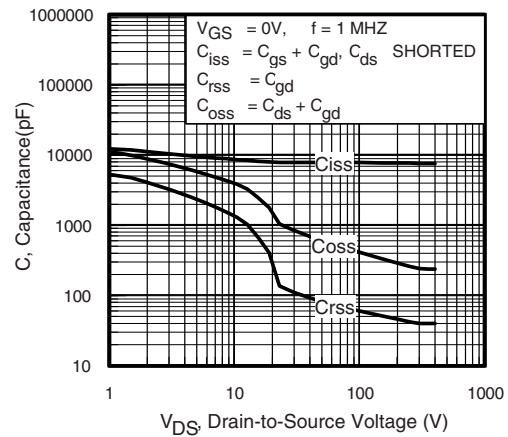


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

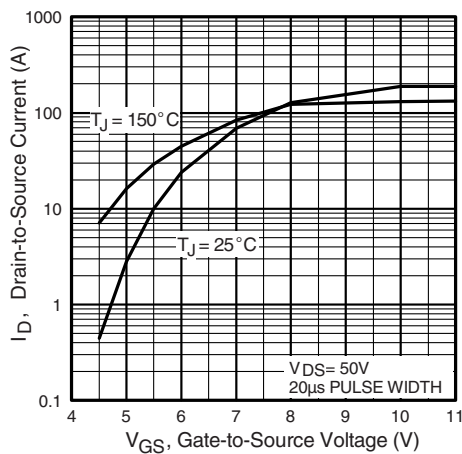


Fig. 3 - Typical Transfer Characteristics

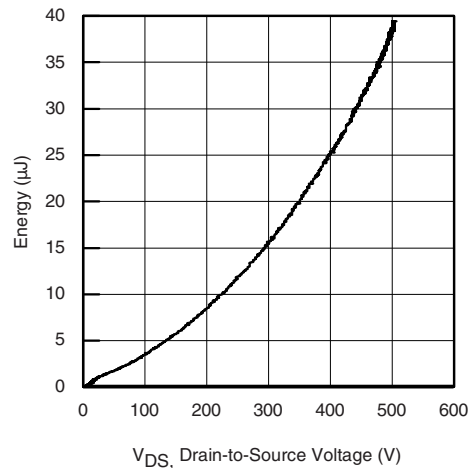


Fig. 6 - Typical Output Capacitance Stored Energy vs. VDS

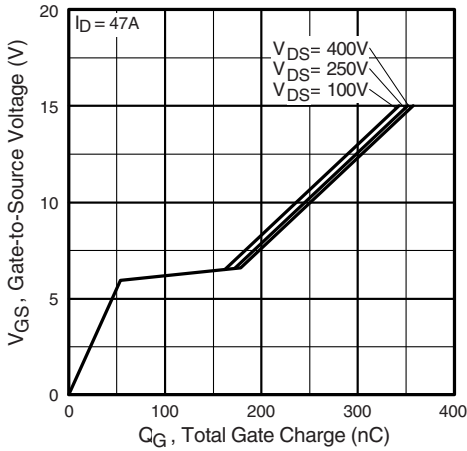


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

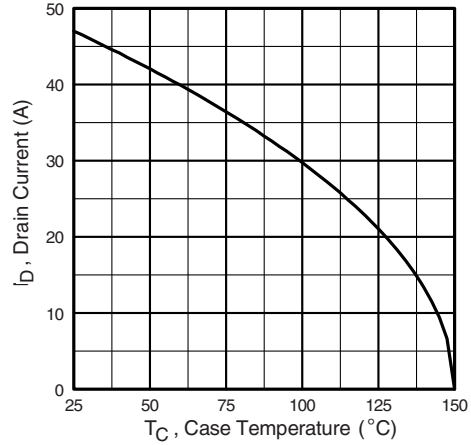


Fig. 9 - Maximum Drain Current vs. Case Temperature

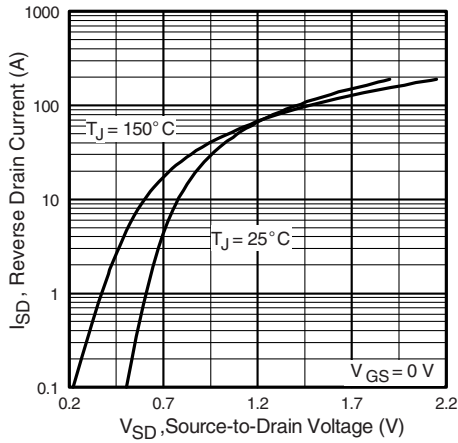


Fig. 8 - Typical Source Drain Diode Forward Voltage

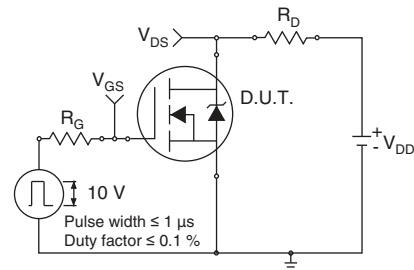


Fig. 10a - Switching Time Test Circuit

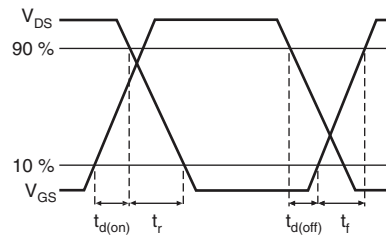


Fig. 10b - Switching Time Waveforms

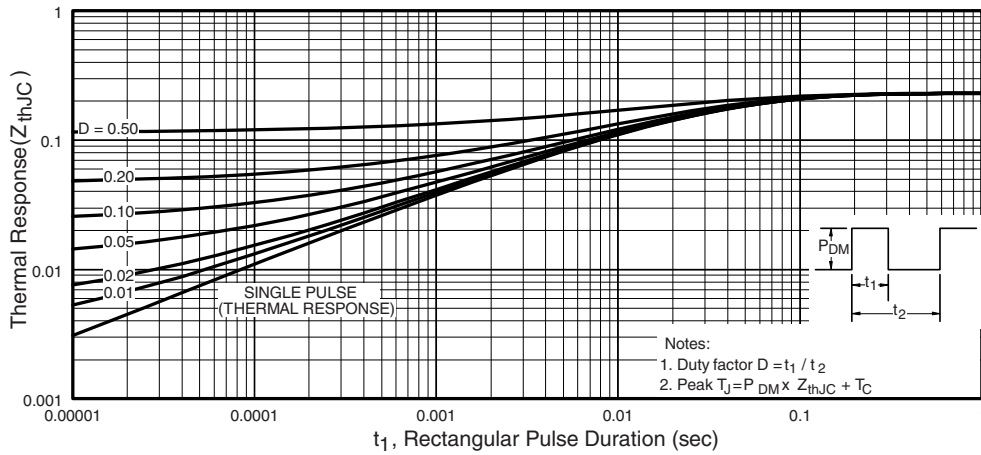


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

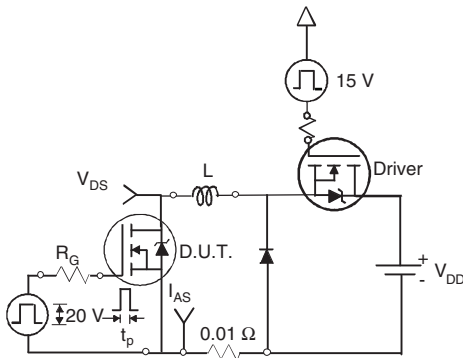


Fig. 12a - Unclamped Inductive Test Circuit

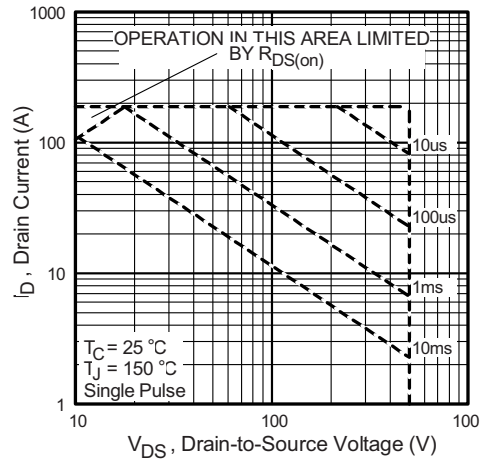


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

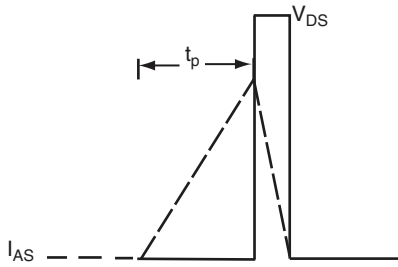


Fig. 12b - Unclamped Inductive Waveforms

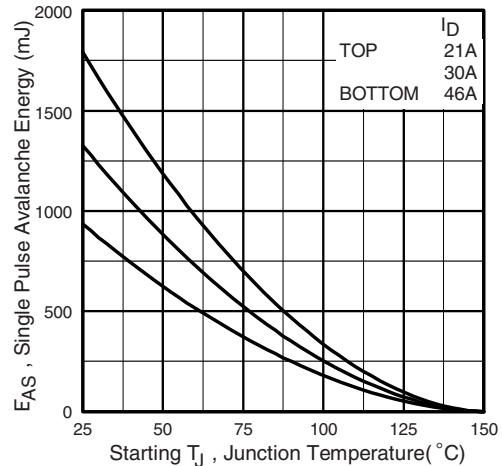


Fig. 12d - Maximum Safe Operating Area

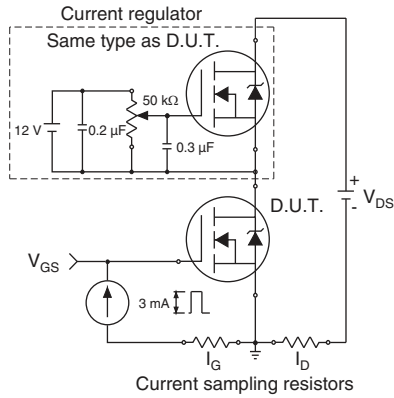


Fig. 13a - Gate Charge Test Circuit

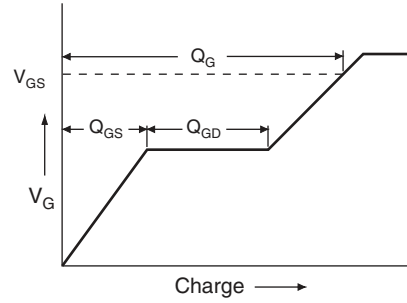
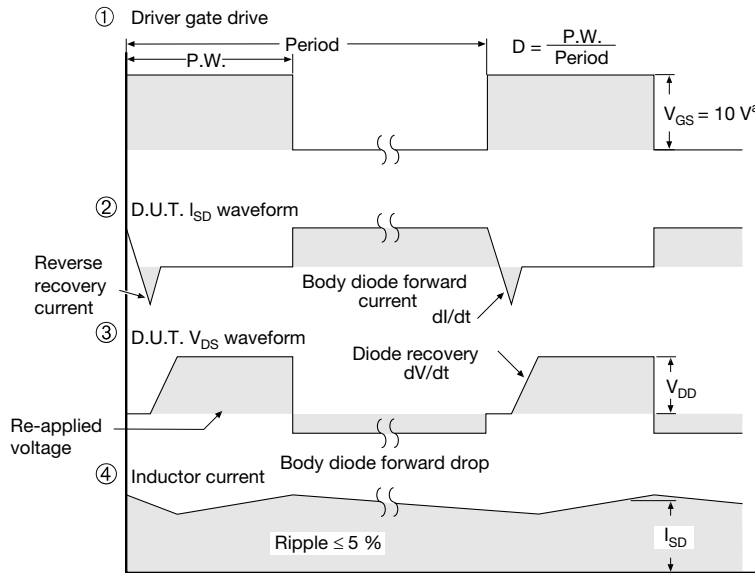
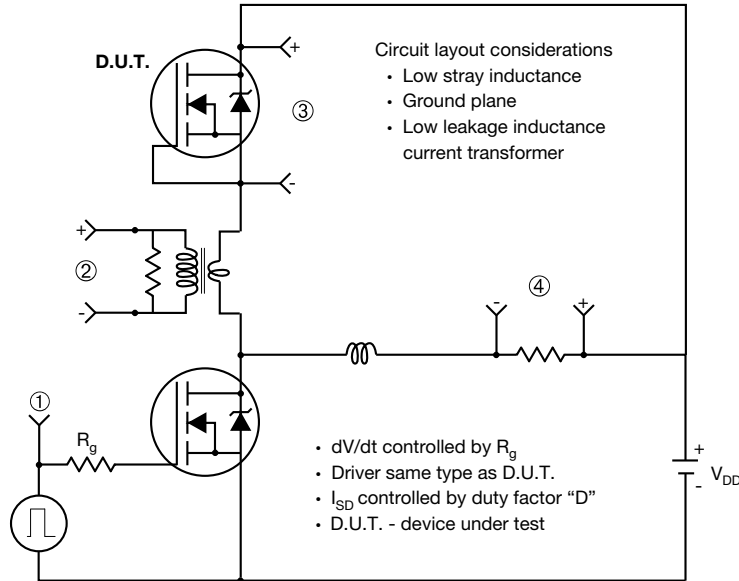


Fig. 13b - Basic Gate Charge Waveform

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

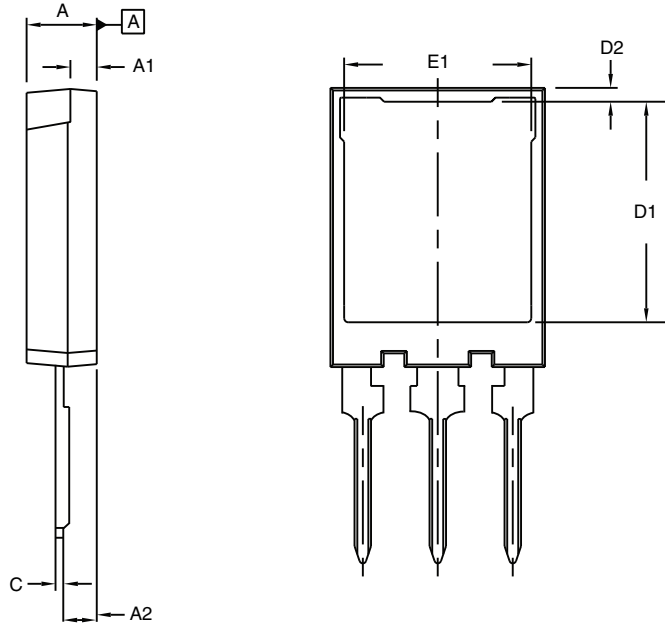
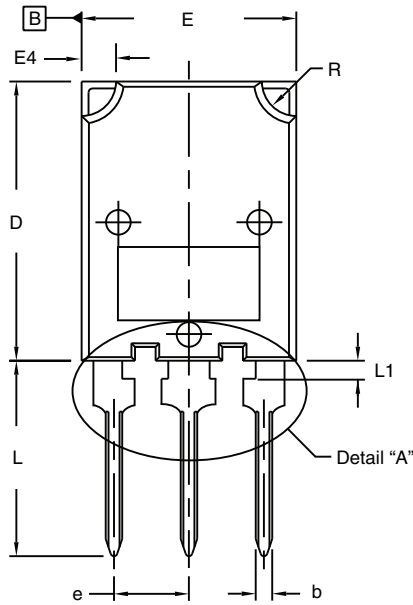
Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91260.

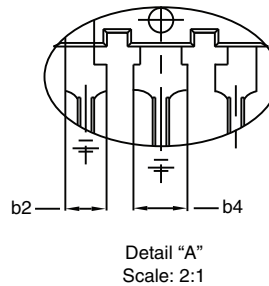
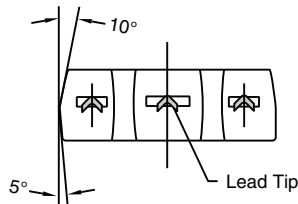


TO-274AA (High Voltage)

VERSION 1: FACILITY CODE = Y



⊕ 0.10 (0.25) ⊖ B A ⊕



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.70	5.30	0.185	0.209
A1	1.50	2.50	0.059	0.098
A2	2.25	2.65	0.089	0.104
b	1.30	1.60	0.051	0.063
b2	1.80	2.20	0.071	0.087
b4	3.00	3.25	0.118	0.128
c ⁽¹⁾	0.38	0.89	0.015	0.035
D	19.80	20.80	0.780	0.819

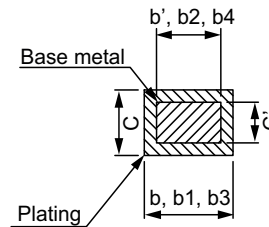
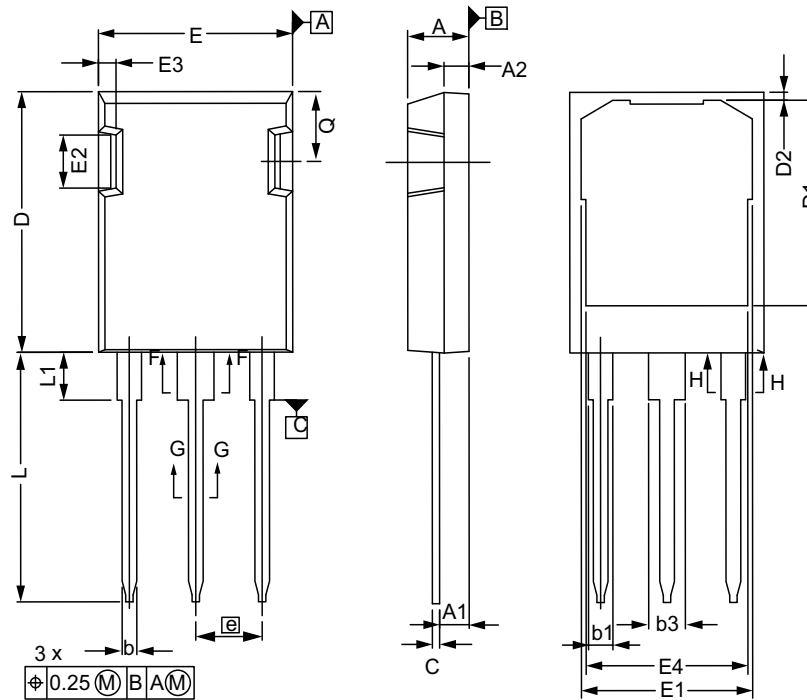
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	15.50	16.10	0.610	0.634
D2	0.70	1.30	0.028	0.051
E	15.10	16.10	0.594	0.634
E1	13.30	13.90	0.524	0.547
e	5.45 BSC		0.215 BSC	
L	13.70	14.70	0.539	0.579
L1	1.00	1.60	0.039	0.063
R	2.00	3.00	0.079	0.118

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outer extremes of the plastic body
- Outline conforms to JEDEC® outline to TO-274AA
- (1) Dimension measured at tip of lead



VERSION 2: FACILITY CODE = N



SECTION "F-F", "G-G" AND "H-H"
SCALE: NONE

DIM.	MILLIMETERS	
	MIN.	MAX.
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b'	1.07	1.28
b	1.07	1.33
b1	1.91	2.41
b2	1.91	2.16
b3	2.87	3.38
b4	2.87	3.13
c'	0.55	0.65
c	0.55	0.68
D	20.80	21.10

DIM.	MILLIMETERS	
	MIN.	MAX.
D1	16.25	17.65
D2	0.50	0.80
E	15.75	16.13
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	5.44 BSC	
N	3	
L	19.81	20.32
L1	3.70	4.00
Q	5.49	6.00

ECN: E20-0538-Rev. C, 19-Oct-2020
DWG: 5975

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Outline conforms to JEDEC® outline to TO-274AD
- Dimensions are measured in mm, angles are in degree
- Metal surfaces are tin plated, except area of cut



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Vishay products are not designed for use in life-saving or life-sustaining applications or any application in which the failure of the Vishay product could result in personal injury or death unless specifically qualified in writing by Vishay. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

⊖ [View SE050B1HQ1/Z01SEZ on WIN SOURCE](#)

⊖ [NXP / Nexperia Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management