THE DATASHEET OF

SEA-B-0500J

PTX30W

NFC Wireless Charging Listener IC

The PTX30W is a powerful and efficient NFC Listener system-on-chip for NFC wireless charging applications together with data communication. The PTX30W features a single-chip solution for NFC-based wireless charging systems which harvest power, handle wireless charging protocol, and charge a Lithium-ion battery. While eliminating external discrete components. The superior RF performance of the PTX30W enables small antenna design, fast charging and allows flexible placement of Poller and Listener antennas.

Applications

- Smartwatches, fitness trackers, wristbands
- Smart rings
- Smart and audio glasses
- Earbuds, headphones, and hearing aids
- Stylus pens and computer mouses
- Industrial and medical devices

Features

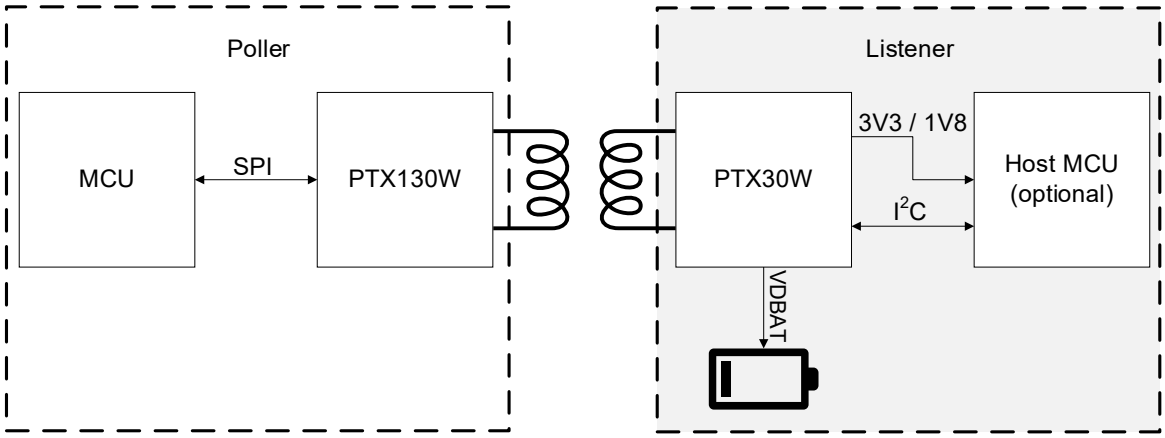
- Highly integrated NFC Wireless Charging Listener device
  - Highly efficient Active Rectifier
  - Up to 1W harvesting power
  - RF interface according to NFC-Forum Type 2 Tag
  - Li-Ion battery charger with charging current from 6mA to 251mA
  - MCU LDO with 1.8V or 3.3V output, up to 50mA
  - Embedded power negotiation logic
- Designed according to NFC Forum Wireless Charging standard
- Custom NFC NDEF feature
- Standalone operation (optional external Host MCU)
- I^2C slave interface
- On-chip overvoltage limiter circuit
- Configurable GPOs

System

The NFC wireless charging system consists of:

- WLC Poller (power transmitter and communication initiator)
- WLC Listener (power receiver)

The NFC wireless charging solution is based on well-established NFC technology operating at 13.56MHz.



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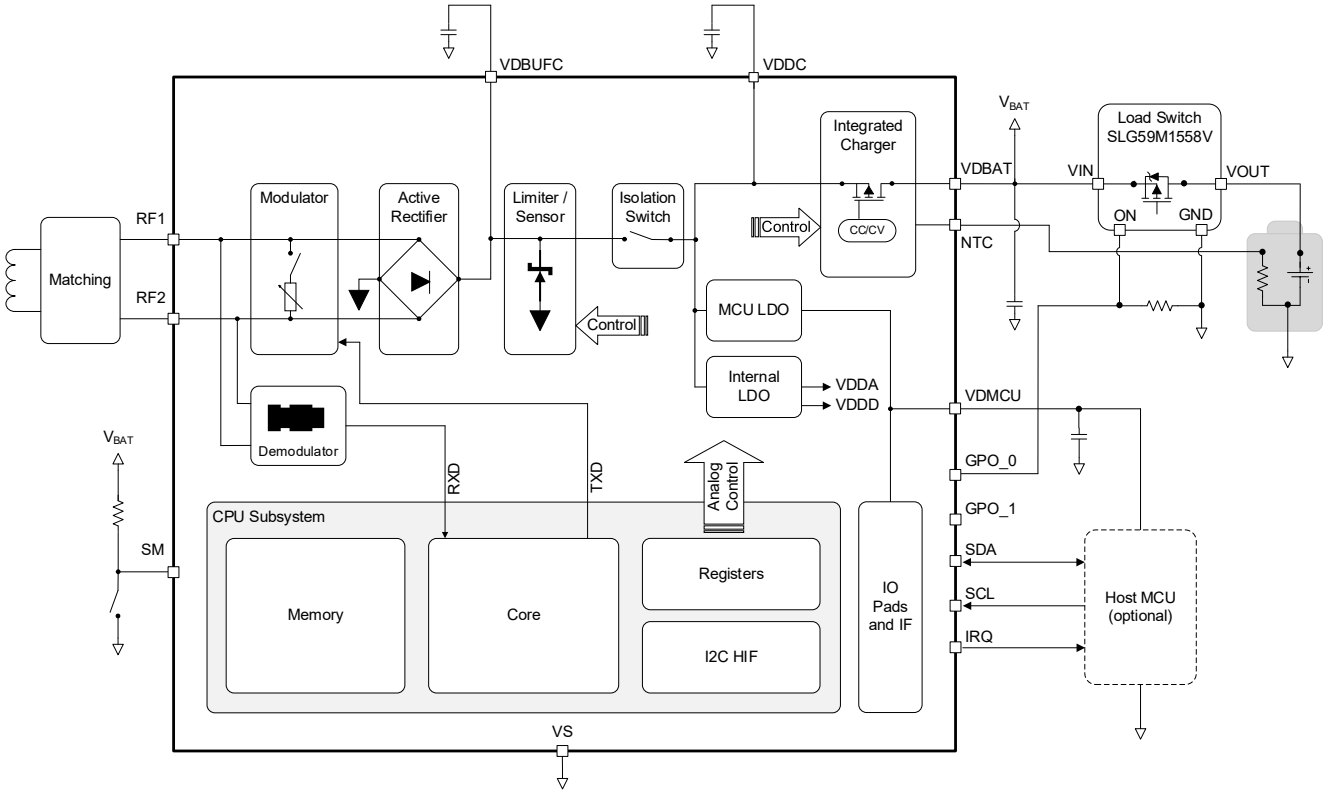


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments

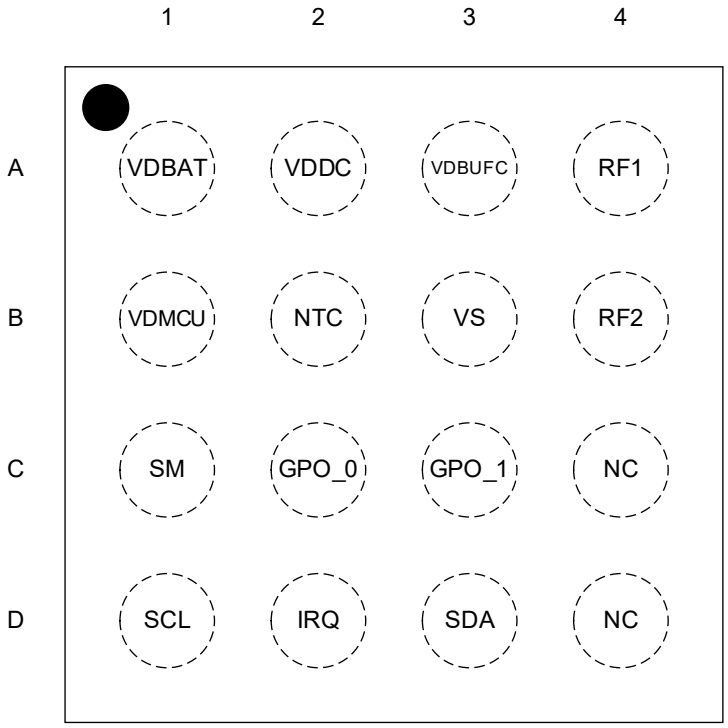


Figure 3. Pin Diagram (Transparent Top View)

2.2 Pin Descriptions

Pin Number	Pin Name	Description
A1	VDBAT	Battery connection (Battery connected with the startup circuit in series).
A2	VDDC	Connection for buffer capacitor and output for system supply.
A3	VDBUFC	Connection for buffer capacitor.
A4	RF1	NFC RF power input. Connected to matching circuit.
B1	VDMCU	MCU LDO output, regulated supply for Host MCU. It is reference voltage for I^2C and GPOs. *Note*: Part type PTX30WCC16D7Ax requires external reference voltage to be provided to the pin.
B2	NTC	Battery thermistor connection.
B3	VS	Reference ground terminal, power return pin.
B4	RF2	NFC RF power input. Connected to matching circuit.
C1	SM	Connection for push-button, to enter/exit shipping mode (active low). Pin requires pull-up resistor with value of 1MΩ connected to VDBAT pin potential. If the SM pin functionality is not used (pin floating) the pull-up resistor is not required.
C2	GPO_0	Configurable General-Purpose Output (open drain, internal pull-up, active low)

Pin Number	Pin Name	Description
C3	GPO_1	Configurable General-Purpose Output (open drain, internal pull-up, active low)
C4	NC	Not connected, leave open
D1	SCL	Serial clock I^2C
D2	IRQ	Dedicated IRQ to Host MCU
D3	SDA	Serial data I^2C
D4	NC	Not connected, leave open

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Max voltage on all Pins	-0.5	+5.5	V
RF input current (RMS)	-	300	mA
Maximum Junction Temperature	-40	+125	°C
Maximum Storage Temperature Range	-40	+150	°C
Human Body Model (Tested per JS-001-2023)	-	2	kV
Charged Device Model (Tested per JS-002-2022)	-	500	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Total allowed long-term power dissipation	-	0.4	W
Ambient Temperature	-40	+70	°C

3.3 Thermal Specifications

Parameter	Package	Symbol	Condition	Typical Value	Unit
Thermal Resistance	WL-CSP16 package	θ_{JA}[1]	Junction to ambient	50	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.

3.4 Electrical Specifications

Values are at T_A = +25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min.[1]	Typ.	Max.[1]	Unit
Battery Charger						
Battery Charging Current Range (during CC phase)	I_{BAT_CC}	OEM configurable parameter	6	-	251	mA
Tolerance of Battery Charging Current during CC Phase, Low Current		< 10mA (OEM configuration) VDDC = 5.2V	-50	-	+50	%
Tolerance of Battery charging current during CC phase, mid current		<= 25mA (OEM configuration) VDDC = 5.2V	-15	-	+15	%
Tolerance of Battery charging current during CC Phase, High Current		> 25mA (OEM configuration) VDDC = 5.2V	-5	-	+5	%
Battery Charging Current during Trickle Charge Phase in Percentage of CC Phase Charging Current	I_{BAT_TRK}	-	-	10	-	%
CV Phase Termination Current Range	I_{BAT_TERM}	OEM configurable parameter	5	-	82	mA
CV Phase Termination Current	-	9.4mA (OEM configuration BC_ITERM_CTRL = 0x07), no load on the VDDC and VDMCU during charging.	5	-	15	mA
CV Phase Termination Current	-	49.7mA (OEM configuration BC_ITERM_CTRL = 0x24), no load on the VDDC and VDMCU during charging.	45	-	55	mA
CV Phase Termination Voltage Range	V_{BAT_TERM}	OEM configurable parameter	3.59	-	4.65	V
CV Phase Termination Voltage Tolerance		-	-1	-	+1	%
Trickle-Charging to CC Phase Voltage Transition Threshold Range	V_{BAT_TRK}	OEM configurable parameter	2.5	-	3.2	V
Trickle-Charging to CC Phase Voltage Transition Threshold Tolerance		-	-5	-	+5	%
Battery Recharge Voltage Threshold Range	V_{BAT_RCHG}	OEM configurable parameter	2.91	-	4.42	V
Battery Recharge Voltage Tolerance		-	-5	-	5	%
Battery Undervoltage Lockout Voltage Range (transition from standby to shipping mode)	V_{BAT_UVLO}	-	2.97	-	3.15	V
Brownout Reset Voltage Thresholds	$V_{VDDC\_BOD\_RESET}$	Power up threshold	2.30	-	3.25	V
	$V_{VDDC\_BOD\_SET}$	Reset threshold	2.2	-	2.8	V

Parameter	Symbol	Test Conditions	Min.[1]	Typ.	Max.[1]	Unit
MOSFET between VDBAT and VDDC ON-Resistance	$R_{DS(ON)}$	-	-	0.2	-	Ω
Current from VDBAT to VDDC	I_{VDDC}	During charging	-	-	I_{BAT_CC} / 2	mA
		During system supply	-	-	250	mA
Current from VDBAT to VDDC (absolute limiting value)	-	During system supply for limited amount of time (t <= 1ms)	-	-	400	mA
Current Consumption						
Standby Current Consumption of the PTX30W	I_{VDBAT_STBY}	No RF field present, no I^2C communication, BC_UVLO_CTRL disabled and MCU LDO disabled, VDBAT = 4.2V, startup circuit pull-up resistor not considered	-	18	-	µA
		No RF field present, no I^2C communication, BC_UVLO_CTRL enabled and MCU LDO disabled, VDBAT = 4.2V, startup circuit pull-up resistor not considered	-	25	-	µA
		No RF field present, no I^2C communication, BC_UVLO_CTRL disabled and MCU LDO enabled, VDBAT = 4.2V, startup circuit pull-up resistor not considered	-	32	-	µA
		No RF field present, no I^2C communication, UVLO enabled (BC_UVLO_CTRL parameter) and MCU LDO enabled, VDBAT = 4.2V, startup circuit pull-up resistor not considered	-	39	-	µA
Shipping Mode Current Consumption	I_{VDBAT_SM}	Leakage current from battery in shipping mode	-	-	100	nA
NTC Monitor Specifications						
NTC Pin Source Current	I_{NTC}	-	62	-	76	µA
NTC Threshold Extreme Cold Flag Set	$V_{NTC\_ECOLD\_SET}$	-	1.77	-	1.795	V
NTC Threshold Cold Flag Set	$V_{NTC\_COLD\_SET}$	-	1.165	-	1.185	V
NTC Threshold Hot Flag Set	$V_{NTC\_HOT\_SET}$	-	0.365	-	0.39	V
NTC Threshold Extreme Hot Flag Set	$V_{NTC\_EHOT\_SET}$	-	0.235	-	0.26	V
NTC Threshold Extreme Cold Flag Reset	$V_{NTC\_ECOLD\_RESET}$	-	1.705	-	1.73	V
NTC Threshold Cold Flag Reset	$V_{NTC\_COLD\_RESET}$	-	1.1	-	1.13	V
NTC Threshold Hot Flag Reset	$V_{NTC\_HOT\_RESET}$	-	0.425	-	0.45	V

Parameter	Symbol	Test Conditions	Min.[1]	Typ.	Max.[1]	Unit
NTC Threshold Extreme Hot Flag Reset	$V_{NTC\_EHOT\_RESET}$	-	0.295	-	0.315	V
Voltage Limiter						
VDDC Pin Voltage	V_{DDC}	-	-	-	5.5	V
VDMCU pin						
VDMCU Pin Output Voltage	V_{DMCU_OUT}	MCU LDO configured as output	1.6	-	3.6	V
VDMCU Output Current	I_{VDMCU}	Current, when MCU LDO is enabled	-	-	50	mA
VDMCU Input Voltage	V_{DMCU_IN}	MCU LDO configured as input	1.6	-	3.6	V
GPOs						
GPO High Output Voltage	V_{GPO_OH}	-	VDMCU - 0.3	-	VDMCU	V
GPO Low Output Voltage	V_{GPO_OL}	-	0	-	0.3	V
GPO Sink and Source Current	I_{GPO_IO}	VDMCU = 3.3V	-	-	8	mA
I^2C						
I^2C High Level Input Voltage	V_{I2C_IH}	-	0.7× VDMCU	-	-	V
I^2C Low Level Input Voltage	V_{I2C_IL}	-	-	-	0.3× VDMCU	V
I^2C Low Level Output Voltage	V_{I2C_OL}	Load current = 8mA, VDMCU = 3.3V	0	-	0.3	V
I^2C Bus Clock Frequency	f_{CLK_I2C}	-	-	-	1	MHz
Voltage Monitor						
VDDC Pin Voltage Monitor Range	V_{MON_VDDC}	-	3	-	5.5	V
VDDC Pin Voltage Monitor Resolution		-	-	12.5	-	mV
VDDC Pin Voltage Monitor Tolerance		-	-50	-	50	mV
VDBAT Pin Voltage Monitor Range	V_{MON_VDBAT}	-	2.4	-	5.5	V
VDBAT Pin Voltage Monitor Resolution		-	-	12.5	-	mV
VDBAT Pin Voltage Tolerance		-	-50	-	50	mV
Thermal Regulation						
Thermal Alert Temperatures	$T_{J\_ALERT\_SET}$	-	-	120	-	°C
	$T_{J\_ALERT\_RESET}$	-	-	100	-	°C

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

4. Functional Description

The PTX30W is a fully integrated NFC wireless charging listener IC that enables NFC power harvesting, NFC communication, battery charging, and wireless charging protocol handling. The NFC interface is based on *NFC Forum Wireless Charging Technical Specification Version 2.0* and *Type 2 Tag Technical Specification Version 1.2*.

In addition to the contactless NFC interface, the PTX30W embeds the I^2C interface, which is intended for initial OEM parameters configuration, read runtime status (RD) parameters, and write runtime (WR) configuration parameters.

Note: Initial OEM configuration can only be done once.

The integrated linear battery charging functionality allows precise charging parameters adjustment, shipping mode, and battery voltage monitoring. The device supports all safety features like overvoltage protection using an embedded limiter circuit, antenna detuning for temperature protection, adjustable voltage limiter on the power path, and battery NTC measurement capability.

The IC supports the following states:

- Power Down – In this state, the PTX30W is not supplied. No battery connected, no RF power and no supply voltage on any other pin (such as. VDDC, VDBUFC).
- Error – Chip came to the state by occurrence of one of the following errors:
  - NTC eCold
  - NTC eHot
  - Battery Disconnect
  - NTC Cold (in combination with BC_ICHG_PCT_COLD param. set to 0%)
  - NTC Hot (in combination with BC_ICHG_PCT_HOT param. set to 0%)
  - Charging timeout

  In this state the charging is stopped, but the chip is still supplied from the battery or NFC. The error flags are indicated to the poller using the WLC Listen Control Record.
- Shipping mode – In this state, the battery supply is disconnected from the internal blocks of PTX30W to minimize discharge from the battery. The chip in that state operates in shipping mode also from power perspective.
- Battery charging and system supply from NFC – In this state, the PTX30W receives the NFC power and supplies the listener's host system using an MCU LDO or directly from the harvesting circuit (VDDC) and at the same time charges the battery using the embedded battery charger.
- System supply from NFC – In this state, the PTX30W receives the NFC power and supplies the system using an MCU LDO or directly from the harvesting circuit (VDDC) but it does not charge the battery. In this state the battery charger functionality (BC_ENABLE parameter) is disabled using the Host interface.
- System supply from Battery (standby mode) – In this state, the PTX30W receives the power from the battery and supplies the system using an MCU LDO or directly from the harvesting circuit (VDDC). In this state the RF field and I^2C detection circuit are enabled. The chip in that state operates in standby mode from power perspective.
- Battery Full – The battery is considered as fully charged in this state. The poller stops providing the WPT cycles (RF power) in this state if the WPT_REQ_SEL parameter is set to 0b00: WPT_REQ controlled by the BC. The chip leaves this state if the battery voltage drops below the recharge voltage level or by BC_ENABLE parameter setting to 0. System is supplied either from the RF power or battery, depending on the availability of the RF power. (For example, WPT_REQ_SEL set to 0b00 would inform the poller to stop the wireless power transfer as the battery is full, so the system is going to be supplied from the battery in that case even though the listener device is placed on the poller).

- Chip Over-Temperature – The PTX30W moves into this state when junction temperature reaches $T_{J\_ALERT\_SET}$. The RF interface is detuned (low ohmic connection between RF1 and RF2 pins) to prevent RF power do dissipate additional power. The chip cannot communicate and receive power from the RF in this state, but it continues to supply the host system from MCU LDO or VDDC pin. State is released when the junction temperature drops below the $T_{J\_ALERT\_RESET}$.

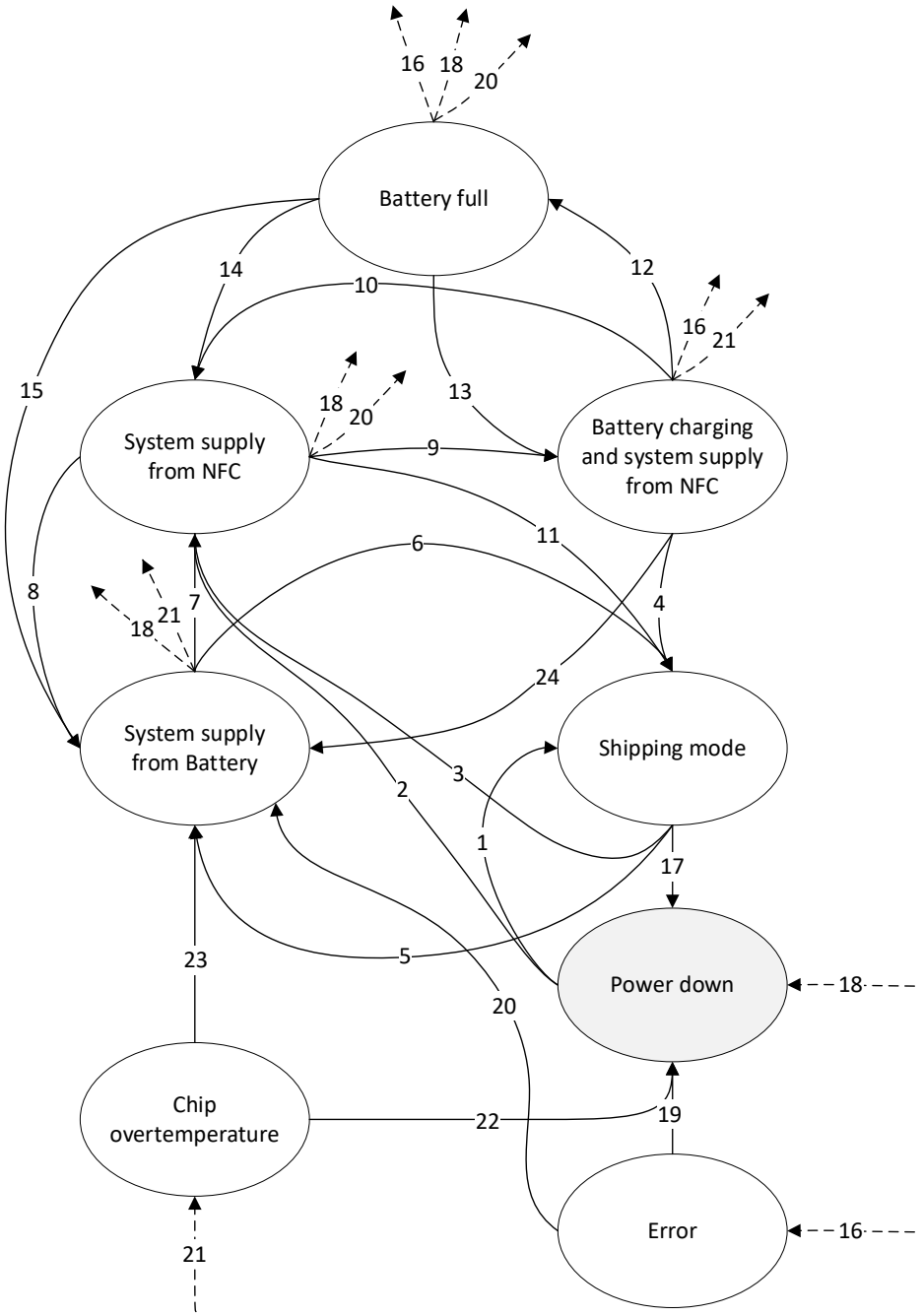


Figure 4. PTX30W State Diagram

Table 1. PTX30W Functional States Transitions

State Transition	Description
1	Initial battery connection to the VDBAT pin
2	RF field appearance (Power received from the antenna) Condition: No battery connected to the VDBAT pin
3	RF field appearance (Power received from the antenna) To stay in the “System supply from NFC state” the Poller shall perform the following procedure: NFC tag activation and NFC wireless charging protocol activation up to WLCL_CTRL NDEF message read from PTX30W. (Protocol activation followed by WLC_CAP message read, followed by WLCP_INFO write from the poller side) The WLCL_CTRL message could request poller for wireless power transfer. If BC_ENABLE OEM parameter is set to 1, the chip moves to the Battery charging and system supply from NFC immediately after NFC WLC protocol activation (above mentioned procedure)
4	RF field removal (if shipping mode enabled using the Host interface upfront, SHIPPING_MODE_ENABLE parameter)
5	SM pin connection to GND for at least 5s (such as SM push button press in application)
6	If of one of the following events occurs: ▪ Battery below VBAT_LOW (if BC_UVLO_CTRL parameter enabled) ▪ Host interface command (SHIPPING_MODE_ENABLE parameter) ▪ >5s SM pin shorted to GND pushbutton press (SM pin)
7	RF field appearance (Power received from the antenna)
8	RF field removal
9	Battery charging enabled (BC_ENABLE parameter set to 1) using the Host interface, additionally NFC WLC protocol activation is required from the Poller side: NFC tag activation and NFC wireless charging protocol activation up to WLCL_CTRL NDEF message read from PTX30W. (Protocol activation followed by WLC_CAP message read, followed by WLCP_INFO write from the poller side) The WLCL_CTRL message could request poller for wireless power transfer
10	Battery charging disabled (BC_ENABLE parameter set to 0) using the Host interface
11	RF field removal (if shipping mode enabled (SHIPPING_MODE_ENABLE parameter) using the Host interface) or the NFC WLC protocol activation has not been performed by the Poller
12	Charging terminated, battery is fully charged
13	Voltage on the battery dropped below recharge level V_{RCHG} (BC_VRCHG_CTRL parameter)
14	Battery charging disabled (BC_ENABLE parameter set to 0)
15	RF field removed and voltage on the battery dropped below recharge level V_{RCHG} (BC_VRCHG_CTRL parameter) or battery charging disable (BC_ENABLE parameter set to 0)

State Transition	Description
16	One of the following errors appears: ▪ NTC eCold ▪ NTC eHot ▪ Battery Disconnect (transition number 16 from Battery full happening only if the RF field is present) ▪ NTC Cold (in combination with BC_ICHG_PCT_COLD param. set to 0%) ▪ NTC Hot (in combination with BC_ICHG_PCT_HOT param. set to 0%) ▪ Charging timeout
17	Battery Disconnect
18	Battery Disconnect (transition number 18 from Battery full can only happen if the RF field is not present)
19	RF field removal Condition: Battery disconnected
20	RF field removal Condition: battery connected
21	Junction temperature of the chip reached above the $T_{J\_ALERT\_SET}$
22	RF field removal, caused by detuning of the RF pins of PTX30W. Condition**:** Battery disconnected
23	Junction temperature dropped below the $T_{J\_ALERT\_RESET}$ Condition: Battery connected
24	RF field removal

4.1 RF Interface and Power Harvesting

Starting at the antenna coil, which connects through the matching circuit to the RF1 and RF2 device pins, the RF signal passes through a high-efficient rectifier circuit. The rectifier is responsible for turning 13.56MHz RF power received on the inductive antenna into DC power used for battery charging and system supply.

The resulting DC output power is stored in a buffer capacitor connected to the VDBUFC device pin. This capacitor powers the analog circuit during modulation because the RF signal is modulated by the poller during NFC communication.

In NFC, the tag communicates with the NFC Poller (NFC reader) using load modulation. This is achieved by the Modulator modulating the connection between RF1 and RF2. The Modulator is responsible for passive load modulation.

The NFC Poller (NFC reader) communicates with the NFC tag using amplitude modulation according to NFC Type A ISO/IEC14443 parts 2 and 3 at 106kbit/s. The Demodulator detects the envelope of the incoming RF signal and passes the resulting demodulated signal to the digital modem for decoding.

4.2 Host System Supply

The host system can be supplied using the VDMCU or VDDC pins. VDMCU is regulated by the integrated MCU LDO and outputs depending on the OEM configuration or the part number (1.8V or 3.3V output). For certain product variant (PTX30WCC16D7A2) the VDMCU pin requires external supply which serves as a reference for interfaces (GPOs and I2C interface). Note that PTX30WCC16D7A2 could be reconfigured using OEM parameter to 1.8V or 3.3V. The VDDC pin holds the BOD circuit (brownout detection) which would reset the PTX30W if the voltage on the pin drops below the VVDDC_BOD_SET. If the host system connected to the VDDC relies on the

RF power, the voltage on the VDDC can drop (possible causes: suddenly increased current consumption on the VDMCU and VDDC, change of the coupling between poller and listener antenna and the poller output power drop). That problem cannot occur while battery provides enough voltage to stay above the BOD level.

4.3 Overvoltage Protection

The final block in the power harvesting stage is the over-voltage Limiter. The primary purpose of the limiter is to limit the rectifier output voltage to a value below the maximum allowed voltage of the transistors and in that way protect the succeeding blocks from overvoltage.

This Limiter is essentially a programmable shunt regulator, limiting the voltage on the output of the rectifier generated by the field. An inbuilt current sensor senses the current being shunted in the Limiter.

The Limiter acts as the first point of protection for the device, able to shunt large excess currents to ground. It also provides ESD protection for the device. Longer-term overcurrent must be avoided to prevent the device from overheating. Longer-term overload protection is provided by the detuning circuit.

4.4 Battery Charger

The power harvesting side of the PTX30W is connected to the local power management system using an isolation switch. It is switched off to minimize losses when the local power management system is running on battery power.

For simple, highly integrated systems, a flexible Integrated Li-Ion charger circuit is integrated. The integrated battery charger is designed to charge a wide range of Lithium-Ion batteries. The integrated battery charger has the following properties.

- Programmable:
  - I_{CHG} charging current – 6mA to 251mA in 2mA steps (BC_ICHG_CTRL parameter)
  - V_{TERM} termination voltage – 3.6V to 4.65V (BC_VTERM_CTRL parameter)
  - $I_{TRICKLE}$ trickle charge current – 10% of I_{CHG} (not programmable parameter)
  - $V_{TRICKLE}$ trickle charge voltage threshold – 2.5V to 3.2V (BC_VTRK_CTRL parameter)
  - I_{TERM} termination current – 5mA to 82mA (BC_ITERM_CTRL parameter)
  - V_{RCHG} recharge voltage threshold – 2.9V to 4.4V (BC_VRCHG_CTRL parameter)
- Voltage and charging status monitor
- Dynamic power management
- Thermal shutdown and battery NTC monitor
- Battery undervoltage, short, overcurrent protection
- Supports ultra-low-leakage Shipping Mode

The charger implements all the necessary charger features, including:

- Shipping mode completely isolates the battery from the rest of the system while the product is being shipped.
- Shipping mode can be activated by one of the following actions:
  - Battery voltage dropping below $V_{BAT\_LOW\_TH}$ (3V)
  - Host interface command (SHIPPING_MODE_ENABLE parameter)
  - Short SM pin to ground for >5 seconds
- Shipping mode can be deactivated by one of the following:
  - RF field appearance and wireless charging protocol activation (WLCL_CTL command read)
  - Short SM pin to ground for >5 seconds
- Trickle charge mode, which is activated at low battery voltage to precondition the battery ready for fast charge.
- The constant current mode, which is activated above the trickle charge voltage threshold and below the terminal voltage threshold.

- Constant voltage mode, which is activated when the battery reaches the termination battery voltage. Charging is stopped at a programmable termination current.

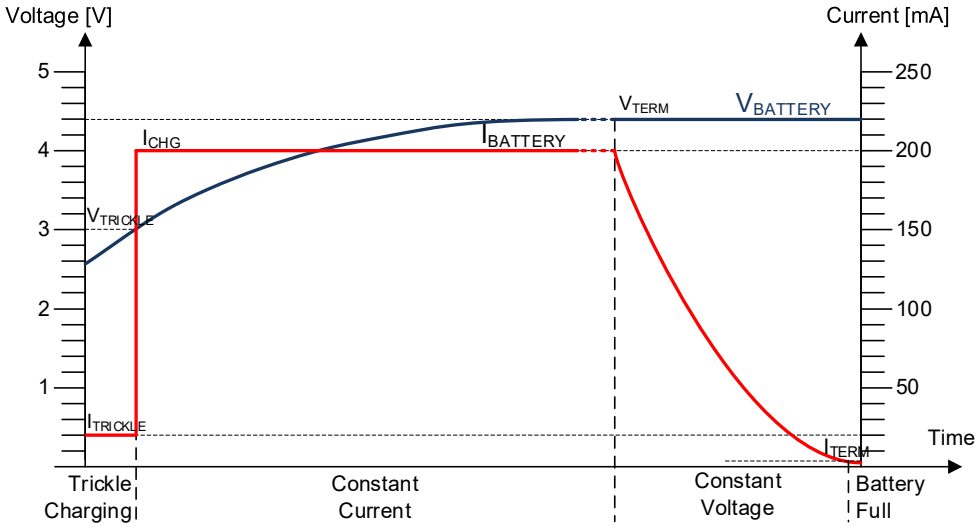


Figure 5. Typical Lithium-Ion Battery Charging Curve

Integrated battery charger allows many system benefits to be realized. The charger circuit provides several parameters to the digital core.

The parameters from the battery charger are used to negotiate for more or less power from the poller side depending upon the needs of the battery charger, therefore, fully optimizing the end-to-end efficiency during the charging cycle.

4.4.1 Startup Circuit

PTX30W requires a mandatory startup circuit connected between the battery and VDBAT pin of the PTX30W. Startup circuit consist of two MOSFET switches and ensures connection of the battery once stable conditions are meet. More information about the startup circuit implementation can be found in the *PTX30W startup circuit* application note.

4.4.2 Temperature Sensing on NTC

The NTC pin of PTX30W is used for temperature sensing, typically using NTC resistor connected between NTC pin and ground. Connection of the NTC resistor is mandatory to run the battery charger. A resistor with value of 10kΩ might be connected to NTC pin if temperature sensing functionality is not used.

The NTC pin senses the voltage and switches between the following temperature ranges:

- Extreme cold temperature (typically below 0°C),
- Cold temperature (typically below 10°C),
- Hot temperature (typically above 45°C) and
- Extreme hot temperature (typically above 60°C).

The charger adjusts charging according to the temperature range.

- Normal temperature range (typically above 10°C and below 45°C) – The charger operates with BC_ICHG_CTRL parameter configured charging current and BC_ICHG_CTRL parameter configured termination voltage.
- Cold temperature range (typically below 10°C) – The charger operates with BC_ICHG_PCT_COLD parameter configured charging current and BC_VTERM_OFFSET_COLD parameter configured termination voltage. If

BC_ICHG_PCT_COLD is set to 100b (0mA), the charging process is stopped, and battery temperature error is reported to the poller.

- Extreme cold temperature range (typically below 0°C) – The charging process is stopped, and temperature error reported to the poller.
- Hot temperature range (typically above 45°C) – The charger operates with BC_ICHG_PCT_HOT parameter configured charging current and BC_VTERM_OFFSET_HOT parameter configured termination voltage. If BC_ICHG_PCT_HOT is set to 100b (0 mA), the charging process is stopped, and the battery temperature error is reported to the poller.
- Extreme hot temperature range (typically above 60°C) – The charging process is stopped, and temperature error reported to the poller.

Note: Actual temperature thresholds and hysteresis are recalculated based on actual β value and voltage thresholds (see Electrical Specifications).

Proposed NTC thermistor type: R = 10kΩ and β = 3435 (typical), β value depends on the required temperature thresholds. Renesas recommends adding a serial resistor for finetuning between NTC pin and NTC connection on the battery.

Table 2: Example of Temperature Thresholds for NTC B = 3435 without Serial Resistance

Temperature Range	Set / Reset	Nominal Temperature Threshold (°C)
Extreme cold	Set	2
	Reset	3
Cold	Set	12
	Reset	13
Hot	Set	42
	Reset	37
Extreme hot	Set	54
	Reset	48

4.5 System Supply

The VDDC node is powered either from the RF power harvesting side or a connected battery. Additionally, the VDDC powers the MCU LDO, which provides regulated voltage levels and is designed to power an external Host MCU.

The system can be powered from the PTX30W using the following nodes:

- VDDC pin – Voltage is not regulated but defined by the poller side output power. During charging the voltage, typically follows the battery voltage with additional headroom, and the limits are defined by the maximum voltage of the limiter (5.2V typical) and battery voltage as minimum and
- VDMCU pin – Regulated voltage (1.8V, 3.3V or externally supplied).

Note: Power required by the host system (on VDDC and VDMCU) at the start-up is lower than power provided by the initial power step by the poller.

4.5.1 Power Source Selection

The Power selector feature dynamically handles power sourcing between RF power harvesting and battery.

No system supply (no current consumption on VDMCU / VDDC):

- When the current provided from the RF power harvesting is lower than the programmed charging current, the battery is charged with the available current.

System supply (current consumption on VDMCU / VDDC)

- When the current provided from the RF power harvesting side is lower than the current required for the system and programmed battery charging current, the system supply gets priority, and the battery is charged with residual current from the RF power harvesting,
- When the system supply current exceeds the RF power harvesting available current, the battery provides additional current for the system supply,
- When the battery is fully charged:
  - WPT_REQ_SEL = 00b: Protocol stops WPT requests (power on the RF power harvesting disappears), the system is supplied from the battery.
  - WPT_REQ_SEL = 10b: Protocol continues WPT requests, the system remains supplied from the RF power harvesting.
- When there is no current available from the RF power harvesting, the system supplies it from the battery.

4.6 Protocol

Wireless charging protocol is implemented based on the embedded Core. The CPU is a small low-power Harvard architecture RISC design supported by non-volatile program memory and volatile data memory. Several hardware assist features are added to offload many of the required real-time functions from the CPU. Together they form a highly efficient NFC core system. The CPU is designed to spend most of its time asleep, waking only when prompted by external stimuli or the very low-frequency system timer. The firmware, which is running on the core, is fixed.

The core handles protocol implementation according to mandatory features specified in *NFC Forum Wireless Charging Technical Specification Version 2.0*, including power negotiation. PTX30W works as a wireless charging listener in negotiated or static charging mode.

Negotiated wireless charging protocol consists of the following states:

- NFC LE (Link Establishment)
  - NFC activation according to Type 2 Tag activation.
- WCCA (Wireless Charging Control Activation)
  - Poller reads the WLC_CAP message from the PTX30W.
- WCC (Wireless Charging Control)
  - Poller writes the WLCP_INFO message to the PTX30W.
- Negotiated WPT (Wireless Power Transfer)
  - Poller reads WLCL_CTL message from the PTX30W.

Power is negotiated based on the needs of the battery charger. The regulation loop is targeting the minimum voltage difference between VDDC and VDBAT nodes, to keep losses inside PTX30W low.

NDEF messages used in Wireless Charging Protocol:

- WLC_CAP
  - Protocol version
  - Charging mode (negotiated / static)
  - Waiting times
- WLCP_INFO
  - Last wireless transfer power level
  - WLC Poller capability
  - WLC Poller power class

- Information for power regulation (number of power steps, current power step…)

- WLCL_CTL
  - Requests for wireless power transfer (WPT) phases
  - WPT duration
  - WPT_DURATION_INT parameters, which define the duration for different charging states.
  - Battery level
  - Power adjustment request

4.6.1 Charging Process

A typically Lithium-Ion battery has three different charging modes depending on the level of charge the battery has:

- Trickle Charge Mode (TCM),
- Constant Current Mode (CCM), sometimes also referred to as Fast-Charge Mode
- Constant Voltage Mode (CVM)

For each of these modes, different charging parameters may be used. Figure 6 shows an example of a charging process. *Note*: The NFC communication that takes place between the WPT cycles is not shown in Figure 6.

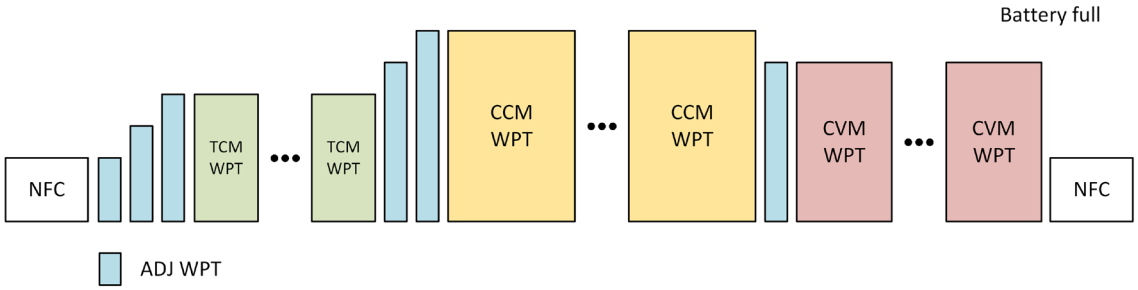


Figure 6. Example Charging Process with Different WPT Durations

Initially, and every time the listener device detects that an input power must be adjusted, it asks for an ADJ_WPT cycle to quickly regulate its input power to an optimum level. When the input power has been adjusted, the listener increases the length of the WPT cycle according to the charging mode (TCM, CCM, or CVM). *Note*: The duration of the WPT cycles shown in Figure 6 is configurable using the following parameters:

- ADJ_WPT_DURATION_INT
- TCM_WPT_DURATION_INT
- CCM_WPT_DURATION_INT
- CVM_WPT_DURATION_INT

4.6.1.1 Power Regulation Loop

The PTX30W optimizes the charging process by continuous power regulation based on power adjustment requests in WLCL_CTL message.

The power regulation generates power adjustment requests based on the needs of the battery charger during the charging process.

- Power regulation limits during system supply:

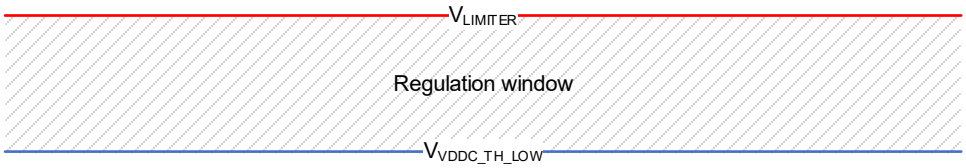


Figure 7. Power Regulation Window for System Supply

- Power regulation limits during constant current charging mode:

  For low voltage on the battery, the $V_{VDDC\_TH\_LOW}$ threshold is considered for regulation. Do not set $V_{VDDC\_TH\_LOW}$ lower than 3V.

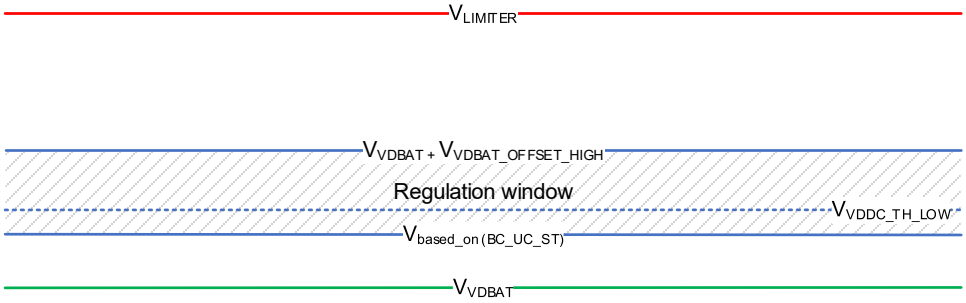


Figure 8. Power Regulation Window for the Constant Current Mode

- Power regulation limits during constant voltage and trickle charge mode:

  For low voltage on the battery, the $V_{VDDC\_TH\_LOW}$ threshold is considered for regulation. Do not set $V_{VDDC\_TH\_LOW}$ lower than 3V.

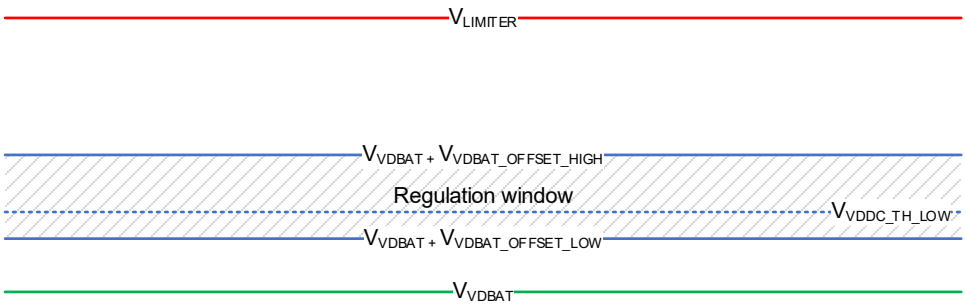


Figure 9. Power Regulation Window for Constant Voltage and Trickle Charge Mode

The firmware version 5123 introduces additional OEM parameter LIM_TH_SEL, which is used for improvement of the charging current stability in the CV charging mode. Set the LIM_TH_SEL parameter to the closest available setting that is more than 500mV above the BC_VTERM_CTRL. For example, if the BC_VTERM_CTRL is set to 0x14: 4.29V, set LIM_TH_SEL to 4.8V.

Note: CV termination current accuracy can be impacted if the BC_VTERM_CTRL and LIM_TH_SEL is set too far apart.

4.6.2 Transparent Data Channel (TDC)

This section describes the Transparent Data Channel (TDC) to exchange arbitrary data between poller and listener devices in both directions. The protocol is based on a shared memory mechanism and uses the T2T memory organization to store data.

Two 64-byte buffers are used to transfer data between the poller and listener devices. TDC_BUF_POL sends data from the poller to listener, and TDC_BUF_LIS sends data in the other direction.

Data must be encapsulated in NSC_DATA_MSG format.

Note: PTX30W keeps the battery charger activated during data transfer, typically the charging power is reduced.

4.6.2.1 Data Transfer from Poller to Listener using NFC Forum T2T Commands

Figure 10 shows a data transfer of 70 bytes (Data [0:69]) from poller to listener Host using standard NFC Forum T2T read and write commands. Because the data exceeds the size of the TDC_BUF_POL buffer (64-bytes), it is split into two parts.

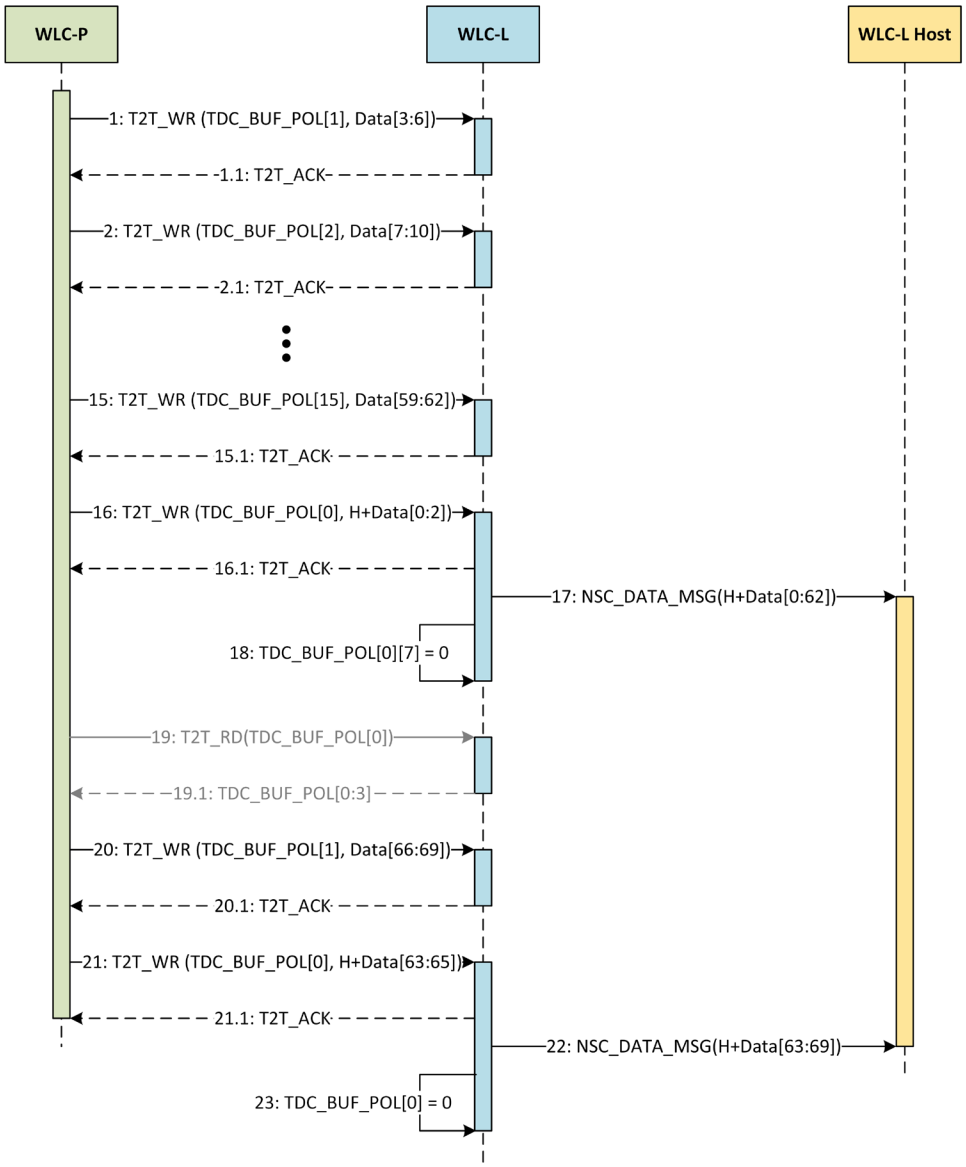


Figure 10. TDC: Data Transfer from Poller to Listener using T2T Commands

- Steps 1 through 16 – Poller writes H[1]+Data[0:62] to TDC_BUF_POL buffer using NFC Forum T2T WRITE commands. *Note*: The first block of the buffer (H[1]+Data[0:2]) must be written at the end (Step 16) to indicate

that the transfer is complete. Each successful write is acknowledged by an NFC Forum T2T acknowledge. If an error occurs, the poller may retransmit the last block.

- Step 17 – When the first block of TDC_BUF_POL is written, the listener forwards the data to the Host using an NSC_DATA_MSG.
- Step 18 – After the NSC_DATA _MSG has been read by the Host, the listener sets the first byte of TDC_BUF_POL[0] to 0, indicating to the poller that the buffer is free for the next data message.
- Step 19 (optional) – The poller periodically reads the first block of TDC_BUF_POL to check if the buffer is free to send the next data message.
- Steps 20 through 21 – The poller writes the second part of the message to the TDC_BUF_POL (H^1+Data[63:69], again writing the first block at the end (Step 21).
- Step 22 – The listener forwards H^1+Data[63:69] to the Host using an NSC_DATA_MSG message.
- Step 23 – When the NSC_DATA_MSG has been read by the Host, TDC_BUF_POL[0] is set to 0.

4.6.2.2 Data Transfer from Poller to Host using Proprietary PTX NFC Commands

Figure 11 shows a sequence to transfer 70 bytes of data from the poller to the listener Host using proprietary PTX NFC commands.

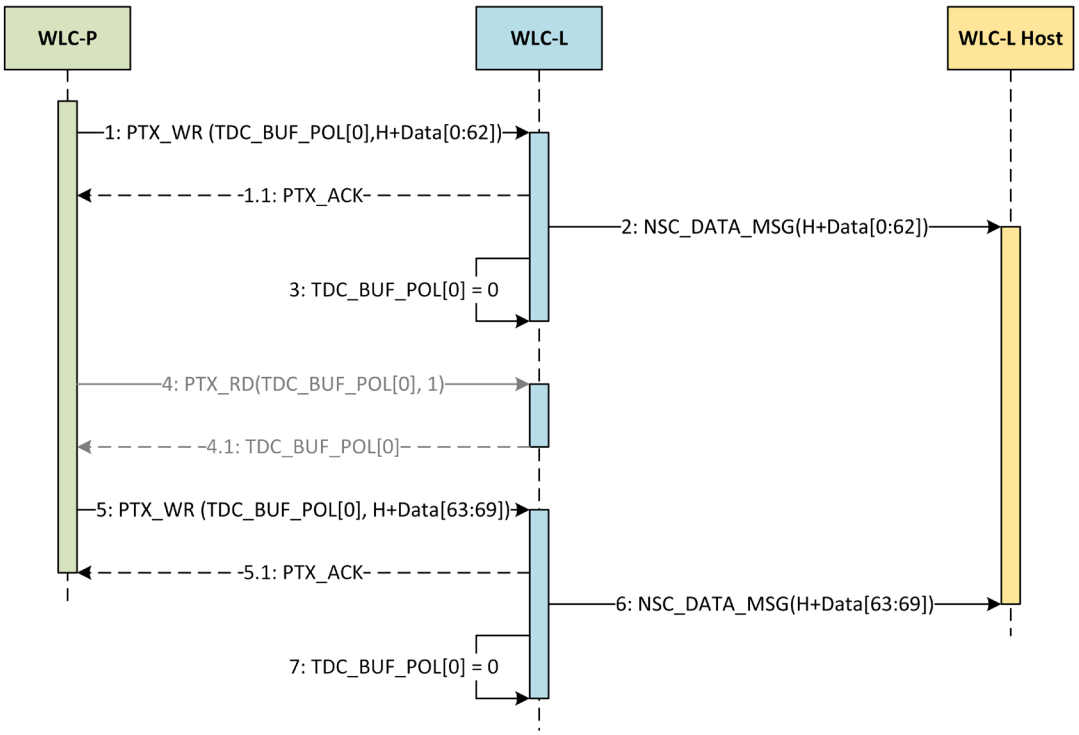


Figure 11. TDC: Data Transfer from Poller to Listener using PTX Commands

- Step 1 – The poller writes H^1+Data[0:62] to TDC_BUF_POL buffer using a proprietary PTX write command. The successful Write is acknowledged by a PTX Acknowledge. If an error occurs, the poller may retransmit the data.
- Step 2 – The listener forwards the data to the Host using an NSC_DATA_MSG message.
- Step 3 – After the NSC_DATA _MSG has been read by the Host, the listener sets the first byte of TDC_BUF_POL[0] to 0, indicating to the poller that the buffer is free for the next data message.
- Step 4 (optional) – The poller periodically reads the first block of TDC_BUF_POL to check if the buffer is free to send the next message.
- Step 5 – The poller writes the second part of the message to the TDC_BUF_POL (H^1+Data[63:69], again writing the first block at the end (Step 21).

- Step 6 – The listener forwards H[1]+Data[63:69] to the Host using an NSC_DATA_MSG message.
- Step 7 – When the NSC_DATA_MSG has been read by the Host, TDC_BUF_POL[0] is set to 0.

4.6.2.3 Data Transfer from Listener to Poller using NFC Forum T2T Commands

An example of a sequence to transfer 70-byte data from the listener Host to the poller is shown in Figure 12.

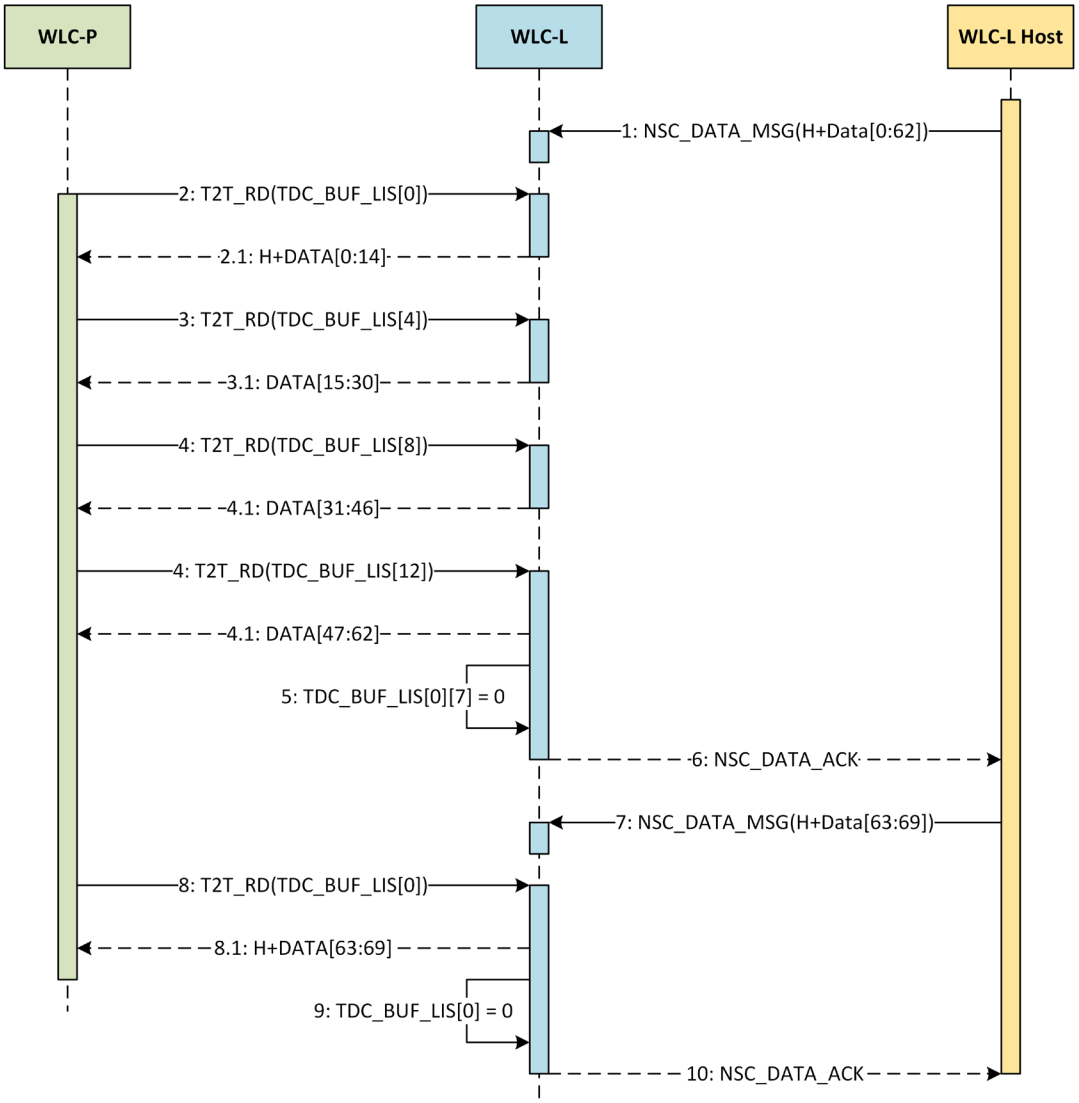


Figure 12. TDC: Data Transfer from Listener to Poller using T2T Commands

- Step 1 – The listener Host sends an NSC_DATA_MSG with H[1]+Data[0:62] payload to listener. The listener copies the data to the TDC_BUF_LIS buffer.
- Steps 2 through 4 – The poller reads the data from the buffer using NFC Forum T2T read commands. *Note*: The poller periodically checks the status of the TDC_BUF_LIS buffer. If TDC_BUF_LIS[0][7] bit is set, the buffer contains a valid message.
- Step 5 – After the last block of the message has been read (Step 4), the listener clears the buffer by setting TDC_BUF_LIS[0][7] to 0.
- Step 6 – The listener sends NSC_DATA_ACK to the Host indicating that it may send the next NSC_DATA_MSG.
- Step 7 – The listener Host sends the second NSC_DATA_MSG (H[1]+Data[63:69]) to the listener.
- Step 8 – The poller reads the second message using one NFC Forum T2T read command.
- Step 9 – The listener clears TDC_BUF_LIS[0][7] bit.

- Step 10 – The listener sends NSC_DATA_ACK to the Host finishing the second transaction.

4.6.2.4 Data Transfer from Host to Poller using Proprietary PTX NFC Commands

Figure 13 shows a data transaction of 70 bytes between the listener Host to poller device.

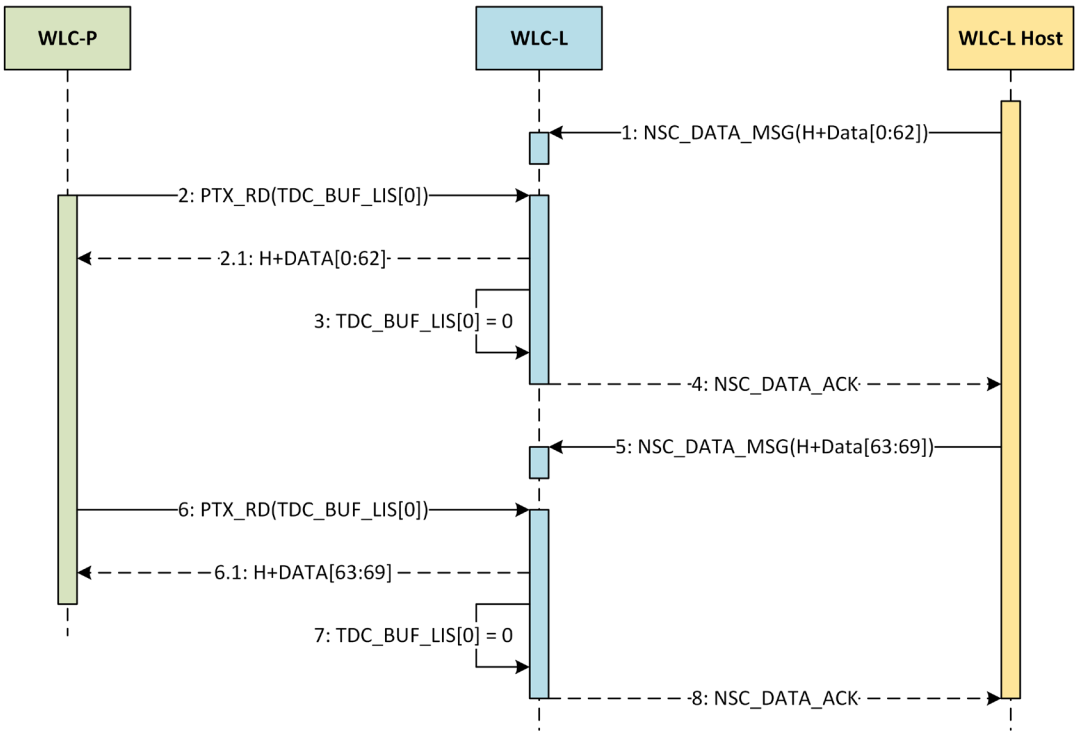


Figure 13. TDC: Data Transfer from Listener to Poller using PTX Commands

- Step 1 – The listener Host sends an NSC_DATA_MSG with H[1]+Data[0:62] payload to listener. Listener copies the data to TDC_BUF_LIS buffer.
- Steps 2 through 4 – The poller reads the data from the buffer using a proprietary PTX NFC read command. *Note*: The poller periodically checks the status of the TDC_BUF_LIS buffer. If the TDC_BUF_LIS[0][7] bit is set, the buffer contains a valid message.
- Step 5 – After the last block of the message has been read (Step 4), the listener clears the buffer by setting TDC_BUF_LIS[0][7] to 0.
- Step 6 – The listener sends NSC_DATA_ACK to the Host indicating that it may send the next NSC_DATA_MSG.
- Step 7 – The listener Host sends the second NSC_DATA_MSG (H[1]+Data[63:69]) to listener.
- Step 8 – The poller reads the second message using one proprietary PTX NFC read command.
- Step 9 – The listener clears the TDC_BUF_LIS[0][7] bit.
- Step 10 – The listener sends NSC_DATA_ACK to the Host finishing the second transaction.

4.7 NFC Interface

The NFC interface of PTX30W operates according to the standards listed in Table 3.

Table 3. NFC Interface Standards

	NFC Forum	ISO/IEC
Modulation, coding, frames, and activation command set	*Digital Protocol Technical Specification*	ISO/IEC14443-2 and ISO/IEC14443-3
State diagram	*Type 2 Tag Operation Technical Specification*	
Memory structure and management, command set	*Type 2 Tag Operation Technical Specification*	

NFC is typically communication between two devices one being the poller device and the other is the listener device. The Poller device generates an alternating current that passes through the primary coil and creates a magnetic field that is induced in the secondary coil which powers the listener device.

Table 4. Coding and Modulation Types

	Poller	Listener
Renesas NFC device	PTX130W	PTX30W
Modulation	ASK, 100% modulation	Load modulation with On-Off Keying of subcarrier modulation (847.5kHz)
Coding	Modified Miller	Manchester

4.7.1 Unique Identifier

The PTX30W implements all data integrity and measures like parity and 16-bit CRC as specified by the NFC forum specifications.

The device implements a fixed 7-byte UID where the first byte (UID0) is fixed to the value of 20h - the manufacturer ID for Renesas in accordance with *ISO/IEC 14443-3*.

4.7.2 NFC Commands

PTX30W implements the following standard commands from the NFC interface perspective:

Table 5. PTX30W Standard NFC Commands

NFC Forum	ISO/IEC14443	Command
SENSE_REQ	REQA	26h
ALL_REQ	WUPA	52h
SDD_REQ CL1	ANTICOLISION CL1	93h 20h
SEL_REQ CL1	SELECT CL1	93h 70h
SDD_REQ CL2	ANTICOLISION CL2	95h 20h
SEL_REQ CL2	SELECT CL2	95h 70h

NFC Forum	ISO/IEC14443	Command
HLTA	SLP_REQ	50h 00h
READ	-	30h
WRITE	-	A2h
SECTOR SELECT	-	C2h

The PTX30W implements additional proprietary commands for fast data exchange between the poller and listener:

4.7.2.1 PTX Read

The PTX Read command reads an arbitrary number of blocks [NoB] from the T2T memory starting at the address [Addr]. Figure 14 describes the command format.

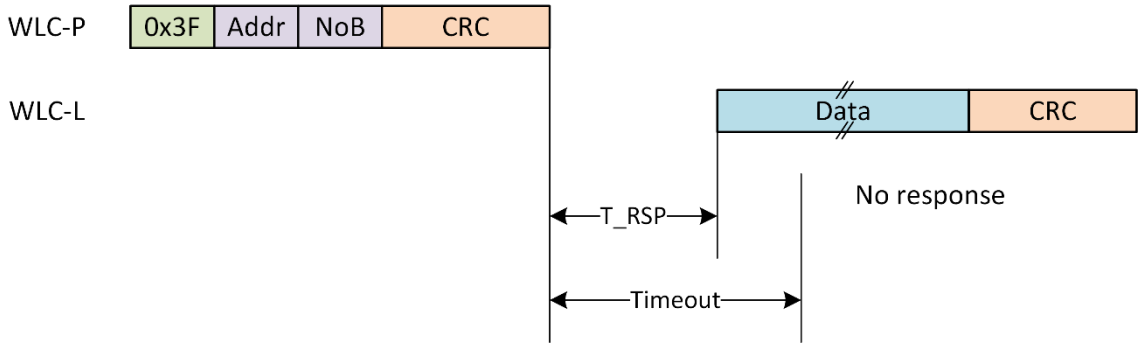


Figure 14. PTX Read Command

Table 6. PTX Read Command

Parameter	ISO/IEC14443	Command
0x3F	1 byte	Command opcode
Addr	1 byte	Read block address
NoB	1 byte	Number of blocks to read
CRC	2 bytes	CRC according to NFC-A technology
Data	N bytes	Read data

Table 7. PTX Read Command, Timings

Parameter	Value	Description
T_RSP	Maximum time in which the listener provides a response data.	10ms
Timeout	Maximum time the poller waits for a response data.	25ms

Parameter	Value	Description
NoB	1 byte	Number of blocks to read

4.7.2.2 PTX Write

The PTX Write command writes an arbitrary number of blocks to the T2T memory. Figure 15 shows the command format.

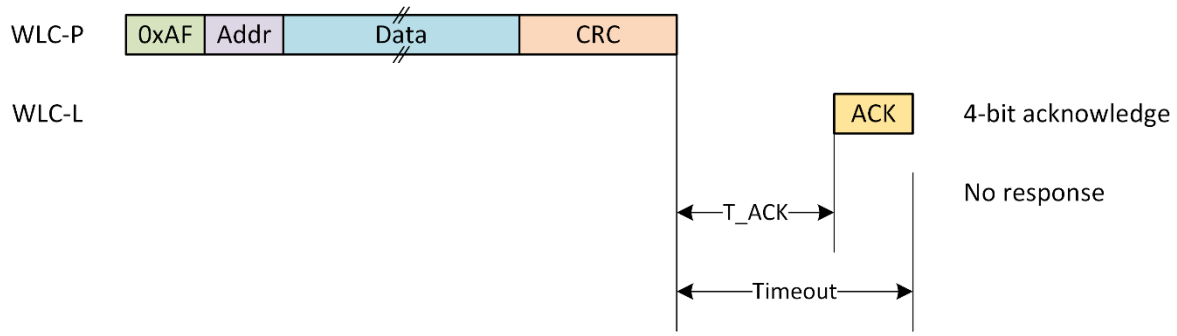


Figure 15. PTX Write Command

Table 8. PTX Write Command

Parameter	Value	Description
0xAF	1 byte	Command opcode.
Addr	1 byte	Write block address.
Data	N bytes	Write data. Minimum is 4 bytes; number of bytes is multiple of 4. (N = 4,8,12…)
CRC	2 bytes	CRC according to NFC-A technology.
ACK	4 bits	Acknowledge (0xA)

Table 9. PTX Write Command, Timings

Parameter	Value	Description
T_ACK	10ms	Maximum time in which the listener provides an acknowledge.
Timeout	25ms	Maximum time the poller waits for a response data.

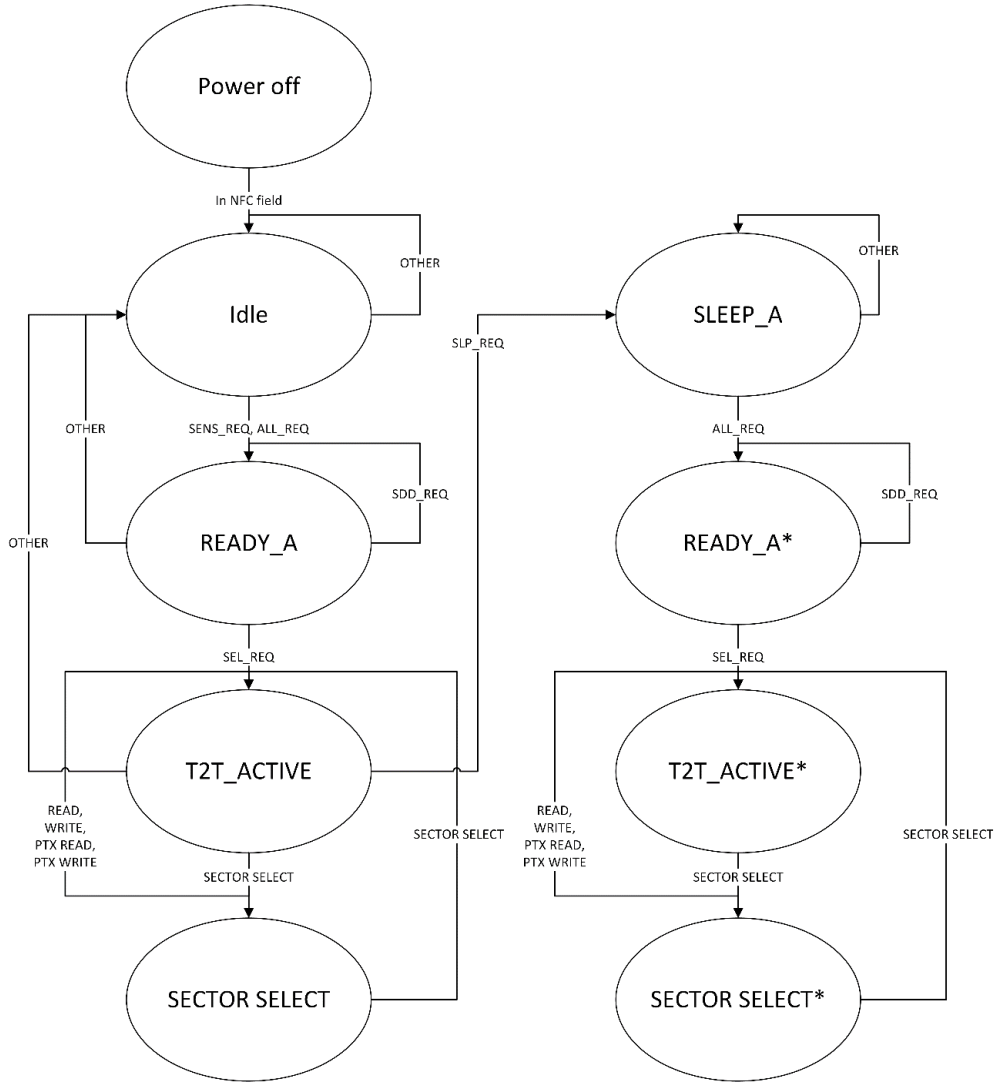


Figure 16. PTX30W NFC Interface State Machine

4.7.3 Memory Structure

PTX30W uses a dynamic T2T memory structure with 168 bytes reserved for an NDEF message and additional 68 bytes reserved for a transparent data channel (TDC) protocol. Table 10 shows an example of the memory layout with some fixed values. For more information, please refer to the *NFC Forum T2T Technical Specification*.

Table 10. PTX30W Memory Structure

Parameter	Byte 0	Byte 1	Byte 2	Byte 3
Block 0	Internal	Internal	Internal	Internal
Block 1	Internal	Internal	Internal	Internal
Block 2	Internal	Internal	StatLock_0	StatLock_1
Block 3	CC_0 = E1h Indicates T2T device	CC_1 = 10h Version = 1.0	CC_2 = 21 T2T_Area = 168B	CC_3 = 00h Access Conditions
Block 4	NDEF_TLV = 03h	TLV length	NDEF record header	…
Block 5	…	…	…	…

Parameter	Byte 0	Byte 1	Byte 2	Byte 3
…	…	…	…	…
Block 45	…	…	…	Byte 167
Block 46	DynLock_0	DynLock_1	Reserved	Reserved
Block 47	GPO_0	GPO_1	Reserved	Reserved
Block 48	TDC_BUF_POL_0	…	…	…
…	…	…	…	…
Block 63	…	….	….	TDC_BUF_POL_63
Block 64	TDC_BUF_LIS_0	…	…	…
…	…	…	…	…
Block 79	…	…	…	TDC_BUF_LIS_63
Block 80	NTC_STATUS	Reserved	Reserved	Reserved
Block 81	Reserved	Reserved	Reserved	Reserved
Block 82	Reserved	Reserved	Reserved	Reserved
Block 83	Reserved	Reserved	Reserved	Reserved

The first 10 bytes (Internal bytes) are reserved for manufacturing information. The next two bytes (StatLock_*) lock certain parts of the memory.

- Block 3 – This block is called Capability Container (CC) and contains the information for reading and writing NDEF messages.
- Blocks 4 to 45 – These blocks are reserved for NDEF messages. The area consists of an NDEF message TLV (03h), followed by a Terminator TLV (FEh). The unused area is left undefined.
- Block 46 – This block holds information about Dynamic Lock Bits.
- Block 47 – This block provides a mechanism to control the GPO pads. Setting and resetting of a GPO is enabled by writing to the GPO_0 and GPO_1 bytes in the memory. Writing 0x01 to the byte sets the GPO (active low logic of the GPO; 0x01 - GPO low, 0x00 - GPO pulled high using embedded pull-up)
- Blocks 48 to 63 – These blocks are reserved for the TDC protocol; to transfer data from a poller to a listener (TDC_BUF_POL).
- Blocks 64 to 79 – These blocks are reserved for the TDC protocol; to transfer data from a listener to a poller (TDC_BUF_LIS).
- Block 80 – The first byte of Block 80 provides the NTC_STATUS information.

4.7.4 Custom NDEF Record

The user has the possibility to define a custom NDEF record of a maximum size of 144 bytes. The record is added at the beginning of the NDEF message together with the WLC_CAP NDEF record. During a charging process, the custom NDEF record is not be part of the NDEF message.

The custom NDEF record is formatted according to the *[NDEF] specification* and does not exceed 144 bytes. The MB (Message Begin) flag is set to 1, and the ME (Message End) flag is set to 0.

Custom NDEF message can be provided using CUSTOM_NDEF_MSG and CUSTOM_NDEF_MSG_LEN parameters.

4.8 Host Interface

PTX30W uses an I²C Host Interface and supports the following features:

- I²C target device
- Fast mode, up to 1Mbit/s
- 7-bit addressing

The PTX30W Host interface layering:

- NSC command
- (HIP) Host interface protocol frame
- I²C frame

An I²C frame composition example is shown in the I²C interface chapter.

4.8.1 Host Interface Parameters

- OEM Parameters – Written by a customer/OEM during the customization or personalization process and cannot be overwritten (one-time programmable). *Note*: Functionality of the chip is limited without the OEM parameter configuration.
- RD Parameters – Read by Host MCU during operation. RD parameter read returns actual value, values set by WR, if existing, otherwise it returns value set during OEM configuration (if parameter has an OEM value).
- WR Parameters – Written by Host MCU during operation; however, the changes are lost when the device is reset (device state is lost in shipping mode)

Before the OEM configuration, the chip functions with the default OEM values.

Table 11. Host Interface Parameters

Parameter	Size	Description	RD	WR	OEM	Default OEM value
BC_ICHG_CTRL	7 bits	Defines the value of the current for constant current charging mode. ICHG = 1.96mA × ICHG_CODE + 1.92mA Where ICHG_CODE = decimal value of BC_ICHG_CTRL and ICHG_CODE valid value range is from 0x02 to 0x7F with steps of 1. Range: 0x7F: 251mA 0x65: 200mA 0x02: 6mA	-	✓	✓	0x02: 6mA

Parameter	Size	Description	RD	WR	OEM	Default OEM value
BC_ICHG_PCT_COLD	3 bits	Percentage of the charging current (BC_ICHG_CTRL) for COLD NTC temperature range. Range: 0b000: 100% 0b001: 75% 0b010: 50% 0b011: 25% 0b100: 0% others: RFU (is interpreted as 0) *Note*: Actual temperature threshold is defined by the NTC type. If the charging current (BC_ICHG_CTRL) is reduced below the minimum setting (02), the charger is disabled. If 0b100: 0% configuration is used, the PTX30W stops WPT cycle requests, and the battery temperature error is reported in the ERROR_STATUS parameter. Poller must reset the RF filed to restart charging.	-	-	✓	0b000: 100%
BC_ICHG_PCT_HOT	3 bits	Percentage of the charging current (BC_ICHG_CTRL) for HOT NTC temperature range. Range: 0b000: 100% 0b001: 75% 0b010: 50% 0b011: 25% 0b100: 0% others: RFU (is interpreted as 0) *Note*: Actual temperature threshold is defined by the NTC type. If the charging current (BC_ICHG_CTRL) is reduced below the minimum setting (02), the charger is disabled. If 0b100: 0% configuration is used, the PTX30W stops WPT cycle requests, and the battery temperature error is reported in ERROR_STATUS parameter. Poller must reset the RF filed to restart charging.	-	-	✓	0b000: 100%

Parameter	Size	Description	RD	WR	OEM	Default OEM value
BC_VTERM_CTRL	3 bits	Defines termination voltage for constant voltage charging mode. Range: 0x00: 3.59V 0x01: 3.62V 0x02: 3.65V 0x03: 3.67V 0x04: 3.70V 0x05: 3.73V 0x06: 3.75V 0x07: 3.81V 0x08: 3.83V 0x09: 3.86V 0x0A: 3.91V 0x0B: 3.94V 0x0C: 3.97V 0x0D: 4.02V 0x0E: 4.08V 0x0F: 4.13V 0x10: 4.16V 0x11: 4.18V 0x12: 4.24V 0x13: 4.26V 0x14: 4.29V 0x15: 4.32V 0x16: 4.34V 0x17: 4.40V 0x18: 4.42V 0x19: 4.45V 0x1A: 4.51V 0x1B: 4.53V 0x1C: 4.56V 0x1D: 4.59V 0x1E: 4.61V 0x1F: 4.65V	-	✓	✓	0x11: 4.18V
BC_VTERM_ OFFSET_COLD	3 bits	BC_VTERM_CTRL offset in steps for the COLD NTC temperature range. Range: 0b000: BC_VTERM_CTRL 0b001: BC_VTERM_CTRL - 1 0b010: BC_VTERM_CTRL - 2 0b011: BC_VTERM_CTRL - 3 0b100: BC_VTERM_CTRL - 4 0b101: BC_VTERM_CTRL - 5 0b110: BC_VTERM_CTRL - 6 0b111: BC_VTERM_CTRL – 7 *Note*: Actual temperature threshold is defined by the NTC type.	-	-	✓	0b000: BC_VTERM_CTRL

Parameter	Size	Description	RD	WR	OEM	Default OEM value
BC_VTERM_ OFFSET_HOT	3 bits	BC_VTERM_CTRL offset in steps for the HOT NTC temperature range. Range: 0b000: BC_VTERM_CTRL 0b001: BC_VTERM_CTRL - 1 0b010: BC_VTERM_CTRL - 2 0b011: BC_VTERM_CTRL - 3 0b100: BC_VTERM_CTRL - 4 0b101: BC_VTERM_CTRL - 5 0b110: BC_VTERM_CTRL - 6 0b111: BC_VTERM_CTRL – 7 *Note*: Actual temperature threshold is defined by the NTC type.	-	-	✓	0b000: BC_VTERM_CTRL
BC_VTRK_CTRL	3 bits	Defines the value of the voltage for the transition between trickle charge and constant current charging. Sets trickle voltage threshold to: 0b000: 3.00V 0b001: 2.50V 0b010: 2.60V 0b011: 2.70V 0b100: 2.80V 0b101: 2.90V 0b110: 3.10V 0b111: 3.20V	-	✓	✓	0b000: 3.00V
BC_VRCHG_CTRL	4 bits	Battery charger recharge control bits. If the voltage on the battery drops below the configured threshold, the battery charger restarts the charging. Sets recharge voltage threshold to: 0b0000: 2.91V 0b0001: 3.02V 0b0010: 3.13V 0b0011: 3.23V 0b0100: 3.34V 0b0101: 3.44V 0b0110: 3.55V 0b0111: 3.66V 0b1000: 3.73V 0b1001: 3.77V 0b1010: 3.82V 0b1011: 3.87V 0b1100: 4.04V 0b1101: 4.20V 0b1110: 4.30V 0b1111: 4.42V *Note*: BC_VRCHG_CTRL voltage threshold is set at least 300mV lower than BC_VTERM_CTRL (termination voltage).	-	✓	✓	0b1011: 3.87V

Parameter	Size	Description	RD	WR	OEM	Default OEM value
BC_ITERM_CTRL	6 bits	Defines the value of the termination current of the constant voltage mode. ITERM = 1.39mA × BC_ITERM_CTRL- 0.34mA BC_ITERM_CTRL valid value range is from 4 to 59 with steps of 1. Range: 0x04: 5.2mA ... 0x3B: 81.7mA	-	-	✓	0x0E: 19mA
BC_LO_BATOFF_EN	1 bit	If set to 0, the battery connection check is disabled. The charging starts the charging process even without the battery connected. Can be used for systems with a battery that has a built-in protection circuit.	-	-	✓	0b0: disabled
BC_ENABLE	1 bit	If set to 1, the battery charger block is enabled. Otherwise, the battery charger is disabled. *Note*: Writing this parameter to 0 disables battery charging, but the listener is still request for WPT to the poller. To stop the RF field provided by the poller, the WPT_REQ_SEL parameter is used.	✓	✓	✓	0b1: enabled
VDMCU_MODE	2 bits	Defines the configuration of the MCU LDO (VDMCU pin): 0b11: Input (default), external voltage to be provided for I^2C and GPO reference voltage. 0b01: 1.8V output 0b10: 3.3V output 0b00: RFU *Note*: VDMCU_MODE parameter is only configurable for PTX30WA1 (VDMCU as input) product variant. For PTX30WB1 and PTX30WC1 product variants, configuration is not effective.	-	-	✓	Defined by product variant, configurable only for 30WA1.

Parameter	Size	Description	RD	WR	OEM	Default OEM value
NFC_RESISTIVE_MOD	4 bits	Resistor value for modulation during NFC communication. 0b0000: Disabled 0b0001: 170.0Ω 0b0010: 85Ω 0b0011: 57Ω 0b0100: 43Ω 0b0101: 34Ω 0b0110: 27Ω 0b0111: 24Ω 0b1000: 21Ω 0b1001: 19Ω 0b1010: 17Ω 0b1011: 15Ω 0b1100: 14Ω 0b1101: 13Ω 0b1110: 12Ω 0b1111: 11Ω	-	-	✓	0b1111: 11Ω
NFC_RESISTIVE_SET	4 bits	Resistor value for constant wave during NFC communication. 0b0000: Disabled 0b0001: 170.0Ω 0b0010: 85Ω 0b0011: 57Ω 0b0100: 43Ω 0b0101: 34Ω 0b0110: 27Ω 0b0111: 24Ω 0b1000: 21Ω 0b1001: 19Ω 0b1010: 17Ω 0b1011: 15Ω 0b1100: 14Ω 0b1101: 13Ω 0b1110: 12Ω 0b1111: 11Ω	-	-	✓	0b1010: 17Ω

Parameter	Size	Description	RD	WR	OEM	Default OEM value
WPT_RESISTIVE_MOD		Resistor value for modulation during a WPT cycle. 0b0000: Disabled 0b0001: 170.0Ω 0b0010: 85Ω 0b0011: 57Ω 0b0100: 43Ω 0b0101: 34Ω 0b0110: 27Ω 0b0111: 24Ω 0b1000: 21Ω 0b1001: 19Ω 0b1010: 17Ω 0b1011: 15Ω 0b1100: 14Ω 0b1101: 13Ω 0b1110: 12Ω 0b1111: 11Ω	-	-	✓	0b0000: Disabled
WPT_RESISTIVE_SET		Resistor value for constant wave during a WPT cycle. 0b0000: Disabled 0b0001: 170.0Ω 0b0010: 85Ω 0b0011: 57Ω 0b0100: 43Ω 0b0101: 34Ω 0b0110: 27Ω 0b0111: 24Ω 0b1000: 21Ω 0b1001: 19Ω 0b1010: 17Ω 0b1011: 15Ω 0b1100: 14Ω 0b1101: 13Ω 0b1110: 12Ω 0b1111: 11Ω	-	-	✓	0b0000: Disabled
CURSENS_TH_SEL	2 bits	Voltage limiter current sensor threshold selection: 0b00: 2mA 0b01: 5mA 0b10: 10mA 0b11: 20mA *Note*: This is used for power regulation. If the configured current is exceeded, the PTX30W requests for power reduction to the poller.	-	-	✓	0b01: 5mA

Parameter	Size	Description	RD	WR	OEM	Default OEM value
LIM_TH_SEL *(present in firmware version 5259 and newer)*		Voltage limiter threshold: 0b0000: Invalid 0b0001: Invalid 0b0010: 3.2V 0b0011: 3.4V 0b0100: 3.6V 0b0101: 3.8V 0b0110: 4.0V 0b0111: 4.2V 0b1000: 4.4V 0b1001: 4.6V 0b1010: 4.8V 0b1011: 5.0V 0b1100: 5.2V others: Invalid *Note*: Setting the parameter to the Invalid value can result in unwanted behavior.	-	✓	✓	0b1100: 5.2V
VDDC_TH_LOW	1 byte	Power regulation VDDC threshold, low. Used during system supply and charging. Value = 12.5mV × VDDC_TH_LOW + 2.4V *Note*: The VDDC threshold is not set lower than 3V (to keep margin to BOD reset threshold).	-	-	✓	0x60: 3.6V
VDBAT_OFFSET_HIGH	1 byte	Power regulation VDBAT offset, high. Used during trickle charge and constant current mode. Value = 12.5mV × VDBAT_OFFSET_HIGH	-	-	✓	0x40: 0.8V
VDBAT_OFFSET_LOW	1 byte	Power regulation VDBAT offset, low. Used during trickle charge and constant voltage mode. Value = 12.5mV × VDBAT_OFFSET_LOW	-	-	✓	0x18: 0.3V
IRQ_POLARITY	1 bit	Selects the polarity of the IRQ. 0b0: active high 0b1: active low	-	-	✓	0b0: active high
I2C_ADDR	7 bits	System I^2C address. Default value is 0x4B.	-	-	✓	0x4B

Parameter	Size	Description	RD	WR	OEM	Default OEM value
HOST_WPT_ DURATION_INT	5 bits	If set to a value 0 - 0x13, the HOST_WPT_DURATION_INT overrides the {ADJ, TCM, CCM, CVM} WPT_DURATION_INT values defined below. Otherwise, the defined values apply. The WPT duration (in ms) is calculated according to the following formula: HOST_WPT_DURATION = $2^{(HOST\_WPT\_DURATION\_INT+3)}$. *Note*: When that parameter is set by the Host, the control of WPT duration is taken over by that parameter (ADJ_WPT_DURATION_INT, TCM_WPT_ DURATION_INT, CCM_WPT_ DURATION_INT and CVM_WPT_ DURATION_INT is not valid any longer). This is valid until the reset of the chip (entering shipping mode).	-	✓	-	-
ADJ_WPT_ DURATION_INT	5 bits	Defines WPT duration during adjustment phase in milliseconds (ms) using the following formula: ADJ_WPT_DURATION = $2^{(ADJ\_WPT\_DURATION\_INT+3)}$. The valid range is 0 - 0x13. Other values are truncated to 0x13. *Note*: PTX30W requests for WPT phases with duration of ADJ_WPT_DURATION_INT until the voltage on VDDC appears within the regulation window.	-	-	✓	0x04: 128ms
TCM_WPT_ DURATION_INT	5 bits	Defines WPT duration that is used during trickle charging mode using the following formula: TCM_WPT_DURATION = $2^{(TCM\_WPT\_DURATION\_INT+3)}$. The valid range is 0 - 0x13. Other values are truncated to 0x13.	-	-	✓	0x06: 512ms
CCM_WPT_ DURATION_INT	5 bits	Defines WPT duration that is used during constant current charging mode using the following formula: CCM_WPT_DURATION = $2^{(CCM\_WPT\_DURATION\_INT+3)}$. The valid range is 0 - 0x13. Other values are truncated to 0x13.	-	-	✓	0x09: 4096ms

Parameter	Size	Description	RD	WR	OEM	Default OEM value
CVM_WPT_ DURATION_INT	5 bits	Defines WPT duration that is used during constant voltage charging mode using the following formula: CVM_WPT_DURATION = $2^{(CVM\_WPT\_DURATION\_INT+3)}$. The valid range is 0 - 0x13. Other values are truncated to 0x13.	-	-	✓	0x08: 2048ms
TCM_TIMEOUT	1 byte	Defines the TCM timeout value in 2^{16}ms units (~1.1min). If set to 0, the TCM timeout check is disabled. *Note*: When the timeout expires, the ERROR_STATUS parameter is set, and the error is reported to the poller using ERROR_INFO in the WLCL_CTL record. ERROR_INFO value reported to the poller: 0x04: TCM_TIMEOUT_ERR	-	-	✓	0x00: disabled
CCM_TIMEOUT	1 byte	Defines the CCM timeout value in 2^{16}ms units (~1.1min). If set to 0, the CCM timeout check is disabled. *Note*: When the timeout expires, the ERROR_STATUS parameter is set, and the error is reported to the poller using ERROR_INFO in the WLCL_CTL record. ERROR_INFO value reported to the poller: 0x05: CCM_TIMEOUT_ERR	-	-	✓	0x00: disabled
CVM_TIMEOUT_INT	1 byte	Defines the CVM timeout value in 2^{16} ms units (~1.1min). If set to 0, the CVM timeout check is disabled. *Note*: When the timeout expires, the ERROR_STATUS parameter is set, and the error is reported to the poller using ERROR_INFO in the WLCL_CTL record. ERROR_INFO value reported to the poller: 0x06: CVM_TIMEOUT_ERR	-	-	✓	0x00: disabled
CUSTOM_NDEF_ MSG	1-145 bytes	Defines custom NDEF message. The first byte defines the length of the message. If the length is set to 0, the NDEF message is not set.	-	✓	-	-

Parameter	Size	Description	RD	WR	OEM	Default OEM value
CAP_WT_INT	1 byte	Defines the time the poller must wait before re-reading the WLC_CAP message. The parameter is only used when the listener is operating in the static charging mode (this is the case for battery full scenario). The valid values are 00h - 13h. All other values are RFU and imply that the listener operates in the negotiated mode. CAP_WT = $2^{(CAP\_WT\_INT+3)}$	-	-	✓	0x0B: 16384ms
GPO_0_CONFIG	4 bits	Defines the functionality of GPO_0 pin: 0b0000: GPO disabled 0b0001: Error status (out) 0b0010: Charging status (out) 0b0011: RF field present (out) 0b0100: Poller device connected (out) 0b0101: Controlled by poller (out) 0b0110: Startup circuit enable (out) others: RFU (is treated as 0000b)	-	-	✓	0b0110: Startup circuit enable
GPO_1_CONFIG	4 bits	Defines the functionality of GPO_1 pin: 0b0000: GPO disabled 0b0001: Error status (out) 0b0010: Charging status (out) 0b0011: RF field present (out) 0b0100: Poller device connected (out) 0b0101: Controlled by poller (out) others: RFU (is treated as 0000b)	-	-	✓	0b0000: GPO disabled
RFF_STATUS	1 bit	Indicates the status of the NFC RF field. If set to 1, RF field is present.	✓	-	-	-
SHIPPING_MOD_ ENABLE	1 bit	If set to 1, the SHIPPING MODE is enabled. Otherwise, it is disabled.	-	✓	-	-
BC_LO_UVLO_EN	1 bit	If set to 1, Undervoltage Lockout feature is enabled. Otherwise, the UVLO is disabled.	-	-	✓	0b0: disabled

Parameter	Size	Description	RD	WR	OEM	Default OEM value
WPT_REQ_SEL	2 bits	Defines the WPT_REQ functionality. 0b00: WPT_REQ is controlled by the BC. 0b01: WPT_REQ is disabled. 0b10: WPT_REQ always set (NFC supply) 0b11: RFU *Note*: If the parameter is configured to 0b00, the PTX30W does not further request for WPT when the battery is full. If set to 0b10, the PTX30W continues requesting for WPT to supply the Host system.	-	✓	✓	0b00: WPT_REQ controlled by the BC
DETUNE_ENABLE	1 bit	If set to 1, the detuning circuitry is enabled. Otherwise, the detuning circuitry is disabled.	-	✓	-	-
NFC_ENABLE	1 bit	NFC Interface Enable. PTX30W does not respond to any NFC command when NFC interface is disabled. 0b0: Disabled 0b1: Enabled	-	✓	-	-
ERROR_STATUS	1 byte	Error status. 0x00: No error 0x01: IC temperature error 0x02: Protocol error 0x04: Battery not connected error 0x08: Battery temperature error 0x0C: TCM timeout error 0x10: CCM timeout error 0x14: CVM timeout error Others: RFU *Note*: Error status is cleared when the ERROR_STATUS parameter is read using the Host interface.	✓	-	-	-
BC_STATUS	1 byte	Battery charger status. 0x00: Undefined/Disabled 0x01: Trickle Charge Mode (TCM) 0x02: Constant Current Mode (CCM) 0x03: Constant Voltage Mode (CVM) 0x04: Charging completed others: RFU Find mode details in Table 12.	✓	-	-	-

Parameter	Size	Description	RD	WR	OEM	Default OEM value
VDBAT_ADC_VAL	1 byte	ADC value of VDBAT node. Voltage can be calculated based on: V_{VDBAT} = 12.5mV × VDBAT_ADC_VAL + 2.4V *Note*: Current value of the voltage is reported. If ADC cannot measure, the VDBAT_ADC_VAL is 0.	✓	-	-	-
VDDC_ADC_VAL	1 byte	ADC value of VDDC node. Voltage can be calculated based on: VVDDC = 12.5mV × VDDC_ADC_VAL + 2.4V *Note*: Current value of the voltage is reported. If ADC cannot measure, the VDDC_ADC_VAL is 0.	✓	-	-	-
NTC_STATUS	1 byte	0x00: Normal 0x04: Hot 0x0C: eHot 0x02: Cold 0x03: eCold	✓	-	-	-
WPT_OSC_MOD_EN	1 bit	Enables the oscillator mode during a WPT cycle.	-	-	✓	0b1: enabled
NFC_ICHG	6 bits	Defines the charging current during NFC communication: 0x00: Use the current charging current. 0x01: BC disabled 0x02 – 0x3F: As defined in BC_ICHG_REG	-	-	✓	0x02: 6mA
WLCP_CONNECTED	2 bits	Indicates the status of a poller device connected over the RF interface: 0b00: No poller device connected 0b01: Poller device connected (WLCP-INFO record written) 0b11: Charging started (First WLCL-CTL record read) *Note*: The parameter is reset to 00b when RF field is removed.	✓	-	-	-
NTC_MODE	1 bit	NTC mode: 0b0: PTX30W updates the NTC_STATUS parameter with a period of 1ms. 0b1: PTX30W updates the NTC_STATUS parameter once before each WPT cycle.	-	-	✓	0b0: update with a period of 1ms

Table 12 provides an overview of battery charger state in different system states on the PTX30W device. The BC_STATUS parameter is going to indicate 0 (disabled) when the RF filed is off (System supply from battery functional state), and the battery is not fully charger.

Table 12. BC_STATUS Parameter Description

BC Internal State / System State	Battery Charger Disabled	Trickle Charge Mode	Constant Current Mode	Constant Voltage Mode	Charging Completed
RF field off	0 – Battery charger disabled	0 – Battery charger disabled	0 – Battery charger disabled	0 – Battery charger disabled	4 – Charging completed
WPT cycle	0 – Battery charger disabled	1 – Trickle charge mode	2 – Constant current mode	3 – Constant voltage mode	4 – Charging completed
NFC communication	0 – Battery charger disabled	NC[1]	NC[1]	NC[1]	4 – Charging completed

1. No change, the PTX30W returns the last BC status.

4.8.2 NSC Interface

This section describes an interface between PTX30W and Host MCU.

The interface supports three different message types:

- NSC command message
- NSC response message
- NSC data message

The NSC command message can be sent by the Host only and provides an option for the Host to control and/or check the status of the PTX30W device. The Host can send one outstanding command message and must wait for the response from PTX30W before sending the next command.

The NSC response message is only sent by the PTX30W as a response to a command message.

The NSC data message can be sent by the Host and PTX30W and transfers binary data between the devices using the transparent data channel.

To send an NSC command/message to PTX30W, the Host must use the WMSG command of the HIP with an **input buffer address set to 0**. The payload of the WMSG command must contain the NSC command. The maximum length of the NSC data command/message is 256+8 bytes.

To receive an NSC response or NSC data message from the PTX30W, the Host must perform the following steps:

1. Wait for IRQ pin to get asserted.
2. Read the length of the pending message using RML command of the HIP.
3. Read the message using RMSG command of the HIP. The payload of the RMSG command contains the NSC response or NSC data message from the PTX30W.

4.8.2.1 NSC_CONFIG_CMD/RSP [0x01]

NSC_CONFIG_CMD writes the OEM parameters to the NVM. The command is executed only once and is deactivated afterwards.

The command reads and compares the written parameters. If they do not match, the command returns ERROR_CODE 0x03 (NVM write error).

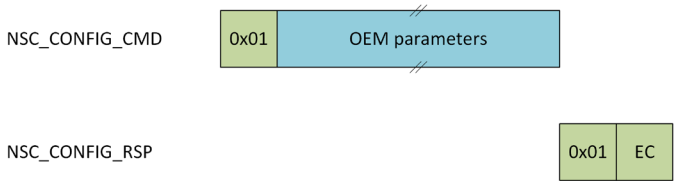


Figure 17. NSC_CONFIG_CMD/RSP

Table 13. NSC_CONFIG_CMD/RSP

Item	Definition
0x01	Command and response opcode
OEM parameters	See Table 14 for more information
EC	Error Code

Table 14 shows the ordered list of the parameters that are supported by the NSC_CONFIG_CMD.

Note: Ensure that the value of each parameter is aligned with its bitfield position. Furthermore, the unused bits are RFU and set to 0.

Table 14. NSC OEM Parameter List

Number	Parameter	Size	Bitfield
1	CAP_WT_INT	1 byte	7:0
2	NFC_ICHG	1 byte	6:0
3	VDBAT_OFFSET_HIGH	1 byte	7:0
4	VDBAT_OFFSET_LOW	1 byte	7:0
5	RFU	1 byte	7:0
6	CURSENS_TH_SEL	1 byte	3:2
7	NFC_RESISTIVE_MODE NFC_RESISTIVE_SET	1 byte	7:4 3:0
8	LIM_TH_SEL *(present in firmware version 5259 and newer)*	1 byte	3:0
9	RFU BC_LO_UVLO_EN BC_LO_BATOFF_EN	1 byte	7:7 2:2 1:1
10	BC_ENABLE	1 byte	0:0
11	BC_VTERM_OFFSET_COLD	1 byte	2:0
12	BC_VTERM_OFFSET_HOT	1 byte	2:0
13	BC_ICHG_PCT_COLD	1 byte	2:0
14	BC_ICHG_PCT_HOT	1 byte	2:0

Number	Parameter	Size	Bitfield
15	BC_ITERM_CTRL	1 byte	5:0
16	BC_VTRK_CTRL BC_VTERM_CTRL	1 byte	7:5 4:0
17	BC_VRCHG_CTRL	1 byte	3:0
18	BC_ICHG_CTRL	1 byte	6:0
19	RFU	1 byte	2:0
20	WPT_RESISTIVE_MOD WPT_RESISTIVE_SET	1 byte	7:4 3:0
21	VDMCU_MODE	1 byte	1:0
22	IRQ_POLARITY I2C_ADDR	1 byte	7:7 6:0
23	GPO_1_CONFIG	1 byte	3:0
24	GPO_0_CONFIG	1 byte	3:0
25	VDDC_TH_LOW	1 byte	7:0
26	WPT_REQ_SEL	1 byte	1:0
27	WPT_OSC_MODE_EN NTC_MODE	1 byte	1:1 0:0
28	ADJ_WPT_DURATION_INT	1 byte	4:0
29	TCM_WPT_DURATION_INT	1 byte	4:0
30	CCM_WPT_DURATION_INT	1 byte	4:0
31	CVM_WPT_DURATION_INT	1 byte	4:0
32	TCM_TIMEOUT_INT	1 byte	7:0
33	CCM_TIMEOUT_INT	1 byte	7:0
34	CVM_TIMEOUT_INT	1 byte	7:0

4.8.2.2 NSC_SET_PARAM_CMD/RSP [0x02]

NSC_SET_PARAM_CMD changes the PTX30W parameters during the operation. The command specifies a list of parameters to be changed. Each parameter comprises of a parameter ID and its value. The command is terminated by an end-of-command (EoC) terminator.

Note: The parameters must be provided in the correct format as specified in the parameter description.

When the command is parsed, the response is sent to the Host to finish the transaction. The response consists of an opcode [0x02] and an error code. The list of error codes can be found later in the document.

Figure 18 shows the NSC_SET_PARAM_CMD/RSP with three parameters.

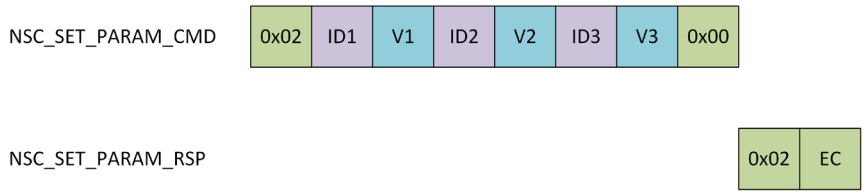


Figure 18. NSC_SET_PARAM_CMD/RSP

Table 15. NSC_SET_PARAM_CMD/RSP

Item	Definition
0x02	Command and response opcode
IDx	ID of the first, second, and third parameter
Vx	Value of the first, second, and third parameter
0x00	EoC (End-of-Command)
EC	Error code

The following parameters are supported by the NSC_SET_PARAM_CMD.

Note: Ensure that the parameters are formatted according to their bitfield position. Furthermore, the unused bits are RFU and are set to 0.

Table 16. NSC WR Parameter List

Parameter	ID	Bitfield
BC_ICHG_CTRL	01h	6:0
BC_VTERM_CTRL	02h	4:0
BC_VTRK_CTRL	03h	7:5
BC_VRCHG_CTRL	04h	3:0
BC_ENABLE	05h	0:0
HOST_WPT_DURATION_INT	06h	4:0
CUSTOM_NDEF_MSG[1]	07h	7:0
SHIPPING_MODE_ENABLE	08h	0:0
WPT_REQ_SEL	09h	1:0
DETUNE_ENABLE	0Ah	0:0
NFC_ENABLE	0Bh	0:0
LIM_TH_SEL (present in firmware version 5259 and newer)	0Ch	3:0

1. CUSTOM_NDEF_MSG comprises of a length byte and a message payload. The maximum length of the payload is 144 bytes.

4.8.2.3 NSC_GET_PARAM_CMD/RSP [0x03]

NSC_GET_PARAM_CMD returns the current values of PTX30W RD parameters. The command consists of the command opcode only.

The NSC_GET_PARAM_RSP response consists of an opcode [0x03], an error code and a list of parameter values in a specific order (see Table 17). If the error code is not 0, the list of values is omitted.

Figure 19 shows an example of the NSC_GET_PARAM_CMD and NSC_GET_PARAM_CMD responses.

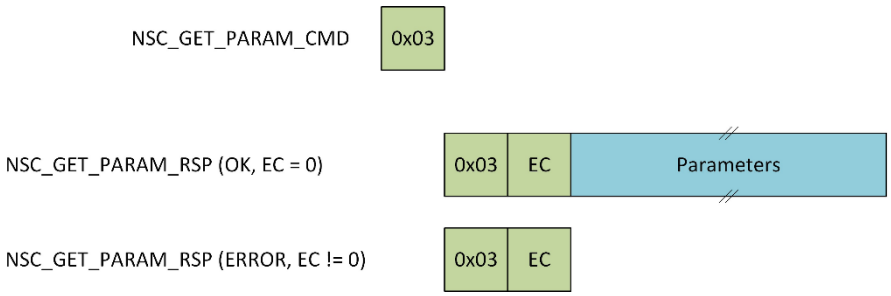


Figure 19. NSC_GET_PARAM_CMD/RSP

Table 17. NSC RD Parameter List

Number	Parameter	Bitfield
1	BC_ENABLE	0:0
2	RFF_STATUS	0:0
3	ERROR_STATUS	7:0
4	BC_STATUS	7:0
5	VDBAT_ADC_VAL	7:0
6	VDDC_ADC_VAL	7:0
7	NTC_STATUS	7:0
8	WLCP_CONNECTED	1:0

4.8.2.4 RSS Response

PTX30W returns the following parameters to an RSS HIP command.

Table 18. RSS Command Response

Parameter	Size	Bitfield
ACK/NAK	1 byte	Acknowledge value of the previous command.
HW_VERSION	1 byte	7:0
FW_VERSION	2 bytes	7:0
DIE_INFO	16 bytes	7:0
OEM_VALID_FLAG	1 byte	If the PTX30W has valid OEM parameters configured, the OEM_VALID_FLAG is set to 1, otherwise it is set to 0.

4.8.2.5 NSC_DATA_MSG [0x80]

NSC_DATA_MSG transfer binary data between PTX30W and the Host, and vice-versa.

See the Transparent Data Channel (TDC) section for more information about the data transfer between the poller and the Host.

Figure 20 shows a format of the NSC_DATA_MSG.

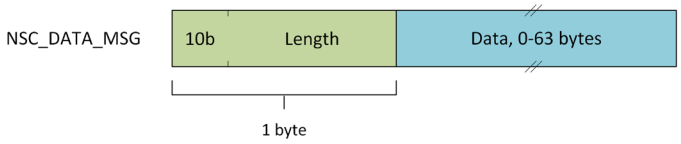


Figure 20. NSC_DATA_MSG

Table 19. NSC_DATA_MSG

Parameter	Size	Bitfield
10b	2 bits	NSC_DATA_MSG opcode
Length	6 bits	The length of the data parameter
Data	0 - 63 bytes	Payload

4.8.2.5.1 Chaining

The payload length of an NSC_DATA_MSG is limited to 63 bytes. If a longer message needs to be transferred, the initiator might split the message into smaller chunks.

Here is an example of how a longer message might be transferred using multiple NSC_DATA_MSG frames.

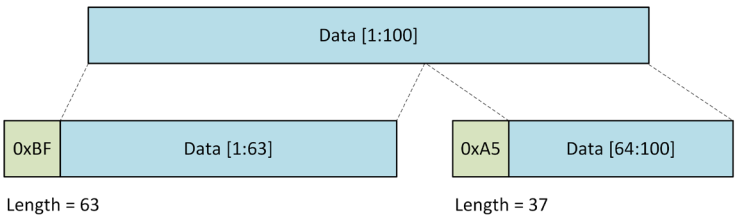


Figure 21. Chaining of NSC_DATA_MSG

4.8.2.5.2 Flow Control

Figure 22 shows an example of the data transfer from PTX30W to the Host.

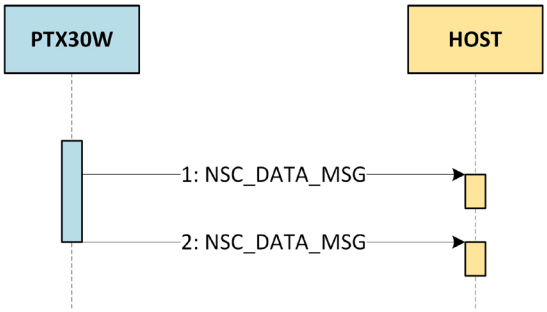


Figure 22. Data Transfer from PTX30W to the Host

- Step 1 – The PTX30W sends the NSC_DATA_MSG to the Host. *Note*: There is no explicit Acknowledge required from the Host, as the Acknowledge is implicit in the transaction.

- Step 2 – The PTX30W sends the second NSC_DATA_MS. Again, no explicit Acknowledge is required from the Host.

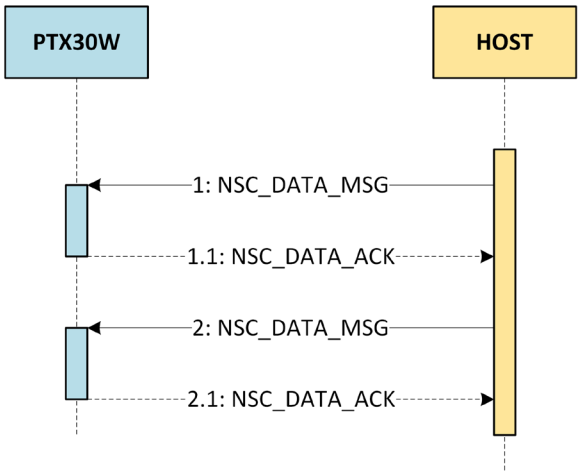


Figure 23. Data Transfer from the Host to PTX30W

- Step 1 – The Host sends an NSC_DATA_MSG to PTX30W. The Host must wait for the Acknowledge (Step 1.1) before sending the next message.
- Step 2 – The Host sends the next NSC_DATA_MSG. Again, the Host must wait for the Acknowledge (Step 2.1) before sending the next message.

The Acknowledge is represented by an NSC_DATA_MSG with Length set to 0, and without the Data parameter, as shown in Figure 24.

Figure 24. NSC_DATA_ACK

4.8.2.6 Error Codes

Table 20. Error Codes Description

Parameter	Bitfield
0x00	No error
0x01	Invalid command
0x02	Invalid parameter
0x03	NVM write error

4.8.3 Host Interface Protocol (HIP)

Host-Interface Protocol is a low-level protocol on top of the HW protocols supported by the Host-Interface.

4.8.3.1 Frame Format

The frame format of the protocol is shown in Figure 25. The frame sent in the direction from the Host to the PTX device is called a command frame and a frame sent in the direction from the PTX device to the Host is called a response frame.

Figure 25. Host Interface Frame Format

Each frame (command or response) consists of several parameters. Most of the parameters are mandatory, but some are optional (for example CRC). All parameters are byte aligned and consist of one or multiple bytes. The multiple-byte parameters use MSB (Most Significant Bye) first format, unless otherwise specified. If not explicitly specified a parameter is one byte long.

- LEN – A 2-byte parameter that defines the length of the frame including FCB, payload, and CRC (excluding SOF, LEN, and padding). The valid range of the LEN parameter is 1 - 4095. An invalid LEN parameter is treated as an invalid length error.
- FCB (Frame Control Byte) – Determines the type of the frame and includes additional information required for the data transaction. Table 21 defines the format of the FCB.

Table 21. HIP, FCB Format

Bits [7:4]	Bit 3	Bit 2	Bit 1	Bit 0
OPCODE	RFU	RAK	CRC	RFU

- OPCODE – Defines a type of command conveyed by the frame. All available commands are described in the following section.
- RFU (Reserved for future use) – Renesas recommends setting this bit to 0.
- RAK (Request Acknowledge) – When the RAK bit is set, the PTX device sends an Acknowledge (ACK) response to a write command. For a read command, the RAK is ignored.
- CRC – Defines whether the CRC field is included in the frame. If CRC is included in a command frame, the corresponding response frame is also included.
- Payload – The content of a command or response.
- CRC (Cyclic-Redundancy-Check) – A 2-byte value used to verify the integrity of the frame. The CRC field is optional and is only present if the CRC bit of the FCB is set. The CRC is calculated over the whole frame except the SOF and the padding fields. The CRC is calculated as defined in ISO/IEC 14443-3, Type-B standard (CRC_B, see also ISO/IEC 13239 and ITU-T X.25 #2.2.7 and V.42 #8.1.1.6.1). Initial Value is 0xFFFF, CRC is inverted.
- Padding – The padding of arbitrary content and length can be added at the end of the command frame if a certain byte alignment is required by the Host. The padding is discarded by the PTX device.
  Note: The padding bytes are not included in the LEN parameter.

4.8.3.2 Maximum Frame Size

The maximum frame size is limited by the size of the LEN parameter; however, an additional limit can be set to reduce the maximum frame size. Refer to the actual implementation documentation of your product for more information.

4.8.3.3 No Response

No response is sent by the PTX device in the following two cases:

- If an erroneous command frame is received.
- A valid write command frame with the FCB.RAK bit set to 0 is received.

4.8.3.4 Acknowledge

The Host may request a write command frame to be acknowledged by setting the FCB.RAK bit to 1, otherwise no response is sent to the Host. Figure 26 shows the format of an acknowledge frame.

Figure 26. Host Interface Acknowledge

The PTX device sets the FCB.RAK bit of the response to 1, indicating an acknowledge frame.

The ACK value is set to 0x00.

4.8.3.5 Error Handling

If an erroneous command frame is received by the PTX device, no response is sent to the Host. Additionally, the PTX device stores the corresponding NAK (Not Acknowledge) value for further analysis. The NAK value may be retrieved by the RSS (Read System Status) command described in one of the following sections. Table 22 lists all ACK/NAK values.

Table 22. Error Handling, ACK and NAK Values

ACK / NAK Value	Description
0x00	No error (ACK)
0x01	Invalid command (NAK)
0x02	Invalid length (NAK)
0x03	CRC error (NAK)
0x04	Invalid parameter (NAK)
0x05	Write buffer full (NAK)
others	RFU (Reserved for future use)

4.8.3.6 HIP Commands

Table 23 shows commands supported by the HIP protocol.

Table 23. HIP Command List

Command Name	FCB.OPCODE	Description
RST	0x1	System reset
RSS	0x2	Read System Status
WMSG	0x7	Write Message
RMSG	0x8	Read Message
RML	0x9	Read Message Length

4.8.3.6.1 System Reset (RST) Command

The system reset command places the PTX device to a known reset state and/or to enable the PTX30W device core (DFY). The following figure shows the format of the command.

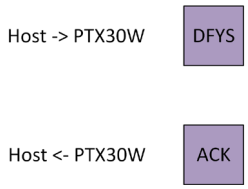


Figure 27: System Reset HIP Command

- DFYS – Determines the action the command is supposed to trigger. The following options are available:
  - 0x01 - Perform system reset and enable DFY afterwards.
  - Others - RFU (invalid parameter, NAK value of 0x4)
- ACK – An ACK is sent by the PTX device if the command frame is valid and the FCB.RAK bit is set. Otherwise, no response is sent.

The system reset is performed after the acknowledge (if requested by the Host) is sent to the Host.

4.8.3.6.2 Read System Status (RSS) Command

Read system status command returns the status of the PTX device. Figure 28 shows the format of the command and response payload.

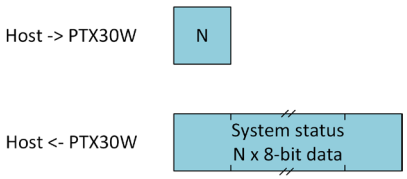


Figure 28: Read System Status HIP Command

- N – N defines the number of bytes to be returned by the command. If N is bigger than the actual number of bytes comprising the system status, the response is padded with 0x00 at the back of the response.

  If N is set to 0, the command is invalid (Invalid parameter NAK 0x4).
- System status (N bytes) – The System status includes the following parameters:
  - 8-bit ACK/NAK value of the previous command
  - Optional parameters such as HW product number, HW serial number, and FW version

Note: The definition of optional parameters might be product specific and is out of the scope of this document.

No response is sent by the PTX device if an erroneous RSS command frame is received.

4.8.3.6.3 Write Message (WMSG) Command

The Write Message command sends a message (command or data) to the PTX device. The message is written in one of the selected input buffers of the PTX device. A format of the command is shown in Figure 29.

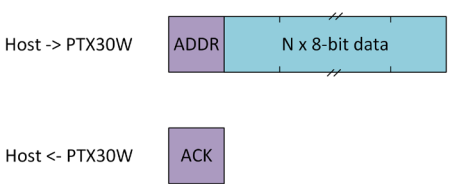


Figure 29: Write Message HIP Command

- ADDR – Defines an 8-bit logical address of a PTX device input buffer. A valid address range depends on the actual implementation of the protocol and is out of the scope of this document. An invalid address is treated as an “invalid parameter” error.
- Data (N bytes) – Data is the content of the message.
- ACK – ACK response is sent by the PTX device if a valid command is received and the command FCB.RAK bit is set, otherwise, no response is sent.

  If the WMSG command tries to write to a full input buffer, the transaction fails and NAK value 0x05 (write buffer full) is stored for further analysis.

  If the payload length of a WMSG command exceeds the size of the target input buffer, the transaction fails and NAK value 0x02 (invalid length) is stored for further analysis.

4.8.3.6.4 Read Message Length (RML)

Read message length determines the length of a message pending in the output buffer of PTX device. If a zero-message length is returned by the PTX device, no message is pending. Figure 30 shows the format of the RML command.

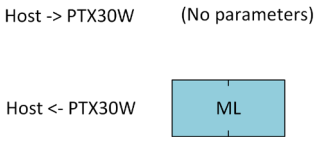


Figure 30: Read Message Length HIP Command

There are no parameters in the RML command.

- ML (2 bytes) – Defines the length of the pending message. ML is 16 bits long with MSB first.

  No response is sent when an erroneous command frame is received.

4.8.3.6.5 Read Message (RMSG) Command

The read message command reads a message (response, notification, or data) pending in the output buffer of the PTX device. The format of the command is shown in Figure 31.

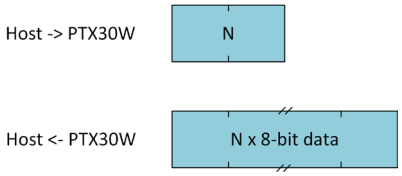


Figure 31. Read Message HIP Command

- N (2 bytes) – Determines the number of bytes to be sent in the response. If N is 0, the whole message is sent. If N is 0, the RML command must be used to determine the actual pending message length.
- Data (N bytes) – Data represents the pending message. If N is larger than the actual size of the message, the message is padded at the end with 0x00 to form an N-byte response payload.

  No response is sent if an erroneous command is received.

4.8.4 I²C Interface

The PTX30W communicates with the Host MCU using an I²C compatible, 2-wire serial interface composed of a bidirectional serial data line (SDA) and a serial clock line (SCL). The PTX30W acts as a target device that relies on an external clock (SCL) generated by the master I²C device (typically a Host MCU). A repeated start is required for every following HIP command after the initial one (see examples in the following sub-sections).

When PTX30W is in standby mode, it cannot process the incoming command (the I²C module does not acknowledge the target address). However, the command wakes up the device, and the device stays in normal mode for at least 100ms for the command to be resent. Figure 32 shows the procedure to be implemented by the Host.

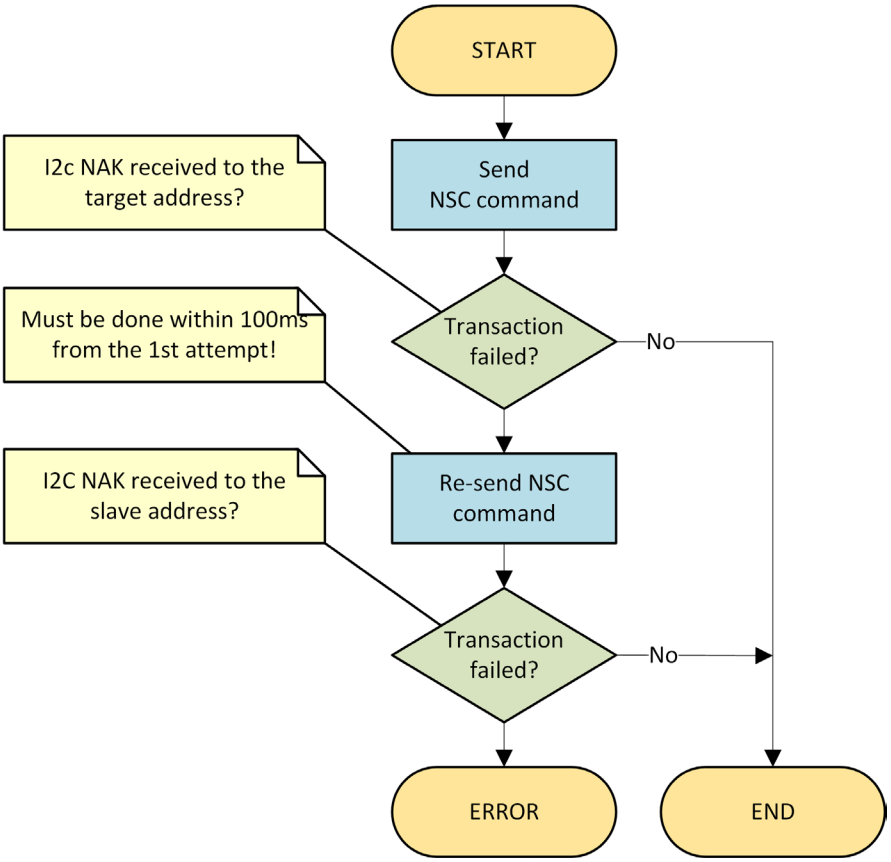


Figure 32. Host I²C Procedure

4.8.4.1 Read System Status (RSS) Command and Response

The following example shows how to send RSS (read system status) command and receive the response.

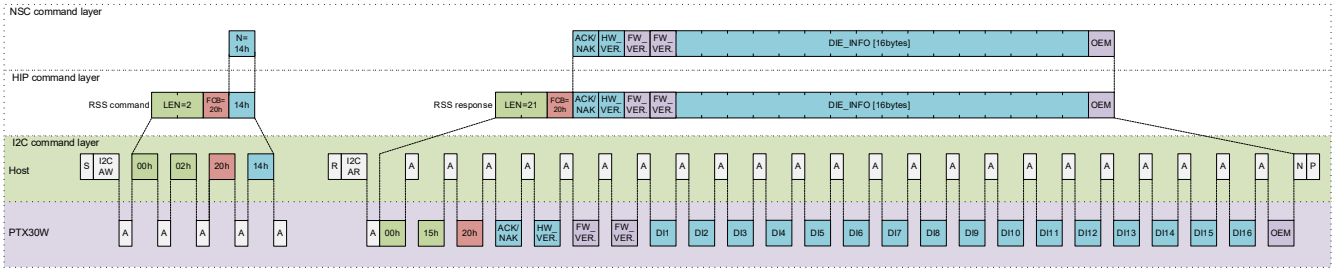


Figure 33. RSS Command and Response

4.8.4.2 NCS_CONFIG_CMD/RSP Example

The following example shows how to configure parameters and read back the response without using CRC bytes. Note that the multibyte parameters, such as LEN and FCB, are sent with the most significant byte (MSB) first.

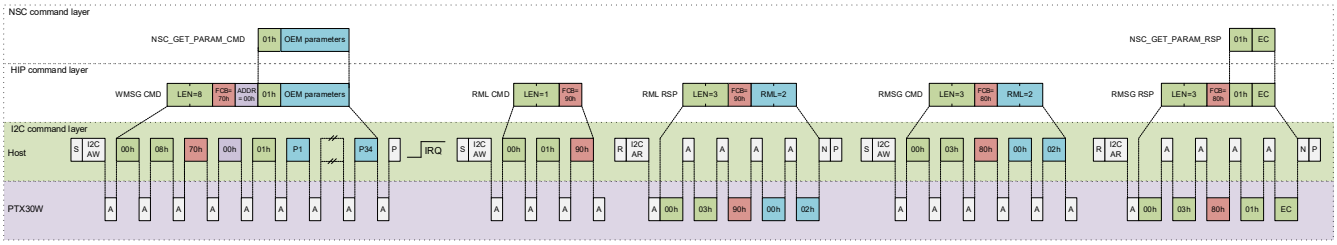


Figure 34. NSC_CONFIG_CMD/RSP Example

4.8.4.3 NSC_SET_PARAM_CMD/RSP Example

The following example shows how to set two parameters and read back the response without using CRC bytes. Note that the multibyte parameters, such as LEN and FCB, are sent with the most significant byte (MSB) first.

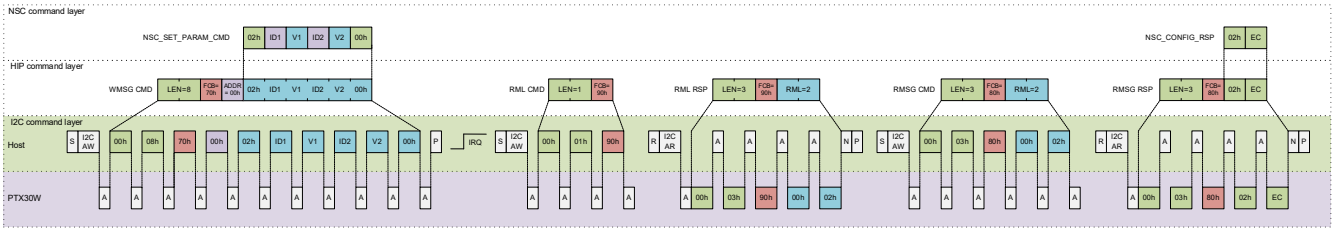


Figure 35. NSC_SET_PARAM_CMD/RSP Example

4.8.4.4 NSC_GET_PARAM_CMD/RSP Example

The following example shows how to read two parameters without using CRC bytes. Note that the multibyte parameters, such as LEN and FCB, are sent with the most significant byte (MSB) first.

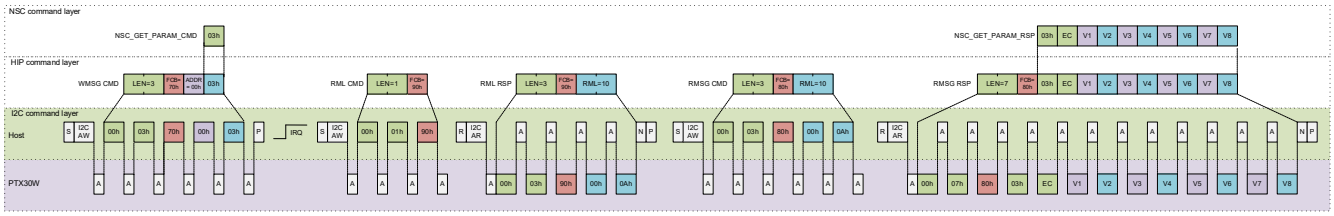


Figure 36. NSC_GET_PARAM_CMD/RSP Example

Table 24. NCS Commands Examples Symbols Description

Symbol	Description
S	Start condition
A	Acknowledge
R	Restart condition
N	Not acknowledge
P	Stop condition
I2C AW	Target address and write condition
I2C AR	Target address and read condition
LEN	Length of the command
FCB	Frame Control Byte
ACK/NAK	Acknowledge / not acknowledge
HW_VER.	HW version
FW_VER.	FW version
DIE_INFO	Die info bits
OEM parameters	OEM parameters values in the order according to the order in NSC OEM parameter list table
EC	Error code according to Error codes description table
IDx	ID of the parameter that is getting set
Vx	Value of the parameter that is getting set

5. Firmware Versions

Table 25. FW Versions

SDK Version	FW Version[1]	Description	Part Number
SDK 2.1.0	5123		PTX30WCC16D7x1
SDK 2.2.0	5123	Added option to enable/disable DC_CHARGING in the SDK	-
SDK 2.3.0	5259	Added possibility to change voltage limiter threshold through LIM_TH_SEL OEM parameter. Removed DC_CHARGING option from the SDK	-
SDK 2.4.2[2]	5279	Stability improvements	PTX30WCC16D7x2

1. Firmware of the device is upgradable using SDK.
2. Firmware downgrade is not allowed and could lead to misbehavior or failure.

6. Package Information

6.1 Marking Diagram

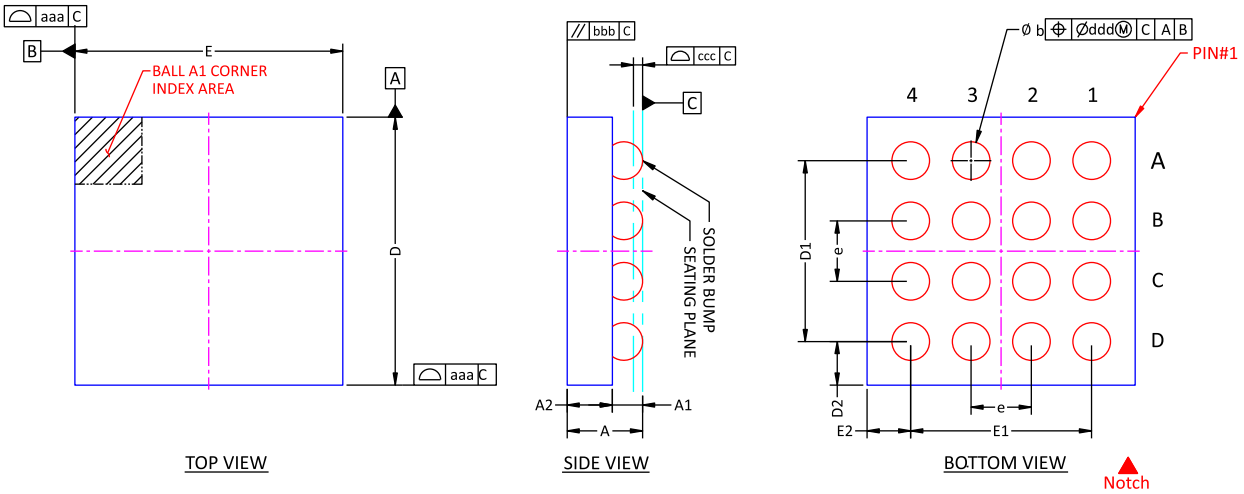
Figure 37: Package Marking Diagram

Table 26. Package Description

Symbol	Description
30Wcf	Device name, c – configuration version and f – firmware version 30WAf → A – VDMCU as input 30WBf → B – VDMCU as output – 1.8V 30WCf → C – VDMCU as output – 3.3V 30Wc1 → 1 – firmware version 5123 30Wc2 → 2 – firmware version 5279
YYWW	2-digit production year followed by 2-digit production week
XXXXXX	Wafer lot number

6.2 Package Outline Drawings

The PTX30 is packaged in a 1.78 × 1.78 mm WL-CSP package with 0.4mm ball pitch.



Control dimensions are in millimeter

Symbol	Dimension in mm		
	Min	Nom	Max
A	0.445	0.500	0.555
A1	0.170	0.200	0.230
A2	0.275	0.300	0.325
D	1.7480	1.7780	1.8080
E	1.7480	1.7780	1.8080
D1	-	1.200	-
E1	-	1.200	-
D2		0.289	
E2		0.289	
e	-	0.400	-
b	0.220	0.250	0.280
aaa		0.030	
bbb		0.060	
ccc		0.050	
ddd		0.015	

NOTE :
1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL PRIMARY DATUM C.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
3. THIS POD IS WITHOUT BACKSIDE COATING

The WL-CSP package is Pb Free (Lead-Free). The Soldering Profile should follow Pb Free rules. Normally Peak temperature of 245°C ±15°C, Dwell Time of 40–90 secs (Above 220°C) - this is the typical Reflow Machine recipe.

7. Ordering Information

Part Number	MCU LDO Configuration	Package Description	Carrier Type	Temperature Range
PTX30WCC16D7A2	VDMCU – input	CSP16, 1.78 × 1.78 mm	Tape and Reel dry pack 7"	-40°C to +70°C
PTX30WCC16D7B2	VDMCU – 1.8V			
PTX30WCC16D7C2	VDMCU – 3.3V			

8. Revision History

Revision	Date	Description
1.02	Sep 4, 2024	▪ Changed SDK version to 2.4.2 from 2.4.0 and added note 2 in Table 25. ▪ Updated Figure 36.
1.01	Aug 13, 2024	▪ Updated block diagram (external load switch instead of multiple MOSFET switches proposed) ▪ Changed maximum value of ambient temperature to +70°C from +85°C ▪ Updated PTX30W state diagram ▪ Added host parameters introduced with firmware version 5259 ▪ Added table with firmware versions
1.00	Aug 2, 2023	Initial release.

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