



**THE DATASHEET OF  
JANTXV1N5313UR-1**



## ISO652x General Purpose Dual-Channel Functional Isolators

### 1 Features

- Dual channel, CMOS output functional isolators
- 50Mbps data rate
- Robust SiO<sub>2</sub> isolation barrier with ±150kV/μs typical CMTI
- Functional Isolation (8-REU):
  - 450V<sub>RMS</sub>, 637V<sub>DC</sub> working voltage
  - 2000V<sub>RMS</sub>, 2828V<sub>DC</sub> transient voltage (60s)
- Functional Isolation (8-D):
  - 450V<sub>RMS</sub>, 637V<sub>DC</sub> working voltage
  - 2000V<sub>RMS</sub>, 2828V<sub>DC</sub> transient voltage (60s)
- Available in a compact 8-REU package with >2.2mm creepage
- Wide supply range: 1.71V to 1.89V and 2.25V to 5.5V
- 1.71V to 5.5V level translation
- Default output *High* (ISO652x) and *Low* (ISO652xF) Options
- Wide temperature range: –40°C to 125°C
- 1.8mA per channel typical at 1Mbps at 3.3V
- Low propagation delay: 11ns typical at 3.3V
- Robust electromagnetic compatibility (EMC)
  - System-Level ESD, EFT, and surge immunity
  - Ultra-low emissions
- Leadless-DFN (8-REU) package and Narrow-SOIC (8-D) package options

### 2 Applications

- [Power supplies](#)
- [Grid, Electricity meter](#)
- [Motor drives](#)
- [Factory automation](#)
- [Building automation](#)
- [Lighting](#)
- [Appliances](#)

### 3 Description

The ISO652x devices are high-performance, dual-channel functional isolators designed for cost sensitive, space constrained applications that require isolation for non-safety applications. The isolation barrier supports a working voltage of 450V<sub>RMS</sub> / 637V<sub>DC</sub> and transient over voltages of 2000V<sub>RMS</sub> / 2828V<sub>DC</sub>.

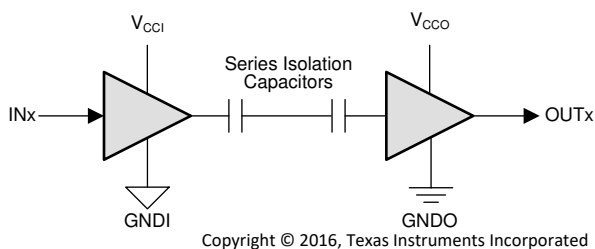
The devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by TI's double capacitive silicon dioxide (SiO<sub>2</sub>) insulation barrier. ISO6520 has two isolation channels with both channels in the same direction. ISO6521 has two isolation channels with one channel in each direction. In the event of input power or signal loss, the default output is *high* for devices without suffix F and *low* for devices with suffix F. See [Device Functional Modes](#) section for further details.

These devices help prevent noise currents on data buses, such as UART, SPI, RS-485, RS-232, and CAN from damaging sensitive circuitry. Through chip design and layout techniques, the electromagnetic compatibility of the devices have been significantly enhanced to ease system-level ESD and emissions compliance.

#### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
ISO6520, ISO6520F	DFN (8-REU)	3.0mm × 2.0mm
ISO6521, ISO6521F		
ISO6520, ISO6520F	D (8)	4.9mm × 6.0mm
ISO6521, ISO6521F		

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



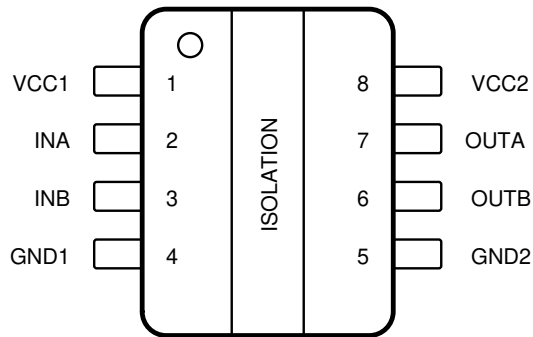
V<sub>CCI</sub>=Input supply, V<sub>CCO</sub>=Output supply  
GNDI=Input ground, GNDO=Output ground

### Simplified Schematic

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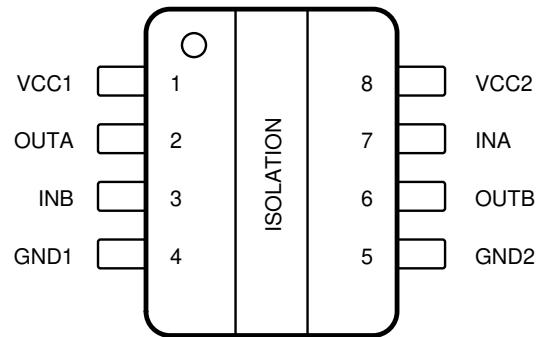
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## 4 Pin Configuration and Functions



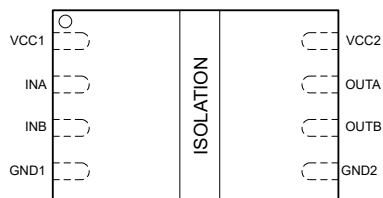
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**Figure 4-1. ISO6520 D Package 8-Pin SOIC Top View**

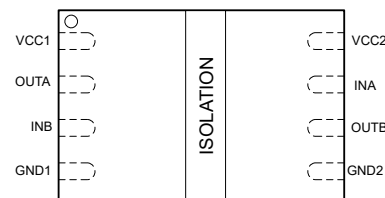


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**Figure 4-2. ISO6521 D Package 8-Pin SOIC Top View**



**Figure 4-3. ISO6520 DFN Package 8-Pin REU Top View**



**Figure 4-4. ISO6521 DFN Package 8-Pin REU Top View**

**Table 4-1. Pin Functions**

NAME	PIN		TYPE <sup>(1)</sup>	Description
	ISO6520	ISO6521		
GND1	4	4	-	Ground connection for V <sub>CC1</sub>
GND2	5	5	-	Ground connection for V <sub>CC2</sub>
INA	2	7	I	Input, channel A
INB	3	3	I	Input, channel B
OUTA	7	2	O	Output, channel A
OUTB	6	6	O	Output, channel B
V <sub>CC1</sub>	1	1	P	Power supply, V <sub>CC1</sub>
V <sub>CC2</sub>	8	8	P	Power supply, V <sub>CC2</sub>

(1) I = Input, O = Output, P = Power

## 5 Specifications

### 5.1 Absolute Maximum Ratings

See<sup>(1)</sup>

		MIN	MAX	UNIT
Supply Voltage <sup>(2)</sup>	V <sub>CC1</sub> to GND1	-0.5	6	V
	V <sub>CC2</sub> to GND2	-0.5	6	
Input/Output Voltage	INx to GNDx	-0.5	V <sub>CCX</sub> + 0.5 <sup>(3)</sup>	V
	OUTx to GNDx	-0.5	V <sub>CCX</sub> + 0.5 <sup>(3)</sup>	
Output Current	I <sub>o</sub>	-15	15	mA
Temperature	Operating junction temperature, T <sub>J</sub>		150	°C
	Storage temperature, T <sub>stg</sub>	-65	150	°C
Transient Isolation Voltage (REU-8)	AC Voltage, t=60s		2000	V <sub>RMS</sub>
	DC Voltage, t=60s		2828	V <sub>DC</sub>
Transient Isolation Voltage (SOIC-8)	AC Voltage, t=60s		2000	V <sub>RMS</sub>
	DC Voltage, t=60s		2828	V <sub>DC</sub>

- Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
- Maximum voltage must not exceed 6 V.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1500	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V <sub>CC1</sub> <sup>(1)</sup>	Supply Voltage Side 1	V <sub>CC</sub> = 1.8 V <sup>(3)</sup>	1.71		1.89	V
V <sub>CC1</sub> <sup>(1)</sup>	Supply Voltage Side 1	V <sub>CC</sub> = 2.5 V to 5 V <sup>(3)</sup>	2.25		5.5	V
V <sub>CC2</sub> <sup>(1)</sup>	Supply Voltage Side 2	V <sub>CC</sub> = 1.8 V <sup>(3)</sup>	1.71		1.89	V
V <sub>CC2</sub> <sup>(1)</sup>	Supply Voltage Side 2	V <sub>CC</sub> = 2.5 V to 5 V <sup>(3)</sup>	2.25		5.5	V
V <sub>CC</sub> (UVLO+)	UVLO threshold when supply voltage is rising			1.53	1.71	V
V <sub>CC</sub> (UVLO-)	UVLO threshold when supply voltage is falling		1.1	1.41		V
V <sub>hys</sub> (UVLO)	Supply voltage UVLO hysteresis		0.08	0.13		V
V <sub>IH</sub>	High level Input voltage		0.7 × V <sub>CCI</sub> <sup>(2)</sup>		V <sub>CCI</sub>	V
V <sub>IL</sub>	Low level Input voltage		0		0.3 × V <sub>CCI</sub>	V

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I <sub>OH</sub>	High level output current	V <sub>CCO</sub> <sup>(2)</sup> = 5 V	-4			mA
		V <sub>CCO</sub> = 3.3 V	-2			mA
		V <sub>CCO</sub> = 2.5 V	-1			mA
		V <sub>CCO</sub> = 1.8 V	-1			mA
I <sub>OL</sub>	Low level output current	V <sub>CCO</sub> = 5 V			4	mA
		V <sub>CCO</sub> = 3.3 V			2	mA
		V <sub>CCO</sub> = 2.5 V			1	mA
		V <sub>CCO</sub> = 1.8 V			1	mA
DR	Data Rate		0		50	Mbps
T <sub>A</sub>	Ambient temperature		-40	25	125	°C
V <sub>IOWM</sub>	Functional Isolation Working Voltage (REU-8)	AC Voltage (sine wave), Time dependent dielectric breakdown (TDDB) Test; See <a href="#">Figure 8-3</a>			450	V <sub>RMS</sub>
		DC Voltage			637	V <sub>DC</sub>
V <sub>IOWM</sub>	Functional Isolation Working Voltage (SOIC-8)	AC Voltage (sine wave)			450	V <sub>RMS</sub>
		DC Voltage			637	V <sub>DC</sub>

- (1) V<sub>CC1</sub> and V<sub>CC2</sub> can be set independent of one another  
(2) V<sub>CC1</sub> = Input-side V<sub>CC</sub>; V<sub>CCO</sub> = Output-side V<sub>CC</sub>  
(3) The channel outputs are in undetermined state when 1.89 V < V<sub>CC1</sub>, V<sub>CC2</sub> < 2.25 V and 1.05 V < V<sub>CC1</sub>, V<sub>CC2</sub> < 1.71 V

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ISO652x		UNIT
		DFN (REU-8)	D (SOIC-8)	
		8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	143.4	104.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	70.0	48.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	78.3	52.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	4.2	7.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	77.7	52.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.5 Package Characteristics

PARAMETER		TEST CONDITIONS	VALUE	VALUE	UNIT
			8-REU	8-D	
CLR	External clearance <sup>(1)</sup>	Shortest pin to pin distance through air	>2.2	>4	mm
CPG	External creepage <sup>(1)</sup>	Shortest pin to pin distance across the package surface	>2.2	>4	mm
CTI	Comparative tracking index	IEC 60112; UL 746A	>400	>400	V
	Material Group	According to IEC 60664-1	II	II	
C <sub>IO</sub>	Capacitance, input to output <sup>(2)</sup>	V <sub>IO</sub> = 0.4 × sin (2 πft), f = 1 MHz	≅0.5	≅0.5	pF
R <sub>IO</sub>	Resistance, input to output <sup>(2)</sup>	T <sub>A</sub> = 25°C	>10 <sup>12</sup>	>10 <sup>12</sup>	Ω

- (1) Creepage and clearance requirements must be applied according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to verify that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.  
(2) All pins on each side of the barrier tied together creating a two-pin device.

## 5.6 Electrical Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -4\text{ mA}$ ; See <a href="#">Figure 6-1</a>	$V_{CCO} - 0.4$			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 4\text{ mA}$ ; See <a href="#">Figure 6-1</a>			0.4	V
$V_{IT+(IN)}$	Rising input switching threshold			$0.7 \times V_{CC1}$ <sup>(1)</sup>		V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CC1}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CC1}$			V
$I_{IH}$	High-level input current	$V_{IH} = V_{CC1}$ <sup>(1)</sup> at INx			10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{IL} = 0\text{ V}$ at INx	-10			$\mu\text{A}$
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V, $V_{CM} = 700\text{V}$ ; See <a href="#">Figure 6-3</a>	100	150		kV/ $\mu\text{s}$
$C_i$	Input Capacitance <sup>(2)</sup>	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$ , $f = 2\text{ MHz}$ , $V_{CC} = 5\text{ V}$		2.8		pF

(1)  $V_{CC1}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ .

(2) Measured from input pin to same side ground.

## 5.7 Supply Current Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
<b>ISO6520</b>								
Supply current - DC signal <sup>(2)</sup>	$V_I = V_{CC1}$ <sup>(1)</sup> (ISO6520), $V_I = 0\text{ V}$ (ISO6520 with F suffix)		$I_{CC1}$		1.1	1.7	mA	
			$I_{CC2}$		1.3	2.2		
	$V_I = 0\text{ V}$ (ISO6520), $V_I = V_{CC1}$ (ISO6520 with F suffix)		$I_{CC1}$		3.2	4.6		
			$I_{CC2}$		1.4	2.3		
Supply current - AC signal <sup>(3)</sup>	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}$		2.1	3.1		
			$I_{CC2}$		1.5	2.4		
		10 Mbps	$I_{CC1}$		2.2	3.2		
			$I_{CC2}$		2.7	3.6		
		50 Mbps	$I_{CC1}$		2.5	3.6		
			$I_{CC2}$		7.9	9.5		
<b>ISO6521</b>								
Supply current - DC signal <sup>(2)</sup>	$V_I = V_{CC1}$ <sup>(1)</sup> (ISO6521); $V_I = 0\text{ V}$ (ISO6521 with F suffix)		$I_{CC1}, I_{CC2}$		1.2	2.2	mA	
			$I_{CC1}, I_{CC2}$		2.3	3.5		
Supply current - AC signal <sup>(3)</sup>	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}, I_{CC2}$		1.9	2.9		
			10 Mbps	$I_{CC1}, I_{CC2}$		2.5		3.6
				50 Mbps	$I_{CC1}, I_{CC2}$			5.2

(1)  $V_{CC1}$  = Input-side  $V_{CC}$

(2) Supply current valid for ENx =  $V_{CCx}$  and ENx = 0V

(3) Supply current valid for ENx =  $V_{CCx}$

## 5.8 Electrical Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -2\text{mA}$ ; See <a href="#">Figure 6-1</a>	$V_{CCO} - 0.2$			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 2\text{mA}$ ; See <a href="#">Figure 6-1</a>			0.2	V
$V_{IT+(IN)}$	Rising input switching threshold			$0.7 \times V_{CCI}$ <sup>(1)</sup>		V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$			V
$I_{IH}$	High-level input current	$V_{IH} = V_{CCI}$ <sup>(1)</sup> at INx			10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{IL} = 0\text{ V}$ at INx	-10			$\mu\text{A}$
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V, $V_{CM} = 700\text{V}$ ; See <a href="#">Figure 6-3</a>	100	150		kV/ $\mu\text{s}$
$C_i$	Input Capacitance <sup>(2)</sup>	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$ , $f = 2\text{ MHz}$ , $V_{CC} = 3.3\text{ V}$		2.8		pF

- (1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ .  
(2) Measured from input pin to same side ground.

## 5.9 Supply Current Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
<b>ISO6520</b>						
Supply current - DC signal <sup>(2)</sup>	$V_I = V_{CCI}$ <sup>(1)</sup> (ISO6520), $V_I = 0\text{ V}$ (ISO6520 with F suffix)	$I_{CC1}$		1.1	1.6	mA
		$I_{CC2}$		1.3	2.2	
	$V_I = 0\text{ V}$ (ISO6520), $V_I = V_{CC1}$ (ISO6520 with F suffix)	$I_{CC1}$		3.2	4.5	
		$I_{CC2}$		1.4	2.3	
Supply current - AC signal <sup>(3)</sup>	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}$		2.1	3.1
			$I_{CC2}$		1.4	2.3
		10 Mbps	$I_{CC1}$		2.2	3.1
			$I_{CC2}$		2.3	3.2
		50 Mbps	$I_{CC1}$		2.4	3.4
			$I_{CC2}$		6	7.3
<b>ISO6521</b>						
Supply current - DC signal <sup>(2)</sup>	$V_I = V_{CCI}$ <sup>(1)</sup> (ISO6521); $V_I = 0\text{ V}$ (ISO6521 with F suffix)	$I_{CC1}, I_{CC2}$		1.2	2.2	mA
		$I_{CC1}, I_{CC2}$		2.3	3.5	
Supply current - AC signal <sup>(3)</sup>	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}, I_{CC2}$		1.8	
		10 Mbps	$I_{CC1}, I_{CC2}$		2.3	3.4
		50 Mbps	$I_{CC1}, I_{CC2}$		4.2	5.5

- (1)  $V_{CCI}$  = Input-side  $V_{CC}$ .  
(2) Supply current valid for  $ENx = V_{CCx}$  and  $ENx = 0\text{ V}$ .  
(3) Supply current valid for  $ENx = V_{CCx}$ .

## 5.10 Electrical Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -1\text{ mA}$ ; See <a href="#">Figure 6-1</a>	$V_{CCO} - 0.1$			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 1\text{ mA}$ ; See <a href="#">Figure 6-1</a>			0.1	V
$V_{IT+(IN)}$	Rising input switching threshold			$0.7 \times V_{CCI}$ <sup>(1)</sup>		V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$			V
$I_{IH}$	High-level input current	$V_{IH} = V_{CCI}$ <sup>(1)</sup> at INx			10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{IL} = 0\text{ V}$ at INx	-10			$\mu\text{A}$
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or $0\text{ V}$ , $V_{CM} = 700\text{ V}$ ; See <a href="#">Figure 6-3</a>	100	150		kV/ $\mu\text{s}$
$C_i$	Input Capacitance <sup>(2)</sup>	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$ , $f = 2\text{ MHz}$ , $V_{CC} = 2.5\text{ V}$		2.8		pF

(1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ .

(2) Measured from input pin to same side ground.

## 5.11 Supply Current Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
<b>ISO6520</b>							
Supply current - DC signal <sup>(2)</sup>	$V_I = V_{CCI}$ <sup>(1)</sup> (ISO6520), $V_I = 0\text{ V}$ (ISO6520 with F suffix)	$I_{CC1}$		1.1	1.6	mA	
		$I_{CC2}$		1.3	2.1		
	$V_I = 0\text{ V}$ (ISO6520), $V_I = V_{CC1}$ (ISO6520 with F suffix)	$I_{CC1}$		3.1	4.5		
		$I_{CC2}$		1.4	2.3		
Supply current - AC signal <sup>(3)</sup>	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}$		2.1		3.1
			$I_{CC2}$		1.4		2.3
		10 Mbps	$I_{CC1}$		2.1	3.1	
			$I_{CC2}$		2	2.9	
		50 Mbps	$I_{CC1}$		2.3	3.3	
			$I_{CC2}$		4.8	6	
<b>ISO6521</b>							
Supply current - DC signal <sup>(2)</sup>	$V_I = V_{CCI}$ <sup>(1)</sup> (ISO6521); $V_I = 0\text{ V}$ (ISO6521 with F suffix)	$I_{CC1}, I_{CC2}$		1.2	2.2	mA	
		$I_{CC1}, I_{CC2}$		2.3	3.5		
Supply current - AC signal <sup>(3)</sup>	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}, I_{CC2}$		1.8		2.9
			$I_{CC1}, I_{CC2}$		2.1		3.2
		10 Mbps	$I_{CC1}, I_{CC2}$		2.1		3.2
			$I_{CC1}, I_{CC2}$		3.6		4.9
		50 Mbps	$I_{CC1}, I_{CC2}$		3.6	4.9	
			$I_{CC1}, I_{CC2}$		3.6	4.9	

(1)  $V_{CCI}$  = Input-side  $V_{CC}$

(2) Supply current valid for  $ENx = V_{CCx}$  and  $ENx = 0\text{ V}$

(3) Supply current valid for  $ENx = V_{CCx}$

## 5.12 Electrical Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2} = 1.8\text{ V} \pm 5\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -1\text{mA}$ ; See <a href="#">Figure 6-1</a>	$V_{CCO} - 0.1$			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 1\text{mA}$ ; See <a href="#">Figure 6-1</a>			0.1	V
$V_{IT+(IN)}$	Rising input switching threshold			$0.7 \times V_{CCI}^{(1)}$		V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$			V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$			V
$I_{IH}$	High-level input current	$V_I = V_{CCI}^{(1)}$ at INx			10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{IL} = 0\text{ V}$ at INx	-10			$\mu\text{A}$
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or $0\text{ V}$ , $V_{CM} = 700\text{V}$ ; See <a href="#">Figure 6-3</a>	100	150		$\text{kV}/\mu\text{s}$
$C_i$	Input Capacitance <sup>(2)</sup>	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$ , $f = 2\text{ MHz}$ , $V_{CC} = 1.8\text{ V}$		2.8		pF

(1)  $V_{CCI}$  = Input-side  $V_{CC}$ ;  $V_{CCO}$  = Output-side  $V_{CC}$ .

(2) Measured from input pin to same side ground.

## 5.13 Supply Current Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2} = 1.8\text{ V} \pm 5\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
<b>ISO6520</b>							
Supply current - DC signal <sup>(2)</sup>	$V_I = V_{CCI}^{(1)}$ (ISO6520), $V_I = 0\text{ V}$ (ISO6520 with F suffix)		$I_{CC1}$		0.8	1.5	mA
			$I_{CC2}$		1.2	2.1	
	$V_I = 0\text{ V}$ (ISO6520), $V_I = V_{CC1}$ (ISO6520 with F suffix)		$I_{CC1}$		2.8	4.3	
			$I_{CC2}$		1.3	2.3	
Supply current - AC signal <sup>(3)</sup>	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}$		1.8	2.9	
			$I_{CC2}$		1.3	2.3	
		10 Mbps	$I_{CC1}$		1.8	2.9	
			$I_{CC2}$		1.8	2.7	
		50 Mbps	$I_{CC1}$		2	3.1	
			$I_{CC2}$		3.8	4.9	
<b>ISO6521</b>							
Supply current - DC signal <sup>(2)</sup>	$V_I = V_{CCI}^{(1)}$ (ISO6521); $V_I = 0\text{ V}$ (ISO6521 with F suffix)		$I_{CC1}, I_{CC2}$		1.1	2.1	mA
			$I_{CC1}, I_{CC2}$		2.1	3.4	
Supply current - AC signal <sup>(3)</sup>	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}, I_{CC2}$		1.6	2.7	
		10 Mbps	$I_{CC1}, I_{CC2}$		1.9	3	
		50 Mbps	$I_{CC1}, I_{CC2}$		3	4.2	

(1)  $V_{CCI}$  = Input-side  $V_{CC}$

(2) Supply current valid for ENx =  $V_{CCx}$  and ENx = 0V

(3) Supply current valid for ENx =  $V_{CCx}$

## 5.14 Switching Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	See <a href="#">Figure 6-1</a>		11	18	ns
$t_{P(dft)}$	Propagation delay drift			8		ps/°C
$t_{UI}$	Minimum pulse width	See <a href="#">Figure 6-1</a>	20			ns
PWD	Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $	See <a href="#">Figure 6-1</a>		0.2	7	ns
$t_{sk(o)}$	Channel-to-channel output skew time <sup>(2)</sup>	Same direction channels			6	ns
$t_{sk(p-p)}$	Part-to-part skew time <sup>(3)</sup>				6	ns
$t_r$	Output signal rise time	See <a href="#">Figure 6-1</a>		2.6	4.5	ns
$t_f$	Output signal fall time			2.6	4.5	ns
$t_{PU}$	Time from UVLO to valid output data				300	μs
$t_{DO}$	Default output delay time from input power loss	Measured from the time $V_{CC}$ goes below 1.2V. See <a href="#">Figure 6-2</a>		0.1	0.3	μs
$t_{ie}$	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.

(2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 5.15 Switching Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	See <a href="#">Figure 6-1</a>		11	18	ns
$t_{P(dft)}$	Propagation delay drift			9.2		ps/°C
$t_{UI}$	Minimum pulse width	See <a href="#">Figure 6-1</a>	20			ns
PWD	Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $	See <a href="#">Figure 6-1</a>		0.5	7	ns
$t_{sk(o)}$	Channel-to-channel output skew time <sup>(2)</sup>	Same direction channels			6	ns
$t_{sk(p-p)}$	Part-to-part skew time <sup>(3)</sup>				6	ns
$t_r$	Output signal rise time	See <a href="#">Figure 6-1</a>		1.6	3.2	ns
$t_f$	Output signal fall time			1.6	3.2	ns
$t_{PU}$	Time from UVLO to valid output data				300	μs
$t_{DO}$	Default output delay time from input power loss	Measured from the time $V_{CC}$ goes below 1.2V. See <a href="#">Figure 6-2</a>		0.1	0.3	μs
$t_{ie}$	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.

(2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 5.16 Switching Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	See <a href="#">Figure 6-1</a>		12	20.5	ns
$t_{P(dft)}$	Propagation delay drift			14.3		ps/°C
$t_{UI}$	Minimum pulse width	See <a href="#">Figure 6-1</a>	20			ns
PWD	Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $	See <a href="#">Figure 6-1</a>		0.6	7.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time <sup>(2)</sup>	Same direction channels			6	ns
$t_{sk(p-p)}$	Part-to-part skew time <sup>(3)</sup>				6.1	ns
$t_r$	Output signal rise time	See <a href="#">Figure 6-1</a>		2	4	ns
$t_f$	Output signal fall time			2	4	ns
$t_{PU}$	Time from UVLO to valid output data				300	μs
$t_{DO}$	Default output delay time from input power loss	Measured from the time $V_{CC}$ goes below 1.2V. See <a href="#">Figure 6-2</a>		0.1	0.3	μs
$t_{ie}$	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.

(2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 5.17 Switching Characteristics—1.8-V Supply

$V_{CC1} = V_{CC2} = 1.8\text{ V} \pm 5\%$  (over recommended operating conditions unless otherwise noted)

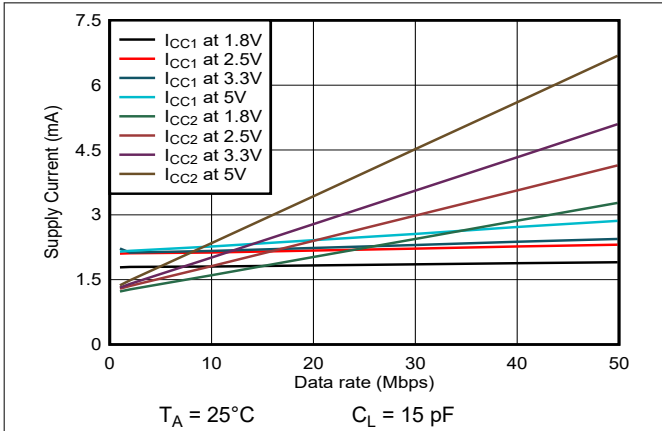
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay time	See <a href="#">Figure 7-1</a>		15	25.1	ns
$t_{P(dft)}$	Propagation delay drift			15.2		ps/°C
$t_{UI}$	Minimum pulse width	See <a href="#">Figure 7-1</a>	20			ns
PWD	Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $	See <a href="#">Figure 7-1</a>		0.7	8.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time <sup>(2)</sup>	Same direction channels			6	ns
$t_{sk(p-p)}$	Part-to-part skew time <sup>(3)</sup>				8.8	ns
$t_r$	Output signal rise time	See <a href="#">Figure 7-1</a>		2.7	5.3	ns
$t_f$	Output signal fall time			2.7	5.3	ns
$t_{PU}$	Time from UVLO to valid output data				300	μs
$t_{DO}$	Default output delay time from input power loss	Measured from the time $V_{CC}$ goes below 1.2V. See <a href="#">Figure 6-2</a>		0.1	0.3	μs
$t_{ie}$	Time interval error	$2^{16} - 1$ PRBS data at 50 Mbps		1		ns

(1) Also known as pulse skew.

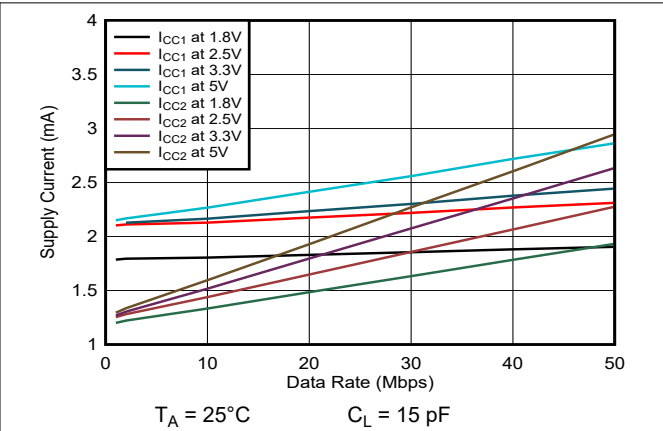
(2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

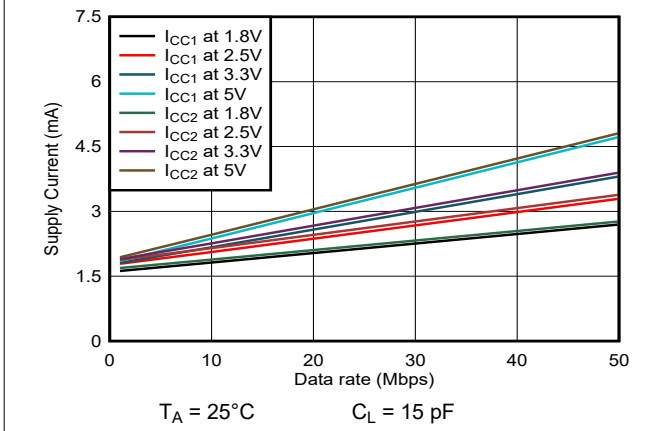
### 5.18 Typical Characteristics



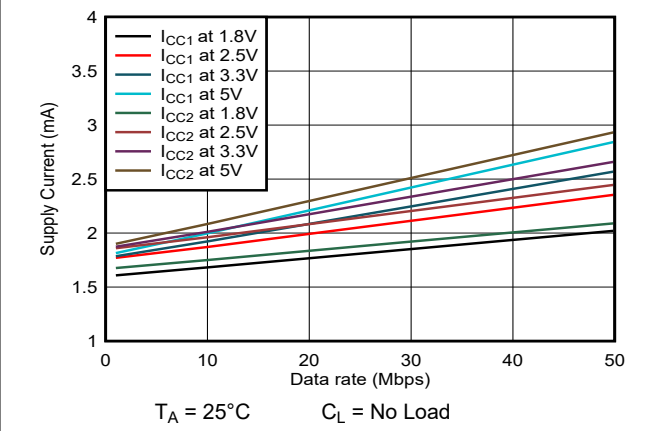
**Figure 5-1. ISO6520 Supply Current vs Data Rate (With 15-pF Load)**



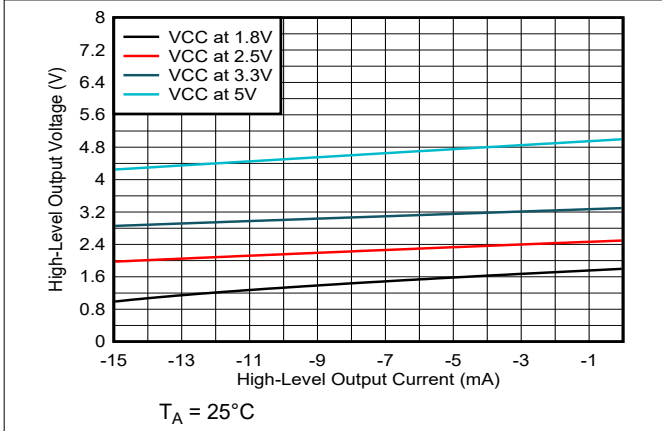
**Figure 5-2. ISO6520 Supply Current vs Data Rate (With No Load)**



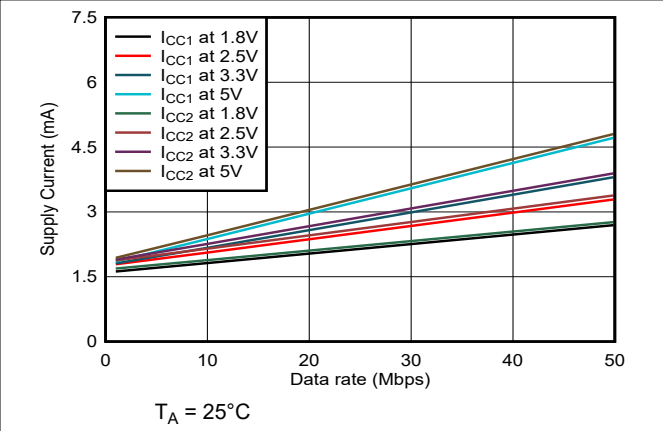
**Figure 5-3. ISO6521 Supply Current vs Data Rate (With 15-pF Load)**



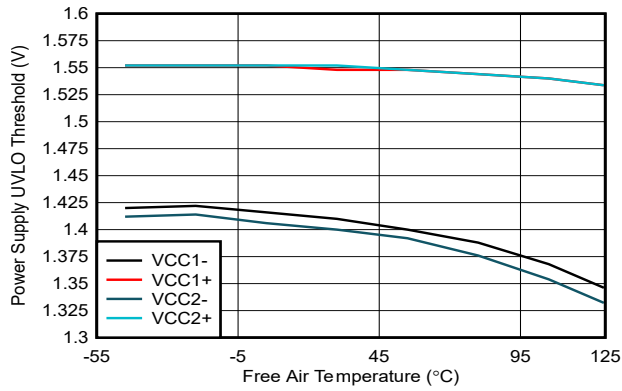
**Figure 5-4. ISO6521 Supply Current vs Data Rate (With No Load)**



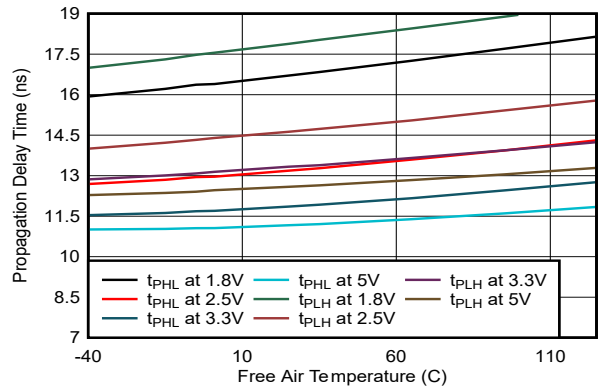
**Figure 5-5. High-Level Output Voltage vs High-level Output Current**



**Figure 5-6. Low-Level Output Voltage vs Low-Level Output Current**

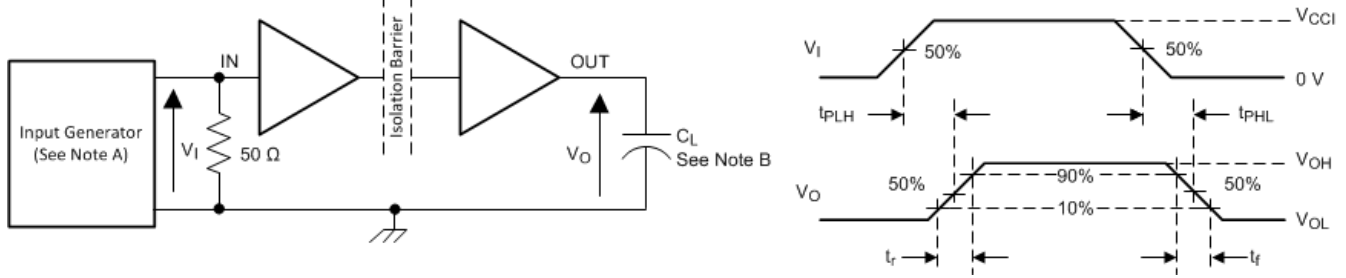


**Figure 5-7. Power Supply Undervoltage Threshold vs Free-Air Temperature**



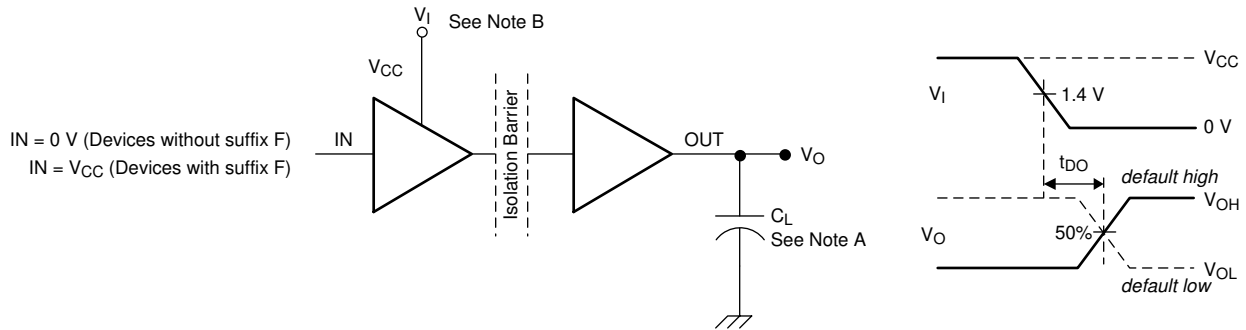
**Figure 5-8. Propagation Delay Time vs Free-Air Temperature**

## 6 Parameter Measurement Information



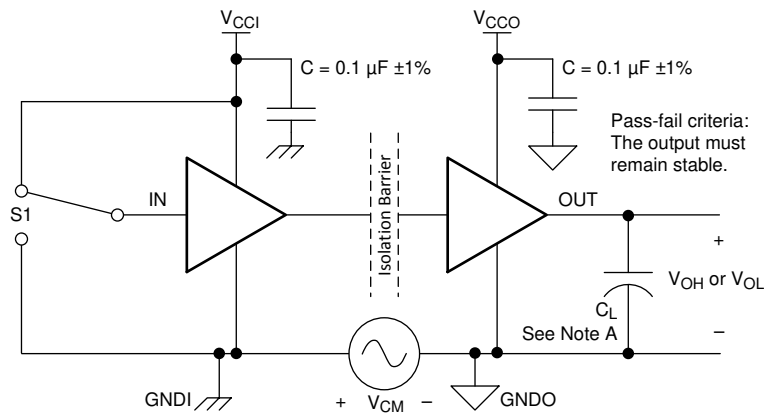
- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  50 kHz, 50% duty cycle,  $t_r \leq$  3 ns,  $t_f \leq$  3 ns,  $Z_O = 50 \Omega$ . At the input, 50  $\Omega$  resistor is required to terminate Input Generator signal. The 50  $\Omega$  resistor is not needed in the actual application.
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Figure 6-1. Switching Characteristics Test Circuit and Voltage Waveforms**



- A.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .
- B. Power Supply Ramp Rate = 10 mV/ns

**Figure 6-2. Default Output Delay Time Test Circuit and Voltage Waveforms**



- A.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

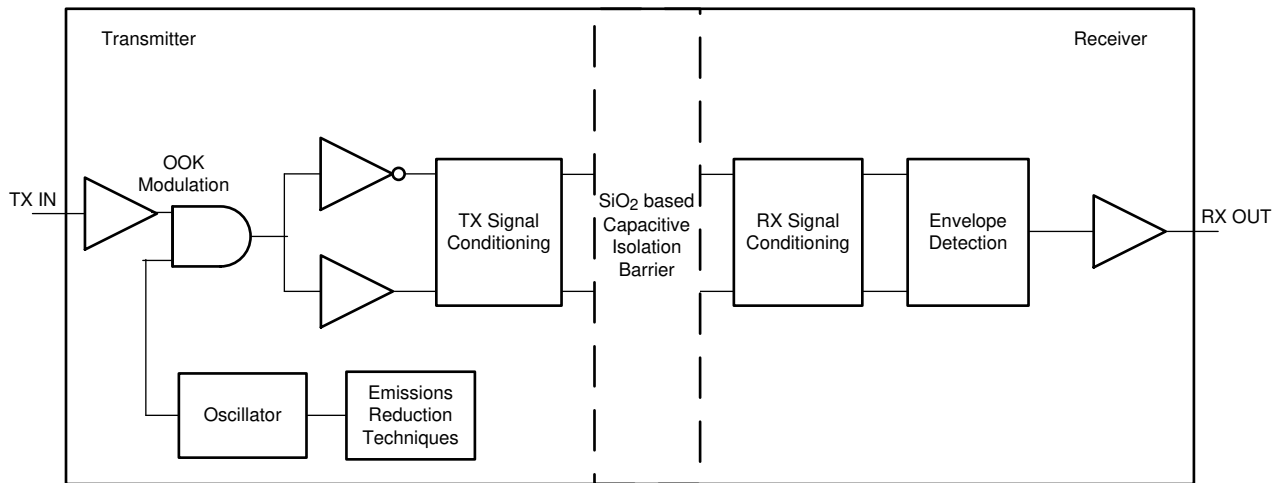
**Figure 6-3. Common-Mode Transient Immunity Test Circuit**

## 7 Detailed Description

### 7.1 Overview

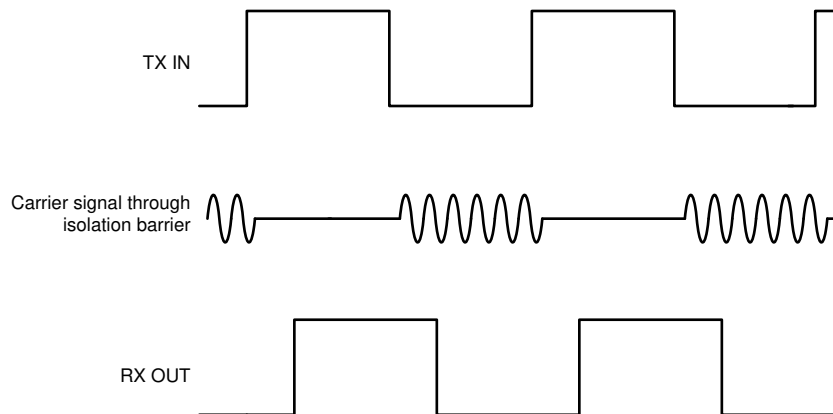
The ISO652x family of devices has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. These devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, [Figure 7-1](#), shows a functional block diagram of a typical channel.

### 7.2 Functional Block Diagram



**Figure 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator**

[Figure 7-2](#) shows a conceptual detail of how the OOK scheme works.



**Figure 7-2. On-Off Keying (OOK) Based Modulation Scheme**

### 7.3 Feature Description

family of devices is available in two channel configurations and default output state options to enable a variety of application uses. lists the device features of the devices.

**Table 7-1. Device Features**

PART NUMBER	MAXIMUM DATA RATE	CHANNEL DIRECTION	DEFAULT OUTPUT STATE	PACKAGE
ISO6520	50 Mbps	2 Forward, 0 Reverse	High	REU-8
ISO6520F	50 Mbps	2 Forward, 0 Reverse	Low	REU-8
ISO6521	50 Mbps	1 Forward, 1 Reverse	High	REU-8
ISO6521F	50 Mbps	1 Forward, 1 Reverse	Low	REU-8

### 7.4 Device Functional Modes

Table 7-2 lists the functional modes for the devices.

**Table 7-2. Function Table**

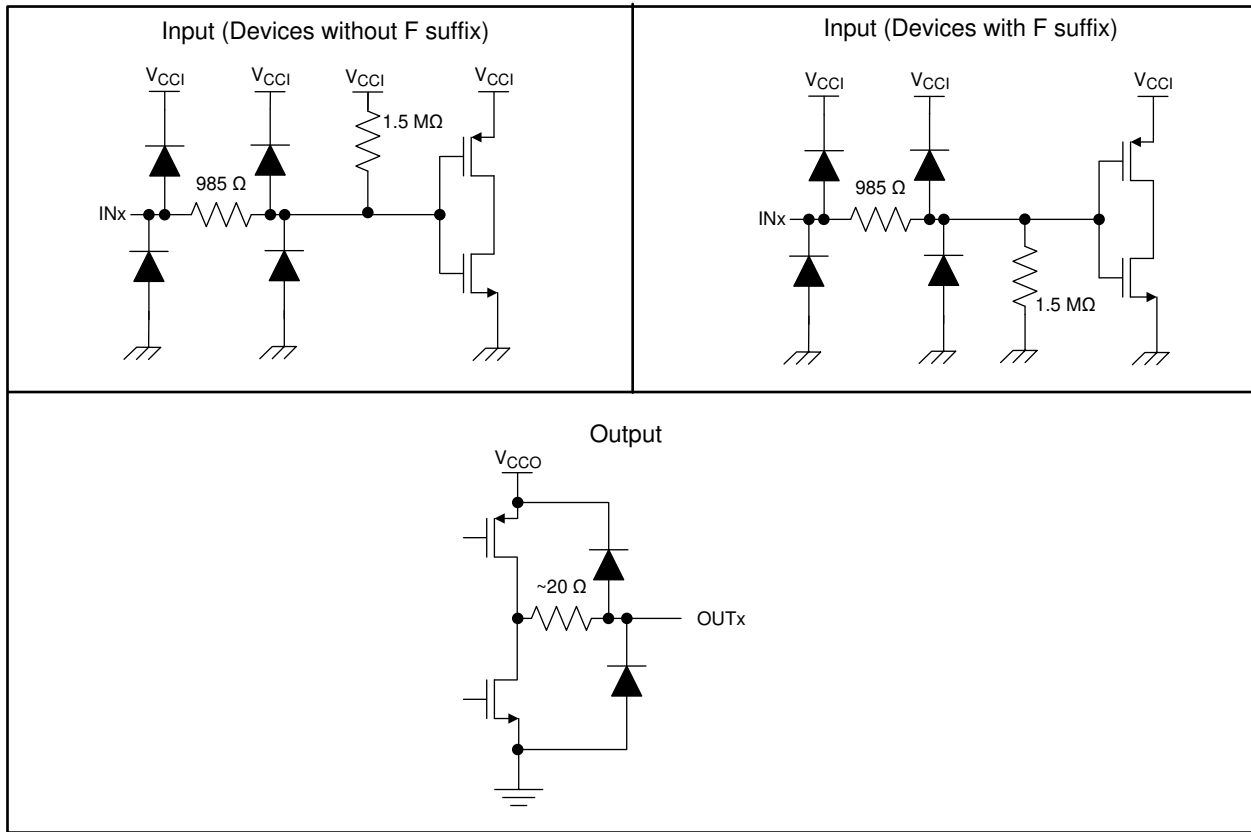
V <sub>CCI</sub> <sup>(1)</sup>	V <sub>CCO</sub>	INPUT (IN <sub>x</sub> ) <sup>(2)</sup>	OUTPUT (OUT <sub>x</sub> )	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode: When IN <sub>x</sub> is open, the corresponding channel output goes to the default logic state. The default is <i>High</i> for and <i>Low</i> for with F suffix.
PD	PU	X	Default	Default mode: When V <sub>CCI</sub> is unpowered, a channel output assumes the logic state based on the selected default option. The default is <i>High</i> for and <i>Low</i> for with F suffix. When V <sub>CCI</sub> transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V <sub>CCI</sub> transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V <sub>CCO</sub> is unpowered, a channel output is undetermined <sup>(3)</sup> . When V <sub>CCO</sub> transitions from unpowered to powered-up, a channel output assumes the logic state of the input

(1) V<sub>CCI</sub> = Input-side V<sub>CC</sub>; V<sub>CCO</sub> = Output-side V<sub>CC</sub>; PU = Powered up (V<sub>CC</sub> ≥ 1.71V); PD = Powered down (V<sub>CC</sub> ≤ 1.05 V); X = Irrelevant; H = High level; L = Low level

(2) A strongly driven input signal can weakly power the floating V<sub>CC</sub> via an internal protection diode and cause undetermined output.

(3) The outputs are in undetermined state when 1.89 V < V<sub>CCI</sub>, V<sub>CCO</sub> < 2.25 V and 1.05 V < V<sub>CCI</sub>, V<sub>CCO</sub> < 1.71 V

### 7.4.1 Device I/O Schematics



**Figure 7-3. Device I/O Schematics**



### 8.2.1 Design Requirements

To design with these devices, use the parameters listed in [Table 8-1](#).

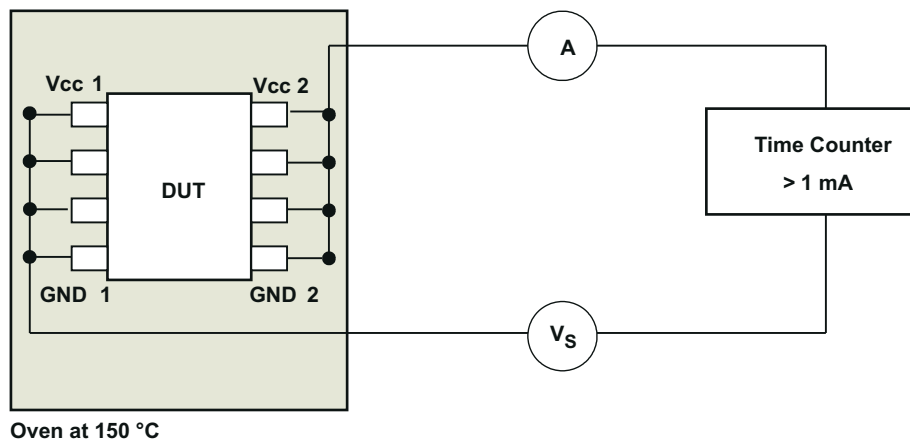
**Table 8-1. Design Parameters**

PARAMETER	VALUE
Supply voltage, $V_{CC1}$ and $V_{CC2}$	1.71 V to 1.89 V and 2.25 V to 5.5 V
Decoupling capacitor between $V_{CC1}$ and GND1	0.1 $\mu$ F
Decoupling capacitor from $V_{CC2}$ and GND2	0.1 $\mu$ F

### 8.3 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See [Figure 8-2](#) for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature.

[Figure 8-3](#) shows the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the barrier. Based on the TDDB data, the intrinsic capability of the insulation is 450  $V_{RMS}$  with a lifetime of >100 years for ISO652x including both REU-8 and 8-D package. Other factors, such as package size, pollution degree, material group, and more can further limit the working voltage of the component. At the lower working voltages, the corresponding insulation lifetime is much longer than 100 years.



**Figure 8-2. Test Setup for Insulation Lifetime Measurement**

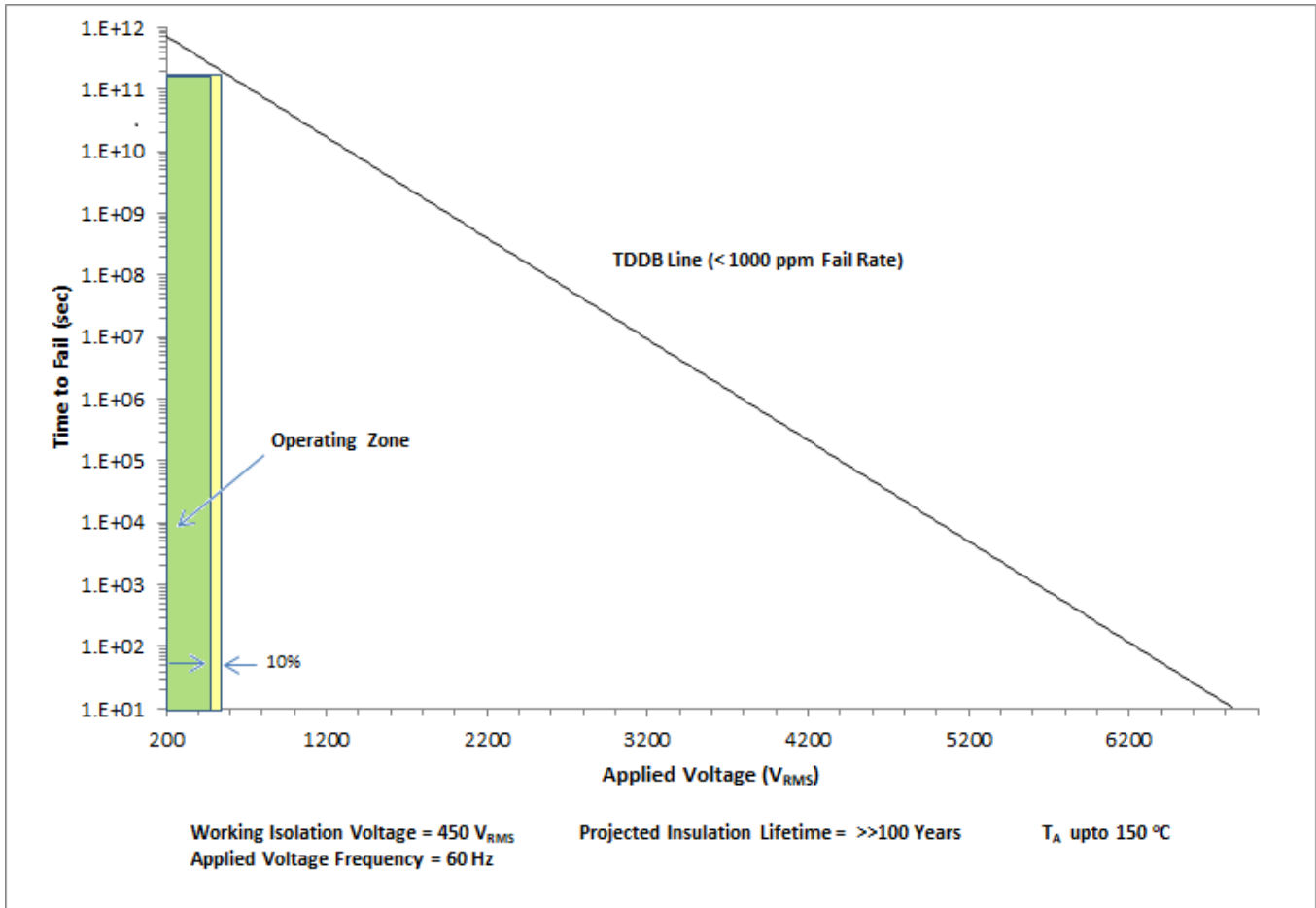


Figure 8-3. Insulation Lifetime Projection Data

## 8.4 Power Supply Recommendations

To provide reliable operation at data rates and supply voltages, a 0.1- $\mu$ F bypass capacitor is recommended at the input and output supply pins ( $V_{CC1}$  and  $V_{CC2}$ ). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver. For industrial applications, please use Texas Instruments' [SN6501](#) or [SN6505B](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501 Transformer Drivers for Isolated Power Supplies](#) or [SN6505B-Q1 Low-noise, 1-A Transformer Drivers for Isolated Power Supplies](#).

## 8.5 Layout

### 8.5.1 Layout Guidelines

A minimum of two layers is required to accomplish a cost optimized and low EMI PCB design. To further improve EMI, a four layer board can be used. Layer stacking for a four layer board must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in<sup>2</sup>.

- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.
- Bypass the VCC pin to ground with a low-ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1µF when using a ceramic capacitor with an X5R- or X7R-rated dielectric. The capacitor must be placed as close to the VCC pin as possible in the PCB layout and on the same layer. The capacitor must have a voltage rating greater than the VCC voltage level.

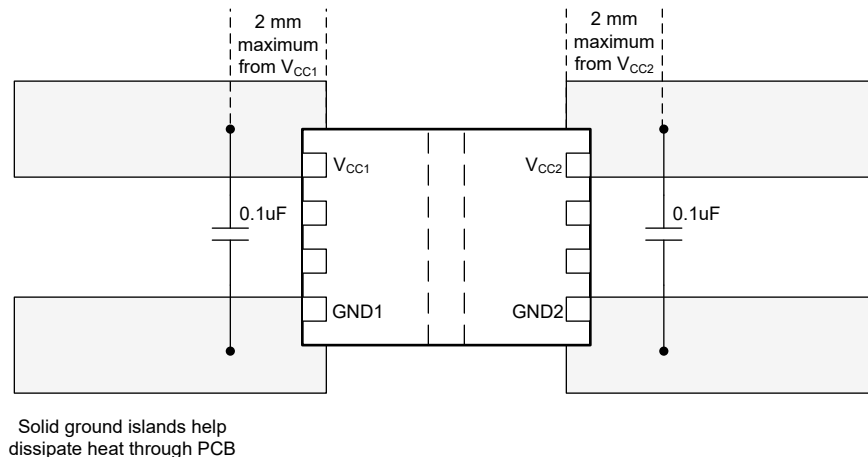
If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This design makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#).

#### 8.5.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

#### 8.5.2 Layout Example



**Figure 8-4. Layout Example**

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Isolation Glossary](#), application note
- Texas Instruments, [SN6501 Transformer Driver for Isolated Power Supplies](#), data sheet
- Texas Instruments, [SN6505x Low-Noise 1-A Transformer Drivers for Isolated Power Supplies](#), data sheet
- Texas Instruments, [SN6507 Low-Emissions, 36-V Push-Pull Transformer Driver with Duty Cycle Control for Isolated Power Supplies](#), data sheet
- Texas Instruments, [LMG341xR070 600-V 70-mΩ GaN with Integrated Driver and Protection](#), data sheet

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

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### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2024) to Revision C (August 2025)	Page
• Updated the number formatting for tables, figures, and cross-references throughout the document.....	1
• Updated Transient Isolation Voltage for REU-8 package to 2000Vrms(AC) and 2828V(DC).....	4
• Updated Transient Isolation Voltage for 8D package to 2000Vrms(AC) and 2828V(DC).....	4
• VIOWM AC Voltage updated for REU-8 package variant.....	4
• VIOWM DC Voltage updated for REU-8 package variant.....	4
• Updated <i>Insulation Lifetime Projection Data</i> image.....	19
• Updated <i>Power Supply Recommendations</i> document references.....	20

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<b>Changes from Revision A (December 2023) to Revision B (April 2024)</b>	<b>Page</b>
• Updated the number formatting for tables, figures, and cross-references throughout the document.....	<a href="#">1</a>
• Added information about the ISO6521F variant throughout the document .....	<a href="#">1</a>

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<b>Changes from Revision * (August 2023) to Revision A (December 2023)</b>	<b>Page</b>
• Updated device status to Production Data.....	<a href="#">1</a>
• Updated Typical Application Diagram.....	<a href="#">18</a>

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## **11 Mechanical, Packaging, and Orderable Information**

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">ISO6520DR</a>	Active	Production	SOIC (D)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6520
ISO6520DR.A	Active	Production	SOIC (D)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6520
<a href="#">ISO6520FDR</a>	Active	Production	SOIC (D)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6520F
ISO6520FDR.A	Active	Production	SOIC (D)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6520F
<a href="#">ISO6520FREUR</a>	Active	Production	VSON (REU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6520F
ISO6520FREUR.A	Active	Production	VSON (REU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6520F
<a href="#">ISO6520REUR</a>	Active	Production	VSON (REU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6520
ISO6520REUR.A	Active	Production	VSON (REU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6520
<a href="#">ISO6521DR</a>	Active	Production	SOIC (D)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6521
ISO6521DR.A	Active	Production	SOIC (D)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6521
<a href="#">ISO6521FDR</a>	Active	Production	SOIC (D)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6521F
ISO6521FDR.A	Active	Production	SOIC (D)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6521F
<a href="#">ISO6521FREUR</a>	Active	Production	VSON (REU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6521F
ISO6521FREUR.A	Active	Production	VSON (REU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6521F
<a href="#">ISO6521REUR</a>	Active	Production	VSON (REU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6521
ISO6521REUR.A	Active	Production	VSON (REU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	6521

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF ISO6520, ISO6521 :**

- Automotive : [ISO6520-Q1](#), [ISO6521-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO6520DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6520FDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6520FREUR	VSON	REU	8	3000	180.0	12.4	2.3	3.3	1.2	4.0	12.0	Q2
ISO6520REUR	VSON	REU	8	3000	180.0	12.4	2.3	3.3	1.2	4.0	12.0	Q2
ISO6521DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6521FDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO6521FREUR	VSON	REU	8	3000	180.0	12.4	2.3	3.3	1.2	4.0	12.0	Q2
ISO6521REUR	VSON	REU	8	3000	180.0	12.4	2.3	3.3	1.2	4.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO6520DR	SOIC	D	8	3000	353.0	353.0	32.0
ISO6520FDR	SOIC	D	8	3000	353.0	353.0	32.0
ISO6520FREUR	VSON	REU	8	3000	210.0	185.0	35.0
ISO6520REUR	VSON	REU	8	3000	210.0	185.0	35.0
ISO6521DR	SOIC	D	8	3000	353.0	353.0	32.0
ISO6521FDR	SOIC	D	8	3000	353.0	353.0	32.0
ISO6521FREUR	VSON	REU	8	3000	210.0	185.0	35.0
ISO6521REUR	VSON	REU	8	3000	210.0	185.0	35.0



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

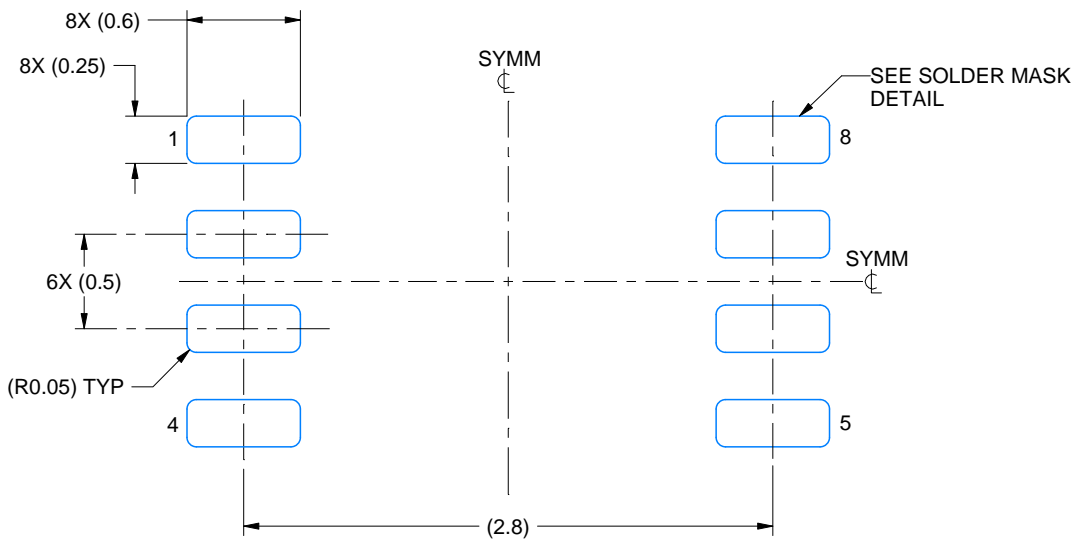


# EXAMPLE BOARD LAYOUT

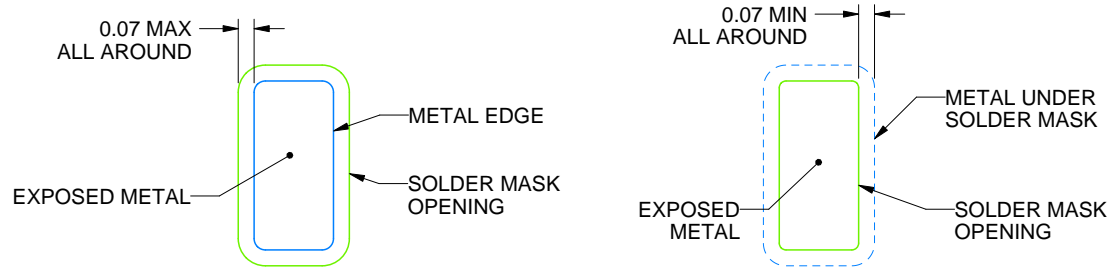
REU0008A

VSON - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



SOLDER MASK DETAILS

4229400/A 02/2023

NOTES: (continued)

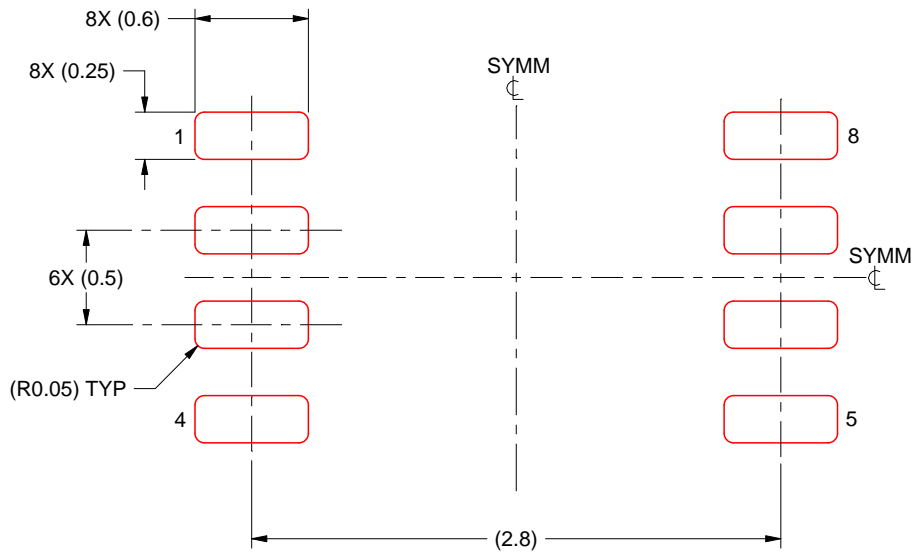
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

REU0008A

VSON - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 25X

4229400/A 02/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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