THE DATASHEET OF

LTC4331IUFD#TRPBF

16V_{IN}, 8A Ultralow Noise Silent Switcher 3 µModule Regulator

FEATURES

- **Complete Solution in <1cm² (Single-Sided PCB) or 0.5cm² (Dual-Sided PCB)**
- **Low Noise Silent Switcher® 3 Architecture**
  - **Ultralow EMI Emissions**
  - **Ultralow RMS Noise (10Hz to 100kHz): 8µV_{RMS}**
- **±1.5% Maximum Total DC Output Voltage Error Over Line, Load, and Temperature**
- Input Voltage Range: 3V to 16V
- Output Voltage Range: 0.3V to 5.7V
- 8A Maximum Continuous Output Current
- Adjustable and Synchronizable: 300kHz to 3MHz
- Current Mode Control, Fast Transient Response
- Forced Continuous Mode (FCM) Capability
- Multiphase Parallel with Current Sharing
- Programmable Power Good
- 6.25mm × 6.25mm × 5.07mm BGA Package

APPLICATIONS

- Telecom, Networking, and Industrial Equipment
- RF Power Supplies: PLLs, VCOs, Mixers, LNAs, PAs
- Low Noise Instrumentation
- High Speed/High Precision Data Converters

DESCRIPTION

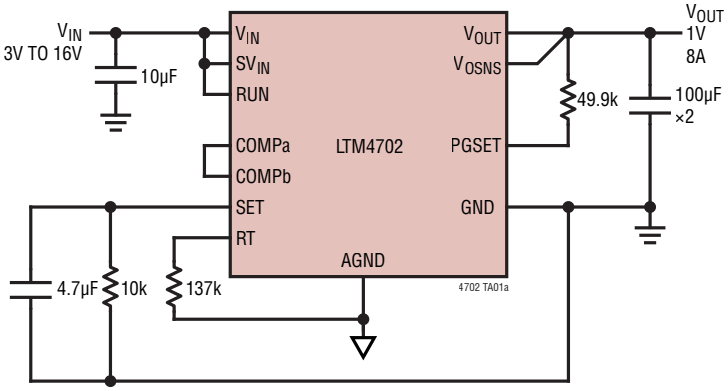
The LTM®4702 is a complete 8A step-down Silent Switcher® 3 µModule® regulator in a tiny 6.25mm × 6.25mm × 5.07mm BGA package. Included in the package are the switching controller, the power MOSFETs, an inductor, and support components. Operating over an input voltage range of 3V to 16V, the LTM4702 supports an output range of 0.3V to 5.7V. A single resistor sets the output voltage, providing unity gain operation over the output range and resulting in virtually constant output noise independent of the output voltage. Only bulk input and output capacitors are needed to finish the design.

The LTM4702 employs Silent Switcher 3 architecture with internal hot loop bypass capacitors to achieve both low EMI and high efficiency. Also, the LTM4702 has an ultralow noise architecture to obtain exceptional low-frequency (<100kHz) output noise. These low EMI and low noise features make the LTM4702 ideal for high current and noise-sensitive applications, which benefit from the high efficiency of a synchronous switching regulator.

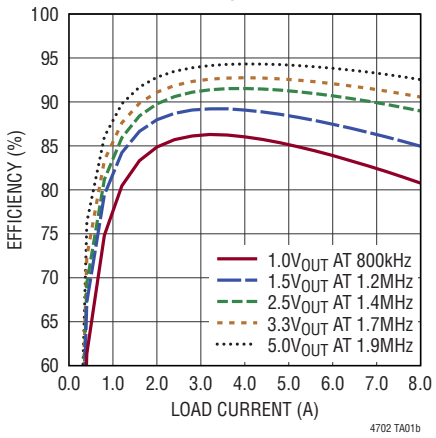
The LTM4702 is available with SnPb or RoHS-compliant terminal finish.

TYPICAL APPLICATION

3V to 16V Input to 1V, 8A Output



Efficiency, V_{IN} = 12V

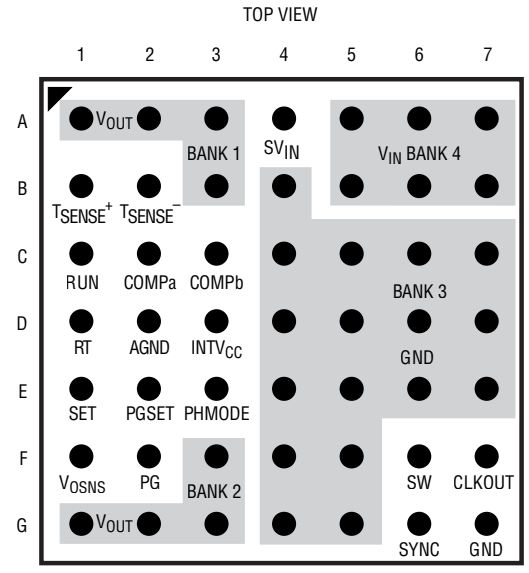


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{IN}, SV_{IN}, RUN, PG 18V
SYNC, V_{OUT}, V_{OSNS}, SET, PGSET 6V
PHMODE, COMPa, RT 4V
T_{SENSE}^+ to T_{SENSE}^- (Current) 5mA
Internal Operating Junction Temperature Range
E-Grade, I-Grade ..... –40° to 125°C
Storage Temperature Range ..... –55° to 125°C
Peak Solder Reflow Body Temperature ..... 250°C

PIN CONFIGURATION



BGA PACKAGE
49-PIN (6.25mm × 6.25mm × 5.07mm)
T_{JMAX} = 125°C, θ_{JA} = 20°C/W, θ_{JCtop} = 31°C/W,
$\theta_{JCbottom}$ = 13.3°C/W, WEIGHT = 0.7g

NOTE:
1. θ VALUES ARE DETERMINED BY SIMULATION PER JESD-51 CONDITIONS.
2. θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
3. SEE THE TYPICAL PERFORMANCE CHARACTERISTICS SECTION FOR LAB MEASUREMENT AND DERATING CURVES.

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4702EY#PBF	SAC305 (RoHS)	4702	e1	BGA	4	–40°C to 125°C
LTM4702IY#PBF	SAC305 (RoHS)	4702	e1	BGA	4	–40°C to 125°C
LTM4702IY	SnPb (63/37)	4702	e0	BGA	4	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the specified internal operating junction temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 12V, per the typical application (Note 5).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Power Input DC Voltage		●	3		16	V
SV_{IN}	Signal Input DC Voltage (Note 8)		●	3		16	V
$V_{OUT(RANGE)}$	Output Voltage Range	V_{PGSET} = 0.5V	●	0.3		5.7	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 10µF, C_{OUT} = 200µF Ceramic, R_{SET} = 10k, FCM, V_{IN} = 3V to 16V, SV_{IN} = 6V, I_{OUT} = 100mA to 8A	●	0.985	1	1.015	V
I_{SET}	SET Pin Current	V_{IN} = SV_{IN} = 6V, R_{SET} = 10k, I_{OUT} = 100mA		99.5	100	100.5	µA
I_{SET_START}	Fast Start-Up Set Pin Current	V_{IN} = SV_{IN} = 6V, V_{SET} = 1V, V_{PGSET} = 0V		2	2.5	3	mA
t_{START}	Start-Up Time (Notes 3, 9)	V_{OUT} = 1V, C_{SET} = 1µF, V_{PGSET} = 0.5V V_{OUT} = 1V, C_{SET} = 4.7µF, V_{PGSET} = 0.5V V_{OUT} = 1V, C_{SET} = 1µF, R_{PGSET} = 49.9k, V_{OUT} = 1V, C_{SET} = 4.7µF, R_{PGSET} = 49.9k			25 120 1 2.5		ms ms ms ms
V_{RUN}	RUN Pin ON Threshold	V_{IN} = SV_{IN} = 6V, V_{RUN} Rising			1.32	1.37	V
	RUN Pin Hysteresis				50		mV
V_{INTVCC}	Internal V_{CC} Voltage			3.2	3.4	3.6	V
I_{Q_SVIN}	SV_{IN} Quiescent Current	SV_{IN} = 12V, V_{RUN} = 0V, Shutdown SV_{IN} = 12V, R_T = 47k, FCM			50 13	 17	µA mA
$V_{OUT\_SPOTNOISE}$	Output Noise Spectral Density (2kHz) (Notes 3, 4, 6, 7)	SV_{IN} = 12V, V_{OUT} = 1V, C_{OUT} = 200µF, R_{SET} = 10k, C_{SET} = 4.7µF, f_{SW} = 2MHz			4		nV/√Hz
$V_{OUT\_RMSNOISE}$	Output RMS Noise (10Hz to 100kHz) (Notes 3, 4, 6, 7)	SV_{IN} = 12V, V_{OUT} = 1V, BW = 10Hz to 100kHz, I_{OUT} = 0.5A, C_{OUT} = 200µF, R_{SET} = 10k, C_{SET} = 4.7µF, 2MHz			8		μV_{RMS}
$I_{OUT(DC)}$	Output Continuous Current	V_{IN} = 12V, V_{OUT} = 1V				8	A
ΔV_{OUT} (LINE)/V_{OUT}	Output Voltage Line Regulation	V_{OUT} = 1V, V_{IN} = 3V to 16V, SV_{IN} = 6V, I_{OUT} = 100mA	●		0.025	0.15	%/V
ΔV_{OUT} (LOAD)/V_{OUT}	Output Voltage Load Regulation	V_{OUT} = 1V, V_{IN} = 6V, SV_{IN} = 6V, I_{OUT} = 100mA to 8A	●			1.35	%
I_{VOSNS}	V_{OSNS} Output Current (Note 10)			80	160	240	nA
$V_{OUT(AC)}$	Output Ripple Voltage (Note 3)	I_{OUT} = 100mA, C_{OUT} = 200µF, V_{IN} = 12V, V_{OUT} = 1V			8		mV
I_{OUT_PK}	Output Current Limit				15		A
t_{ON_MIN}	Minimum On-Time				15		ns
V_{PGSET}	PGSET Upper Threshold PGSET Upper Threshold Hysteresis PGSET Lower Threshold PGSET Lower Threshold Hysteresis	V_{IN} = SV_{IN} = 6V, PGSET Rising PGSET Falling		525 455	540 5 465 5	550 475	mV mV mV mV
I_{PGSET}	PGSET Pin Current	V_{IN} = 6V, V_{PGSET} = 0.5V			10		µA
I_{PG}	PG Leakage	V_{PG} = 3.3V, SV_{IN} = 0V		–40		40	nA
R_{PG}	PG Pull-Down Resistance	V_{PG} = 0.5V			380	650	Ω
f_{OSC}	Oscillator Frequency	R_T = 392k R_T = 47k R_T = 28.7k			300 2 3		kHz MHz MHz
SYNC_LEVEL	SYNC Threshold	V_{IN} = SV_{IN} = 6V, SYNC DC and Clock Low Level Voltage SYNC DC and Clock High Level Voltage		0.7		 1.5	V V
V_{PHMODE}	PHMODE Thresholds	V_{IN} = SV_{IN} = 6V,180° Phase Shift 90° Phase Shift		 2.7		0.7	V V

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4702 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4702E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4702I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: Not subject to production test.

Note 4: V_{OSNS} ties directly to V_{OUT}.

Note 5: EC table test circuits and test conditions could be different than typical applications.

Note 6: Adding a capacitor across the SET pin resistor decreases output voltage noise. Adding this capacitor bypasses the SET pin resistor's thermal noise as well as the reference current's noise. The use of a SET pin bypass capacitor also increases start-up time.

Note 7: See Thermal Considerations for different V_{IN}, V_{OUT}, and T_A.

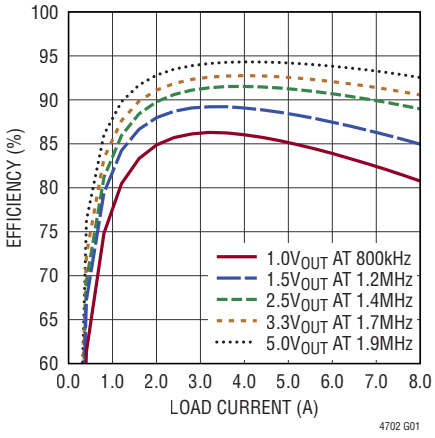
Note 8: SV_{IN} supplies current to the internal circuitry and regulator. SV_{IN} should be above 4V to achieve regulation of ±1.5% maximum total DC output voltage error over line, load, and temperature. Also, in order to provide sufficient headroom for the SET pin current reference, SV_{IN} must be 0.4V higher than the desired V_{OUT}.

Note 9: The start-up time is defined as the time it takes from the RUN pin rising above the RUN threshold to when V_{OUT} has reached 90% of final values.

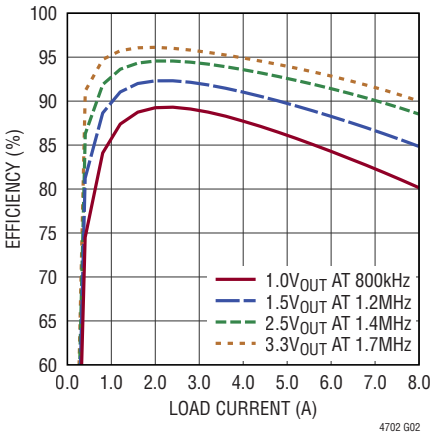
Note 10: Wafer level tested.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

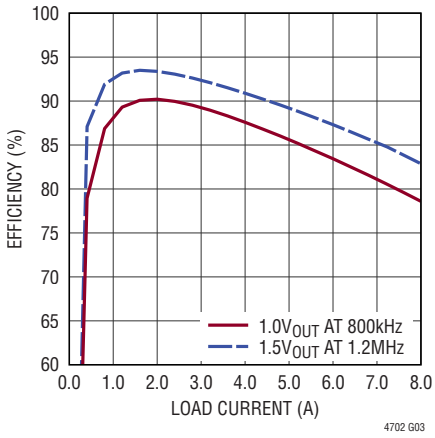
Efficiency vs Load, V_{IN} = 12V



Efficiency vs Load, V_{IN} = 5V

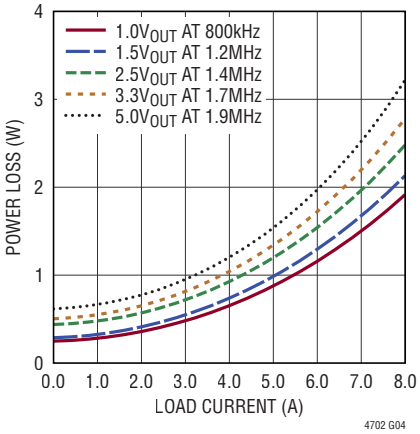


Efficiency vs Load, V_{IN} = 3.3V

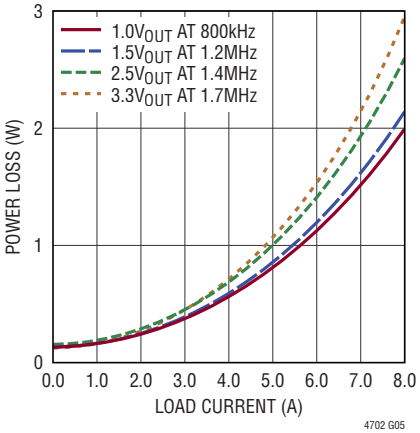


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

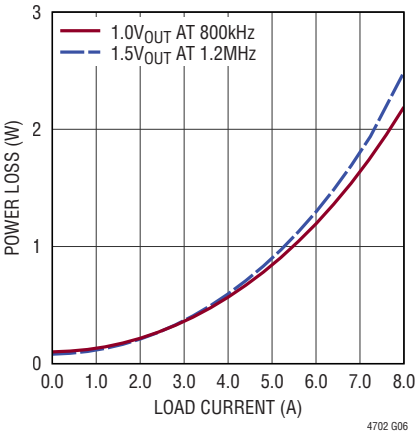
Power Loss vs Load, V_{IN} = 12V



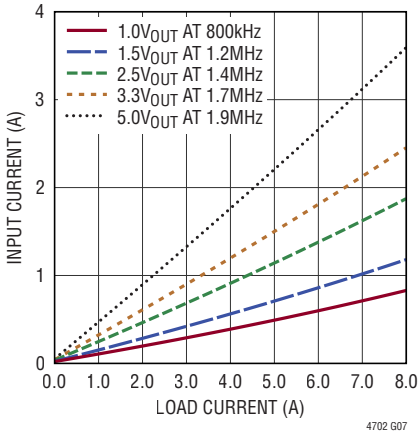
Power Loss vs Load, V_{IN} = 5V



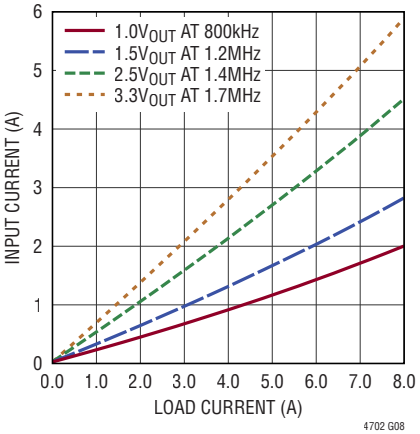
Power Loss vs Load, V_{IN} = 3.3V



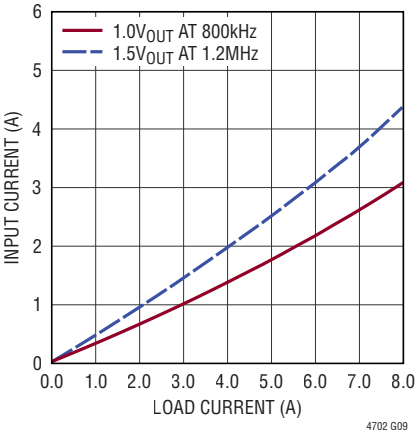
Input vs Load Current, V_{IN} = 12V



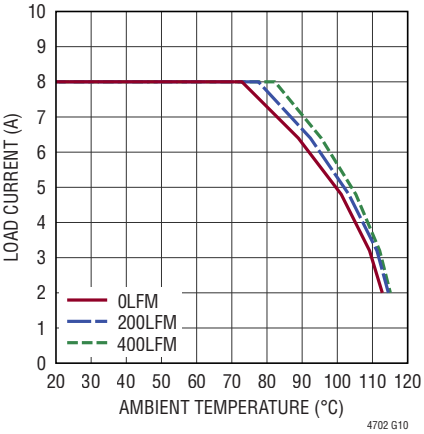
Input vs Load Current, V_{IN} = 5V



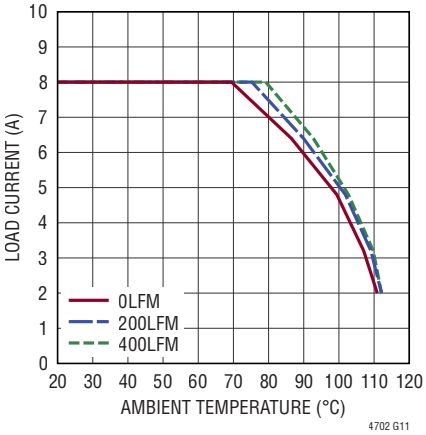
Input vs Load Current, V_{IN} = 3.3V



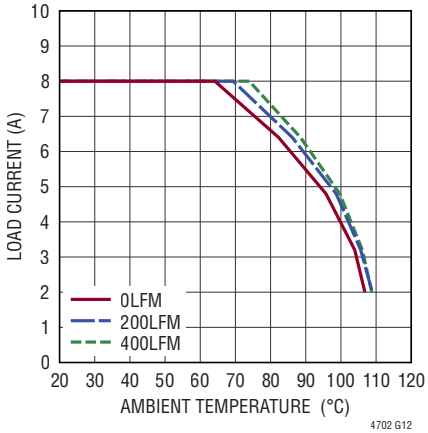
Derating Curve, V_{IN} = 12V, V_{OUT} = 1V



Derating Curve, V_{IN} = 12V, V_{OUT} = 1.5V

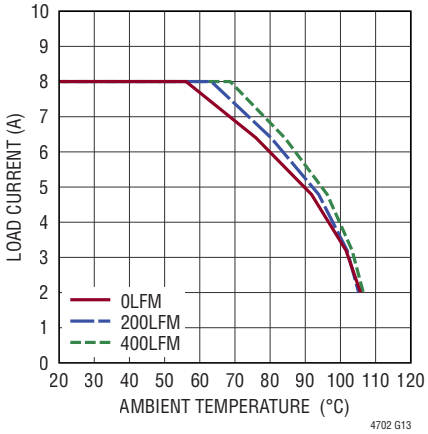


Derating Curve, V_{IN} = 12V, V_{OUT} = 2.5V

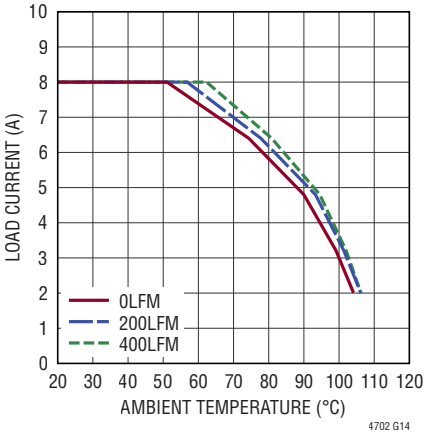


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

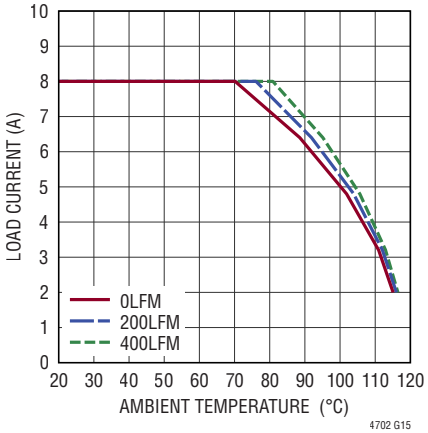
Derating Curve, V_{IN} = 12V, V_{OUT} = 3.3V



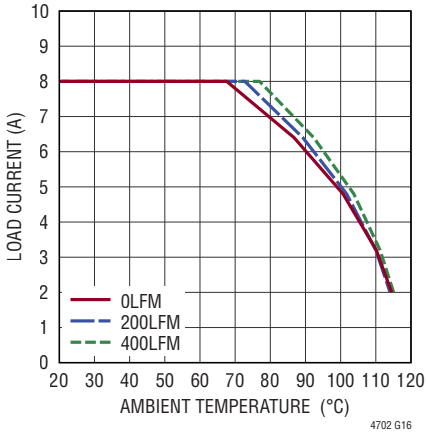
Derating Curve, V_{IN} = 12V, V_{OUT} = 5V



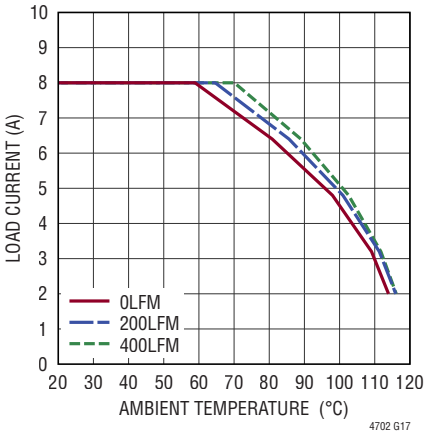
Derating Curve, V_{IN} = 5V, V_{OUT} = 1V



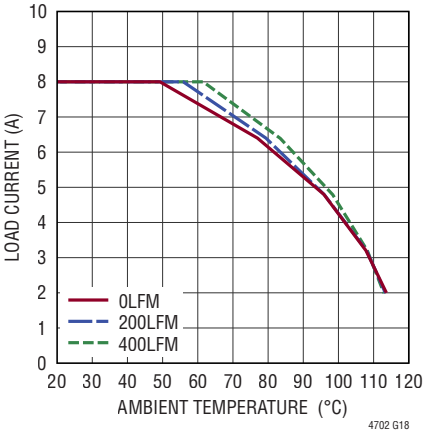
Derating Curve, V_{IN} = 5V, V_{OUT} = 1.5V



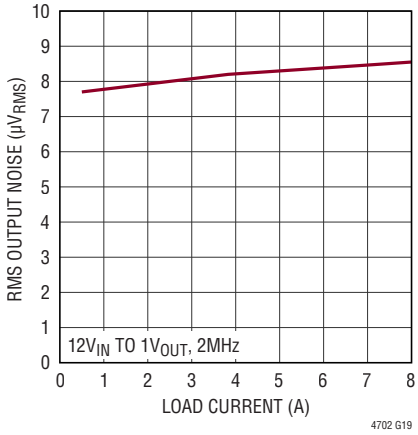
Derating Curve, V_{IN} = 5V, V_{OUT} = 2.5V



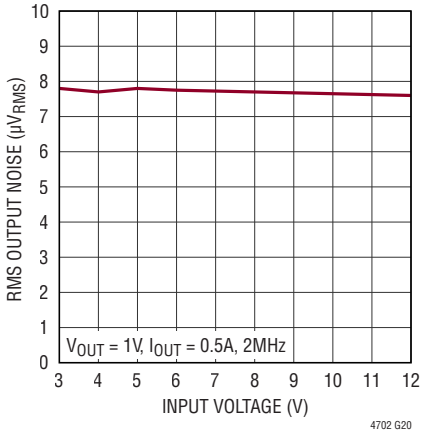
Derating Curve, V_{IN} = 5V, V_{OUT} = 3.3V



Integrated RMS Output Noise vs Load (10Hz to 100kHz)

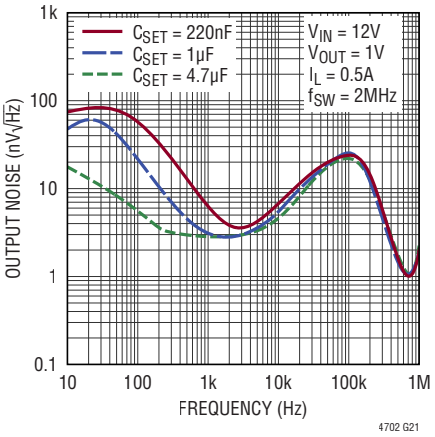


Integrated RMS Output Noise vs Input (10Hz to 100kHz)

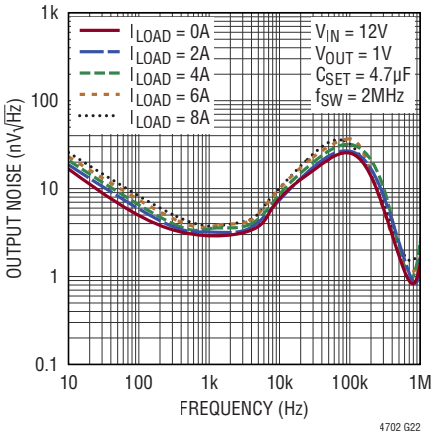


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

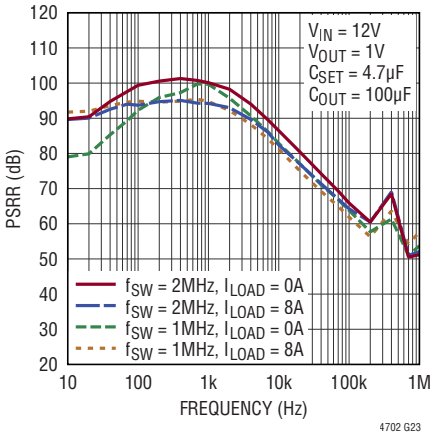
Noise Spectral Density vs C_{SET}



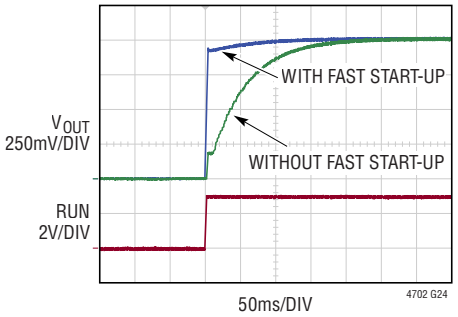
Noise Spectral Density vs Load



Power Supply Ripple Rejection

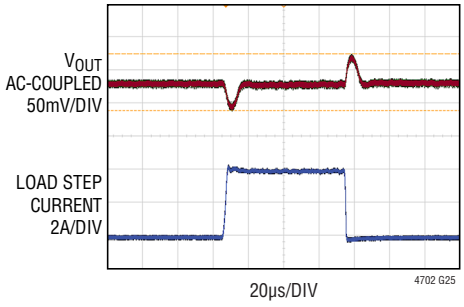


Start-Up Time with and without Fast Start-Up Circuitry (Large C_{SET})



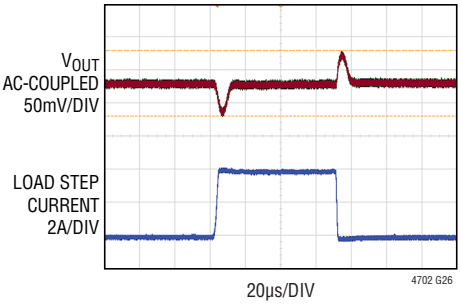
SV$_{IN}$ = 5V
R_{SET} = 10k, C_{SET} = 4.7µF
F_{SW} = 2MHz
R_L = 1Ω

1V Output Transient Response



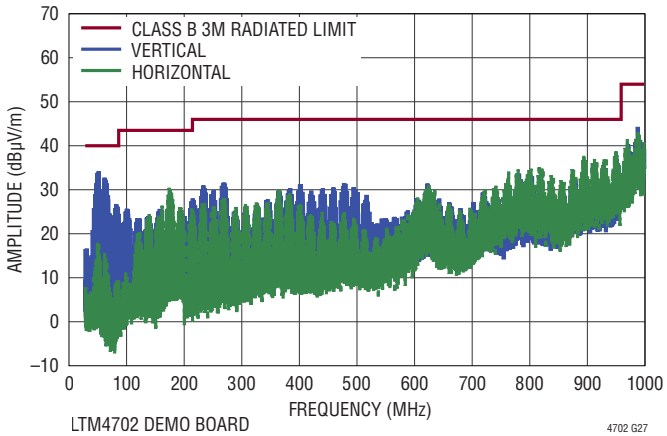
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 4A TO 8A
C_{OUT} = 100µF ×2 CERAMIC CAPACITOR
INTERNAL COMPENSATION, CONNECT COMPa TO COMPb

5V Output Transient Response



V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 4A TO 8A
C_{OUT} = 100µF ×2 CERAMIC CAPACITOR
INTERNAL COMPENSATION, CONNECT COMPa TO COMPb

CISPR22 Class B Emissions



LTM4702 DEMO BOARD
NO EMI FILTER, V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 8A, f_{SW} = 2MHz

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

SV_{IN} (Pin A4): Signal V_{IN}. This pin supplies current to the LTM4702 internal circuitry and regulator. If tied to a different supply other than V_{IN}, place a 1µF local bypass capacitor on this pin.

V_{OUT} (Banks 1 and 2): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitor directly between these pins and GND pins.

GND (Bank 3 and Pin G7): Power Ground Pins for Both Input and Output Returns.

V_{IN} (Bank 4): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitor directly between V_{IN} pins and GND pins.

T_{SENSE}^+ (Pin B1): High Side of the Internal Temperature Monitor Pin. An internal diode connected NPN transistor is placed between T_{SENSE}^+ and T_{SENSE}^- pins. See the Applications Information section.

T_{SENSE}^- (Pin B2): Low Side of the Internal Temperature Monitor Pin.

RUN (Pin C1): Run Control Input. Enables chip operation by tying RUN above 1.32V (Typ). Tying it below 0.4V shuts down the part.

COMPa (Pin C2): Output of the Internal Error Amplifier. The voltage on this pin controls the peak switch current. Tie the COMPa pins from different channels together for parallel operation. Connect to COMPb to use the internal compensation. Or connect to an external RC network to use customized compensation.

COMPb (Pin C3): Internal Compensation Network. Connect to COMPa to use the internal compensation in the majority of applications.

RT (Pin D1): This pin sets the oscillator frequency with an external resistor to AGND.

AGND (Pin D2): Analog Ground. Ground return for SYNC, RT, and COMP pins.

$INTV_{CC}$ (Pin D3): Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. Do not load the $INTV_{CC}$ pin with external circuitry. This pin should be floated.

SET (Pin E1): Output Voltage Set. This pin is the noninverting input of the error amplifier and the regulation setpoint for the LTM4702. SET sources a precision 100µA current that flows through an external resistor connected between SET and GND. The LTM4702's output voltage is determined by $V_{SET} = I_{SET} \bullet R_{SET}$. Output voltage range is from 0.3V to 5.7V. Adding a capacitor from SET to GND improves noise at the expense of increased start-up time. For optimum load regulation, Kelvin connects the ground side of the SET pin resistor directly to the load.

PGSET (Pin E2): Power Good Set. The PG pin pulls low if PGSET increases above 540mV or decreases below 465mV. Connecting a pull-up resistor between V_{OUT} and PGSET sets the programmable power good threshold with Equation 1.

$$R_{PGSET} = (2 \bullet V_{OUT} - 1) \bullet 49.9k \quad (1)$$

As discussed in the Applications Information section, PGSET also activates the fast start-up circuitry. If the power is good and fast start-up functionalities are not needed, the PGSET pin must be tied to an external 0.5V. Do not float the PGSET pin.

PHMODE (Pin E3): The PHMODE pin sets the phase shift of the clock signal of the CLKOUT pin. Tie PHMODE to the ground for a 180-degree phase shift, float for a 120-degree phase shift, and tie high to $INTV_{CC}$ (~3.4V) or an external supply >3V for a 90-degree phase shift.

V_{OSNS} (Pin F1): Output Voltage Sense. This pin is the inverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connects V_{OSNS} directly to the output capacitor and the load. Also, tie the GND connections of the output capacitor and the SET pin capacitor directly together.

PIN FUNCTIONS

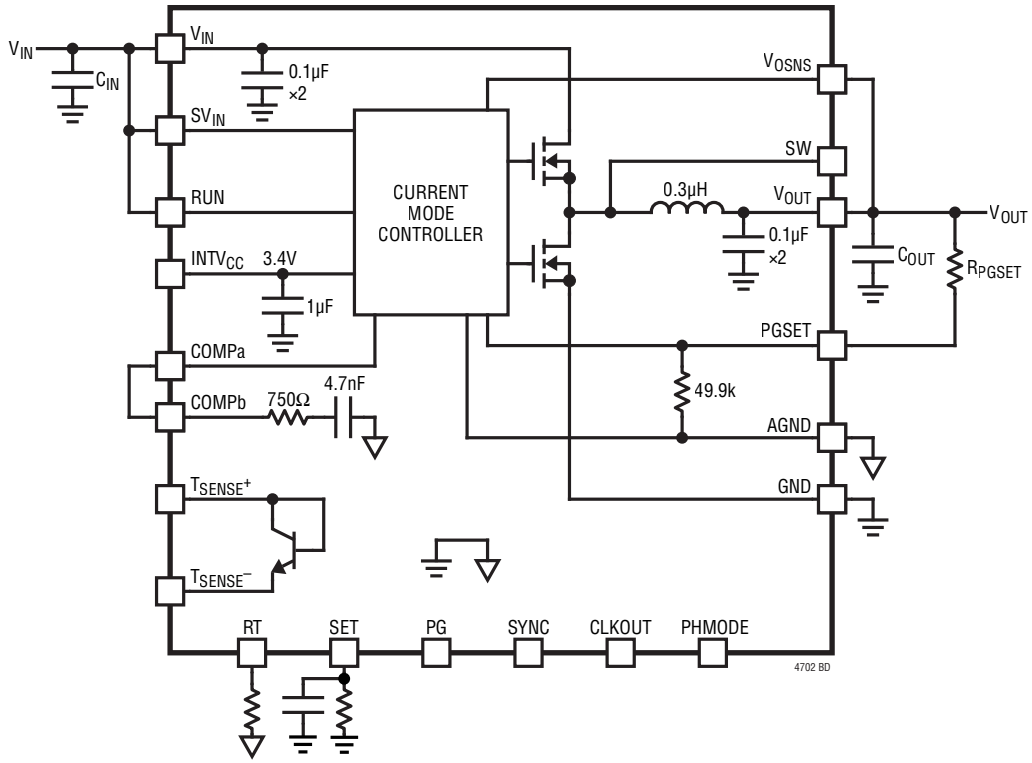
PG (Pin F2): Output Power Good Indicator. The PG pin is the open-drain output of an internal comparator. PG remains low until the V_{OSNS} pin is within ±7.5% of the final regulation voltage, and there are no fault conditions. PG is also pulled low when RUN is below 1V, $INTV_{CC}$ has fallen too low, SV_{IN} is too low, or during the thermal shutdown. PG is valid when SV_{IN} is above 3V.

SW (Pin F6): Switching node of the LTM4702. This pin is for test purposes only. Do not load the SW pin with external circuitry.

CLKOUT (Pin F7): Output Clock Signal for PolyPhase® Operation. The CLKOUT pin provides a 50% duty-cycle square wave of the switching frequency. The phase of CLKOUT with respect to the LTM4702 internal clock is determined by the state of the PHMODE pin. CLKOUT's peak-to-peak amplitude is $INTV_{CC}$ to GND. Float this pin if the CLKOUT function is not used.

SYNC (Pin G6): This pin programs three different operating modes: 1) Pulse-skipping mode. Tie this pin to GND for pulse-skipping mode for improved efficiency at light loads. 2) Forced continuous mode (FCM). This mode offers fast transient response and full frequency operation over a wide load range. Tie this pin high to $INTV_{CC}$ (~3.4V) or an external supply >3V for FCM. The part will operate in this mode by default if this pin is left floating. 3) Synchronization mode. Drive this pin with a clock source synchronize to an external clock and put the part in FCM.

BLOCK DIAGRAM



OPERATION

The LTM4702 is a standalone nonisolated switching DC/DC power supply that can deliver up to 8A. The continuous current is determined by the internal operating temperature. It provides a precisely regulated output voltage programmable via one external resistor from 0.3V to 5.7V. The input voltage range is 3V to 16V. Given that the LTM4702 is a step-down regulator, make sure that the input voltage is high enough to support the desired output voltage and load current. See the simplified Block Diagram.

The LTM4702 contains a current mode controller, power switching elements, power inductor, and a modest amount of input and output capacitance. The LTM4702 is a fixed-frequency PWM regulator. The switching frequency is set by simply connecting a resistor from the RT pin to AGND.

An internal regulator provides power to the control circuitry. To improve efficiency across all loads, the SV_{IN} pin can be powered from an independent supply at a voltage lower than V_{IN}. If the RUN pin is below 0.4V, the LTM4702 is shutdown and draws 50µA from the input. When the RUN pin rises above 1.32V (Typ), LTM4702 becomes active.

In applications where low output ripple and high efficiency at light load conditions are desired, pulse-skipping mode should be used by connecting the SYNC pin to GND. At light loads, the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode.

In applications where fixed frequency operation is more critical than low current efficiency and where the lowest output ripple is desired, forced continuous mode (FCM) operation should be used. FCM operation can be enabled by tying the SYNC pin to $INTV_{CC}$. In this mode, the inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, the FCM is disabled and the inductor current is prevented from reversing until the LTM4702's output voltage is in regulation.

The LTM4702 incorporates fast start-up circuitry that allows the part start-up at a short time while using a larger value SET pin capacitor for ultralow noise applications. See the Applications Information section for more details.

The LTM4702 contains a power good comparator, which trips when the PGSET pin is between 465mV and 540mV. The PG output is an open-drain transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. The PG signal is valid when SV_{IN} is above 3V. If SV_{IN} is above 3V and RUN is low, PG will remain low.

The LTM4702 is equipped with a thermal shutdown that inhibits power switching at high junction temperatures. The activation threshold of this function is above 125°C to avoid interfering with normal operation, so prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.

Two or more LTM4702s may be operated in parallel to produce higher currents. The COMPa and CLKOUT pins enable multiple LTM4702 to run out-of-phase, reducing the amount of required input and output capacitors. The PHMODE pin selects the phasing of CLKOUT for different multiphase applications. The COMPa pin allows the loop compensation of the LTM4702 to be optimized for a fast-transient response.

APPLICATIONS INFORMATION

For most applications, the design process is straightforward and summarized below.

1. See Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{SET}, and R_T values.
3. Apply the C_{SET} (from SET to GND).

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load, and environmental conditions. Remember that the maximum output current is limited by the junction temperature, the relationship between the input and output voltage magnitude and polarity, and other factors. See the graphs in the Typical Performance Characteristics section for more details.

The maximum frequency (and attendant R_T value) at which the LTM4702 should be allowed to switch is shown in Table 1 in the Maximum f_{SW} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the f_{SW} column. There are additional conditions that must be satisfied if the synchronization function is used. See the Synchronization section for details.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those shown in Table 1 is not recommended and may result in undesirable operation. Using larger values is generally acceptable and can yield improved dynamic response if necessary. Again, it is incumbent upon the user to verify the proper operation over the intended system's line, load, and environmental conditions.

Ceramic capacitors are small, robust, and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U, have a very large temperature and voltage coefficients of capacitance. In an application circuit, they may have only a small fraction of their nominal capacitance, resulting in a much higher output voltage ripple than expected.

Ceramic capacitors are also piezoelectric. Since the LTM4702 operates at a lower current limit during pulse-skipping mode operation, the noise is typically very quiet to a casual ear.

If this audible noise is unacceptable, use a high-performance electrolytic capacitor at the output. It may also be a parallel combination of a ceramic capacitor and a low-cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM4702. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM4702 circuit is plugged into a live supply, the input voltage can ring twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

Table 1. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN}* (V)	V_{OUT} (V)	R_{SET} (kΩ)	C_{IN}**	C_{OUT}	f_{SW} (kHz)	R_T (kΩ)	MAX f_{SW} (kHz)	MIN R_T (kΩ)
3 to 16	1	10	10µF X7R 25V 1210	100µF ×2 X7R 6.3V 1210	800	137	2500	35.7
3.3 to 16	1.5	15	10µF X7R 25V 1210	100µF ×2 X7R 6.3V 1210	1200	86.6	2500	35.7
3.9 to 16	2.5	24.9	10µF X7R 25V 1210	100µF ×2 X7R 6.3V 1210	1400	71.5	2500	35.7
4.5 to 16	3.3	33.2	10µF X7R 25V 1210	100µF ×2 X7R 6.3V 1210	1700	57.1	2500	35.7
7.5 to 16	5	49.9	10µF X7R 25V 1210	100µF ×2 X7R 10V 1210	1900	49.9	3000	28.7

*The LTM4702 may be capable of the operating at lower input voltage but may skip switching cycles.

**A bulk capacitor is required.

APPLICATIONS INFORMATION

Frequency Selection

The LTM4702 uses a constant-frequency PWM architecture that can be programmed to switch from 300kHz to 3MHz by using a resistor tied from the RT pin to the ground. Table 2 provides a list of R_T resistor values and their resultant frequencies.

Table 2. Switching Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.3	392
0.4	287
0.5	226
0.6	187
0.7	154
0.8	137
0.9	118
1.0	105
1.2	86.6
1.4	71.5
1.6	61.9
1.8	53.6
2	47
2.5	35.7
3	28.7

Operating Frequency Trade-Offs

It is recommended that the user applies the optimal R_T value shown in Table 2 for the input and output operating conditions. System level or other considerations, however, may necessitate another operating frequency. While the LTM4702 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat, or even damage the LTM4702 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

Maximum Load

The maximum practical continuous load that the LTM4702 can drive, while rated at 8A, actually depends upon both the internal current limit and the internal temperature. The internal current limit is designed to prevent damage to the LTM4702 in the case of overload or short-circuit. The internal temperature of the LTM4702 depends upon operating conditions such as the ambient temperature, the power delivered, and the system's heat-sinking capability. For example, if the LTM4702 is configured to regulate at 1V, it may continuously deliver 8A from $12V_{IN}$ if the ambient temperature is controlled to less than 73°C with no airflow. See the $12V_{IN}$ and $1V_{OUT}$ derating curves in the Typical Performance Characteristics section. Similarly, if the output voltage is 5V and the ambient temperature is 85°C, the LTM4702 will deliver at most 5.5A from $12V_{IN}$, which is less than the 8A continuous rating.

Load Sharing

Two or more LTM4702 may be paralleled to produce a higher currents. To do this, tie the V_{IN}, V_{OUT}, V_{OSNS}, COMPa, and COMPb pins of all the paralleled LTM4702s together. Examples of multiple LTM4702s configured for load sharing are shown in the Typical Application section (Figure 11 and Figure 12).

The CLKOUT signal can be connected to the SYNC pin of the following LTM4702 to line up both the frequency and the phase of the entire system. Tying the PHMODE pin to GND, $INTV_{CC}$, or floating the pin generates a phase difference between the LTM4702's internal clock and CLKOUT of 180°, 90°, or 120°, respectively, which corresponds to a 2-phase, 4-phase, or 3-phase operation. A total of 12 phases can be paralleled to run simultaneously out-of-phase with respect to each other by programming the PHMODE pin of each LTM4702 to different voltage levels. Figure 1 shows a 4-phase application where four LTM4702 are paralleled to get one output capable of up to 32A. During FCM and synchronization modes, all devices will operate at the same frequency. When load sharing

APPLICATIONS INFORMATION

among n units and using a single R_{SET} resistor, the value of the resistor is given by Equation 2.

$$R_{SET} = \frac{V_{OUT}}{n \bullet 100\mu A} \quad (2)$$

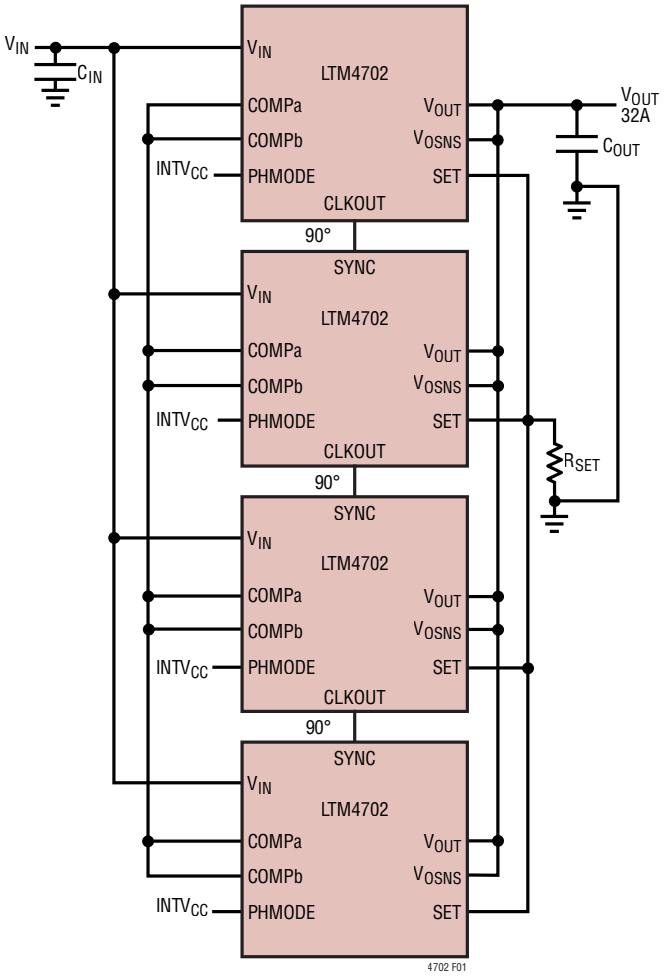


Figure 1. Paralleling Four LTM4702 Devices

Minimum Input Voltage

The LTM4702 is a step-down regulator, so a minimum amount of headroom is required to keep the output in regulation. Keep V_{IN} above 3V to ensure proper operation. If the SV_{IN} and V_{IN} are powered from different sources, keep the SV_{IN} above 4V to maintain $INTV_{CC}$ = 3.4V and ensure optimum regulation. Voltage transients or ripple valleys that cause the SV_{IN} to fall below 3V may turn off the LTM4702.

SET Pin (Bypass) Capacitance: Noise, Transient Response, and Soft-Start

In addition to reducing output noise, using a SET pin bypass capacitor reduces sensitivity to any parasitic coupling of voltage spikes onto the SET pin. Note that any bypass capacitor leakage deteriorates the LTM4702 DC regulation. Capacitor leakage of even 100nA is a 0.1% DC error. Therefore, it is recommended to use a good quality low leakage ceramic capacitor.

Using a SET pin bypass capacitor also soft-starts the output and limits inrush current. Soft-starting the output prevents a current surge on the input supply. The SET pin capacitor and resistor values set the ramp-up time of the reference voltage, and the output voltage will track this voltage. The SET pin resistance is determined by the application's desired output voltage; however, the capacitance may be selected to achieve the desired ramp up time.

Without fast start-up enabled, the RC time constant, formed by the SET pin resistor and capacitor, controls soft-start time. Tie the PGSET pin to 0.5V to disable fast start-up. Ramp-up rate from 0% to 90% of nominal V_{OUT} shown in Equation 3.

$$t_{START\_NO\_FAST\_START-UP} = 2.3 \bullet R_{SET} \bullet C_{SET} \quad (3)$$

With fast-start-up enabled, the start-up time can be significantly reduced with the ramp-up time from 0% to 90% of the nominal V_{OUT} given by Equation 4.

$$t_{START\_FAST\_START-UP} = \frac{100\mu A \bullet R_{SET} \bullet C_{SET}}{2.7mA} \quad (4)$$

In most applications, fast start-up will be enabled, in which case a minimum 1µF SET capacitor is recommended for preventing reference voltage overcharge as well as ensuring good noise performance.

Soft-Start and Power Sequencing

As discussed in SET Pin (Bypass) Capacitance: Noise, Transient Response, and Soft-Start section, soft-start is achieved through the controlled ramp up time of the SET pin voltage. Soft-start is guaranteed when V_{IN} and SV_{IN} are tied together.

APPLICATIONS INFORMATION

When V_{IN} and SV_{IN} are powered by independent supplies, power sequencing must be considered to guarantee soft-start. The SET pin voltage should start at 0V when V_{IN} is applied. To guarantee soft-start, do not power V_{IN} last when sequencing V_{IN}, SV_{IN}, and RUN. An example of a specific case to avoid is having SV_{IN} and RUN powered up before V_{IN}; in this instance, the SET pin voltage will have risen to some voltage greater than 0V when V_{IN} is applied, and the LTM4702 will not soft-start properly.

Fast Start-Up

For ultralow noise applications that require low 1/f noise (i.e., at frequencies below 100Hz), a larger value SET pin capacitor is required, up to 22µF. A larger value capacitor can be used, but care should be taken regarding leakage. While normally larger capacitors would significantly increase the regulator's start-up time, the LTM4702 incorporates fast start-up circuitry that increases the SET pin current to about 2.7mA during start-up.

Upon start-up, a 2.7mA current source remains engaged while PGSET is below the power good threshold of 465mV, unless the regulator is in thermal shutdown, SV_{IN} is too low, or $INTV_{CC}$ has fallen too low.

The fast start-up circuit is disabled permanently once PGSET rises above the power good threshold, until either the part is powered down or the part is placed into SHDN by pulling the RUN pin to GND.

There is one more condition under which the 2.7mA current source is disabled during start-up. The purpose of this is to prevent overcharging V_{SET}. Since the part assumes that the PGSET pin is an accurate indication of the voltage on the SET pin, it assumes that V_{OSNS} follows V_{SET} closely. However, this may not always be the case—for example, if the output capacitance is very large or if, for some reason, the output is shorted to GND. Therefore, fast charge is also disabled whenever the COMPa pin has railed at its maximum value (when V_{SET} has risen significantly about V_{OSNS}). This prevents incorrect behavior where the 2.7mA current sources stay on even if the V_{SET} has risen above its intended value.

This means that there is also a minimum SET capacitor requirement for using a fast start-up without overcharging the reference voltage. This will depend on the compensation network, as the part depends on the COMPa pin voltage rising to its maximum value to inform the part to pause fast charge.

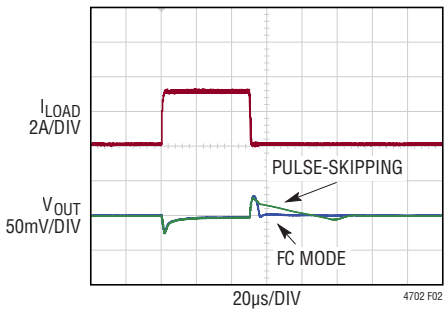
The recommended minimum SET capacitance value to prevent overcharging the reference voltage is shown in Equation 5.

$$\text{Minimum } C_{SET} = 27 \bullet \frac{C_{COMP}}{V_{SET}} \quad (5)$$

If programmable power good and fast start-up capabilities are not required, the PGSET pin must be tied to 0.5V. This 0.5V could be an external voltage reference for PGSET. Figure 9 circuit shows an example.

Forced Continuous Mode

The LTM4702 can operate in forced continuous mode (FCM) for fast transient response and full frequency operation over a wide load range. When in FCM, the oscillator operates continuously, and positive SW transitions are aligned to the clock. Negative inductor current is allowed at light loads or under large transient conditions. FCM improves load step transient response (see Figure 2). At light loads, FCM operation is less efficient than pulse-skipping operation but may be desirable in applications where it is necessary to keep switching harmonics out of the signal band. FCM must be used if the output is required to sink current. To enable FCM, tie the SYNC pin to $INTV_{CC}$ or > 3V, or float the pin.



V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 2MHz
C_C = 2.2nF, R_C = 1k
C_{OUT} = 100µF ×2 + 22µF ×2

Figure 2. 0.1A to 3.1A Load Step Transient Response with and without Forced Continuous Mode

APPLICATIONS INFORMATION

FCM is disabled under V_{IN} overvoltage conditions (the V_{IN} pin is held above 18V) if V_{OUT} is too high (the PGSET pin is held greater than 540mV) and is also disabled during start-up until the voltage on V_{OUT} has charged up to 92.5% of its final value (as indicated when the PGSET pin rises to above 465mV). For the latter two conditions, it is assumed the PGSET pin is tied to the output voltage through an appropriate resistor. When FCM is disabled in these ways, negative inductor current is not allowed and the LTM4702 operates in pulse-skipping mode.

Pulse-Skipping Mode

When not operating in forced continuous mode, the LTM4702 will operate in pulse-skipping mode. The negative inductor current is not allowed in this mode. Additionally, in pulse-skipping mode, the LTM4702 may also skip switching cycles at very light loads for improved efficiency or at very high duty cycles in order to achieve better dropout. To enable pulse-skipping mode, tie the SYNC pin to GND.

Synchronization

To synchronize the LTM4702 oscillator to an external frequency, connect a square wave to the SYNC pin. The square wave amplitude should have valleys below 0.4V and peaks above 1.5V (up to 6V), with a minimum on-time and off-time of 50ns.

The LTM4702 will run in forced continuous mode to maintain regulations while synchronized to an external clock. The LTM4702 may be synchronized over a 300kHz to 3MHz range. The R_T resistor should be chosen to set the LTM4702 switching frequency to below the lowest synchronization input by approximately 20%. For example, if the synchronization signal is 500kHz and higher, the R_T should be selected for 400kHz.

Programmable Power Good

The LTM4702 features a programmable power good by using a single resistor across OUT pin and PGSET pin (Equation 6).

$$V_{OUT(PG\_THRESHOLD)} = 0.5V \bullet \left(1+\frac{R_{PGSET}}{49.9k}\right)+I_{PGSET} \bullet R_{PGSET} \quad (6)$$

If the PGSET pin increases above 540mV or decreases below 465mV, the open-drain PG pin de-asserts and becomes low impedance. The power good comparator has 5mV hysteresis. The PGSET pin current (I_{PGSET}) from the Electrical Characteristics table must be considered when determining the resistor. Note that the programmable power good and fast start-up capabilities are disabled when PGSET is tied to 0.5V or when the device is in shutdown. Table 3 suggests some 1% R_{PGSET} resistor values for common V_{OUT} configurations.

Table 3. Suggested R_{PGSET} Resistor Values

V_{OUT} (V)	R_{PGSET} (kΩ)
0.8	30.1
0.9	40.2
1	49.9
1.2	69.8
1.5	100
1.8	130
2.5	200
3.3	280
5	453

Shorted or Reversed Input Protection

Care needs to be taken in systems where the output is held high when the power input to the LTM4702 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR-ed with the LTM4702's output. If the V_{IN} pin is allowed to float and the RUN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LTM4702's internal circuitry pulls its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN pin, the internal current drops to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, parasitic diodes inside the LTM4702 can pull large currents from the output through the V_{IN} pin. Figure 3 shows a connection of V_{IN} and RUN pins that will allow LTM4702 to run only when the input voltage is present and that protects against a shorted or reversed input.

APPLICATIONS INFORMATION

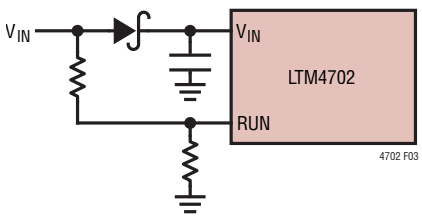


Figure 3. Reverse Input Protection

Temperature Monitoring

Measuring the absolute temperature of a diode is possible due to the relationship between current, voltage, and temperature described by the classic diode Equation 7.

$$I_D = I_S \bullet e\left(\frac{V_D}{\eta \bullet V_T}\right)$$

or (7)

$$V_D = \eta \bullet V_T \bullet \ln\frac{I_D}{I_S}$$

where I_D is the diode current, V_D is the diode voltage, η is the ideal factor (typically close to 1.0) and I_S (saturation current) is a process dependent parameter. V_T can be broken out by Equation 8.

$$V_T = \frac{k \bullet T}{q} \quad (8)$$

where T is the diode junction temperature in Kelvin, q is the electron charge, and k is Boltzmann's constant. V_T is approximately 26mV at room temperature (298K) and scales linearly with Kelvin temperature. It is this linear temperature relationship that makes diodes suitable temperature sensors. The I_S term in Equation 8 is the extrapolated current through a diode junction when the diode has zero volts across the terminals. The I_S term varies from process to process, varies with temperature, and by definition must always be less than I_D. Combining all of the constants into one term (Equation 9).

$$K_D = \frac{\eta \bullet k}{q} \quad (9)$$

where $K_D = 8.26^{-5}$, and knowing ln (I_D/I_S) is always positive because I_D is always greater than I_S, as shown in Equation 10.

$$V_D = T_{(KELVIN)} \bullet K_D \bullet \ln\frac{I_D}{I_S} \quad (10)$$

where V_D appears to increase with temperature. It is common knowledge that a silicon diode biased with a current source has an approximate –2mV/°C temperature relationship (Figure 4), which is at odds with the equation. In fact, the I_S term increases with temperature, reducing the absolute value yielding an approximate –2mV/°C composite diode voltage slope.

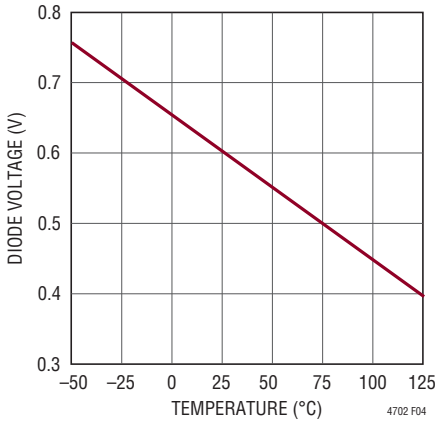


Figure 4. Diode Voltage V_D vs Temperature

To obtain a linear voltage proportional to temperature we cancel the I_S variable in the natural logarithm term to remove the I_S dependency from Equation 9. This is accomplished by measuring the diode voltage at two currents, I_1 and I_2, where $I_1 = 10 \bullet I_2$ and subtracting to get Equation 11.

$$\Delta V_D = T_{(KELVIN)} \bullet K_D \bullet \ln\frac{I_1}{I_S} - T_{(KELVIN)} \bullet K_D \bullet \ln\frac{I_2}{I_S} \quad (11)$$

Combining like terms, then simplifying the natural log terms yields Equation 12.

$$\Delta V_D = T_{(KELVIN)} \bullet K_D \bullet \ln(10) \quad (12)$$

and redefining constant shown in Equation 13.

$$K'_D = K_D \bullet \ln(10) = \frac{198\mu V}{K} \quad (13)$$

APPLICATIONS INFORMATION

yields Equation 14.

$$\Delta V_D = K'_D \bullet T_{(KELVIN)} \quad (14)$$

Use Equation 15 for solving for temperature.

$$T_{(KELVIN)} = \frac{\Delta V_D}{K'_D} (^\circ CELSIUS) = T_{(KELVIN)} - 273.15 \quad (15)$$

Where,

300°K = 27°C

means that is we take the difference in voltage across the diode measured at two currents with a ratio of 10, the resulting voltage is 198µV per Kelvin of the junction with a zero intercept at 0 Kelvin.

The diode connected NPN transistor across the T_{SENSE}^+ pin and T_{SENSE}^- pin can be used to monitor the internal temperature of the LTM4702.

Hot-Plugging Safely

The small size, robustness, and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM4702. However, these capacitors can cause problems if the LTM4702 is plugged into a live supply (Refer to Analog Devices Application Note 88 for a complete discussion). The low-loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pins of the LTM4702 can ring to more than twice the nominal input voltage, possibly exceeding the LTM4702's rating and damaging the part. If the input supply is poorly controlled or the LTM4702 is hot-plugged into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is adding an electrolytic bulk cap to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low-frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

Figure 5. Thermal Image at $12V_{IN}$, 1V, 8A Output without Airflow and Heat Sink

Thermal Considerations

The LTM4702 output current may need to be derated if it is required to operate at a high ambient temperature. The amount of current derating depends upon the input voltage, output power, and ambient temperature. The derating curves shown in the Typical Performance Characteristics section can be used as a guide. These curves were generated by the LTM4702 mounted to a $50cm^2$ 6-layer FR4 printed circuit board. Boards of other sizes and layer counts can exhibit different thermal behaviors, so it is incumbent upon the user to verify proper operation over the intended system's line, load, and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use FEA (finite element analysis) to predict thermal performance. To that end, below are the four thermal coefficients.

1. θ_{JA} – Thermal resistance from junction to ambient.
2. θ_{JCbot} – Thermal resistance from junction to the bottom of the product case.
3. θ_{JCtop} – Thermal resistance from junction to top of the product case.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD51-12 and are quoted or paraphrased below.

APPLICATIONS INFORMATION

1. θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as “still air” although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. θ_{JCbot} is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModudle regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don’t generally match the user’s application.
3. θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of θ_{JCbot}, this value may be useful for comparing packages, but the test conditions don’t generally match the user’s application.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none can be individually used to predict the product's thermal performance accurately. Likewise, it would be inappropriate to attempt to use anyone coefficient to correlate to the junction temperature vs load graphs given in the product’s data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all thermal resistances simultaneously.

A graphical representation of these thermal resistances is shown in Figure 6. Some thermal resistance elements, such as heat flow out the side of the package, are not defined by the JEDEC standard and are not shown. The blue resistances are contained within the µModule regulator, and the green is outside.

The die temperature of the LTM4702 must be lower than the maximum rating, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM4702. The bulk of the heat flow out of the LTM4702 is through the bottom of the package and the pads into the printed circuit board. Consequently, a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. See the PCB Layout section for printed circuit board design suggestions.

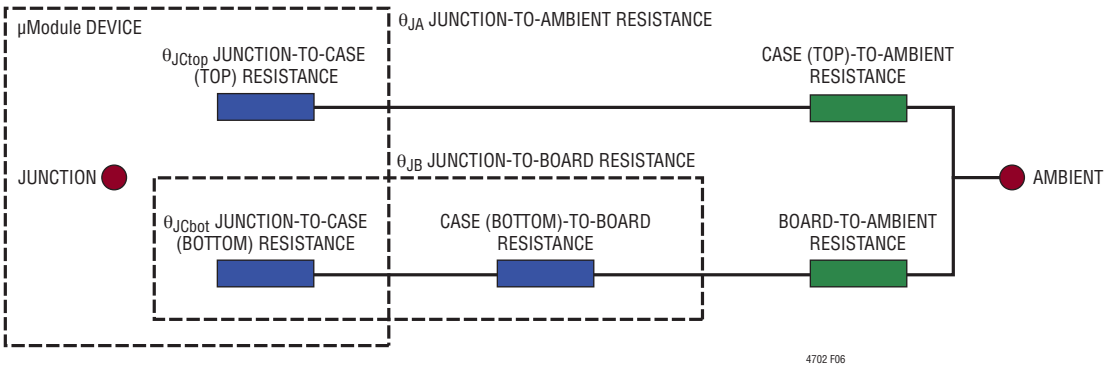


Figure 6. Graphical Representation of Thermal Coefficients, Including JESD51-12 Terms

APPLICATIONS INFORMATION

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM4702. The LTM4702 is, nevertheless, a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with a high level of integration, you may fail to achieve the specified operation with a haphazard or poor layout. See Figure 7 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place C_{SET}, R_{SET}, and R_T as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN}/SV_{IN} and GND connection of the LTM4702.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM4702.
4. Place the C_{IN} and C_{OUT} capacitors so that their ground current flow directly adjacent to or underneath the LTM4702.
5. Connect all the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM4702.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias, as shown in Figure 7. The LTM4702 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

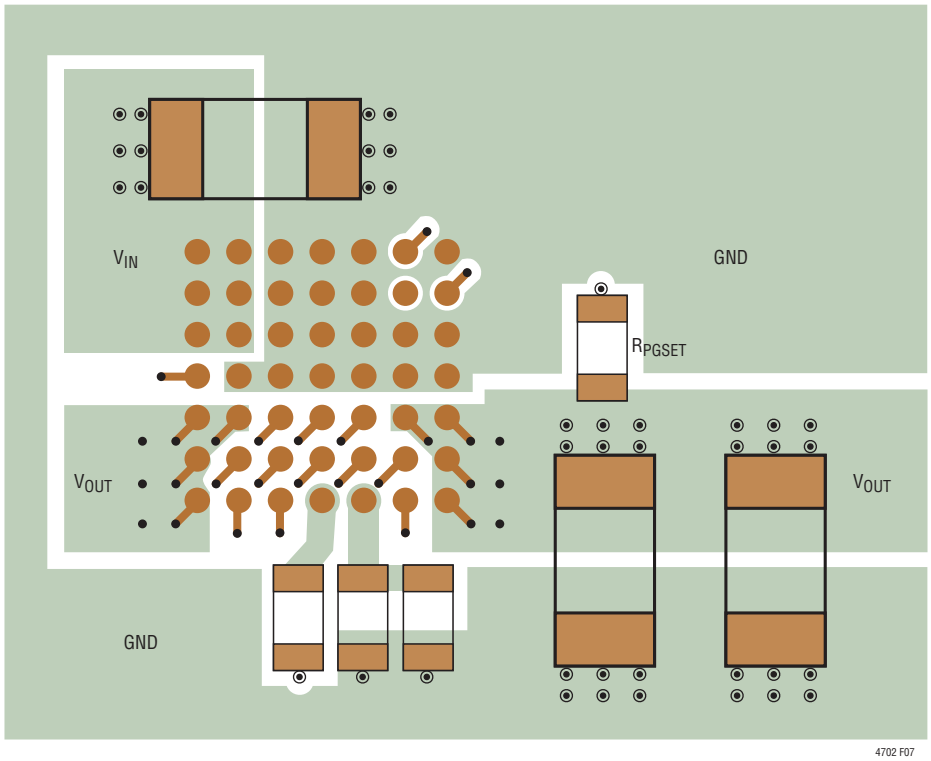
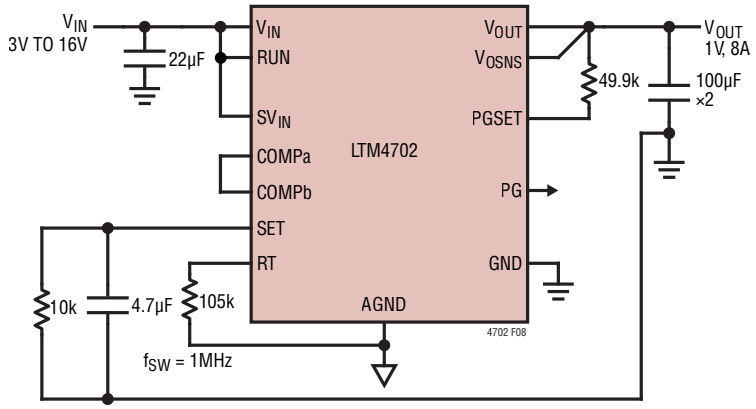


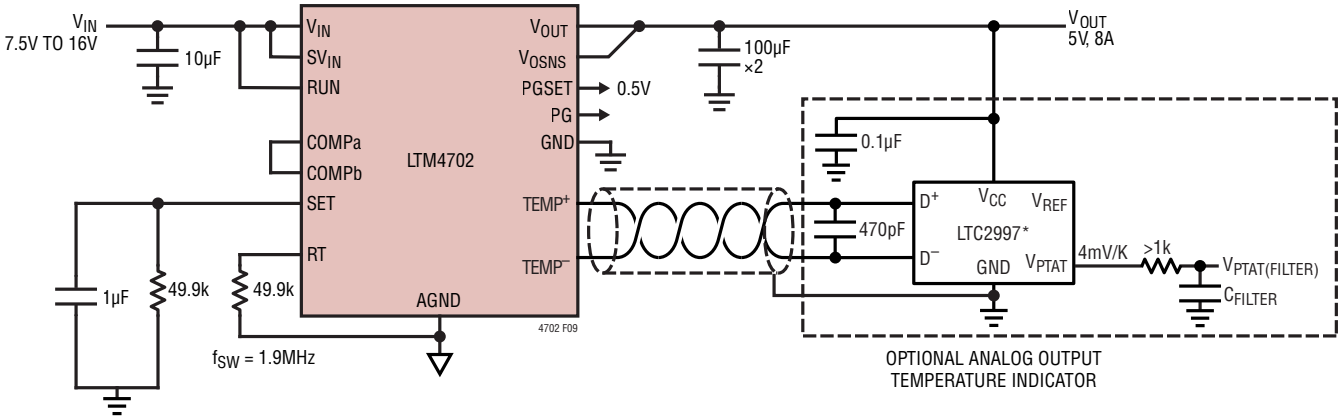
Figure 7. Layout Showing Suggested External Components, GND Plane and Thermal Vias (Top Layer)

TYPICAL APPLICATIONS



PINS NOT USED: SW, SYNC, PHMODE, CLKOUT, $INTV_{CC}$, T_{SENSE}^{+}, T_{SENSE}^{-}.
TO GUARANTEE SOFT-START, DO NOT POWER V_{IN} LAST WHEN SEQUENCING V_{IN}, SV_{IN} AND RUN.

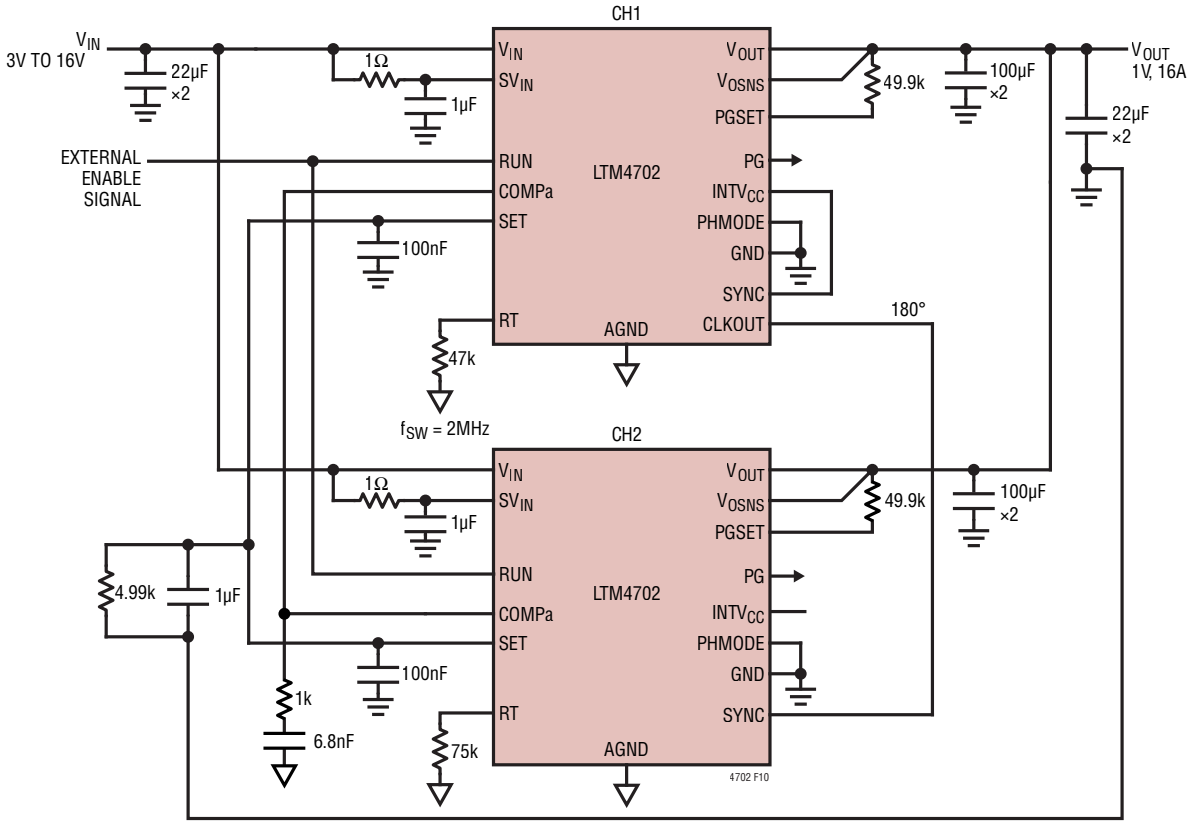
Figure 8. 1V, 8A from 3V to 16V_{IN}, 1MHz with Soft-Start, Fast Start-Up and Power Good



PINS NOT USED: SW, SYNC, PHMODE, CLKOUT, $INTV_{CC}$.

Figure 9. 5V, 8A from 7.5V to 16V_{IN}, 1.9MHz with Soft-Start, Temperature Indicator and Power Good

TYPICAL APPLICATION



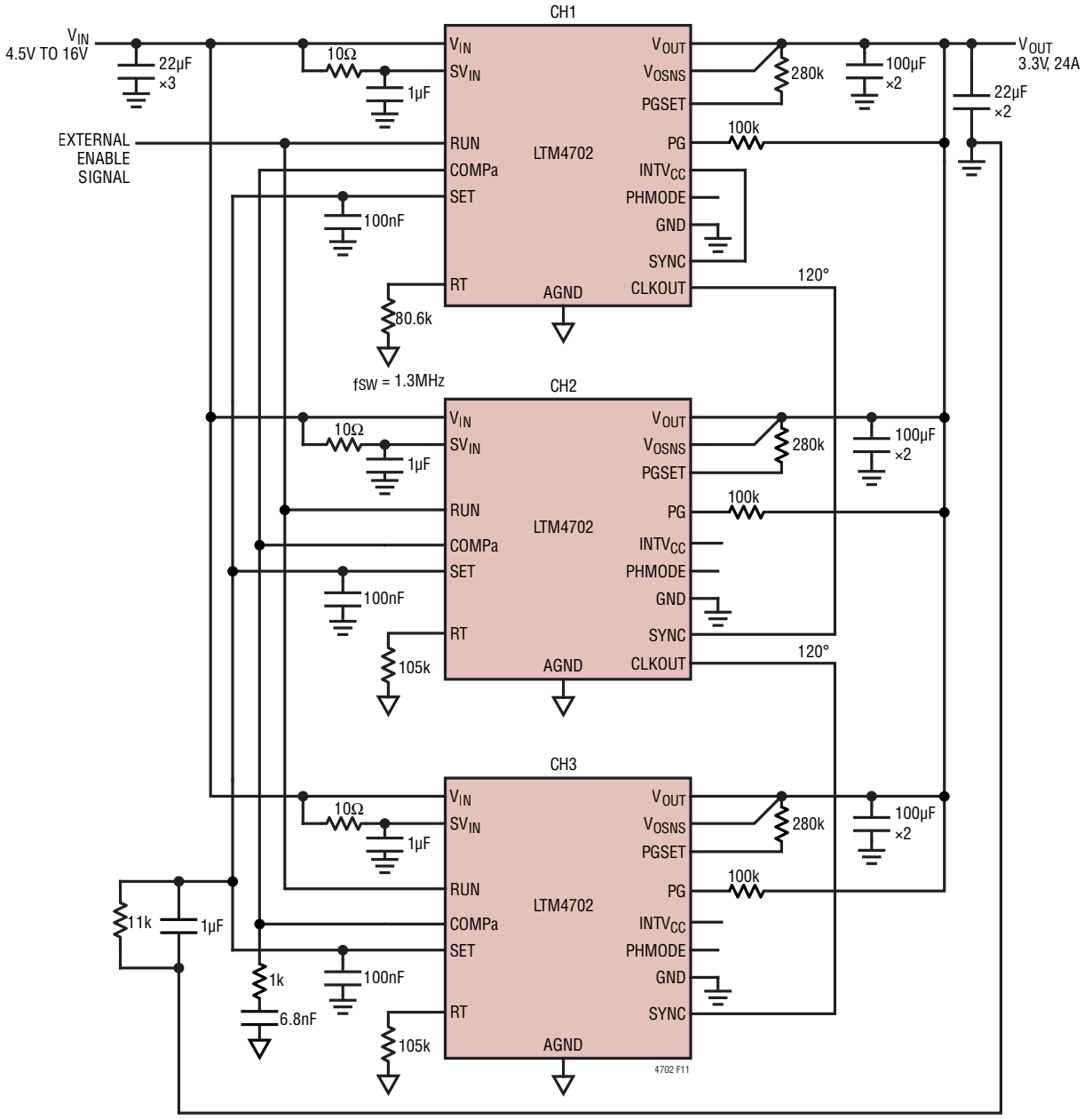
PINS NOT USED: COMPb, SW, T_{SENSE}^+, T_{SENSE}^-.

NOTES:

1. CH2 IS SYNCHRONIZED TO 2MHz VIA SYNC PIN. R_T RESISTOR VALUE MUST SET INTERNAL OSCILLATOR TO <1.6MHz (80% OF 2MHz).
2. COMPa PINS TIED TOGETHER.
3. PHMODE TIED TO GND FOR 180 DEG. PHASE SHIFT AT CLKOUT.
4. SET PINS CAN BE TIED TOGETHER FOR 200µA CURRENT REFERENCE; THIS PROVIDES LOWER 1/f NOISE AND BETTER CURRENT SHARING.

Figure 10. 2-Phase 1V, 16A from 3V to 16V_{IN}, 2MHz with Soft-Start, Fast Start-Up and Power Good

TYPICAL APPLICATION



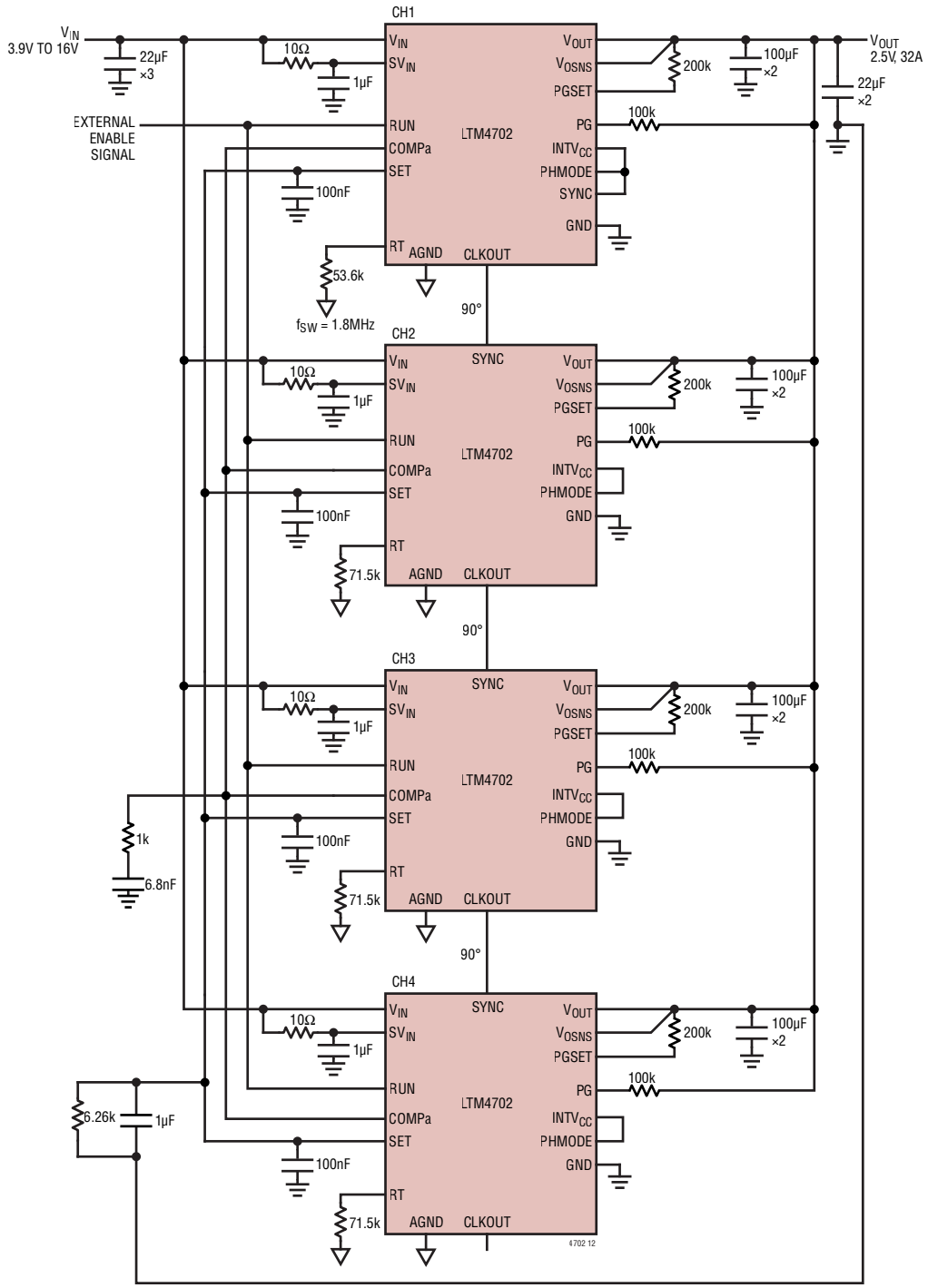
PINS NOT USED: COMPb, SW, T_{SENSE}^{+}, T_{SENSE}^{-}.

NOTES:

1. CH2 AND CH3 ARE SYNCHRONIZED TO 1.3MHz VIA SYNC PIN. R_T RESISTOR VALUE MUST SET INTERNAL OSCILLATOR TO <1MHz (80% OF 1.3MHz).
2. COMPa PINS TIED TOGETHER.
3. PHMODE PIN FLOATS FOR 120 DEG. PHASE SHIFT AT CLKOUT.
4. SET PINS CAN BE TIED TOGETHER FOR 300µA CURRENT REFERENCE; THIS PROVIDES LOWER 1/f NOISE AND BETTER CURRENT SHARING.

Figure 11. 3-Phase 3.3V, 24A from 4.5V to 16V_{IN}, 1.3MHz with Soft-Start, Fast Start-Up and Power Good

TYPICAL APPLICATION



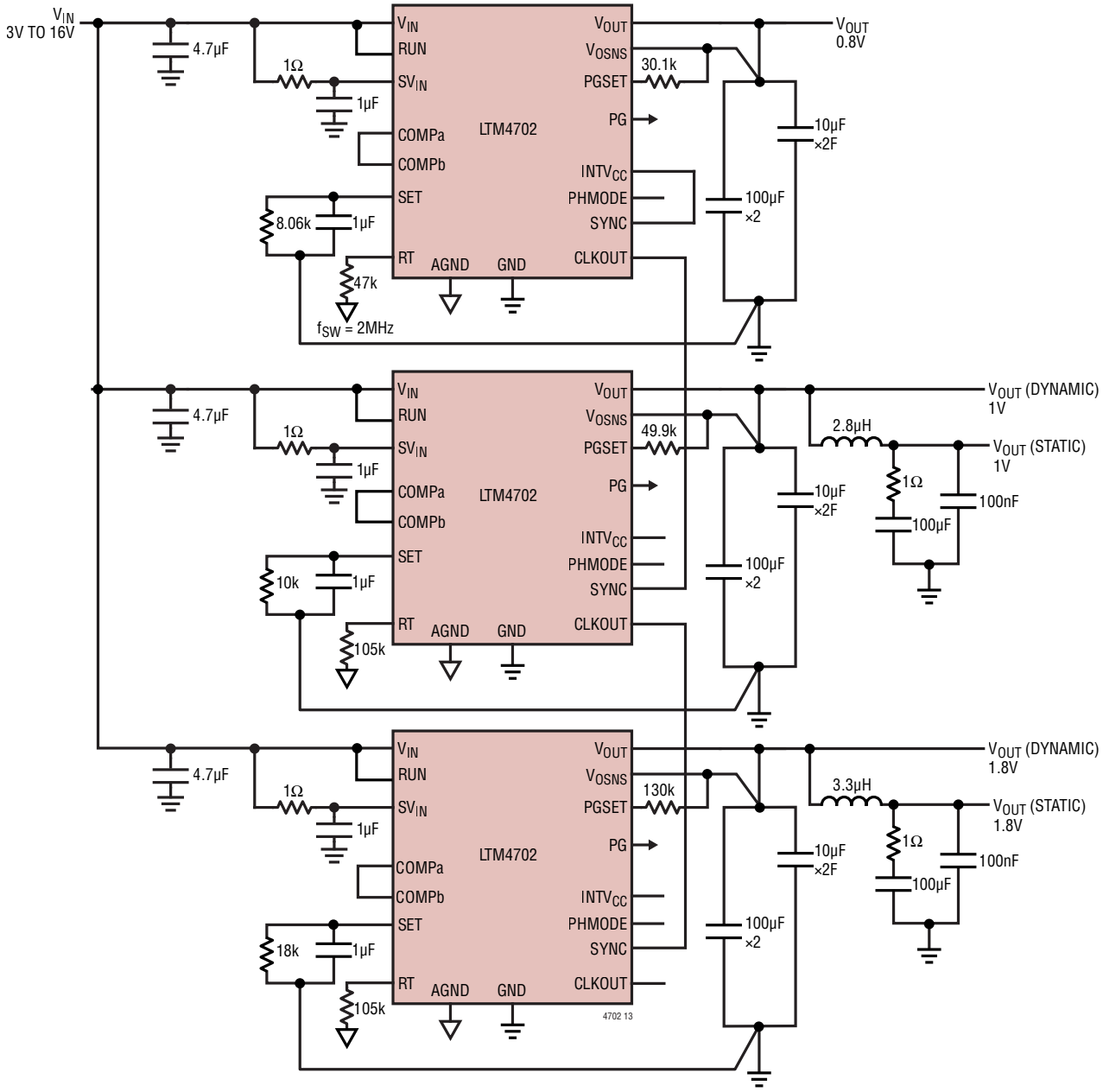
PINS NOT USED: COMPb, SW, T_{SENSE}^+, T_{SENSE}^-.

NOTES:

1. CH2 AND CH3 ARE SYNCHRONIZED TO 1.8MHz VIA SYNC PIN. R_T RESISTOR VALUE MUST SET INTERNAL OSCILLATOR TO <1.4MHz (80% OF 1.8MHz).
2. COMPa PINS TIED TOGETHER.
3. PHMODE TIED TO $INTV_{CC}$ FOR 90 DEG. PHASE SHIFT AT CLKOUT.
4. SET PINS CAN BE TIED TOGETHER FOR 400µA CURRENT REFERENCE; THIS PROVIDES LOWER 1/f NOISE AND BETTER CURRENT SHARING.

Figure 12. 4-Phase 2.5V, 32A from 3.9V to 16V_{IN}, 1.8MHz with Soft-Start, Fast Start-Up and Power Good

TYPICAL APPLICATION



PINS NOT USED: SW, T_{SENSE}^+, T_{SENSE}^-.
NOTE: LC FILTER IS ADDED FOR 1V AND 1.8V STATIC OUTPUTS TO ACHIEVE A VERY LOW OUTPUT NOISE BELOW 55µV_{RMS}.

Figure 13. Powering a Transceiver Using 3× LTM4702

PACKAGE DESCRIPTION

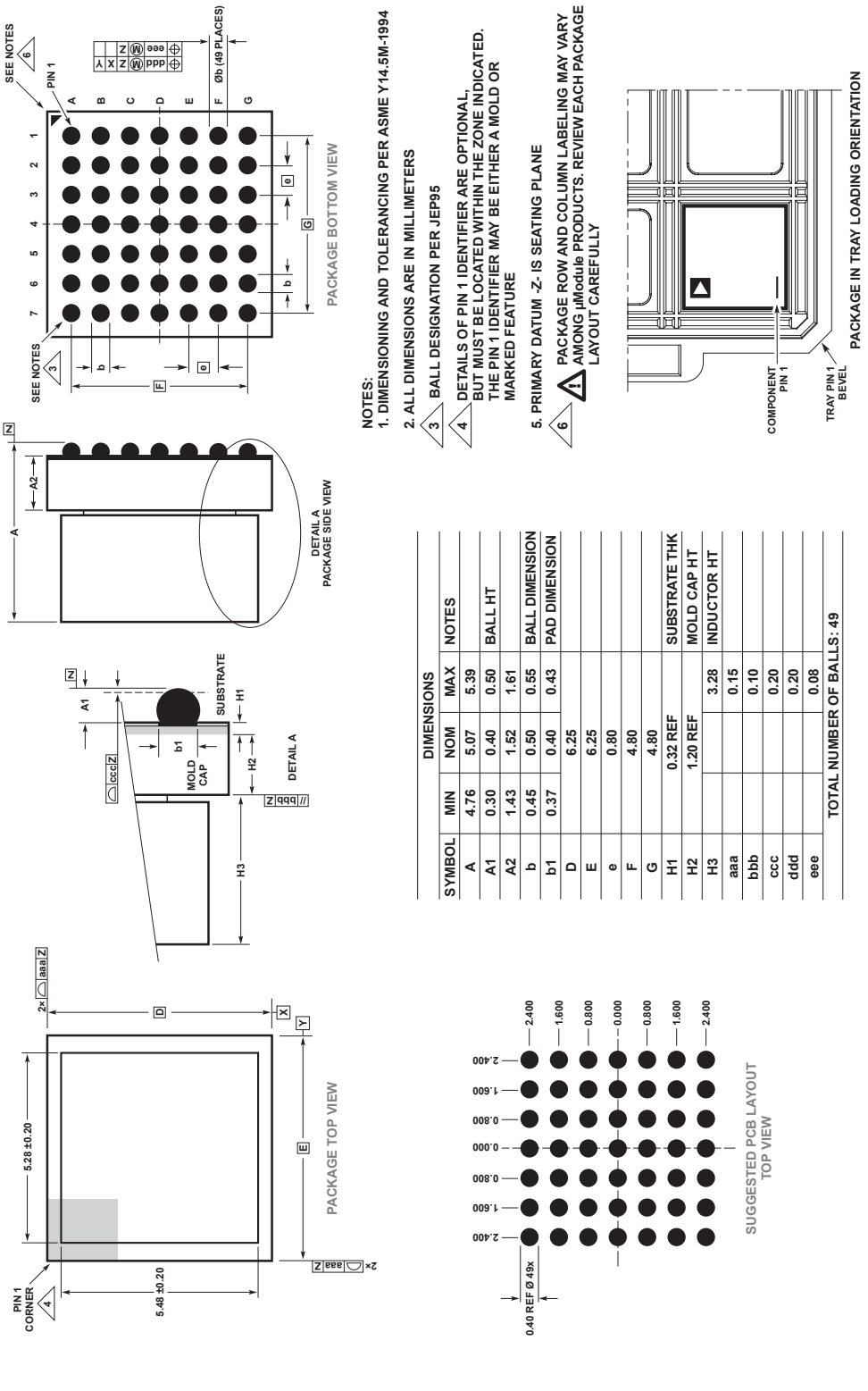
PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Table 4. LTM4702 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT}	A2	V_{OUT}	A3	V_{OUT}	A4	SV_{IN}	A5	V_{IN}	A6	V_{IN}	A7	V_{IN}
B1	T_{SENSE}^+	B2	T_{SENSE}^-	B3	V_{OUT}	B4	GND	B5	V_{IN}	B6	V_{IN}	B7	V_{IN}
C1	RUN	C2	COMPa	C3	COMPb	C4	GND	C5	GND	C6	GND	C7	GND
D1	RT	D2	AGND	D3	$INTV_{CC}$	D4	GND	D5	GND	D6	GND	D7	GND
E1	SET	E2	PGSET	E3	PHMODE	E4	GND	E5	GND	E6	GND	E7	GND
F1	V_{OSNS}	F2	PG	F3	V_{OUT}	F4	GND	F5	GND	F6	SW	F7	CLKOUT
G1	V_{OUT}	G2	V_{OUT}	G3	V_{OUT}	G4	GND	G5	GND	G6	SYNC	G7	GND

PACKAGE DESCRIPTION

49-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
6.25mm × 6.25mm × 5.07mm
(Reference DWG # BC-49-9)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

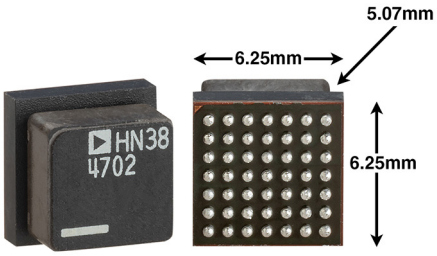
DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.76	5.07	5.39	
A1	0.30	0.40	0.50	BALL HT
A2	1.43	1.52	1.61	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		6.25		
E		6.25		
e		0.80		
F		4.80		
G		4.80		
H1		0.32 REF		SUBSTRATE THK
H2		1.20 REF		MOLD CAP HT
H3			3.28	INDUCTOR HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.20	
eee			0.08	
TOTAL NUMBER OF BALLS: 49				

REVISION HISTORY

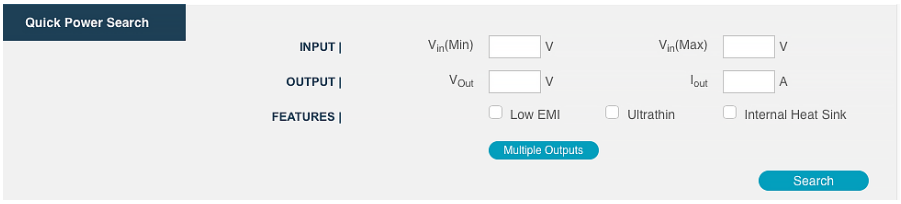
REV	DATE	DESCRIPTION	PAGE NUMBER
0	04/23	Initial Release.	—
A	06/23	Updated I_{PGSET} units. Updated Figure 11.	3 22
B	2/24	Added Note 10, V_{IN} = SV_{IN} = 6V conditions on Electrical Characteristics table.	3, 4
C	6/24	Updated Description section Updated Order Information table	1 2
D	9/24	Updated Title Updated Features section Updated Description section Updated Table 1	1 1 1 11

PACKAGE PHOTOS

Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8053	40V, 3.5A Low EMI Silent Switcher µModule Regulator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 15V, 6.25mm × 9mm × 3.32mm BGA
LTM8065	40V, 2.5A Low EMI Silent Switcher µModule Regulator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 18V, 6.25mm × 6.25mm × 2.32mm BGA
LTM8063	40V, 2A Low EMI Silent Switcher µModule Regulator	3.2V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 15V, 4mm × 6.25mm × 2.22mm BGA
LTM8074	40V, 1.2A Low EMI Silent Switcher µModule Regulator	3.2V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 12V, 4mm × 4mm × 1.82mm BGA
LTM8024	40V, Dual 3.5A Low EMI Silent Switcher µModule Regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 9mm × 11.25mm × 3.32mm BGA
LTM8078	40V, Dual 1.4A Low EMI Silent Switcher µModule Regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 10V, 6.25mm × 6.25mm × 2.32mm BGA
LTM8060	40V, Quad 3A Low EMI Silent Switcher µModule Regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 11.9mm × 16mm × 3.32mm BGA
LTM8051	40V, Quad 1.2A Low EMI Silent Switcher µModule Regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 6.25mm × 11.25mm × 2.32mm BGA
LTM8080	40VIN, Dual 500mA or Single 1A Ultralow Noise, Ultrahigh PSRR µModule Regulator	3.5V ≤ V_{IN} ≤ 40V, 0V ≤ V_{OUT} ≤ 8V, 6.25mm × 9mm × 3.32mm BGA
LTM4657	8A µModule Regulator, Pin Compatible with LTM4638	3.1V ≤ V_{IN} ≤ 20V. 0.5V ≤ V_{OUT} ≤ 5.5V. 6.25mm × 6.25mm × 3.87mm BGA
LTM4626	12A µModule Regulator, Pin Compatible with LTM4638	3.1V ≤ V_{IN} ≤ 20V. 0.6V ≤ V_{OUT} ≤ 5.5V. 6.25mm × 6.25mm × 3.87mm BGA
LTM4638	15A µModule Regulator, Pin Compatible with LTM4657/LTM4626	3.1V ≤ V_{IN} ≤ 20V. 0.6V ≤ V_{OUT} ≤ 5.5V. 6.25mm × 6.25mm × 5.02mm BGA

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