THE DATASHEET OF

GJM1555C1H2R1WB01D

MOSFET – Power, Dual, N-Channel, for 1-Cell Lithium-ion Battery Protection

12 V, 2.75 mΩ, 33 A

EFC2K102ANUZ

ON Semiconductor®

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V_{SSS}	$R_{SS(on)}$ Max	I_S Max
12 V	2.75 mΩ @ 4.5 V	33 A
	2.85 mΩ @ 3.8 V	
	3.95 mΩ @ 3.1 V	
	6.1 mΩ @ 2.5 V	

Overview

This Power MOSFET features a low on−state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1−cell lithium−ion battery applications.

Features

- 2.5 V Drive
- Common−Drain type
- ESD Diode−Protected Gate
- Pb−Free, Halogen Free and RoHS Compliance

Applications

- 1−Cell Lithium−ion Battery Charging and Discharging Switch

Specifications

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Value	Unit
Source to Source Voltage	V_{SSS}	12	V
Gate to Source Voltage	V_{GSS}	±8	V
Source Current (DC)	I_S	33	A
Source Current (Pulse) PW ≤ 10 μs, duty cycle ≤ 1%	I_{SP}	135	A
Total Dissipation (Note 1)	P_T	3.1	W
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	−55 to +150	°C

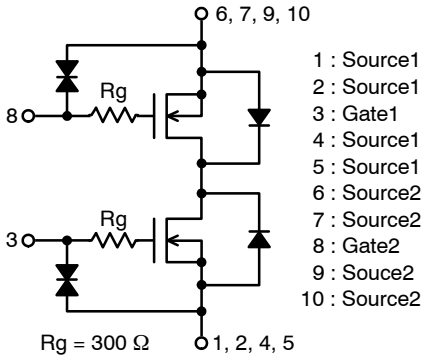
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

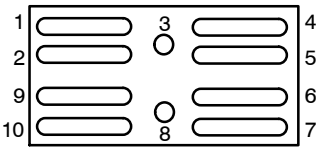
Parameter	Symbol	Value	Unit
Junction to Ambient (Note 1)	$R_{\theta JA}$	40.3	°C/W

1. Surface mounted on ceramic substrate (5000 $mm^2 \times 0.8$ mm).

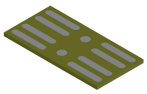
ELECTRICAL CONNECTION
N−Channel



PIN ASSIGNMENT



MARKING DIAGRAM



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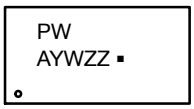


PW	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Work Week
ZZ	= Assembly Lot
▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Source to Source Breakdown Voltage	$V_{(BR)SSS}$	I_S = 1 mA, V_{GS} = 0 V Test Circuit 1	12	–	–	V
Zero−Gate Voltage Source Current	I_{SSS}	V_{SS} = 10 V, V_{GS} = 0 V Test Circuit 1	–	–	1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±8 V, V_{SS} = 0 V Test Circuit 2	–	–	±1	μA
Gate Threshold Voltage	$V_{GS(th)}$	V_{SS} = 6 V, I_S = 1 mA Test Circuit 3	0.4	–	1.3	V
Static Source to Source On−State Resistance	$R_{SS(on)}$	I_S = 5 A, V_{GS} = 4.5 V Test Circuit 4	1.55	2.10	2.75	mΩ
		I_S = 5 A, V_{GS} = 3.8 V Test Circuit 4	1.60	2.20	2.85	mΩ
		I_S = 5 A, V_{GS} = 3.1 V Test Circuit 4	1.65	2.40	3.95	mΩ
		I_S = 5 A, V_{GS} = 2.5 V Test Circuit 4	1.90	3.10	6.10	mΩ
Turn−ON Delay Time	$t_{d(on)}$	V_{SS} = 6 V, V_{GS} = 3.8 V, I_S = 5 A, R_g = 10 kΩ Test Circuit 5	–	20	–	μs
Rise Time	t_r		–	58	–	μs
Turn−OFF Delay Time	$t_{d(off)}$		–	115	–	μs
Fall Time	t_f		–	94	–	μs
Total Gate Charge	Qg	V_{SS} = 6 V,V_{GS} = 3.8 V, I_S = 5 A	–	42	–	nC
Forward Source to Source Voltage	$V_{F(S-S)}$	I_S = 3 A, V_{GS} = 0 V Test Circuit 7	–	0.75	1.20	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

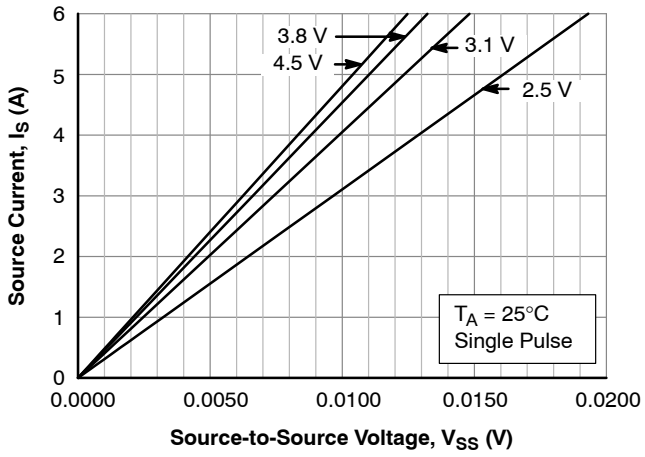


Figure 1. I_S – V_{SS}

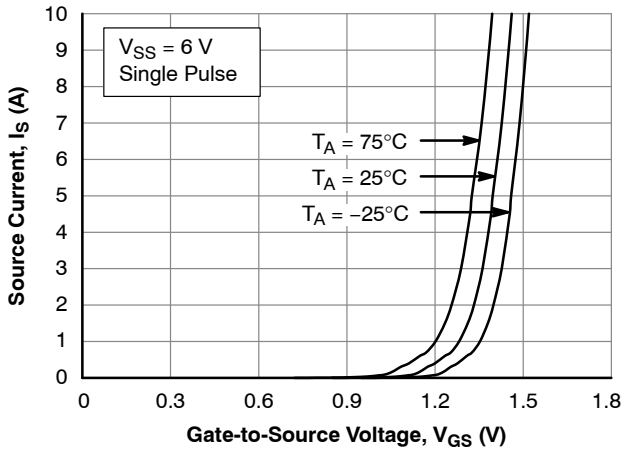


Figure 2. I_S – V_{GS}

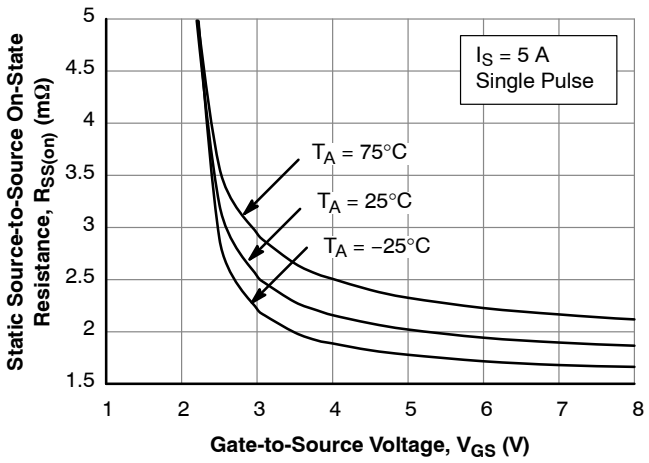


Figure 3. $R_{SS(on)}$ – V_{GS}

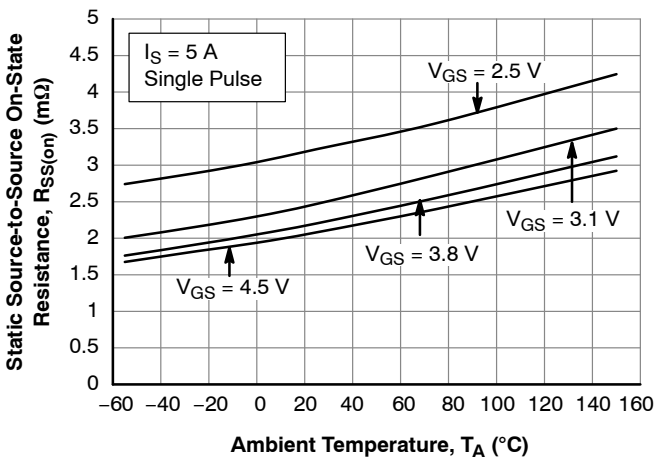


Figure 4. $R_{SS(on)}$ – T_A

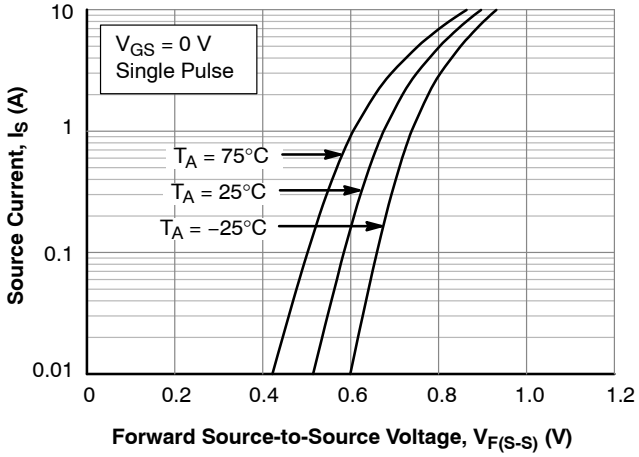


Figure 5. I_S – $V_{F(S-S)}$

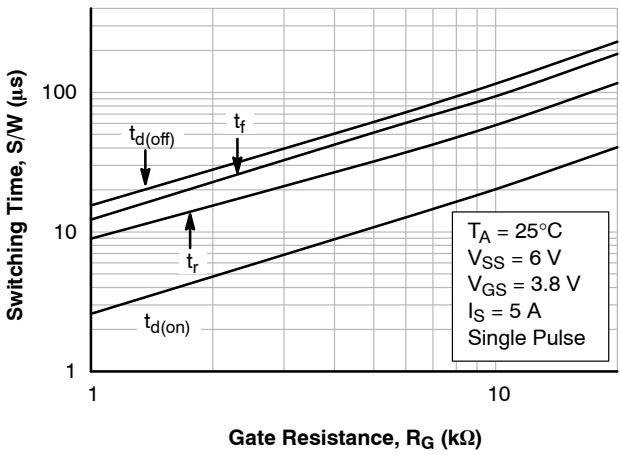


Figure 6. SW Time – R_G

TYPICAL CHARACTERISTICS (Continued)

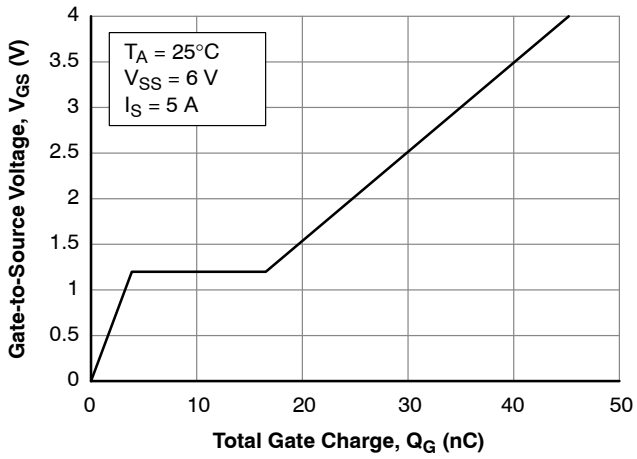


Figure 7. V_{GS} – Q_G

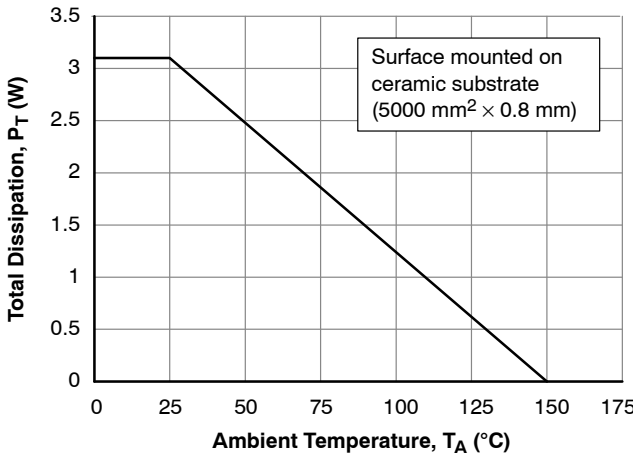


Figure 8. P_T – T_A

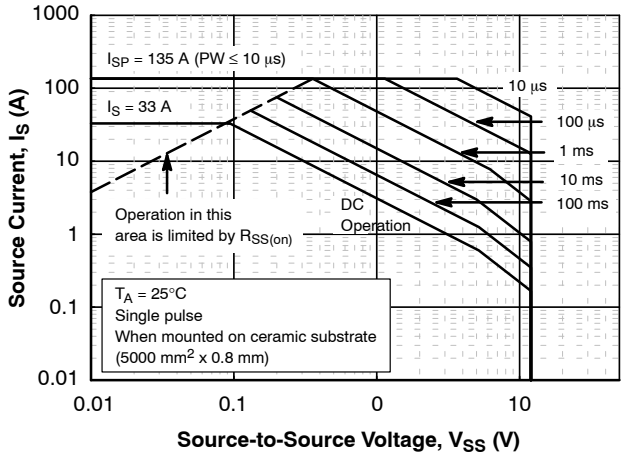


Figure 9. Safe Operating Area

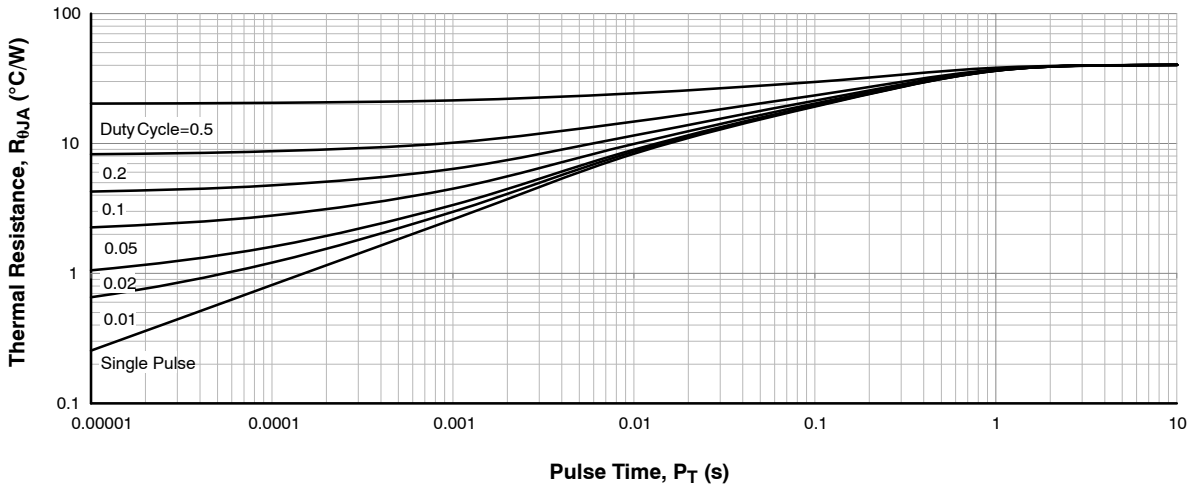
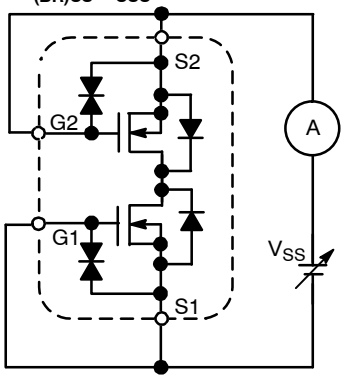


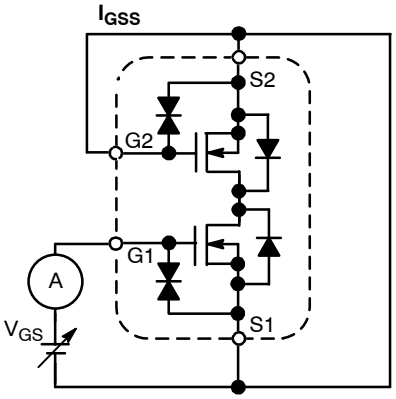
Figure 10. Thermal Response

Test Circuits are Example of Measuring FET1 Side

Test Circuit 1
$V_{(BR)SS}$ / I_{SSS}

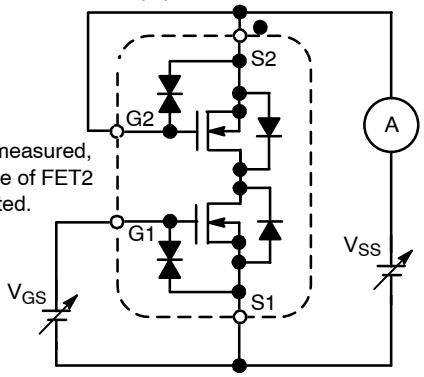


Test Circuit 2
I_{GSS}



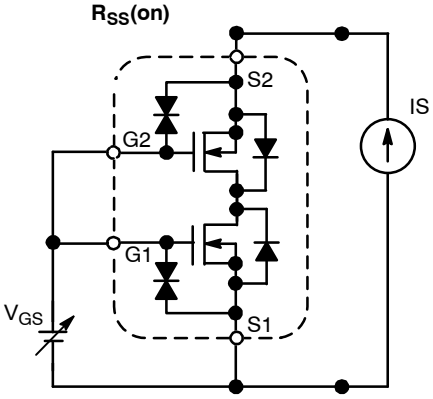
When FET1 is measured, Gate and Source of FET2 are short−circuited.

Test Circuit 3
$V_{GS(th)}$

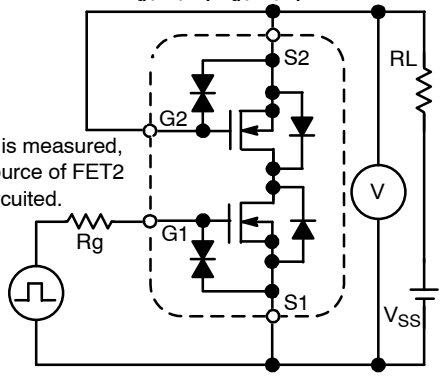


When FET1 is measured, Gate and Source of FET2 are short−circuited.

Test Circuit 4
$R_{SS(on)}$

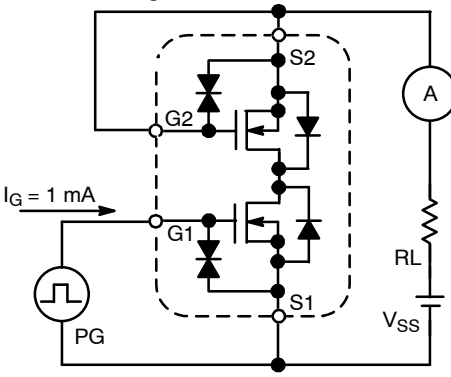


Test Circuit 5
$t_{d(on)}$, t_r, $t_{d(off)}$ t_f



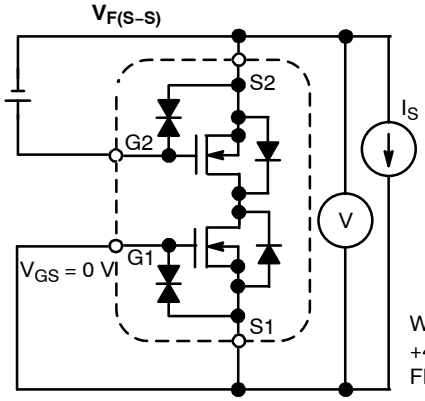
When FET1 is measured, Gate and Source of FET2 are short−circuited.

Test Circuit 6
Rg



When FET1 is measured, Gate and Source of FET2 are short−circuited.

Test Circuit 7
$V_{F(S-S)}$



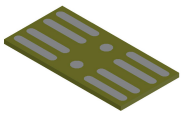
When FET1 is measured, +4.5 V is added to V_{GS} of FET2.

ORDERING INFORMATION

Device	Marking	Package	Shipping (Qty / Packing)†
EFC2K102ANUZTDG	PW	WLCSP10, 2.98x1.49x0.1 (Pb−Free/Halogen Free)	5,000 / Tape & Reel

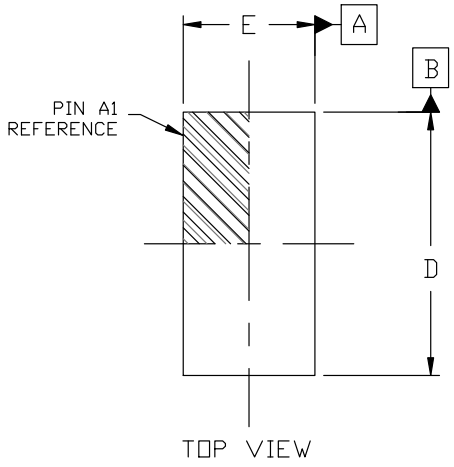
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: Since the EFC2K102ANUZ is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.



WLCSP10 2.98x1.49x0.1
CASE 567ZG
ISSUE O

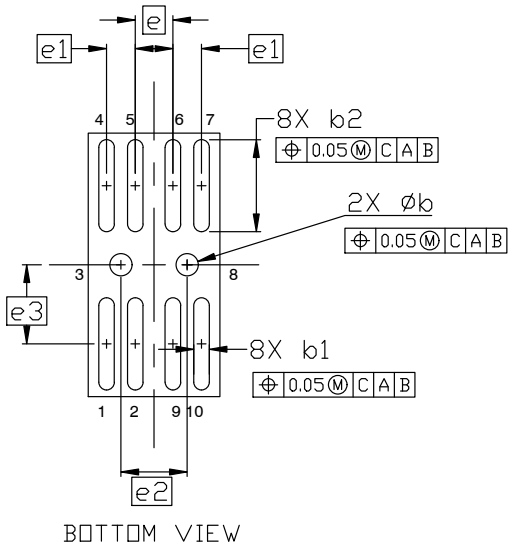
DATE 27 MAY 2020

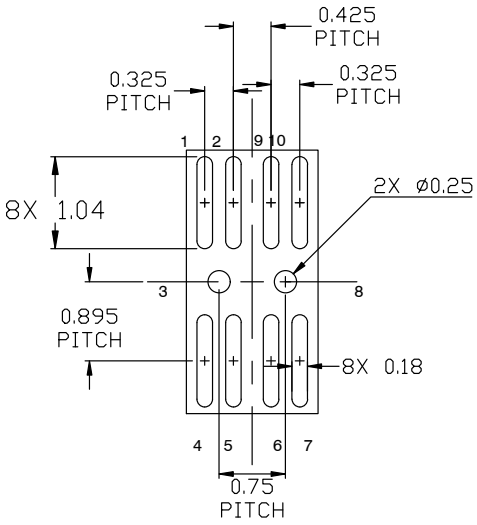


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO ALL PADS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.07	0.10	0.13
b	0.22	0.25	0.28
b1	0.145	0.175	0.205
b2	1.01	1.04	1.07
D	2.95	2.98	3.01
E	1.46	1.49	1.52
e	0.425 BSC		
e1	0.325 BSC		
e2	0.75 BSC		
e3	0.895 BSC		





* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WLCSP10 2.98x1.49x0.1**		**PAGE 1 OF 1**

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