THE DATASHEET OF

DF51K-14DP-2DS(800)

DS1558
Watchdog Clock with NV RAM Control

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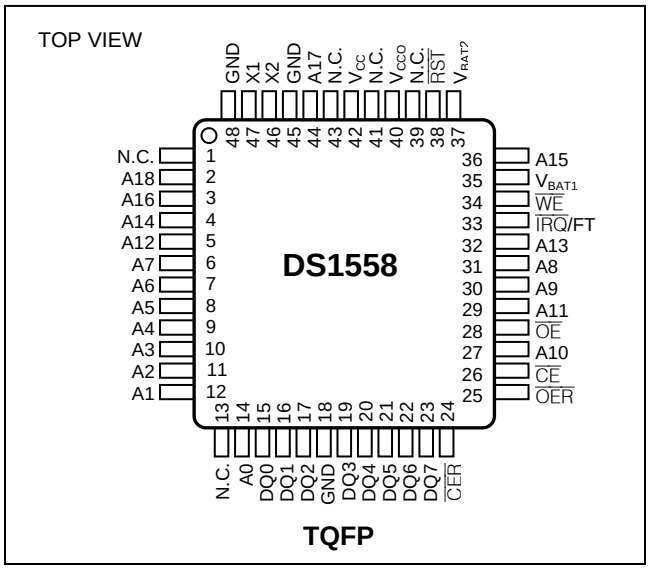
FEATURES

- Integrated Real-Time Clock (RTC), Power-Fail Control Circuit, and NV RAM Controller
- Clock Registers are Accessed Identically to the Static RAM; These Registers are Resident in the 16 Top RAM Locations
- Century Register
- Greater than 10 Years of Timekeeping and Data Retention in the Absence of Power with Small Lithium Coin Cell(s) and Low-Leakage SRAM
- Precision Power-On Reset
- Programmable Watchdog Timer and RTC Alarm
- BCD-Coded Year, Month, Date, Day, Hours, Minutes, and Seconds with Automatic Leap-Year Compensation Valid Up to the Year 2100
- Battery Voltage-Level Indicator Flag
- Power-Fail Write Protection Allows for ±10% V_{CC} Power-Supply Tolerance
- Underwriters Laboratory (UL) Recognized

PIN CONFIGURATION



TQFP

ORDERING INFORMATION

PART	TEMP RANGE	VOLTAGE (V)	PIN-PACKAGE	TOP MARK*
DS1558W	-40°C to +85°C	3.3	48 TQFP (7 x 7 x 1mm)	DS1558D
DS1558W+	-40°C to +85°C	3.3	48 TQFP (7 x 7 x 1mm)	DS1558D
DS1558W-TRL	-40°C to +85°C	3.3	48 TQFP (7 x 7 x 1mm)	DS1558D
DS1558W+TRL	-40°C to +85°C	3.3	48 TQFP (7 x 7 x 1mm)	DS1558D
DS1558Y	-40°C to +85°C	5.0	48 TQFP (7 x 7 x 1mm)	DS1558B
DS1558Y+	-40°C to +85°C	5.0	48 TQFP (7 x 7 x 1mm)	DS1558B
DS1558Y-TRL	-40°C to +85°C	5.0	48 TQFP (7 x 7 x 1mm)	DS1558B
DS1558Y+TRL	-40°C to +85°C	5.0	48 TQFP (7 x 7 x 1mm)	DS1558B

+ Denotes a lead(Pb)-free/RoHS-compliant device.
** A "+" anywhere on the top mark indicates a lead-free device.*

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

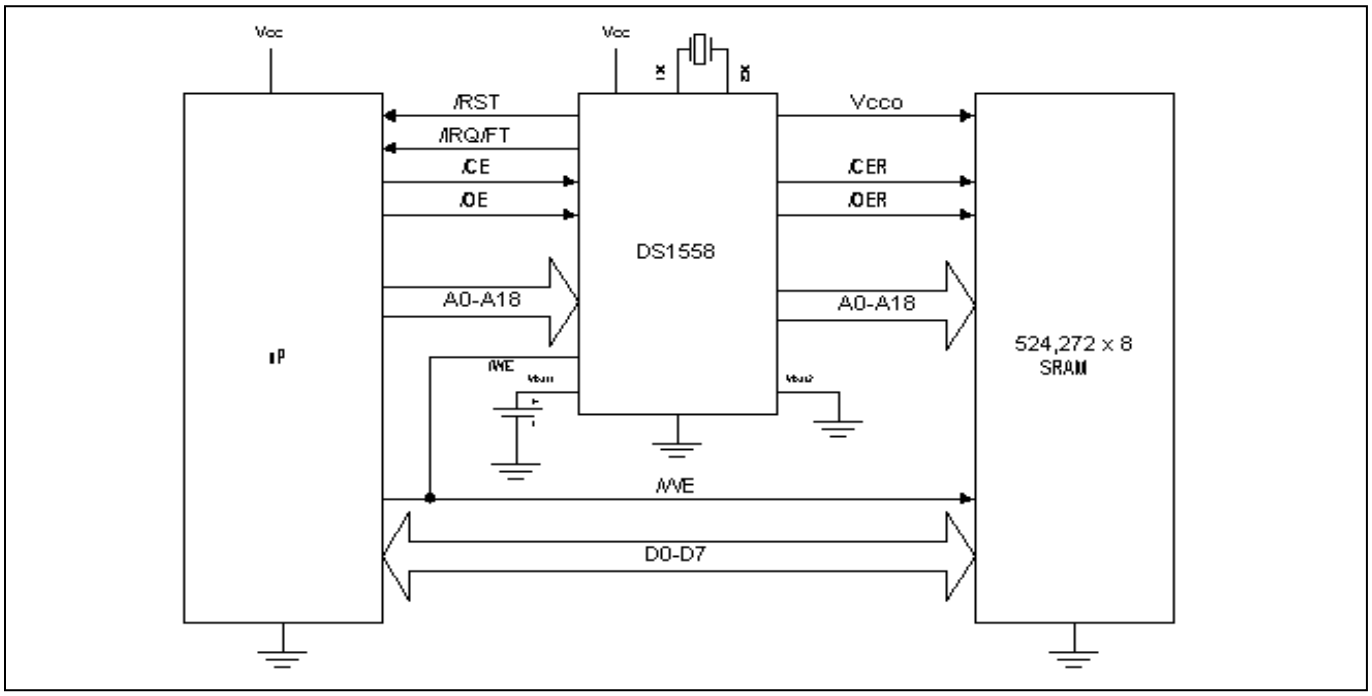
PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 13, 39 41, 43	N.C.	No Connection
2	A18	Address Inputs for Address Decode. The DS1558 uses the address inputs to determine whether or not a read or write cycle should be directed to the attached SRAM or to the RTC registers.
3	A16	
4	A14	
5	A12	
6	A7	
7	A6	
8	A5	
9	A4	
10	A3	
11	A2	
12	A1	
14	A0	
27	A10	
29	A11	
30	A9	
31	A8	
32	A13	
36	A15	
44	A17	
15	DQ0	Data Input/Outputs. Data input/output pins for the RTC registers.
16	DQ1	
17	DQ2	
19	DQ3	
20	DQ4	
21	DQ5	
22	DQ6	
23	DQ7	
18, 45, 48	GND	Ground
24	$\overline{CER}$	Active-Low Chip-Enable RAM. $\overline{CE}$ is passed through to $\overline{CER}$, with an added propagation delay. When the signals on A0–A18 match an RTC address, $\overline{CER}$ is held high, disabling the SRAM. If $\overline{OE}$ is also low, the RTC outputs data on DQ0–DQ7.
25	$\overline{OER}$	Active-Low Output-Enable RAM. $\overline{OE}$ is passed through to $\overline{OER}$, with an added propagation delay. When the signals on A0–A18 match an RTC address, $\overline{CER}$ is held high, disabling the SRAM. If $\overline{CE}$ is also low, the RTC outputs data on DQ0–DQ7.
26	$\overline{CE}$	Active-Low Chip-Enable Input. Used to access the RTC and the external SRAM.
28	$\overline{OE}$	Active-Low Output-Enable Input. Used to access the RTC and the external SRAM.
33	$\overline{IRQ}$/FT	Active-Low Interrupt/Frequency-Test Output. This pin is used to output the alarm interrupt or the frequency test signal. It is open drain and requires an external pullup resistor.
34	$\overline{WE}$	Active-Low Write Enable. Used to write data to the RTC registers.

PIN DESCRIPTION (continued)

PIN	NAME	FUNCTION
35	V_{BAT1}	Battery Inputs for Any Standard +3V Lithium Cell or Other Energy Source. Battery voltage must be held between 2.5V and 3.7V for proper operation. UL recognized to ensure against reverse charging current when used with a lithium battery. If only one battery is used, it should be attached to V_{BAT1}, and V_{BAT2} should be grounded. See "Conditions of Acceptability" at www.maxim-ic.com/TechSupport/QA/ntrl.htm.
37	V_{BAT2}	
38	$\overline{RST}$	Active-Low Power-On Reset Output (Open Drain). This pin is an output used to signal that V_{CC} is out of tolerance. On power-up, $\overline{RST}$ is held low for a period of time to allow the system to stabilize. The RTC and SRAM are not accessible while $\overline{RST}$ is active. This pin is open drain and requires an external pullup resistor.
40	V_{CCO}	V_{CC} Output to RAM. While V_{CC} is above V_{BAT}, the external SRAM is powered by V_{CC}. When V_{CC} is below the battery level, the SRAM is powered by one of the V_{BAT} inputs.
42	V_{CC}	Power-Supply Input. DC power is provided to the device on these pins. V_{CC} is the +5V input. When 5V (or 3.3V for the 3.3V version) is applied within normal limits, the device is fully accessible and data can be written and read. Reads and writes are inhibited when a 3V battery is connected to the device and V_{CC} is V_{TP}. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below V_{BAT}, the RAM and RTC are switched over to the external power supply (nominal 3.0V DC) at V_{BAT}.
46	X1	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (C_L) of 6pF. For more information about crystal selection and crystal layout considerations, refer to *Application Note 58: Crystal Considerations with Dallas Real-Time Clocks*. The DS1558 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
47	X2	

TYPICAL OPERATING CIRCUIT



DESCRIPTION

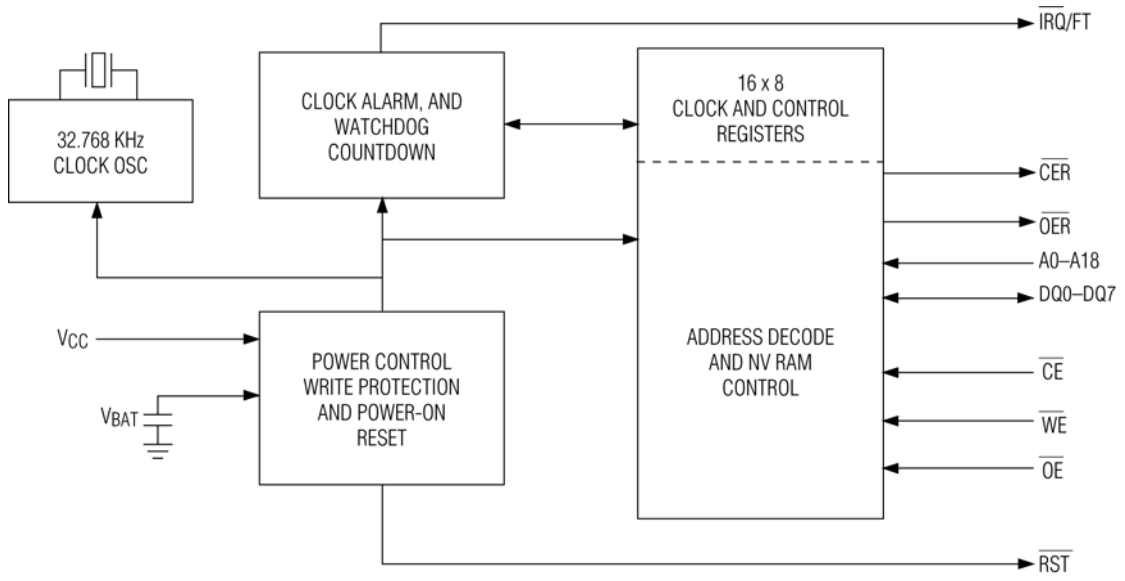
The DS1558 is a full-function, year 2000-compliant (Y2KC), real-time clock/calendar with an RTC alarm, watchdog timer, power-on reset, battery monitor, and NV SRAM controller. User access to all registers within the DS1558 is accomplished with a byte-wide interface as shown in Figure 1. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for day of month and leap year are made automatically.

The DS1558 maps the RTC registers into the SRAM address space and constantly monitors A0–A18. When any of the upper 16 address locations are accessed, the DS1558 inhibits $\overline{CER}$ and $\overline{OER}$ to the SRAM, and redirects reads and writes to the RTC registers within the DS1558. The DS1558 can be used with SRAMs up to 524,272 addresses. Smaller SRAMs can be used, provided that the unused upper address lines on the DS1558 are connected to V_{CC}.
The RTC registers are double-buffered into an internal and external set. The user has direct access to the external set. Clock/calendar updates to the external set of registers can be disabled and enabled to allow the user to access static data. Assuming the internal oscillator is turned on, the internal set of registers is continuously updated; this occurs regardless of external register settings to guarantee that accurate RTC information is always maintained.

The DS1558 has interrupt ($\overline{IRQ}$/FT) and reset ($\overline{RST}$) outputs that can be used to control CPU activity. The $\overline{IRQ}$/FT interrupt output can be used to generate an external interrupt when the RTC register values match user-programmed alarm values. The interrupt is always available while the device is powered from the system supply, and it can be programmed to occur when in the battery-backed state to serve as a system wake-up. The $\overline{IRQ}$/FT output can also be used as a CPU watchdog timer. CPU activity is monitored and an interrupt or reset output are activated if the correct activity is not detected within programmed limits. The DS1558 power-on reset can be used to detect a system power-down or failure and hold the CPU in a safe reset state until normal power returns and stabilizes; the $\overline{RST}$ output is used for this function.

The DS1558 also contains its own power-fail circuitry, which automatically protects the data in the clock and SRAM against out-of-tolerance V_{CCI} conditions by inhibiting the $\overline{CE}$ input when the V_{CC} supply enters an out-of-tolerance condition. When V_{CCI} goes below the level of V_{BAT}, the external battery is switched on to supply energy to the clock and the external SRAM. This feature provides a high degree of data security during unpredictable system operation brought on by low V_{CC} levels.

Figure 1. BLOCK DIAGRAM



NOTE: ANY UNUSED UPPER ADDRESS PINS MUST BE CONNECTED TO V_{CC} TO PROPERLY ADDRESS THE RTC.

Table 1. OPERATING MODES

V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ0–DQ7	MODE	POWER
$V_{CC} > V_{PF}$	V_{IH}	X	X	High-Z	Deselect	Standby
	V_{IL}	X	V_{IL}	D_{IN}	Write	Active
	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Read	Active
	V_{IL}	V_{IH}	V_{IH}	High-Z	Read	Active
$V_{SO} < V_{CC} < V_{PF}$	X	X	X	High-Z	Deselect	CMOS Standby
$V_{CC} < V_{SO} < V_{PF}$	X	X	X	High-Z	Data Retention	Battery Current

DATA READ MODE

The DS1558 is in the read mode whenever $\overline{CE}$ is low and $\overline{WE}$ is high. The device architecture allows ripple-through access to any valid address location. Valid data is available at the DQ pins within t_{AA} after the last address input is stable, provided that $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data is available at the latter of chip-enable access (t_{CEA}) or at output-enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data remains valid for output-data hold time (t_{OH}), but then goes indeterminate until the next address access.

DATA WRITE MODE

The DS1558 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ and $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of a subsequent read or write cycle. Data in must be valid t_{DS} prior to the end of the write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal is high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low, the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ then disables the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

The 5V device is fully accessible and data can be written and read only when V_{CC} is greater than V_{PF}. However, when V_{CC} is below the power-fail point V_{PF} (point at which write protection occurs), the internal clock registers and SRAM are blocked from any access. When V_{CC} falls below the battery switch point V_{SO} (battery supply level), device power is switched from the V_{CC} pin to the backup battery. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels.

The 3.3V device is fully accessible and data can be written and read only when V_{CC} is greater than V_{PF}. When V_{CC} falls below V_{PF}, access to the device is inhibited. If V_{PF} is less than V_{SO}, the device power is switched from V_{CC} to the internal backup lithium battery when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{SO}, the device power is switched from V_{CC} to the internal backup lithium battery when V_{CC} drops below V_{SO}. RTC operation and SRAM data are maintained from the battery until V_{CC} is returned to nominal levels.

All control, data, and address signals must be powered down when V_{CC} is powered down.

BATTERY LONGIVITY

The battery lifetime is dependent on the RAM battery standby current and the DS1558 internal clock oscillator current. The total battery current is $I_{OSC} + I_{CCO}$. When V_{CC} is above V_{PF}, I_{BAT} current is less than 50nA. The DS1558 has an internal circuit to prevent battery charging. No external protection components are required, and none should be used. The DS1558 has two battery pins that operate independently; the DS1558 selects the higher of the two inputs. If only one battery is used, the battery should be attached to V_{BAT1}, and V_{BAT2} should be grounded.

INTERNAL BATTERY MONITOR

The DS1558 constantly monitors the battery voltage of the internal battery. The battery-low flag (BLF) bit of the flags register (B4 of 7FFF0h) is not writable and should always be a 0 when read. If a 1 is ever present, both battery inputs are below 1.8V and both the contents of the RTC and RAM are questionable.

POWER-ON RESET

A temperature-compensated comparator circuit monitors the level of V_{CC}. When V_{CC} falls to the power-fail trip point, the $\overline{RST}$ signal (open drain) is pulled low. When V_{CC} returns to nominal levels, the $\overline{RST}$ signal continues to be pulled low for a period of 40ms to 200ms. The power-on reset function is independent of the RTC oscillator and thus is operational whether or not the oscillator is enabled.

CLOCK OPERATIONS

Table 2 and the following paragraphs describe the operation of the RTC, alarm, and watchdog functions.

Table 2. DS1558 REGISTER MAP

ADDRESS	DATA								FUNCTION/RANGE	
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
7FFFFh	10 YEAR				YEAR				YEAR	00–99
7FFFEh	X	X	X	10 M	MONTH				MONTH	01–12
7FFFDh	X	X	10 DATE		DATE				DATE	01–31
7FFFCh	X	FT	X	X	X	DAY			DAY	01–07
7FFFBh	X	X	10 HOUR		HOUR				HOUR	00–23
7FFFAh	X	10 MINUTES			MINUTES				MINUTES	00–59
7FFF9h	$\overline{OSC}$	10 SECONDS			SECONDS				SECONDS	00–59
7FFF8h	W	R	10 CENTURY		CENTURY				CONTROL	00–39
7FFF7h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	WATCHDOG	—
7FFF6h	AE	Y	ABE	Y	Y	Y	Y	Y	INTERRUPTS	—
7FFF5h	AM4	Y	10 DATE		DATE				ALARM DATE	01–31
7FFF4h	AM3	Y	10 HOURS		HOURS				ALARM HOURS	00–23
7FFF3h	AM2	10 MINUTES			MINUTES				ALARM MINUTES	00–59
7FFF2h	AM1	10 SECONDS			SECONDS				ALARM SECONDS	00–59
7FFF1h	Y	Y	Y	Y	Y	Y	Y	Y	UNUSED	—
7FFF0h	WF	AF	0	BLF	0	0	0	0	FLAGS	—

X = Unused, Read/Writeable Under Write and Read Bit Control

FT = Frequency Test Bit

$\overline{OSC}$ = Oscillator Start/Stop Bit

W = Write Bit

R = Read Bit

WEN = Watchdog Enable Bit

BMB0–BMB4 = Watchdog Multiplier Bits

RB0–RB1 = Watchdog Resolution Bits

AE = Alarm Flag Enable

Y = Unused, Read/Writeable Without Write and Read Bit Control

ABE = Alarm in Backup-Battery Mode Enable

AM1–AM4 = Alarm Mask Bits

WF = Watchdog Flag

AF = Alarm Flag

0 = Reads as a 0 and Cannot Be Changed

BLF = Battery Low Flag

CLOCK OSCILLATOR CONTROL

The oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB of the seconds register (B7 of 7FFF9h). Setting $\overline{OSC}$ to a 1 stops the oscillator; setting to a 0 starts the oscillator. The initial state of $\overline{OSC}$ is not guaranteed. When power is applied for the first time, the $\overline{OSC}$ bit should be enabled. Oscillator operation and frequency can be verified by setting the FT bit and monitoring the $\overline{IRQ}$/FT pin for 512Hz.

OSCILLATOR STARTUP TIME

Oscillator startup times are highly dependent upon crystal characteristics and layout. High ESR and excessive capacitive loads are the major contributors to long startup times. A circuit using a crystal with the recommended characteristics and following the recommended layout usually starts within 1 second.

READING THE CLOCK

When reading the RTC data, it is recommended to halt updates to the external set of double-buffered RTC registers. This puts the external registers into a static state, allowing data to be read without register values changing during the read process. Normal updates to the internal registers continue while in this state. External updates are halted when a 1 is written into the read bit, B6 of the control register (7FFF8h). As long as a 1 remains in the control register read bit, updating is halted. After a halt is issued, the registers reflect the RTC count (day, date, and time) that was current at the moment the halt command is issued. Normal updates to the external set of registers resume within 1 second after the read bit is set to a 0 for a minimum of 500µs. The read bit must be a 0 for a minimum of 500µs to ensure the external registers are updated.

SETTING THE CLOCK

The MSB bit, B7, of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the 7FFF8h–7FFFFh registers. After setting the write bit to a 1, RTC registers can be loaded with the desired RTC count (day, date, and time) in 24-hour BCD format. Setting the write bit to a 0 then transfers the values written to the internal RTC registers and allows normal operation to resume.

CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by the crystal-frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Refer to *Application Note 58* "Crystal Considerations with Dallas Real-Time Clocks" for detailed information.

FREQUENCY TEST MODE

The DS1558 frequency test mode uses the open-drain $\overline{IRQ}$/FT output. With the oscillator running, the $\overline{IRQ}$/FT output toggles at 512Hz when the FT bit is a 1, the alarm-flag enable bit (AE) is a 0, and the watchdog-enable bit (WDS) is a 1, or the watchdog register is reset (register 7FFF7h = 00h). The $\overline{IRQ}$/FT output and the frequency test mode can be used as a measure of the actual frequency of the 32.768kHz RTC oscillator. The $\overline{IRQ}$/FT pin is an open-drain output that requires a pullup resistor for proper operation. The FT bit is cleared to a 0 on power-up.

USING THE CLOCK ALARM

The alarm settings and control for the DS1558 reside within registers 7FFF2h–7FFF5h. Register 7FFF6h contains two alarm-enable bits: alarm enable (AE) and alarm in backup enable (ABE). The AE and ABE bits must be set as described below for the $\overline{IRQ}$/FT output to be activated for a matched alarm condition.

The alarm can be programmed to activate on a specific day of the month or repeat every day, hour, minute, or second. It can also be programmed to go off while the DS1558 is in the battery-backed state of operation to serve as a system wake-up. Alarm mask bits AM1–AM4 control the alarm mode. Table 3 shows the possible settings. Configurations not listed in the table default to the once-per-second mode to notify the user of an incorrect alarm setting.

Table 3. ALARM MASK BITS

AM4	AM3	AM2	AM1	ALARM RATE
1	1	1	1	Once per second
1	1	1	0	When seconds match
1	1	0	0	When minutes and seconds match
1	0	0	0	When hours, minutes, and seconds match
0	0	0	0	When date, hours, minutes, and seconds match

When the RTC register values match alarm register settings, AF is set to a 1. If AE is also set to a 1, the alarm condition activates the $\overline{IRQ}$/FT pin. The $\overline{IRQ}$/FT signal is cleared by a read or write to the flags register (address 7FFF0h). When $\overline{CE}$ is active, the $\overline{IRQ}$/FT signal can be cleared by having the address stable for as short as 15ns and either $\overline{OE}$ or $\overline{WE}$ active, but is not guaranteed to be cleared unless t_{RC} is fulfilled (Figure 2). Once the address has been selected for at least 15ns, the $\overline{IRQ}$/FT signal can be cleared immediately, but is not guaranteed to be cleared until t_{RC} is fulfilled (Figure 3). The alarm flag is also cleared by a read or write to the flags register, but the flag does not change states until the end of the read/write cycle and the $\overline{IRQ}$/FT signal has been cleared.

The $\overline{IRQ}$/FT pin can also be activated in the battery-backed mode. The $\overline{IRQ}$/FT goes low if an alarm occurs and both ABE and AE are set. The ABE and AE bits are cleared during the power-up transition, but an alarm generated during power-up sets AF. Therefore, the AF bit can be read after system power-up to determine if an alarm was generated during the power-up sequence. Figure 4 illustrates alarm timing during the backup-battery mode and power-up states.

Figure 2. CLEARING IRQ WAVEFORMS ACTIVE

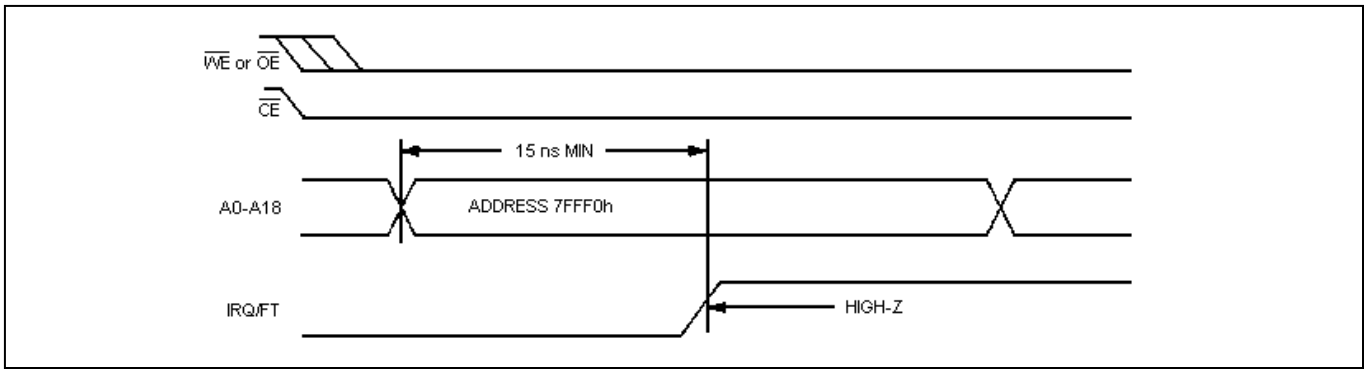


Figure 3. CLEARING IRQ WAVEFORMS

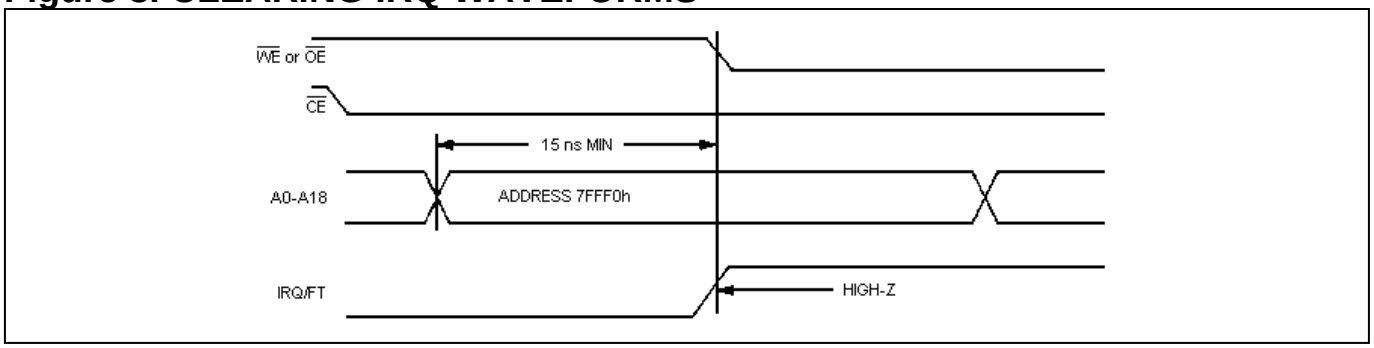
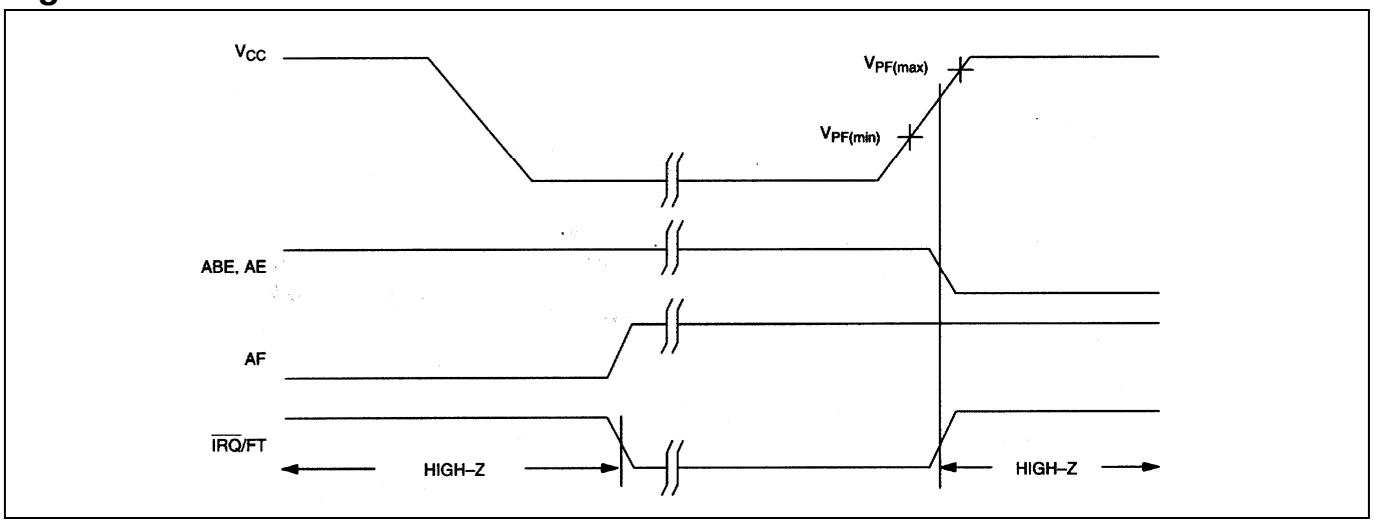


Figure 4. BACKUP MODE ALARM WAVEFORMS



USING THE WATCHDOG TIMER

The watchdog timer can be used to detect an out-of-control processor. The user programs the watchdog timer by setting the desired amount of timeout into the 8-bit watchdog register (address 7FFF7h). The five watchdog register bits BMB4–BMB0 store a binary multiplier and the two lower-order bits RB1–RB0 select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds. The watchdog timeout value is then determined by the multiplication of the 5-bit multiplier value with the 2-bit resolution value. (For example: writing 00001110 in the watchdog register = 3 x 1 second or 3 seconds.) If the processor does not reset the timer within the specified period, the watchdog flag (WF) is set and a processor interrupt is generated and stays active until either WF is read or the watchdog register (7FFF7h) is read or written.

The MSB of the watchdog register is the watchdog steering bit (WDS). When set to a 0, the watchdog activates the $\overline{\text{IRQ}}$/FT output when the watchdog times out. WDS should not be written to a 1, and should be initialized to a 0 if the watchdog function is enabled.

The watchdog timer resets when the processor performs a read or write of the watchdog register. The timeout period then starts over. The watchdog timer is disabled by writing a value of 00h to the watchdog register. The watchdog function is automatically disabled upon power-up and the watchdog register is cleared.

POWER-ON DEFAULT STATES

Upon application of power to the device, the following register bits are set to a 0:

WDS = 0, BMB0–BMB4 = 0, RB0–RB1 = 0, AE = 0, and ABE = 0

All other bits are undefined.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.3V to +6.0V
Storage Temperature Range…….-55°C to +125°C
Soldering Temperature…….See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 3.3V ±10% or 5V ±10%, T_A = -40°C to +85°C.)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1 Voltage (All Inputs)	V_{CC} = +5V ±10%	V_{IH}	2.2		V_{CC} + 0.3V	V	1
	V_{CC} = +3.3V ±10%		2.0		V_{CC} + 0.3V		
Logic 0 Voltage (All Inputs)	V_{CC} = +5V ±10%	V_{IL}	-0.3		+0.8	V	1
	V_{CC} = +3.3V ±10%		-0.3		+0.6		
Battery Voltage		V_{BAT}	2.5	3.3	3.7	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V ±10% or +5V ±10%, T_A = -40°C to +85°C.)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current, +5V		I_{CC}		6	25	mA	2, 3
Active Supply Current, +3.3V		I_{CC}		4	15	mA	2, 3
TTL Standby, +5V ($\overline{CE}$ = V_{IH})		I_{CC1}		3	6	mA	2, 3
TTL Standby, +3.3V ($\overline{CE}$ = V_{IH})		I_{CC1}		2	6	mA	2, 3
CMOS Standby Current, +5V ($\overline{CE}$ ≥ V_{CC} - 0.2V)		I_{CC2}		2	6	mA	2, 3
CMOS Standby Current, +3.3V ($\overline{CE}$ ≥ V_{CC} - 0.2V)		I_{CC2}		1	2	mA	2, 3
Input Leakage Current (Any Input)		I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)		I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)		V_{OH}	2.4			V	1
Output Logic 0 Voltage	I_{OUT} = 2.1mA, DQ0–DQ7 Outputs	V_{OL1}			0.4	V	1
	I_{OUT} = 7.0mA, $\overline{IRQ}$/FT and $\overline{RST}$ Outputs	V_{OL2}			0.4	V	1, 5
Write Protection Voltage, +5V		V_{PF}	4.20	4.37	4.50	V	1
Write Protection Voltage, +3.3V		V_{PF}	2.75	2.88	2.97	V	1
Battery Switchover Voltage, +5V		V_{SO}		V_{BAT}		V	1
Battery Switchover Voltage, +3.3V		V_{SO}		V_{PF}		V	1, 4
Battery Current OSC On		I_{OSC}		0.3	0.5	µA	6,7
Battery Current OSC Off		I_{BACKUP}			100	nA	7
Output Voltage I_{CCO} = 70mA, +5V		V_{CC01}	V_{CC1} - 0.3			V	
Output Voltage I_{CCO} = 40mA, +3.3V		V_{CC01}	V_{CC1} - 0.3			V	
Output Voltage I_{CCO} = 10µA		V_{CC02}	V_{BAT} - 0.2	V_{BAT} - 0.031		V	10

CRYSTAL SPECIFICATIONS*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Nominal Frequency	f_O		32.768		kHz	
Series Resistance	ESR			45	kΩ	
Load Capacitance	C_L		6		pF	

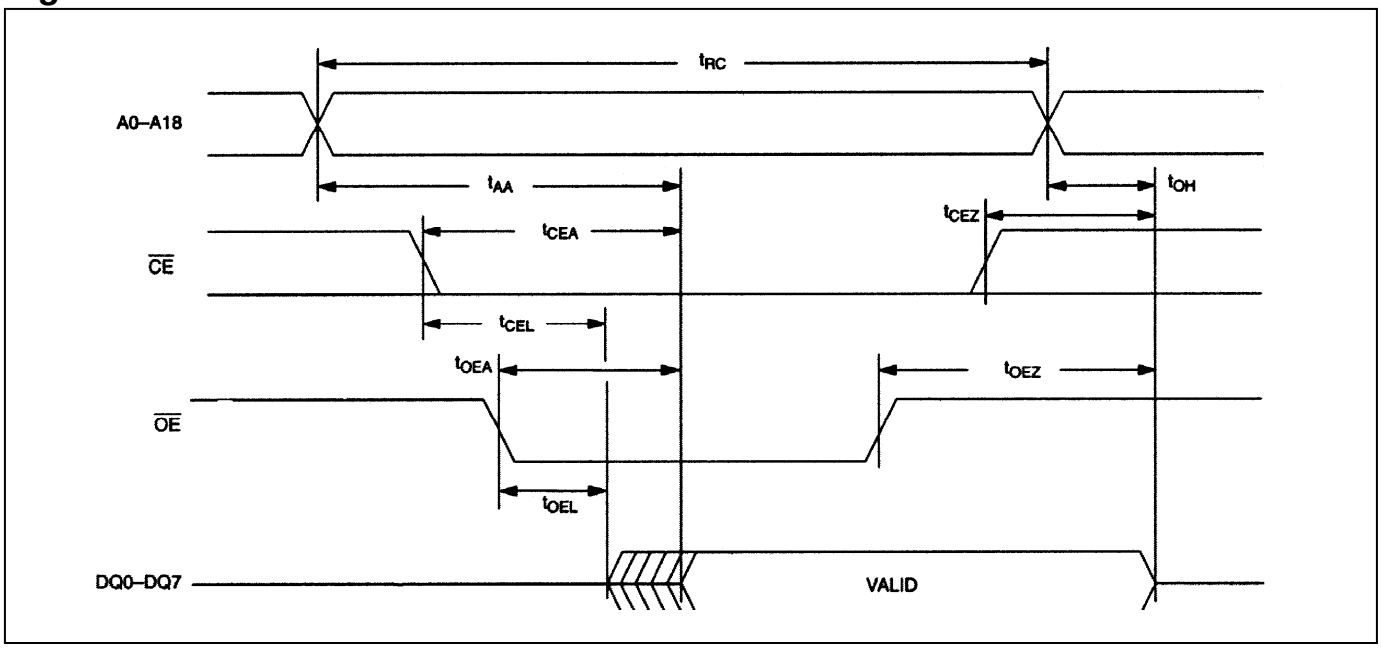
**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to* Application Note 58: Crystal Considerations for Dallas Real-Time Clocks *for additional specifications.*

READ CYCLE, AC CHARACTERISTICS

(V_{CC} = +3.3V ±10% or +5V ±10%, T_A = -40°C to +85°C.) (Figure 5)

PARAMETER	SYMBOL	V_{CC} = +5.5V ±10%		V_{CC} = +3.3V ±10%		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	70		120		ns	
Address Access Time	t_{AA}		70		120	ns	
$\overline{CE}$ to DQ Low-Z	t_{CEL}	5		5		ns	
$\overline{CE}$ Access Time	t_{CEA}		70		120	ns	
$\overline{CE}$ Data Off Time	t_{CEZ}		25		40	ns	
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5		5		ns	
$\overline{OE}$ Access Time	t_{OEA}		35		100	ns	
$\overline{OE}$ Data Off Time	t_{OEZ}		25		35	ns	
Output Hold from Address	t_{OH}	5		5		ns	
$\overline{CE}$ to $\overline{CER}$ Propagation Delay, +5V	t_{CEPD}		15			ns	
$\overline{OE}$ to $\overline{OER}$ Propagation Delay, +5V	t_{OEPD}		20			ns	
$\overline{CE}$ to $\overline{CER}$ Propagation Delay, +3.3V	t_{CEPD}		30			ns	
$\overline{OE}$ to $\overline{OER}$ Propagation Delay, +3.3V	t_{OEPD}		40			ns	

Figure 5. READ CYCLE TIMING DIAGRAM



WRITE CYCLE, AC CHARACTERISTICS

(V_{CC} = +3.3V ±10% or +5V ±10%, T_A = -40°C to +85°C.) (Figure 6 and Figure 7)

PARAMETER	SYMBOL	V_{CC} = +5.0V ±10%		V_{CC} = +3.3V ±10%		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Write Cycle Time	t_{WC}	70		120		ns	
Address Access Time	t_{AS}	0		0		ns	
$\overline{WE}$ Pulse Width	t_{WEW}	50		100		ns	
$\overline{CE}$ Pulse Width	t_{CEW}	60		110		ns	
Data Setup Time	t_{DS}	30		80		ns	
Data Hold Time	t_{DH1}	5		5		ns	8
Data Hold Time	t_{DH2}	5		5		ns	9
Address Hold Time	t_{AH1}	5		0		ns	8
Address Hold Time	t_{AH2}	5		5		ns	9
$\overline{WE}$ Data Off Time	t_{WEZ}		25		40	ns	
Write Recovery Time	t_{WR}	5		10		ns	

Figure 6. WRITE CYCLE TIMING, WRITE-ENABLE CONTROLLED

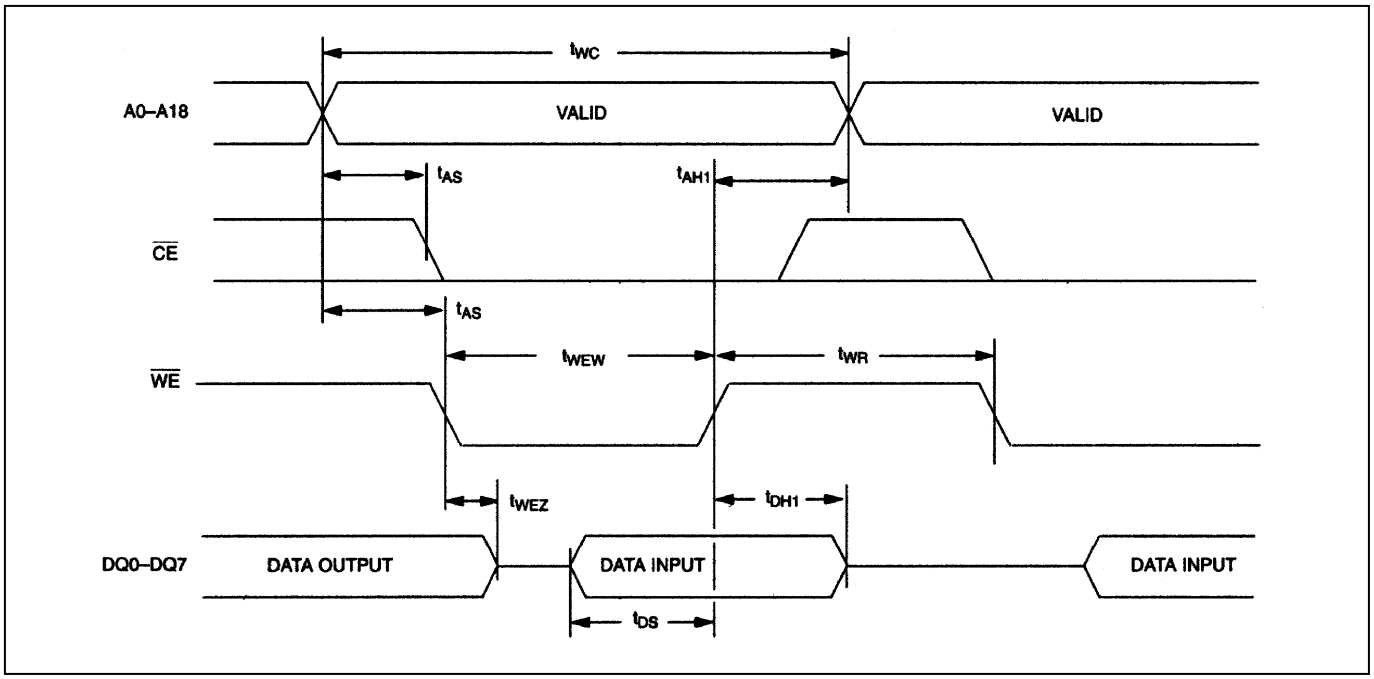
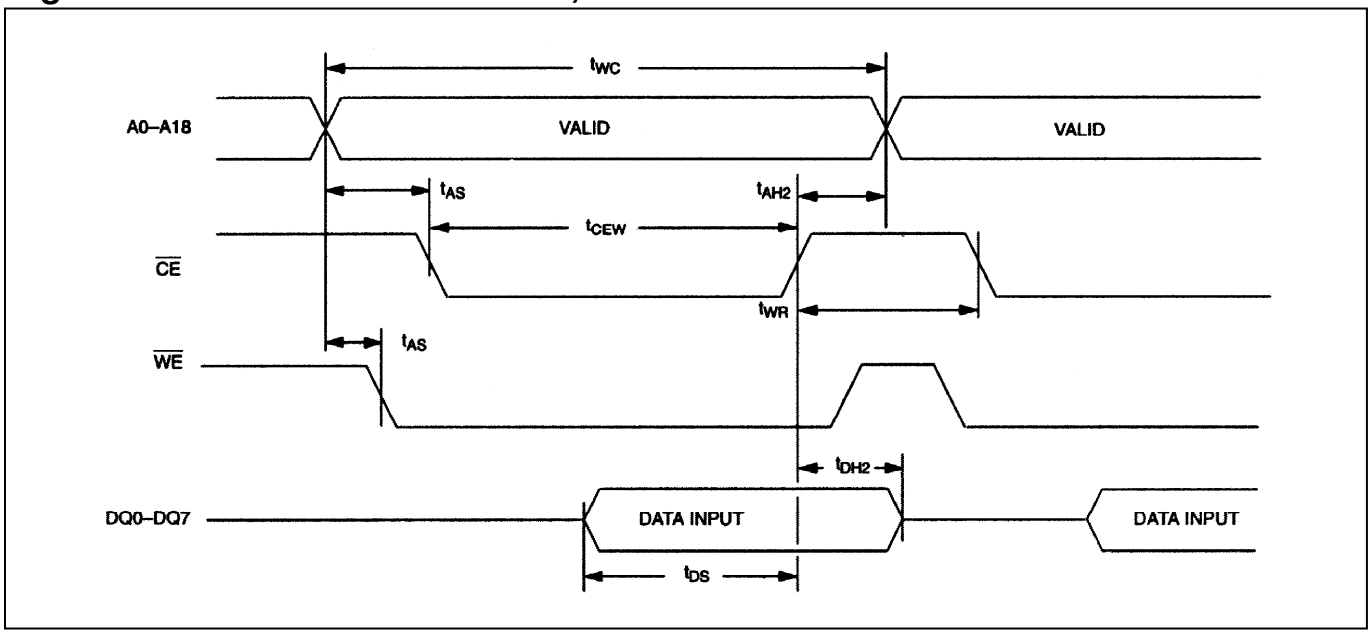


Figure 7. WRITE CYCLE TIMING, CHIP-ENABLE CONTROLLED

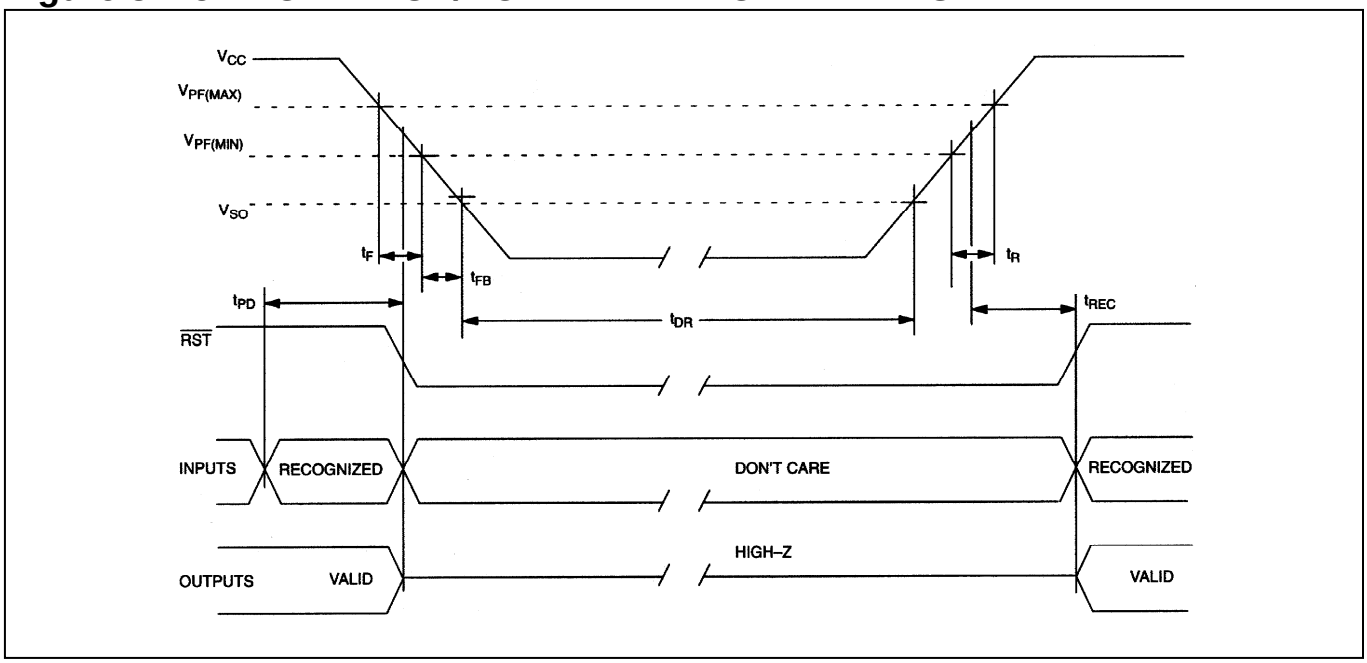


POWER-UP/DOWN CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C.) (Figure 8)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH}, Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Fall Time: $V_{PF(MIN)}$ to V_{SO}	t_{FB}	10			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
V_{PF} to $\overline{RST}$ High	t_{REC}	40		200	ms	

Figure 8. +5V POWER-UP/DOWN WAVEFORM TIMING

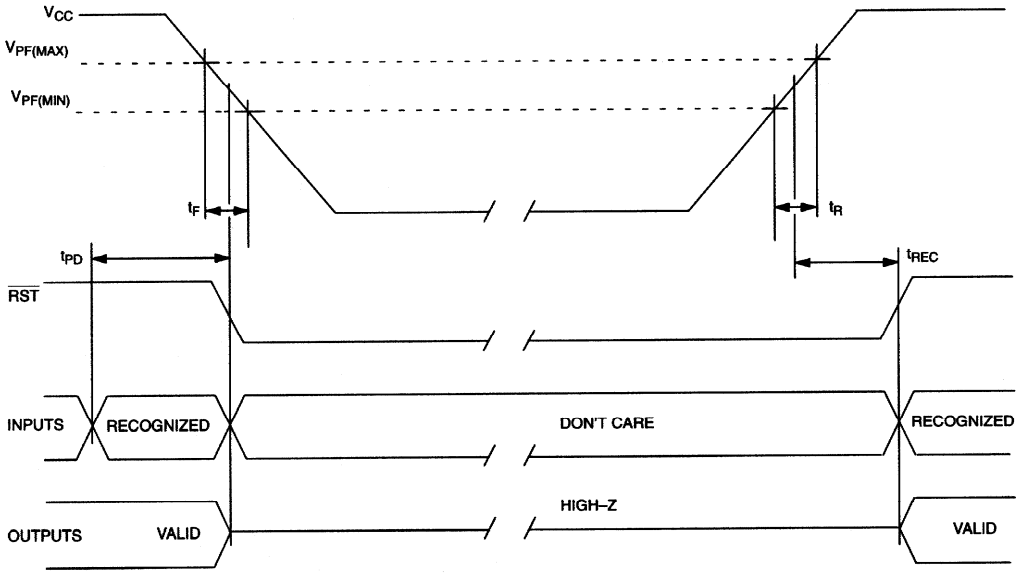


POWER-UP/DOWN CHARACTERISTICS

(V_{CC} = +3.3V ±10%, T_A = -40°C to +85°C.) (Figure 9)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH}, Before Power-Down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
V_{PF} to $\overline{RST}$ High	t_{REC}	40		200	ms	

Figure 9. +3.3V POWER-UP/DOWN WAVEFORM TIMING



CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance On All Input Pins	C_{IN}			7	pF	1
Capacitance On $\overline{IRQ}$/FT, $\overline{RST}$, and DQ Pins	C_{IO}			10	pF	1

AC TEST CONDITIONS

Output Load: 25pF
Input Pulse Levels: 0 to +3V
Timing Measurement Reference Levels:
Input: +1.5V
Output: +1.5V
Input Pulse Rise and Fall Times: 5ns

NOTES:

1) Voltage referenced to ground.
2) Typical values are at +25°C and nominal supplies.
3) Outputs are open.
4) Battery switchover occurs at the lower of either the battery voltage or V_{PF}.
5) The $\overline{IRQ}$/FT and $\overline{RST}$ outputs are open drain.
6) Using the recommended crystal on X1 and X2.
7) V_{CCO}, $\overline{CER}$, and $\overline{OER}$ pins open.
8) t_{AH1}, t_{DH1} are measured from $\overline{WE}$ going high.
9) t_{AH2}, t_{DH2} are measured from $\overline{CE}$ going high.
10) Typical measured with V_{BAT} at 3.0V. Typical with I_{CCO} = 100µA and V_{BAT} = 3.0V is V_{BAT} - 0.322.

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 TQFP	C48+1	**21-0054**

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