



**THE DATASHEET OF
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High Voltage COG Dielectric, 500 – 3,000 VDC (Automotive Grade)

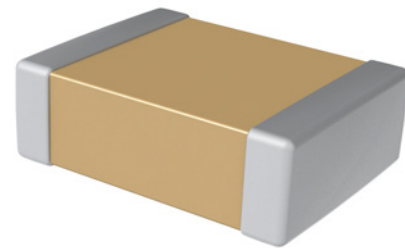
Overview

KEMET's Automotive Grade High Voltage surface mount MLCCs in COG dielectric are temperature compensating and are suited for resonant circuit applications or those where Q and stability of capacitance characteristics are required. COG exhibits no change in capacitance with respect to time and voltage and boasts a negligible change in capacitance with reference to ambient temperature. Capacitance change is limited to $\pm 30\text{ppm}/^\circ\text{C}$ from -55°C to $+125^\circ\text{C}$.

Their exceptional performance at high frequencies has made COG high voltage the preferred dielectric choice of design engineers worldwide. Whether under-hood or in-cabin, these capacitors are designed to provide reliable performance in mission and safety critical automotive circuits. Stricter testing protocol and inspection criteria have been established for automotive grade products in recognition of potentially harsh environmental conditions. KEMET automotive grade series capacitors meet the demanding Automotive Electronics Council's AEC-Q200 qualification requirements.

Benefits

- AEC-Q200 automotive qualified
- Operating temperature range of -55°C to $+125^\circ\text{C}$
- Capacitance offerings ranging from 1 pF to 0.15 μF
- DC voltage ratings of 500 V, 630 V, 1 KV, 1.5 KV, 2 KV, 2.5 KV and 3 KV
- EIA 0402, 0603, 0805, 1206, 1210, 1808, 1812, 1825, 2220, 2225, 2824, 3040, 3640 and 4540 case sizes
- Extremely low ESR and ESL
- High ripple current capability
- No capacitance shift with voltage
- Negligible capacitance shift with respect to temperature
- No piezoelectric noise
- Lead (Pb)-Free, RoHS and REACH compliant



Applications

- High frequency power converters
- Wide bandgap (WBG), silicon carbide (SiC) and gallium nitride (GaN) systems
- Snubber (high dV/dT)
- Resonant circuits (LLC, Wireless Charging, etc)
- Timing
- Filtering

Ordering Information

C	1210	C	332	J	C	G	A	C	AUTO
Ceramic	Case Size (L" x W")	Specification/ Series	Capacitance Code (pF)	Capacitance Tolerance ¹	Rated Voltage (VDC)	Dielectric	Failure Rate/ Design	Termination Finish ²	Packaging/Grade (C-Spec)
	0402 0603 0805 1206 1210 1808 1812 1825 2220 2225 2824 3040 3640 4540	C = Standard	Two significant digits and number of zeros.	B = ±0.10 pF C = ±0.25 pF D = ±0.5 pF F = ±1% G = ±2% J = ±5% K = ±10% M = ±20%	C = 500 B = 630 D = 1,000 F = 1,500 G = 2,000 Z = 2,500 H = 3,000	G = COG	A = N/A	C = 100% Matte Sn	See "Packaging C-Spec Ordering Options Table"

¹ Additional capacitance tolerance offerings may be available. Contact KEMET for details.

² Additional termination finish options may be available. Contact KEMET for details.

Packaging C-Spec Ordering Options Table

Packaging Type ¹	Packaging/Grade Ordering Code (C-Spec) ²
7" Reel	AUTO
13" Reel/Unmarked	AUTO7411 (EIA 0603 and smaller case sizes) AUTO7210 (EIA 0805 and larger case sizes)

¹ Reeling tape options (Paper or Plastic) are dependent on capacitor case size (L" x W") and thickness dimension. See "Chip Thickness/Tape & Reel Packaging Quantities" and "Tape & Reel Packaging Information".

² All Automotive packaging C-Specs listed exclude the option to laser mark components. Please contact KEMET if you require a laser marked option. For more information see "Capacitor Marking".

² For additional information regarding "AUTO" C-Spec options, see "Automotive C-Spec Information."

Automotive C-Spec Information

KEMET automotive grade products meet or exceed the requirements outlined by the Automotive Electronics Council. Details regarding test methods and conditions are referenced in document AEC-Q200, Stress Test Qualification for Passive Components. These products are supported by a Product Change Notification (PCN) and Production Part Approval Process warrant (PPAP).

Automotive products offered through our distribution channel have been assigned an inclusive ordering code C-Spec, "AUTO." This C-Spec was developed in order to better serve small and medium-sized companies that prefer an automotive grade component without the requirement to submit a customer Source Controlled Drawing (SCD) or specification for review by a KEMET engineering specialist. This C-Spec is therefore not intended for use by KEMET OEM automotive customers and are not granted the same "privileges" as other automotive C-Specs. Customer PCN approval and PPAP request levels are limited (see details below.)

Product Change Notification (PCN)

The KEMET product change notification system is used to communicate primarily the following types of changes:

- Product/process changes that affect product form, fit, function, and/or reliability
- Changes in manufacturing site
- Product obsolescence

KEMET Automotive C-Spec	Customer Notification Due To:		Days Prior To Implementation
	Process/Product change	Obsolescence*	
KEMET assigned ¹	Yes (with approval and sign off)	Yes	180 days minimum
AUTO	Yes (without approval)	Yes	90 days minimum

¹ KEMET assigned C-Specs require the submittal of a customer SCD or customer specification for review. For additional information contact KEMET.

Production Part Approval Process (PPAP)

The purpose of the Production Part Approval Process is:

- To ensure that supplier can meet the manufacturability and quality requirements for the purchased parts.
- To provide the evidence that all customer engineering design records and specification requirements are properly understood and fulfilled by the manufacturing organization.
- To demonstrate that the established manufacturing process has the potential to produce the part.

KEMET Automotive C-Spec	PPAP Level				
	1	2	3	4	5
KEMET assigned ¹	●	●	●	●	●
AUTO			○		

¹ KEMET assigned C-Specs require the submittal of a customer SCD or customer specification for review. For additional information contact KEMET.

- Part number specific PPAP available with customer information included.
- Product family PPAP only

Dimensions – Millimeters (Inches)



EIA Size Code	Metric Size Code	L Length	W Width	T Thickness	B Bandwidth	S Separation Minimum	Mounting Technique
0402	1005	1.00 (0.040) ±0.05 (0.002)	0.50 (0.020) ±0.05 (0.002)	See Table 2 for Thickness	0.30 (0.012) ±0.10 (0.004)	0.30 (0.012)	Solder Reflow Only
0603	1608	1.60 (0.063) ±0.15 (0.006)	0.80 (0.032) ±0.15 (0.006)		0.35 (0.014) ±0.15 (0.006)	0.50 (0.020)	Solder Wave or Solder Reflow
0805	2012	2.00 (0.079) ±0.20 (0.008)	1.25 (0.049) ±0.20 (0.008)		0.50 (0.02) ±0.25 (0.010)	0.70 (0.028)	
1206	3216	3.20 (0.126) ±0.20 (0.008)	1.60 (0.063) ±0.20 (0.008)		0.50 (0.02) ±0.25 (0.010)	1.50 (0.060)	Solder Reflow Only
1210	3225	3.20 (0.126) ±0.20 (0.008)	2.50 (0.098) ±0.20 (0.008)		0.50 (0.02) ±0.25 (0.010)	1.50 (0.060)	
1808	4520	4.70 (0.185) ±0.50 (0.020)	2.00 (0.079) ±0.20 (0.008)		0.60 (0.024) ±0.35 (0.014)	2.90 (0.114)	Solder Reflow Only
1812	4532	4.50 (0.177) ±0.30 (0.012)	3.20 (0.126) ±0.30 (0.012)		0.60 (0.024) ±0.35 (0.014)	2.30 (0.091)	
1825	4564	4.50 (0.177) ±0.30 (.012)	6.40 (0.252) ±0.40 (0.016)		0.60 (0.024) ±0.35 (0.014)	2.30 (0.091)	
2220	5650	5.70 (0.224) ±0.40 (0.016)	5.00 (0.197) ±0.40 (0.016)		0.60 (0.024) ±0.35 (0.014)	3.50 (0.138)	
2225	5664	5.60 (0.220) ±0.40 (0.016)	6.40 (0.248) ±0.40 (0.016)		0.60 (0.024) ±0.35 (0.014)	3.20 (0.126)	
2824	7260	7.10 (0.280) ±0.40 (0.016)	6.10 (0.240) ±0.40 (0.016)		1.27 (0.050) ±0.40 (0.016)	4.20 (0.165)	
3040	7610	7.60 (0.300) ±0.40 (0.016)	10.20 (0.402) ±0.40 (0.016)		1.27 (0.050) ±0.40 (0.016)	4.20 (0.165)	
3640	9210	9.10 (0.358) ±0.40 (0.016)	10.20 (0.402) ±0.40 (0.016)		1.27 (0.050) ±0.40 (0.016)	6.30 (0.248)	
4540	-	11.40 (0.449) ±0.40 (0.016)	10.20 (0.402) ±0.40 (0.016)		1.27 (0.050) ±0.40 (0.016)	6.30 (0.248)	

Qualification/Certification

Automotive Grade products meet or exceed the requirements outlined by the Automotive Electronics Council. Details regarding test methods and conditions are referenced in document AEC-Q200, Stress Test Qualification for Passive Components. For additional information regarding the Automotive Electronics Council and AEC-Q200, please visit their website at www.aecouncil.com.

Environmental Compliance

Lead (Pb)-free, RoHS, and REACH compliant without exemptions.

Electrical Parameters/Characteristics

Item	Parameters/Characteristics
Operating Temperature Range	-55°C to +125°C
Capacitance Change with Reference to +25°C and 0 VDC Applied (TCC)	±30 ppm/°C
Aging Rate (Maximum % Capacitance Loss/Decade Hour)	0%
¹ Dielectric Withstanding Voltage (DWV)	See Dielectric Withstanding Voltage (DWV) Table (5 ±1 seconds and charge/discharge not exceeding 50 mA)
² Dissipation Factor (DF) Maximum Limit at 25°C	0.1%
³ Insulation Resistance (IR) Limit at 25°C	1,000 megohm microfarads or 100 GΩ (500 VDC applied for 120 ±5 seconds at 25°C)

¹ DWV is the voltage a capacitor can withstand (survive) for a short period of time. It exceeds the nominal and continuous working voltage of the capacitor.

² Capacitance and dissipation factor (DF) measured under the following conditions:

1 MHz ±100 kHz and 1.0 V_{rms} ±0.2 V if capacitance ≤ 1,000 pF

1 kHz ±50 Hz and 1.0 V_{rms} ±0.2 V if capacitance > 1,000 pF

³ To obtain IR limit, divide MΩ-μF value by the capacitance and compare to GΩ limit. Select the lower of the two limits.

Note: When measuring capacitance it is important to ensure the set voltage level is held constant. The HP4284 and Agilent E4980 have a feature known as Automatic Level Control (ALC). The ALC feature should be switched to "ON."

Dielectric Withstanding Voltage (DWV)

EIA Case Size	500V	630V	≥ 1000V
0402	120% of rated voltage	N/A	N/A
0603	150% of rated voltage	130% of rated voltage	120% of rated voltage
0805		< 620pF 150% of rated voltage ≥ 620pF 130% of rated voltage	
1206		< 5.1nF 150% of rated voltage ≥ 5.1nF 130% of rated voltage	
1210		< 7.5nF 150% of rated voltage ≥ 7.5nF 130% of rated voltage	
1808		< 5.1nF 150% of rated voltage ≥ 5.1nF 130% of rated voltage	
1812		< 12nF 150% of rated voltage ≥ 12nF 130% of rated voltage	
1825		< 22nF 150% of rated voltage ≥ 22nF 130% of rated voltage	
2220		< 27nF 150% of rated voltage ≥ 27nF 130% of rated voltage	
±2225		< 33nF 150% of rated voltage ≥ 33nF 130% of rated voltage	

Post Environmental Limits

High Temperature Life, Biased Humidity, Moisture Resistance					
Dielectric	Rated DC Voltage	Capacitance Value	Dissipation Factor (Maximum %)	Capacitance Shift	Insulation Resistance
COG	All	All	0.5	0.3% or ±0.25 pF	10% of Initial Limit

Table 1B – Capacitance Range/Selection Waterfall (1812 – 2225 Case Sizes) cont.

Capacitance	Cap Code	Case Size/ Series		C1812C						C1825C						C2220C						C2225C									
		Voltage Code		C	B	D	F	G	Z	H	C	B	D	F	G	Z	H	C	B	D	F	G	Z	H	C	B	D	F	G	Z	H
		Rated Voltage (VDC)		500	630	1000	1500	2000	2500	3000	500	630	1000	1500	2000	2500	3000	500	630	1000	1500	2000	2500	3000	500	630	1000	1500	2000	2500	3000
		Capacitance Tolerance		Product Availability and Chip Thickness Codes See Table 2 for Chip Thickness Dimensions																											
68,000 pF	683		F	G	J	K	M								HJ	HJ											JL	JL	KF	KF	
82,000 pF	823		F	G	J	K	M								HK	HK											JL	JL	KH	KH	
0.1 µF	104		F	G	J	K	M								HK	HK											JN	JN	KH	KH	
0.12 µF	124		F	G	J	K	M																						KJ	KJ	
Capacitance	Cap Code	Rated Voltage (VDC)		500	630	1000	1500	2000	2500	3000	500	630	1000	1500	2000	2500	3000	500	630	1000	1500	2000	2500	3000	500	630	1000	1500	2000	2500	3000
		Voltage Code		C	B	D	F	G	Z	H	C	B	D	F	G	Z	H	C	B	D	F	G	Z	H	C	B	D	F	G	Z	H
		Case Size/Series		C1812C						C1825C						C2220C						C2225C									

*Capacitance range Includes E24 decade values only (i.e., 10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, and 91.)
 KEMET reserves the right to substitute product with an improved temperature characteristic, tighter capacitance tolerance and/or higher voltage capability within the same form factor (configuration and dimensions.)
 These products are protected under US Patents 7,172,985 and 7,670,981, other patents pending, and any foreign counterparts.

Table 1C – Capacitance Range/Selection Waterfall (2824 – 4540 Case Sizes)

Capacitance	Cap Code	Case Size/ Series			C2824C					C3040C					C3640C					C4540C									
		Voltage Code			C	B	D	F	G	C	B	D	F	G	C	B	D	F	G	C	B	D	F	G					
		Rated Voltage (VDC)			500	630	1000	1500	2000	500	630	1000	1500	2000	500	630	1000	1500	2000	500	630	1000	1500	2000					
		Capacitance Tolerance			Product Availability and Chip Thickness Codes See Table 2 for Chip Thickness Dimensions																								
2,200 pF	222	J	K	M	TA	TA	TA	TA	TA																				
2,700 pF	272	J	K	M	TA	TA	TA	TA	TA																				
3,300 pF	332	J	K	M	TA	TA	TA	TA	TA						QB	QB	QB	QB	QB										
3,900 pF	392	J	K	M	TA	TA	TA	TA	TB						QB	QB	QB	QB	QB	MA	MA	MA	MA	MA					
4,700 pF	472	J	K	M	TA	TA	TA	TB	TB						QB	QB	QB	QB	QB	MA	MA	MA	MA	MA	SA	SA	SA	SA	SA
5,600 pF	562	J	K	M	TA	TA	TA	TB	TC						QB	QB	QB	QB	QB	MA	MA	MA	MA	MA	SA	SA	SA	SA	SA
6,800 pF	682	J	K	M	TA	TA	TA	TB							QB	QB	QB	QB	QC	MA	MA	MA	MA	MA	SA	SA	SA	SA	SA
8,200 pF	822	J	K	M	TA	TA	TA	TB	TC						QB	QB	QB	QC	QC	MA	MA	MA	MA	MA	SA	SA	SA	SA	SA
10,000 pF	103	J	K	M	TA	TA	TA								QB	QB	QB	QC	QD	MA	MA	MA	MA	MA	SA	SA	SA	SA	SB
12,000 pF	123	J	K	M	TA	TA	TA								QB	QB	QB	QD		MA	MA	MA	MA	MA	SA	SA	SA	SA	SB
15,000 pF	153	J	K	M	TA	TA	TB								QB	QB	QB	QD		MA	MA	MA	MA	MA	SA	SA	SA	SA	SB
18,000 pF	183	J	K	M	TA	TA	TB								QB	QB	QB			MA	MA	MA	MA	MA	SA	SA	SA	SA	SB
22,000 pF	223	J	K	M	TA	TB	TC								QB	QB	QC			MA	MA	MA			SA	SA	SA	SA	SB
27,000 pF	273	J	K	M	TA	TB									QB	QB	QC			MA	MA	MA			SA	SA	SA	SA	SC
33,000 pF	333	J	K	M	TB	TB									QB	QC	QC			MA	MA	MA			SA	SA	SA		
39,000 pF	393	J	K	M	TB	TC									QB	QC	QC			MA	MA	MA	MB		SA	SA	SA	SB	
47,000 pF	473	J	K	M	TB										QB	QC				MA	MA	MA	MC		SA	SA	SA	SB	
56,000 pF	563	J	K	M	TC										QC	QC				MA	MA	MA			SA	SA	SA	SB	
68,000 pF	683	J	K	M											QC	QC				MA	MA	MA			SA	SA	SA	SB	SC
82,000 pF	823	J	K	M											QC	QC				MA	MA	MA			SA	SA	SA	SB	SC
0.1 µF	104	J	K	M											QD					MC					SB	SC			
0.12 µF	124	J	K	M																MC					SB	SC			
0.15 µF	154	J	K	M																MC					SB	SC			
Capacitance	Cap Code	Rated Voltage (VDC)			500	630	1000	1500	2000	500	630	1000	1500	2000	500	630	1000	1500	2000	500	630	1000	1500	2000					
		Voltage Code			C	B	D	F	G	C	B	D	F	G	C	B	D	F	G	C	B	D	F	G					
		Case Size/Series			C2824C					C3040C					C3640C					C4540C									

*Capacitance range Includes E24 decade values only (i.e., 10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, and 91.)
 KEMET reserves the right to substitute product with an improved temperature characteristic, tighter capacitance tolerance and/or higher voltage capability within the same form factor (configuration and dimensions.)
 These products are protected under US Patents 7,172,985 and 7,670,981, other patents pending, and any foreign counterparts.

Table 2 – Chip Thickness/Tape & Reel Packaging Quantities

Thickness Code	Case Size	Thickness ± Range (mm)	Paper Quantity		Plastic Quantity	
			7" Reel	13" Reel	7" Reel	13" Reel
BB	0402	0.50 ± 0.05	10000	50000	0	0
BD	0402	0.55 ± 0.05	10000	50000	0	0
CG	0603	0.80 ± 0.10*	4,000	15,000	0	0
DN	0805	0.78 ± 0.10*	4,000	15,000	0	0
DP	0805	0.90 ± 0.10*	4,000	15,000	0	0
DG	0805	1.25 ± 0.15	0	0	2,500	10,000
EB	1206	0.78 ± 0.10	0	0	4,000	10,000
EC	1206	0.90 ± 0.10	0	0	4,000	10,000
ED	1206	1.00 ± 0.10	0	0	2,500	10,000
EE	1206	1.10 ± 0.10	0	0	2,500	10,000
EF	1206	1.20 ± 0.15	0	0	2,500	10,000
EG	1206	1.60 ± 0.15	0	0	2,000	8,000
EH	1206	1.60 ± 0.20	0	0	2,000	8,000
FE	1210	1.00 ± 0.10	0	0	2,500	10,000
FF	1210	1.10 ± 0.10	0	0	2,500	10,000
FG	1210	1.25 ± 0.15	0	0	2,500	10,000
FL	1210	1.40 ± 0.15	0	0	2,000	8,000
FM	1210	1.70 ± 0.20	0	0	2,000	8,000
FY	1210	2.00 ± 0.20	0	0	2,000	8,000
FK	1210	2.10 ± 0.20	0	0	2,000	8,000
FS	1210	2.50 ± 0.30	0	0	1,000	4,000
LA	1808	1.40 ± 0.15	0	0	1,000	4,000
LB	1808	1.60 ± 0.15	0	0	1,000	4,000
LC	1808	2.00 ± 0.15	0	0	1,000	4,000
Thickness Code	Case Size	Thickness ± Range (mm)	7" Reel	13" Reel	7" Reel	13" Reel
			Paper Quantity		Plastic Quantity	

Package quantity based on finished chip thickness specifications.

Table 2 – Chip Thickness/Tape & Reel Packaging Quantities cont.

Thickness Code	Case Size	Thickness ± Range (mm)	Paper Quantity		Plastic Quantity	
			7" Reel	13" Reel	7" Reel	13" Reel
GB	1812	1.00 ± 0.10	0	0	1,000	4,000
GD	1812	1.25 ± 0.15	0	0	1,000	4,000
GH	1812	1.40 ± 0.15	0	0	1,000	4,000
GK	1812	1.60 ± 0.20	0	0	1,000	4,000
GM	1812	2.00 ± 0.20	0	0	500	2,000
GO	1812	2.50 ± 0.20	0	0	500	2,000
HE	1825	1.40 ± 0.15	0	0	1,000	4,000
HG	1825	1.60 ± 0.20	0	0	1,000	4,000
HJ	1825	2.00 ± 0.20	0	0	500	2,000
HK	1825	2.50 ± 0.20	0	0	500	2,000
JE	2220	1.40 ± 0.15	0	0	1,000	4,000
JK	2220	1.60 ± 0.20	0	0	1,000	4,000
JL	2220	2.00 ± 0.20	0	0	500	2,000
JN	2220	2.50 ± 0.20	0	0	500	2,000
KE	2225	1.40 ± 0.15	0	0	1,000	4,000
KF	2225	1.60 ± 0.20	0	0	1,000	4,000
KH	2225	2.00 ± 0.20	0	0	500	2,000
KJ	2225	2.50 ± 0.20	0	0	500	2,000
TA	2824	1.40 ± 0.15	0	0	750	1,500
TB	2824	2.00 ± 0.20	0	0	300	1,500
TC	2824	2.50 ± 0.20	0	0	300	1,500
QB	3040	1.40 ± 0.15	0	0	500	1,000
QC	3040	2.00 ± 0.20	0	0	500	1,000
QD	3040	2.50 ± 0.20	0	0	350	1,000
MA	3640	1.40 ± 0.15	0	0	250	1,000
MB	3640	2.00 ± 0.20	0	0	250	1,000
MC	3640	2.50 ± 0.20	0	0	250	1,000
SA	4540	1.40 ± 0.15	0	0	200	1,000
SB	4540	2.00 ± 0.20	0	0	200	1,000
SC	4540	2.50 ± 0.20	0	0	200	1,000
Thickness Code	Case Size	Thickness ± Range (mm)	7" Reel	13" Reel	7" Reel	13" Reel
			Paper Quantity		Plastic Quantity	

Package quantity based on finished chip thickness specifications.

Table 3 – Chip Capacitor Land Pattern Design Recommendations per IPC–7351

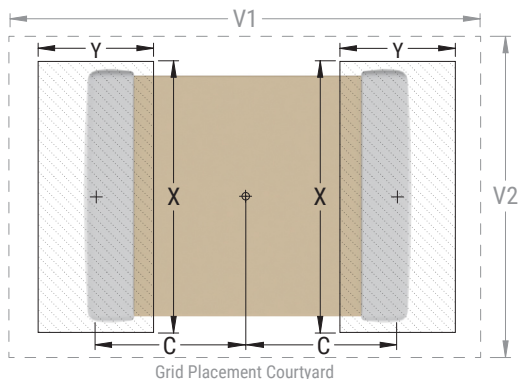
EIA Size Code	Metric Size Code	Density Level A: Maximum (Most) Land Protrusion (mm)					Density Level B: Median (Nominal) Land Protrusion (mm)					Density Level C: Minimum (Least) Land Protrusion (mm)				
		C	Y	X	V1	V2	C	Y	X	V1	V2	C	Y	X	V1	V2
0402	1005	0.50	0.72	0.72	2.20	1.20	0.45	0.62	0.62	1.90	1.00	0.40	0.52	0.52	1.60	0.80
0603	1608	0.90	1.15	1.10	4.00	2.10	0.80	0.95	1.00	3.10	1.50	0.60	0.75	0.90	2.40	1.20
0805	2012	1.00	1.35	1.55	4.40	2.60	0.90	1.15	1.45	3.50	2.00	0.75	0.95	1.35	2.80	1.70
1206	3216	1.60	1.35	1.90	5.60	2.90	1.50	1.15	1.80	4.70	2.30	1.40	0.95	1.70	4.00	2.00
1210	3225	1.60	1.35	2.80	5.65	3.80	1.50	1.15	2.70	4.70	3.20	1.40	0.95	2.60	4.00	2.90
1808	4520	2.30	1.75	2.30	7.40	3.30	2.20	1.55	2.20	6.50	2.70	2.10	1.35	2.10	5.80	2.40
1812	4532	2.15	1.60	3.60	6.90	4.60	2.05	1.40	3.50	6.00	4.00	1.95	1.20	3.40	5.30	3.70
1825	4564	2.15	1.60	6.90	6.90	7.90	2.05	1.40	6.80	6.00	7.30	1.95	1.20	6.70	5.30	7.00
2220	5650	2.75	1.70	5.50	8.20	6.50	2.65	1.50	5.40	7.30	5.90	2.55	1.30	5.30	6.60	5.60
2225	5664	2.70	1.70	6.90	8.10	7.90	2.60	1.50	6.80	7.20	7.30	2.50	1.30	6.70	6.50	7.00
2824	7260	3.45	1.70	6.60	9.60	7.60	3.35	1.50	6.50	8.70	7.00	3.25	1.30	6.40	8.00	6.70
3040	7610	3.70	1.70	10.70	10.10	11.70	3.60	1.50	10.60	9.20	11.10	3.50	1.30	10.50	8.50	10.80
3640	9210	4.45	1.70	10.70	11.60	11.70	4.35	1.50	10.60	10.70	11.10	4.25	1.30	10.50	10.00	10.80
4540	-	5.60	1.70	10.70	13.90	11.70	5.50	1.50	10.60	13.00	11.10	5.40	1.30	10.50	12.30	10.80

Density Level A: For low-density product applications. Recommended for wave solder applications and provides a wider process window for reflow solder processes. KEMET only recommends wave soldering of EIA 0603, 0805 and 1206 case sizes.

Density Level B: For products with a moderate level of component density. Provides a robust solder attachment condition for reflow solder processes.

Density Level C: For high component density product applications. Before adapting the minimum land pattern variations the user should perform qualification testing based on the conditions outlined in IPC Standard 7351 (IPC–7351).

Image below based on Density Level B for an EIA 1210 case size.



Soldering Process

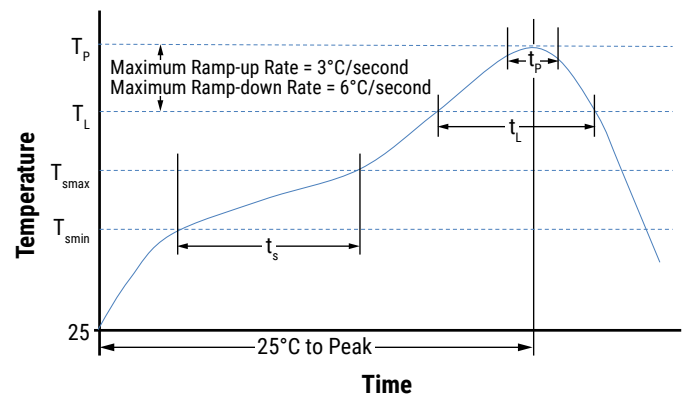
Recommended Soldering Technique:

- Solder wave or solder reflow for EIA case sizes 0603, 0805 and 1206
- All other EIA case sizes are limited to solder reflow only

Recommended Reflow Soldering Profile:

KEMET's families of surface mount multilayer ceramic capacitors (SMD MLCCs) are compatible with wave (single or dual), convection, IR or vapor phase reflow techniques. Preheating of these components is recommended to avoid extreme thermal stress. KEMET's recommended profile conditions for convection and IR reflow reflect the profile conditions of the IPC/J-STD-020 standard for moisture sensitivity testing. These devices can safely withstand a maximum of three reflow passes at these conditions.

Profile Feature	Termination Finish	
	SnPb	100% Matte Sn
Preheat/Soak		
Temperature Minimum (T_{Smin})	100°C	150°C
Temperature Maximum (T_{Smax})	150°C	200°C
Time (t_s) from T_{Smin} to T_{Smax}	60 – 120 seconds	60 – 120 seconds
Ramp-Up Rate (T_L to T_p)	3°C/second maximum	3°C/second maximum
Liquidous Temperature (T^l)	183°C	217°C
Time Above Liquidous (t^l)	60 – 150 seconds	60 – 150 seconds
Peak Temperature (T_p)	235°C	260°C
Time Within 5°C of Maximum Peak Temperature (t_p)	20 seconds maximum	30 seconds maximum
Ramp-Down Rate (T_p to T_L)	6°C/second maximum	6°C/second maximum
Time 25°C to Peak Temperature	6 minutes maximum	8 minutes maximum

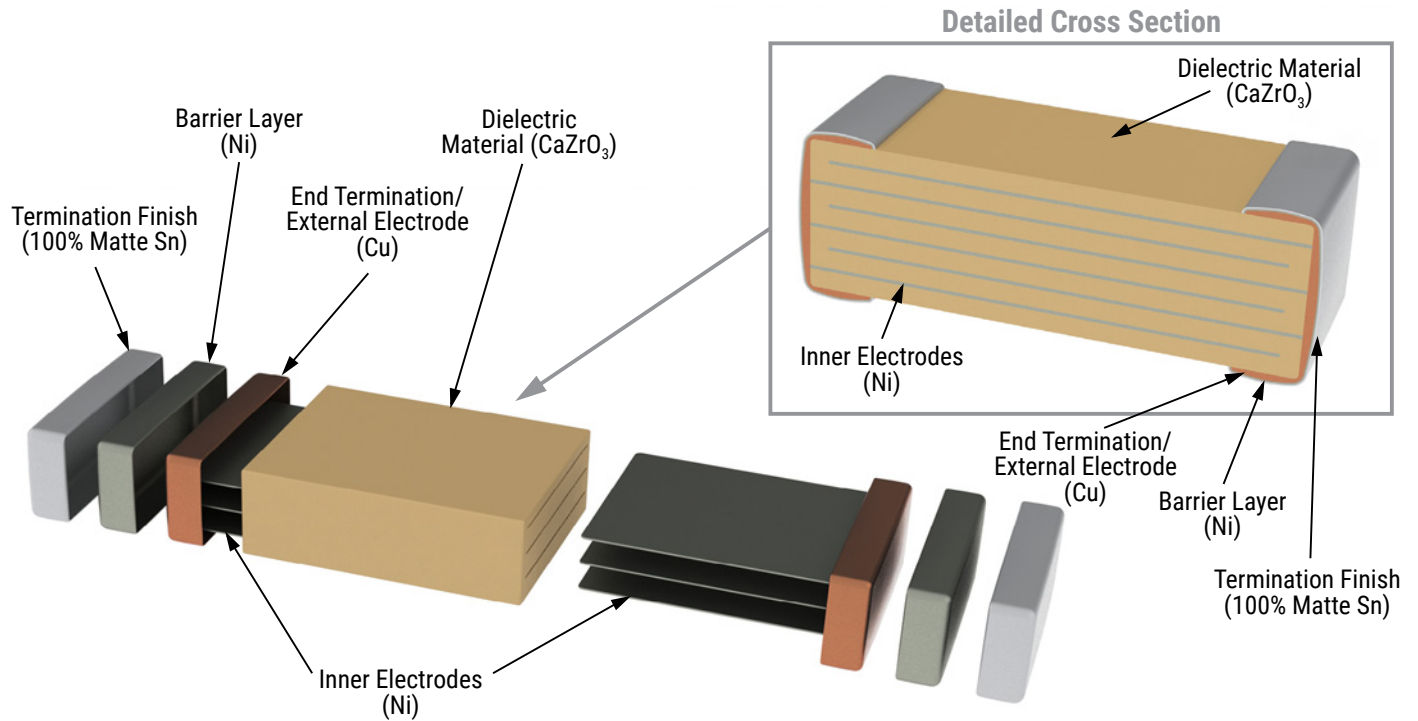


Note 1: All temperatures refer to the center of the package, measured on the capacitor body surface that is facing up during assembly reflow.

Storage and Handling

Ceramic chip capacitors should be stored in normal working environments. While the chips themselves are quite robust in other environments, solderability will be degraded by exposure to high temperatures, high humidity, corrosive atmospheres, and long term storage. In addition, packaging materials will be degraded by high temperature—reels may soften or warp and tape peel force may increase. KEMET recommends that maximum storage temperature not exceed 40°C and maximum storage humidity not exceed 70% relative humidity. Temperature fluctuations should be minimized to avoid condensation on the parts and atmospheres should be free of chlorine and sulfur bearing compounds. For optimized solderability chip stock should be used promptly, preferably within 1.5 years of receipt.

Construction



Capacitor Marking (Optional):

Laser marking option is not available on:

- COG, Ultra Stable X8R and Y5V dielectric devices
- EIA 0402 case size devices
- EIA 0603 case size devices with Flexible Termination option.
- KPS Commercial and Automotive grade stacked devices.

These capacitors are supplied unmarked only.

Tape & Reel Packaging Information

KEMET offers multilayer ceramic chip capacitors packaged in 8, 12, 16 and 24 mm tape on 7" and 13" reels in accordance with EIA Standard 481. This packaging system is compatible with all tape-fed automatic pick and place systems. See Table 2 for details on reeling quantities for commercial chips.

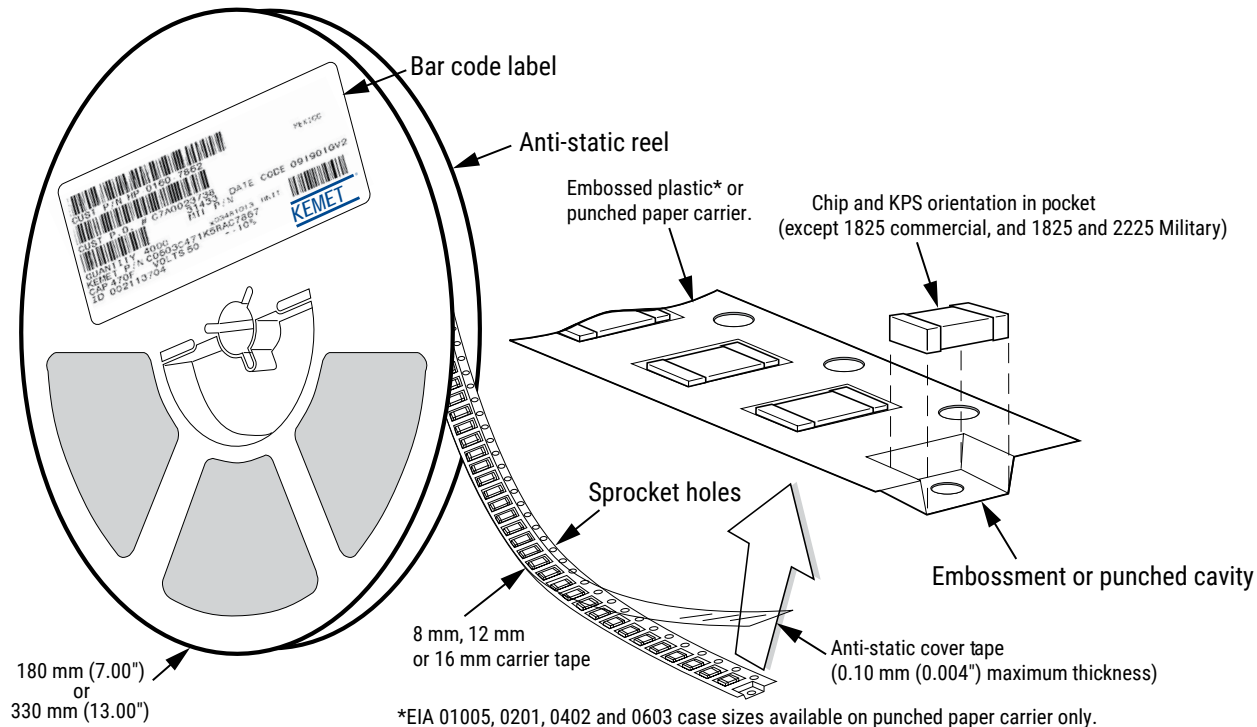


Table 5 – Carrier Tape Configuration, Embossed Plastic & Punched Paper (mm)

EIA Case Size	Tape Size (W)*	Embossed Plastic		Punched Paper	
		7" Reel	13" Reel	7" Reel	13" Reel
		Pitch (P ₁)*		Pitch (P ₁)*	
01005 – 0402	8			2	2
0603	8			4	4
0805	8	4	4	4	4
1206 – 1210	8	4	4	4	4
1805 – 1808	12	4	4		
≥ 1812	12	8	8		
2824	16	12	12		
3040 – 4540	24	16	16		
KPS 1210	12	8	8		
KPS 1812 & 2220	16	12	12		
Array 0508 & 0612	8	4	4		

*Refer to Figures 1 and 2 for W and P₁ carrier tape reference locations.

*Refer to Tables 6 and 7 for tolerance specifications.

Figure 1 – Embossed (Plastic) Carrier Tape Dimensions

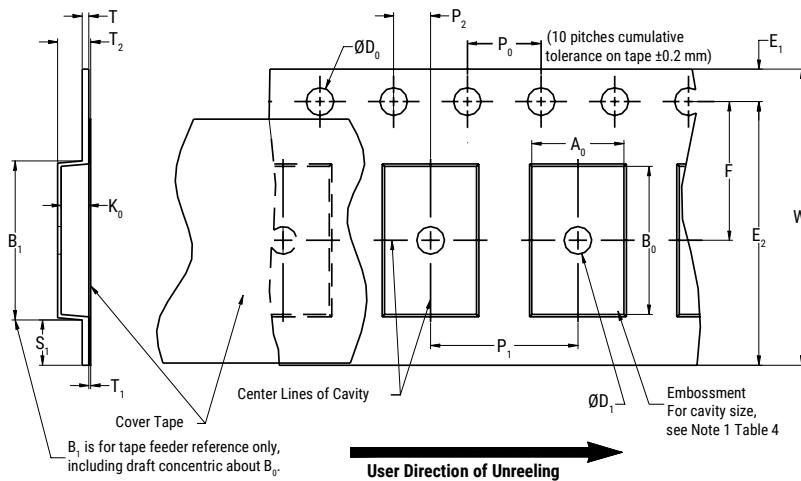


Table 6 – Embossed (Plastic) Carrier Tape Dimensions

Metric will govern

Constant Dimensions – Millimeters (Inches)								
Tape Size	D ₀	E ₁	P ₀	P ₂	R Reference Note 2	S ₁ Minimum Note 3	T Maximum	T1 Maximum
8 mm	1.5+0.10/-0.0 (0.059+0.004/-0.0)	1.75±0.10 (0.069±0.004)	4.0±0.10 (0.157±0.004)	2.0±0.05 (0.079±0.002)	25.0 (0.984)	0.600 (0.024)	0.600 (0.024)	0.100 (0.004)
12 mm					30 (1.181)			
16 mm								
24 mm	1.5+0.10/-0.0 (0.059+0.004/-0.0)	1.75±0.10 (0.069±0.004)	4.0±0.10 (0.157±0.004)	2.0±0.10 (0.078±0.003)	30 (1.181)	5 (0.196)	0.250 (0.009)	0.350 (0.013)
Variable Dimensions – Millimeters (Inches)								
Tape Size	Pitch	E ₂ Minimum	F	P ₁	T ₂ Maximum	W Maximum	A ₀ , B ₀ & K ₀	
8 mm	Single (4 mm)	6.25 (0.246)	3.5±0.05 (0.138±0.002)	4.0±0.10 (0.157±0.004)	2.5 (0.098)	8.3 (0.327)	Note 5	
12 mm	Single (4 mm) & Double (8 mm)	10.25 (0.404)	5.5±0.05 (0.217±0.002)	8.0±0.10 (0.315±0.004)	4.6 (0.181)	12.3 (0.484)		
16 mm	Triple (12 mm)	14.25 (0.561)	7.5±0.05 (0.138±0.002)	12.0±0.10 (0.157±0.004)	4.6 (0.181)	16.3 (0.642)		
24 mm	16 mm	22.25 (0.875)	11.5±0.10 (0.452±0.003)	16.0±0.10 (0.629±0.004)	3 (0.118)	24.3 (0.956)		

- The embossment hole location shall be measured from the sprocket hole controlling the location of the embossment. Dimensions of embossment location and hole location shall be applied independent of each other.
- The tape with or without components shall pass around R without damage (see Figure 6).
- If S₁ < 1.0 mm, there may not be enough area for cover tape to be properly applied (see EIA Standard 481 paragraph 4.3 section b).
- B₁ dimension is a reference dimension for tape feeder clearance only.
- The cavity defined by A₀, B₀ and K₀ shall surround the component with sufficient clearance that:
 - the component does not protrude above the top surface of the carrier tape.
 - the component can be removed from the cavity in a vertical direction without mechanical restriction, after the top cover tape has been removed.
 - rotation of the component is limited to 20° maximum for 8 and 12 mm tapes and 10° maximum for 16 mm tapes (see Figure 3).
 - lateral movement of the component is restricted to 0.5 mm maximum for 8 and 12 mm wide tape and to 1.0 mm maximum for 16 mm tape (see Figure 4).
 - for KPS Series product, A₀ and B₀ are measured on a plane 0.3 mm above the bottom of the pocket.
 - see Addendum in EIA Standard 481 for standards relating to more precise taping requirements.

Figure 2 – Punched (Paper) Carrier Tape Dimensions

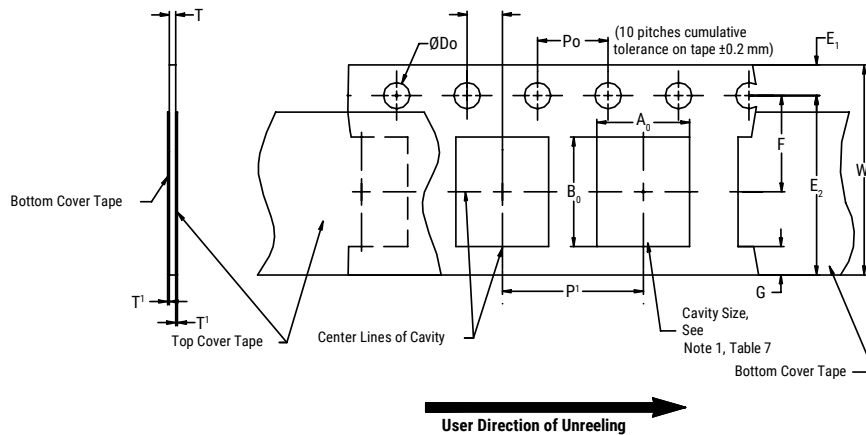


Table 7 – Punched (Paper) Carrier Tape Dimensions

Metric will govern

Constant Dimensions – Millimeters (Inches)							
Tape Size	D_0	E_1	P_0	P_2	T_1 Maximum	G Minimum	R Reference Note 2
8 mm	1.5+0.10/-0.0 (0.059+0.004/-0.0)	1.75±0.10 (0.069±0.004)	4.0±0.10 (0.157±0.004)	2.0±0.05 (0.079±0.002)	0.10 (0.004) Maximum	0.75 (0.030)	2 (0.984)
Variable Dimensions – Millimeters (Inches)							
Tape Size	Pitch	E2 Minimum	F	P_1	T Maximum	W Maximum	$A_0 B_0$
8 mm	Half (2 mm)	6.25 (0.246)	3.5±0.05 (0.138±0.002)	2.0±0.05 (0.079±0.002)	1.1 (0.043)	8.3 (0.327)	Note 1
8 mm	Single (4 mm)			4.0±0.10 (0.157±0.004)			

- The cavity defined by A_0 , B_0 and T shall surround the component with sufficient clearance that:
 - the component does not protrude beyond either surface of the carrier tape.
 - the component can be removed from the cavity in a vertical direction without mechanical restriction, after the top cover tape has been removed.
 - rotation of the component is limited to 20° maximum (see Figure 3).
 - lateral movement of the component is restricted to 0.5 mm maximum (see Figure 4).
 - see Addendum in EIA Standard 481 for standards relating to more precise taping requirements.
- The tape with or without components shall pass around R without damage (see Figure 6).

Packaging Information Performance Notes

- Cover Tape Break Force:** 1.0 Kg minimum.
- Cover Tape Peel Strength:** The total peel strength of the cover tape from the carrier tape shall be:

Tape Width	Peel Strength
8 mm	0.1 to 1.0 newton (10 to 100 gf)
12 and 16 mm	0.1 to 1.3 newton (10 to 130 gf)
24 mm	0.1 to 1.6 newton (10 to 160 gf)

The direction of the pull shall be opposite the direction of the carrier tape travel. The pull angle of the carrier tape shall be 165° to 180° from the plane of the carrier tape. During peeling, the carrier and/or cover tape shall be pulled at a velocity of 300 ±10 mm/minute.

- Labeling:** Bar code labeling (standard or custom) shall be on the side of the reel opposite the sprocket holes. Refer to EIA Standards 556 and 624.

Figure 3 – Maximum Component Rotation

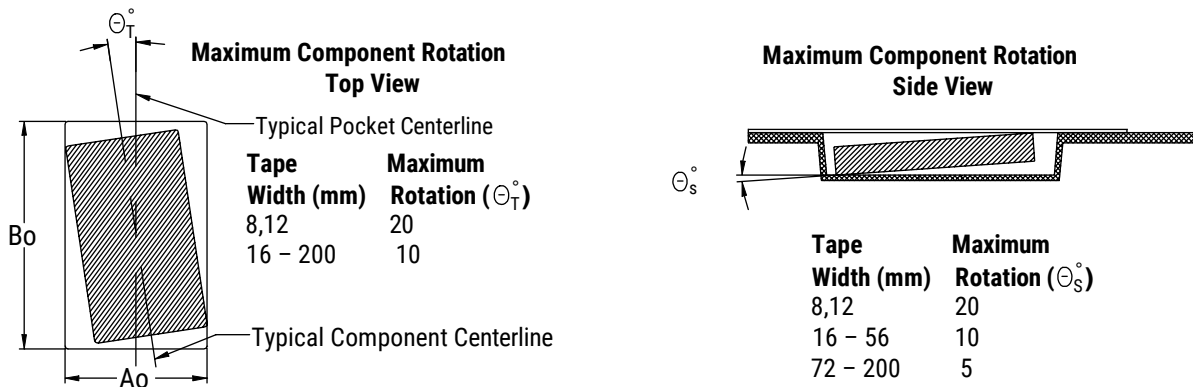


Figure 4 – Maximum Lateral Movement

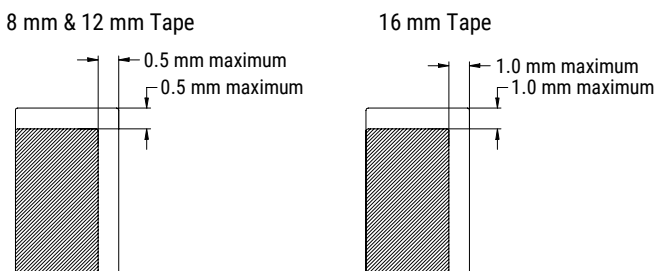


Figure 5 – Bending Radius

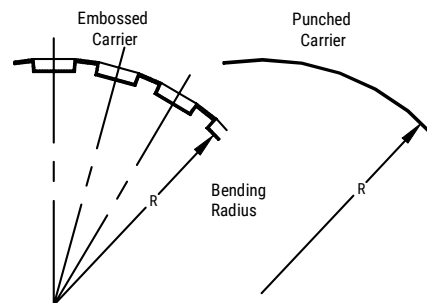


Figure 6 – Reel Dimensions



Table 8 – Reel Dimensions

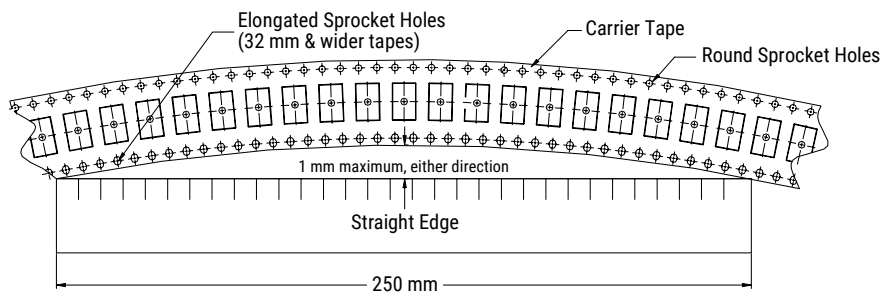
Metric will govern

Constant Dimensions – Millimeters (Inches)				
Tape Size	A	B Minimum	C	D Minimum
8 mm	178±0.20 (7.008±0.008) or 330±0.20 (13.000±0.008)	1.5 (0.059)	13.0+0.5/-0.2 (0.521+0.02/-0.008)	20.2 (0.795)
12 mm				
16 mm				
24 mm		1.2 (0.047)	13.0 + -0.2 (0.521 + -0.008)	21 (0.826)
Variable Dimensions – Millimeters (Inches)				
Tape Size	N Minimum	W ₁	W ₂ Maximum	W ₃
8 mm	50 (1.969)	8.4+1.5/-0.0 (0.331+0.059/-0.0)	14.4 (0.567)	Shall accommodate tape width without interference
12 mm		12.4+2.0/-0.0 (0.488+0.078/-0.0)	18.4 (0.724)	
16 mm		16.4+2.0/-0.0 (0.646+0.078/-0.0)	22.4 (0.882)	
24 mm		25+1.0/-0.0 (0.984+0.039/-0.0)	27.4+1.0/-1.0 (1.078+0.039/-0.039)	

Figure 7 – Tape Leader & Trailer Dimensions



Figure 8 – Maximum Camber



Application Guide

Solder Fluxes and Cleaning

The use of water-soluble fluxes provides advantages of excellent solderability due to high activation. However, these fluxes contain organic acids that can induce arcing under high DC or AC voltages. Notable problem areas are underneath the MLCC where flux can be trapped between the ceramic material and PCB. It is therefore critical that PCBs are properly cleaned to remove all flux residue to maintain reliability.

Coating for High Voltage MLCCs

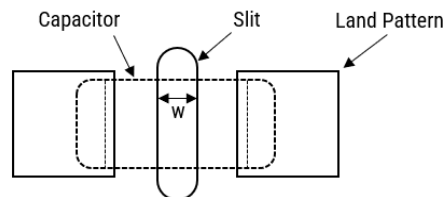
For MLCC ratings $\geq 1500V$, it is recommended to apply a conformal coating to MLCC to prevent surface arcing. To reduce possibility of inducing cracks in the MLCC, select a coating with thermal expansions close to that of the MLCC.

Dielectric	CTE (ppm/°C)
Class II BaTiO ₃	10.7
Class I CaZrO ₃	9.8

Slits in PCB

It is recommended to apply a slit in the PCB under the MLCC to improve washing of flux residue that may get trapped underneath. In some cases, it is not possible to slit entirely through the PCB due to underlying metal planes. It is also acceptable to apply a recessed slit under the MLCC which will also promote cleaning.

- Recommended for case sizes ≥ 1206
- The width (w) of the slit should be 1mm
- Length of the slit should be as short as possible to prevent damaging the MLCC due to mechanical stress of the PCB.
- Slits also reduce the risk of solder balls under MLCC which decreased the creepage distance.



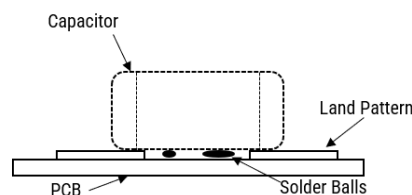
Solder Resist

If a slit cannot be applied as above, it is recommended to not use solder resist directly under the MLCC. The use of solder resist material reduces the distance between MLCC ceramic material and PCB thus making it difficult to clean.

Solder Balls

Improper reflow techniques and/or improper washing can induce solder balls under or adjacent to the MLCC. Solder balls reduce the creepage distance between the MLCC terminations and increase the risk of arcing or damage to the ceramic material. To reduce the risk of solder balls:

- Follow KEMET's solder recommendations as outlined in the datasheet.
- If performing a cleaning procedure, properly clean the PCB per KEMET's cleaning recommendations.
- Add slit to the PCB as shown above.



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