



# THE DATASHEET OF

## 36900000

## Dual Channel, 16-Bit, 33 MUPS, Multispan, Multi-IO SPI DAC

### FEATURES

- ▶ 16-bit resolution
- ▶ 33 MUPS rate in fast mode
- ▶ 22 MUPS rate in precision mode
- ▶ 65 ns small signal settling time to 0.1% accuracy
- ▶ 100 ns large signal settling time to 0.1% accuracy
- ▶ Ultra small glitch: < 50 pV×s
- ▶ Ultra low latency: 5 ns
- ▶ THD: -105 dB at 1 kHz
- ▶ Highly configurable output voltage span and offset
- ▶ 1.2 V and 1.8 V logic level compatible
- ▶ Single (classic), dual, and quad SPI modes
- ▶ Multiple error detectors, both analog and digital domains
- ▶ 2.5 V internal voltage reference, 10 ppm/°C maximum temperature coefficient
- ▶ 5 mm × 5 mm LFCSP

### APPLICATIONS

- ▶ Instrumentation
- ▶ Hardware in the loop
- ▶ Process control equipment
- ▶ Medical devices
- ▶ Automated test equipment
- ▶ Data acquisition system
- ▶ Programmable voltage sources
- ▶ Optical communications

### FUNCTIONAL BLOCK DIAGRAM

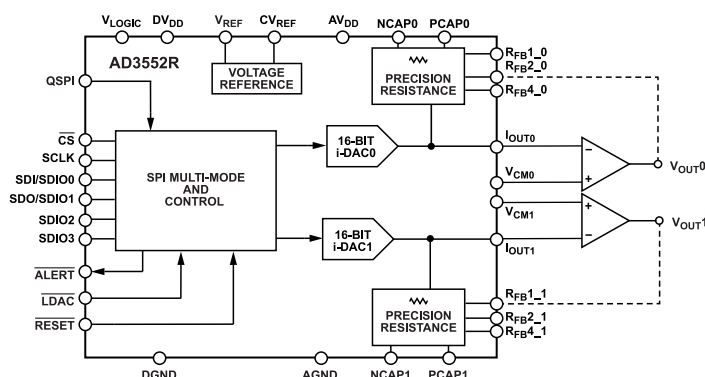


Figure 1.

### GENERAL DESCRIPTION

The AD3552R is a low drift, dual channel, ultra-fast, 16-bit accuracy, current output digital-to-analog converter (DAC) that can be configured in multiple voltage span ranges. The AD3552R operates with a fixed 2.5 V reference.

Each DAC incorporates three drift compensating feedback resistors for the required external transimpedance amplifier (TIA) that scales the output voltage. Offset and gain scaling registers allow for generation of multiple output span ranges, such as 0 V to 2.5 V, 0 V to 5 V, 0 V to 10 V, -5 V to +5 V, and -10 V to +10 V, and custom intermediate ranges with full 16-bit resolution.

The DAC can operate in fast mode for maximum speed or precision mode for maximum accuracy.

The serial peripheral interface (SPI) can be configured in quad SPI mode, dual synchronous SPI mode, dual SPI mode, and single SPI (classic SPI) mode with single data rate (SDR) or double data rate (DDR), with logical levels from 1.2 V to 1.8 V.

The AD3552R is specified over the extended industrial temperature range (-40°C to +105°C).

Table 1. Related Devices

| Part No.                  | Description                                                          |
|---------------------------|----------------------------------------------------------------------|
| <a href="#">AD8675</a>    | 36 V precision, 2.8 nV/√Hz rail-to-rail output operational amplifier |
| <a href="#">AD8065</a>    | High performance, 145 MHz <i>FastFET™</i> operational amplifiers     |
| <a href="#">ADA4807-1</a> | 3.1 nV/√Hz, 1 mA, 180 MHz, rail-to-rail input/output amplifier       |
| <a href="#">LTC6655</a>   | 0.25 ppm noise, low drift precision reference                        |
| <a href="#">ADR4525</a>   | Ultralow noise, high accuracy, 2.5 V voltage reference               |

Analog Devices is in the process of updating documentation to provide terminology and language that is culturally appropriate. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

Rev. B

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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## REVISION HISTORY

**2/2023—Rev. A to Rev. B**

|                                                                                                                                                                |    |
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| Changed 16-Bit, 33 MUPS, Multispan, Multi-IO SPI DAC to Dual Channel, 16-Bit, 33 MUPS, Multispan, Multi-IO SPI DAC.....                                        | 1  |
| Changed DVDD to DV <sub>DD</sub> , IOVDD to V <sub>LOGIC</sub> , VREF to V <sub>REF</sub> , AVDD to AV <sub>DD</sub> , VDD to AV <sub>DD</sub> (Throughout)... | 1  |
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**1/2022—Revision 0: Initial Version**

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$AV_{DD} = 5.0\text{ V} \pm 5\%$ ,  $DV_{DD} = 1.8\text{ V} \pm 5\%$ ,  $1.1\text{ V} \leq V_{\text{LOGIC}} \leq 1.9\text{ V}$ ,  $V_{\text{REF}} = 2.5\text{ V}$ ,  $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ , output amplifier [AD8675](#), unless otherwise noted.

Table 2.

| Parameter <sup>1</sup>                                      | Symbol            | Min                            | Typ     | Max                            | Unit                         | Test Conditions/Comments                                                                                                    |
|-------------------------------------------------------------|-------------------|--------------------------------|---------|--------------------------------|------------------------------|-----------------------------------------------------------------------------------------------------------------------------|
| STATIC PERFORMANCE                                          |                   |                                |         |                                |                              |                                                                                                                             |
| Resolution                                                  |                   | 16                             |         |                                | Bits                         |                                                                                                                             |
| Relative Accuracy (INL)                                     |                   | -2                             |         | +2                             | LSB                          | 5 V range only                                                                                                              |
|                                                             |                   | -4                             |         | +4                             | LSB                          | All other ranges <sup>2</sup>                                                                                               |
| Differential Nonlinearity (DNL)                             |                   | -1                             |         | +1                             | LSB                          | Precision mode: $-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$ ,<br>fast mode: $0^{\circ}\text{C}$ to $85^{\circ}\text{C}$ |
|                                                             |                   | -2                             |         | +2                             | LSB                          | Fast mode: $-40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$                                                                  |
|                                                             |                   | -2                             |         | +2                             | LSB                          | 0 V to 2.5 V range, fast or precision modes <sup>2</sup>                                                                    |
| Offset Error                                                |                   |                                | 0.03    |                                | %FSR                         | Midscale, $25^{\circ}\text{C}$                                                                                              |
| Offset Error Drift <sup>2</sup>                             |                   |                                | 2       | 8                              | ppm FSR/ $^{\circ}\text{C}$  | 0 V to 5 V and 0 V to 10 V ranges                                                                                           |
|                                                             |                   |                                | 4       | 16                             | ppm FSR/ $^{\circ}\text{C}$  | All other ranges                                                                                                            |
| Full-Scale Error                                            |                   |                                | 0.04    |                                | %FSR                         | $25^{\circ}\text{C}$                                                                                                        |
| Full-Scale Error Drift <sup>2</sup>                         |                   |                                | 1       | 5                              | ppm FSR/ $^{\circ}\text{C}$  | 0 V to 5 V and 0 V to 10 V ranges                                                                                           |
|                                                             |                   |                                | 4       | 12                             | ppm FSR/ $^{\circ}\text{C}$  | All other ranges                                                                                                            |
| Zero-Scale Error <sup>3</sup>                               |                   |                                | 0.05    |                                | %FSR                         | $25^{\circ}\text{C}$                                                                                                        |
| Zero-Scale Error Drift <sup>2</sup>                         |                   |                                | 3.5     | 8                              | ppm FSR/ $^{\circ}\text{C}$  | 0 V to 5 V and 0 V to 10 V ranges                                                                                           |
|                                                             |                   |                                | 7       | 16                             | ppm FSR/ $^{\circ}\text{C}$  | All other ranges                                                                                                            |
| Total Unadjusted Error (TUE)                                |                   | -0.5                           |         | +0.5                           | %FSR                         |                                                                                                                             |
| DC Power Supply Rejection Ratio (PSRR)                      |                   |                                | 0.6     |                                | mV/V                         | DAC code = midscale                                                                                                         |
| DC Crosstalk                                                |                   |                                | 3       |                                | $\mu\text{V/V}$              | Full-scale step                                                                                                             |
| OUTPUT CHARACTERISTICS                                      |                   |                                |         |                                |                              |                                                                                                                             |
| Output Current                                              | $I_{\text{OUTX}}$ |                                | 1.6     |                                | mA                           | Absolute value                                                                                                              |
| REFERENCE OUTPUT                                            |                   |                                |         |                                |                              |                                                                                                                             |
| Output Voltage                                              |                   | 2.492                          | 2.5     | 2.508                          | V                            | At $25^{\circ}\text{C}$ , over lifetime                                                                                     |
| Voltage Reference Temperature Coefficient (TC) <sup>4</sup> |                   |                                | 3       | 10                             | ppm/ $^{\circ}\text{C}$      |                                                                                                                             |
| Output Impedance                                            |                   |                                | 50      |                                | m $\Omega$                   |                                                                                                                             |
| Output Voltage Noise                                        |                   |                                | 2.7     |                                | $\mu\text{V rms}$            | 0.1 Hz to 10 Hz                                                                                                             |
| Output Voltage Noise Density                                |                   |                                | 173     |                                | $\text{nV}/\sqrt{\text{Hz}}$ | $f = 1\text{ kHz}$ , no load on $V_{\text{REF}}$                                                                            |
|                                                             |                   |                                | 164     |                                | $\text{nV}/\sqrt{\text{Hz}}$ | $f = 10\text{ kHz}$ , no load on $V_{\text{REF}}$                                                                           |
| Capacitive Load Stability <sup>2</sup>                      |                   |                                |         | 10                             | $\mu\text{F}$                |                                                                                                                             |
| Load Regulation                                             |                   |                                | 50      |                                | $\mu\text{V}/\text{mA}$      | At $25^{\circ}\text{C}$                                                                                                     |
| Output Current Load Capability                              |                   |                                | $\pm 8$ |                                | mA                           |                                                                                                                             |
| Line Regulation                                             |                   |                                | 135     |                                | $\mu\text{V/V}$              | At $25^{\circ}\text{C}$                                                                                                     |
| REFERENCE INPUT                                             |                   |                                |         |                                |                              |                                                                                                                             |
| Reference Current                                           |                   |                                | 1       |                                | $\mu\text{A}$                |                                                                                                                             |
| Reference Input Range <sup>2</sup>                          | $V_{\text{REF}}$  | 2.4                            | 2.5     | 2.6                            | V                            |                                                                                                                             |
| Reference Input Impedance                                   |                   |                                | 3       |                                | M $\Omega$                   |                                                                                                                             |
| LOGIC INPUTS                                                |                   |                                |         |                                |                              |                                                                                                                             |
| Input Current                                               | $I_{\text{I}}$    | -1                             |         | +1                             | $\mu\text{A}$                | Per pin                                                                                                                     |
| Input Low Voltage                                           | $V_{\text{IL}}$   |                                |         | $0.35 \times V_{\text{LOGIC}}$ | V                            |                                                                                                                             |
| Input High Voltage                                          | $V_{\text{IH}}$   | $0.65 \times V_{\text{LOGIC}}$ |         |                                | V                            |                                                                                                                             |

## SPECIFICATIONS

Table 2. (Continued)

| Parameter <sup>1</sup>              | Symbol                     | Min                       | Typ | Max                       | Unit | Test Conditions/Comments                                                                                              |
|-------------------------------------|----------------------------|---------------------------|-----|---------------------------|------|-----------------------------------------------------------------------------------------------------------------------|
| Pin Capacitance                     | C <sub>I</sub>             |                           | 4   |                           | pF   |                                                                                                                       |
| LOGIC OUTPUTS                       |                            |                           |     |                           |      |                                                                                                                       |
| Output Low Voltage                  | V <sub>OL</sub>            |                           |     | 0.20 × V <sub>LOGIC</sub> | V    | I <sub>SINK</sub> = 100 μA                                                                                            |
| Output High Voltage                 | V <sub>OH</sub>            | 0.80 × V <sub>LOGIC</sub> |     |                           | V    | I <sub>SOURCE</sub> = 100 μA                                                                                          |
| Pin Capacitance                     | C <sub>O</sub>             |                           | 4   |                           | pF   |                                                                                                                       |
| POWER REQUIREMENTS                  |                            |                           |     |                           |      |                                                                                                                       |
| V <sub>LOGIC</sub> Pin              |                            | 1.1                       | 1.8 | 1.89                      | V    |                                                                                                                       |
| V <sub>LOGIC</sub> Current          | I <sub>LOGIC</sub>         |                           | 1   | 7.5                       | μA   | V <sub>IH</sub> = V <sub>LOGIC</sub> × 0.9, V <sub>IL</sub> = V <sub>LOGIC</sub> × 0.1                                |
| V <sub>LOGIC</sub> Dynamic Current  | I <sub>LOGIC_DYNAMIC</sub> |                           | 3   | 5                         | mA   | SCLK = 66 MHz, quad SPI DDR, V <sub>IH</sub> = V <sub>LOGIC</sub> × 0.65, V <sub>IL</sub> = V <sub>LOGIC</sub> × 0.35 |
| DV <sub>DD</sub> Pin                |                            | 1.71                      | 1.8 | 1.89                      | V    |                                                                                                                       |
| DV <sub>DD</sub> Current            | I <sub>DVDD</sub>          |                           | 0.5 | 0.8                       | mA   |                                                                                                                       |
| DV <sub>DD</sub> Dynamic Current    | I <sub>DVDD_DYNAMIC</sub>  |                           | 53  | 60                        | mA   | SCLK = 66 MHz, quad SPI DDR, simultaneous update                                                                      |
| AV <sub>DD</sub> Pin                |                            | 4.75                      | 5   | 5.25                      | V    |                                                                                                                       |
| AV <sub>DD</sub> Current            | I <sub>DD</sub>            |                           | 22  | 28.5                      | mA   | Channel 0 and Channel 1 zero-scale, 0 V to ±5 V range                                                                 |
| AV <sub>DD</sub> Power-Down Current | I <sub>DD</sub>            |                           | 0.6 |                           | mA   | After reset, DACs powered down                                                                                        |
| AV <sub>DD</sub> Reset Current      | I <sub>DD</sub>            |                           | 120 |                           | μA   | RESET asserted                                                                                                        |

<sup>1</sup> See the [Terminology](#) section.

<sup>2</sup> Guaranteed by design and characterization, not production tested.

<sup>3</sup> Measured at zero code.

<sup>4</sup> Reference temperature coefficient is calculated as per the box method.

## AC CHARACTERISTICS

AV<sub>DD</sub> = 5.0 V ± 5%, DV<sub>DD</sub> = 1.8 V ± 5%, 1.1 V ≤ V<sub>LOGIC</sub> ≤ 1.9 V, -40°C ≤ T<sub>A</sub> ≤ +105°C, measured with the [ADA4807-1](#) external amplifier, unless otherwise noted.

Table 3.

| Parameter <sup>1</sup>           | Min | Typ | Max | Unit   | Test Conditions/Comments                                                                          |
|----------------------------------|-----|-----|-----|--------|---------------------------------------------------------------------------------------------------|
| DYNAMIC PERFORMANCE              |     |     |     |        |                                                                                                   |
| Output Voltage Settling Time     |     | 100 |     | ns     | 2 V step, 0.1% error, 0 V to 5 V range                                                            |
|                                  |     | 75  |     | ns     | 2 V step, 1% error, 0 V to 5 V range                                                              |
|                                  |     | 65  |     | ns     | 60 mV step, 0.1% error, 0 V to 5 V range                                                          |
|                                  |     | 15  |     | ns     | 60 mV step, 1% error, 0 V to 5 V range                                                            |
| Slew Rate                        |     | 100 |     | V/μs   | Full-scale step, 0 V to 2.5 V range                                                               |
| Digital-to-Analog Glitch Impulse |     | 50  |     | pV×s   | 0 V to 5 V range, ±1 LSB change around major carry                                                |
| Digital Feedthrough              |     | 25  |     | pV×s   | 50 MHz clock, R <sub>FB2_x</sub>                                                                  |
| DAC to DAC Crosstalk             |     | 6.5 |     | pV×s/V | Full-scale step, R <sub>FB2_x</sub>                                                               |
| AC PSRR                          |     | 80  |     | dB     | 1 kHz, R <sub>FB1_x</sub>                                                                         |
|                                  |     | 43  |     | dB     | 1 MHz, R <sub>FB1_x</sub>                                                                         |
| Output Noise Spectral Density    |     | 15  |     | nV/√Hz | DAC code = midscale, external reference, 10 kHz, NCAPx = 1.2 μF, PCAPx = none, R <sub>FB1_x</sub> |
|                                  |     | 30  |     | nV/√Hz | R <sub>FB2_x</sub>                                                                                |
|                                  |     | 60  |     | nV/√Hz | R <sub>FB4_x</sub>                                                                                |

## SPECIFICATIONS

Table 3. (Continued)

| Parameter <sup>1</sup>             | Min | Typ  | Max | Unit                       | Test Conditions/Comments                                                                                               |
|------------------------------------|-----|------|-----|----------------------------|------------------------------------------------------------------------------------------------------------------------|
| Output Noise                       |     | 3.8  |     | $\mu\text{V}_{\text{RMS}}$ | DAC code = midscale, external reference, 1 Hz to 10 kHz, NCAPx = 1.2 $\mu\text{F}$ , PCAPx = none, $R_{\text{FB}1\_x}$ |
|                                    |     | 7.6  |     | $\mu\text{V}_{\text{RMS}}$ | $R_{\text{FB}2\_x}$                                                                                                    |
|                                    |     | 15.4 |     | $\mu\text{V}_{\text{RMS}}$ | $R_{\text{FB}4\_x}$                                                                                                    |
| Total Harmonic Distortion (THD)    |     | -105 |     | dB                         | 0 V to 5 V range, $f_{\text{OUT}} = 1 \text{ kHz}$                                                                     |
|                                    |     | -101 |     | dB                         | $f_{\text{OUT}} = 10 \text{ kHz}$                                                                                      |
|                                    |     | -84  |     | dB                         | $f_{\text{OUT}} = 100 \text{ kHz}$                                                                                     |
| Spurious-Free Dynamic Range (SFDR) |     | -105 |     | dB                         | 0 V to 5 V range, $f_{\text{OUT}} = 1 \text{ kHz}$                                                                     |

<sup>1</sup> See the [Terminology](#) section.

## TIMING CHARACTERISTICS

$\text{AV}_{\text{DD}} = 5.0 \text{ V} \pm 5\%$ ,  $\text{DV}_{\text{DD}} = 1.8 \text{ V} \pm 5\%$ ,  $1.1 \text{ V} \leq V_{\text{LOGIC}} \leq 1.9 \text{ V}$ ,  $-40^\circ\text{C} \leq T_{\text{A}} \leq +105^\circ\text{C}$ , unless otherwise noted.

Table 4.

| Parameter <sup>1, 2</sup> | Description                                                                 | Min  | Typ  | Max | Unit              | Test Conditions / Comments                              |
|---------------------------|-----------------------------------------------------------------------------|------|------|-----|-------------------|---------------------------------------------------------|
| $f_{\text{SCLK}}$         | SCLK frequency                                                              |      |      | 66  | MHz               |                                                         |
| $t_1$                     | SCLK cycle time                                                             | 15.2 |      |     | ns                |                                                         |
| $t_{\text{SCLK}2}$        | SCLK half period                                                            | 7.6  |      |     | ns                |                                                         |
| $t_2$                     | $\overline{\text{CS}}$ falling edge to first SCLK rising edge               | 5    |      |     | ns                |                                                         |
| $t_3$                     | Last SCLK sampling edge <sup>3</sup> to $\overline{\text{CS}}$ rising edge  | 10   |      |     | ns                |                                                         |
| $t_4$                     | $\overline{\text{CS}}$ falling edge from SCLK sampling edge ignored         | 5    |      |     | ns                |                                                         |
| $t_5$                     | $\overline{\text{CS}}$ rising edge to SCLK rising edge ignored              | 5    |      |     | ns                |                                                         |
| $t_6$                     | Minimum $\overline{\text{CS}}$ high time                                    | 10   |      |     | ns                |                                                         |
| $t_7$                     | Data setup time                                                             | 2    |      |     | ns                |                                                         |
| $t_8$                     | Data hold time                                                              | 2    |      |     | ns                |                                                         |
| $t_9$                     | SCLK falling edge to SDO data valid                                         |      |      | 15  | ns                | $1.7 < V_{\text{LOGIC}} < 1.9$                          |
|                           |                                                                             |      |      | 25  | ns                | $1.1 < V_{\text{LOGIC}} < 1.7$                          |
| $t_{10}$                  | SCLK sampling edge to $\overline{\text{LDAC}}$ falling edge                 | 7.6  |      |     | ns                |                                                         |
| $t_{11}$                  | $\overline{\text{LDAC}}$ pulse width low                                    | 7.6  |      |     | ns                |                                                         |
| $t_{12}$                  | $\overline{\text{CS}}$ rising edge to SDO disabled                          |      | 50   |     | ns                |                                                         |
| $t_{13}$                  | $\overline{\text{LDAC}}$ rising edge to $\overline{\text{CS}}$ falling edge | 5    |      |     | ns                |                                                         |
| $t_{14}$                  | $\overline{\text{RESET}}$ pulse width low                                   | 10   |      |     | ns                | $t_{14}$ to $t_{19}$ shown in <a href="#">Figure 12</a> |
| $t_{15}$                  | $\overline{\text{RESET}}$ pulse activation time                             |      |      | 100 | ns                |                                                         |
| $t_{16}$                  | $V_{\text{OUT}}$ Update from CHx_DAC Register Write                         |      | 12.6 |     | ns                |                                                         |
| $t_{17}$                  | $V_{\text{OUT}}$ update from $\overline{\text{LDAC}}$ falling edge          |      | 5    |     | ns                |                                                         |
| $t_{18}^4$                | Wait time before DAC register access                                        | 100  |      |     | ms                |                                                         |
| $t_{19}^5$                | Shutdown exit time                                                          |      | 5    |     | ms                |                                                         |
| Update Rate               | Quad SPI mode, DDR and streaming enabled, precision mode                    |      |      | 22  | MUPS <sup>6</sup> |                                                         |
|                           | Quad SPI mode, DDR and streaming enabled, fast mode                         |      |      | 33  | MUPS <sup>6</sup> |                                                         |

<sup>1</sup> All input signals are specified with  $t_{\text{R}} = t_{\text{F}} = 1 \text{ ns/V}$  (10% to 90%) and timed from a voltage level of  $(V_{\text{IL}} + V_{\text{IH}})/2$ .

<sup>2</sup> Guaranteed by design and characterization, not production tested.

<sup>3</sup> The SCLK sampling edge refers to the SCLK edge where the data is read in (sampled)

<sup>4</sup> Same timing must be expected at power-up from the instant that  $\text{AV}_{\text{DD}} = 4 \text{ V}$  or  $\text{DV}_{\text{DD}} = 0.8 \text{ V}$ .

## SPECIFICATIONS

<sup>5</sup> Time required to exit power-down to normal mode.

<sup>6</sup> MUPS is mega updates per second.

## Timing Diagrams

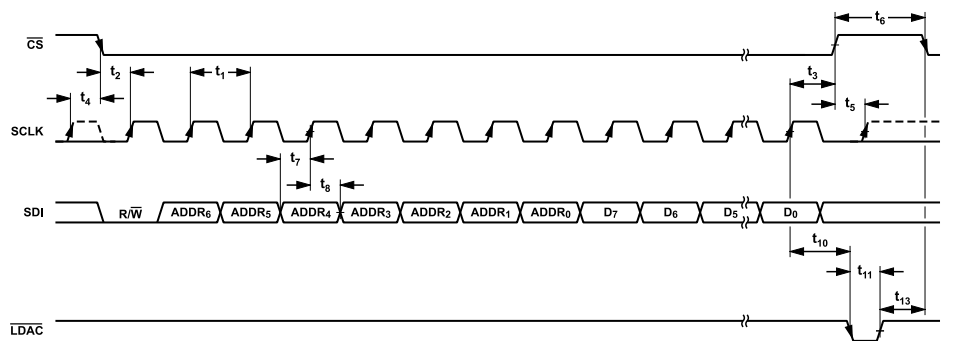


Figure 2. Classic SPI Write Operation with Single Data Rate

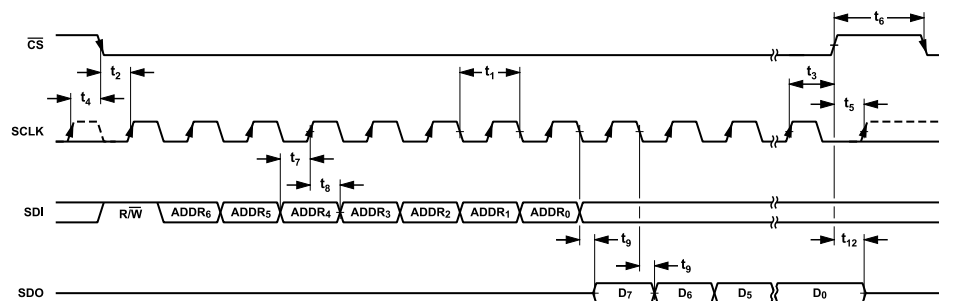


Figure 3. Classic SPI Read Operation with Single Data Rate

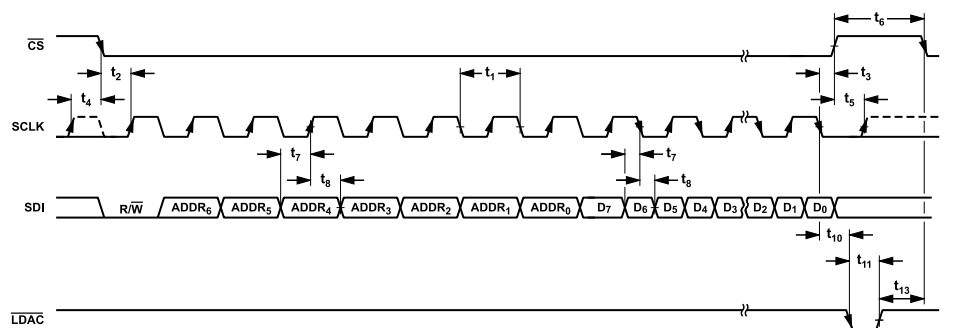


Figure 4. Classic SPI Write Operation with Double Data Rate

## SPECIFICATIONS

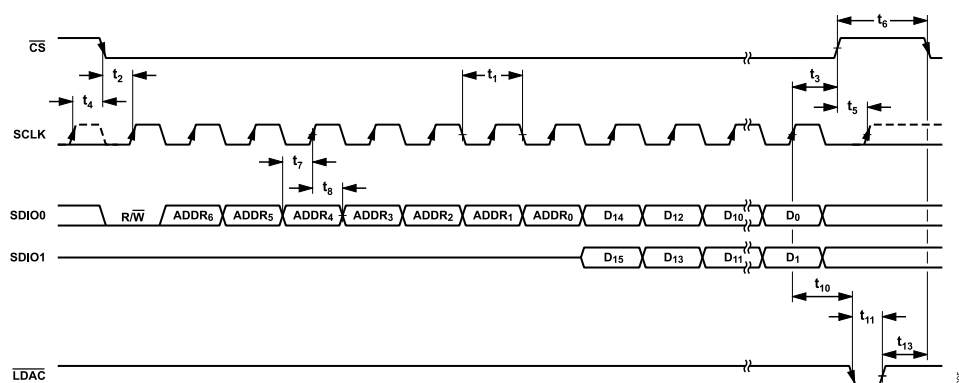


Figure 5. Dual SPI Write Operation with Single Data Rate

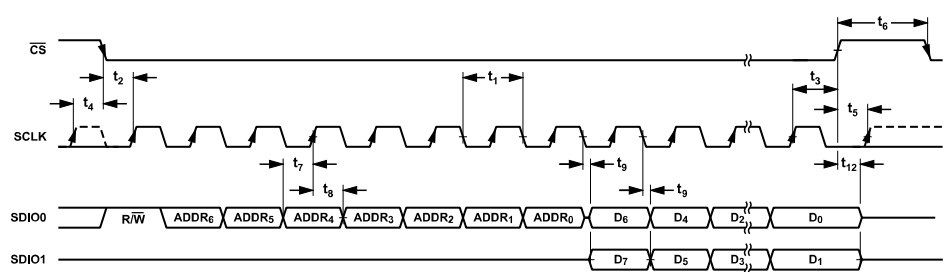


Figure 6. Dual SPI Read Operation with Single Data Rate

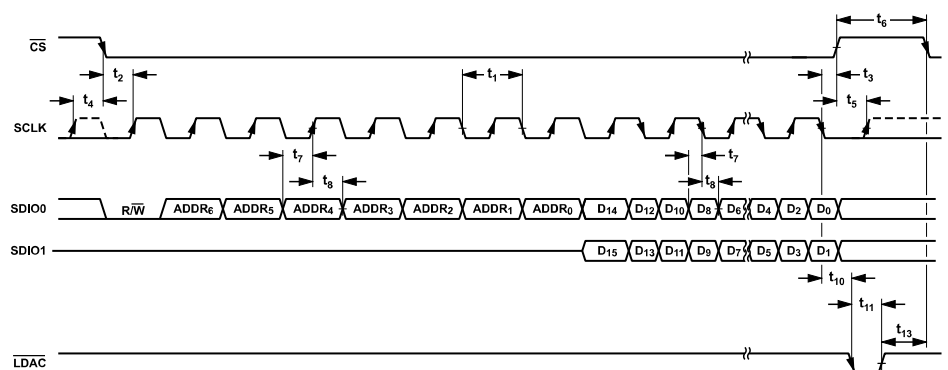


Figure 7. Dual SPI Write Operation with Double Data Rate

SPECIFICATIONS

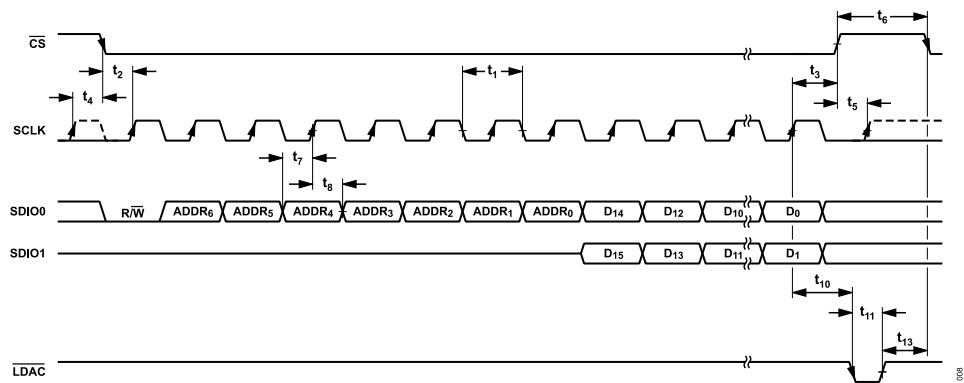


Figure 8. Dual Synchronous SPI Write Operation with Single Data Rate

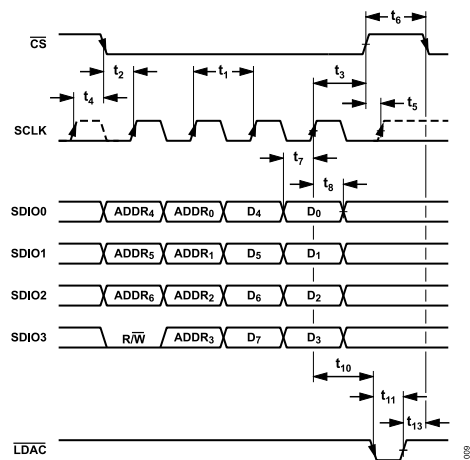


Figure 9. Quad SPI Write Operation with Single Data Rate

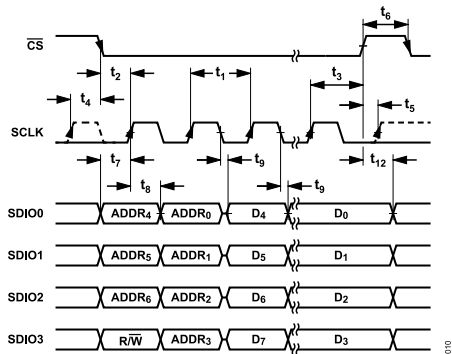


Figure 10. Quad SPI Read Operation with Single Data Rate

SPECIFICATIONS

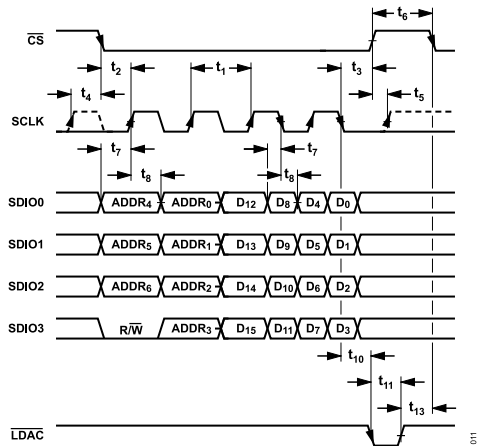


Figure 11. Quad SPI Write Operation with Double Data Rate

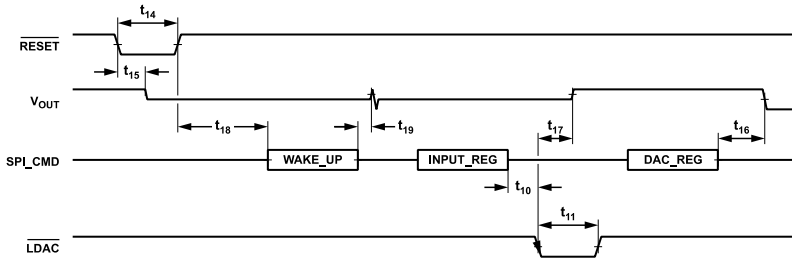


Figure 12. Start-Up Sequence Timing

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 5.

| Parameter                              | Rating                                                         |
|----------------------------------------|----------------------------------------------------------------|
| $AV_{DD}$ to AGND                      | -0.3 V to +6 V                                                 |
| $DV_{DD}$ to DGND                      | -0.3 V to +2.1 V                                               |
| AGND to DGND                           | -0.3 V to +0.3 V                                               |
| $V_{LOGIC}$ to DGND                    | -0.3 V to $DV_{DD} + 0.3$ V or<br>+2.1 V (whichever is less)   |
| $V_{REF}$ to AGND                      | -0.3 V to +3 V                                                 |
| $R_{FBX\_y}$ to AGND                   | -18 V to +18 V                                                 |
| Digital Input Voltage to DGND          | -0.3 V to $V_{LOGIC} + 0.3$ V or +2.1 V<br>(whichever is less) |
| Operating Temperature Range            |                                                                |
| Industrial                             | -40°C to +105°C                                                |
| Storage Temperature Range              | -65°C to +150°C                                                |
| Maximum Junction Temperature ( $T_J$ ) | 125°C                                                          |
| Power Dissipation                      | (Maximum $T_J - T_A$ )/ $\theta_{JA}$                          |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operation environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$  is the natural convection junction to ambient thermal resistance.

$\theta_{JC}$  is the junction to case thermal resistance. Both  $\theta_{JA}$  and  $\theta_{JC}$  are defined by the JEDEC JESD51 standard, and their values are dependent on the test board and test environment.

Table 6. Thermal Resistance

| Package Type <sup>1</sup> | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---------------------------|---------------|---------------|------|
| CP-32-30                  | 43.5          | 23.6          | °C/W |

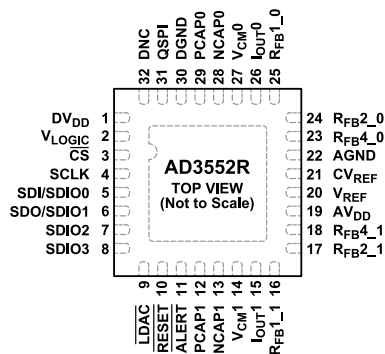
<sup>1</sup> Simulation values on JEDEC 2S2P board with 9 thermal vias, still air (0 m/sec airflow).

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
 1. DNC = DO NOT CONNECT, LEAVE THIS PIN FLOATING.  
 2. ANALOG GROUND REFERENCE. IT IS RECOMMENDED TO CONNECT DGND AND AGND TO THE SAME GROUND PLANE UNDER THE DEVICE.

013

Figure 13. Pin Configuration

Table 7. Pin Function Descriptions

| Pin No. | Mnemonic                  | Type | Description                                                                                                                                                                                                                                                                                                                               |
|---------|---------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | DV <sub>DD</sub>          | S    | Digital Core Power Supply. 1.8 V $\pm$ 5%.                                                                                                                                                                                                                                                                                                |
| 2       | V <sub>LOGIC</sub>        | S    | Digital Interface Power Supply. 1.2 V to 1.8 V.                                                                                                                                                                                                                                                                                           |
| 3       | $\overline{\text{CS}}$    | DI   | Chip Select, Active Low Logic Input. This is the frame synchronization signal for the input data.                                                                                                                                                                                                                                         |
| 4       | SCLK                      | DI   | Serial Clock Input.                                                                                                                                                                                                                                                                                                                       |
| 5       | SDI/SDIO0                 | DI/O | Serial Data Input in Classic SPI Mode.                                                                                                                                                                                                                                                                                                    |
| 6       | SDO/SDIO1                 | DI/O | Serial Bidirectional Input/Output Bit 0 in Dual or Quad SPI Modes.                                                                                                                                                                                                                                                                        |
| 7       | SDIO2                     | DI/O | Serial Bidirectional Input/Output Bit 1 in Dual or Quad SPI Modes.                                                                                                                                                                                                                                                                        |
| 8       | SDIO3                     | DI/O | Serial Bidirectional Input/Output Bit 2 in Quad SPI Mode. Pull down if not used.                                                                                                                                                                                                                                                          |
| 9       | $\overline{\text{LDAC}}$  | DI   | Serial Bidirectional Input/Output Bit 3 in Quad SPI Mode. Pull down if not used.                                                                                                                                                                                                                                                          |
| 10      | $\overline{\text{RESET}}$ | DI   | Load DAC, Active Low Logic Input. $\overline{\text{LDAC}}$ can be operated in synchronous mode or asynchronous mode. Pulsing this pin low causes the DAC register to be updated if the input register has new data. If this pin is tied permanently low, the DAC is automatically updated when new data is written to the input register. |
| 11      | $\overline{\text{ALERT}}$ | DI   | Asynchronous Reset Input. Active low logic input. When $\overline{\text{RESET}}$ is low, all registers are reset to their default values and the activity on the digital interface is ignored. The AD3552R incorporates a power-on reset (POR) circuit. If this pin is not used it must be tied to V <sub>LOGIC</sub> .                   |
| 12      | PCAP1                     | AI/O | Alert Pin. Active low logic output. This pin is driven low if an alert condition is detected and it is not masked by the corresponding bit in the mask register. This pin has an internal configurable pull-up resistor.                                                                                                                  |
| 13      | NCAP1                     | AI/O | Noise Reduction Capacitor for DAC1, Optional. Capacitor connected to AV <sub>DD</sub> .                                                                                                                                                                                                                                                   |
| 14      | V <sub>CM1</sub>          | AI/O | Noise Reduction Capacitor for DAC1, Optional. Capacitor connected to GND.                                                                                                                                                                                                                                                                 |
| 15      | I <sub>OUT1</sub>         | AO   | Common Mode Voltage for DAC1. Analog input/output.                                                                                                                                                                                                                                                                                        |
| 16      | R <sub>FB1_1</sub>        | AI/O | DAC1 Output Current.                                                                                                                                                                                                                                                                                                                      |
| 17      | R <sub>FB2_1</sub>        | AI/O | Hardware Gain Selection for DAC1, Gain = 1.                                                                                                                                                                                                                                                                                               |
| 18      | R <sub>FB4_1</sub>        | AI/O | Hardware Gain Selection for DAC1, Gain = 2.                                                                                                                                                                                                                                                                                               |
| 19      | AV <sub>DD</sub>          | AI/O | Hardware Gain Selection for DAC1, Gain = 4.                                                                                                                                                                                                                                                                                               |
| 20      | V <sub>REF</sub>          | S    | Analog Power Supply. 5 V $\pm$ 5%.                                                                                                                                                                                                                                                                                                        |
| 21      | CV <sub>REF</sub>         | AI/O | Voltage Reference, 2.5 V. Input when using external reference, output or floating when using internal reference.                                                                                                                                                                                                                          |
| 22      | AGND                      | AI/O | Decoupling Capacitor for Internal Reference, Optional.                                                                                                                                                                                                                                                                                    |
| 23      | R <sub>FB4_0</sub>        | S    | Analog Ground Reference. It is recommended to connect DGND and AGND to the same ground plane under the device.                                                                                                                                                                                                                            |
| 24      | R <sub>FB2_0</sub>        | AI/O | Hardware Gain Selection for DAC0, Gain = 4.                                                                                                                                                                                                                                                                                               |
| 25      | R <sub>FB1_0</sub>        | AI/O | Hardware Gain Selection for DAC0, Gain = 2.                                                                                                                                                                                                                                                                                               |
| 26      | I <sub>OUT0</sub>         | AI/O | Hardware Gain Selection for DAC0, Gain = 1.                                                                                                                                                                                                                                                                                               |
| 27      | V <sub>CM0</sub>          | AI/O | DAC0 Output Current.                                                                                                                                                                                                                                                                                                                      |
|         |                           | AO   | DAC0 Output Current.                                                                                                                                                                                                                                                                                                                      |
|         |                           | AO   | Common Mode Voltage for DAC0 External TIA.                                                                                                                                                                                                                                                                                                |

**PIN CONFIGURATION AND FUNCTION DESCRIPTIONS****Table 7. Pin Function Descriptions (Continued)**

| Pin No. | Mnemonic | Type | Description                                                                                                                    |
|---------|----------|------|--------------------------------------------------------------------------------------------------------------------------------|
| 28      | NCAP0    | AI/O | Noise Reduction Capacitor for DAC0, Optional. Capacitor connected to GND.                                                      |
| 29      | PCAP0    | AI/O | Noise Reduction Capacitor for DAC0, Optional. Capacitor connected to $AV_{DD}$ .                                               |
| 30      | DGND     | S    | Digital Ground Reference. It is recommended to connect DGND and AGND to the same ground plane under the device.                |
| 31      | QSPI     | DI   | QSPI Mode Enable. Digital input. A high level enables quad SPI interface mode.                                                 |
| 32      | DNC      | DNC  | Do Not Connect. Leave pin floating.                                                                                            |
| EPAD    |          |      | Exposed Pad. Connect this pad to AGND and provide thermal vias, as explained in the <a href="#">Layout Guidelines</a> section. |

## TYPICAL PERFORMANCE CHARACTERISTICS

$AV_{DD} = 5\text{ V}$ ,  $DV_{DD} = V_{LOGIC} = 1.8\text{ V}$ , external voltage reference, temperature =  $25^{\circ}\text{C}$  (ambient), decoupling as outlined in the [Power Supply Recommendations](#) section, unless otherwise noted.

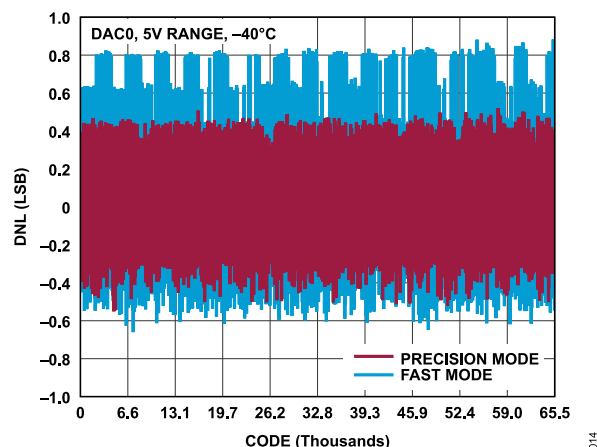


Figure 14. DNL vs. Code, 0 V to 5 V Range,  $-40^{\circ}\text{C}$ , Fast Mode and Precision Mode

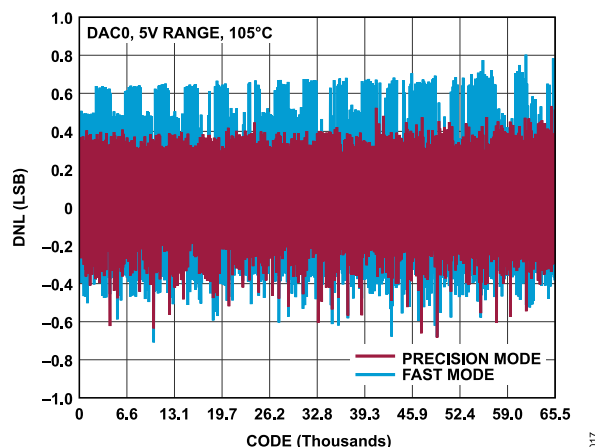


Figure 17. DNL vs. Code, 0 V to 5 V Range,  $105^{\circ}\text{C}$ , Fast Mode and Precision Mode

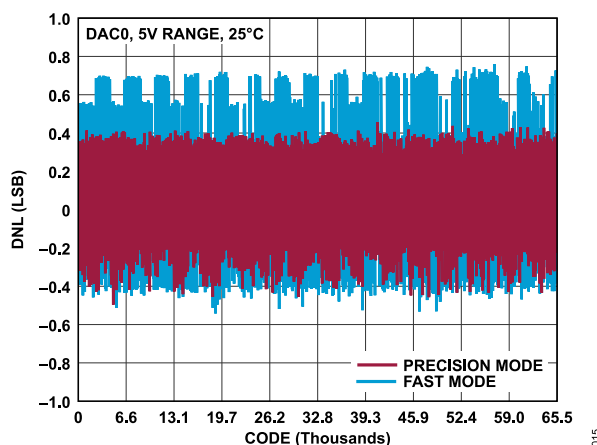


Figure 15. DNL vs. Code, 0 V to 5 V Range,  $25^{\circ}\text{C}$ , Fast Mode and Precision Mode

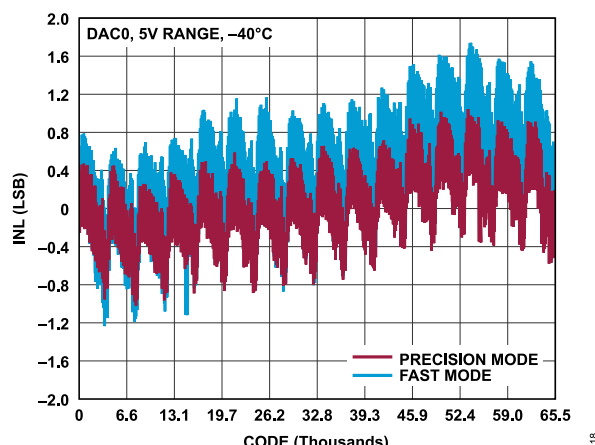


Figure 18. INL vs. Code, 0 V to 5 V Range,  $-40^{\circ}\text{C}$ , Fast Mode and Precision Mode

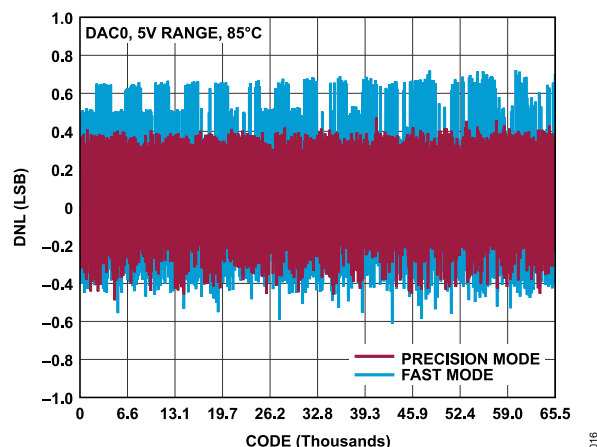


Figure 16. DNL vs. Code, 0 V to 5 V Range,  $85^{\circ}\text{C}$ , Fast Mode and Precision Mode

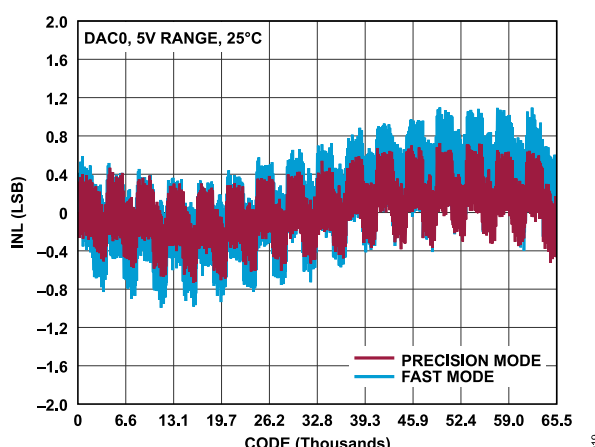


Figure 19. INL vs. Code, 0 V to 5 V Range,  $25^{\circ}\text{C}$ , Fast Mode and Precision Mode

TYPICAL PERFORMANCE CHARACTERISTICS

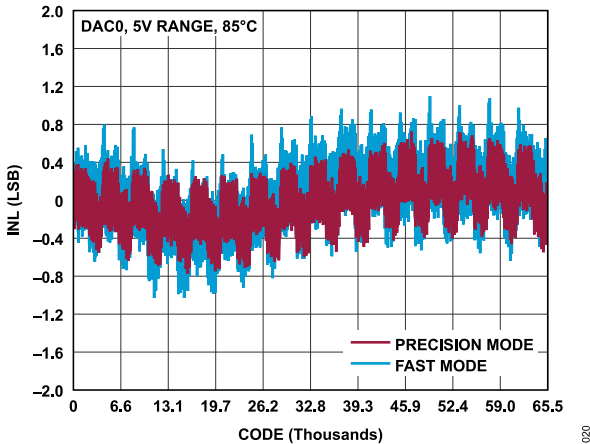


Figure 20. INL vs. Code, 0 V to 5 V Range, 85°C, Fast Mode and Precision Mode

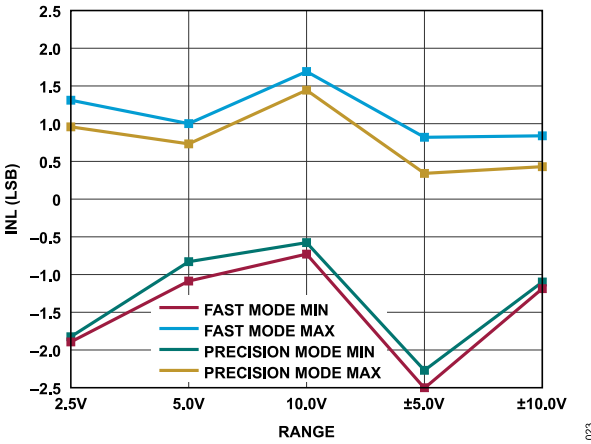


Figure 23. INL vs. Range, Fast Mode and Precision Mode

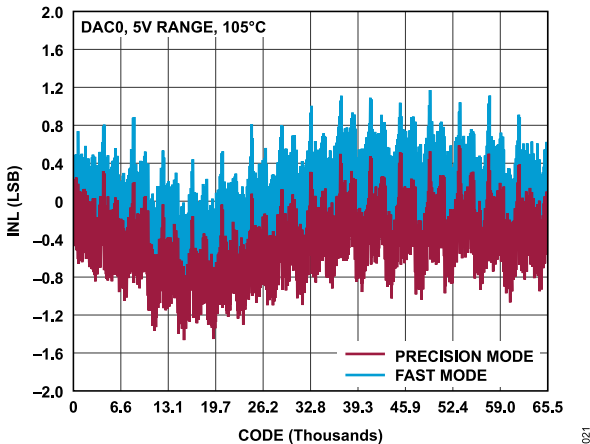


Figure 21. INL vs. Code, 0 V to 5 V Range, 105°C, Fast Mode and Precision Mode

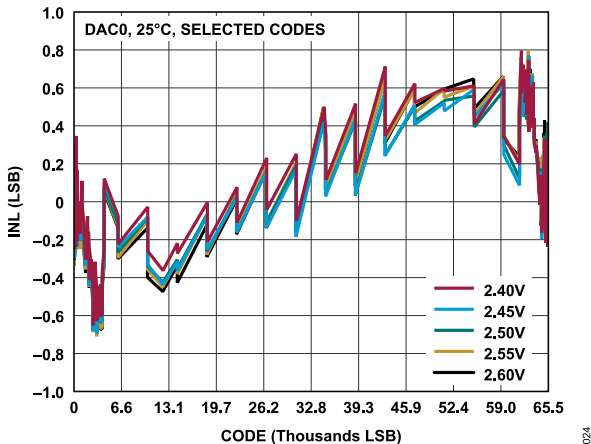


Figure 24. INL vs. Code, Reference Voltage

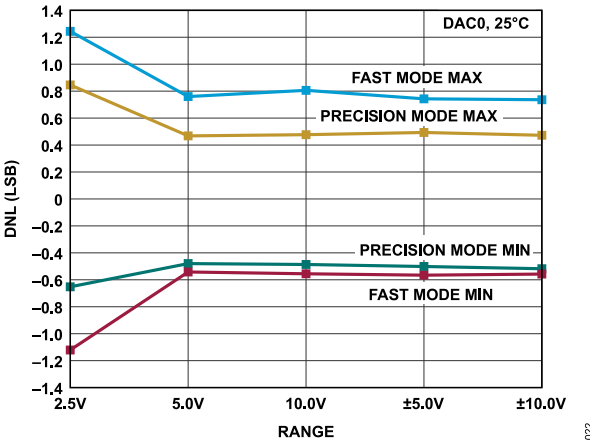


Figure 22. DNL vs. Range, Fast Mode and Precision Mode

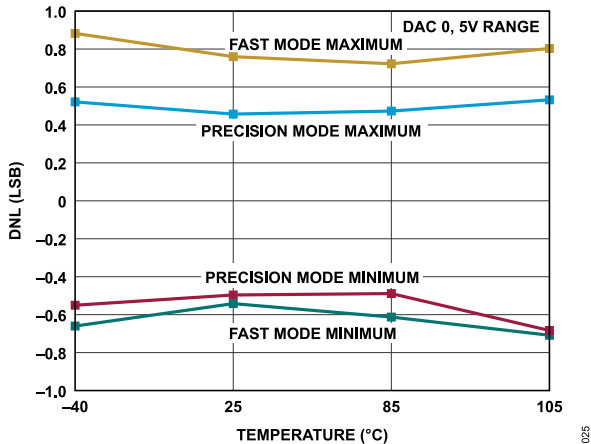


Figure 25. DNL vs. Temperature

## TYPICAL PERFORMANCE CHARACTERISTICS

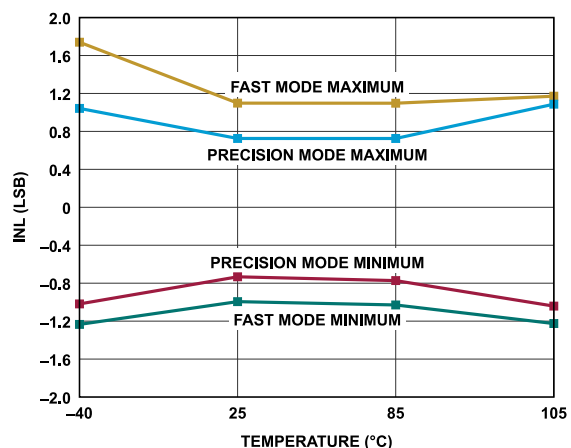


Figure 26. INL vs. Temperature

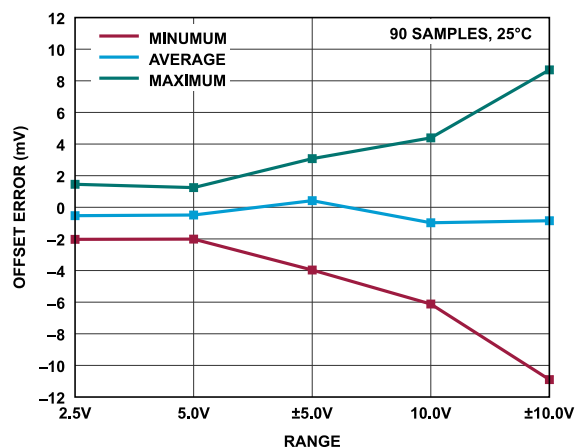


Figure 29. Offset Error vs. Range

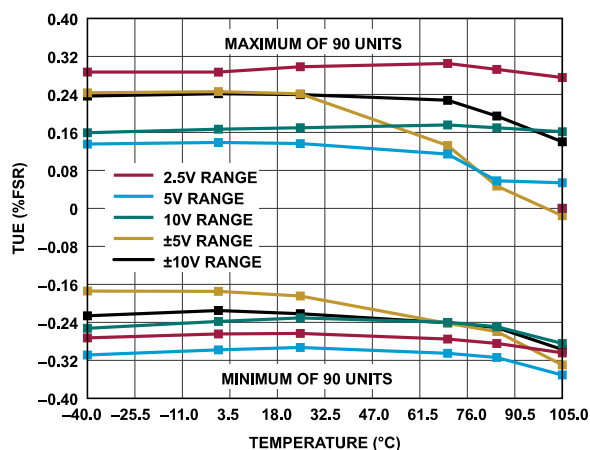


Figure 27. TUE vs. Temperature

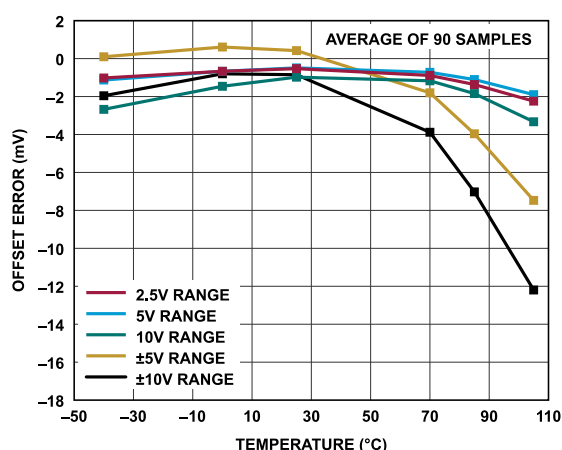


Figure 30. Offset Error vs. Temperature

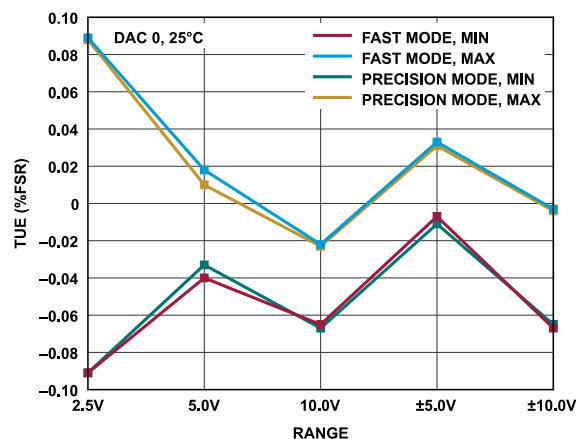


Figure 28. TUE vs. Range

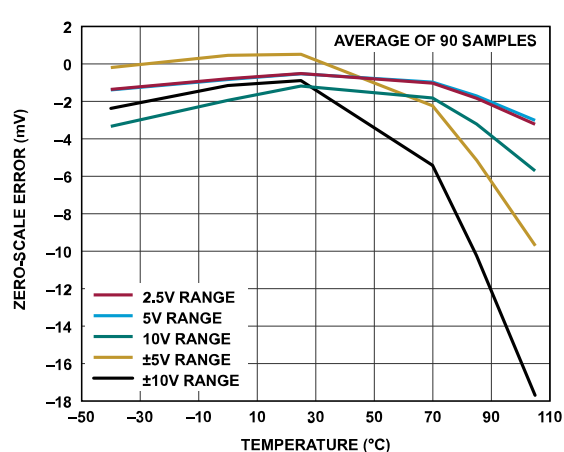


Figure 31. Zero-Scale Error vs. Temperature

## TYPICAL PERFORMANCE CHARACTERISTICS

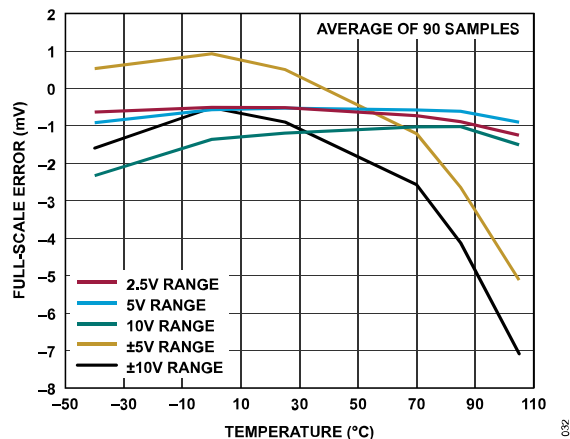


Figure 32. Full-Scale Error vs. Temperature

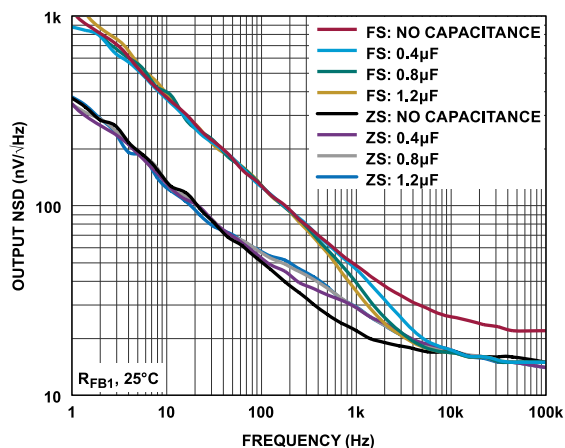


Figure 33. Output NSD vs. Frequency, PCAPx and NCAPx Capacitor Values

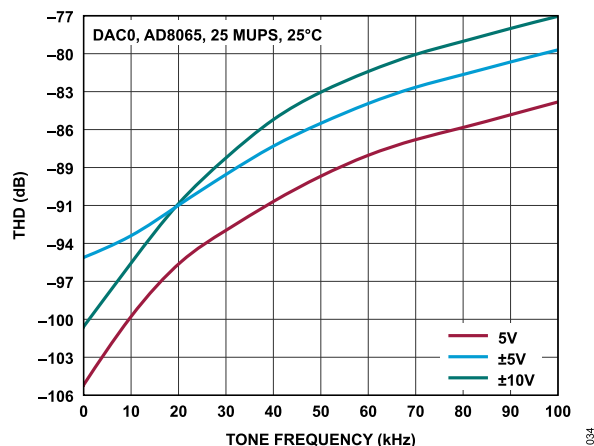


Figure 34. Total Harmonic Distortion (THD) vs. Tone Frequency

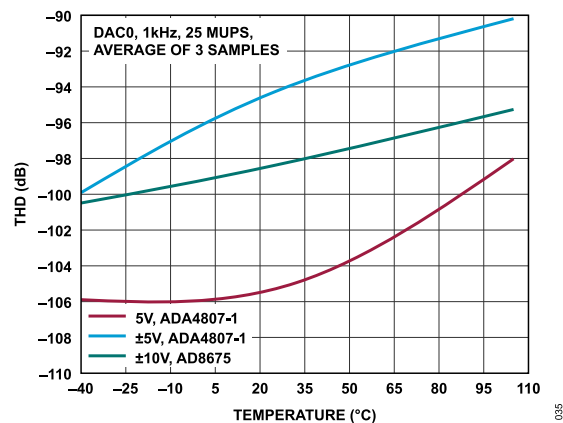


Figure 35. THD vs. Temperature

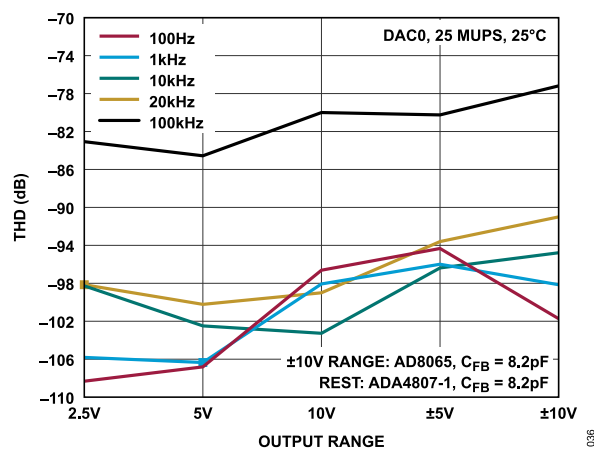


Figure 36. THD vs. Output Range

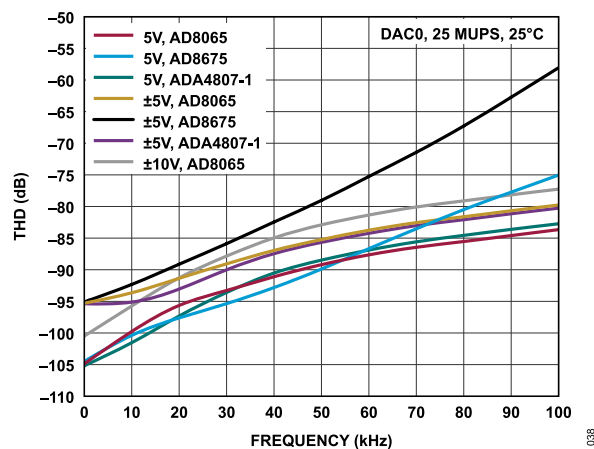


Figure 37. THD vs. Frequency, Amplifier

## TYPICAL PERFORMANCE CHARACTERISTICS

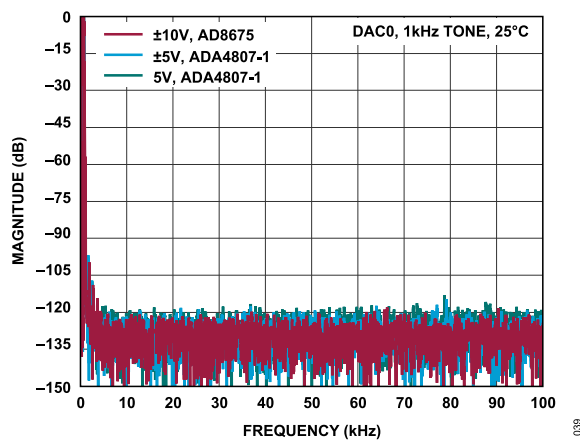


Figure 38. Fast Fourier Transform (FFT) with 1 kHz Sinewave, 25 MUPS

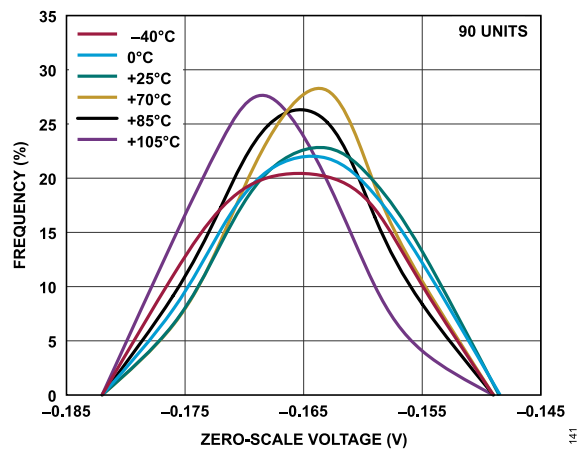


Figure 41. Zero-Scale Voltage Distribution, 0 V to 10 V Range

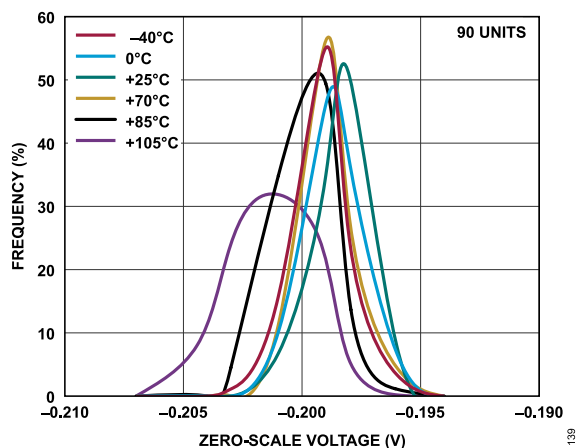


Figure 39. Zero-Scale Voltage Distribution, 0 V to 2.5 V Range

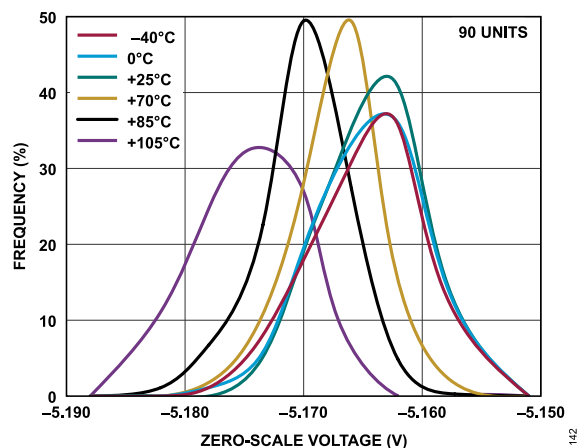


Figure 42. Zero-Scale Voltage Distribution, -5 V to +5 V Range

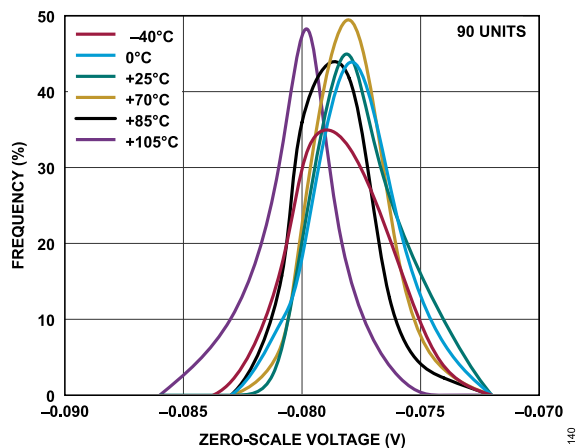


Figure 40. Zero-Scale Voltage Distribution, 0 V to 5 V Range

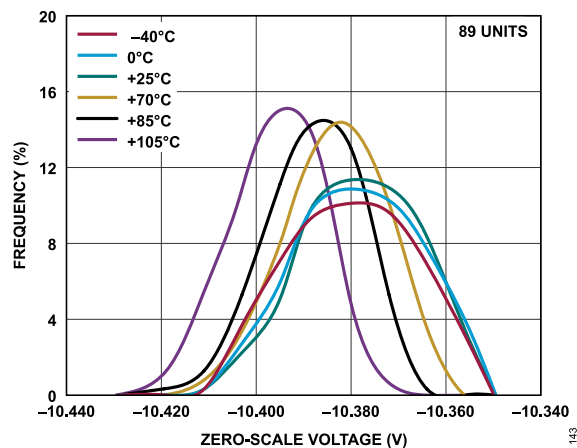


Figure 43. Zero-Scale Voltage Distribution, -10 V to +10 V Range

## TYPICAL PERFORMANCE CHARACTERISTICS

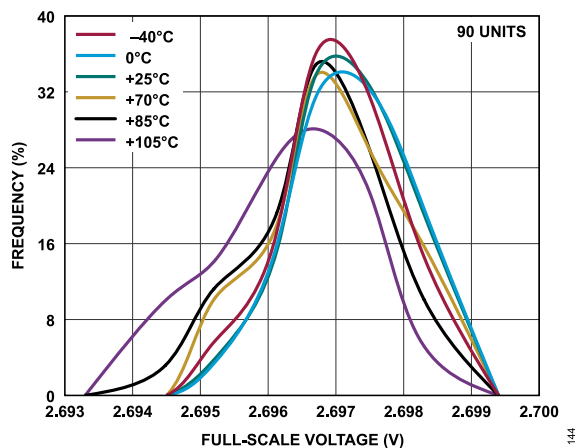


Figure 44. Full-Scale Voltage Distribution, 0 V to 2.5 V Range

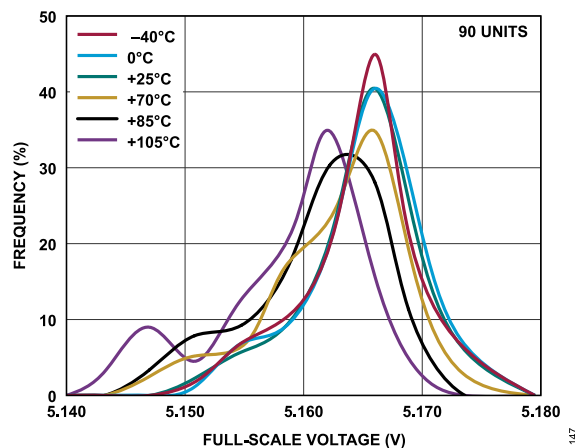


Figure 47. Full-Scale Voltage Distribution, -5 V to +5 V Range

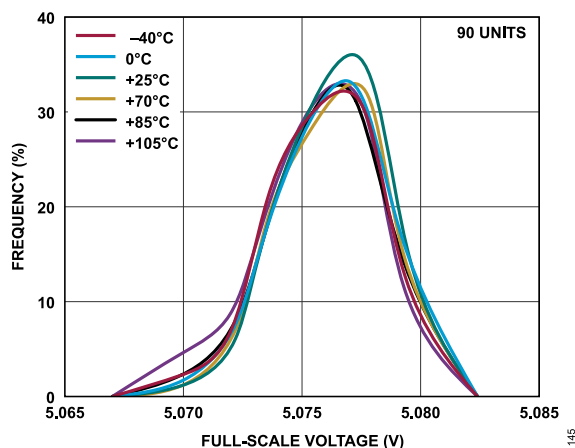


Figure 45. Full-Scale Voltage Distribution, 0 V to 5 V Range

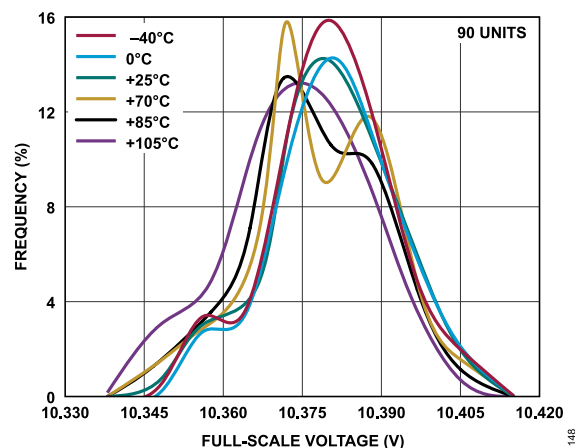


Figure 48. Full-Scale Voltage Distribution, -10 V to +10 V Range

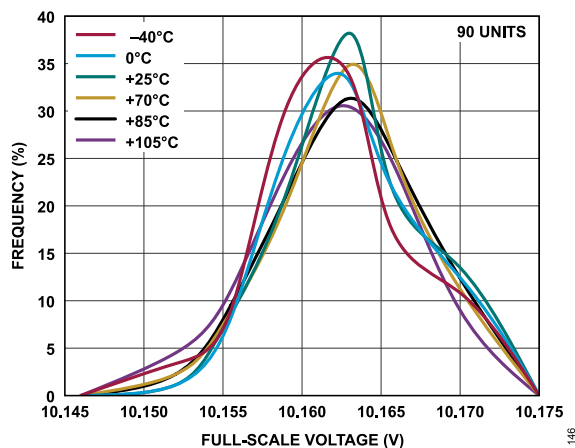


Figure 46. Full-Scale Voltage Distribution, 0 V to 10 V Range

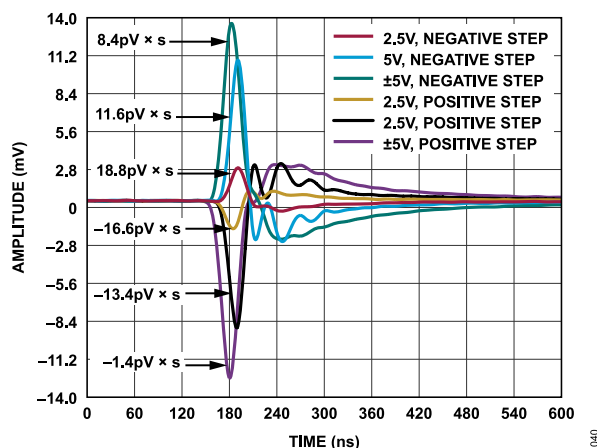


Figure 49. Digital to Analog Glitch

## TYPICAL PERFORMANCE CHARACTERISTICS

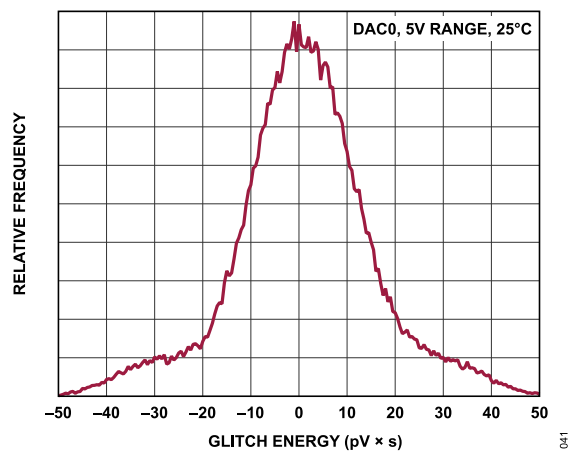


Figure 50. Digital to Analog Glitch Energy Histogram

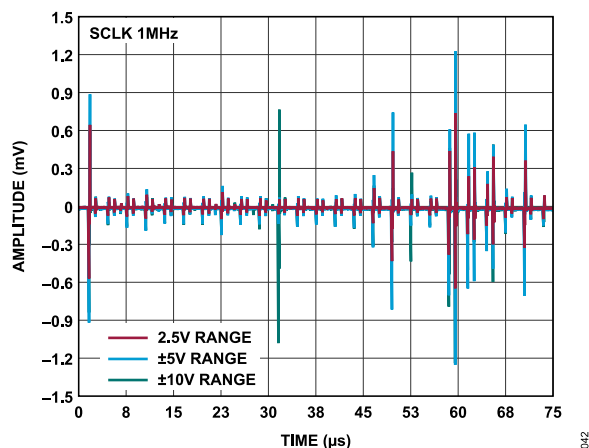


Figure 51. Digital Feedthrough

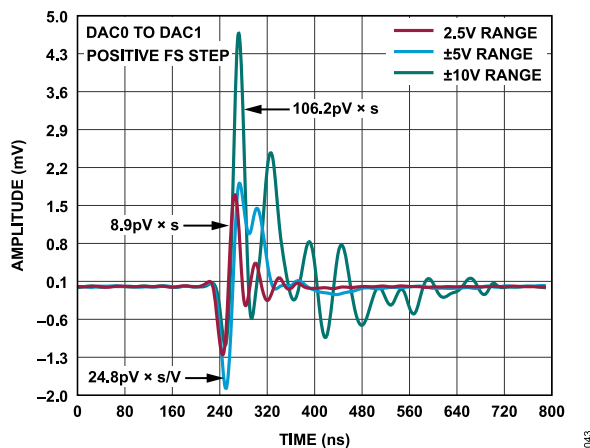


Figure 52. DAC-to-DAC Crosstalk

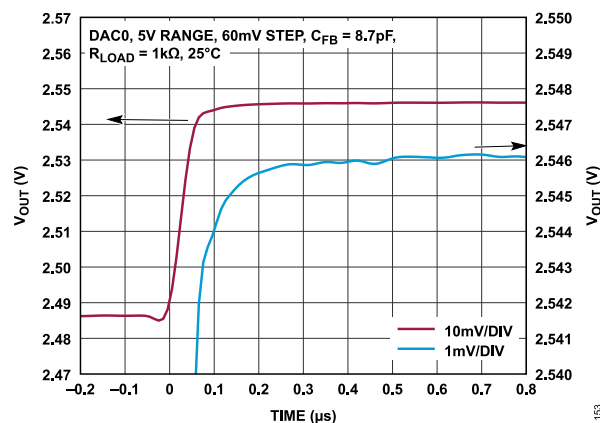


Figure 53. Small Signal Settling Time, 0 V to 5 V Range

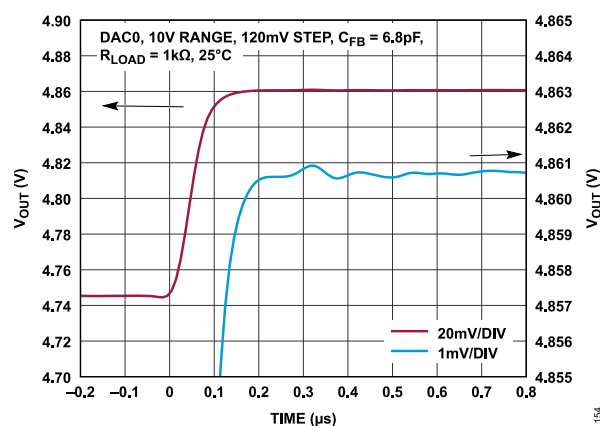


Figure 54. Small Signal Settling Time, 0 V to 10 V Range

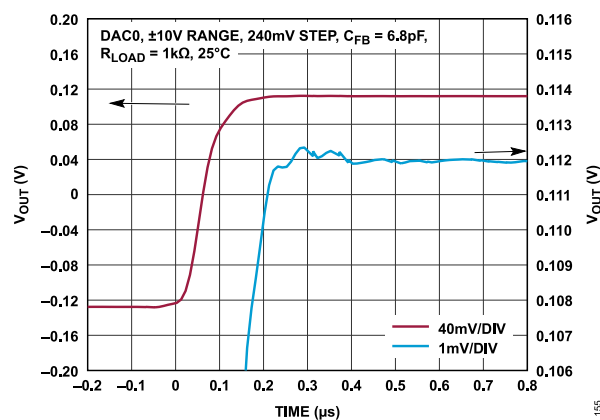


Figure 55. Small Signal Settling Time, -10 V to +10 V Range

## TYPICAL PERFORMANCE CHARACTERISTICS

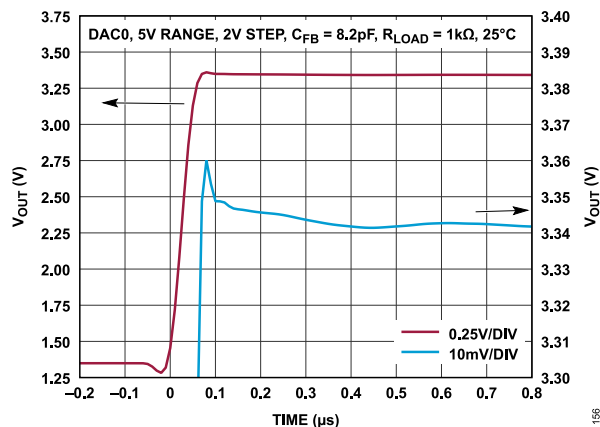


Figure 56. Large Signal Settling Time, 0 V to 5 V Range

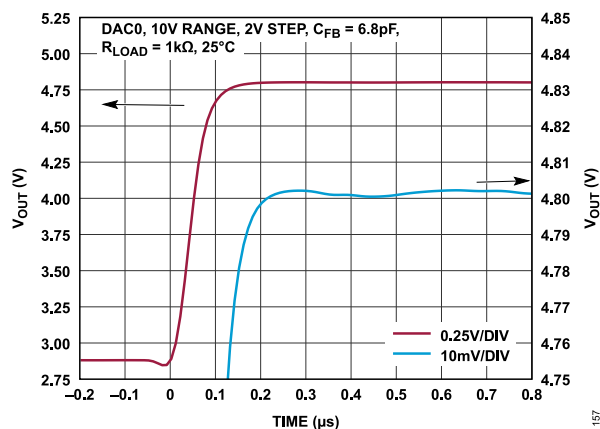


Figure 57. Large Signal Settling Time, 0 V to 10 V Range

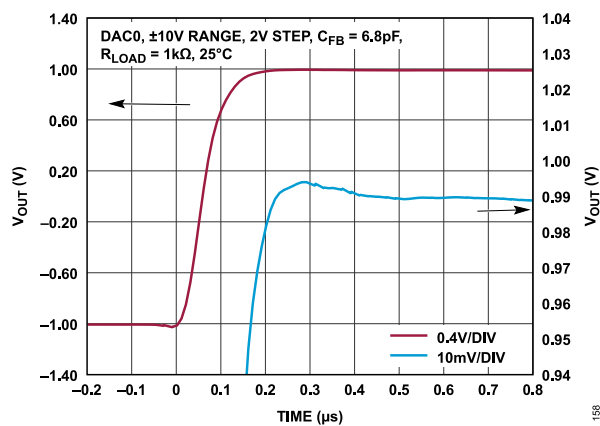


Figure 58. Large Signal Settling Time, -10 V to +10 V Range

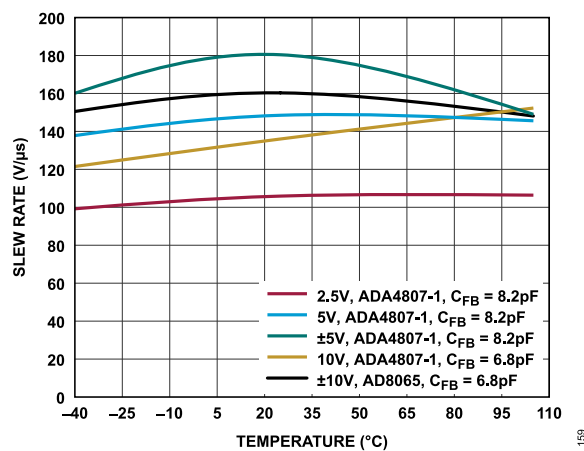


Figure 59. Slew Rate vs. Temperature

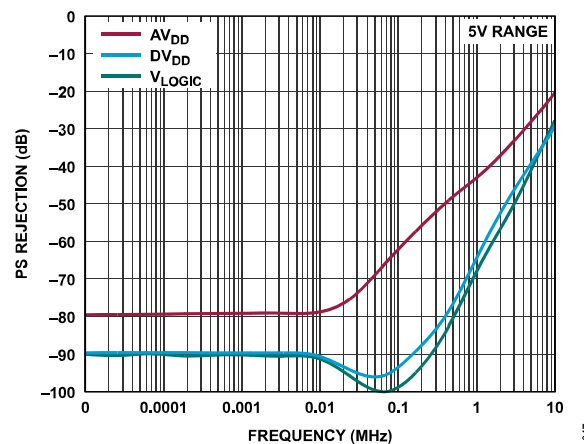
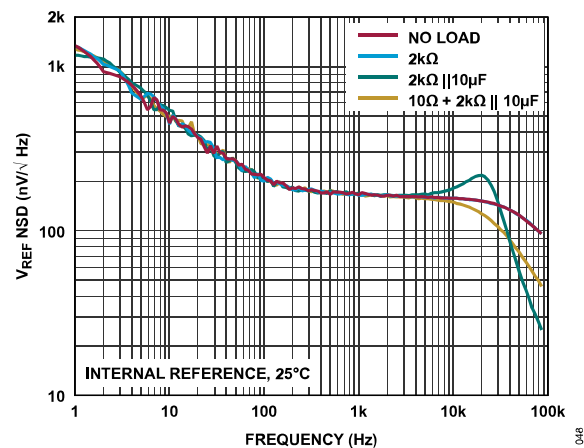


Figure 60. AC PSRR

Figure 61. Reference Voltage ( $V_{REF}$ ) NSD vs. Frequency, Load Impedance

## TYPICAL PERFORMANCE CHARACTERISTICS

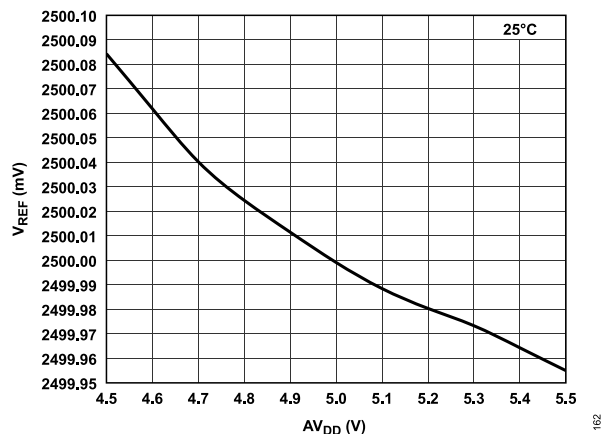
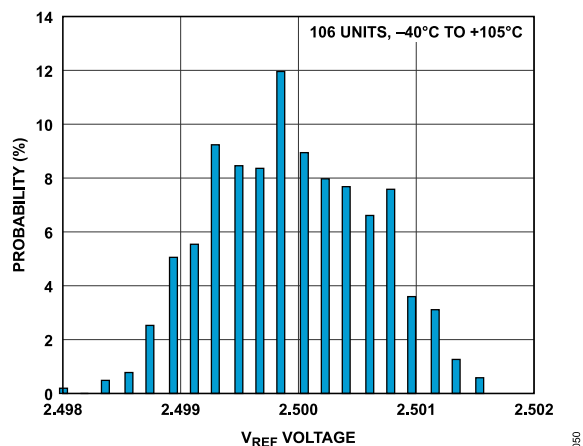
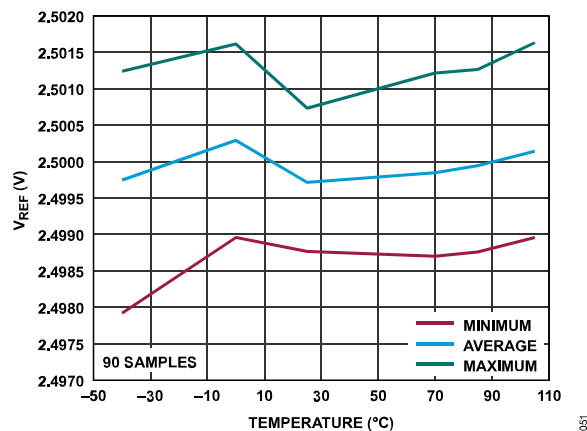
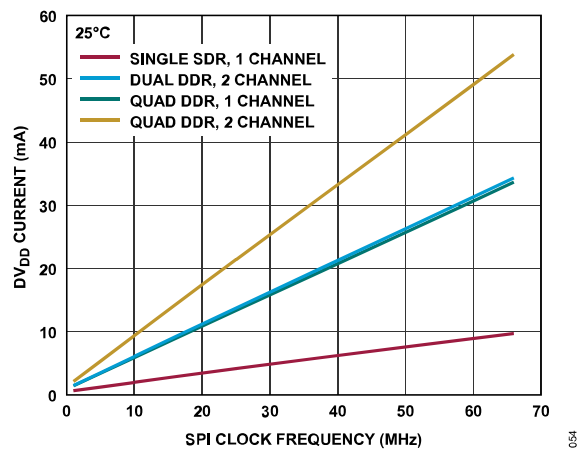
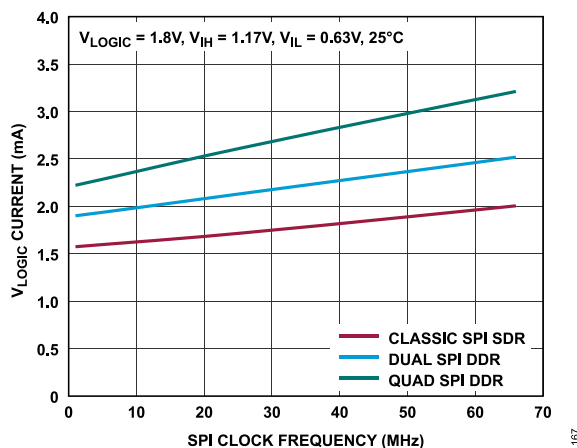
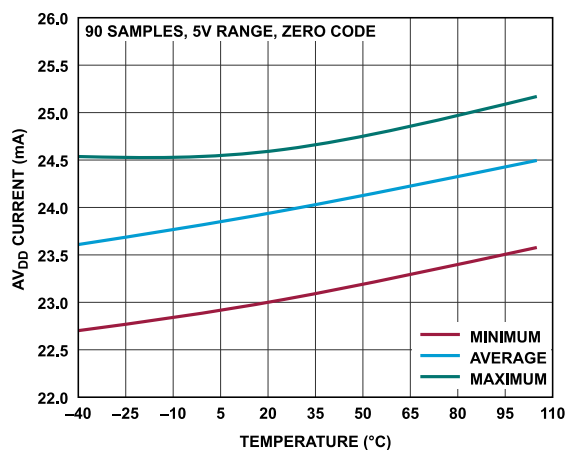
Figure 62.  $V_{REF}$  vs. Supply ( $AV_{DD}$ )

Figure 63. Reference Voltage Spread

Figure 64.  $V_{REF}$  vs. TemperatureFigure 65.  $DV_{DD}$  Current vs. SPI Clock Frequency, SPI ModeFigure 66.  $V_{LOGIC}$  Current vs. SPI Clock Frequency, SPI ModeFigure 67.  $AV_{DD}$  Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

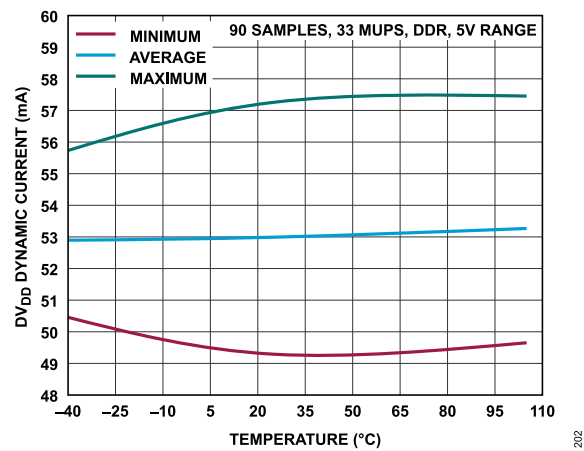


Figure 68.  $DV_{DD}$  Dynamic Current vs. Temperature

## TERMINOLOGY

### Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

### Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes.

### Offset Error

Offset error is the vertical deviation from the ideal transfer function after the gain error has been compensated. Offset error is expressed in mV. In the AD3552R, offset error is measured at midscale. The comparison between the ideal output and the actual output is performed at midscale.

### Offset Error Drift

The offset error drift is a measurement of the relative variation of the offset with temperature. It is expressed in ppm/°C. Total offset at a given temperature is calculated as

$$Offset_T = Offset_{25^\circ C} + \frac{TC \times (T - 25) \times V_{RANGE}}{10^6}$$

### Full-Scale and Zero-Scale Error

These errors measure the deviation from the ideal value at full scale and zero scale, at 25°C. The error is expressed as % of full-scale range (FSR). In the case of the AD3552R, the ideal value is calculated as the average of a sufficiently high number of samples.

### Full-Scale and Zero-Scale Error Drift

These parameters measure the variation of the zero-scale and full-scale voltage as a function of the temperature, relative to the ideal zero-scale and full-scale voltages. They are expressed in ppm/°C. The total deviation over temperature is calculated using the same formula used for the offset.

### DC PSRR and AC PSRR

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in  $V_{OUT}$  to a change in the supplies for midscale output of the DAC. DC PSRR is measured in mV/V, and AC PSRR is measured in dB.  $V_{REF}$  is held at 2.5 V, and the supplies are varied by  $\pm 200$  mV p-p.

### Output Voltage Settling Time

Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level within a given accuracy for a given step change. Typically, it is evaluated for a small step and a large step to account for the effect of amplifier slewing.

### Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV × sec and is measured when the digital input code is changed by 1 LSB.

### Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but it is measured when the DAC output is not updated. Digital feedthrough is specified in nV × sec and measured with a full-scale code change on the data bus, which means from all 0s to all 1s and vice versa.

### Output Noise Spectral Density

Noise spectral density is a measurement of the internally generated random noise. Noise is measured at the DAC output when it is loaded with the midscale code and using an ideal external reference. Noise is also measured at the output of the internal reference, if available. Noise density is expressed in nV/√Hz.

Figure 33 depicts the spectral density of the noise in the 1/f region and the flat (broadband) region, whereas the specification quoted in Table 2 pertains to the flat region.

### Total Harmonic Distortion (THD)

THD is the difference between the sine wave played by the DAC and an ideal sine wave of the same frequency and amplitude. The deviation from an ideal sine wave is due to time and amplitude discretization and nonlinear distortion. THD is measured as the power ratio of the sum of harmonic components to the fundamental component. It is expressed in dB.

### Voltage Reference Temperature Coefficient (TC)

Voltage reference TC is a measure of the change in the reference output voltage with a change in temperature. The reference TC is calculated using the box method, which defines the TC as the maximum change in the reference output over a given temperature range expressed in ppm/°C, as shown in the following equation:

$$TC = \left( \frac{V_{REF\_MAX} - V_{REF\_MIN}}{V_{REF\_NOM} \times TEMP\_RANGE} \right) \times 10^6 \quad (1)$$

where:

$V_{REF\_MAX}$  is the maximum reference output measured over the total temperature range.

$V_{REF\_MIN}$  is the minimum reference output measured over the total temperature range.

$V_{REF\_NOM}$  is the nominal reference output voltage, 2.5 V.

$TEMP\_RANGE$  is the specified temperature range, -40°C to +105°C.

**TERMINOLOGY****DC Crosstalk**

DC crosstalk is the DC change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in  $\mu\text{V/V}$ .

## THEORY OF OPERATION

## PRODUCT DESCRIPTION

The AD3552R is a dual channel, 16-bit, 33 MUPS DAC with programmable output ranges and a 2.5 V internal reference.

The AD3552R has the following two update modes:

- Fast Mode: data written in this mode is 16 bits long, resulting in a single-channel update rate of 33 MUPS. The DNL specification is valid for the reduced temperature range defined in [Table 2](#). The data for this mode is written in the registers ending in `_16B`.
- Precision Mode: data written in this mode is 24 bits long, resulting in a single-channel update rate of 22 MUPS. The DNL specification is guaranteed over the full operating temperature range. The data for this mode is written in the registers ending in `_24B`.

The AD3552R offers a versatile SPI interface capable of operating in classic, dual, and quad SPI modes with single or double data rate. The AD3552R features multiple error checkers, both in the analog and digital domains to guarantee a safe operation.

## DAC ARCHITECTURE

The AD3552R uses a current steering DAC architecture with a  $V_{REF}$  voltage of 2.5 V. The DAC current is converted to voltage by means of an external TIA.

[Figure 69](#) shows the internal block diagram.

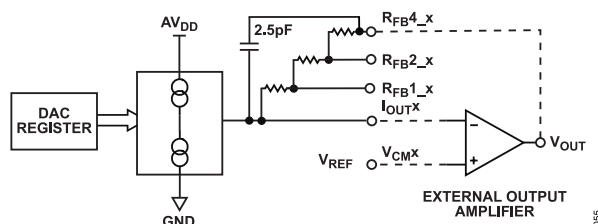


Figure 69. DAC Channel Architecture Block Diagram

Table 8. Predefined Output Span Ranges and Corresponding Feedback Resistor

| $R_{FBx\_y}$ | CH0_CH1_OUTPUT_RANGE | Output Span | CHx_GAIN_SCALING_P | CHx_GAIN_SCALING_N | CHx_OFFSET | $V_{ZS}$ (V) | $V_{FS}$ (V) |
|--------------|----------------------|-------------|--------------------|--------------------|------------|--------------|--------------|
| $R_{FB1\_y}$ | 0x000                | 2.5 V       | 0                  | 3                  | -48        | -0.198       | 2.701        |
|              | 0x001                | 5 V         | 0                  | 0                  | 0          | -0.078       | 5.077        |
| $R_{FB2\_y}$ | 0x010                | 10 V        | 0                  | 0                  | 495        | -0.165       | 10.163       |
|              | 0x011                | ±5 V        | 0                  | 0                  | -495       | -5.165       | 5.166        |
| $R_{FB4\_y}$ | 0x100                | ±10 V       | 0                  | 0                  | -245       | -10.382      | 10.380       |

The TIA feedback loop is closed by hardwiring the  $V_{OUT}$  pin to any of the available  $R_{FBx\_y}$  pins. The  $R_{FBx\_y}$  value sets the maximum voltage span that can be achieved. These voltage spans can be decreased using the gain scaling registers and repositioned within the supply rails of the TIA using the offset registers.

## PREDEFINED OUTPUT VOLTAGE SPANS

The AD3552R comes with five predefined voltage spans that are selected using the `CH0_CH1_OUTPUT_RANGE` register. The selected span must be in accordance with the feedback resistor being used, as shown in [Table 8](#). The `CHx_GAIN_SCALING_P`, `CHx_GAIN_SCALING_N`, and `CHx_OFFSET` parameters do not have to be set because their preset values are provided only as starting points for the user to create custom range values. Setting a voltage span that is not achievable with the current  $R_{FBx\_y}$  resistor results in an incorrect voltage value.

There is approximately a 3% overrange equally split on each end of the span to ensure that the nominal range is covered in any condition.

If the predefined voltage spans do not fit the intended application, custom spans can be defined using the gain scaling and offset registers as described in the [Custom Output Voltage Span](#) section.

## THEORY OF OPERATION

## CUSTOM OUTPUT VOLTAGE SPAN

In addition to the predefined output span ranges configured via the CH0\_CH1\_OUTPUT\_RANGE register, the output span range can be customized by programming the offset and gain registers in conjunction with the external feedback resistor. The CHx\_RANGE\_OVERRIDE bit must be set in the CHx\_GAIN register to override the predefined range and offset values. Gain is configured as a combination of two parameters, CHx\_GAIN\_SCALING\_P and CHx\_GAIN\_SCALING\_N, in the CHx\_GAIN register. The absolute value and the sign of the offset are configured in the CHx\_OFFSET register and the lower bits of the CHx\_GAIN register, as shown in Table 10.

The zero-scale output voltage ( $V_{OUT\_ZS}$ ) and full-scale output voltage ( $V_{OUT\_FS}$ ) are calculated using the following equations:

$$V_{OUT\_ZS} = 2.5 + 1.6 \times R_{FB} \times (Offset - Gain_P)$$

$$V_{OUT\_FS} = 2.5 + 1.6 \times R_{FB} \times (Offset + Gain_N)$$

where:

$$Gain_P = \frac{1}{2^{CHx\_GAIN\_SCALING\_P}}$$

$$Gain_N = \frac{1}{2^{CHx\_GAIN\_SCALING\_N}}$$

$$Offset = \frac{OFFSET\_POLARITY \times CHx\_OFFSET}{1024}$$

OFFSET\_POLARITY = 1 if CHx\_OFFSET\_POLARITY = 0 and -1 if CHx\_OFFSET\_POLARITY = 1, and the value of  $R_{FB}$  depends on which  $R_{FBx\_y}$  pin is connected, as shown in Table 9.

Table 9. Value of Resistors on  $R_{FBx\_y}$  pins

| Pin          | Resistor Value (kΩ) |
|--------------|---------------------|
| $R_{FB1\_y}$ | 1.610938            |
| $R_{FB2\_y}$ | 3.228125            |
| $R_{FB4\_y}$ | 6.488125            |

Table 10. Mapping of Offset Value

| Item                  | Register   | Bit   | Field Name          |
|-----------------------|------------|-------|---------------------|
| Offset Sign           | CHx_GAIN   | 2     | CHx_OFFSET_POLARITY |
| Offset Bit 8          | CHx_GAIN   | 0     | CHx_OFFSET[8]       |
| Offset Bit 7 to Bit 0 | CHx_OFFSET | [7:0] | CHx_OFFSET          |

At zero offset, a custom range is centered at  $V_{CM}$  (2.5 V). The offset register allows moving the range up or down by 25% of its span. That is, a 10 V range spans from -2.5 V to 7.5 V at zero offset, and can be shifted by  $\pm 2.5$  V using the offset register and polarity bit. The gain scaling configuration does not affect the amplitude of the offset.

While several combinations of  $R_{FB}$  and gain scaling values are possible to define a given range, it is recommended to use the lowest possible value of  $R_{FB}$  to minimize the noise density at the output of the TIA.

## TRANSFER FUNCTION

The conversion of the digital code to the DAC output current follows a linear relation with the code in plain binary. The ideal output current, in mA, is given by the following equation:

$$I_{OUTx} = 1.6 \times \left( Gain_P - Offset - \frac{D}{2^{16}} \times (Gain_P + Gain_N) \right)$$

where:

$D$  is the decimal equivalent of the binary code that is loaded in the DAC register..

$Offset$ ,  $Gain_P$ , and  $Gain_N$  are according to the definitions given in the Custom Output Voltage Span section.

The conversion of current to voltage is performed in the external TIA. If the internal feedback resistor is used, the output voltage follows the following equation:

$$V_{OUT} = V_{CM} - R_{FB} \times I_{OUT}$$

where:

$V_{CM}$  is the common-mode voltage at the  $V_{CMx}$  pin that is connected to the noninverting input of the TIA, nominally 2.5 V.

$R_{FB}$  is according to the definition given in Table 9.

 $V_{REF}$ 

The AD3552R has an internal 2.5 V voltage reference with a 3 ppm/°C temperature coefficient that is enabled at power-up. The  $V_{REF}$  pin is in high impedance at power-up to avoid electrical problems. If the internal reference must be used externally, the REFERENCE\_VOLTAGE\_SEL bits in the REFERENCE\_CONFIG register must be written to enable the  $V_{REF}$  output as described in Table 11.

When the external reference is selected, the  $V_{REF}$  pin behaves as an input.

Table 11. Voltage Reference Selection

| REFERENCE_VOLTAGE_SEL | Source   | $V_{REF}$ I/O |
|-----------------------|----------|---------------|
| 00                    | Internal | Floating      |
| 01                    | Internal | 2.5 V         |
| 10                    | External | Input         |
| 11                    | External | Input         |

## SPI REGISTER MAP ACCESS

## SPI Frame Synchronization

The  $\overline{CS}$  signal frames data during an SPI transaction. A falling edge on  $\overline{CS}$  enables the digital interface and initiates an SPI transaction. Each SPI transaction consists of at least one instruction phase and data phase, as described in the Instruction Phase section and the Data Phase section. For all SPI transactions, data is aligned MSB first. Deasserting  $\overline{CS}$  during an SPI transaction terminates part or all of the data transfer and disables the digital interface. If  $\overline{CS}$  is deasserted (returned high) after one or more register addresses are issued, those registers are written or read, but any partially

## THEORY OF OPERATION

addressed register is ignored. Figure 70 and Figure 71 outline the stages of a basic SPI write and read frame, respectively, for the AD3552R in register mode.

Detailed timing diagrams for register read and write operations are shown in Figure 2 through Figure 11. The timing specification is given in the [Timing Characteristics](#) section.

The AD3552R SPI protocol is flexible and can be configured to suit the needs of a variety of digital hosts. Data from multiple registers can be accessed in a single SPI frame, enabling efficient device configuration. All the different access modes are described in the [Single Instruction Mode](#) section and the [Streaming Mode](#) section.

### Instruction Phase

Every SPI frame starts with an instruction phase. The instruction phase immediately follows the falling edge of  $\overline{CS}$  that initiates the SPI transaction.

The instruction phase consists of a read/write bit ( $R/\overline{W}$ ) followed by a register address word. Setting  $R/\overline{W}$  low initiates a write instruction, whereas setting  $R/\overline{W}$  high initiates a read instruction. The register address word specifies the address of the register to be accessed. The register address word is 7 bits in length (7-bit addressing) by default. If required, 15-bit addressing can be enabled by setting the `SHORT_INSTRUCTION` bit to 0 in the `INTERFACE_CONFIG_B` register. If the user is using single instruction mode, each register read or write transaction in a single SPI frame also begins with an instruction phase. If the user is using streaming mode, only one instruction phase is required per SPI frame to access a set of consecutive registers. See the [Single Instruction Mode](#) section and the [Streaming Mode](#) section for instructions on selecting and using these modes.

### Data Phase

The data phase immediately follows the instruction phase, as shown in Figure 70 and Figure 71. The data phase can include the data for a single-byte register, a multibyte register, or multiple registers depending on the selected registers and access modes. See the [Single Instruction Mode](#) section, [Streaming Mode](#) section, and [Address Direction](#) section for descriptions of how these modes affect the read and write data in the data phase.

In a write operation, the content of the addressed register is updated immediately after the SCLK edge, which shifts in the last bit of the register data, regardless if it is a one-byte, two-byte, or three-byte register. Multibyte registers cannot be written partially, as explained in the [Multibyte Registers](#) section.

In a read operation, the content of the addressed register starts shifting out on the first SCLK edge of the data phase.

Data must be written to the AD3552R configuration registers in full bytes to ensure they are updated. If the data phase of an SPI write transaction does not include the entire byte of data for the register being updated, the contents of the register are not updated, and the

`CLOCK_COUNTING_ERROR` bit in the `INTERFACE_STATUS_A` register is set.

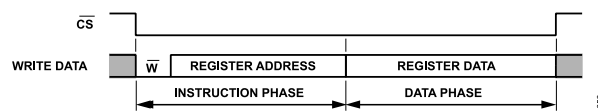


Figure 70. Basic SPI Write Frame

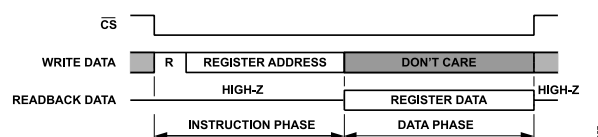


Figure 71. Basic SPI Read Frame

### Multibyte Registers

Some AD3552R registers consist of 2 or 3 bytes of data stored in adjacent addresses and are referred to as multibyte registers. Multibyte registers end with a 16B or 24B suffix when they are 2 bytes or 3 bytes, respectively.

When writing to a multibyte register of the AD3552R, all bytes must be transferred in a single SPI transaction. For this reason, the `STRICT_REGISTER_ACCESS` bit in the `INTERFACE_CONFIG_C` register is read only and set to 1. If an SPI write transaction to a multibyte register is attempted on a per byte basis, the register contents are not updated and the `PARTIAL_REGISTER_ACCESS` bit in the `INTERFACE_STATUS_A` register is set. A write transaction to a multibyte register of the AD3552R takes effect after the 24<sup>th</sup> or 16<sup>th</sup> SCLK edge of the data phase, which shifts in the last bit of the register data.

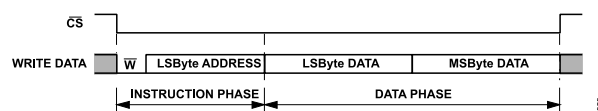


Figure 72. Multibyte Register Write with Ascending Addressing

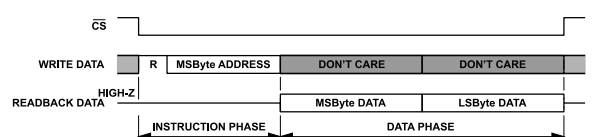


Figure 73. Multibyte Register Read with Descending Addressing

The address of a multibyte register always depends on the `ADDR_DIRECTION` bit in the `INTERFACE_CONFIG_A` register (see the [Address Direction](#) section for more details). With descending addressing, the first byte accessed in the data phase must be the most significant byte of the multibyte register, and each subsequent byte corresponds to the data in the next lower address. With ascending addressing, the first byte accessed in the data phase must be the least significant byte of the multibyte register, and each subsequent byte corresponds to the data in the next higher address.

# THEORY OF OPERATION

Multibyte registers can be read in a single SPI transaction or each byte can be addressed separately. If an SPI read transaction to a multibyte register is attempted on a per byte basis, the PARTIAL\_REGISTER\_ACCESS bit in the INTERFACE\_STATUS\_A register is set. For example, the VENDOR\_ID register is 2 bytes long, and the addresses of its least significant byte and most significant byte are 0x0C and 0x0D, respectively. [Figure 72](#) and [Figure 73](#) show write and read transactions to a multibyte register (2 bytes) for address ascending and descending mode, respectively. See the [Address Direction](#) section for more information on selecting address descending (auto-decrementing) or ascending (auto-incrementing).

## Address Direction

The address direction option is used to control whether the register address is set to automatically increment (address ascending) or decrement (address descending) when transferring multiple bytes of data in a single data phase (for example, when accessing multibyte registers, as shown in [Figure 72](#) and [Figure 73](#), or when accessing multiple registers with streaming mode, as shown in [Figure 75](#)).

Address direction is selected with the ADDR\_DIRECTION bit in the INTERFACE\_CONFIG\_A register. If ADDR\_DIRECTION is set to 0, the address decrements after each byte is accessed. If ADDR\_DIRECTION is set to 1, the address increments after each byte is accessed.

When accessing multibyte registers, use descending addresses to shift in the most significant byte first.

Multibyte registers from Address 0x29 onwards can only be accessed in descending mode.

## Single Instruction Mode

When the SINGLE\_INSTRUCTION bit in the INTERFACE\_CONFIG\_B register is set to 1, streaming mode is disabled, and single instruction mode is enabled. In single instruction mode, the data phase only contains data for a single register, and each data phase must be followed by a new instruction phase, even if  $\overline{CS}$  remains low. Single instruction mode allows the digital host to quickly read from and write to registers with nonadjacent addresses in a single SPI frame, whereas streaming mode only allows either reading or writing to contiguous registers without pulsing  $\overline{CS}$  high to initiate a new instruction phase.

[Figure 74](#) shows an example of an SPI transaction in single instruction mode with the following register accesses:

- Sets the output range.
- Enables the output stage.
- Reads the CHIP\_TYPE register.

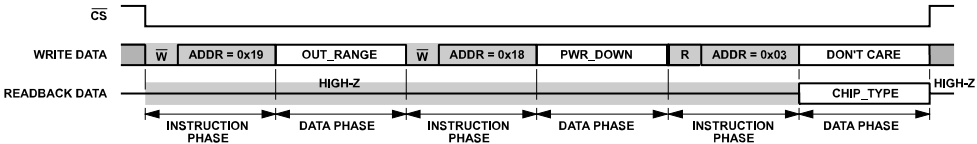


Figure 74. Single Instruction Mode Register Access Example with Address Descending

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## Streaming Mode

When the SINGLE\_INSTRUCTION bit in the INTERFACE\_CONFIG\_B register is set to 0, single instruction mode is disabled and streaming mode is enabled. In streaming mode, multiple registers with adjacent addresses can be accessed with a single instruction phase and data phase, allowing efficient access of contiguous regions of memory (for example, during initial device configuration). The AD3552R is configured in streaming mode by default.

When in streaming mode, each SPI frame consists of a single instruction phase and the following data phase contains data for multiple registers with adjacent addresses. A starting register address is specified by the digital host in the instruction phase, and this address is automatically incremented or decremented (based on the address direction setting) after each byte of data is accessed. The data phase can, therefore, be multiple bytes long, and each consecutive byte of read or write data corresponds to the next higher or lower register address (for ascending and descending address direction, respectively).

When writing or reading from a multibyte register in streaming mode with address ascending, the user must address the least significant byte of the register in the instruction phase. The data phase starts transferring data from the least significant byte in first place.

When writing or reading from a multibyte register in streaming mode with the address descending, the user must start addressing the most significant byte of the register in the instruction phase. The data phase starts transferring the most significant byte in first place.

Figure 75 shows the instruction and data phase when using streaming mode with address descending to write some registers of the AD3552R starting from Address 0x16. The length of the data phase determines the number of data bytes to be transferred to consecutive addresses. CS is brought high at the end of the write transaction (in Figure 75, the end of the write transaction occurs after Address 0x02).

Figure 76 shows the instruction and data phase when using streaming mode with address descending to read some registers of the AD3552R starting from Address 0x16. The length of the data phase determines the number of data bytes to be transferred to consecutive addresses. CS is brought high at the end of the read

transaction (in Figure 76, the end of the read transaction occurs after Address 0x02).

The STREAM\_MODE register can be used to specify a range of consecutive registers to loop through in the data phase. Looping allows the digital host to repeatedly read from or write to a set of registers (for example, CHx\_DAC\_16B register at Address 0x29 to Address 0x2C) as efficiently as possible. When accessing register addresses after and including Address 0x29, the address direction must always be set as descending.

If STREAM\_MODE is set to 0, looping is disabled and the following occurs:

- If address direction is set to descending, the address decrements until it reaches 0x00. On the subsequent byte accesses, the address is set to the top of the addressable space (Address 0x4B). Note that restrictions may apply in terms of SPI mode access depending on the register address.
- If address direction is set to ascending, the address increments until it reaches the top of the addressable space (Address 0x4B). On the subsequent byte access, the address is reset to 0x00. Note that restrictions may apply in terms of SPI mode access depending on the register address. Multibyte registers greater than 0x29 do not update in ascending mode.

If STREAM\_MODE is set to a value other than 0, looping is enabled and the value corresponds to the number of bytes to be accessed in the data phase before the address loops back to the value specified in the address phase. An example is shown in Figure 77, where the CH0\_DAC\_16B register is accessed twice using the looping feature.

The value of the STREAM\_MODE register can be preserved or reset to 0 at the end of the transaction (when CS returns high) depending on the value of the STREAM\_LENGTH\_KEEP\_VALUE bit in the TRANSFER\_REGISTER, as shown in Table 12. This feature allows writing the same range of registers continuously within the same transaction, which is useful for waveform playback.

Table 12. Stream Mode Autoreset

| STREAM_LENGTH_KEEP_VALUE | STREAM_MODE Register |
|--------------------------|----------------------|
| 0                        | Autoreset            |
| 1                        | Keeps previous value |

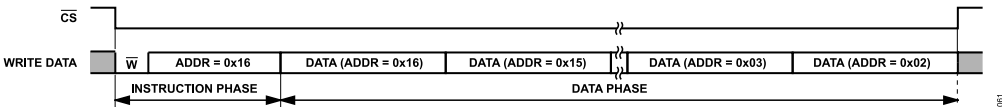


Figure 75. Streaming Mode Register Write with Address Descending

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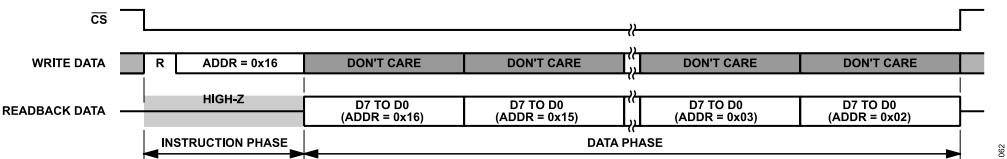


Figure 76. Streaming Mode Register Read with Address Descending

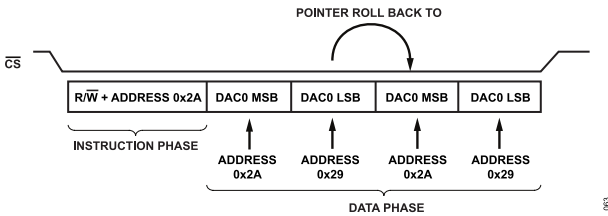


Figure 77. Looping Enabled with Address Descending and  $STREAM\_MODE = 2$

## THEORY OF OPERATION

## CRC Error Detection

The AD3552R features an optional CRC to provide error detection for SPI transactions between the digital host (master) and the AD3552R (slave).

CRC error detection allows SPI masters and slaves to detect bit transfer errors with significant reliability. The CRC algorithm involves using a seed value and polynomial division to generate a CRC code. The master and slave both calculate the CRC code independently and compare it to determine the validity of the transferred data.

The AD3552R uses the CRC-8 standard with the following polynomial:

$$x^8 + x^2 + x + 1 \quad (2)$$

CRC error detection is enabled with the `CRC_EN` and `CRC_EN_B` bits in the `INTERFACE_CONFIG_C` register. The value of `CRC_EN` is only updated if `CRC_EN_B` is set to the `CRC_EN` inverted value in the same register write instruction. Therefore, to enable the CRC, `CRC_EN` must be set to 0b01 while `CRC_EN_B` is set to 0b10 in the same write transaction.

To disable the CRC, `CRC_ENABLE` must be set to 0b00 while `CRC_ENABLE_B` is set to 0b11 in the same write transaction. Writing inverted values to two separate fields reduces the chances of CRC being enabled by mistake.  $\overline{CS}$  must be brought high at the end of the enable or disable write. The transaction following the enabling of the CRC must already include the CRC byte, regardless if it is a write or read operation. A register write transaction that disables CRC must still include the CRC code at the end, but the transaction following the disabling of the CRC does not have to include the CRC byte.

Figure 78 and Figure 79 show how a CRC code is appended at the end of a write or read transaction, respectively, in single SPI mode (classic mode). For register writes, the digital host must generate the CRC by performing the calculation described in Equation 2 on the seed, the address, and the data. The AD3552R performs the

same calculation and shifts out the CRC code on SDO at the same time as the host. The transaction is free of error if both CRC codes match. For register reads, the host calculates the CRC on the seed, the address, and a zero padding while the AD3552R calculates the CRC on the seed, the address, and the readout data. Both nodes then shift out the CRC code at the same time so that it can be checked on both sides.

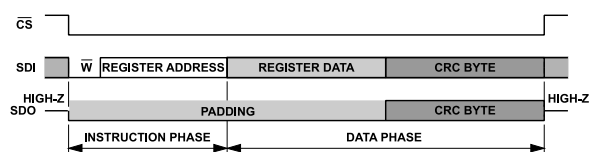


Figure 78. Basic SPI Write Frame with CRC

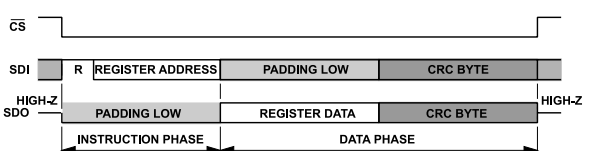


Figure 79. Basic SPI Read Frame with CRC

When accessing multibyte registers with CRC error detection enabled, the CRC code is placed after all of the bytes of register data.

When CRC error detection is enabled, the AD3552R does not update its register contents in response to a register write transaction unless it receives a valid CRC code at the end of the register data. If the CRC code is invalid, or if the digital host fails to transmit the CRC code, the AD3552R does not update its register contents, and the `INVALID_OR_NO_CRC` flag in the `INTERFACE_STATUS_A` register is set. The `INVALID_OR_NO_CRC` flag is cleared when 1 is written to this bit, and the correct CRC is required for the write to clear the bit to take effect.

Table 13 shows the seed value used in the CRC code calculation and how it is calculated for both single instruction mode and streaming mode.

Table 13. CRC Seed Values and Extent of CRC Calculation

| SPI Transaction Type | Pin | Single Instruction Mode             | Streaming Mode, First Data Phase    | Streaming Mode, Subsequent Data Phases        |
|----------------------|-----|-------------------------------------|-------------------------------------|-----------------------------------------------|
| Read                 | SDI | 0xA5, instruction phase, padding    | 0xA5, instruction phase, padding    | No CRC sent                                   |
|                      | SDO | 0xA5, instruction phase, read data  | 0xA5, instruction phase, read data  | Least significant byte of address, read data  |
| Write                | SDI | 0xA5, instruction phase, write data | 0xA5, instruction phase, write data | Least significant byte of address, write data |
|                      | SDO | 0xA5, instruction phase, write data | 0xA5, instruction phase, write data | Least significant byte of address, write data |

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When using single instruction mode, every CRC code in an SPI frame uses 0xA5 as the seed value to prevent stuck at fault conditions for Address 0x00.

When using streaming mode, the first CRC code in an SPI frame also uses 0xA5 as the seed value, but subsequent CRC codes in the same frame are calculated using the least significant byte of the register address being accessed in the SPI transaction as the seed value.

Because enabling the CRC in single SPI (classic) mode requires that the SDO pin shifts out the CRC calculated by the AD3552R,

the transaction must respect the limitations of a read operation, which is that DDR is disabled. CRC is not allowed in synchronous dual SPI mode.

In dual and quad SPI modes, the CRC is appended at the end of the byte or multibyte register transaction but the CRC is generated only by the controller (write) or by the AD3552R (read), as shown in [Figure 80](#) and [Figure 81](#).

When CRC error detection is enabled, do not use streaming mode, including looping, if the range of registers being addressed includes unused or reserved registers.

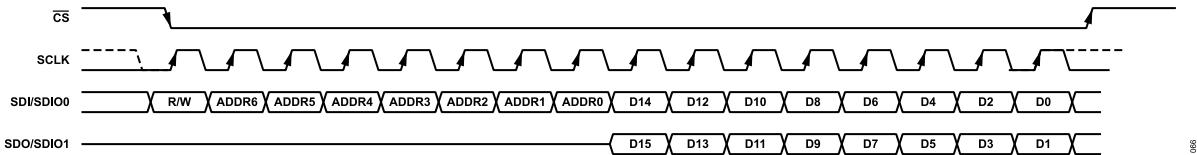


Figure 80. Dual SPI Transaction with CRC

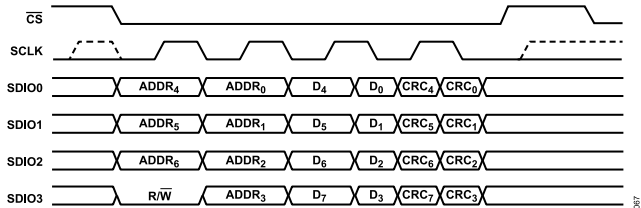


Figure 81. Quad SPI Transaction with CRC

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SERIAL INTERFACE

The AD3552R implements a versatile serial interface that is compatible with several SPI modes. When the QSPI pin is tied low, the interface is configured in single SPI (classic SPI) mode by default and can be switched to dual SPI or synchronous dual SPI mode by acting on the configuration registers. When the QSPI pin is pulled high, the interface is configured in quad SPI mode. DDR can be enabled in any of the modes to duplicate the transfer speed in the data phase.

Clock polarity (CPOL) can be 1 or 0, but clock phase (CPHA) must be always 0. These combinations correspond to SPI Mode 0 and Mode 3, which are applicable when the SPI interface is in single data rate (SDR) mode.

Single SPI (Classic) Mode

In single SPI (classic) mode, the SDI/SDIO0 and SDO/SDIO1 data lines are unidirectional. The SDI signal behaves as an input to transfer data from master to slave and the SDO signal behaves as an output to transfer data from slave to master, as shown in Figure 82. Single SPI (classic) mode is compatible with SPI Mode 0 and Mode 3, as well as with completely synchronous interfaces, such as synchronous serial port (SPORT™). See Figure 2 for a timing diagram of a typical write sequence. See the AN-1248 Application Note, SPI Interface, for more information about the classic SPI mode.

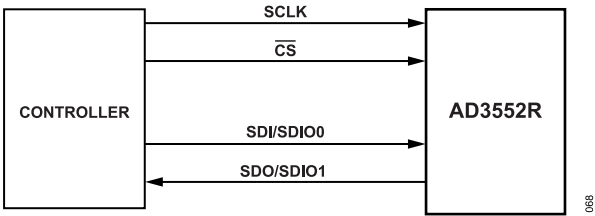


Figure 82. Single SPI (Classic SPI) Connection

Dual SPI Mode

In dual SPI mode, the SDI/SDIO0 and SDO/SDIO1 data lines are bidirectional, as shown in Figure 83. During the data phase, the R/W bit of the instruction phase defines the direction of the data lines. During the instruction phase, the data lines are always configured as inputs. In dual SPI mode, consecutive bits are serialized in groups of two, as shown in Figure 84.

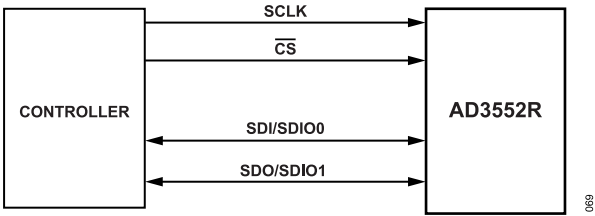


Figure 83. Dual SPI Connection

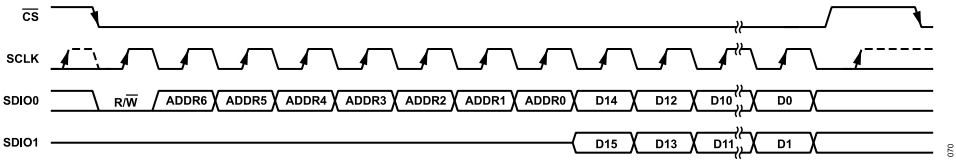


Figure 84. Dual SPI Mode

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Synchronous Dual SPI Mode

In synchronous dual SPI mode, similar to dual SPI mode, the SDI/SDIO0 and SDO/SDIO1 data lines are bidirectional, as shown in Figure 83. During the data phase, the  $R/\overline{W}$  bit of the instruction phase defines the direction of the data lines. During the instruction phase, the data lines are always configured as inputs. In contrast to dual SPI mode, in synchronous dual SPI mode each SDIO line serializes the data of one DAC, as shown in Figure 85.

In this mode, the data transferred on the SDIO0 line is loaded to the register addressed in the instruction phase, while the data transferred on the SDIO1 line is loaded to the register at the address given in the instruction phase that is incremented by 3

bytes in precision mode or the address given in the instruction phase that is incremented by 2 bytes in fast mode.

Synchronous dual SPI mode can only be used to write the CHx\_DAC\_16B, CHx\_DAC\_24B, CHx\_INPUT\_16B, and CHx\_INPUT\_24B registers. To write other registers within the secondary region, classic SPI must be used.

This transfer mode is useful when the controller is made up of two entities, each one addressing one DAC with a single bit stream, or when the CPU cannot serialize the data in groups of two bits. This mode also allows the simultaneous update of both channels without any time skew when the  $\overline{LDAC}$  signal is not used.

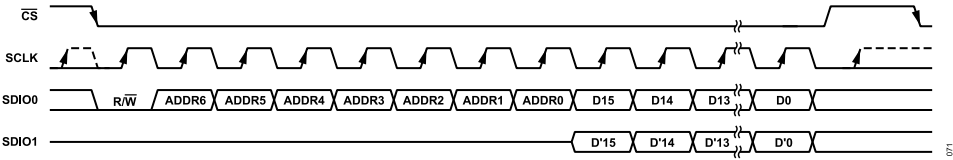


Figure 85. Synchronous Dual SPI Mode

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## Quad SPI Mode

In quad SPI mode, the SDI/SDIO0, SDO/SDIO1, SDIO2, and SDIO3 data lines are bidirectional, as shown in Figure 86. During the data phase, the R/W bit of the instruction phase defines the direction of the data lines. During the instruction phase, the data lines are always configured as inputs. In quad SPI mode, consecutive bits are serialized in groups of four, as shown in Figure 87.

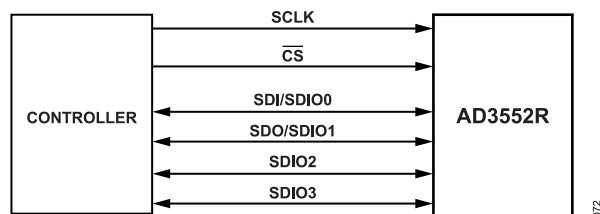


Figure 86. Quad SPI Connection

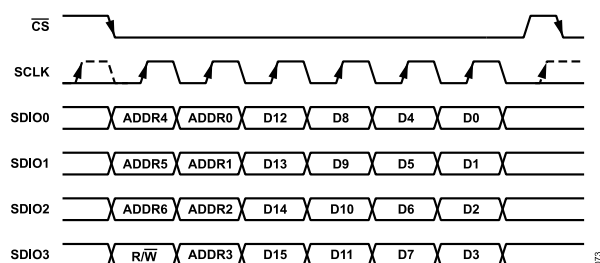


Figure 87. Quad SPI Mode

## Double Data Rate (DDR)

Irrespective of the SPI mode being used, DDR can be enabled by setting the SPI\_CONFIG\_DDR bit in the INTERFACE\_CONFIG\_D register, which allows sampling data during the data phase on both clock edges, as shown in Figure 88. After this mode is enabled, all data must be written using DDR.

DDR is only usable in the data phase during write operations. In readback operations, the SPI\_CONFIG\_DDR bit is ignored, and data is transferred from the AD3552R to the controller in single data rate, as shown in Figure 2, Figure 6, and Figure 10.

After changing the SPI mode or the SPI\_CONFIG\_DDR bit, CS must be brought high and a new access cycle must be started in the appropriate mode.

All valid SPI mode combinations are listed in Table 14.

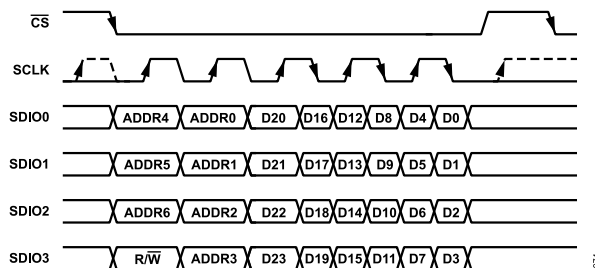


Figure 88. Quad SPI Mode DDR on a 24-Bit Register

Table 14. SPI Mode Combinations

| SPI Mode                  | MULTI_IO_MODE  | DUAL_SPI_SYNCHRONOUS_EN | SPI_CONFIG_DDR |
|---------------------------|----------------|-------------------------|----------------|
| Single SPI SDR            | 00             | 0                       | 0              |
| Single SPI DDR            | 00             | 0                       | 1              |
| Dual SPI SDR              | 01             | 0                       | 0              |
| Dual SPI DDR              | 01             | 0                       | 1              |
| Synchronous Dual SPI SDR  | 01             | 1                       | 0              |
| Synchronous Dual SPI DDR  | 01             | 1                       | 1              |
| Quad SPI SDR <sup>1</sup> | Not applicable | 0                       | 0              |
| Quad SPI DDR <sup>1</sup> | Not applicable | 0                       | 1              |

<sup>1</sup> Enabled by the QSPI pin only.

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### Register Map SPI Access Modes

The register map is divided in two regions, primary and secondary.

The registers related to interface configuration, DAC configuration, and error flags are comprised in the primary region from Address 0x0 to Address 0x1E. If the QSPI pin is low, this region can only be accessed in classic SPI mode with or without DDR, regardless of the value of MULTI\_IO\_MODE in the TRANSFER\_REGISTER.

The registers affecting the output value of the DAC are comprised in the secondary region from Address 0x28 to Address 0x4B. This region can be accessed in any of the SPI modes, with or without DDR.

If the QSPI pin is high, the interface is configured in full quad SPI mode for any communication to primary or secondary region registers.

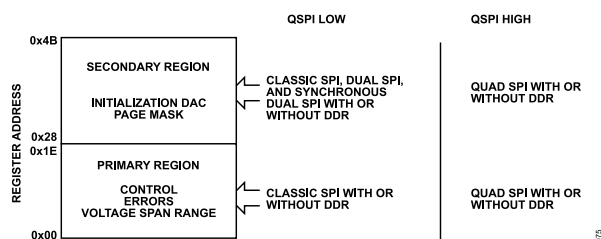


Figure 89. Register Access Modes

### SDIO Drive Strength

The driving strength of the SDIO lines on the SDIO3, SDIO2, SDO/SDIO1, and SDI/SDIO0 pins can be configured to four different levels by setting the SDIO\_DRIVE\_STRENGTH bits in the INTERFACE\_CONFIG\_D register.

Higher drive strength value corresponds to a faster signal slew rate, as shown in Figure 90. However, higher slew rate means higher peak current and higher digital noise in the system. The default value is medium low strength.

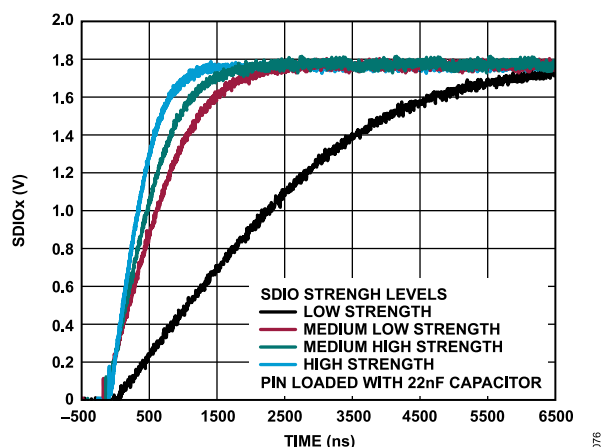


Figure 90. Driving Strength Options

### DAC UPDATE MODES

There are several ways to update the DAC outputs, synchronously or asynchronously, simultaneously, or individually.

A synchronous update occurs when the change of the DAC output is triggered by an external signal, such as  $\overline{\text{LDAC}}$ , which can be common to many devices. In this case, the controller loads a value in the input register that is later transferred to the DAC register on the falling edge of the  $\overline{\text{LDAC}}$  signal, causing the simultaneous update of all  $V_{\text{OUTX}}$  signals.

If the synchronous update is only required in one of the DACs, the  $\overline{\text{LDAC}}$  signal can be masked using the HW\_LDAC\_MASK\_CHx bits in the HW\_LDAC\_16B or the HW\_LDAC\_24B registers depending on the precision mode.

An asynchronous update occurs when the change of the DAC output follows an operation on the register set. In this case, the change is aligned with the SCLK edge that shifts the last register bit in. The update can be on one DAC or both DACs simultaneously following the several combinations described in Table 15.

Page mask registers can be used to transfer the same data to one or both channels, according to the value of the SEL\_CHx bits in the CH\_SELECT\_16B or CH\_SELECT\_24B registers. Writing to the DAC\_PAGE register transfers the data to the CHx\_DAC registers and writing to the INPUT\_PAGE register transfers the data to the CHx\_INPUT registers. The data flow between registers is summarized in Figure 91.

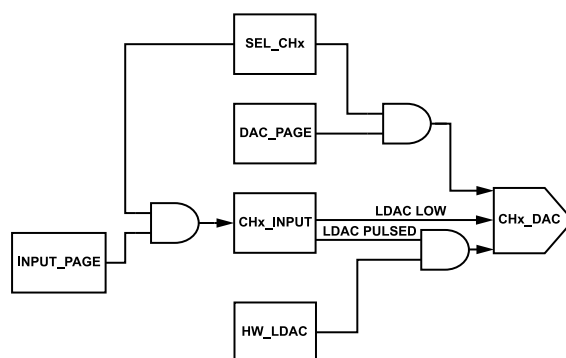


Figure 91. DAC Data Flow Between Registers

## THEORY OF OPERATION

Table 15. DAC Update Modes

| SPI Mode                  | Register Written | LDAC Pin       | Synchronous | Simultaneous | Notes                                                                                                                              |
|---------------------------|------------------|----------------|-------------|--------------|------------------------------------------------------------------------------------------------------------------------------------|
| Quad, Dual and Single SPI | CHx_INPUT        | Falling edge   | Yes         | Yes          | No $\overline{\text{LDAC}}$ mask applied                                                                                           |
| Quad, Dual and Single SPI | CHx_INPUT        | Falling edge   | Yes         | No           | $\overline{\text{LDAC}}$ mask applied, HW_LDAC register                                                                            |
| Quad, Dual and Single SPI | CHx_INPUT        | High           | No          | Yes          | Write to SW_LDAC triggers the update                                                                                               |
| Quad, Dual and Single SPI | CHx_INPUT        | Low            | No          | No           | Output updates automatically                                                                                                       |
| Quad, Dual and Single SPI | CHx_DAC          | Not applicable | No          | No           | Output updates immediately                                                                                                         |
| Quad, Dual and Single SPI | DAC_PAGE         | Not applicable | No          | Yes          | Same data written to the DAC registers selected using the SEL_CHx bits in the CH_SELECT_16B register or the CH_SELECT_24B register |
| Quad, Dual and Single SPI | INPUT_PAGE       | Not applicable | No          | No           | Same data written to input registers selected using the SEL_CHx bits in the CH_SELECT_16B register or the CH_SELECT_24B register   |
| Synchronous SPI           | CHx_INPUT        | Falling edge   | Yes         | Yes          | No $\overline{\text{LDAC}}$ mask applied                                                                                           |
| Synchronous SPI           | CHx_INPUT        | Falling edge   | Yes         | No           | $\overline{\text{LDAC}}$ mask applied, HW_LDAC register                                                                            |
| Synchronous SPI           | CHx_INPUT        | Low            | No          | Yes          | No $\overline{\text{LDAC}}$ mask applied                                                                                           |
| Synchronous SPI           | CHx_DAC          | Not applicable | No          | Yes          | Output updates immediately                                                                                                         |

## POWER-DOWN

Each of the two DAC cores in the AD3552R can be disabled to reduce power consumption when the channel is not in use. Control is performed using the CHx\_DAC\_POWERDOWN bits in the POWERDOWN\_CONFIG register. The DAC core is powered down after reset and becomes active on the first update.

## RESET

The AD3552R implements three different ways to reset the device. All three methods trigger the same reset procedure internally, except for the difference explained in the [Software Reset](#) section.

## Power-On Reset

The device integrates a power-on reset (POR) circuit that monitors  $\text{AV}_{\text{DD}}$  and  $\text{DV}_{\text{DD}}$ . Whenever  $\text{AV}_{\text{DD}}$  falls below 4 V or  $\text{DV}_{\text{DD}}$  falls below 1.3 V, an internal reset pulse is generated. This circuit ensures that the chip is correctly initialized at power-up or after a power dip.

## Reset Pin

A low level on the  $\overline{\text{RESET}}$  pin sets the chip in default mode, clearing the values of all registers, setting the  $\text{I}_{\text{OUT}x}$  and  $\text{V}_{\text{CM}x}$  outputs to 0 V, and keeping the SPI lines in high impedance. When the  $\overline{\text{RESET}}$  line is released (returns high), the device starts executing the initialization procedure that can take up to 100 ms ( $t_{18}$  time). After reset, the DAC core is in power-down mode and the  $\text{I}_{\text{OUT}x}$  and  $\text{V}_{\text{CM}x}$  outputs are still at 0 V.

During reset, the external transimpedance amplifier is still powered up and it may produce some glitch in the  $\text{V}_{\text{OUT}}$  signal, depending on the sequencing of the supplies.

## Software Reset

The device can be reset from the SPI interface by setting the SW\_RESET\_MSB and SW\_RESET\_LSB bits in the INTERFACE\_CONFIG\_A register. The main difference between the software reset and the hardware reset using the  $\overline{\text{RESET}}$  pin is that the former does not affect the INTERFACE\_CONFIG\_A register. The SW\_RESET\_MSB and SW\_RESET\_LSB bits clear after the reset operation has concluded.

## ERROR DETECTION

The AD3552R can detect abnormal conditions both in the analog and digital domains. These errors are reported in the INTERFACE\_STATUS\_A and ERR\_STATUS registers. The list of the errors mapped to the ERR\_ALARM\_MASK register and its corresponding source is shown in [Table 16](#). The errors listed in [Table 16](#) can assert the  $\overline{\text{ALERT}}$  pin if it is not masked in the ERR\_ALARM\_MASK register. The  $\overline{\text{ALERT}}$  pin is also asserted after reset and in case of initialization failure.

The error bits in the INTERFACE\_STATUS\_A and ERR\_STATUS registers are sticky and keep their value until cleared with a write 1 operation. That is, to clear an error bit, write 1 on that specific bit location.

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Table 16. Alarm Mask Register and Corresponding Error Source

| Bit Number | Alarm Mask Register Bit Name        | Error Source Register Name | Error Source Bit Name       |
|------------|-------------------------------------|----------------------------|-----------------------------|
| 6          | REF_RANGE_ALARM_MASK                | ERR_STATUS                 | REF_RANGE_ERR_STATUS        |
| 5          | CLOCK_COUNT_ALARM_MASK              | INTERFACE_STATUS_A         | CLOCK_COUNTING_ERROR        |
| 4          | MEM_CRC_ALARM_MASK                  | ERR_STATUS                 | MEM_CRC_ERR_STATUS          |
| 3          | SPI_CRC_ERR_ALARM_MASK              | INTERFACE_STATUS_A         | INVALID_OR_NO_CRC           |
| 2          | WRITE_TO_READ_ONLY_ALARM_MASK       | INTERFACE_STATUS_A         | WRITE_TO_READ_ONLY_REGISTER |
| 1          | PARTIAL_REGISTER_ACCESS_ALARM_MASK  | INTERFACE_STATUS_A         | PARTIAL_REGISTER_ACCESS     |
| 0          | REGISTER_ADDRESS_INVALID_ALARM_MASK | INTERFACE_STATUS_A         | REGISTER_ADDRESS_INVALID    |

## ERR\_STATUS Register

V<sub>REF</sub> Detection

The REF\_RANGE\_ERR\_STATUS bit in the ERR\_STATUS register is set when the reference voltage drops below 1 V for more than 5 ms. The error is detected irrespective of the reference voltage source, whether it is generated internally or provided externally via the V<sub>REF</sub> pin. This feature is useful to detect an interruption in the external reference voltage or an overload condition on the V<sub>REF</sub> pin when the internal reference is shared with another device.

## SPI Mode Error

The SPI mode error is produced during streaming when the address pointer crosses the boundary between the secondary and the primary region with the SPI interface configured in synchronous dual SPI mode or dual SPI mode because this region can only be accessed in quad SPI mode or classic SPI mode. The DUAL\_SPI\_STREAM\_EXCEEDS\_DAC\_ERR\_STATUS bit is set in the ERR\_STATUS register.

## Register CRC

The AD3552R includes an internal CRC for the register map and the read only memory (ROM). The CRC is executed every 4.1 μs, and only includes the primary region of the register map because the secondary region is expected to be continuously written. The CRC can be disabled by clearing the MEM\_CRC\_EN bit in the INTERFACE\_CONFIG\_D register. If a CRC error is detected, the MEM\_CRC\_ERR\_STATUS bit is set in the ERR\_STATUS register. It is advisable to reset the device if this error occurs.

## Reset Status

The RESET\_STATUS bit in the ERR\_STATUS register indicates that the AD3552R has been reset, either internally (POR or SW reset) or externally (via the RESET pin). The RESET\_STATUS bit is set when the POR completes correctly. It is useful to detect unexpected reset conditions, such as a dip in power supply, and take corrective actions.

The RESET\_STATUS bit causes the assertion of the ALERT pin and it is not maskable. Therefore, it must be cleared after reset or power-up to be able to detect new events via the ALERT signal.

## INTERFACE\_STATUS\_A Register

## Device Busy

The INTERFACE\_NOT\_READY bit in the INTERFACE\_STATUS\_A register is not an error, but a status bit. This bit can be polled to know when the device is ready to receive data from the controller.

## SPI Clock Counter

The error reported in the CLOCK\_COUNTING\_ERR bit is produced when the number of SCLK cycles is not in accordance with the amount required to shift a multiple of 8 bits, taking into account the SPI mode (quad, dual, or single) and the DDR mode. The CLOCK\_COUNTING\_ERR bit is set in the ERR\_STATUS register.

Valid combinations are shown in Table 17.

Table 17. Clock Cycles Required to Transfer One Byte

| SPI Mode   | DDR | Clock Cycles for 1 Byte |
|------------|-----|-------------------------|
| Single SPI | No  | 8                       |
| Single SPI | Yes | 4                       |
| Dual SPI   | No  | 4                       |
| Dual SPI   | Yes | 2                       |
| Quad SPI   | No  | 2                       |
| Quad SPI   | Yes | 1                       |

## SPI CRC

The INVALID\_OR\_NO\_CRC bit in the INTERFACE\_STATUS\_A register is set when the CRC is enabled and the CRC byte in the SPI transaction is missing or it does not match the calculated value. To clear this error, write 1 to this bit. Note that because CRC is enabled, this SPI transaction must have a valid CRC code to succeed.

## Write to Read Only Register

If the host tries to write to a read only register, the WRITE\_TO\_READ\_ONLY\_REGISTER bit field is asserted in the INTERFACE\_STATUS\_A register. To clear this error, write 1 to the WRITE\_TO\_READ\_ONLY\_REGISTER bit.



## THEORY OF OPERATION

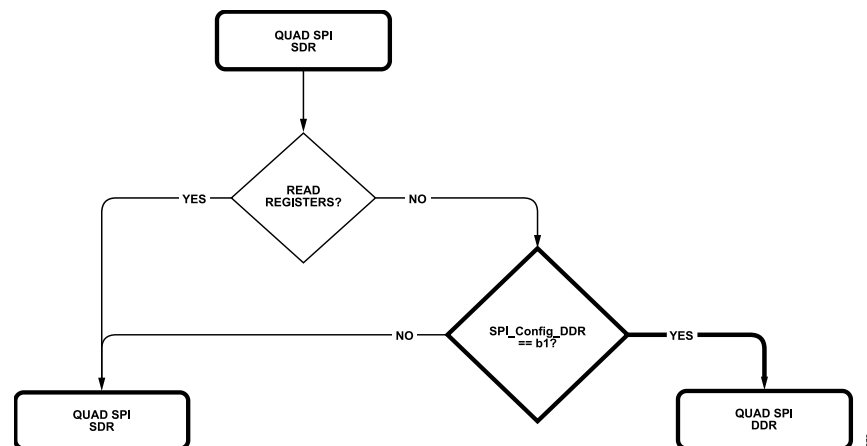


Figure 93. Register Access Modes when QSPI Pin is High

## REGISTERS

## REGISTER SUMMARY

## Register List

Table 18. Register Summary

| Address | Name                 | Description                                        | Reset    | Access |
|---------|----------------------|----------------------------------------------------|----------|--------|
| 0x00    | INTERFACE_CONFIG_A   | Interface Configuration A Register.                | 0x10     | R/W    |
| 0x01    | INTERFACE_CONFIG_B   | Interface Configuration B Register.                | 0x08     | R/W    |
| 0x02    | DEVICE_CONFIG        | Device Configuration Register.                     | 0x00     | R      |
| 0x03    | CHIP_TYPE            | Chip Type Register.                                | 0x04     | R      |
| 0x04    | PRODUCT_ID_L         | Product ID Low Register.                           | 0x08     | R      |
| 0x05    | PRODUCT_ID_H         | Product ID High Register.                          | 0x40     | R      |
| 0x06    | CHIP_GRADE           | Chip Grade Register.                               | 0x05     | R      |
| 0x0A    | SCRATCH_PAD          | Scratch Pad Register.                              | 0x00     | R/W    |
| 0x0B    | SPI_REVISION         | SPI Revision Register.                             | 0x83     | R      |
| 0x0C    | VENDOR_L             | Vendor ID Low Register.                            | 0x56     | R      |
| 0x0D    | VENDOR_H             | Vendor ID High Register.                           | 0x04     | R      |
| 0x0E    | STREAM_MODE          | Stream Mode Register.                              | 0x00     | R/W    |
| 0x0F    | TRANSFER_REGISTER    | Transfer Configuration Register.                   | 0x00     | R/W    |
| 0x10    | INTERFACE_CONFIG_C   | Interface Configuration C Register.                | 0x23     | R/W    |
| 0x11    | INTERFACE_STATUS_A   | Interface Status A Register.                       | 0x00     | R/W    |
| 0x14    | INTERFACE_CONFIG_D   | Interface Configuration D Register.                | 0x04     | R/W    |
| 0x15    | REFERENCE_CONFIG     | Reference Configuration Register.                  | 0x00     | R/W    |
| 0x16    | ERR_ALARM_MASK       | Error Alarm Mask Register.                         | 0x00     | R/W    |
| 0x17    | ERR_STATUS           | Error Status Register.                             | 0x01     | R/W    |
| 0x18    | POWERDOWN_CONFIG     | Power-Down Configuration Register.                 | 0x00     | R/W    |
| 0x19    | CH0_CH1_OUTPUT_RANGE | Output Range Register.                             | 0x00     | R/W    |
| 0x1B    | CH0_OFFSET           | Channel 0 Offset Register.                         | 0x00     | R/W    |
| 0x1C    | CH0_GAIN             | Channel 0 Gain Register.                           | 0x00     | R/W    |
| 0x1D    | CH1_OFFSET           | Channel 1 Offset Register.                         | 0x00     | R/W    |
| 0x1E    | CH1_GAIN             | Channel 1 Gain Register.                           | 0x00     | R/W    |
| 0x28    | HW_LDAC_16B          | Hardware LDAC Mask Register, Fast Mode.            | 0x00     | R/W    |
| 0x29    | CH0_DAC_16B          | DAC Register for Channel 0, Fast Mode.             | 0x0000   | R/W    |
| 0x2B    | CH1_DAC_16B          | DAC Register for Channel 1, Fast Mode.             | 0x0000   | R/W    |
| 0x2D    | DAC_PAGE_16B         | DAC Page Register, Fast Mode.                      | 0x0000   | R/W    |
| 0x2F    | CH_SELECT_16B        | Channel Select for Page Registers, Fast Mode.      | 0x00     | R/W    |
| 0x30    | INPUT_PAGE_16B       | Input Page Register, Fast Mode.                    | 0x0000   | R/W    |
| 0x32    | SW_LDAC_16B          | Software LDAC Register, Fast Mode.                 | 0x00     | W      |
| 0x33    | CH0_INPUT_16B        | Input Register for Channel 0, Fast Mode.           | 0x0000   | R/W    |
| 0x35    | CH1_INPUT_16B        | Input Register for Channel 1, Fast Mode.           | 0x0000   | R/W    |
| 0x37    | HW_LDAC_24B          | Hardware LDAC Mask Register, Precision Mode.       | 0x00     | R/W    |
| 0x38    | CH0_DAC_24B          | DAC Register for Channel 0, Precision Mode.        | 0x000000 | R/W    |
| 0x3B    | CH1_DAC_24B          | DAC Register for Channel 1, Precision Mode.        | 0x000000 | R/W    |
| 0x3E    | DAC_PAGE_24B         | DAC Page Register, Precision Mode.                 | 0x000000 | R/W    |
| 0x41    | CH_SELECT_24B        | Channel Select for Page Registers, Precision Mode. | 0x00     | R/W    |
| 0x42    | INPUT_PAGE_24B       | Input Page Register, Precision Mode.               | 0x000000 | R/W    |
| 0x45    | SW_LDAC_24B          | Software LDAC Register, Precision Mode.            | 0x00     | W      |
| 0x46    | CH0_INPUT_24B        | Input Register for Channel 0, Precision Mode.      | 0x000000 | R/W    |
| 0x49    | CH1_INPUT_24B        | Input Register for Channel 1, Precision Mode.      | 0x000000 | R/W    |

## REGISTERS

## Detailed Register Map

Table 19. Detailed Register Summary

| Reg  | Name                 | Bits  | Bit 7                | Bit 6                | Bit 5                                  | Bit 4                  | Bit 3                  | Bit 2                         | Bit 1                              | Bit 0                               | Reset | RW  |
|------|----------------------|-------|----------------------|----------------------|----------------------------------------|------------------------|------------------------|-------------------------------|------------------------------------|-------------------------------------|-------|-----|
| 0x00 | INTERFACE_CONFIG_A   | [7:0] | SW_RESET_MSB         | RESERVED             | ADDR_DIRECTION                         | SDO_ACTIVE             | RESERVED               |                               |                                    | SW_RESET_LSB                        | 0x10  | R/W |
| 0x01 | INTERFACE_CONFIG_B   | [7:0] | SINGLE_INSTRUCTION   | RESERVED             |                                        |                        | SHORT_INSTRUCTION      | RESERVED                      |                                    |                                     | 0x08  | R/W |
| 0x02 | DEVICE_CONFIG        | [7:0] | DEVICE_STATUS_3      | DEVICE_STATUS_2      | DEVICE_STATUS_1                        | DEVICE_STATUS_0        | CUSTOM_MODES           |                               | OPERATING_MODES                    |                                     | 0x00  | R   |
| 0x03 | CHIP_TYPE            | [7:0] | RESERVED             |                      |                                        |                        | CLASS                  |                               |                                    |                                     | 0x04  | R   |
| 0x04 | PRODUCT_ID_L         | [7:0] | PRODUCT_ID[7:0]      |                      |                                        |                        |                        |                               |                                    |                                     | 0x08  | R   |
| 0x05 | PRODUCT_ID_H         | [7:0] | PRODUCT_ID[15:8]     |                      |                                        |                        |                        |                               |                                    |                                     | 0x40  | R   |
| 0x06 | CHIP_GRADE           | [7:0] | DEVICE_GRADE         |                      |                                        |                        | DEVICE_REVISION        |                               |                                    |                                     | 0x05  | R   |
| 0x0A | SCRATCH_PAD          | [7:0] | VALUE                |                      |                                        |                        |                        |                               |                                    |                                     | 0x00  | R/W |
| 0x0B | SPI_REVISION         | [7:0] | VERSION              |                      |                                        |                        |                        |                               |                                    |                                     | 0x83  | R   |
| 0x0C | VENDOR_L             | [7:0] | VID[7:0]             |                      |                                        |                        |                        |                               |                                    |                                     | 0x56  | R   |
| 0x0D | VENDOR_H             | [7:0] | VID[15:8]            |                      |                                        |                        |                        |                               |                                    |                                     | 0x04  | R   |
| 0x0E | STREAM_MODE          | [7:0] | LENGTH               |                      |                                        |                        |                        |                               |                                    |                                     | 0x00  | R/W |
| 0x0F | TRANSFER_REGISTER    | [7:0] | MULTI_IO_MODE        |                      | RESERVED                               |                        |                        | STREAM_LENGTH_KEEP_VALUE      | RESERVED                           |                                     | 0x00  | R/W |
| 0x10 | INTERFACE_CONFIG_C   | [7:0] | CRC_ENABLE           |                      | STRICT_REGISTER_ACCESS                 | RESERVED               |                        |                               | CRC_ENABLE_B                       |                                     | 0x23  | R/W |
| 0x11 | INTERFACE_STATUS_A   | [7:0] | INTERFACE_NOT_READY  | RESERVED             | CLOCK_COUNTING_ERROR                   | RESERVED               | INVALID_OR_NO_CRC      | WRITE_TO_READ_ONLY_REGISTER   | PARTIAL_REGISTER_ACCESS            | REGISTER_ADDRESS_INVALID            | 0x00  | R/W |
| 0x14 | INTERFACE_CONFIG_D   | [7:0] | RESERVED             | ALERT_ENABLE_PULLUP  | RESERVED                               | MEM_CRC_EN             | SDIO_DRIVE_STRENGTH    |                               | DUAL_SPI_SYNCHRONOUS_EN            | SPI_CONFIG_DDR                      | 0x04  | R/W |
| 0x15 | REFERENCE_CONFIG     | [7:0] | RESERVED             | IDUMP_FASTMODE       | RESERVED                               |                        |                        |                               | REFERENCE_VOLTAGE_SEL              |                                     | 0x00  | R/W |
| 0x16 | ERR_ALARM_MASK       | [7:0] | RESERVED             | REF_RANGE_ALARM_MASK | CLOCK_COUNT_ERR_ALARM_MASK             | MEM_CRC_ERR_ALARM_MASK | SPI_CRC_ERR_ALARM_MASK | WRITE_TO_READ_ONLY_ALARM_MASK | PARTIAL_REGISTER_ACCESS_ALARM_MASK | REGISTER_ADDRESS_INVALID_ALARM_MASK | 0x00  | R/W |
| 0x17 | ERR_STATUS           | [7:0] | RESERVED             | REF_RANGE_ERR_STATUS | DUAL_SPI_STREAM_EXCEEDS_DAC_ERR_STATUS | MEM_CRC_ERR_STATUS     | RESERVED               |                               |                                    | RESET_STATUS                        | 0x01  | R/W |
| 0x18 | POWERDOWN_CONFIG     | [7:0] | RESERVED             |                      | CH1_DAC_POWERDOWN                      | CH0_DAC_POWERDOWN      | RESERVED               |                               |                                    |                                     | 0x00  | R/W |
| 0x19 | CH0_CH1_OUTPUT_RANGE | [7:0] | CH1_OUTPUT_RANGE_SEL |                      |                                        |                        | CH0_OUTPUT_RANGE_SEL   |                               |                                    |                                     | 0x00  | R/W |
| 0x1B | CH0_OFFSET           | [7:0] | CH0_OFFSET           |                      |                                        |                        |                        |                               |                                    |                                     | 0x00  | R/W |
| 0x1C | CH0_GAIN             | [7:0] | CH0_RANGE_OVERRIDE   | CH0_GAIN_SCALING_N   |                                        | CH0_GAIN_SCALING_P     |                        | CH0_OFFSET_POLARITY           | RESERVED                           | CH0_OFFSET[8]                       | 0x00  | R/W |

## REGISTERS

Table 19. Detailed Register Summary (Continued)

| Reg  | Name           | Bits    | Bit 7              | Bit 6              | Bit 5 | Bit 4              | Bit 3 | Bit 2               | Bit 1            | Bit 0            | Reset | RW  |
|------|----------------|---------|--------------------|--------------------|-------|--------------------|-------|---------------------|------------------|------------------|-------|-----|
| 0x1D | CH1_OFFSET     | [7:0]   | CH1_OFFSET         |                    |       |                    |       |                     |                  |                  | 0x00  | R/W |
| 0x1E | CH1_GAIN       | [7:0]   | CH1_RANGE_OVERRIDE | CH1_GAIN_SCALING_N |       | CH1_GAIN_SCALING_P |       | CH1_OFFSET_POLARITY | RESERVED         | CH1_OFFSET[8]    | 0x00  | R/W |
| 0x28 | HW_LDAC_16B    | [7:0]   | RESERVED           |                    |       |                    |       |                     | HW_LDAC_MASK_CH1 | HW_LDAC_MASK_CH0 | 0x00  | R/W |
| 0x2A | CH0_DAC_16B    | [15:8]  | DAC_DATA0[15:8]    |                    |       |                    |       |                     |                  |                  | 0x00  | R/W |
| 0x29 |                | [7:0]   | DAC_DATA0[7:0]     |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x2C | CH1_DAC_16B    | [15:8]  | DAC_DATA1[15:8]    |                    |       |                    |       |                     |                  |                  | 0x00  | R/W |
| 0x2B |                | [7:0]   | DAC_DATA1[7:0]     |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x2E | DAC_PAGE_16B   | [15:8]  | DAC_PAGE[15:8]     |                    |       |                    |       |                     |                  |                  | 0x00  | R/W |
| 0x2D |                | [7:0]   | DAC_PAGE[7:0]      |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x2F | CH_SELECT_16B  | [7:0]   | RESERVED           |                    |       |                    |       |                     | SEL_CH1          | SEL_CH0          | 0x00  | R/W |
| 0x31 | INPUT_PAGE_16B | [15:8]  | INPUT_PAGE[15:8]   |                    |       |                    |       |                     |                  |                  | 0x00  | R/W |
| 0x30 |                | [7:0]   | INPUT_PAGE[7:0]    |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x32 | SW_LDAC_16B    | [7:0]   | RESERVED           |                    |       |                    |       |                     | SW_LDAC_CH1      | SW_LDAC_CH0      | 0x00  | W   |
| 0x34 | CH0_INPUT_16B  | [15:8]  | INPUT_DATA0[15:8]  |                    |       |                    |       |                     |                  |                  | 0x00  | R/W |
| 0x33 |                | [7:0]   | INPUT_DATA0[7:0]   |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x36 | CH1_INPUT_16B  | [15:8]  | INPUT_DATA1[15:8]  |                    |       |                    |       |                     |                  |                  | 0x00  | R/W |
| 0x35 |                | [7:0]   | INPUT_DATA1[7:0]   |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x37 | HW_LDAC_24B    | [7:0]   | RESERVED           |                    |       |                    |       |                     | HW_LDAC_MASK_CH1 | HW_LDAC_MASK_CH0 | 0x00  | R/W |
| 0x3A | CH0_DAC_24B    | [23:16] | DAC_DATA0[15:8]    |                    |       |                    |       |                     |                  |                  | 0x00  | R/W |
| 0x39 |                | [15:8]  | DAC_DATA0[7:0]     |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x38 |                | [7:0]   | RESERVED           |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x3D | CH1_DAC_24B    | [23:16] | DAC_DATA1[15:8]    |                    |       |                    |       |                     |                  |                  | 0x00  | R/W |
| 0x3C |                | [15:8]  | DAC_DATA1[7:0]     |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x3B |                | [7:0]   | RESERVED           |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x40 | DAC_PAGE_24B   | [23:16] | DAC_PAGE[15:8]     |                    |       |                    |       |                     |                  |                  | 0x00  | R/W |
| 0x3F |                | [15:8]  | DAC_PAGE[7:0]      |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x3E |                | [7:0]   | RESERVED           |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x41 | CH_SELECT_24B  | [7:0]   | RESERVED           |                    |       |                    |       |                     | SEL_CH1          | SEL_CH0          | 0x00  | R/W |
| 0x44 | INPUT_PAGE_24B | [23:16] | INPUT_PAGE[15:8]   |                    |       |                    |       |                     |                  |                  | 0x00  | R/W |
| 0x43 |                | [15:8]  | INPUT_PAGE[7:0]    |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x42 |                | [7:0]   | RESERVED           |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x45 | SW_LDAC_24B    | [7:0]   | RESERVED           |                    |       |                    |       |                     | SW_LDAC_CH1      | SW_LDAC_CH0      | 0x00  | W   |
| 0x48 | CH0_INPUT_24B  | [23:16] | INPUT_DATA0[15:8]  |                    |       |                    |       |                     |                  |                  | 0x00  | R/W |
| 0x47 |                | [15:8]  | INPUT_DATA0[7:0]   |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x46 |                | [7:0]   | RESERVED           |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x4B | CH1_INPUT_24B  | [23:16] | INPUT_DATA1[15:8]  |                    |       |                    |       |                     |                  |                  | 0x00  | R/W |
| 0x4A |                | [15:8]  | INPUT_DATA1[7:0]   |                    |       |                    |       |                     |                  |                  | 0x00  |     |
| 0x49 |                | [7:0]   | RESERVED           |                    |       |                    |       |                     |                  |                  | 0x00  |     |

## REGISTERS

## INTERFACE REGISTER DETAILS

## Interface Configuration A Register

Address: 0x00, Reset: 0x10, Name: INTERFACE\_CONFIG\_A

Interface configuration settings.

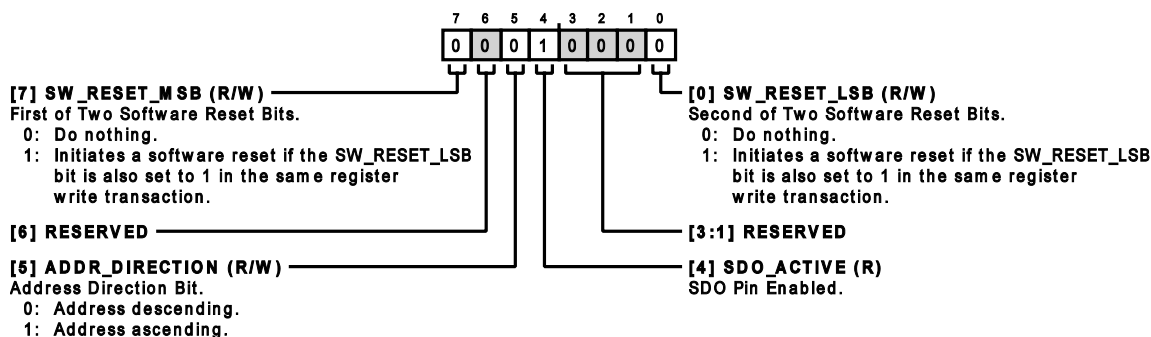


Table 20. Bit Descriptions for INTERFACE\_CONFIG\_A

| Bits  | Bit Name       | Settings | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Reset | Access |
|-------|----------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 7     | SW_RESET_MSB   |          | First of Two Software Reset Bits. Setting both software reset bits (SW_RESET_MSB and SW_RESET_LSB) in a single SPI write performs a software device reset, returning all registers (except the INTERFACE_CONFIG_A register) to the default power-up state.<br>0 Do nothing.<br>1 Initiates a software reset if the SW_RESET_LSB bit is also set to 1 in the same register write transaction.                                                                      | 0x0   | R/W    |
| 6     | RESERVED       |          | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 0x0   | R      |
| 5     | ADDR_DIRECTION |          | Address Direction Bit. Determines sequential addressing behavior when performing register reads and writes on multiple bytes of data in a single data phase.<br>0 Address descending. Address accessed is automatically decremented by one for each data byte when streaming or addressing multibyte registers.<br>1 Address ascending. Address accessed is automatically incremented by one for each data byte when streaming or addressing multibyte registers. | 0x0   | R/W    |
| 4     | SDO_ACTIVE     |          | SDO Pin Enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 0x1   | R      |
| [3:1] | RESERVED       |          | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 0x0   | R      |
| 0     | SW_RESET_LSB   |          | Second of Two Software Reset Bits. Setting both software reset bits (SW_RESET_MSB and SW_RESET_LSB) in a single SPI write performs a software device reset, returning all registers (except the INTERFACE_CONFIG_A register) to the default power-up state.<br>0 Do nothing.<br>1 Initiates a software reset if the SW_RESET_LSB bit is also set to 1 in the same register write transaction.                                                                     | 0x0   | R/W    |

## REGISTERS

## Interface Configuration B Register

Address: 0x01, Reset: 0x08, Name: INTERFACE\_CONFIG\_B

Additional interface configuration settings.

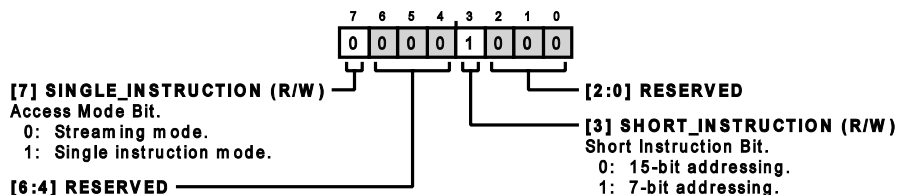


Table 21. Bit Descriptions for INTERFACE\_CONFIG\_B

| Bits  | Bit Name           | Settings | Description                                                                                                                                                                                                                                                                                                                           | Reset | Access |
|-------|--------------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 7     | SINGLE_INSTRUCTION |          | Access Mode Bit. Select streaming mode or single instruction mode.<br>0 Streaming mode. The address increments/decrements as successive data bytes are received according to the ADDR_DIRECTION bit setting in the INTERFACE_CONFIG_A register and the LENGTH bits setting in the STREAM_MODE register.<br>1 Single instruction mode. | 0x0   | R/W    |
| [6:4] | RESERVED           |          | Reserved.                                                                                                                                                                                                                                                                                                                             | 0x0   | R      |
| 3     | SHORT_INSTRUCTION  |          | Short Instruction Bit. Sets the length of the address in the instruction phase to 7 bits or 15 bits.<br>0 15-bit addressing.<br>1 7-bit addressing.                                                                                                                                                                                   | 0x1   | R/W    |
| [2:0] | RESERVED           |          | Reserved.                                                                                                                                                                                                                                                                                                                             | 0x0   | R      |

## Device Configuration Register

Address: 0x02, Reset: 0x00, Name: DEVICE\_CONFIG

This register is intended for compatibility with the standardized register map and it has no effect on this device.

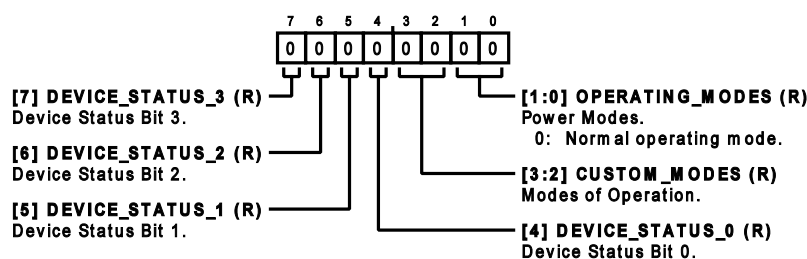


Table 22. Bit Descriptions for DEVICE\_CONFIG

| Bits  | Bit Name        | Settings | Description                              | Reset | Access |
|-------|-----------------|----------|------------------------------------------|-------|--------|
| 7     | DEVICE_STATUS_3 |          | Device Status Bit 3.                     | 0x0   | R      |
| 6     | DEVICE_STATUS_2 |          | Device Status Bit 2.                     | 0x0   | R      |
| 5     | DEVICE_STATUS_1 |          | Device Status Bit 1.                     | 0x0   | R      |
| 4     | DEVICE_STATUS_0 |          | Device Status Bit 0.                     | 0x0   | R      |
| [3:2] | CUSTOM_MODES    |          | Modes of Operation.                      | 0x0   | R      |
| [1:0] | OPERATING_MODES |          | Power Modes.<br>0 Normal operating mode. | 0x0   | R      |

# REGISTERS

## Chip Type Register

Address: 0x03, Reset: 0x04, Name: CHIP\_TYPE

The chip type register contains the identifier of the precision DAC family, which includes the AD3552R. This register must be used in conjunction with the product ID to uniquely identify the AD3552R.

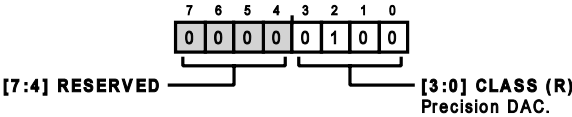


Table 23. Bit Descriptions for CHIP\_TYPE

| Bits  | Bit Name | Settings | Description    | Reset | Access |
|-------|----------|----------|----------------|-------|--------|
| [7:4] | RESERVED |          | Reserved.      | 0x0   | R      |
| [3:0] | CLASS    |          | Precision DAC. | 0x4   | R      |

## Product ID Low Register

Address: 0x04, Reset: 0x08, Name: PRODUCT\_ID\_L

Low byte of the product ID.

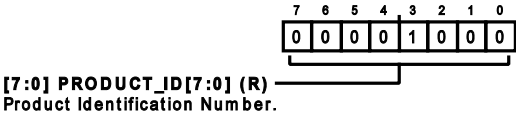


Table 24. Bit Descriptions for PRODUCT\_ID\_L

| Bits  | Bit Name        | Settings | Description                    | Reset | Access |
|-------|-----------------|----------|--------------------------------|-------|--------|
| [7:0] | PRODUCT_ID[7:0] |          | Product Identification Number. | 0x8   | R      |

## Product ID High Register

Address: 0x05, Reset: 0x40, Name: PRODUCT\_ID\_H

High byte of the product ID.

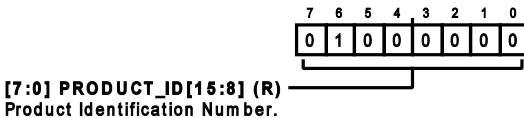


Table 25. Bit Descriptions for PRODUCT\_ID\_H

| Bits  | Bit Name         | Settings | Description                    | Reset | Access |
|-------|------------------|----------|--------------------------------|-------|--------|
| [7:0] | PRODUCT_ID[15:8] |          | Product Identification Number. | 0x40  | R      |

# REGISTERS

## Chip Grade Register

Address: 0x06, Reset: 0x05, Name: CHIP\_GRADE

Identifies product variations and device revisions. The device revision refers to the version of the silicon and the device grade refers to the version of the test procedure.

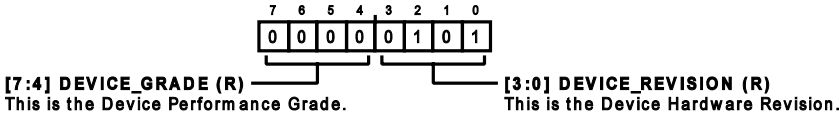


Table 26. Bit Descriptions for CHIP\_GRADE

| Bits  | Bit Name        | Settings | Description                           | Reset | Access |
|-------|-----------------|----------|---------------------------------------|-------|--------|
| [7:4] | DEVICE_GRADE    |          | This is the Device Performance Grade. | 0x0   | R      |
| [3:0] | DEVICE_REVISION |          | This is the Device Hardware Revision. | 0x5   | R      |

## Scratch Pad Register

Address: 0x0A, Reset: 0x00, Name: SCRATCH\_PAD

This register has no functional purpose. It is provided to test write and read operations.

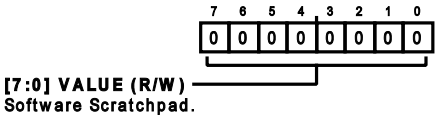


Table 27. Bit Descriptions for SCRATCH\_PAD

| Bits  | Bit Name | Settings | Description          | Reset | Access |
|-------|----------|----------|----------------------|-------|--------|
| [7:0] | VALUE    |          | Software Scratchpad. | 0x0   | R/W    |

## SPI Revision Register

Address: 0x0B, Reset: 0x83, Name: SPI\_REVISION

Indicates the SPI interface revision.

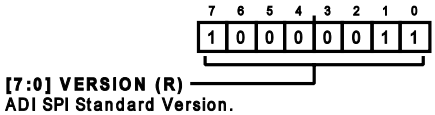


Table 28. Bit Descriptions for SPI\_REVISION

| Bits  | Bit Name | Settings | Description               | Reset | Access |
|-------|----------|----------|---------------------------|-------|--------|
| [7:0] | VERSION  |          | ADI SPI Standard Version. | 0x83  | R      |

# REGISTERS

## Vendor ID Low Register

Address: 0x0C, Reset: 0x56, Name: VENDOR\_L

Low byte of the vendor ID.

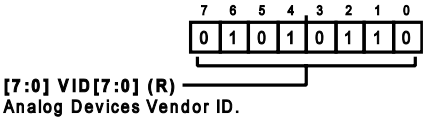


Table 29. Bit Descriptions for VENDOR\_L

| Bits  | Bit Name | Settings | Description               | Reset | Access |
|-------|----------|----------|---------------------------|-------|--------|
| [7:0] | VID[7:0] |          | Analog Devices Vendor ID. | 0x56  | R      |

## Vendor ID High Register

Address: 0x0D, Reset: 0x04, Name: VENDOR\_H

High byte of the vendor ID.

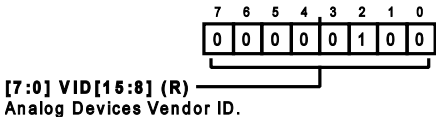


Table 30. Bit Descriptions for VENDOR\_H

| Bits  | Bit Name  | Settings | Description               | Reset | Access |
|-------|-----------|----------|---------------------------|-------|--------|
| [7:0] | VID[15:8] |          | Analog Devices Vendor ID. | 0x4   | R      |

## Stream Mode Register

Address: 0x0E, Reset: 0x00, Name: STREAM\_MODE

Defines the length of the loop when streaming data.

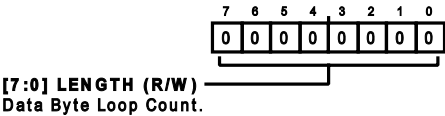


Table 31. Bit Descriptions for STREAM\_MODE

| Bits  | Bit Name | Settings | Description                                                                                                                                                                                                                                                                                                                                                                                                                 | Reset | Access |
|-------|----------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:0] | LENGTH   |          | Data Byte Loop Count. Specifies the data byte count before looping back to the start address. Only valid in streaming mode. A nonzero value sets the number of data bytes written or read before the address loops back to the start address. A maximum of 255 bytes can be transmitted using this approach. A value of 0x00 disables the loopback so that addressing wraps around at the upper and lower limits of memory. | 0x0   | R/W    |

## REGISTERS

## Transfer Configuration Register

Address: 0x0F, Reset: 0x00, Name: TRANSFER\_REGISTER

This register configures the SPI mode used to transfer data and enables looping over the same register section when streaming data.

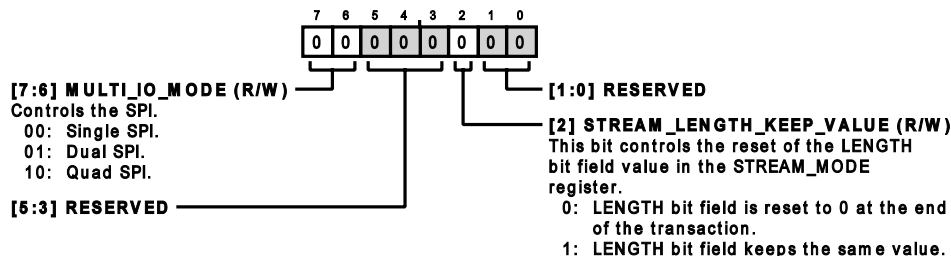


Table 32. Bit Descriptions for TRANSFER\_REGISTER

| Bits  | Bit Name                 | Settings       | Description                                                                                                                                                                                       | Reset | Access |
|-------|--------------------------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:6] | MULTI_IO_MODE            | 00<br>01<br>10 | Controls the SPI.<br>Single SPI.<br>Dual SPI.<br>Quad SPI.                                                                                                                                        | 0x0   | R/W    |
| [5:3] | RESERVED                 |                | Reserved.                                                                                                                                                                                         | 0x0   | R      |
| 2     | STREAM_LENGTH_KEEP_VALUE | 0<br>1         | This bit controls the reset of the LENGTH bit field value in the STREAM_MODE register.<br>LENGTH bit field is reset to 0 at the end of the transaction.<br>LENGTH bit field keeps the same value. | 0x0   | R/W    |
| [1:0] | RESERVED                 |                | Reserved.                                                                                                                                                                                         | 0x0   | R      |

## Interface Configuration C Register

Address: 0x10, Reset: 0x23, Name: INTERFACE\_CONFIG\_C

Additional interface configuration settings.

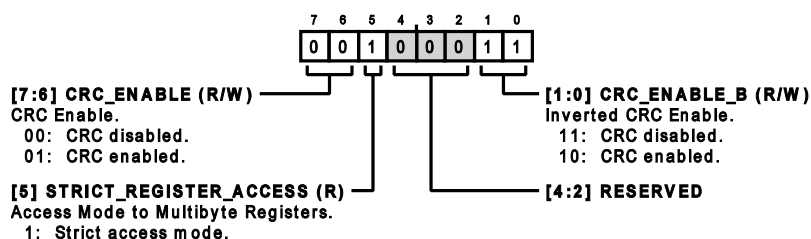


Table 33. Bit Descriptions for INTERFACE\_CONFIG\_C

| Bits  | Bit Name               | Settings | Description                                                                                                                                                                                                                                                                                                                                   | Reset | Access |
|-------|------------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:6] | CRC_ENABLE             | 00<br>01 | CRC Enable. This field is written to enable/disable the use of the CRC error detection on the interface (when the device is in register mode). The CRC_ENABLE_B bits must also be written with the inverted value of the CRC_ENABLE bits in the same SPI write transaction for the CRC status to be changed.<br>CRC disabled.<br>CRC enabled. | 0x0   | R/W    |
| 5     | STRICT_REGISTER_ACCESS |          | Access Mode to Multibyte Registers. This bit is read only. Register write transactions to multibyte registers must include data for                                                                                                                                                                                                           | 0x1   | R      |

## REGISTERS

Table 33. Bit Descriptions for INTERFACE\_CONFIG\_C (Continued)

| Bits  | Bit Name     | Settings | Description                                                                                                                                                                                                                                                                   | Reset | Access |
|-------|--------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
|       |              |          | each of its individual bytes for the register to be updated. Failure to write data to the entire multibyte register (entity) results in the register contents not being updated in memory, and the PARTIAL_REGISTER_ACCESS flag in the INTERFACE_STATUS_A register being set. |       |        |
|       |              | 1        | Strict access mode. Multibyte registers require all bytes to be read/written in full to avoid the PARTIAL_REGISTER_ACCESS bit being flagged.                                                                                                                                  |       |        |
| [4:2] | RESERVED     |          | Reserved.                                                                                                                                                                                                                                                                     | 0x0   | R      |
| [1:0] | CRC_ENABLE_B |          | Inverted CRC Enable. This field must be written with the complementary value of the CRC_ENABLE field.                                                                                                                                                                         | 0x3   | R/W    |
|       |              | 11       | CRC disabled.                                                                                                                                                                                                                                                                 |       |        |
|       |              | 10       | CRC enabled.                                                                                                                                                                                                                                                                  |       |        |

## Interface Status A Register

Address: 0x11, Reset: 0x00, Name: INTERFACE\_STATUS\_A

This register flags several error conditions related to SPI communication and register addressing.

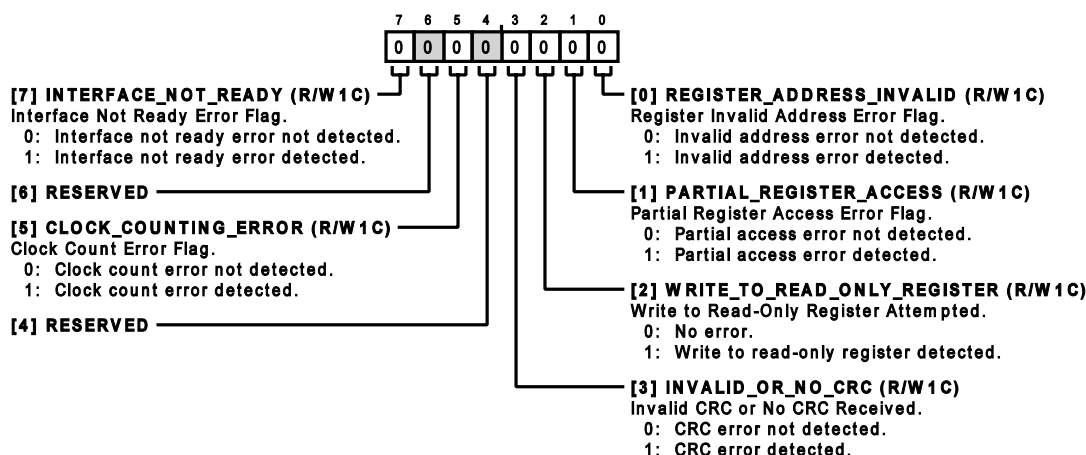


Table 34. Bit Descriptions for INTERFACE\_STATUS\_A

| Bits | Bit Name             | Settings | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Reset | Access |
|------|----------------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 7    | INTERFACE_NOT_READY  |          | Interface Not Ready Error Flag. Indicates if the device interface was not ready for a transaction when an SPI read or write transaction was requested by the digital host (master). This flag bit is set if an SPI frame begins before the device is ready after a power-on reset. This error flag is write-1-to-clear (when this error flag is set, it can only be reset by writing a 1 to this bit).<br><br>0 Interface not ready error not detected.<br>1 Interface not ready error detected. | 0x0   | R/W1C  |
| 6    | RESERVED             |          | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 0x0   | R      |
| 5    | CLOCK_COUNTING_ERROR |          | Clock Count Error Flag. Indicates if the incorrect number of serial clock edges was detected in an SPI read or write transaction (for example, if the transaction was terminated in the middle of a byte). This error flag is write-1-to-clear                                                                                                                                                                                                                                                   | 0x0   | R/W1C  |

## REGISTERS

Table 34. Bit Descriptions for INTERFACE\_STATUS\_A (Continued)

| Bits | Bit Name                    | Settings | Description                                                                                                                                                                                                                                                                            | Reset | Access |
|------|-----------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
|      |                             |          | (when this error flag is set, it can only be reset by writing a 1 to this bit).                                                                                                                                                                                                        |       |        |
|      |                             | 0        | Clock count error not detected.                                                                                                                                                                                                                                                        |       |        |
|      |                             | 1        | Clock count error detected.                                                                                                                                                                                                                                                            |       |        |
| 4    | RESERVED                    |          | Reserved.                                                                                                                                                                                                                                                                              | 0x0   | R      |
| 3    | INVALID_OR_NO_CRC           |          | Invalid CRC or No CRC Received. This is set when the master fails to send a CRC or when the device calculates and checks the CRC and finds its value is incorrect. This error flag is write-1-to-clear (when this error flag is set, it can only be reset by writing a 1 to this bit). | 0x0   | R/W1C  |
|      |                             | 0        | CRC error not detected.                                                                                                                                                                                                                                                                |       |        |
|      |                             | 1        | CRC error detected.                                                                                                                                                                                                                                                                    |       |        |
| 2    | WRITE_TO_READ_ONLY_REGISTER |          | Write to Read-Only Register Attempted. This bit indicates if the digital host attempts an SPI write to a register that contains exclusively read only fields. This error flag is write-1-to-clear (when this error flag is set, it can only be reset by writing a 1 to this bit).      | 0x0   | R/W1C  |
|      |                             | 0        | No error.                                                                                                                                                                                                                                                                              |       |        |
|      |                             | 1        | Write to read-only register detected.                                                                                                                                                                                                                                                  |       |        |
| 1    | PARTIAL_REGISTER_ACCESS     |          | Partial Register Access Error Flag. This bit is asserted when there are not enough bytes of data in a transaction addressed to a multibyte register. This error flag is write-1-to-clear (when this error flag is set, it can only be reset by writing a 1 to this bit).               | 0x0   | R/W1C  |
|      |                             | 0        | Partial access error not detected.                                                                                                                                                                                                                                                     |       |        |
|      |                             | 1        | Partial access error detected.                                                                                                                                                                                                                                                         |       |        |
| 0    | REGISTER_ADDRESS_INVALID    |          | Register Invalid Address Error Flag. Indicates if an SPI read or write transaction was attempted on an invalid register address. This error flag is write-1-to-clear (when this error flag is set, it can only be reset by writing a 1 to this bit).                                   | 0x0   | R/W1C  |
|      |                             | 0        | Invalid address error not detected.                                                                                                                                                                                                                                                    |       |        |
|      |                             | 1        | Invalid address error detected.                                                                                                                                                                                                                                                        |       |        |

## Interface Configuration D Register

Address: 0x14, Reset: 0x04, Name: INTERFACE\_CONFIG\_D

This register contains miscellaneous configuration bits affecting SPI communication and electrical parameters of digital signals.

## REGISTERS

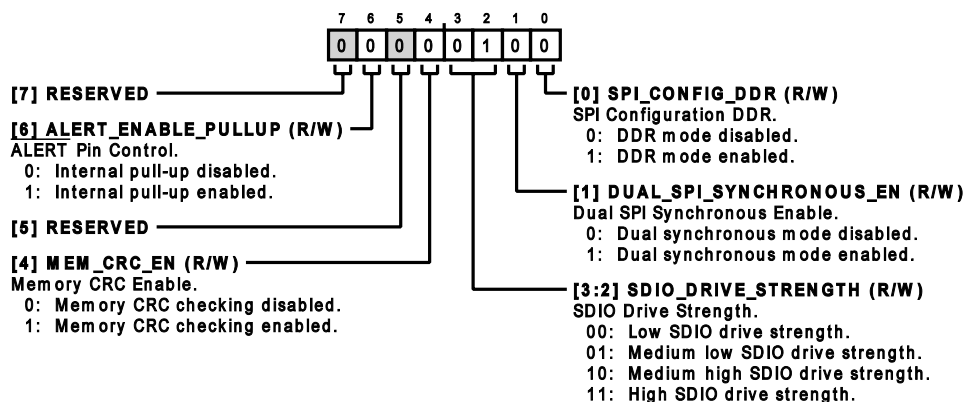


Table 35. Bit Descriptions for INTERFACE\_CONFIG\_D

| Bits  | Bit Name                | Settings | Description                                                                                                                                                                                                                    | Reset | Access |
|-------|-------------------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 7     | RESERVED                |          | Reserved.                                                                                                                                                                                                                      | 0x0   | R      |
| 6     | ALERT_ENABLE_PULLUP     |          | ALERT Pin Control. Enable internal 2.5 kΩ pull-up resistor.<br>0 Internal pull-up disabled. An external pull-up is required.<br>1 Internal pull-up enabled.                                                                    | 0x0   | R/W    |
| 5     | RESERVED                |          | Reserved.                                                                                                                                                                                                                      | 0x0   | R      |
| 4     | MEM_CRC_EN              |          | Memory CRC Enable. This bit controls the continuous checking of the primary register set and the ROM memory.<br>0 Memory CRC checking disabled.<br>1 Memory CRC checking enabled.                                              | 0x0   | R/W    |
| [3:2] | SDIO_DRIVE_STRENGTH     |          | SDIO Drive Strength. These two bits allow for the increase in SDIO drive strength.<br>00 Low SDIO drive strength.<br>01 Medium low SDIO drive strength.<br>10 Medium high SDIO drive strength.<br>11 High SDIO drive strength. | 0x1   | R/W    |
| 1     | DUAL_SPI_SYNCHRONOUS_EN |          | Dual SPI Synchronous Enable. This bit controls the dual synchronous data transfer using one SDIO line for each DAC stream.<br>0 Dual synchronous mode disabled.<br>1 Dual synchronous mode enabled.                            | 0x0   | R/W    |
| 0     | SPI_CONFIG_DDR          |          | SPI Configuration DDR. This bit controls the use of DDR for data transfers.<br>0 DDR mode disabled.<br>1 DDR mode enabled.                                                                                                     | 0x0   | R/W    |

## REGISTERS

## DAC REGISTER DETAILS

## Reference Configuration Register

Address: 0x15, Reset: 0x00, Name: REFERENCE\_CONFIG

This register controls the source and driving of the voltage reference.

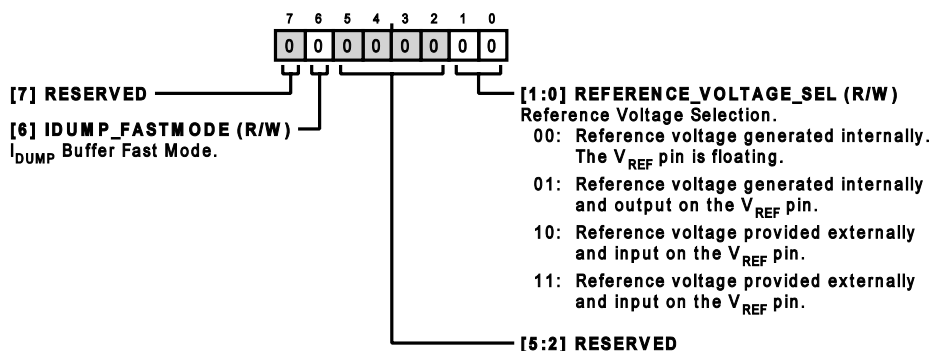


Table 36. Bit Descriptions for REFERENCE\_CONFIG

| Bits  | Bit Name              | Settings | Description                                                                                                                                                                                                                                                                                                                                                                                                                           | Reset | Access |
|-------|-----------------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 7     | RESERVED              |          | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                             | 0x0   | R      |
| 6     | IDUMP_FASTMODE        |          | IDUMP Buffer Fast Mode. Set this bit to increase the $I_{DD}$ of the IDUMP buffer of the amplifier to allow for a greater gain bandwidth.                                                                                                                                                                                                                                                                                             | 0x0   | R/W    |
| [5:2] | RESERVED              |          | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                             | 0x0   | R      |
| [1:0] | REFERENCE_VOLTAGE_SEL |          | Reference Voltage Selection. These two bits are used to select the configuration of the reference voltage circuit.<br>00 Reference voltage generated internally. The $V_{REF}$ pin is floating.<br>01 Reference voltage generated internally and output on the $V_{REF}$ pin.<br>10 Reference voltage provided externally and input on the $V_{REF}$ pin.<br>11 Reference voltage provided externally and input on the $V_{REF}$ pin. | 0x0   | R/W    |

## Error Alarm Mask Register

Address: 0x16, Reset: 0x00, Name: ERR\_ALARM\_MASK

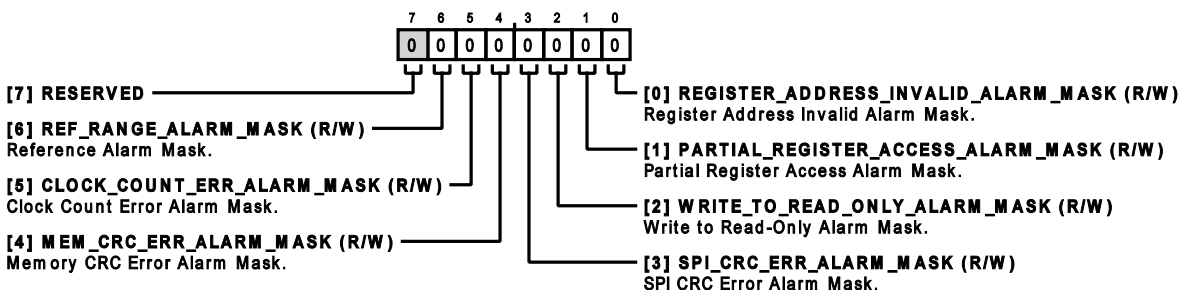
This register selects which error conditions cause the assertion of the  $\overline{ALERT}$  pin.

Table 37. Bit Descriptions for ERR\_ALARM\_MASK

| Bits | Bit Name | Settings | Description | Reset | Access |
|------|----------|----------|-------------|-------|--------|
| 7    | RESERVED |          | Reserved.   | 0x0   | R      |

## REGISTERS

Table 37. Bit Descriptions for ERR\_ALARM\_MASK (Continued)

| Bits | Bit Name                            | Settings | Description                                                                                                                         | Reset | Access |
|------|-------------------------------------|----------|-------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 6    | REF_RANGE_ALARM_MASK                |          | Reference Alarm Mask. When set, the user can ignore alarms due to the reference dipping below 2 V.                                  | 0x0   | R/W    |
| 5    | CLOCK_COUNT_ERR_ALARM_MASK          |          | Clock Count Error Alarm Mask. When set, the user can ignore alarms due to an insufficient number of clock periods for a user write. | 0x0   | R/W    |
| 4    | MEM_CRC_ERR_ALARM_MASK              |          | Memory CRC Error Alarm Mask. When set, the user can ignore alarms due to a memory CRC error.                                        | 0x0   | R/W    |
| 3    | SPI_CRC_ERR_ALARM_MASK              |          | SPI CRC Error Alarm Mask. When set, the user can ignore alarms due to the SPI CRC checker.                                          | 0x0   | R/W    |
| 2    | WRITE_TO_READ_ONLY_ALARM_MASK       |          | Write to Read-Only Alarm Mask. When set, the user can ignore alarms due to the user writing to a read-only register.                | 0x0   | R/W    |
| 1    | PARTIAL_REGISTER_ACCESS_ALARM_MASK  |          | Partial Register Access Alarm Mask. When set, the user can ignore alarms due to the user not completing the write to a register.    | 0x0   | R/W    |
| 0    | REGISTER_ADDRESS_INVALID_ALARM_MASK |          | Register Address Invalid Alarm Mask. When set, the user can ignore alarms due to the user writing to an invalid register address.   | 0x0   | R/W    |

## Error Status Register

Address: 0x17, Reset: 0x01, Name: ERR\_STATUS

This register signals a combination of errors in the analog and digital domains. All the bits are sticky and can be cleared by writing 1.

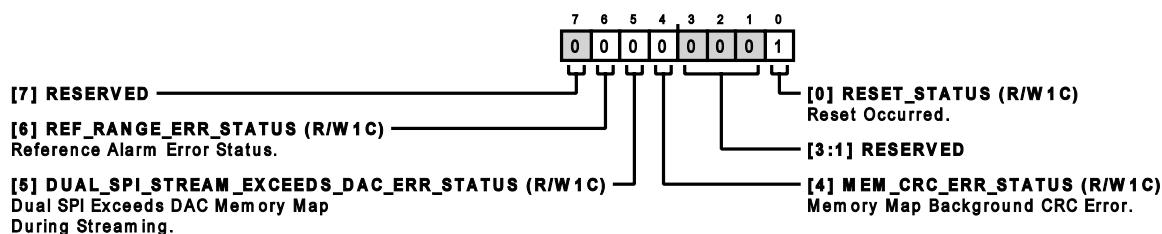


Table 38. Bit Descriptions for ERR\_STATUS

| Bits | Bit Name                               | Settings | Description                                                                                                                                         | Reset | Access |
|------|----------------------------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 7    | RESERVED                               |          | Reserved.                                                                                                                                           | 0x0   | R      |
| 6    | REF_RANGE_ERR_STATUS                   |          | Reference Alarm Error Status. This bit indicates an alarm if the reference dips below 2 V.                                                          | 0x0   | R/W1C  |
| 5    | DUAL_SPI_STREAM_EXCEEDS_DAC_ERR_STATUS |          | Dual SPI Exceeds DAC Memory Map During Streaming. This bit indicates an alarm when in dual SPI and streaming access goes beyond the DAC memory map. | 0x0   | R/W1C  |
| 4    | MEM_CRC_ERR_STATUS                     |          | Memory Map Background CRC Error. This bit indicates an alarm when the background CRC detects                                                        | 0x0   | R/W1C  |

## REGISTERS

Table 38. Bit Descriptions for ERR\_STATUS (Continued)

| Bits  | Bit Name     | Settings | Description                                                                                                                                                                                                                                 | Reset | Access |
|-------|--------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
|       |              |          | bit corruption within the memory map.                                                                                                                                                                                                       |       |        |
| [3:1] | RESERVED     |          | Reserved.                                                                                                                                                                                                                                   | 0x0   | R      |
| 0     | RESET_STATUS |          | Reset Occurred. This bit indicates that the device has just completed initialization following a reset. This bit asserts the $\overline{\text{ALERT}}$ pin and it is nonmaskable. Therefore, it must be cleared right after initialization. | 0x1   | R/W1C  |

## Power-Down Configuration Register

Address: 0x18, Reset: 0x00, Name: POWERDOWN\_CONFIG

This register controls the individual power-down of the DAC channels.

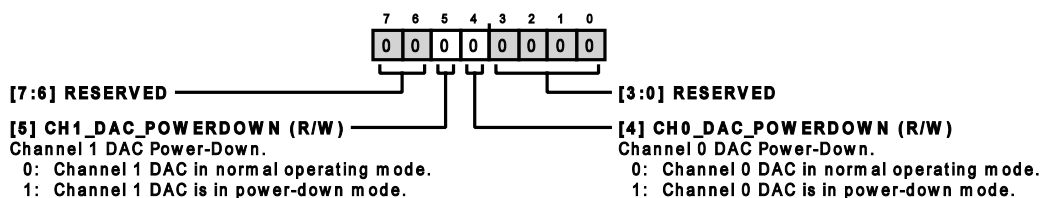


Table 39. Bit Descriptions for POWERDOWN\_CONFIG

| Bits  | Bit Name          | Settings | Description                                                                                                      | Reset | Access |
|-------|-------------------|----------|------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:6] | RESERVED          |          | Reserved.                                                                                                        | 0x0   | R      |
| 5     | CH1_DAC_POWERDOWN |          | Channel 1 DAC Power-Down.<br>0 Channel 1 DAC in normal operating mode.<br>1 Channel 1 DAC is in power-down mode. | 0x0   | R/W    |
| 4     | CH0_DAC_POWERDOWN |          | Channel 0 DAC Power-Down.<br>0 Channel 0 DAC in normal operating mode.<br>1 Channel 0 DAC is in power-down mode. | 0x0   | R/W    |
| [3:0] | RESERVED          |          | Reserved.                                                                                                        | 0x0   | R      |

# REGISTERS

## Output Range Register

Address: 0x19, Reset: 0x00, Name: CH0\_CH1\_OUTPUT\_RANGE

This register sets the output range of the DAC channels to one of the preconfigured ranges listed in Table 8. In addition to setting this register, the corresponding RFBx\_y resistor must be connected to obtain the expected result.

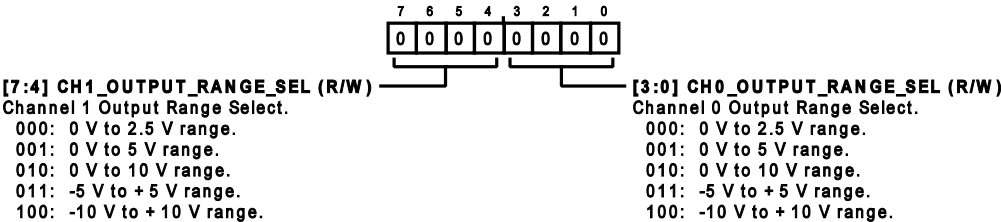


Table 40. Bit Descriptions for CH0\_CH1\_OUTPUT\_RANGE

| Bits  | Bit Name             | Settings | Description                                                                                                                                                                                                                                                                                                                                                                 | Reset | Access |
|-------|----------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:4] | CH1_OUTPUT_RANGE_SEL |          | Channel 1 Output Range Select. The user can select which voltage output range is desired.<br>000 0 V to 2.5 V range. Requires RFB1_1 connection.<br>001 0 V to 5 V range. Requires RFB1_1 connection.<br>010 0 V to 10 V range. Requires RFB2_1 connection.<br>011 -5 V to +5 V range. Requires RFB2_1 connection.<br>100 -10 V to +10 V range. Requires RFB4_1 connection. | 0x0   | R/W    |
| [3:0] | CH0_OUTPUT_RANGE_SEL |          | Channel 0 Output Range Select. The user can select which voltage output range is desired.<br>000 0 V to 2.5 V range. Requires RFB1_0 connection.<br>001 0 V to 5 V range. Requires RFB1_0 connection.<br>010 0 V to 10 V range. Requires RFB2_0 connection.<br>011 -5 V to +5 V range. Requires RFB2_0 connection.<br>100 -10 V to +10 V range. Requires RFB4_0 connection. | 0x0   | R/W    |

## Channel 0 Offset Register

Address: 0x1B, Reset: 0x00, Name: CH0\_OFFSET

This register configures the dc offset of the Channel 0 DAC. For this value to take effect, the CH0\_RANGE\_OVERRIDE bit must be set in the CH0\_GAIN register.

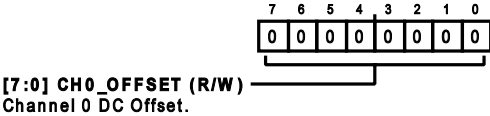


Table 41. Bit Descriptions for CH0\_OFFSET

| Bits  | Bit Name   | Settings | Description          | Reset | Access |
|-------|------------|----------|----------------------|-------|--------|
| [7:0] | CH0_OFFSET |          | Channel 0 DC Offset. | 0x0   | R/W    |

# REGISTERS

## Channel 0 Gain Register

Address: 0x1C, Reset: 0x00, Name: CH0\_GAIN

This register enables the configuration of custom span modes, configures the scaling of the PMOS DAC and NMOS DAC current sources, and controls the polarity of the offset value.

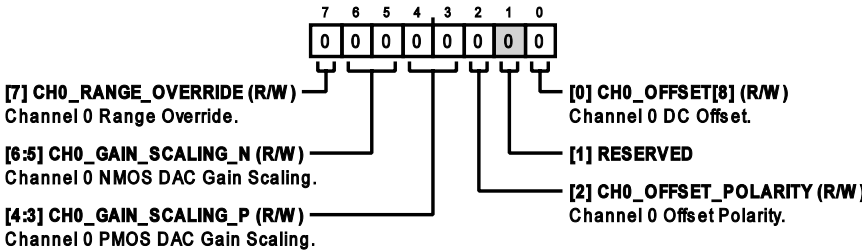


Table 42. Bit Descriptions for CH0\_GAIN

| Bits  | Bit Name            | Description                                                                                                                                                                                                                             | Reset | Access |
|-------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 7     | CH0_RANGE_OVERRIDE  | Channel 0 Range Override. This bit allows the user to override the preconfigured range settings and manually set offset and gain.<br>0: Use preconfigured range settings.<br>1: Use custom range settings.                              | 0x0   | R/W    |
| [6:5] | CH0_GAIN_SCALING_N  | Channel 0 NMOS DAC Gain Scaling. This field controls the multiplying factor for the codes applied to the NMOS DAC current sources.<br>00: Gain scaling 1.<br>01: Gain scaling 0.5.<br>10: Gain scaling 0.25.<br>11: Gain scaling 0.125. | 0x0   | R/W    |
| [4:3] | CH0_GAIN_SCALING_P  | Channel 0 PMOS DAC Gain Scaling. This field controls the multiplying factor for the codes applied to the PMOS DAC current sources.<br>00: Gain scaling 1.<br>01: Gain scaling 0.5.<br>10: Gain scaling 0.25.<br>11: Gain scaling 0.125. | 0x0   | R/W    |
| 2     | CH0_OFFSET_POLARITY | Channel 0 Offset Polarity. This bit sets the polarity of the offset.<br>0: Positive offset.<br>1: Negative offset.                                                                                                                      | 0x0   | R/W    |
| 1     | RESERVED            | Reserved.                                                                                                                                                                                                                               | 0x0   | R      |
| 0     | CH0_OFFSET[8]       | Channel 0 DC Offset.                                                                                                                                                                                                                    | 0x0   | R/W    |

## Channel 1 Offset Register

Address: 0x1D, Reset: 0x00, Name: CH1\_OFFSET

This register configures the dc offset of the Channel 0 DAC. For this value to take effect, the CH1\_RANGE\_OVERRIDE bit must be set in the CH1\_GAIN register.

## REGISTERS

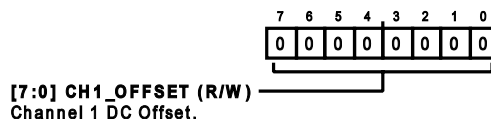


Table 43. Bit Descriptions for CH1\_OFFSET

| Bits  | Bit Name   | Settings | Description          | Reset | Access |
|-------|------------|----------|----------------------|-------|--------|
| [7:0] | CH1_OFFSET |          | Channel 1 DC Offset. | 0x0   | R/W    |

## Channel 1 Gain Register

Address: 0x1E, Reset: 0x00, Name: CH1\_GAIN

This register enables the configuration of custom span modes, configures the scaling of the PMOS DAC and NMOS DAC current sources, and controls the polarity of the offset value.

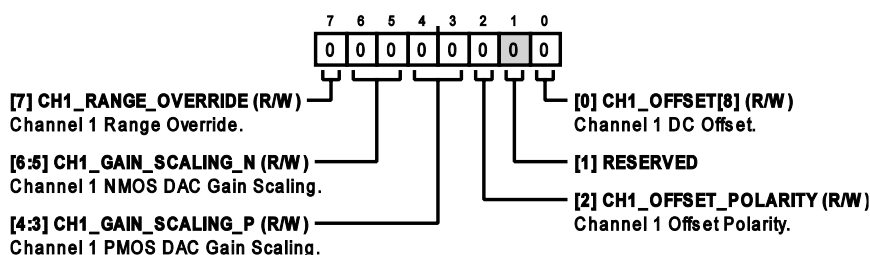


Table 44. Bit Descriptions for CH1\_GAIN

| Bits  | Bit Name            | Description                                                                                                                                                                                                                             | Reset | Access |
|-------|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| 7     | CH1_RANGE_OVERRIDE  | Channel 1 Range Override. This bit allows the user to override the preconfigured range settings and manually set offset and gain.<br>0: Use preconfigured range settings.<br>1: Use custom range settings.                              | 0x0   | R/W    |
| [6:5] | CH1_GAIN_SCALING_N  | Channel 1 NMOS DAC Gain Scaling. This field controls the multiplying factor for the codes applied to the NMOS DAC current sources.<br>00: Gain scaling 1.<br>01: Gain scaling 0.5.<br>10: Gain scaling 0.25.<br>11: Gain scaling 0.125. | 0x0   | R/W    |
| [4:3] | CH1_GAIN_SCALING_P  | Channel 1 PMOS DAC Gain Scaling. This field controls the multiplying factor for the codes applied to the PMOS DAC current sources.<br>00: Gain scaling 1.<br>01: Gain scaling 0.5.<br>10: Gain scaling 0.25.<br>11: Gain scaling 0.125. | 0x0   | R/W    |
| 2     | CH1_OFFSET_POLARITY | Channel 1 Offset Polarity. This bit sets the polarity of the offset.<br>0: Positive offset.<br>1: Negative offset.                                                                                                                      | 0x0   | R/W    |
| 1     | RESERVED            | Reserved.                                                                                                                                                                                                                               | 0x0   | R      |
| 0     | CH1_OFFSET[8]       | Channel 1 DC Offset.                                                                                                                                                                                                                    | 0x0   | R/W    |

## REGISTERS

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## Hardware LDAC Mask Register, Fast Mode

Address: 0x28, Reset: 0x00, Name: HW\_LDAC\_16B

This register controls the masking of the external  $\overline{\text{LDAC}}$  signal to latch data into each of the DAC channels.

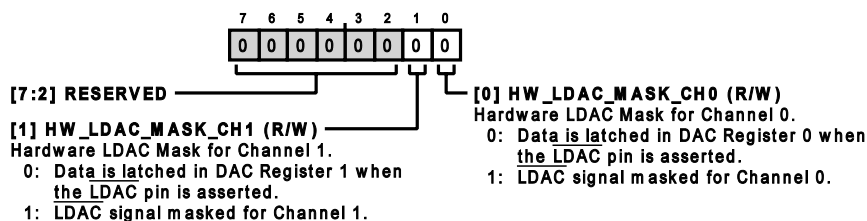


Table 45. Bit Descriptions for HW\_LDAC\_16B

| Bits  | Bit Name         | Settings | Description                                                                                                                                                                                                                                                                                                                                                                      | Reset | Access |
|-------|------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | RESERVED         |          | Reserved.                                                                                                                                                                                                                                                                                                                                                                        | 0x0   | R      |
| 1     | HW_LDAC_MASK_CH1 |          | Hardware LDAC Mask for Channel 1. This bit controls the latching of data into the DAC register when the $\overline{\text{LDAC}}$ signal is asserted.<br>0 Data is latched in DAC Register 1 when the $\overline{\text{LDAC}}$ pin is asserted.<br>1 $\overline{\text{LDAC}}$ signal masked for Channel 1. DAC register is not updated when $\overline{\text{LDAC}}$ is asserted. | 0x0   | R/W    |
| 0     | HW_LDAC_MASK_CH0 |          | Hardware LDAC Mask for Channel 0. This bit controls the latching of data into the DAC register when the $\overline{\text{LDAC}}$ signal is asserted.<br>0 Data is latched in DAC Register 0 when the $\overline{\text{LDAC}}$ pin is asserted.<br>1 $\overline{\text{LDAC}}$ signal masked for Channel 0. DAC register is not updated when $\overline{\text{LDAC}}$ is asserted. | 0x0   | R/W    |

## DAC Register for Channel 0, Fast Mode

Address: 0x29, Reset: 0x0000, Name: CH0\_DAC\_16B

This register contains the data currently played on DAC Channel 0.

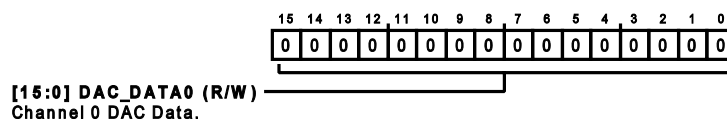


Table 46. Bit Descriptions for CH0\_DAC\_16B

| Bits   | Bit Name  | Settings | Description         | Reset | Access |
|--------|-----------|----------|---------------------|-------|--------|
| [15:0] | DAC_DATA0 |          | Channel 0 DAC Data. | 0x0   | R/W    |

## DAC Register for Channel 1, Fast Mode

Address: 0x2B, Reset: 0x0000, Name: CH1\_DAC\_16B

This register contains the data currently played on DAC Channel 1.

## REGISTERS

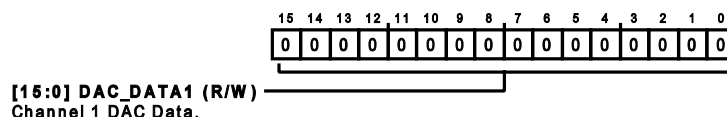


Table 47. Bit Descriptions for CH1\_DAC\_16B

| Bits   | Bit Name  | Settings | Description         | Reset | Access |
|--------|-----------|----------|---------------------|-------|--------|
| [15:0] | DAC_DATA1 |          | Channel 1 DAC Data. | 0x0   | R/W    |

## DAC Page Register, Fast Mode

Address: 0x2D, Reset: 0x0000, Name: DAC\_PAGE\_16B

This register is used to write data to one or both channels according to the configuration of the SEL\_CHx bits in the CH\_SELECT\_16B register. It can be used to write both channels simultaneously without using the  $\overline{\text{LDAC}}$  signal.

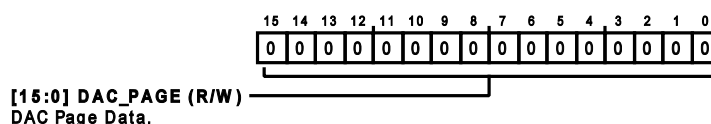


Table 48. Bit Descriptions for DAC\_PAGE\_16B

| Bits   | Bit Name | Settings | Description                                                                                                                                                                       | Reset | Access |
|--------|----------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [15:0] | DAC_PAGE |          | DAC Page Data. Following a write to this register, the DAC code loaded into this register is copied into the DAC register of any channels selected in the CH_SELECT_16B register. | 0x0   | R/W    |

## Channel Select for Page Registers, Fast Mode

Address: 0x2F, Reset: 0x00, Name: CH\_SELECT\_16B

This register selects which channel registers are updated following a write to the DAC\_PAGE\_16B or INPUT\_PAGE\_16B registers.

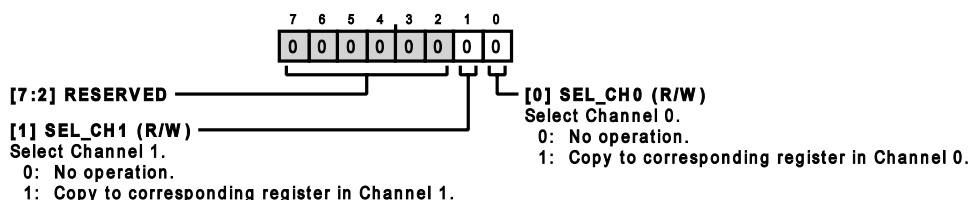


Table 49. Bit Descriptions for CH\_SELECT\_16B

| Bits  | Bit Name | Settings | Description                                                                                                                                                                                                                                                                           | Reset | Access |
|-------|----------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | RESERVED |          | Reserved.                                                                                                                                                                                                                                                                             | 0x0   | R      |
| 1     | SEL_CH1  |          | Select Channel 1. When this bit is set, data written to the INPUT_PAGE_16B register is copied to the CH1_INPUT_16B register and data written to the DAC_PAGE_16B register is copied to the CH1_DAC_16B register.<br>0 No operation.<br>1 Copy to corresponding register in Channel 1. | 0x0   | R/W    |
| 0     | SEL_CH0  |          | Select Channel 0. When this bit is set, data written to the INPUT_PAGE_16B register is copied to the CH0_INPUT_16B register and data written to the DAC_PAGE_16B register is copied to the CH0_DAC_16B register.<br>0 No operation.<br>1 Copy to corresponding register in Channel 0. | 0x0   | R/W    |

# REGISTERS

## Input Page Register, Fast Mode

Address: 0x30, Reset: 0x0000, Name: INPUT\_PAGE\_16B

This register is used to write data to one or both DAC input registers according to the configuration of the SEL\_CHx bits in the CH\_SELECT\_16B register.

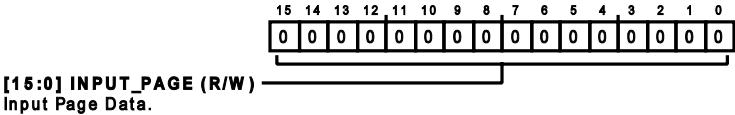


Table 50. Bit Descriptions for INPUT\_PAGE\_16B

| Bits   | Bit Name   | Settings | Description                                                                                                                                                                           | Reset | Access |
|--------|------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [15:0] | INPUT_PAGE |          | Input Page Data. Following a write to this register, the DAC code loaded into this register is copied into the input register of any channels selected in the CH_SELECT_16B register. | 0x0   | R/W    |

## Software LDAC Register, Fast Mode

Address: 0x32, Reset: 0x00, Name: SW\_LDAC\_16B

This register is used to trigger a data transfer between the input registers and the DAC registers. It is the software equivalent of pulsing the LDAC line low.

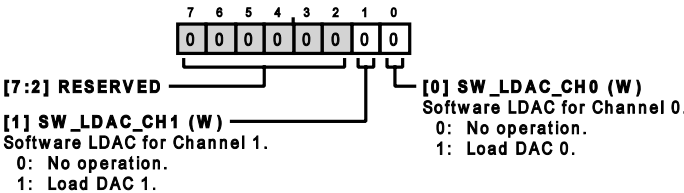


Table 51. Bit Descriptions for SW\_LDAC\_16B

| Bits  | Bit Name    | Settings | Description                                                                                                                                                                                                          | Reset | Access |
|-------|-------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | RESERVED    |          | Reserved.                                                                                                                                                                                                            | 0x0   | R      |
| 1     | SW_LDAC_CH1 |          | Software LDAC for Channel 1. Setting this bit transfers contents from the CH1_INPUT_16B register to the CH1_DAC_16B register. This bit automatically resets after being written.<br>0 No operation.<br>1 Load DAC 1. | 0x0   | W      |
| 0     | SW_LDAC_CH0 |          | Software LDAC for Channel 0. Setting this bit transfers contents from the CH0_INPUT_16B register to the CH0_DAC_16B register. This bit automatically resets after being written.<br>0 No operation.<br>1 Load DAC 0. | 0x0   | W      |

## REGISTERS

## Input Register for Channel 0, Fast Mode

Address: 0x33, Reset: 0x0000, Name: CH0\_INPUT\_16B

This register contains the data to be transferred to the DAC register using one of the various trigger options, hardware LDAC, software LDAC, or automatic transfer.

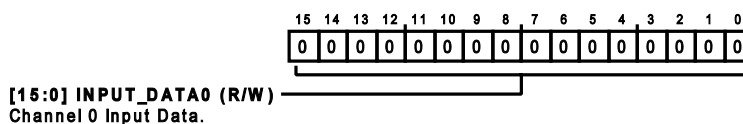


Table 52. Bit Descriptions for CH0\_INPUT\_16B

| Bits   | Bit Name    | Settings | Description           | Reset | Access |
|--------|-------------|----------|-----------------------|-------|--------|
| [15:0] | INPUT_DATA0 |          | Channel 0 Input Data. | 0x0   | R/W    |

## Input Register for Channel 1, Fast Mode

Address: 0x35, Reset: 0x0000, Name: CH1\_INPUT\_16B

This register contains the data to be transferred to the DAC register using one of the various trigger options, hardware LDAC, software LDAC, or automatic transfer.

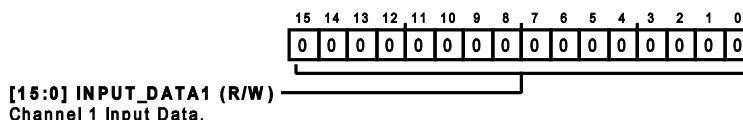


Table 53. Bit Descriptions for CH1\_INPUT\_16B

| Bits   | Bit Name    | Settings | Description           | Reset | Access |
|--------|-------------|----------|-----------------------|-------|--------|
| [15:0] | INPUT_DATA1 |          | Channel 1 Input Data. | 0x0   | R/W    |

## Hardware LDAC Mask Register, Precision Mode

Address: 0x37, Reset: 0x00, Name: HW\_LDAC\_24B

This register controls the masking of the external  $\overline{\text{LDAC}}$  signal to latch data into each of the DAC channels.

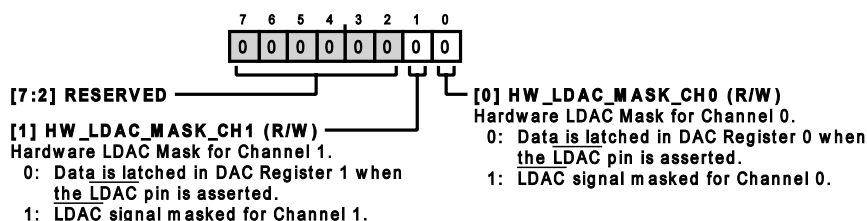


Table 54. Bit Descriptions for HW\_LDAC\_24B

| Bits  | Bit Name         | Settings | Description                                                                                                                                                                                                                                                                                                                                                                      | Reset | Access |
|-------|------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | RESERVED         |          | Reserved.                                                                                                                                                                                                                                                                                                                                                                        | 0x0   | R      |
| 1     | HW_LDAC_MASK_CH1 |          | Hardware LDAC Mask for Channel 1. This bit controls the latching of data into the DAC register when the $\overline{\text{LDAC}}$ signal is asserted.<br>0 Data is latched in DAC Register 1 when the $\overline{\text{LDAC}}$ pin is asserted.<br>1 $\overline{\text{LDAC}}$ signal masked for Channel 1. DAC register is not updated when $\overline{\text{LDAC}}$ is asserted. | 0x0   | R/W    |
| 0     | HW_LDAC_MASK_CH0 |          | Hardware LDAC Mask for Channel 0. This bit controls the latching of data into the DAC register when the $\overline{\text{LDAC}}$ signal is asserted.                                                                                                                                                                                                                             | 0x0   | R/W    |

## REGISTERS

Table 54. Bit Descriptions for HW\_LDAC\_24B (Continued)

| Bits | Bit Name | Settings | Description                                                                          | Reset | Access |
|------|----------|----------|--------------------------------------------------------------------------------------|-------|--------|
|      |          | 0        | Data is latched in DAC Register 0 when the LDAC pin is asserted.                     |       |        |
|      |          | 1        | LDAC signal masked for Channel 0. DAC register is not updated when LDAC is asserted. |       |        |

## DAC Register for Channel 0, Precision Mode

Address: 0x38, Reset: 0x000000, Name: CH0\_DAC\_24B

This register contains the data currently played on DAC Channel 0.

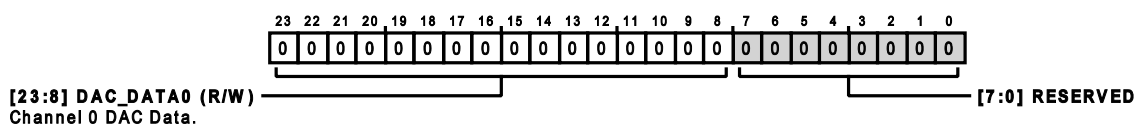


Table 55. Bit Descriptions for CH0\_DAC\_24B

| Bits   | Bit Name  | Settings | Description         | Reset | Access |
|--------|-----------|----------|---------------------|-------|--------|
| [23:8] | DAC_DATA0 |          | Channel 0 DAC Data. | 0x0   | R/W    |
| [7:0]  | RESERVED  |          | Reserved.           | 0x0   | R      |

## DAC Register for Channel 1, Precision Mode

Address: 0x3B, Reset: 0x000000, Name: CH1\_DAC\_24B

This register contains the data currently played on DAC Channel 1.

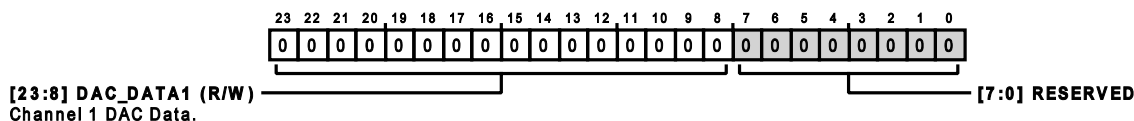


Table 56. Bit Descriptions for CH1\_DAC\_24B

| Bits   | Bit Name  | Settings | Description         | Reset | Access |
|--------|-----------|----------|---------------------|-------|--------|
| [23:8] | DAC_DATA1 |          | Channel 1 DAC Data. | 0x0   | R/W    |
| [7:0]  | RESERVED  |          | Reserved.           | 0x0   | R      |

## DAC Page Register, Precision Mode

Address: 0x3E, Reset: 0x000000, Name: DAC\_PAGE\_24B

This register is used to write data to one or both channels according to the configuration of the SEL\_CHx bits in the CH\_SELECT\_24B register. It can be used to write both channels simultaneously without using the LDAC signal.

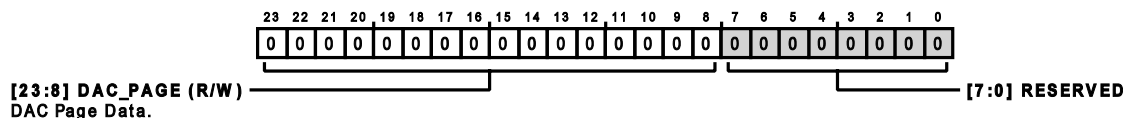


Table 57. Bit Descriptions for DAC\_PAGE\_24B

| Bits   | Bit Name | Settings | Description                                                                                                                                                                       | Reset | Access |
|--------|----------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [23:8] | DAC_PAGE |          | DAC Page Data. Following a write to this register, the DAC code loaded into this register is copied into the DAC register of any channels selected in the CH_SELECT_24B register. | 0x0   | R/W    |
| [7:0]  | RESERVED |          | Reserved.                                                                                                                                                                         | 0x0   | R      |

# REGISTERS

## Channel Select for Page Registers, Precision Mode

Address: 0x41, Reset: 0x00, Name: CH\_SELECT\_24B

This register selects which channel registers are updated following a write to the DAC\_PAGE\_24B or INPUT\_PAGE\_24B registers.

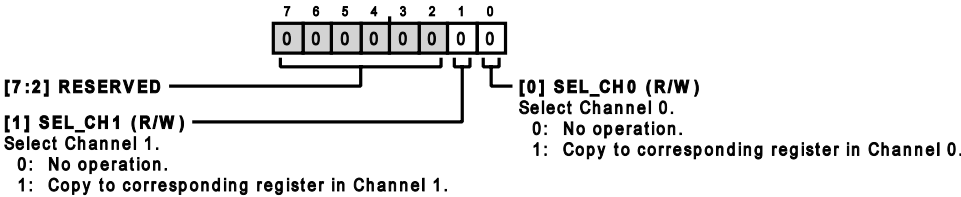


Table 58. Bit Descriptions for CH\_SELECT\_24B

| Bits  | Bit Name | Settings | Description                                                                                                                                                                                                                                                                           | Reset | Access |
|-------|----------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | RESERVED |          | Reserved.                                                                                                                                                                                                                                                                             | 0x0   | R      |
| 1     | SEL_CH1  |          | Select Channel 1. When this bit is set, data written to the INPUT_PAGE_24B register is copied to the CH1_INPUT_24B register and data written to the DAC_PAGE_24B register is copied to the CH1_DAC_24B register.<br>0 No operation.<br>1 Copy to corresponding register in Channel 1. | 0x0   | R/W    |
| 0     | SEL_CH0  |          | Select Channel 0. When this bit is set, data written to the INPUT_PAGE_24B register is copied to the CH0_INPUT_24B register and data written to the DAC_PAGE_24B register is copied to the CH0_DAC_24B register.<br>0 No operation.<br>1 Copy to corresponding register in Channel 0. | 0x0   | R/W    |

## Input Page Register, Precision Mode

Address: 0x42, Reset: 0x000000, Name: INPUT\_PAGE\_24B

This register is used to write data to one or both DAC input registers according to the configuration of the SEL\_CHx bits in the CH\_SELECT\_24B register.

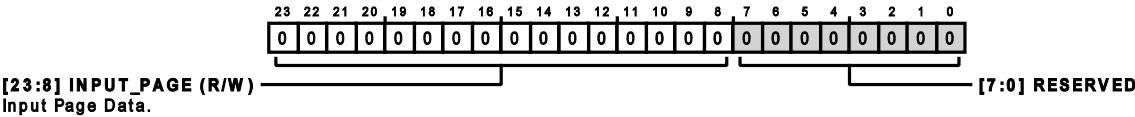


Table 59. Bit Descriptions for INPUT\_PAGE\_24B

| Bits   | Bit Name   | Settings | Description                                                                                                                                                                           | Reset | Access |
|--------|------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [23:8] | INPUT_PAGE |          | Input Page Data. Following a write to this register, the DAC code loaded into this register is copied into the input register of any channels selected in the CH_SELECT_24B register. | 0x0   | R/W    |
| [7:0]  | RESERVED   |          | Reserved.                                                                                                                                                                             | 0x0   | R      |

# REGISTERS

## Software LDAC Register, Precision Mode

Address: 0x45, Reset: 0x00, Name: SW\_LDAC\_24B

This register is used to trigger a data transfer between the input registers and the DAC registers. It is the software equivalent of pulsing the LDAC line low.

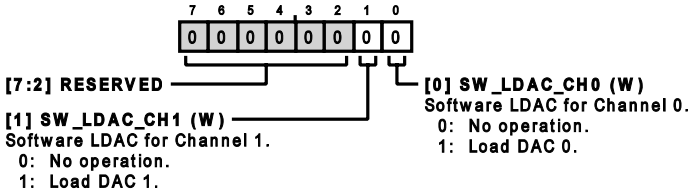


Table 60. Bit Descriptions for SW\_LDAC\_24B

| Bits  | Bit Name    | Settings | Description                                                                                                                                                                                                          | Reset | Access |
|-------|-------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------|
| [7:2] | RESERVED    |          | Reserved.                                                                                                                                                                                                            | 0x0   | R      |
| 1     | SW_LDAC_CH1 |          | Software LDAC for Channel 1. Setting this bit transfers contents from the CH1_INPUT_24B register to the CH1_DAC_24B register. This bit automatically resets after being written.<br>0 No operation.<br>1 Load DAC 1. | 0x0   | W      |
| 0     | SW_LDAC_CH0 |          | Software LDAC for Channel 0. Setting this bit transfers contents from the CH0_INPUT_24B register to the CH0_DAC_24B register. This bit automatically resets after being written.<br>0 No operation.<br>1 Load DAC 0. | 0x0   | W      |

## Input Register for Channel 0, Precision Mode

Address: 0x46, Reset: 0x000000, Name: CH0\_INPUT\_24B

This register contains the data to be transferred to the DAC register using one of the various trigger options, hardware LDAC, software LDAC, or automatic transfer.

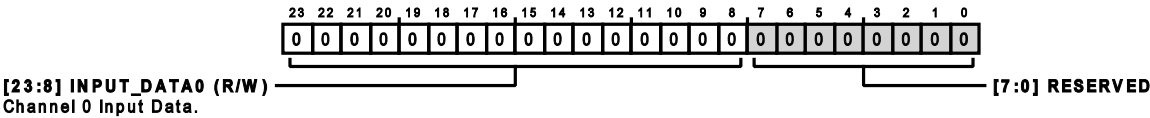


Table 61. Bit Descriptions for CH0\_INPUT\_24B

| Bits   | Bit Name    | Settings | Description           | Reset | Access |
|--------|-------------|----------|-----------------------|-------|--------|
| [23:8] | INPUT_DATA0 |          | Channel 0 Input Data. | 0x0   | R/W    |
| [7:0]  | RESERVED    |          | Reserved.             | 0x0   | R      |

REGISTERS

Input Register for Channel 1, Precision Mode

Address: 0x49, Reset: 0x000000, Name: CH1\_INPUT\_24B

This register contains the data to be transferred to the DAC register using one of the various trigger options, hardware LDAC, software LDAC, or automatic transfer.

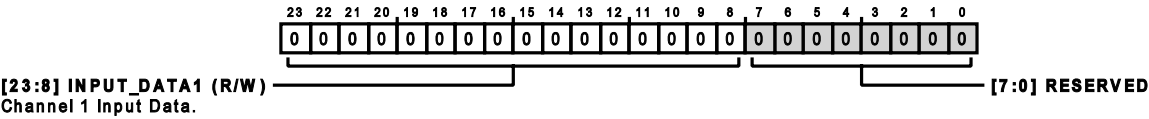


Table 62. Bit Descriptions for CH1\_INPUT\_24B

| Bits   | Bit Name    | Settings | Description           | Reset | Access |
|--------|-------------|----------|-----------------------|-------|--------|
| [23:8] | INPUT_DATA1 |          | Channel 1 Input Data. | 0x0   | R/W    |
| [7:0]  | RESERVED    |          | Reserved.             | 0x0   | R      |

## APPLICATIONS INFORMATION

## POWER SUPPLY RECOMMENDATIONS

The AD3552R does not have any restriction for power supply sequencing. The chip incorporates a power monitor for  $AV_{DD}$  and  $DV_{DD}$  that releases the internal reset when both rails are within specification. Nevertheless, the recommended sequence to turn on the supply rails is GND,  $AV_{DD}$ ,  $DV_{DD}$ ,  $V_{LOGIC}$  because it minimizes the power-up glitch.

It is recommended to connect AGND and DGND together and have a single solid ground plane. The exposed pad under the chip must also be connected to the ground plane.

$AV_{DD}$  has a constant power consumption that is independent of the update rate. The main caution for this rail is ensuring that noise level is low in the high frequencies, where AC PSRR is lower.

$DV_{DD}$  has a variable power consumption that depends on the update rate and the SPI bus mode. Dynamic current has fast variations that cause the rail to be noisy. If  $DV_{DD}$  is derived from  $AV_{DD}$ , a filter is recommended in addition to the LDO to completely remove the effect on the DAC output.

$V_{LOGIC}$  has very low current demand that depends on the SPI bus mode and clock rate. Power consumption is maximum in readout operations in quad SPI mode.

The recommended decoupling for the supply rails and the analog lines is shown in Figure 94.

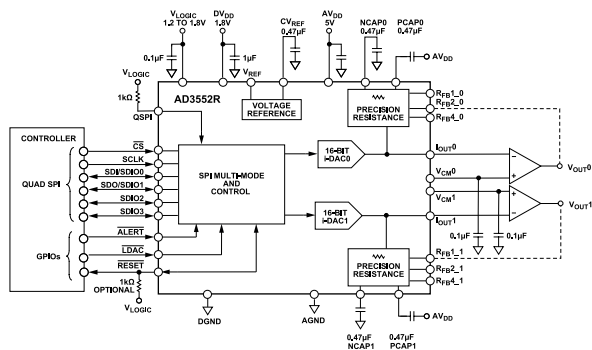


Figure 94. Recommended Application Circuit

The decoupling capacitors on  $PCAPx$ ,  $NCAPx$ ,  $V_{CMx}$ , and  $CV_{REF}$  can be adjusted to achieve the desired trade-off between noise corner frequency and power-up glitch amplitude.

Use capacitors with NP0 dielectric for the  $NCAPx$  and  $PCAPx$  feedback capacitors and any other capacitors on the path of the output voltage to avoid the derating caused by low frequency voltage variations. The decoupling capacitors for the supply rails,  $V_{CM}$  and  $CV_{REF}$ , can use materials with high dielectric constant because the voltage on these lines is constant.

## COMBINING DAC CHANNELS

The AD3552R allows for combining of the two DAC channels to produce a single output. This results in lower noise density and faster settling time with higher power consumption.

To implement this configuration, both  $I_{OUTx}$  pins must be connected together and the same  $R_{FBx,y}$  pins from both DACs must be connected together. However, the feedback capacitor does not need to be duplicated if there is a single amplifier. The  $V_{CMx}$  outputs can be combined using series resistors. An example for  $R_{FB2}$  is shown in Figure 95.

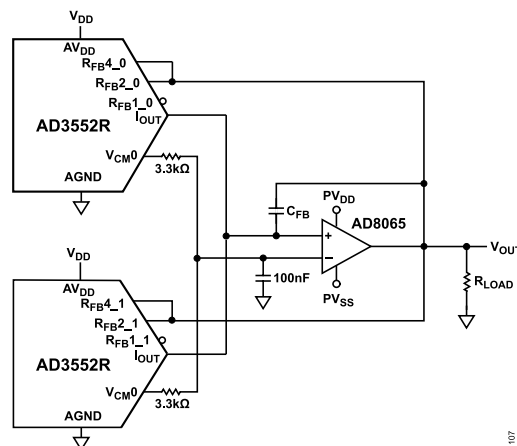


Figure 95. Dual DAC Configuration with  $R_{FB2\_x}$

To obtain the same voltage output as when using a single DAC, both DACs must be updated simultaneously with the same code. The most efficient way to do this is using the `DAC_PAGE` register for a direct update or the `INPUT_PAGE` register for an update via the `LDAC` pin or a software `LDAC` command.

## LAYOUT GUIDELINES

The pin configuration of the AD3552R, shown in Figure 13, is arranged in a way that facilitates the layout of the EVAL-AD3552R, which is shown in Figure 13. Most digital high speed lines are located on one side of the chip, with the analog functions of each DAC symmetrically distributed along the other three sides. This arrangement allows routing of the digital lines straight away from the analog functions, the placement of one amplifier on each side of the chip, and the external reference on the left side, as seen in Figure 96.

## APPLICATIONS INFORMATION

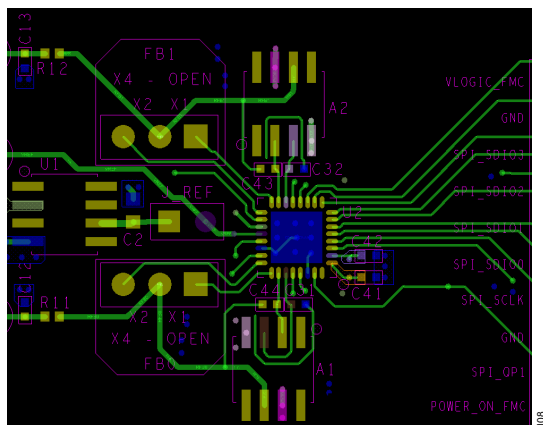


Figure 96. EVAL-AD3552R Component Arrangement and Layout

The following list is a few recommendations to observe to obtain the best performance:

- Keep  $I_{OUT}$  lines as short and thin as possible. This signal is responsible for the slewing of the amplifier to the final value. Therefore, the parasitic capacitance on this line increases the settling time. Use a feedback capacitor with a small footprint to minimize parasitic capacitance to the ground plane.
- Keep the  $I_{OUT}$  line away from repetitive signals, such as clocks and analog signals with high voltage excursion, because this is a high impedance line that can easily pick up electromagnetic interference.

- Connect the exposed pad of the AD3552R to the ground plane with several vias to minimize thermal drift. Note that the chip can dissipate up to 250 mW.
- Keep switching regulators and fast  $dV/dt$  signals away from the feedback loops of the DAC. Any  $\mu A$  induced on these lines becomes a mV at the output of the DAC.
- Do not overlap analog and digital signals. If a crossing cannot be avoided, it must be done at  $45^\circ$  or  $90^\circ$ .
- Route digital lines using traces with a constant characteristic impedance to avoid signal integrity problems that result in timing violations in DDR mode and crosstalk between signals. The traces must have a continuous ground plane underneath. When changing layers, ensure that the destination layer is referred to another ground plane and the traces have the same characteristic impedance. Place a via connecting both ground planes near the via of the digital line. If the destination layer is referred to a power plane, it must be continuous along the path of the line and a decoupling capacitor between power and ground must be placed close to the via of the digital line.

The drawing illustrates the JEDEC BGA package with the following details:

- TOP VIEW:** Shows a square package with a side length of 5.10. The exposed pad area is 5.00 SQ, and the overall area is 4.90. A shaded square in the top-left corner is labeled "PIN 1 INDICATOR AREA".
- SIDE VIEW:** Shows the package height with dimensions 1.00, 0.95, and 0.85. The base is labeled "SEATING PLANE". The top surface features a row of pins with a pitch of 0.05 MAX and a coplanarity of 0.08. A dimension of 0.20 REF is shown for the base thickness.
- DETAIL A:** A cross-sectional view of the package showing the "EXPOSED PAD" and "SOLDER TAIL". Dimensions include 0.30, 0.25, 0.18, 0.50 BSC, 0.50, 0.40, 0.30, 3.70, 3.60 SQ, 3.50, and 0.20 MIN. It also indicates "PIN 1 INDICATOR AREA OPTION (SEE DETAIL A)" and "DIE (JEDEC BGA)".
- NOTES:** A text block states: "FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET."
- COMPLIANCE:** The package is noted as "COMPLIANT TO JEDEC STANDARDS MO-220-VHDD-5".

Updated: October 29, 2021

| Model <sup>1</sup> | Temperature Range | Package Description      | Packing Quantity | Package Option |
|--------------------|-------------------|--------------------------|------------------|----------------|
| AD3552RBCPZ16      | −40°C to +105°C   | LFCSP:LEADFRM CHIP SCALE |                  | CP-32-30       |
| AD3552RBCPZ16-RL7  | −40°C to +105°C   | LFCSP:LEADFRM CHIP SCALE | Reel, 1500       | CP-32-30       |

| Model <sup>1</sup> | Description                                          |
|--------------------|------------------------------------------------------|
| EVAL-AD3552RFMC1Z  | AD3552R Evaluation Board optimized for Settling Time |
| EVAL-AD3552RFMC2Z  | AD3552R Evaluation Board optimized for DC Accuracy   |
| EVAL-SDP-CH1Z      | SDP High Speed Controller Board                      |



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