ESP32-C61 Series

Datasheet v1.0

32-bit RISC-V single-core microprocessor
2.4 GHz Wi-Fi 6 (IEEE 802.11ax)
Bluetooth® 5 (LE)
3.3 V flash or PSRAM in the chip's package
30 GPIOs
QFN40 (5×5 mm) or LGA40 (5×5 mm) Package

Including:

ESP32-C61HF4

ESP32-C61HR2

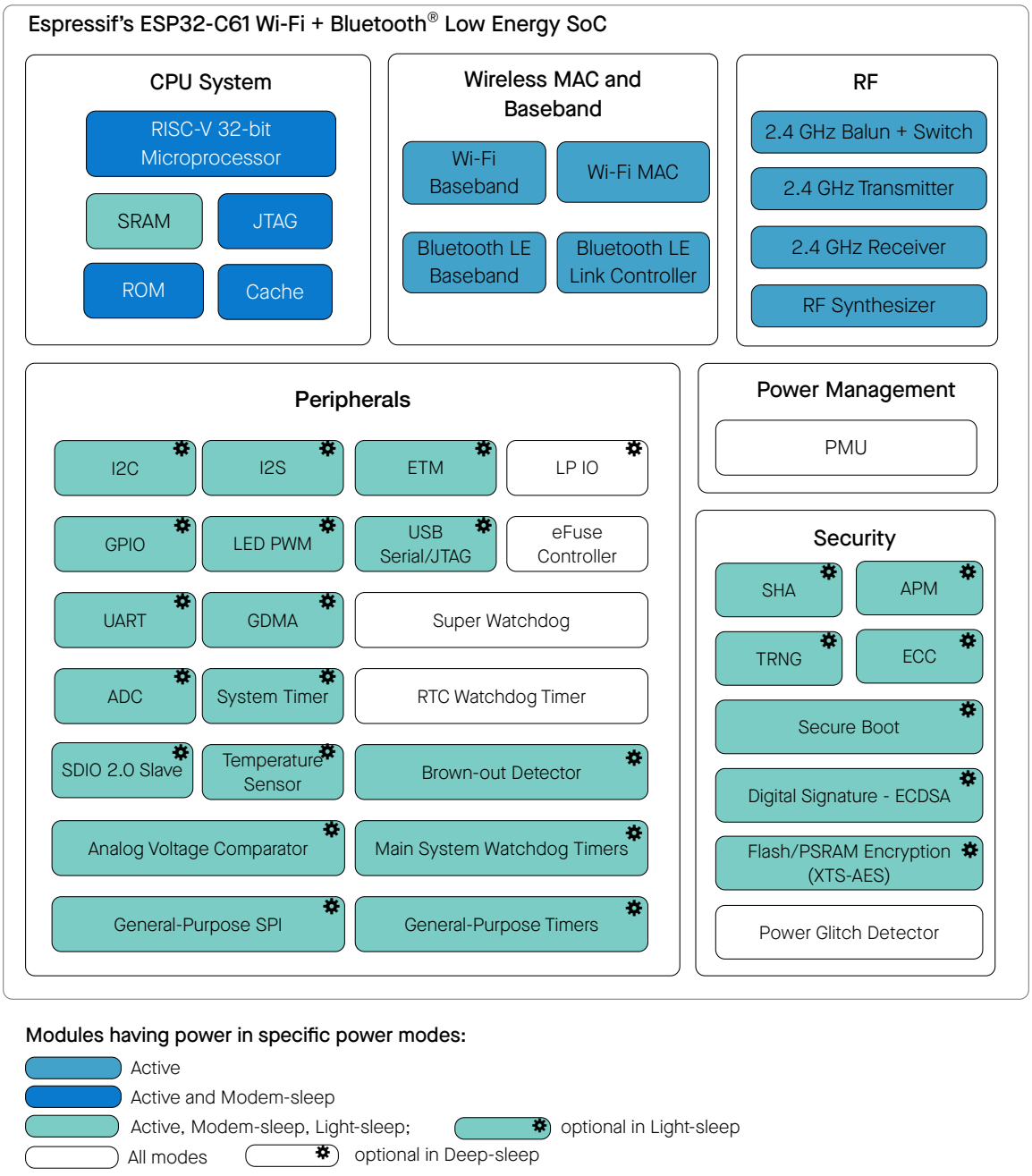
ESP32-C61HR8

ESP32-C61NF8R8LA

Product Overview

ESP32-C61 is a low-power MCU-based system on a chip (SoC). ESP32-C61 integrates 2.4 GHz Wi-Fi 6 and Bluetooth® Low Energy (Bluetooth LE). ESP32-C61 consists of a 32-bit RISC-V single-core microprocessor, a Wi-Fi baseband, a Bluetooth LE baseband, RF module, and numerous peripherals.

The functional block diagram of the SoC is shown below.



ESP32-C61 Functional Block Diagram

For more information on power consumption, see Section 4.1.3.7 *Power Management Unit*.

Features

Wi-Fi

- 1T1R in 2.4 GHz single band
- Operating frequency: 2412 ~ 2484 MHz
- IEEE 802.11ax-compliant
  - 20 MHz-only non-AP mode
  - Uplink and downlink OFDMA to enhance connectivity and performance in congested environments for IoT applications
  - Downlink MU-MIMO (multi-user, multiple input, multiple output) to increase network capacity
  - Beamformee that improves signal quality
  - Spatial reuse to maximize parallel transmissions
  - Target wake time (TWT) that optimizes power saving mechanisms
- Fully compatible with IEEE 802.11b/g/n protocol
  - 20 MHz and 40 MHz bandwidth
  - Data rate up to 150 Mbps
  - Wi-Fi Multimedia (WMM)
  - TX/RX A-MPDU, TX/RX A-MSDU
  - Immediate Block ACK
  - Fragmentation and defragmentation
  - Transmission opportunity (TXOP)
  - Automatic Beacon monitoring (hardware TSF)
  - Four virtual Wi-Fi interfaces
  - Simultaneous support for Infrastructure BSS in Station mode, SoftAP mode, Station + SoftAP mode, and promiscuous mode
    Note that when ESP32-C61 scans in Station mode, the SoftAP channel will change along with the Station channel
  - Antenna diversity
  - 802.11mc FTM

Bluetooth®

- Bluetooth LE: Bluetooth Core 6.0 certified
- Bluetooth mesh 1.1
- High power mode (20 dBm)
- Direction finding (AoA/AoD)

- Periodic advertising with responses (PAwR)
- LE connection subrating
- LE power control
- Speed: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps
- LE advertising extensions and multiple advertising sets
- Allow devices to operate in Broadcaster, Observer, Central, and Peripheral roles concurrently

CPU and Memory

- 32-bit RISC-V single-core processor:
  - Clock speed: up to 160 MHz
  - CoreMark® score at 160 MHz: 553.78 CoreMark; 3.46 CoreMark/MHz (O3)
  - Five-stage pipeline
- L1 cache (32 KB)
- ROM: 256 KB
- SRAM: 320 KB
- Supported SPI protocols: SPI, Dual SPI, Quad SPI, and QPI interfaces that allow connection to flash, external RAM, and other SPI devices
- Flash/external RAM controller with cache is supported
- Flash in-Circuit Programming (ICP) is supported

Advanced Peripheral Interfaces

- 30 programmable GPIOs
  - Five strapping GPIOs
- Digital interfaces:
  - Two SPI ports for communication with flash and PSRAM
  - General-purpose SPI port
  - Three UART
  - I2C
  - I2S
  - LED PWM controller, up to 6 channels
  - USB Serial/JTAG controller
  - SDIO 2.0 slave controller
  - General DMA controller, with 2 transmit channels and 2 receive channels
  - On-chip debug functionality via JTAG

  - Event task matrix (ETM)
- Analog interfaces:
  - 12-bit SAR ADC, up to 4 channels
  - Temperature sensor
  - Brown-out detector
  - Analog voltage comparator
- Timers:
  - Two 54-bit general-purpose timers
  - 52-bit system timer
  - Two main system watchdog timers
  - Three watchdog timers

Power Management

- Fine-resolution power control through a selection of clock frequency, duty cycle, Wi-Fi operating modes, and individual power control of internal components
- Four power modes designed for typical scenarios: Active, Modem-sleep, Light-sleep, Deep-sleep
- Power consumption in Deep-sleep mode is 10 μA

Security

- Secure boot - permission control on accessing internal and external memory
- Flash and PSRAM encryption - external memory encryption and decryption
- 4096-bit OTP, up to 1792 bits for users
- Cryptographic hardware acceleration:
  - Hash (FIPS PUB 180-4)
  - ECC (Curve P-192 and curve P-256 defined in FIPS 186-3 are supported)
  - Elliptic curve digital signature algorithm (ECDSA)
- True random number generator (TRNG)
- Power glitch detector

RF Module

- Antenna switches, RF balun, power amplifier, low-noise receive amplifier
- Up to +19.5 dBm of power for an 802.11ax transmission
- Up to +21 dBm of power for an 802.11b transmission
- Up to –106 dBm receiver sensitivity for Bluetooth LE (125 Kbps)

Applications

With low power consumption, ESP32-C61 is an ideal choice for IoT devices in the following areas:

- Smart Home
- Industrial Automation
- Health Care
- Consumer Electronics
- Smart Agriculture
- POS Machines
- Service Robot
- Audio Devices
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers

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1 ESP32-C61 Series Comparison

1.1 Nomenclature

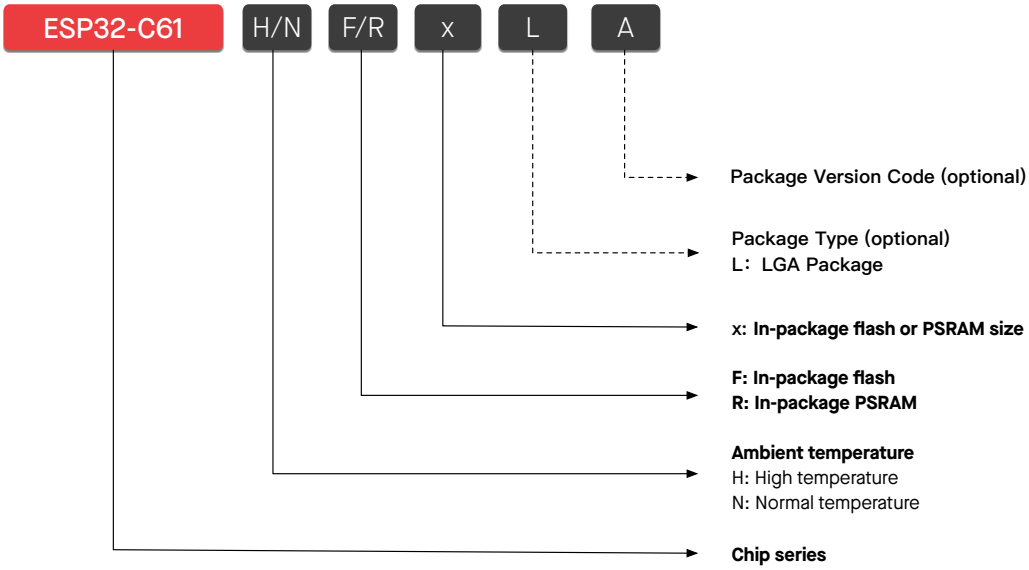

Figure 1-1. ESP32-C61 Series Nomenclature

1.2 Comparison

Table 1-1. ESP32-C61 Series Comparison

Part Number	In-Package Flash	In-Package PSRAM	Ambient Temp.[1]	Off-Package Flash	Off-Package PSRAM
ESP32-C61HF4	4 MB (Quad SPI)[2]	—	–40 ~ 105 °C	—	—
ESP32-C61HR2	—	2 MB (Quad SPI)	–40 ~ 105 °C	Supported	—
ESP32-C61HR8	—	8 MB (Quad SPI)	–40 ~ 105 °C	Supported	—
ESP32-C61NF8R8LA[3]	8 MB (Quad SPI)	8 MB (Quad SPI)	–40 ~ 85 °C	—	—

[1] Ambient temperature specifies the recommended temperature range of the environment immediately outside an Espressif chip.

[2] For details about SPI modes, see Section 2.6 *Pin Mapping Between Chip and Flash/PSRAM*.

[3] This variant uses an LGA package and is not yet in mass production.

2 Pins

2.1 Pin Layout

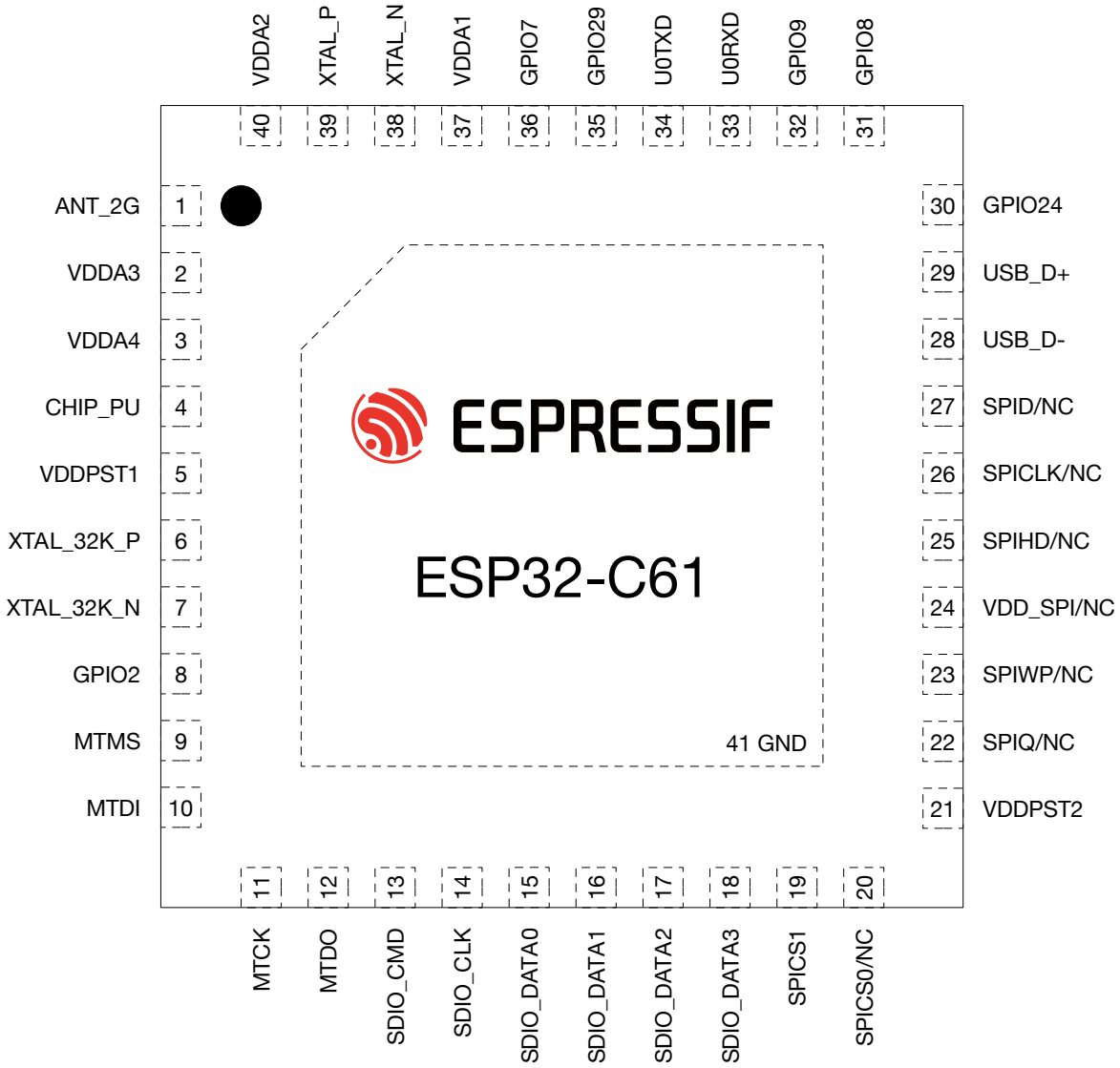

Figure 2-1. ESP32-C61HR2 & ESP32-C61HR8 & ESP32-C61HF4 Pin Layout (Top View)

Notice: For ESP32-C61HF4, SPICS0, SPIQ, SPIWP, VDD_SPI, SPIHD, SPICLK, and SPID pins are not connected (NC).

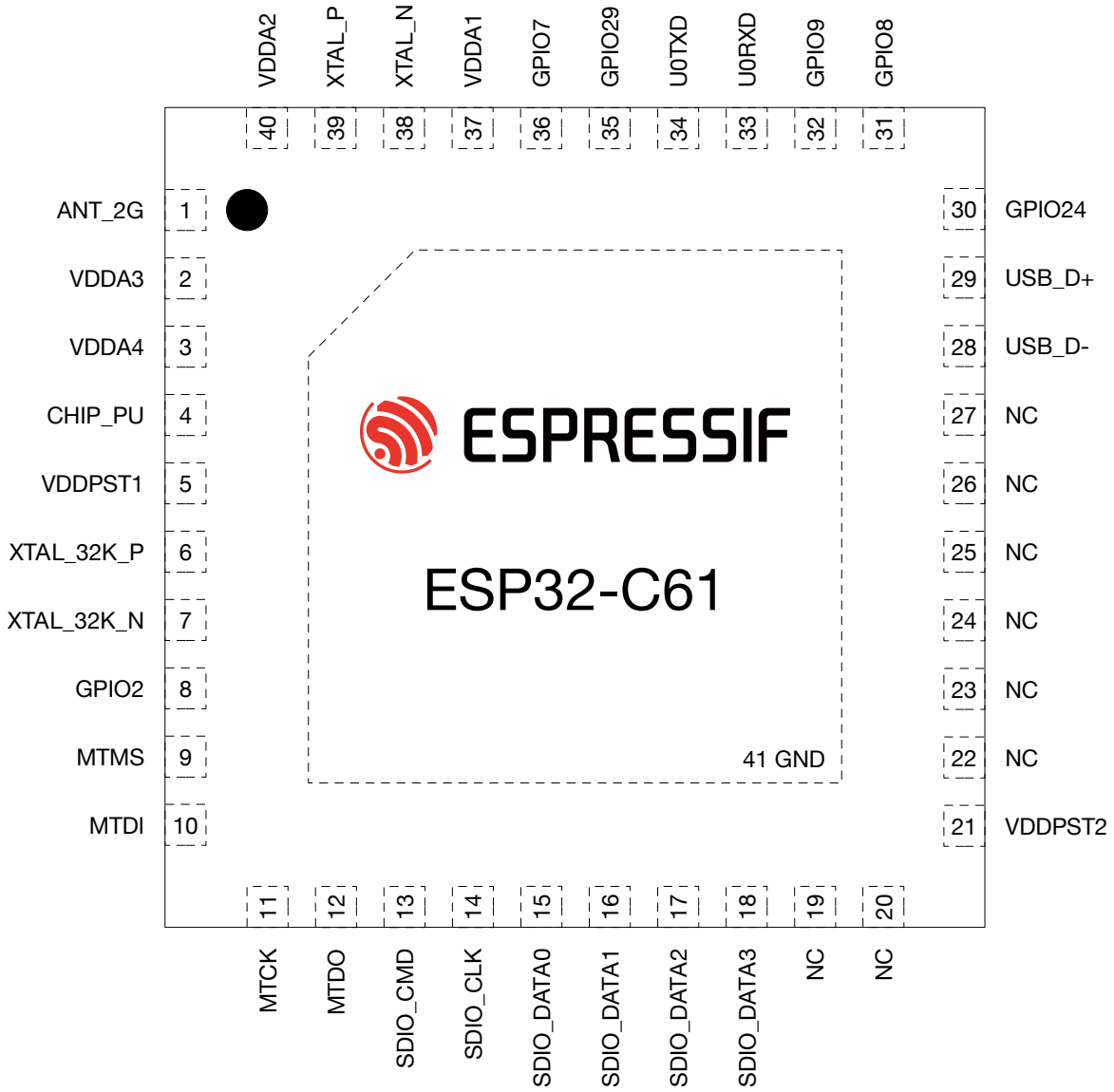

Figure 2-2. ESP32-C61NF8R8LA Pin Layout (Top View)

2.2 Pin Overview

The ESP32-C61 chip integrates multiple peripherals that require communication with the outside world. To keep the chip package size reasonably small, the number of available pins has to be limited. So the only way to route all the incoming and outgoing signals is through pin multiplexing. Pin muxing is controlled via software programmable registers.

All in all, the ESP32-C61 chip has the following types of pins:

- **IO pins** with the following predefined sets of functions to choose from:
  - **Each** IO pin has predefined **IO MUX functions** – see Table 2-3 *IO MUX Functions*
  - **Some** IO pins have predefined **LP IO MUX functions** – see Table 2-4 *LP IO MUX Functions*
  - **Some** IO pins have predefined **analog functions** – see Table 2-6 *Analog Functions*

  Predefined functions means that each IO pin has a set of direct connections to certain signals from on-chip peripherals. During run-time, the user can configure which peripheral signal from a predefined set to connect to a certain pin at a certain time via memory mapped registers.
- **Analog pins** that have exclusively-dedicated **analog functions** – see Table 2-7 *Analog Pins*
- **Power pins** that supply power to the chip components and non-power pins – see Table 2-8 *Power Pins*

Table 2-1 *Pin Overview* gives an overview of all the pins. For more information, see the respective sections for each pin type below, or Appendix A – ESP32-C61 Consolidated Pin Overview.

Table 2-1. ESP32-C61 Pin Overview

Pin No.	Pin Name	Pin Type	Pin Providing Power [2]	Pin Settings [3]		Pin Function Sets [1]		
				At Reset	After Reset	IO MUX	LP IO MUX	Analog
1	ANT_2G	Analog	–	–	–	–	–	–
2	VDDA3	Power	–	–	–	–	–	–
3	VDDA4	Power	–	–	–	–	–	–
4	CHIP_PU	I	VDDPST1	–	–	–	–	–
5	VDDPST1	Power	–	–	–	–	–	–
6	XTAL_32K_P	I/O/T	VDDPST1	–	–	**IO MUX**	LP IO MUX	Analog
7	XTAL_32K_N	I/O/T	VDDPST1	–	–	**IO MUX**	LP IO MUX	Analog
8	GPIO2	I/O/T	VDDPST1	–	–	**IO MUX**	LP IO MUX	–
9	MTMS	I/O/T	VDDPST1	IE	IE	**IO MUX**	LP IO MUX	Analog
10	MTDI	I/O/T	VDDPST1	IE	IE	**IO MUX**	LP IO MUX	Analog
11	MTCK	I/O/T	VDDPST1	–	IE	**IO MUX**	LP IO MUX	Analog
12	MTDO	I/O/T	VDDPST1	–	IE	**IO MUX**	LP IO MUX	–
13	SDIO_CMD	I/O/T	VDDPST2	–	IE	**IO MUX**	–	–
14	SDIO_CLK	I/O/T	VDDPST2	–	IE	**IO MUX**	–	–
15	SDIO_DATA0	I/O/T	VDDPST2	–	IE	**IO MUX**	–	–
16	SDIO_DATA1	I/O/T	VDDPST2	–	IE	**IO MUX**	–	–
17	SDIO_DATA2	I/O/T	VDDPST2	–	IE	**IO MUX**	–	–
18	SDIO_DATA3	I/O/T	VDDPST2	–	IE	**IO MUX**	–	–
19	SPICS1 [5]	I/O/T	VDD_SPI/VDDPST2	–	–	**IO MUX**	–	–
20	SPICS0 [4,5]	I/O/T	VDD_SPI/VDDPST2	–	–	**IO MUX**	–	–

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Table 2-1 – cont'd from previous page

Pin No.	Pin Name	Pin Type	Pin Providing Power [2]	Pin Settings [3]		Pin Function Sets [1]		
				At Reset	After Reset	IO MUX	LP IO MUX	Analog
21	VDDPST2	Power	–	–	–	–	–	–
22	SPIQ [4,5]	I/O/T	VDD_SPI/VDDPST2	–	–	**IO MUX**	–	–
23	SPIWP [4,5]	I/O/T	VDD_SPI/VDDPST2	–	–	**IO MUX**	–	–
24	VDD_SPI [5]	Power	VDDPST2	–	–	IO MUX	–	**Analog**
25	SPIHD [4,5]	I/O/T	VDD_SPI/VDDPST2	–	–	**IO MUX**	–	–
26	SPICLK [4,5]	O	VDD_SPI/VDDPST2	–	–	**IO MUX**	–	–
27	SPID [4,5]	I/O/T	VDD_SPI/VDDPST2	–	–	**IO MUX**	–	–
28	USB_D-	I/O/T	VDDPST2	–	IE	IO MUX	–	**Analog**
29	USB_D+	I/O/T	VDDPST2	–	IE,WPU	IO MUX	–	**Analog**
30	GPIO24	I/O/T	VDDPST2	–	–	**IO MUX**	–	–
31	GPIO8	I/O/T	VDDPST2	IE	IE	**IO MUX**	–	Analog
32	GPIO9	I/O/T	VDDPST2	IE,WPU	IE,WPU	**IO MUX**	–	Analog
33	U0RXD	I/O/T	VDDPST2	–	IE,WPU	**IO MUX**	–	–
34	U0TXD	I/O/T	VDDPST2	–	IE,WPU	**IO MUX**	–	–
35	GPIO29	I/O/T	VDDPST2	–	–	**IO MUX**	–	–
36	GPIO7	I/O/T	VDDPST2	IE	IE	**IO MUX**	–	–
37	VDDA1	Power	–	–	–	–	–	–
38	XTAL_N	Analog	–	–	–	–	–	–
39	XTAL_P	Analog	–	–	–	–	–	–
40	VDDA2	Power	–	–	–	–	–	–

1. **Bold** marks the pin function set in which a pin has its default function in the default boot mode. See Section 3.1 *Chip Boot Mode Control*.
2. Except for GPIO12 and GPIO13 whose default drive strength is 40 mA, the default drive strength for all the other pins is 20 mA.
3. Column **Pin Settings** shows predefined settings at reset and after reset with the following abbreviations:
   - IE – input enabled
   - WPU – internal weak pull-up resistor enabled
   - WPD – internal weak pull-down resistor enabled
   - USB_PU – USB pull-up resistor enabled
     - By default, the USB function is enabled for USB pins (i.e., GPIO12 and GPIO13), and the pin pull-up is decided by the USB pull-up resistor. This resistor is controlled by USB_SERIAL_JTAG_DP/DM_PULLUP and the pull-up value is managed by USB_SERIAL_JTAG_PULLUP_VALUE.
     - When the USB function is disabled, USB pins are used as regular GPIOs and the pin's internal weak pull-up and pull-down resistors are disabled by default (configurable by IO_MUX_FUN_WPU/WPD).
4. For ESP32-C61HF4, the SPICS0, SPIQ, SPIWP, VDD_SPI, SPIHD, SPICLK, and SPID pins are not connected (NC).
5. For ESP32-C61NF8R8LA, the SPICS1, SPICS0, SPIQ, SPIWP, VDD_SPI, SPIHD, SPICLK, and SPID pins are not connected (NC).

2.3 IO Pins

2.3.1 IO MUX Functions

The IO MUX allows multiple input/output signals to be connected to a single input/output pin. Each IO pin of ESP32-C61 can be connected to one of the three signals (IO MUX functions, i.e., F0–F2), as listed in Table 2-3 *IO MUX Functions*.

Among the three sets of signals:

- Some are routed via the GPIO Matrix (**GPIO0, GPIO1, etc.**), which incorporates internal signal routing circuitry for mapping signals programmatically. It gives the pin access to almost any peripheral signals. However, the flexibility of programmatic mapping comes at a cost as it might affect the latency of routed signals.
- Some are directly routed from certain peripherals (**U0TXD, MTCK, etc.**), including UART0, JTAG, SPI0/1, SPI2 and SDIO 2.0 Slave - see Table 2-2 *IO MUX Functions*.

Table 2-2. Peripheral Signals Routed via IO MUX

Pin Function	Signal	Description
U0TXD U0RXD	Transmit data Receive data	UART0 interface
MTCK MTDO MTDI MTMS	Test clock Test data out Test data in Test mode select	JTAG interface for debugging
SPIQ SPID SPIHD SPIWP SPICLK SPICS...	Data out Data in Hold Write protect Clock Chip select	3.3 V SPI0/1 interface for connection to in-package or off-package-flash/PSRAM via the SPI bus. It supports 1-, 2-, 4-line SPI modes. See also Section 2.6 *Pin Mapping Between Chip and Flash/PSRAM*
FSPIQ FSPID FSPIHD FSPIWP FSPICLK FSPICS0	Data out Data in Hold Write protect Clock Chip select	SPI2 interface for fast SPI connection. It supports 1-, 2-, 4-line SPI modes
SDIO_CLK SDIO_CMD SDIO_DATA...	Clock Command Data	The Secure Digital Input Output (SDIO) interface for connecting to an external SDIO host

Table 2-3 *IO MUX Functions* shows the IO MUX functions of IO pins.

Table 2-3. IO MUX Pin Functions

Pin No.	IO MUX / GPIO Name [2]	IO MUX Function [1, 2]					
		F0	Type	F1	Type	F2	Type
6	XTAL_32K_P	GPIO0	I/O/T	**GPIO0**	I/O/T		

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Table 2-3 – cont'd from previous page

Pin No.	IO MUX / GPIO Name [2]	IO MUX Function [1, 2]					
		F0	Type	F1	Type	F2	Type
7	XTAL_32K_N	GPIO1	I/O/T	**GPIO1**	I/O/T		
8	GPIO2	GPIO2	I/O/T	**GPIO2**	I/O/T	FSPIQ	I1/O/T
9	MTMS	**MTMS**	I1	GPIO3	I/O/T	FSPIHD	I1/O/T
10	MTDI	**MTDI**	I1	GPIO4	I/O/T	FSPIWP	I1/O/T
11	MTCK	**MTCK**	I1	GPIO5	I/O/T		
12	MTDO	**MTDO**	O/T	GPIO6	I/O/T	FSPICLK	I1/O/T
13	SDIO_CMD	SDIO_CMD	I1/O/T	**GPIO25**	I/O/T		
14	SDIO_CLK	SDIO_CLK	I1	**GPIO26**	I/O/T		
15	SDIO_DATA0	SDIO_DATA0	I1/O/T	**GPIO27**	I/O/T		
16	SDIO_DATA1	SDIO_DATA1	I1/O/T	**GPIO28**	I/O/T		
17	SDIO_DATA2	SDIO_DATA2	I1/O/T	**GPIO22**	I/O/T		
18	SDIO_DATA3	SDIO_DATA3	I1/O/T	**GPIO23**	I/O/T		
19	SPICS1/NC	**SPICS1**	O/T	GPIO14	I/O/T		
20	SPICS0/NC	**SPICS0**	O/T	GPIO15	I/O/T		
22	SPIQ/NC	**SPIQ**	I1/O/T	GPIO16	I/O/T		
23	SPIWP/NC	SPIWP	I1/O/T	**GPIO17**	I/O/T		
24	VDD_SPI/NC	GPIO18	I/O/T	GPIO18	I/O/T		
25	SPIHD/NC	SPIHD	I1/O/T	**GPIO19**	I/O/T		
26	SPICLK/NC	**SPICLK**	O/T	GPIO20	I/O/T		
27	SPID/NC	**SPID**	I1/O/T	GPIO21	I/O/T		
28	USB_D-	GPIO12	I/O/T	GPIO12	I/O/T		
29	USB_D+	GPIO13	I/O/T	GPIO13	I/O/T		
30	GPIO24	GPIO24	I/O/T	**GPIO24**	I/O/T		
31	GPIO8	GPIO8	I/O/T	**GPIO8**	I/O/T	FSPICS0	I1/O/T
32	GPIO9	GPIO9	I/O/T	**GPIO9**	I/O/T		
33	U0RXD	**U0RXD**	I1	GPIO10	I/O/T		
34	U0TXD	**U0TXD**	O	GPIO11	I/O/T		
35	GPIO29	GPIO29	I/O/T	**GPIO29**	I/O/T		
36	GPIO7	GPIO7	I/O/T	**GPIO7**	I/O/T	FSPID	I1/O/T

[1] **Bold** marks the default pin functions in the default boot mode. See Section 3.1 *Chip Boot Mode Control*.

[2] Regarding highlighted cells, see Section 2.3.4 *Restrictions for GPIOs and LP GPIOs*.

[3] Each IO MUX function (F*n*, *n* = 0 ~ 2) is associated with a *type*. The description of *type* is as follows:

- I – input. O – output. T – high impedance.
- I1 – input; if the pin is assigned a function other than F*n*, the input signal of F*n* is always `1`.
- I0 – input; if the pin is assigned a function other than F*n*, the input signal of F*n* is always `0`.

2.3.2 LP IO MUX Functions

The LP IO MUX function is activated when the HP digital system is shut down, thereby saving power.

Table 2-4. LP IO MUX Functions

Pin No.	LP IO Name	LP IO MUX Function F0
6	LP_GPIO0	LP_GPIO0
7	LP_GPIO1	LP_GPIO1
8	LP_GPIO2	LP_GPIO2
9	LP_GPIO3	LP_GPIO3
10	LP_GPIO4	LP_GPIO4
11	LP_GPIO5	LP_GPIO5
12	LP_GPIO6	LP_GPIO6

2.3.3 Analog Functions

Some IO pins also have **analog functions**, for analog peripherals (such as ADC) in any power mode. Internal analog signals are routed to these analog functions, see Table 2-5 *Analog Functions*.

Table 2-5. Analog Signals Routed to Analog Functions

Pin Function	Signal	Description
ADC1_CH*n*	ADC1 channel *n* signal	ADC1 channel *n* interface
XTAL_32K_N XTAL_32K_P	Negative clock signal Positive clock signal	The differential clock input of the chip, connecting to the 32 kHz differential clock output of the external crystal
USB_D- USB_D+	USB data differential signal	USB Serial/JTAG function
ZCD*n*	Voltage from GPIO Pad	Analog Pad voltage comparator interface

Table 2-6 *Analog Functions* shows the analog functions of IO pins.

Table 2-6. Analog Functions

Pin No.	Analog IO Name [1, 2]	Analog Function [3]	
		F0	F1
6	XTAL_32K_P	XTAL_32K_P	–
7	XTAL_32K_N	XTAL_32K_N	ADC1_CH0
9	MTMS	–	ADC1_CH1
10	MTDI	–	ADC1_CH2
11	MTCK	–	ADC1_CH3
28	USB_D-	**USB_D-** [1]	–
29	USB_D+	**USB_D+**	–
24	VDD_SPI	**VDD_SPI**	–
31	GPIO8 [2]	ZCD0	–
32	GPIO9	ZCD1	–

[1] **Bold** marks the default pin functions in the default boot mode. See Section 3.1 *Chip Boot Mode Control*.

[2] Regarding highlighted cells, see Section 2.3.4 *Restrictions for GPIOs and LP GPIOs*.

2.3.4 Restrictions for GPIOs and LP GPIOs

All IO pins of ESP32-C61 have GPIO and some have RTC_GPIO pin functions. However, the IO pins are multiplexed and can be configured for different purposes based on the requirements. Some IOs have restrictions for usage. It is essential to consider the multiplexed nature and the limitations when using these IO pins.

In tables of this chapter, some pin functions are highlighted. The non-highlighted GPIO or RTC_GPIO pins are recommended for use first. If more pins are needed, the highlighted GPIOs or RTC_GPIOs should be chosen carefully to avoid conflicts with important pin functions.

The highlighted IO pins have the following important pin functions:

- GPIO – allocated for communication with in-package flash/PSRAM and NOT recommended for other uses. For details, see Section 2.6 *Pin Mapping Between Chip and Flash/PSRAM*.
- GPIO – have one of the following important functions:
  - **Strapping pins** – need to be at certain logic levels at startup. See Section 3 *Boot Configurations*.
  - **USB_D+/-** – by default, connected to the USB Serial/JTAG Controller. To function as GPIOs, these pins need to be reconfigured.
  - **JTAG interface** – often used for debugging. See Table 2-2 *IO MUX Functions*. To free these pins up, the pin functions USB_D+/- of the USB Serial/JTAG Controller can be used instead. See also Section 3.4 *JTAG Signal Source Control*.
  - **UART interface** – often used for debugging. See Table 2-2 *IO MUX Functions*.

See also Appendix A – ESP32-C61 Consolidated Pin Overview.

2.4 Analog Pins

Table 2-7. Analog Pins

Pin No.	Pin Name	Pin Type	Pin Function
1	ANT_2G	I/O	RF input/output
4	CHIP_PU	—	High: on, enables the chip (powered up). Low: off, disables the chip (powered down). Note: Do not leave the CHIP_PU pin floating.
38	XTAL_N	—	External clock input/output connected to chip's crystal. P/N means differential clock positive/negative.
39	XTAL_P	—	

2.5 Power Supply

2.5.1 Power Pins

The chip is powered via the power pins described in Table 2-8 *Power Pins*.

Table 2-8. Power Pins

Pin No.	Pin Name	Direction	Power Supply [1,2] Power Domain / Other	IO Pins [3]
2	VDDA3	Input	Analog power domain	
3	VDDA4	Input	Analog power domain	
5	VDDPST1	Input	HP digital and part of LP digital power domains	LP IO
24	VDD_SPI	Output	A power supply from VDDPST2 used to power the flash	
21	VDDPST2	Input	HP digital power domain	HP IO
37	VDDA1	Input	Analog power domain	
40	VDDA2	Input	Analog power domain	
41	GND	—	External ground connection	

[1] See in conjunction with Section 2.5.2 *Power Scheme*.

[2] For recommended and maximum voltage and current, see Section 5.1 *Absolute Maximum Ratings* and Section 5.2 *Recommended Operating Conditions*.

[3] LP IO pins are those powered by VDDPST1 and so on, as shown in Figure 2-3 *ESP32-C61 Power Scheme*. See also Table 2-1 *Pin Overview* > Column *Pin Providing Power*.

2.5.2 Power Scheme

The power scheme is shown in Figure 2-3 *ESP32-C61 Power Scheme*.

The components on the chip are powered via voltage regulators.

Table 2-9. Voltage Regulators

Voltage Regulator	Output	Power Supply
HP	1.1 V	HP power domain
LP	1.1 V	LP power domain

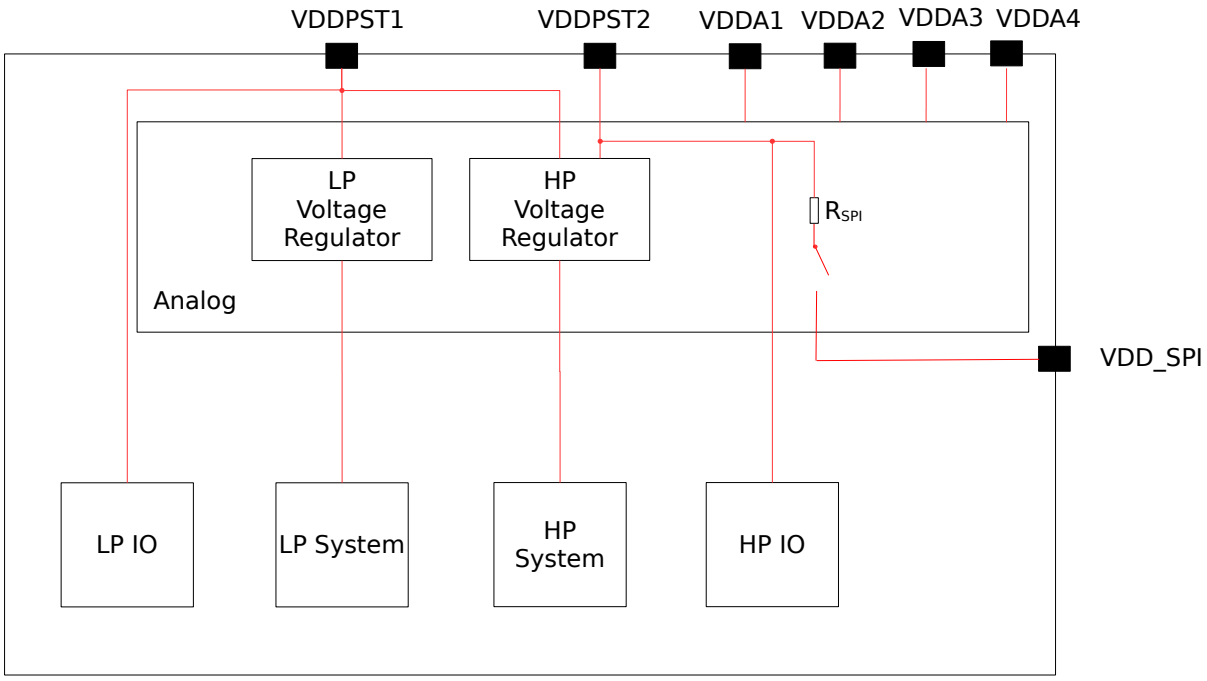

Figure 2-3. ESP32-C61 Power Scheme

2.5.3 Chip Power-up and Reset

Once the power is supplied to the chip, its power rails need a short time to stabilize. After that, CHIP_PU – the pin used for power-up and reset – is pulled high to activate the chip. For information on CHIP_PU as well as power-up and reset timing, see Figure 2-4 and Table 2-10.

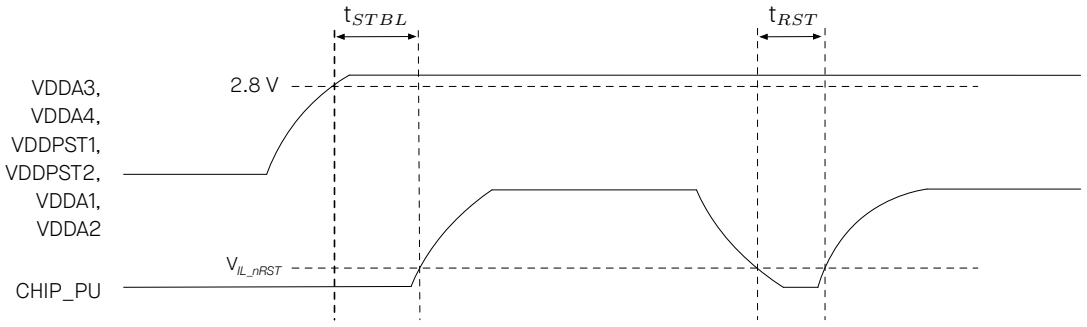

Figure 2-4. Visualization of Timing Parameters for Power-up and Reset

Table 2-10. Description of Timing Parameters for Power-up and Reset

Parameter	Description	Min (μs)
t_{STBL}	Time reserved for the power rails of VDDA3, VDDA4, VDDPST1, VDDPST2, VDDA1 and VDDA2 to stabilize before the CHIP_PU pin is pulled high to activate the chip	50
t_{RST}	Time reserved for CHIP_PU to stay below V_{IL_nRST} to reset the chip	50

2.6 Pin Mapping Between Chip and Flash/PSRAM

Table 2-11 lists the pin mapping between the chip and flash/PSRAM for all SPI modes.

For chip variants with in-package flash/PSRAM (see Table 1-1 *Comparison*), the pins allocated for communication with in-package flash/PSRAM can be identified depending on the SPI mode used. The recommended pins for connecting to off-package flash/PSRAM can be found in table below.

For variants with in-package flash/PSRAM, the in-package flash or PSRAM must be powered by VDD_SPI, and the corresponding pin cannot be used as a digital function pin.

For off-package flash or PSRAM, the power supply is optional. It can be provided either by VDD_SPI or by an external power source supplied by the user. In general, if VDD_SPI is used to power flash or PSRAM, then the pin cannot be used as a digital function pin.

For more information on SPI controllers, see also Section 4.2.1.2 *SPI Controller*.

Notice:

It is not recommended to use the pins connected to flash/PSRAM for any other purposes.

Table 2-11. Pin Mapping Between Chip and Off-Package Flash for ESP32-C61[1]

Pin No.	Pin Name	Single SPI Flash	Dual SPI Flash	Quad SPI Flash
26	SPICLK	CLK	CLK	CLK
20	SPICS0 [2]	CS#	CS#	CS#
27	SPID	MOSI	SIO0 [3]	SIO0
22	SPIQ	MISO	SIO1	SIO1
23	SPIWP	WP#		SIO2
25	SPIHD	HOLD#		SIO3

[1] An off-package flash can only be connected if the chip variant does not have in-package flash.

[2] SPICS0 is used to access flash

[3] SIO: Serial Data Input and Output

Table 2-12. Pin Mapping Between Chip and Off-Package PSRAM[1]

QFN48 Pin No.	Pin Name	Single SPI PSRAM	Quad SPI PSRAM
26	SPICLK	CLK	CLK
19	SPICS1 [2]	CE#	CE#
27	SPID	SI [3]	SIO0
22	SPIQ	SO [4]	SIO1
23	SPIWP		SIO2
25	SPIHD		SIO3

[1] An off-package PSRAM can only be connected if the chip variant does not have in-package PSRAM. If PSRAM is not connected, these pins cannot be used as GPIO pins.

[2] SPICS1 is used to access PSRAM

[3] SI: Serial Data Input, equivalent to MOSI

[4] SO: Serial Data Output, equivalent to MISO

3 Boot Configurations

The chip allows for configuring the following boot parameters through strapping-pins and eFuse parameter at power-up or a hardware reset, without microcontroller interaction.

- **Chip boot mode**
  - Strapping pin: GPIO8 and GPIO9
- **SDIO sampling and driving clock edge**
  - Strapping pin: MTDI and MTMS
- **ROM message printing**
  - Strapping pin: GPIO8
  - eFuse parameter: EFUSE_UART_PRINT_CONTROL and EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
- **JTAG signal source**
  - Strapping pin: GPIO7
  - eFuse parameter: EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_JTAG_SEL_ENABLE

The default values of all the above eFuse parameters are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once programmed to 1, it can never be reverted to 0.

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Table 3-1. Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
MTMS	Floating	–
MTDI	Floating	–
GPIO7	Floating	–
GPIO8	Floating	–
GPIO9	Pull-up	1

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances. If the ESP32-C61 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

The timing of signals connected to the strapping pins should adhere to the *setup time* and *hold time* specifications in Table 3-2 and Figure 3-1.

Table 3-2. Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_{H}	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

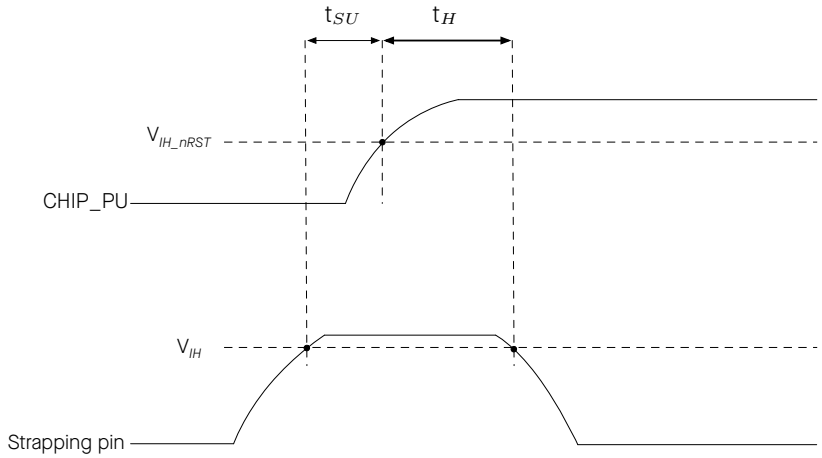

Figure 3-1. Visualization of Timing Parameters for the Strapping Pins

3.1 Chip Boot Mode Control

GPIO8 and GPIO9 control the boot mode after the reset is released. See Table 3-3 *Chip Boot Mode Control*.

Table 3-3. Chip Boot Mode Control

Boot Mode	GPIO8	GPIO9
SPI Boot [1]	Any value	1
Joint Download Boot[2]	1	0

[1] **Bold** marks the default value and configuration.

[2] Joint Download Boot mode supports the following download methods:

- USB-Serial-JTAG Download Boot
- UART Download Boot
- SDIO Slave 2.0 Download Boot

In SPI Boot mode, the ROM bootloader loads and executes the program from SPI flash to boot the system.

In Joint Download Boot mode, users can download binary files into flash using UART0, USB or SDIO Slave interfaces and execute it in SPI Boot mode.

In Joint Download Boot mode, it is also possible to download binary files into SRAM using UART0, USB or SDIO Slave interfaces and execute it from SRAM.

3.2 SDIO Sampling and Driving Clock Edge Control

The strapping pin MTMS and MTDI can be used to decide on which clock edge to sample signals and drive output lines. See Table 3-4 *SDIO Input Sampling Edge/Output Driving Edge Control*.

Table 3-4. SDIO Input Sampling Edge/Output Driving Edge Control

Edge behavior	MTMS	MTDI
Falling edge sampling, falling edge output	0	0
Falling edge sampling, rising edge output	0	1
Rising edge sampling, falling edge output	1	0
Rising edge sampling, rising edge output	1	1

[1] MTMS and MTDI are floating by default, so above are not default configurations.

3.3 ROM Messages Printing Control

During the boot process, the messages by the ROM code can be printed to:

- **(Default) UART0 and USB Serial/JTAG controller**
- USB Serial/JTAG controller
- UART0

LP_AON_STORE4_REG[0], EFUSE_UART_PRINT_CONTROL and GPIO8 control ROM messages printing to **UART0** as shown in Table 3-5 *UART0 ROM Message Printing Control*.

Table 3-5. UART0 ROM Message Printing Control

UART0 ROM Code Printing	EFUSE_UART_PRINT_CONTROL	GPIO8	Register[1]
Always enabled[2]	**0**	Ignored	0
Enabled	1	0	
Disabled		1	
Disabled	2	0	
Enabled		1	
Always disabled	3	Ignored	
Disabled	Ignored	Ignored	1

[1] Register: LP_AON_STORE4_REG[0]

[2] **Bold** marks the default value and configuration.

EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT and LP_AON_STORE4_REG[0] control the printing to **USB Serial/JTAG controller** as shown in Table 3-6 *USB Serial/JTAG ROM Message Printing Control*.

Table 3-6. USB Serial/JTAG ROM Message Printing Control

USB Serial/JTAG ROM Message Printing Control	LP_AON_STORE4_REG[0]	EFUSE_DIS_USB_SERIAL_JTAG _ROM_PRINT
Enabled	**0**	**0**
Disabled	0	1
	1	Ignored

[1] **Bold** marks the default value and configuration.

3.4 JTAG Signal Source Control

The strapping pin GPIO7 can be used to control the source of JTAG signals during the early boot process. This pin does not have any internal pull resistors and the strapping value must be controlled by the external circuit that cannot be in a high impedance state.

As Table 3-7 shows, GPIO7 is used in combination with EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_JTAG_SEL_ENABLE.

Table 3-7. JTAG Signal Source Control

eFuse 1[1]	eFuse 2[2]	eFuse 3[3]	GPIO7	JTAG Signal Source
0	**0**	**0**	x[4]	**USB Serial/JTAG Controller**[5]
		1	1	
			0	JTAG pins MTDI, MTCK, MTMS and MTDO
0	x	x	x	
0	1	x	x	
1	0	x	x	USB Serial/JTAG Controller
1	1	x	x	JTAG is disabled
1	x	x	x	

[1] **eFuse 1**: EFUSE_DIS_PAD_JTAG

[2] **eFuse 2**: EFUSE_DIS_USB_JTAG

[3] **eFuse 3**: EFUSE_JTAG_SEL_ENABLE

[4] x: x indicates that the value has no effect on the result and can be ignored.

[5] **Bold** marks the default value and configuration.

4 Functional Description

4.1 System

This section describes the core of the chip's operation, covering its microprocessor, memory organization, system components, and security features.

4.1.1 Microprocessor and Master

This subsection describes the core processing units within the chip and their capabilities.

4.1.1.1 High-Performance CPU

The ESP-RISC-V CPU (HP CPU) is a high-performance 32-bit core based on the RISC-V instruction set architecture (ISA) comprising base integer (I), multiplication/division (M), atomic (A) and compressed (C) standard extensions.

Feature List

- Five-stage pipeline that supports an operating clock frequency up to 160 MHz
- RV32IMAC ISA (instruction set architecture)
- Zc extensions (Zcb, Zcmp, and Zcmt)
- Two-cycle pipelined multiplier and radix-4 SRT divider
- Compatible with RISC-V ISA Manual Volume I: Unprivileged ISA Version 2.2 and RISC-V ISA Manual, Volume II: Privileged Architecture, Version 1.10
- Zero wait cycle access to on-chip SRAM and cache for program and data access over IRAM/DRAM interface
- Branch predictor BHT, BTB, and RAS
- Compliant with RISC-V Core Local Interrupt (CLINT)
- Compliant with RISC-V Core-Local Interrupt Controller (CLIC)
- Two privilege modes: Machine (M) mode and User (U) mode
- Debug module (DM) compliant with the specification RISC-V External Debug Support Version 0.13 with external debugger support over an industry-standard JTAG/USB port
- Offline trace debug compliant with RISC-V Trace Specification v2.0, see Section 4.1.1.2 *RISC-V Trace Encoder*
- Hardware trigger compliant with the specification RISC-V External Debug Support Version 0.13 with up to three breakpoints/watchpoints
- Physical memory protection (PMP) and attributes (PMA) for up to 16 configurable regions

4.1.1.2 RISC-V Trace Encoder

The RISC-V Trace Encoder in the ESP32-C61 chip provides a way to capture detailed trace information from the High-Performance CPU's execution, enabling deeper analysis and optimization of the system. It connects to the HP CPU's instruction trace interface and compresses the information into smaller packets, which are then stored in internal SRAM.

Feature List

- Compatible with Efficient Trace for RISC-V Version 2.0
- Synchronization packets sent every few clock cycles or packets
- Zero bytes as anchor tags to identify boundaries between data packets
- Configurable memory writing mode: loop mode or non-loop mode
- Trace lost status to indicate packet loss
- Automatic restart after packet loss
- Support for delta address mode and full address mode
- Support for filter unit

4.1.1.3 GDMA Controller

The GDMA Controller is a General Direct Memory Access (GDMA) controller that allows peripheral-to-memory, memory-to-peripheral, and memory-to-memory data transfer without the CPU's intervention. The GDMA has four independent channels, two transmit channels and two receive channels. These channels are shared by peripherals with the GDMA feature, such as SPI2, I2S, SHA, and ADC.

Feature List

- Programmable length of data to be transferred in bytes
- Linked list of descriptors for efficient data transfer management
- INCR burst transfer when accessing internal RAM for improved performance
- Access to internal RAM and off-package PSRAM
- Software-configurable selection of peripheral requesting service
- Fixed-priority and round-robin channel arbitration schemes for managing bandwidth
- Support for Event Task Matrix

4.1.2 Memory Organization

This subsection describes the memory arrangement to explain how data is stored, accessed, and managed for efficient operation.

Figure 4-1 illustrates the address mapping structure of ESP32-C61.

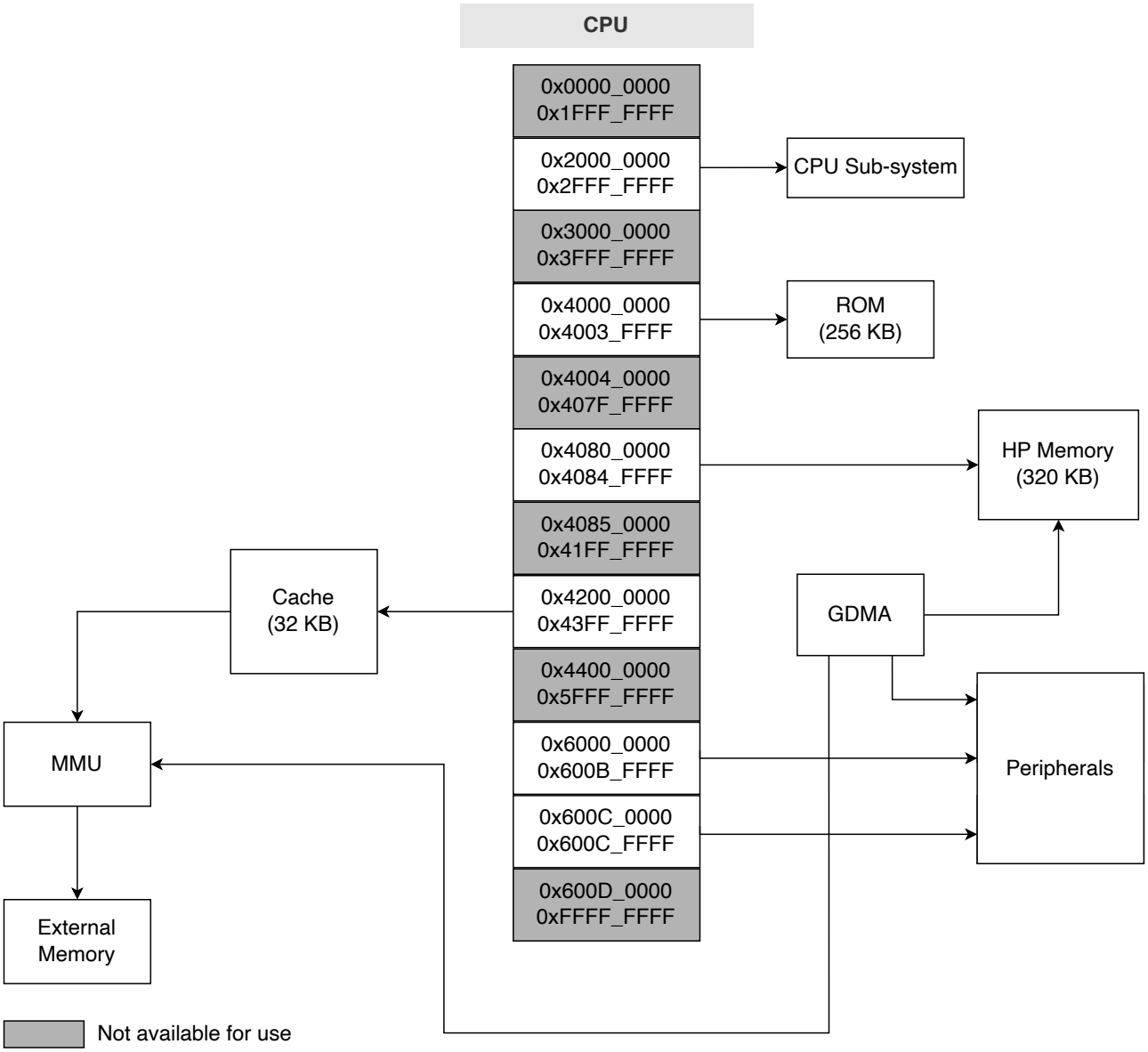

Figure 4-1. Address Mapping Structure

4.1.2.1 Internal Memory

The internal memory of ESP32-C61 refers to the memory integrated on the chip die or in the chip package, including ROM, SRAM, eFuse, flash, and PSRAM.

Feature List

- 256 KB of ROM for booting and core functions
- 320 KB of SRAM for data and instructions
- 4096-bit eFuse memory, with 1792 bits available for users
- In-package flash
  - See flash size in Chapter 1 *ESP32-C61 Series Comparison*
  - More than 100,000 program/erase cycles

  - More than 20 years of data retention time
  - Clock frequency up to 120 MHz
- In-package PSRAM
  - See PSRAM size in Chapter 1 *ESP32-C61 Series Comparison*
  - Clock frequency up to 120 MHz

4.1.2.2 External Memory

Some variants of ESP32-C61 allow connection to flash/PSRAM via the SPI, Dual SPI, Quad SPI, and QPI interfaces. For more information, please refer to Table 1-1.

CPU's instruction memory space and read-only data memory space can map into the flash/PSRAM of ESP32-C61, and the size of the flash/PSRAM can be 32 MB at most respectively. ESP32-C61 supports hardware encryption/decryption based on XTS-AES to protect developers' programs and data in the flash/PSRAM.

Feature List

Through the cache, ESP32-C61 can support at a time up to:

- 32 MB of instruction memory space which can map into the flash/PSRAM as individual blocks of 64/32/16 KB. 32-bit fetch is supported
- 32 MB of data memory space which can map into the flash/PSRAM as individual blocks of 64/32/16 KB. 8-bit, 16-bit, and 32-bit reads are supported by the flash. 8-bit, 16-bit, and 32-bit reads and writes are supported by the PSRAM

Note:
After ESP32-C61 is initialized, software can customize the mapping of flash/PSRAM into the CPU address space.

4.1.2.3 eFuse Controller

The eFuse memory is a one-time programmable memory that stores parameters and user data, and the eFuse controller of ESP32-C61 is used to program and read this eFuse memory.

Feature List

- Configure write protection for some blocks
- Configure read protection for some blocks
- Various hardware encoding schemes against data corruption

4.1.3 System Components

This subsection describes the essential components that contribute to the overall functionality and control of the system.

4.1.3.1 IO MUX and GPIO Matrix

The IO MUX and GPIO Matrix in the ESP32-C61 chip provide flexible routing of peripheral input and output signals to the GPIO pins. These peripherals enhance the functionality and performance of the chip by allowing the configuration of I/O, support for multiplexing, and signal synchronization for peripheral inputs.

Feature List

- 30 GPIO pins for general-purpose I/O or connection to internal peripheral signals
- GPIO matrix:
  - Routing 37 peripheral input and 57 output signals to any GPIO pin
  - Signal synchronization for peripheral inputs based on IO MUX operating clock
  - GPIO Filter hardware for input signal filtering
- IO MUX for directly connecting certain digital signals (SPI, JTAG, UART, SDIO) to pins
- Support for Event Task Matrix

4.1.3.2 Reset

The ESP32-C61 chip provides four types of reset that occur at different levels, namely CPU Reset, Core Reset, System Reset, and Chip Reset. Except for Chip Reset, all reset types preserve the data stored in internal memory.

Feature List

- Four types of reset:
  - CPU Reset – Resets the CPU core
  - Core Reset – Resets the whole digital system except for the LP system
  - System Reset – Resets the whole digital system, including the LP system
  - Chip Reset – Resets the whole chip
- Reset trigger:
  - Directly by hardware
  - Via software by configuring the corresponding registers of the CPU
- Support for retrieving reset cause

4.1.3.3 Clock

The ESP32-C61 chip has clocks sourced from oscillators, RC circuits, and PLL circuits, which are then processed by dividers or selectors. The clocks can be classified into high-speed clocks for devices working at higher frequencies and slow-speed clocks for low-power systems and some peripherals.

Feature List

- High-speed clocks for HP system
  - 40 MHz external crystal clock

    Note:

    * ESP32-C61 cannot operate without the external crystal clock.
    * ESP32-C61 can automatically filter out high-frequency glitches in the external main crystal clock.

  - 480 MHz internal PLL clock
- Slow-speed clocks for LP system and some peripherals working in low-power mode
  - 32 kHz external crystal clock (must be an external differential clock input, generally provided by a passive crystal)
  - Internal fast RC oscillator with adjustable frequency (20 MHz by default)
  - Internal slow RC oscillator with adjustable frequency (150 kHz by default)
  - External slow clock input through XTAL_32K_P (32 kHz by default, can be provided by an active oscillator or other sources)

Note:

- The 32 kHz external crystal clock and the external slow clock input through XTAL_32K_P cannot coexist; only one can be used at a time.

4.1.3.4 Interrupt Matrix

The Interrupt Matrix in the ESP32-C61 chip routes interrupt requests generated by various peripherals to CPU interrupts.

Feature List

- 53 peripheral interrupt sources accepted as input
- 32 CPU peripheral interrupts generated to CPU as output
- Current interrupt status query of peripheral interrupt sources
- Multiple interrupt sources mapping to a single CPU interrupt (i.e., shared interrupts)

4.1.3.5 Event Task Matrix

ESP32-C61 integrates an SoC ETM with multiple channels. Each input event on channels is mapped to an output task. Events are generated by peripherals, while tasks are received by peripherals.

Feature List

- Up to 50 mapping channels, each connected to an event and a task and controlled independently

- An event or a task can be mapped to any tasks or events in the matrix. That is to say, one event can be mapped to different tasks via multiple channels, or different events can be mapped to the same task via their individual channels
- Peripherals supporting ETM include GPIO, LED PWM, general-purpose timers, RTC Timer, system timer, temperature sensor, ADC, I2S, GDMA, and PMU

4.1.3.6 System Timer

The System Timer (SYSTIMER) in the ESP32-C61 chip is a 52-bit timer that can be used to generate tick interrupts for the operating system or as a general timer to generate periodic or one-time interrupts.

Feature List

- Two 52-bit counters and three 52-bit comparators
- 52-bit alarm values and 26-bit alarm periods
- Two modes to generate alarms: target mode and period mode
- Three comparators generating three independent interrupts based on configured alarm value or alarm period
- Ability to load back sleep time recorded by RTC timer via software after Deep-sleep or Light-sleep
- Counters can be stalled if the CPU is stalled or in OCD mode
- Real-time alarm events

4.1.3.7 Power Management Unit

The ESP32-C61 has an advanced Power Management Unit (PMU). It can be flexibly configured to power up different power domains of the chip to achieve the best balance between chip performance, power consumption, and wakeup latency.

Configuring the PMU is a complex procedure. To simplify power management for typical scenarios, there are the following **predefined power modes** that power up different combinations of power domains:

- **Active mode** – The CPU, RF circuits, and all peripherals are on. The chip can process data, receive, transmit, and listen.
- **Modem-sleep mode** – The CPU is on, but the clock frequency can be reduced. The wireless connections can be configured to remain active as RF circuits are periodically switched on when required.
- **Light-sleep mode** – The CPU stops running, and can be optionally powered on. The chip can be woken up via all wake up mechanisms: MAC, host, RTC timer, or external interrupts. Wireless connections can remain active. Some groups of digital peripherals can be optionally powered off.
- **Deep-sleep mode** – Only LP system is powered on

Figure 4-2 *Components and Power Domains* and the following Figure 4-3 Components and Power Domains Table show the distribution of chip components between power domains and power subdomains.

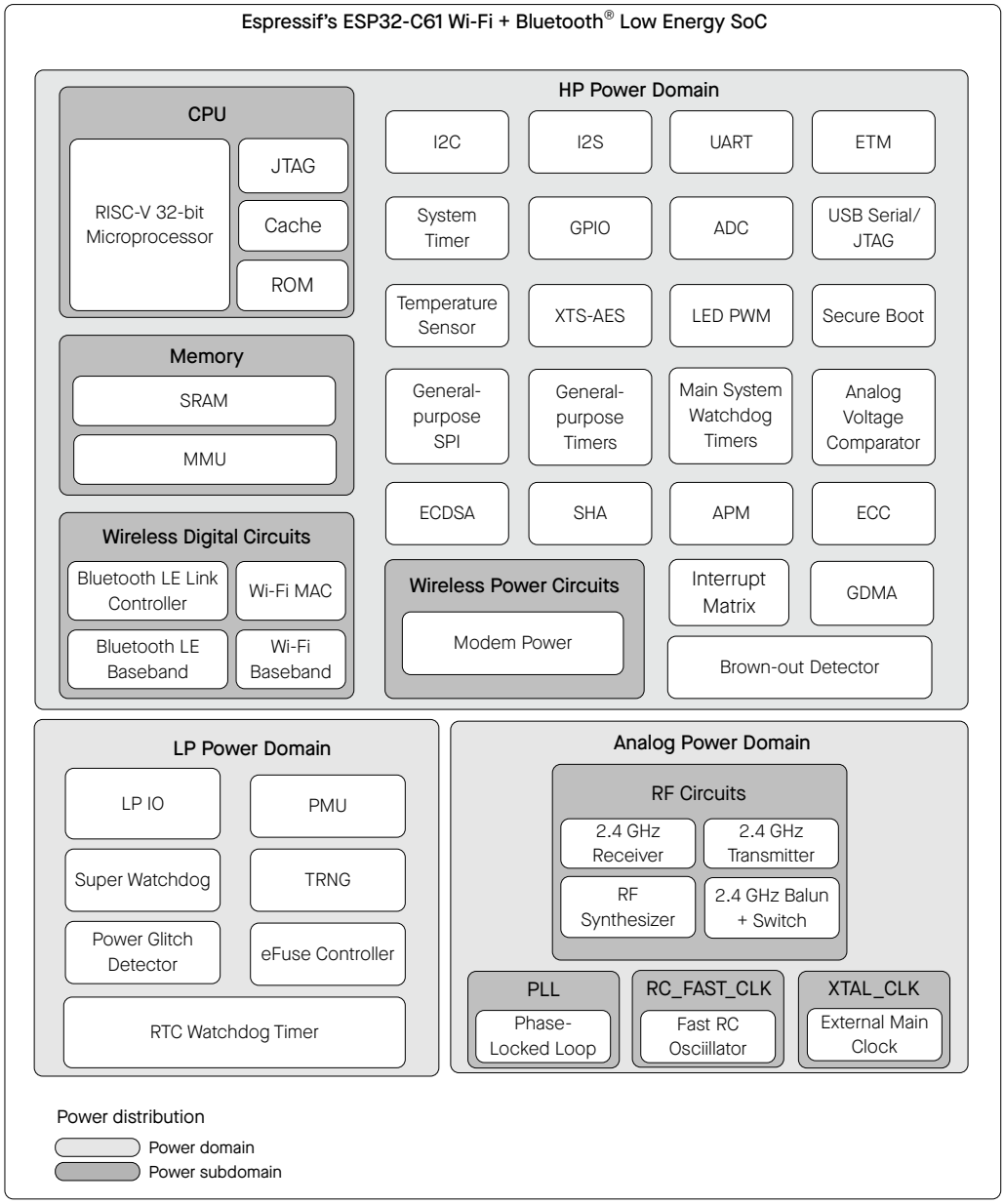

Figure 4-2. Components and Power Domains

Power Domain / Power mode	LP Power Domain		HP Power Domain					Analog Power Domain			
	Always-on	LP Peri	Memory	Wireless Pwr Circuits	CPU	Wireless Digital Curcuits	Others	RC_FAST_CLK	XTAL_CLK	PLL	RF Circuits
Active	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
Modem_sleep	ON	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF
Light-sleep	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Deep-sleep	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Figure 4-3. Components and Power Domains Table

4.1.3.8 Brownout Detector

ESP32-C61 can periodically monitor the voltage of the power supply, and in the event of abnormal voltage, it is capable of generating interrupts or initiating resets.

Feature List

- Configurable detection threshold
- Configurable reset level
- Glitch filtering

4.1.3.9 RTC Timer

ESP32-C61 RTC Timer starts counting once the chip is powered on and keeps counting in any state.

Feature List

- 46-bit counter operating under the RTC clock
- Real-time reading of the time-base counter's value
- Configurable target value for the counter to trigger an interrupt upon timeout

4.1.3.10 Timer Group

The Timer Group (TIMG) in the ESP32-C61 chip can be used to precisely time an interval, trigger an interrupt after a particular interval (periodically and aperiodically), or act as a hardware clock. ESP32-C61 has two timer groups, each consisting of one general-purpose timer and one Main System Watchdog Timer.

Feature List

- 16-bit prescaler
- 54-bit auto-reload-capable up-down counter
- Able to read real-time value of the time-base counter
- Halt, resume, and disable the time-base counter
- Programmable alarm generation
- Timer value reload (auto-reload at an alarm or a software-controlled instant reload)
- RTC slow clock frequency calculation
- Level interrupt generation
- Real-time alarm events
- Support for several ETM tasks and events

4.1.3.11 Watchdog Timers

The Watchdog Timers (WDT) in ESP32-C61 are used to detect and recover from malfunctions. The chip contains three digital watchdog timers: one in each of the two timer groups (MWDT) and one in the RTC Module (RWDT). Additionally, there is one analog watchdog timer called the Super watchdog (SWD) that helps prevent the system from operating in a sub-optimal state.

Feature List

- Digital watchdog timers:
  - Four stages, each with a separately programmable timeout value and timeout action
  - Timeout actions: Interrupt, CPU reset, core reset, system reset (RWDT only)
  - Flash boot protection under SPI Boot mode at stage 0
  - Write protection that makes WDT register read only unless unlocked
  - 32-bit timeout counter
- Analog watchdog timer:
  - Timeout period slightly less than one second
  - Timeout actions: Interrupt, system reset

4.1.3.12 Permission Control

The Permission Control module in ESP32-C61 is responsible for managing access permissions to memory and peripheral registers. It consists of two parts: PMP (Physical Memory Protection) and APM (Access Permission Management).

Feature List

- Access permission management for ROM, HP memory, HP peripheral, and LP peripheral address spaces
- APM supports each master (such as DMA) to select one of the four security modes
- Access permission configuration for up to 16 address ranges
- Interrupt function and exception information record

4.1.3.13 System Registers

The System Registers in the ESP32-C61 chip are used to configure various auxiliary chip features.

Feature List

- Control External memory encryption and decryption
- Control CPU core debugging
- Control Bus timeout protection

4.1.3.14 Debug Assistant

The Debug Assistant provides a set of functions to help locate bugs and issues during software debugging. It offers various monitoring capabilities and logging features to assist in identifying and resolving software errors efficiently.

Feature List

- Read/write monitoring: Monitor whether the CPU bus reads from or writes to a specified memory address space
- Stack pointer (SP) monitoring: Prevent stack overflow or erroneous push/pop operations violation will trigger an interrupt.
- Program counter (PC) logging: Record PC value. The developer can get the last PC value at the most recent CPU reset
- Bus access logging: Record information about bus access when the CPU or DMA writes a specified value

4.1.4 Cryptography and Security Component

This subsection describes the security features incorporated into the chip, which safeguard data and operations.

4.1.4.1 ECC Accelerator

The ECC Accelerator accelerates calculations based on the Elliptic Curve Cryptography (ECC) algorithm and ECC-derived algorithms like ECDSA, which offers the advantages of smaller public keys compared to RSA cryptography with equivalent security.

Feature List

- Supports two different elliptic curves (P-192 and P-256)
- 11 working modes that supports Base Point Verification, Base Point Multiplication, Jacobian Point Verification, and Jacobian Point Multiplication
- Secure operating mode for Base Point Multiplication in a fixed amount of time

4.1.4.2 Elliptic Curve Digital Signature Algorithm (ECDSA)

In cryptography, the Elliptic Curve Digital Signature Algorithm (ECDSA) offers a variant of the Digital Signature Algorithm (DSA) which uses elliptic-curve cryptography.

ESP32-C61's ECDSA accelerator provides a secure and efficient environment for computing ECDSA signatures. It offers fast computations while ensuring the confidentiality of the signing process to prevent information leakage. This makes it a valuable tool for applications that require high-speed cryptographic operations with strong security guarantees. By using the ECDSA accelerator, users can be confident that their data is being protected without sacrificing performance.

Feature List

- Digital signature generation and verification
- Two elliptic curves, namely P-192 and P-256 defined in FIPS 186-3
- Two hash algorithms for message hash in the ECDSA operation, namely SHA-224 and SHA-256 defined in FIPS PUB 180-4
- High security features:
  - Dynamic access permission in different operation statuses to ensure information security, preventing key leakage due to intermediate data leakage
  - Fixed-duration signing and verification processes to resist side-channel attacks

4.1.4.3 SHA Accelerator

ESP32-C61 integrates an SHA accelerator, which is a hardware device that speeds up the SHA algorithm significantly, compared to SHA algorithms implemented solely in software. The SHA accelerator has two working modes, Typical SHA and DMA-SHA.

Feature List

- Support for multiple SHA algorithms: SHA-1, SHA-224, and SHA-256
- Two working modes: Typical SHA based on CPU and DMA-SHA based on DMA
- Interleaved function in Typical SHA working mode
- Interrupt function in DMA-SHA working mode

4.1.4.4 External Memory Encryption and Decryption

The ESP32-C61 integrates an External Memory Encryption and Decryption module that complies with the XTS-AES standard algorithm specified in IEEE Std 1619-2007, providing security for users' application code and data stored in the external memory (flash and PSRAM). Users can store proprietary firmware and sensitive data (e.g., credentials for gaining access to a private network) to the external flash, and securely run data-sensitive applications in PSRAM.

Feature List

- General XTS-AES algorithm, compliant with IEEE Std 1619-2007
- Software-based manual encryption
- High-speed auto decryption without software
- Encryption and decryption functions jointly enabled/disabled by registers configuration, eFuse parameters, and boot mode
- configurable counter measures against DPA attacks
- Flash and PSRAM use their own separate keys

4.1.4.5 True Random Number Generator

The ESP32-C61 contains a true random number generator, which generates 32-bit random numbers that can be used for cryptographical operations, among other things.

The true random number generator in ESP32-C61 generates true random numbers, which means random numbers generated from a physical process, rather than by means of an algorithm. No number generated within the specified range is more or less likely to appear than any other number.

Feature List

- RNG entropy source
  - Thermal noise from high-speed ADC or SAR ADC
  - An asynchronous clock mismatch

4.1.4.6 Power Glitch Detector

ESP32-C61 can monitor the voltage of the power supply in real time. When a voltage glitch occurs, the chip will reset immediately to prevent power glitch attacks.

Feature List

- Configurable threshold for power glitch (around 2.7 V by default)
- Enabled upon power-up

4.2 Peripherals

This section describes the chip's peripheral capabilities, covering connectivity interfaces and on-chip sensors that extend its functionality.

4.2.1 Connectivity Interface

This subsection describes the connectivity interfaces on the chip that enable communication and interaction with external devices and networks.

4.2.1.1 UART Controller

The UART Controller in the ESP32-C61 chip facilitates the transmission and reception of asynchronous serial data between the chip and external UART devices. It supports three UART interfaces.

Feature List

- Programmable baud rates up to 5 MBaud
- RAM shared by TX FIFOs and RX FIFOs
- Support for various lengths of data bits and stop bits
- Parity bit support
- Special character AT_CMD detection
- RS485 protocol support
- IrDA protocol support
- High-speed data communication using GDMA
- Receive timeout feature
- UART as the wake-up source
- Software and hardware flow control

Pin Assignment

The pins connected to transmit and receive signals (U0TXD and U0RXD) for **UART0** are multiplexed with GPIO10 ~ GPIO11 via IO MUX. Other signals can be routed to any GPIOs via the GPIO matrix.

4.2.1.2 SPI Controller

ESP32-C61 has the following SPI interfaces:

- **SPI0** used by ESP32-C61's cache and GDMA to access in-package or off-package flash/PSRAM
- **SPI1** used by the CPU to access in-package or off-package flash/PSRAM
- **SPI2** is a general-purpose SPI controller with access to general-purpose DMA channels

SPI0 and SPI1 are reserved for system use, and only SPI2 is available for users.

Features of SPI0 and SPI1

- Supports Single SPI, Dual SPI, Quad SPI, QPI modes
- Data transmission is in bytes

Features of SPI2

- Supports operation as a master or slave
- Support for DMA
- Supports Single SPI, Dual SPI, Quad SPI, QPI modes
- Configurable clock polarity (CPOL) and phase (CPHA)
- Configurable clock frequency
- Data transmission is in bytes
- Configurable read and write data bit order: most-significant bit (MSB) first, or least-significant bit (LSB) first
- As a master
  - Supports 2-line full-duplex communication with clock frequency up to 80 MHz
  - Supports 1-, 2-, 4-line half-duplex communication with clock frequency up to 80 MHz
  - Provides six FSPICS... pins for connection with six independent SPI slaves
  - Configurable CS setup time and hold time
- As a slave
  - Supports 2-line full-duplex communication with clock frequency up to 60 MHz
  - Supports 1-, 2-, 4-line half-duplex communication with clock frequency up to 60 MHz

Pin Assignment

For SPI0/1, the pins are multiplexed with GPIO14 ~ GPIO17 and GPIO19 ~ GPIO20 via the IO MUX.

For SPI2, the pins for data and clock signals are multiplexed with GPIO2, GPIO7, and JTAG interface via the IO MUX. The pins for chip select signals for multiplexed with GPIO8 via the IO MUX.

For more information about the pin assignment, see Section 2.3 *IO Pins*.

4.2.1.3 I2C Controller

The I2C Controller supports communication between the master and slave devices using the I2C bus.

Feature List

- Communication with multiple external devices
- Master and slave modes for I2C
- Standard mode (100 Kbit/s) and fast mode (400 Kbit/s)

- SCL clock stretching in slave mode
- Programmable digital noise filtering
- Support for 7-bit and 10-bit addressing, as well as dual address mode

Pin Assignment

For regular I2C, the pins used can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see Section 2.3 *IO Pins*.

4.2.1.4 I2S Controller

The I2S Controller in the ESP32-C61 chip provides a flexible communication interface for streaming digital data in multimedia applications, particularly digital audio applications.

Feature List

- Master mode and slave mode
- Full-duplex and half-duplex communications
- Separate TX and RX units that can work independently or simultaneously
- A variety of audio standards supported:
  - TDM Philips standard
  - TDM MSB alignment standard
  - TDM PCM standard
  - PDM standard
- PCM-to-PDM TX interface
- Configurable high-precision BCK clock, with frequency up to 40 MHz
  - Sampling frequencies can be 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 128 kHz, 192 kHz, etc.
- 8-/16-/24-/32-bit data communication
- Direct Memory Access (DMA)
- A-law and μ-law compression/decompression algorithms for improved signal-to-quantization noise ratio
- Flexible data format control

Pin Assignment

The pins for the I2S Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see Section 2.3 *IO Pins*.

4.2.1.5 USB Serial/JTAG Controller

The USB Serial/JTAG controller in the ESP32-C61 chip provides an integrated solution for communicating to the chip over a standard USB CDC-ACM serial port as well as a convenient method for JTAG debugging. It eliminates the need for external chips or JTAG adapters, saving space and reducing cost.

Feature List

- USB 2.0 full speed compliant, capable of up to 12 Mbit/s transfer speed (Note that this controller does not support the faster 480 Mbit/s high-speed transfer mode)
- CDC-ACM virtual serial port and JTAG adapter functionality
- CDC-ACM:
  - CDC-ACM adherent serial port emulation (plug-and-play on most modern OSes)
  - Host controllable chip reset and entry into download mode
- JTAG adapter functionality:
  - Fast communication with CPU debugging core using a compact representation of JTAG instructions
- Support for reprogramming of attached flash memory through the ROM startup code
- Internal PHY

Pin Assignment

The pins for the USB Serial/JTAG Controller are multiplexed with GPIO12 ~ GPIO13 via IO MUX.

For more information about the pin assignment, see Section 2.3 *IO Pins*.

4.2.1.6 LED PWM Controller

The LED PWM controller can generate independent digital waveform on six channels. The LED PWM controller supports:

Feature List

- Generating digital waveform with configurable periods and duty cycle. The resolution of duty cycle can be up to 20 bits
- Multiple clock sources, including 80 MHz PLL clock, external main crystal clock, and internal fast RC oscillator
- Operation when the CPU is in Light-sleep mode
- Gradual increase or decrease of duty cycle, which is useful for the LED RGB color-gradient generator
- Up to 16 duty cycle ranges for gamma curve generation, each can be independently configured in terms of duty cycle direction (increase or decrease), step size, the number of steps, and step frequency

Pin Assignment

The pins for the LED PWM Controller can be chosen from any GPIOs via the GPIO Matrix.

For more information about the pin assignment, see Section 2.3 *IO Pins*.

4.2.1.7 SDIO Slave Controller

The SDIO Slave controller in ESP32-C61 provides hardware support for the Secure Digital Input/Output (SDIO) device interface. It allows an SDIO host to access ESP32-C61 via an SDIO bus protocol.

Feature List

- compatible with SDIO Physical Layer Specification V2.00 and SDIO Specifications V2.00
- support SPI, 1-bit SDIO, and 4-bit SDIO transfer modes
- clock range of 0 ~ 50 MHz
- configurable sample and drive clock edge
- integrated and SDIO-accessible registers for information interaction
- support SDIO interrupts
- automatic padding data and discarding the padded data on the SDIO bus
- block size up to 512 bytes
- interrupt vector between the host and slave for bidirectional interrupt
- support DMA for data transfer
- support wake-up from sleep when connection is retained

Pin Assignment

The pins for the SDIO Slave controller are multiplexed with GPIO22 ~ GPIO23, and GPIO25 ~ GPIO28 via IO MUX.

For more information about the pin assignment, see Section 2.3 *IO Pins*.

4.2.2 Analog Signal Processing

This subsection describes components on the chip that sense and process real-world data.

4.2.2.1 SAR ADC

ESP32-C61 integrates a Successive Approximation Analog-to-Digital Converter (SAR ADC) to convert analog signals into digital representations.

Feature List

- 12-bit sampling resolution
- Analog voltage sampling from up to four pins
- Attenuation of input signals for voltage conversion
- Software-triggered one-time sampling
- Timer-triggered multi-channel scanning

- DMA continuous conversion for seamless data transfer
- Two filters with configurable filter coefficient
- Threshold monitoring which helps to trigger an interrupt
- Support for Event Task Matrix

Pin Assignment

The SAR ADC pins are multiplexed with GPIO1 and GPIO3 ~ GPIO5. These GPIOs are also multiplexed with LP_GPIO1, LP_GPIO3 ~ LP_GPIO5, and with the JTAG interface.

For more information about the pin assignment, see Section 2.3 *IO Pins*.

4.2.2.2 Temperature Sensor

The Temperature Sensor in the ESP32-C61 chip allows for real-time monitoring of temperature changes inside the chip.

Feature List

- Measurement range: –40°C ~ 125°C
- Software triggering, wherein the data can be read continuously once triggered
- Hardware automatic triggering and temperature monitoring
- Configurable temperature offset based on the environment to improve the accuracy
- Adjustable measurement range
- Two automatic monitoring wake-up modes: absolute value mode and incremental value mode
- Support for Event Task Matrix

4.2.2.3 Analog Voltage Comparator

ESP32-C61 provides a group of analog voltage comparators which contain two special pads. This peripheral can be used to compare the voltages of the two pads or compare the voltage of one pad with an internally adjustable stable voltage.

Feature List

- Internal or external reference voltage
- Supported internal reference voltage ranging from 0 to 0.7 × VDD_PST
- Support for ETM
- Interrupt triggered when the measured voltage reaches the reference voltage

Pin Assignment

The analog voltage comparator has dedicated pads, GPIO8 and GPIO9. GPIO9 is the test pad, and GPIO8 serves as the reference pad when using an external reference voltage.

For more information about the pin assignment, see Section 2.3 *IO Pins*.

4.3 Wireless Communication

This section describes the chip's wireless communication capabilities, spanning radio technology, Wi-Fi, and Bluetooth.

4.3.1 Radio

This subsection describes the fundamental radio technology embedded in the chip that facilitates wireless communication and data exchange.

4.3.1.1 2.4 GHz Receiver

The 2.4 GHz receiver demodulates the 2.4 GHz RF signal to quadrature baseband signals and converts them to the digital domain with two high-resolution, high-speed ADCs. To adapt to varying signal channel conditions, ESP32-C61 integrates RF filters, Automatic Gain Control (AGC), DC offset cancelation circuits, and baseband filters.

4.3.1.2 2.4 GHz Transmitter

The 2.4 GHz transmitter modulates the quadrature baseband signals to the 2.4 GHz RF signal, and drives the antenna with a high-powered CMOS power amplifier. The use of digital calibration further improves the linearity of the power amplifier.

Additional calibrations are integrated to cancel any radio imperfections, such as:

- Carrier leakage
- I/Q amplitude/phase matching
- Baseband nonlinearities
- RF nonlinearities
- Antenna matching

These built-in calibration routines reduce the cost, time, and specialized equipment required for product testing.

4.3.1.3 Clock Generator

The clock generator produces quadrature clock signals of 2.4 GHz for both the receiver and the transmitter. All components of the clock generator are integrated into the chip, including inductors, varactors, filters, regulators and dividers.

The clock generator has built-in calibration and self-test circuits. Quadrature clock phases and phase noise are optimized on chip with patented calibration algorithms which ensure the best performance of the receiver and the transmitter.

4.3.2 Wi-Fi

This subsection describes the chip's Wi-Fi capabilities, which facilitate wireless communication at a high data rate.

4.3.2.1 Wi-Fi Radio and Baseband

The ESP32-C61 Wi-Fi radio and baseband support the following features:

- 1T1R in 2.4 GHz band
- 802.11ax
  - 20 MHz-only non-AP mode
  - MCS0 ~MCS9
  - Uplink and downlink OFDMA
  - Downlink MU-MIMO (multi-user, multiple input, multiple output)
  - Longer OFDM symbol, with 0.8, 1.6, 3.2 μs guard interval
  - DCM (dual carrier modulation), up to 16-QAM
  - Single-user/multi-user beamformee
  - Channel quality indication (CQI)
  - RX STBC (single spatial stream)
- 802.11b/g/n
  - MCS0 ~MCS7 that supports 20 MHz and 40 MHz bandwidth
  - MCS32
  - Data rate up to 150 Mbps
  - 0.4 μs guard interval
- Adjustable transmitting power
- Antenna diversity
  ESP32-C61 supports antenna diversity with an external RF switch. This switch is controlled by one or more GPIOs, and used to select the best antenna to minimize the effects of channel imperfections.

4.3.2.2 Wi-Fi MAC

ESP32-C61 implements the full IEEE 802.11 b/g/n/ax Wi-Fi MAC protocol. ESP32-C61 supports the Basic Service Set (BSS) STA and SoftAP operations under the Enhanced Distributed Channel Access (EDCA). Power management is handled automatically with minimal host interaction to minimize the active duty period.

The ESP32-C61 Wi-Fi MAC applies the following low-level protocol functions automatically:

- Four virtual Wi-Fi interfaces
- Infrastructure BSS in Station mode, SoftAP mode, Station + SoftAP mode, and promiscuous mode
- RTS protection, CTS-to-Self protection, Immediate Block ACK
- Fragmentation and defragmentation
- TX/RX A-MPDU, TX/RX A-MSDU
- Transmit opportunity (TXOP)

- Wi-Fi multimedia (WMM)
- GCMP, CCMP, TKIP, WAPI, WEP, BIP, WPA2-PSK, and WPA3-PSK
- Automatic beacon monitoring (hardware TSF)
- 802.11mc FTM
- 802.11ax supports:
  - Target wake time (TWT) requester
  - Multiple BSSIDs
  - Triggered response scheduling
  - Multi-user Request-to-Send (MU-RTS), Multi-user Block ACK Request (MU-BAR), and Multi-STA Block ACK (M-BA) frame
  - Intra-PPDU power saving mechanism
  - Two network allocation vectors (NAV)
  - BSS coloring
  - Spatial reuse
  - Uplink power headroom
  - Operating mode control
  - Buffer status report
  - TXOP duration RTS threshold
  - UL-OFDMA random access (UORA)

4.3.2.3 Networking Features

Espressif provides libraries for TCP/IP networking, ESP-WIFI-MESH networking, and other networking protocols over Wi-Fi. TLS 1.0, 1.1, and 1.2 is also supported.

4.3.3 Bluetooth LE

This subsection describes the chip's Bluetooth capabilities, which facilitate wireless communication for low-power, short-range applications.

4.3.3.1 Bluetooth LE PHY

Bluetooth Low Energy PHY in ESP32-C61 supports:

- 1 Mbps PHY
- 2 Mbps PHY for higher data rates
- coded PHY for longer range (125 Kbps and 500 Kbps)
- HW listen before talk (LBT)

4.3.3.2 Bluetooth LE Link Controller

Bluetooth Low Energy Link Controller and Host in ESP32-C61 support:

- direction finding (AoA/AoD)
- periodic advertising with responses (PAwR)
- LE connection subrating (LE enhanced connection update)
- LE advertising extensions and multiple advertising sets
- allow devices to operate in Broadcaster, Observer, Central, and Peripheral roles concurrently
- adaptive frequency hopping and channel assessment
- LE channel selection algorithm #2
- LE power control
- advertising coding selection
- encrypted advertising data
- LE GATT security levels characteristic
- AdvDataInfo in periodic advertising
- LE channel classification
- enhanced attribute protocol
- advertising channel index
- GATT caching
- periodic advertising sync transfer
- high duty cycle non-connectable advertising
- LE data packet length extension
- LE secure connections
- LE privacy 1.2
- link layer extended scanner filter policies
- low duty cycle directed advertising
- link layer encryption
- LE ping

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses above those listed in Table 5-1 *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and normal operation of the device at these or any other conditions beyond those indicated in Section 5.2 *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 5-1. Absolute Maximum Ratings

Parameter	Description	Min	Max	Unit
Input power pins[1]	Allowed input voltage	–0.3	3.6	V
I_{output}[2]	Cumulative IO output current	—	1500	mA
T_{STORE}	Storage temperature	–40	150	°C

[1] For more information on input power pins, see Section 2.5.1 *Power Pins*.

[2] The product proved to be fully functional after all its IO pins were pulled high while being connected to ground for 24 consecutive hours at ambient temperature of 25 °C.

5.2 Recommended Operating Conditions

Table 5-2. Recommended Operating Conditions

Parameter [1]	Description	Min	Typ	Max	Unit
VDDA1, VDDA2, VDDA3P3	Recommended input voltage	3.0	3.3	3.6	V
VDDPST1	Recommended input voltage	3.0	3.3	3.6	V
VDD_SPI (as input)	—	1.8	3.3	3.6	V
VDDPST2 [2,3]	Recommended input voltage	3.0	3.3	3.6	V
I_{VDD}	Cumulative input current	0.5	—	—	A

[1] See in conjunction with Section 2.5 *Power Supply*.

[2] If VDDPST2 is used to power VDD_SPI (see Section 2.5.2 *Power Scheme*), the voltage drop on R_{SPI} should be accounted for.

[3] If writing to eFuses, the voltage on VDDPST2 should not exceed 3.3 V as the circuits responsible for burning eFuses are sensitive to higher voltages.

5.3 VDD_SPI Output Characteristics

Table 5-3. VDD_SPI Internal and Output Characteristics

Parameter	Description [1]	Typ	Unit
R_{SPI}	VDD_SPI powered by VDD3P3_RTC via R_{SPI} for 3.3 V flash/PSRAM [2]	3	Ω

[1] See in conjunction with Section 2.5.2 *Power Scheme*.

[2] VDD3P3_RTC must be more than *VDD_flash_min* + *I_flash_max* × R_{SPI}; where

- *VDD_flash_min* – minimum operating voltage of flash/PSRAM
- *I_flash_max* – maximum operating current of flash/PSRAM

5.4 ADC Characteristics

The measurements in this section are taken with an external 100 nF capacitor connected to the ADC, using DC signals as input, and at an ambient temperature of 25 °C with disabled Wi-Fi.

Table 5-4. ADC Characteristics

Symbol	Min	Max	Unit
DNL (Differential nonlinearity) [1]	–5	5	LSB
INL (Integral nonlinearity)	–5	5	LSB
Sampling rate	—	2000	kSPS [2]

[1] To get better DNL results, you can sample multiple times and apply a filter, or calculate the average value.

[2] kSPS means kilo samples-per-second.

The calibrated ADC results after hardware calibration and software calibration are shown in Table 5-5. For higher accuracy, you may implement your own calibration methods.

Table 5-5. ADC Calibration Results

Parameter	Description	Min	Max	Unit
Total error	ATTEN0, effective measurement range of 0 ~ 1000	–10	10	mV
	ATTEN1, effective measurement range of 0 ~ 1300	–10	10	mV
	ATTEN2, effective measurement range of 0 ~ 1900	–12	12	mV
	ATTEN3, effective measurement range of 0 ~ 3300	–15	15	mV

5.5 Current Consumption Characteristics

5.5.1 Current Consumption in Active Mode

The current consumption measurements are taken with a 3.3 V supply at 25 °C ambient temperature.

TX current consumption is rated at a 100% duty cycle.

RX current consumption is rated when the peripherals are disabled and the CPU idle.

Table 5-6. Current Consumption for Wi-Fi (2.4 GHz) in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, DSSS @21 dBm	360
		802.11g, 54 Mbps, OFDM @19 dBm	310
		802.11n, HT20, MCS7 @18 dBm	285
		802.11n, HT40, MCS7 @17.5 dBm	267
		802.11ax, MCS9 @15 dBm	240
	RX	802.11b/g/n, HT20	88
		802.11n, HT40	90
		802.11ax, HE20	88

Table 5-7. Current Consumption for Bluetooth LE in Active Mode

Work Mode	RF Condition	Description	Peak (mA)
Active (RF working)	TX	Bluetooth LE @ 18 dBm	283
		Bluetooth LE @ 9 dBm	160
		Bluetooth LE @ 0 dBm	128
		Bluetooth LE @ –15 dBm	96
	RX	Bluetooth LE	81

5.5.2 Current Consumption in Other Modes

Table 5-8. Current Consumption in Modem-sleep Mode

Mode	CPU Frequency (MHz)	Description	Typ (mA)	
			All Peripherals Clocks Disabled	All Peripherals Clocks Enabled[1]
Modem-sleep[2,3]	160	WAITI	11	18
		CPU while loop	16	23
		Run CoreMark	21	28
	80	WAITI	10	16
		CPU while loop	12	19
		Run CoreMark	15	21
	40	WAITI	6	11
		CPU while loop	7	12
		Run CoreMark	9	13

[1] In practice, the current consumption might be different depending on which peripherals are enabled.

[2] In Modem-sleep mode, Wi-Fi is clock gated.

[3] In Modem-sleep mode, the consumption might be higher when accessing flash.

Table 5-9. Current Consumption in Low-Power Modes

Mode	Description	Typ (mA)
Light-sleep	CPU and wireless communication modules are powered down, peripheral clocks are disabled, and all GPIOs are high-impedance	0.2
	CPU, wireless communication modules and peripherals are powered down, and all GPIOs are high-impedance	0.05
Deep-sleep	LP timer and LP memory are powered on	0.01
Power off	CHIP_PU is set to low level, the chip is powered off	0.001

5.6 Memory Specifications

The data below is sourced from the memory vendor datasheet. These values are guaranteed through design and/or characterization but are not fully tested in production. Devices are shipped with the memory erased.

Table 5-10. Flash Specifications

Parameter	Description	Min	Typ	Max	Unit
VCC	Power supply voltage (1.8 V)	1.65	1.80	2.00	V
	Power supply voltage (3.3 V)	2.7	3.3	3.6	V
F_C	Maximum clock frequency	80	—	—	MHz
—	Program/erase cycles	100,000	—	—	cycles
T_{RET}	Data retention time	20	—	—	years
T_{PP}	Page program time	—	0.8	5	ms
T_{SE}	Sector erase time (4 KB)	—	70	500	ms
T_{BE1}	Block erase time (32 KB)	—	0.2	2	s
T_{BE2}	Block erase time (64 KB)	—	0.3	3	s
T_{CE}	Chip erase time (16 Mb)	—	7	20	s
	Chip erase time (32 Mb)	—	20	60	s
	Chip erase time (64 Mb)	—	25	100	s
	Chip erase time (128 Mb)	—	60	200	s
	Chip erase time (256 Mb)	—	70	300	s

Table 5-11. PSRAM Specifications

Parameter	Description	Min	Typ	Max	Unit
VCC	Power supply voltage (1.8 V)	1.62	1.80	1.98	V
	Power supply voltage (3.3 V)	2.7	3.3	3.6	V
F_C	Maximum clock frequency	80	—	—	MHz

5.7 Reliability

Table 5-12. Reliability Qualifications

Test Item	Test Conditions	Test Standard
HTOL (High Temperature Operating Life)	125 °C, 1000 hours	JESD22-A108
ESD (Electro-Static Discharge Sensitivity)	HBM (Human Body Mode)[1] ± 2000 V	JS-001
	CDM (Charge Device Mode)[2] ± 1000 V	JS-002
Latch up	Current trigger ± 200 mA	JESD78
	Voltage trigger 1.5 × VDD_{max}	
Preconditioning	Bake 24 hours @125 °C Moisture soak (level 3: 192 hours @30 °C, 60% RH) IR reflow solder: 260 + 0 °C, 20 seconds, three times	J-STD-020, JESD47, JESD22-A113
TCT (Temperature Cycling Test)	–65 °C / 150 °C, 500 cycles	JESD22-A104
uHAST (Highly Accelerated Stress Test, unbiased)	130 °C, 85% RH, 96 hours	JESD22-A118
HTSL (High Temperature Storage Life)	150 °C, 1000 hours	JESD22-A103
LTSL (Low Temperature Storage Life)	–40 °C, 1000 hours	JESD22-A119

[1] JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

[2] JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6 RF Characteristics

This section contains tables with RF characteristics of the Espressif product.

The RF data is measured at the antenna port, where RF cable is connected, including the front-end loss. The front-end circuit is a 0 Ω resistor.

Devices should operate in the center frequency range allocated by regional regulatory authorities. The target center frequency range and the target transmit power are configurable by software. See ESP RF Test Tool and Test Guide for instructions.

Unless otherwise stated, the RF tests are conducted with a 3.3 V (±5%) supply at 25 °C ambient temperature.

6.1 Wi-Fi Radio (2.4 GHz)

Table 6-1. Wi-Fi RF Characteristics

Name	Description
Center frequency range of operating channel	2412 ~ 2484 MHz
Wi-Fi wireless standard	IEEE 802.11b/g/n/ax

6.1.1 Wi-Fi RF Transmitter (TX) Characteristics

Table 6-2. TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	21.0	—
802.11b, 11 Mbps, CCK	—	21.0	—
802.11g, 6 Mbps, OFDM	—	20.0	—
802.11g, 54 Mbps, OFDM	—	19.0	—
802.11n, HT20, MCS0	—	19.0	—
802.11n, HT20, MCS7	—	18.0	—
802.11n, HT40, MCS0	—	18.5	—
802.11n, HT40, MCS7	—	17.5	—
802.11ax, HE20, MCS0	—	19.0	—
802.11ax, HE20, MCS9	—	15.0	—

Table 6-3. TX EVM Test[1]

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11b, 1 Mbps, DSSS	—	–24.8	–10.0
802.11b, 11 Mbps, CCK	—	–24.8	–10.0

Cont'd on next page

Table 6-3 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Limit (dB)
802.11g, 6 Mbps, OFDM	—	–26.0	–5.0
802.11g, 54 Mbps, OFDM	—	–29.0	–25.0
802.11n, HT20, MCS0	—	–24.5	–5.0
802.11n, HT20, MCS7	—	–31.5	–27.0
802.11n, HT40, MCS0	—	–26.8	–5.0
802.11n, HT40, MCS7	—	–30.5	–27.0
802.11ax, HE20, MCS0	—	–26.0	–5.0
802.11ax, HE20, MCS9	—	–34.0	–32.0

[1] EVM is measured at the corresponding typical TX power provided in Table 6-2 *Wi-Fi RF Transmitter (TX) Characteristics* above.

6.1.2 Wi-Fi RF Receiver (RX) Characteristics

For RX tests, the PER (packet error rate) limit is 8% for 802.11b, and 10% for 802.11g/n/ax.

Table 6-4. RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	–99.5	—
802.11b, 2 Mbps, DSSS	—	–96.5	—
802.11b, 5.5 Mbps, CCK	—	–94.0	—
802.11b, 11 Mbps, CCK	—	–90.0	—
802.11g, 6 Mbps, OFDM	—	–94.0	—
802.11g, 9 Mbps, OFDM	—	–93.0	—
802.11g, 12 Mbps, OFDM	—	–92.0	—
802.11g, 18 Mbps, OFDM	—	–90.0	—
802.11g, 24 Mbps, OFDM	—	–87.0	—
802.11g, 36 Mbps, OFDM	—	–83.5	—
802.11g, 48 Mbps, OFDM	—	–79.0	—
802.11g, 54 Mbps, OFDM	—	–77.5	—
802.11n, HT20, MCS0	—	–94.0	—
802.11n, HT20, MCS1	—	–92.5	—
802.11n, HT20, MCS2	—	–89.5	—
802.11n, HT20, MCS3	—	–86.5	—
802.11n, HT20, MCS4	—	–83.0	—
802.11n, HT20, MCS5	—	–79.0	—
802.11n, HT20, MCS6	—	–77.0	—
802.11n, HT20, MCS7	—	–75.5	—
802.11n, HT40, MCS0	—	–91.0	—
802.11n, HT40, MCS1	—	–90.0	—

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Table 6-4 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11n, HT40, MCS2	—	–87.0	—
802.11n, HT40, MCS3	—	–83.5	—
802.11n, HT40, MCS4	—	–80.5	—
802.11n, HT40, MCS5	—	–76.0	—
802.11n, HT40, MCS6	—	–74.5	—
802.11n, HT40, MCS7	—	–73.5	—
802.11ax, HE20, MCS0	—	–94.0	—
802.11ax, HE20, MCS1	—	–91.0	—
802.11ax, HE20, MCS2	—	–88.0	—
802.11ax, HE20, MCS3	—	–85.5	—
802.11ax, HE20, MCS4	—	–82.0	—
802.11ax, HE20, MCS5	—	–78.0	—
802.11ax, HE20, MCS6	—	–76.5	—
802.11ax, HE20, MCS7	—	–74.5	—
802.11ax, HE20, MCS8	—	–71.0	—
802.11ax, HE20, MCS9	—	–68.0	—

Table 6-5. Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps, DSSS	—	5	—
802.11b, 11 Mbps, CCK	—	5	—
802.11g, 6 Mbps, OFDM	—	5	—
802.11g, 54 Mbps, OFDM	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	0	—
802.11n, HT40, MCS0	—	5	—
802.11n, HT40, MCS7	—	0	—
802.11ax, HE20, MCS0	—	5	—
802.11ax, HE20, MCS9	—	0	—

Table 6-6. RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps, DSSS	—	38	—
802.11b, 11 Mbps, CCK	—	38	—
802.11g, 6 Mbps, OFDM	—	33	—
802.11g, 54 Mbps, OFDM	—	16	—

Cont'd on next page

Table 6-6 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11n, HT20, MCS0	—	32	—
802.11n, HT20, MCS7	—	17	—
802.11n, HT40, MCS0	—	24	—
802.11n, HT40, MCS7	—	13	—
802.11ax, HE20, MCS0	—	37	—
802.11ax, HE20, MCS9	—	13	—

6.2 Bluetooth 5 (LE) Radio

Table 6-7. Bluetooth LE RF Characteristics

Name	Description
Center frequency range of operating channel	2402 ~ 2480 MHz
RF transmit power range	–15 ~ 20 dBm

6.2.1 Bluetooth LE RF Transmitter (TX) Characteristics

Table 6-8. Bluetooth LE - Transmitter Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	10.85	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\,3,\,4,\,\ldots k}$	—	3.5	—	kHz
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\,7,\,8,\,\ldots k}$	—	2.4	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	2.7	—	kHz
Modulation characteristics	$\Delta\, F1_{\text{avg}}$	—	250.0	—	kHz
	Min. $\Delta\, F2_{\text{max}}$ (for at least 99.9% of all $\Delta\, F2_{\text{max}}$)	—	243.0	—	kHz
	$\Delta\, F2_{\text{avg}} / \Delta\, F1_{\text{avg}}$	—	0.88	—	—
In-band emissions	± 2 MHz offset	—	–27	—	dBm
	± 3 MHz offset	—	–36	—	dBm
	> ± 3 MHz offset	—	–42	—	dBm

Table 6-9. Bluetooth LE - Transmitter Characteristics - 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	9.4	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=2,\,3,\,4,\,\ldots k}$	—	3.7	—	kHz
	Max. $\lvert f_n - f_{n-5} \rvert_{n=6,\,7,\,8,\,\ldots k}$	—	1.1	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	3.3	—	kHz
Modulation characteristics	$\Delta\, F1_{\text{avg}}$	—	499.4	—	kHz

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Table 6-9 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	Min. $\Delta F2_{max}$ (for at least 99.9% of all $\Delta F2_{max}$)	—	532.0	—	kHz
	$\Delta F2_{avg}/\Delta F1_{avg}$	—	0.95	—	—
In-band emissions	± 4 MHz offset	—	–41	—	dBm
	± 5 MHz offset	—	–44	—	dBm
	> ± 5 MHz offset	—	–45	—	dBm

Table 6-10. Bluetooth LE - Transmitter Characteristics - 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	10.1	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=1,\,2,\,3,\,\ldots k}$	—	2.1	—	kHz
	$\lvert f_0 - f_3 \rvert$	—	1.2	—	kHz
	Max. $\lvert f_n - f_{n-3} \rvert_{n=7,\,8,\,9,\,\ldots k}$	—	0.7	—	kHz
Modulation characteristics	$\Delta F1_{avg}$	—	253.1	—	kHz
	Min. $\Delta F1_{max}$ (for at least 99.9% of all $\Delta F1_{max}$)	—	270.5	—	kHz
In-band emissions	± 2 MHz offset	—	–27	—	dBm
	± 3 MHz offset	—	–38	—	dBm
	> ± 3 MHz offset	—	–43	—	dBm

Table 6-11. Bluetooth LE - Transmitter Characteristics - 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max. $\lvert f_n \rvert_{n=0,\,1,\,2,\,3,\,\ldots k}$	—	10.2	—	kHz
	Max. $\lvert f_0 - f_n \rvert_{n=1,\,2,\,3,\,\ldots k}$	—	1.2	—	kHz
	$\lvert f_0 - f_3 \rvert$	—	0.6	—	kHz
	Max. $\lvert f_n - f_{n-3} \rvert_{n=7,\,8,\,9,\,\ldots k}$	—	1.8	—	kHz
Modulation characteristics	$\Delta F2_{avg}$	—	223.4	—	kHz
	Min. $\Delta F2_{max}$ (for at least 99.9% of all $\Delta F2_{max}$)	—	243.5	—	kHz
In-band emissions	± 2 MHz offset	—	–27	—	dBm
	± 3 MHz offset	—	–37	—	dBm
	> ± 3 MHz offset	—	43	—	dBm

6.2.2 Bluetooth LE RF Receiver (RX) Characteristics

Table 6-12. Bluetooth LE - Receiver Characteristics - 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–98.0	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm

Cont'd on next page

Table 6-12 – cont'd from previous page

Parameter		Description	Min	Typ	Max	Unit
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	7	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	–2	—	dB
		F = F0 – 1 MHz	—	–3	—	dB
		F = F0 + 2 MHz	—	–34	—	dB
		F = F0 – 2 MHz	—	–27	—	dB
		F = F0 + 3 MHz	—	–33	—	dB
		F = F0 – 3 MHz	—	–40	—	dB
		F $\geq$ F0 + 4 MHz	—	–27	—	dB
		F $\leq$ F0 – 4 MHz	—	–53	—	dB
	Image frequency	—	—	–35	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–34	—	dB
		F = F_{image} – 1 MHz	—	–33	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–20	—	dBm
		2003 MHz ~ 2399 MHz	—	–25	—	dBm
		2484 MHz ~ 2997 MHz	—	–25	—	dBm
		3000 MHz ~ 12.75 GHz	—	–10	—	dBm
Intermodulation		—	—	–32	—	dBm

Table 6-13. Bluetooth LE - Receiver Characteristics - 2 Mbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–94.0	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	9	—	dB
	Adjacent channel	F = F0 + 2 MHz	—	–7	—	dB
		F = F0 – 2 MHz	—	–6	—	dB
		F = F0 + 4 MHz	—	–21	—	dB
		F = F0 – 4 MHz	—	–27	—	dB
		F = F0 + 6 MHz	—	–38	—	dB
		F = F0 – 6 MHz	—	–41	—	dB
		F $\geq$ F0 + 8 MHz	—	–46	—	dB
		F $\leq$ F0 – 8 MHz	—	–46	—	dB
	Image frequency	—	—	–21	—	dB
	Adjacent channel to image frequency	F = F_{image} + 2 MHz	—	–38	—	dB
		F = F_{image} – 2 MHz	—	–7	—	dB
Out-of-band blocking performance		30 MHz ~ 2000 MHz	—	–25	—	dBm
		2003 MHz ~ 2399 MHz	—	–25	—	dBm
		2484 MHz ~ 2997 MHz	—	–25	—	dBm
		3000 MHz ~ 12.75 GHz	—	–10	—	dBm
Intermodulation		—	—	–31	—	dBm

Table 6-14. Bluetooth LE - Receiver Characteristics - 125 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–106.0	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	4	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	–2	—	dB
		F = F0 – 1 MHz	—	–3	—	dB
		F = F0 + 2 MHz	—	–33	—	dB
		F = F0 – 2 MHz	—	–36	—	dB
		F = F0 + 3 MHz	—	–35	—	dB
		F = F0 – 3 MHz	—	–50	—	dB
		F ≥ F0 + 4 MHz	—	–31	—	dB
		F ≤ F0 – 4 MHz	—	–50	—	dB
	Image frequency	—	—	–31	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–36	—	dB
		F = F_{image} – 1 MHz	—	–35	—	dB

Table 6-15. Bluetooth LE - Receiver Characteristics - 500 Kbps

Parameter		Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER		—	—	–102.0	—	dBm
Maximum received signal @30.8% PER		—	—	8	—	dBm
C/I and receiver selectivity performance	Co-channel	F = F0 MHz	—	4	—	dB
	Adjacent channel	F = F0 + 1 MHz	—	–4	—	dB
		F = F0 – 1 MHz	—	–3	—	dB
		F = F0 + 2 MHz	—	–32	—	dB
		F = F0 – 2 MHz	—	–36	—	dB
		F = F0 + 3 MHz	—	–35	—	dB
		F = F0 – 3 MHz	—	–50	—	dB
		F ≥ F0 + 4 MHz	—	–29	—	dB
		F ≤ F0 – 4 MHz	—	–50	—	dB
	Image frequency	—	—	–29	—	dB
	Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–36	—	dB
		F = F_{image} – 1 MHz	—	–35	—	dB

7 Packaging

- For information about tape, reel, and chip marking, please refer to *ESP32-C61 Chip Packaging Information*.
- The pins of the chip are numbered in anti-clockwise order starting from Pin 1 in the top view. For pin numbers and pin names, see also Figure *2-1 ESP32-C61HR2 & ESP32-C61HR8 & ESP32-C61HF4 Pin Layout (Top View)* and *2-2 ESP32-C61NF8R8LA Pin Layout (Top View)*.
- The recommended land pattern source file (asc) is available for download. You can import the file with software such as PADS and Altium Designer.

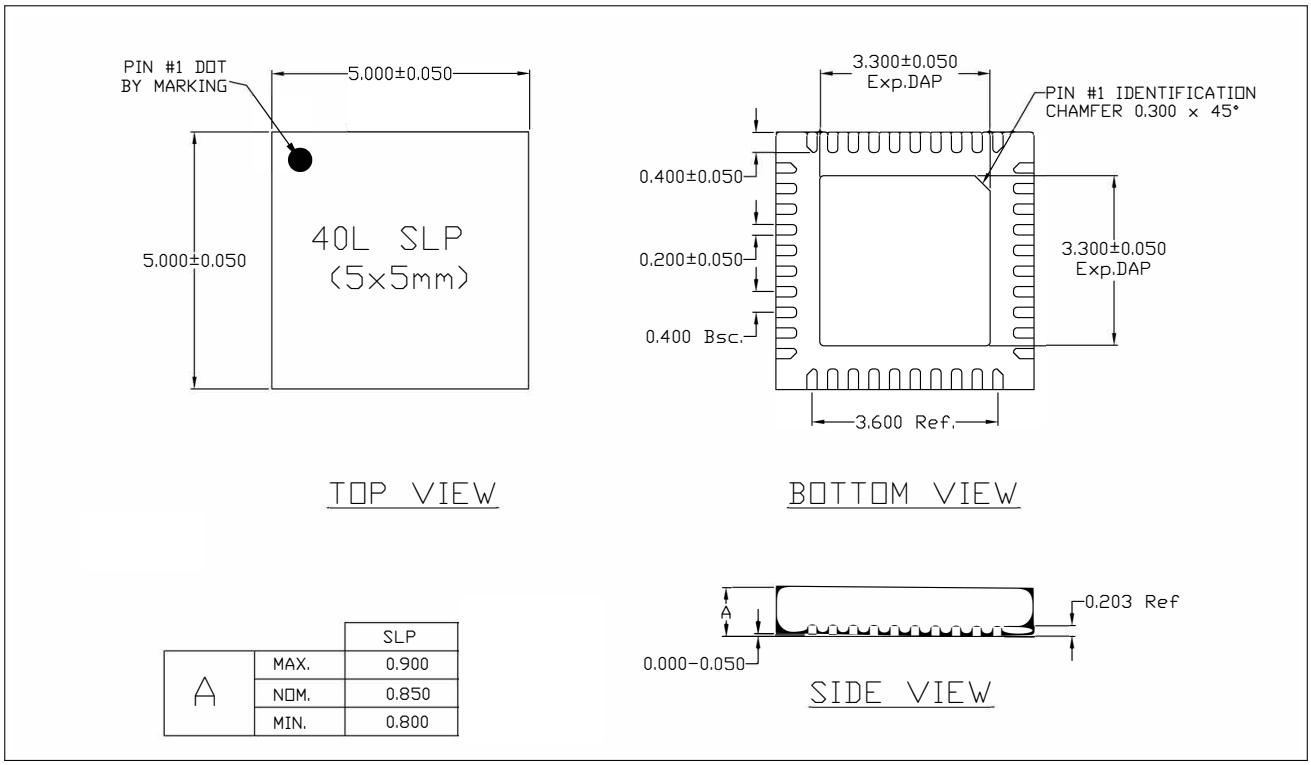
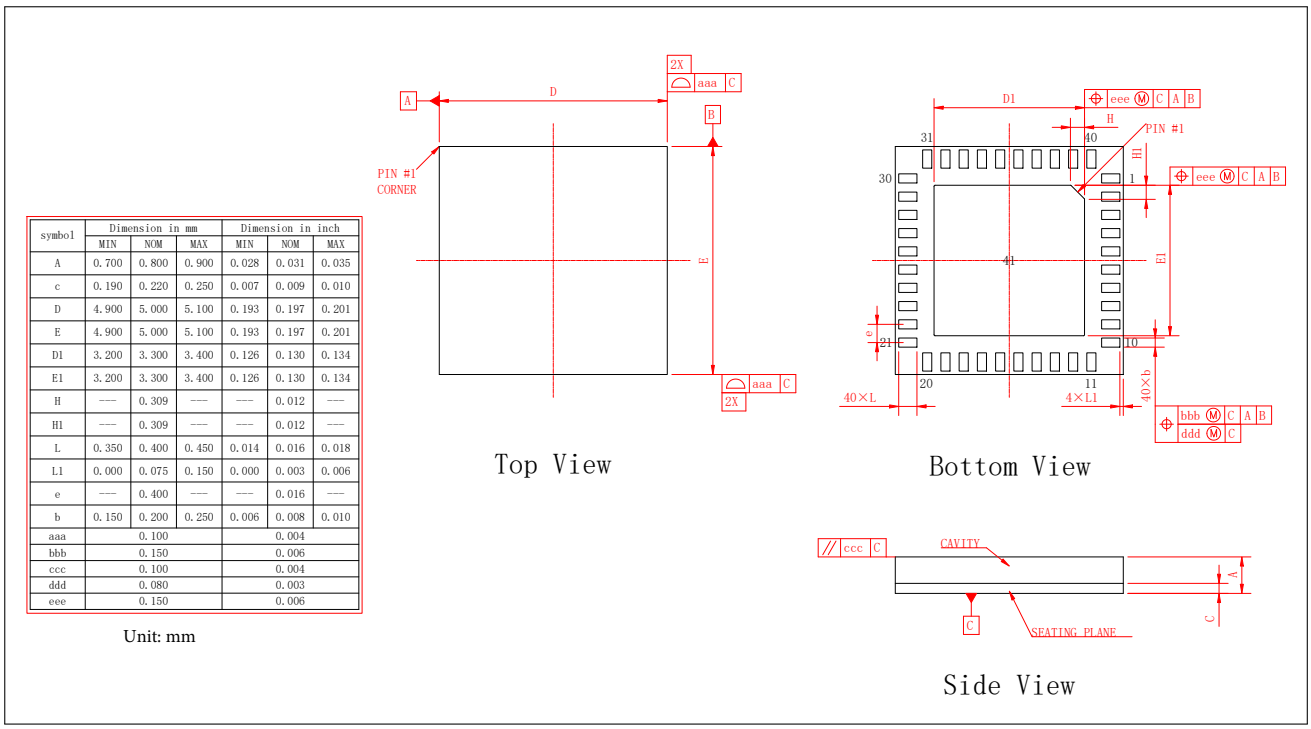


Figure 7-1. QFN40 (5×5 mm) Package



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.800	0.900	0.028	0.031	0.035
c	0.190	0.220	0.250	0.007	0.009	0.010
D	4.900	5.000	5.100	0.193	0.197	0.201
E	4.900	5.000	5.100	0.193	0.197	0.201
D1	3.200	3.300	3.400	0.126	0.130	0.134
E1	3.200	3.300	3.400	0.126	0.130	0.134
H	---	0.309	---	---	0.012	---
H1	---	0.309	---	---	0.012	---
L	0.350	0.400	0.450	0.014	0.016	0.018
L1	0.000	0.075	0.150	0.000	0.003	0.006
e	---	0.400	---	---	0.016	---
b	0.150	0.200	0.250	0.006	0.008	0.010
aaa	0.100			0.004		
bbb	0.150			0.006		
ccc	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		

Figure 7-2. LGA40 (5×5 mm) Package

Related Documentation and Resources

Related Documentation

- ESP32-C61 Technical Reference Manual – Detailed information on how to use the ESP32-C61 memory and peripherals.
- ESP32-C61 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-C61 into your hardware product.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-C61 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-C61
- *ESP32-C61 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-C61
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-C61 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *ESP-FAQ* – A summary document of frequently asked questions released by Espressif.
  https://espressif.com/projects/esp-faq/en/latest/index.html
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-C61 Series SoCs* – Browse through all ESP32-C61 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-C61
- *ESP32-C61 Series Modules* – Browse through all ESP32-C61-based modules.
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  https://espressif.com/en/products/devkits?id=ESP32-C61
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Appendix A – ESP32-C61 Consolidated Pin Overview

Table 7-1. Pin Overview

Pin No.	Pin Name	Pin Type	Pin Providing Power	Pin Settings		IO MUX Function						LP IO MUX Functio
				At Reset	After Reset	F0	Type	F1	Type	F2	Type	F0
1	ANT_2G	Analog	-	–	–	–	–	–	–	–	–	–
2	VDDA3	Power	–	–	–	–	–	–	–	–	–	–
3	VDDA4	Power	–	–	–	–	–	–	–	–	–	–
4	CHIP_PU	I	VDDPST1	–	–	–	–	–	–	–	–	–
5	VDDPST1	Power	–	–	–	–	–	–	–	–	–	–
6	XTAL_32K_P	I/O/T	VDDPST1	–	–	GPIO0	I/O/T	**GPIO0**	I/O/T	–	–	LP_GPIO0
7	XTAL_32K_N	I/O/T	VDDPST1	–	–	GPIO1	I/O/T	**GPIO1**	I/O/T	–	–	LP_GPIO1
8	GPIO2	I/O/T	VDDPST1	–	–	GPIO2	I/O/T	**GPIO2**	I/O/T	FSPIQ	I1/O/T	LP_GPIO2
9	MTMS	I/O/T	VDDPST1	IE	IE	**MTMS**	I1	GPIO3	I/O/T	FSPIHD	I1/O/T	LP_GPIO3
10	MTDI	I/O/T	VDDPST1	IE	IE	**MTDI**	I1	GPIO4	I/O/T	FSPIWP	I1/O/T	LP_GPIO4
11	MTCK	I/O/T	VDDPST1	–	IE*	**MTCK**	I1	GPIO5	I/O/T	–	–	LP_GPIO5
12	MTDO	I/O/T	VDDPST1	–	IE	**MTDO**	O/T	GPIO6	I/O/T	FSPICLK	I1/O/T	LP_GPIO6
13	SDIO_CMD	I/O/T	VDDPST2	–	IE	SDIO_CMD	I1/O/T	**GPIO25**	I/O/T	–	–	–
14	SDIO_CLK	I/O/T	VDDPST2	–	IE	SDIO_CLK	I1	**GPIO26**	I/O/T	–	–	–
15	SDIO_DATA0	I/O/T	VDDPST2	–	IE	SDIO_DATA0	I1/O/T	**GPIO27**	I/O/T	–	–	–
16	SDIO_DATA1	I/O/T	VDDPST2	–	IE	SDIO_DATA1	I1/O/T	**GPIO28**	I/O/T	–	–	–
17	SDIO_DATA2	I/O/T	VDDPST2	–	IE	SDIO_DATA2	I1/O/T	**GPIO22**	I/O/T	–	–	–
18	SDIO_DATA3	I/O/T	VDDPST2	–	IE	SDIO_DATA3	I1/O/T	**GPIO23**	I/O/T	–	–	–
19	SPICS1/NC	I/O/T	VDD_SPI/VDDPST2	–	–	**SPICS1**	O/T	GPIO14	I/O/T	–	–	–
20	SPICS0/NC	I/O/T	VDD_SPI/VDDPST2	–	–	**SPICS0**	O/T	GPIO15	I/O/T	–	–	–
21	VDDPST2	Power	–	–	–	–	–	–	–	–	–	–
22	SPIQ/NC	I/O/T	VDD_SPI/VDDPST2	–	–	**SPIQ**	I1/O/T	GPIO16	I/O/T	–	–	–
23	SPIWP/NC	I/O/T	VDD_SPI/VDDPST2	–	–	SPIWP	I1/O/T	**GPIO17**	I/O/T	–	–	–
24	VDD_SPI/NC	Power	VDDPST2	–	–	GPIO18	I/O/T	GPIO18	I/O/T	–	–	–
25	SPIHD/NC	I/O/T	VDD_SPI/VDDPST2	–	–	SPIHD	I1/O/T	**GPIO19**	I/O/T	–	–	–
26	SPICLK/NC	O	VDD_SPI/VDDPST2	–	–	**SPICLK**	O/T	GPIO20	I/O/T	–	–	–
27	SPID/NC	I/O/T	VDD_SPI/VDDPST2	–	–	**SPID**	I1/O/T	GPIO21	I/O/T	–	–	–
28	USB_D-	I/O/T	VDDPST2	–	IE	GPIO12	I/O/T	GPIO12	I/O/T	–	–	–
29	USB_D+	I/O/T	VDDPST2	–	IE,WPU*	GPIO13	I/O/T	GPIO13	I/O/T	–	–	–
30	GPIO24	I/O/T	VDDPST2	–	–	GPIO24	I/O/T	**GPIO24**	I/O/T	–	–	–
31	GPIO8	I/O/T	VDDPST2	IE	IE	GPIO8	I/O/T	**GPIO8**	I/O/T	FSPICS0	I1/O/T	–
32	GPIO9	I/O/T	VDDPST2	IE,WPU	IE,WPU	GPIO9	I/O/T	**GPIO9**	I/O/T	–	–	–
33	U0RXD	I/O/T	VDDPST2	–	IE,WPU	**U0RXD**	I1	GPIO10	I/O/T	–	–	–
34	U0TXD	I/O/T	VDDPST2	–	IE,WPU	**U0TXD**	O	GPIO11	I/O/T	–	–	–
35	GPIO29	I/O/T	VDDPST2	–	–	GPIO29	I/O/T	**GPIO29**	I/O/T	–	–	–
36	GPIO7	I/O/T	VDDPST2	IE	IE	GPIO7	I/O/T	**GPIO7**	I/O/T	FSPID	I1/O/T	–
37	VDDA1	Power	–	–	–	–	–	–	–	–	–	–
38	XTAL_N	Analog	-	–	–	–	–	–	–	–	–	–
39	XTAL_P	Analog	-	–	–	–	–	–	–	–	–	–
40	VDDA2	Power	–	–	–	–	–	–	–	–	–	–

* For details, see Section 2 *Pins*. Regarding highlighted cells, see Section 2.3.4 *Restrictions for GPIOs and LP GPIOs*.

Revision History

Date	Version	Release notes
2026-01-20	v1.0	• Updated the "Ordering Code" to "Part Number" in Table 1-1 Comparison • Updated the pin VDD_SPI to NC for ESP32-C61HF4
2025-11-18	v0.6	• Added the new variant ESP32-C61NF8R8LA, and updated section 2.1 *Pin Layout* • Updated figure 3-1 *Visualization of Timing Parameters for the Strapping Pins* • Updated figure 7 *Packaging* by removing the TSLP
2025-08-05	v0.5	Preliminary release
2025-04-22	v0.3	• Updated Chapter 2 *Pins* • Added Section 4.2.1.7 *SDIO Slave Controller* • Updated Section 4.1.3.1 *IO MUX and GPIO Matrix* • Updated Section 4.1.3.4 *Interrupt Matrix*
2024-08-26	v0.2	• Updated the package from QFN32 to QFN40 • Added chip series ESP32-C61HF4R2, and removed ESP32-C61NR4 and ESP32-C31 chip series • Updated section 1 *ESP32-C61 Series Comparison*, section 2 *Pins*, section 3 *Boot Configurations* and Appendix ESP32-C61 Consolidated Pin Overview • Updated CoreMark score • Updated section Applications
2024-01-23	v0.1	Draft

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Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management