AsahiKASEI MICRODEVICES

AK2404

45 to 960MHz Direct Conversion Transceiver for high performance narrowband system

1. General Description

The AK2404 is a direct conversion transceiver IC that realizes high-performance narrowband wireless communication. The receiver section incorporates an LNA, quadrature demodulator, PGA, 24-bit ΔΣ A/D Converter, and digital filter to provide a receiver with high sensitivity and high interference immunity without the use of ceramic or SAW filter. In particular, the blocking characteristics of Δ10MHz are over 100dB (Standard: TIA603, EN 300 0861-1). The digital filter with variable bandwidth supports channel selection for multiple different wireless systems, enabling easy system design in wireless platforms. In addition, a ΔΣ fractional N PLL synthesizer is incorporated to configure high-performance PLLs with an external VCO. The transmitter has a built-in DAC and driver amplifier. The compact QFN Package of 8mm square contributes to the miniaturization of radio equipment.

2. Features and Applications

■ Features

- ☐ Operating Frequency: 45MHz to 960MH
- ☐ Power Supply: 2.7 to 3.45V (IOVDD: 1.7 to 1.9V also used 2.7 to 3.45V)
- ☐ Operational Temperature: -40 to +85ºC
- ☐ LNA, Attenuator (ATT) and PDET for interference detection
- ☐ Automatic PGA gain control function for high dynamic range
- ☐ High Linearity Direct Conversion I/Q Demodulator
- ☐ 24-bit ΔΣ A/D Converter: up to 192kHz Output Sampling Rate (TCXO=24.576MHz)
- ☐ Band Changeable Digital Filter (The FIR filter coefficients can be set arbitrarily)
- ☐ RSSI Functions: Data read by SPI and Analog voltage output
- ☐ FM Detection Circuit and Noise Squelch Function
- ☐ Support Zero IF and Very Low IF architecture
- ☐ DC Offset Cancelation: Real-time DC Offset Canceller (RDOC) Function and HPF
- ☐ 23-bit ΔΣ Fractional-N PLL Synthesizer
- ☐ Modulation data input interface suitable for 2-point modulation for FM/FSK applications
- ☐ 12-bit D/A Converter: 96kHz Max. Sampling Rate, S/N 72dB
- ☐ Transmission Drive Amplifier: -10 to +2dBm Output
- ☐ Local Signal Dividing Circuit and Poly Phase Filter
- ☐ TCXO Frequency: 18.432MHz / 19.2MHz / 24.576MHz recommended
- ☐ Clock Rate Converter
- ☐ Package: 68-pin QFN (8×8mm, 0.4 mm pitch)

■ Applications

- ☐ Narrow Band Radio Communications: 6.25kHz / 7.5kHz / 12.5kHz / 15kHz / 20kHz / 25kHz etc.
- ☐ Modulation Method: FM / 2FSK/ 4FSK / QPSK / π/4 DQPSK / 16QAM
  (The demodulation needs to be externally executed except the FM modulation.)
- ☐ Analog/Digital Dual Mode Transceiver
- ☐ Digital Radio System for Industrial Use
- ☐ Public Safety and Community/Emergence Radio System
- ☐ Convenience Transceiver
- ☐ Marine/Mobile Communication System
- ☐ Low power / Telemeter Transmitter
- ☐ Amateur Radio System

3. Table of Contents

4. Representation

Register names and pin names and their polarities are described below.

NameA bit = “0” or “1” …Register
NameB pin = “L” or “H” …Pin
NameC, NameD bits …Multiple registers
NameE, NameF pins …Multiple pins

To specify the bit width of a register or to indicate a specific 1-bit of the register data, describe as follows.

NameG[2:0] bits = “000” or “101”
NameH[1] bit = “0” or “1”

The address is written in the register that appears first for each page or chapter.

<Address0x9A>NameD bits

The AK2404 has multiple register maps, and <Address0x7D>PAGE bits select which register map to access.

<ROpage Address0x06>R_RSSI bits
: Indicates the READ BACK ONLY page accessed by writing PAGE bits=46(hex).
<Address0x09>PLL_R bits
: Unless otherwise specified, it indicates the normal page accessed by writing PAGE bits=00(hex).

Numerical values are described as follows.

0x9A : A hexadecimal number. Mainly used for addresses.
3B(hex) : A hexadecimal number. Mainly used for data.
18(dec) : A decimal number. Mainly used for dates.
“10101” : A binary number. Mainly use for data.

The units used to count coefficients for digital filters are shown below.

FIR：1TAP、2TAP、3TAP…
IIR：one coefficient, two coefficients, three coefficients, …

Abbreviations and acronyms are as follows.

AAF : Anti-Aliasing Filter
ADC : A/D Converter
DAC : D/A Converter
LDO : Low Drop Out
LNA : Low Noise Amplifier
LSB : Least Significant Bit
MCU : Micro Controller Unit
MSB : Most Significant Bit
PGA : Programmable Gain Amplifier

PLL : Phase Locked Loop
RDOC : Real-time DC Offset Canceller
SMF : Smoothing Filter

5. Block Diagram and Functions

5.1. Block Diagram

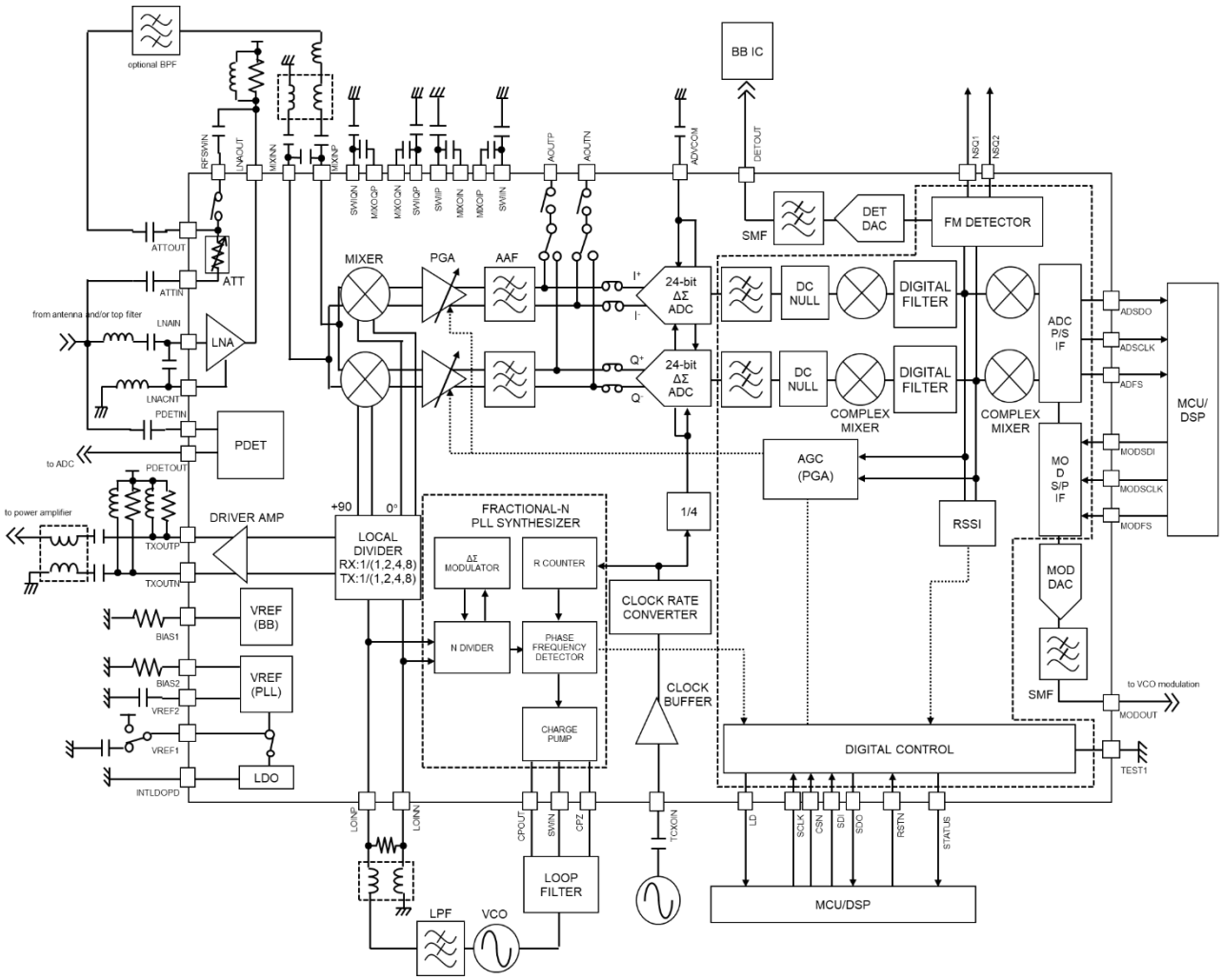


Figure 1 AK2404 Block Diagram

5.2. Block Functions

The AK2404 consists of the Analog RF Receiving Circuit (LNA, ATT and PDET), the Analog Baseband Receiving Circuit (MIXER, PGA and AAF), the Digital Receiving Circuit (ADC, DIGITAL FILTER, DC NULL, COMPLEX MIXER, AGC and ADC P/S IF), the Received Signal Strength Indication Circuit (RSSI), the FM Detection Circuit (FM DETECTION CIRCUIT, DETDAC and SMF), the Local Oscillation Circuit (PLL SYNTHESIZER, LOCAL DIVIDER, CLOCK BUFFER and CLOCK RATE CONVERTER), the Transmitting Data Generation Circuit (MOD S/P IF, MODDAC and SMF), the Transmitting Pre-amplifier Circuit (DRIVER AMP), the Reference Voltage Generation Circuit (VREF), the Internal Low Voltage Generation Circuit (LDO), and the Digital Control Circuit (DIGITAL CONTROL).

■ Analog RF Receiving Circuit (LNA, ATT, PDET)

The LNA amplifies the received signal with low noise. And the ATT attenuates the received signal. The amount of attenuation can be switched to 4 levels of 0, 6, 12 or 18dB based on the insertion loss by register setting. The LNA and the ATT are connected in parallel, and operating block can be switched by register control. The PDET detects the received RF signal strength and outputs a voltage corresponding to the RF signal strength from the PDETOUT pin. The LNA requires a matching circuit. The external filter can be added between the LNA and MIXER for the request of image rejection. Refer to 13.4 Analog Receiving Circuits (LNA, ATT, PDET, MIXER, PGA, AAF) for detail.

- Analog baseband circuit for receiver (MIXER, PGA, AAF)
  The signal amplified by the LNA is down converted to the baseband signal by the MIXER of direct conversion architecture. The MIXER works with two local signal which have a phase difference of 90 degree each other and generates the baseband signal of Ich and Qch. The MIXER input requires a matching circuit. Also, the MIXER configures a first order low pass filter with external elements. The PGA is composed by first order low pass filer with variable gain set by a register and keeps the input level of the ADC to increase the dynamic range. An AGC function is equipped to change the PGA gain automatically according to the signal input level. The AAF is anti-aliasing filter composed by the 3rd order low pass filter (Fc=100kHz) to reduce the anti-aliasing. An analog filter is composed by the MIXER, PGA and AAF to reduce the blocking signal input to the ADC. Refer 13.4 Analog Receiving Circuits (LNA, ATT, PDET, MIXER, PGA, AAF) for detail.

- Local divider (LOCAL DIVIDER)
  The LOCAL DIVIDER converts the signal generated by the PLL SYTHESIZER and input from the LOINP and LOINN pins to the local frequency by dividing the signal by 1 (undivided), 2, 4 or 8. The LOCAL DIVIDER generates two local signals with 90-degree phase difference during receiving. During transmitting, the output signal from LOCAL DIVIDER is amplified by DRIVER AMP and output. Refer 13.5 LOCAL DIVIDER for detail.

- Master clock generator(CLOCK BUFFER, CLOCK RATE CONVERTER)
  The CLOCK BUFFER amplifies the amplitude of the reference clock input from TCXOIN pin. The CLOCK RATE CONVERTER converts the frequency of reference clock and generates an internal master clock (MCLK). If the CLOCK RATE CONVERTER is not used, the reference clock is used as master clock. The master clock is used as for the clock of the ADC and digital filters and for the reference signal generating the local signal. Refer 13.6 CLOCK BUFFER+CLOCK RATE CONVERTER for detail.

- PLL synthesizer (PLL SYNTHESIZER)
  The FRACTIONAL-N PLL is composed by the PLL SYNTHESIZER, external LOOP FILTER and VCO and generates local frequency signal based on the master clock. Refer 13.7 PLL SYNTHESIZER for detail.

- Digital circuit for receiver (ADC, DIGITAL FILTER, DC NULL, COMPLEX MIXER, AGC, ADC P/S IF)
  The 24-bit ΔΣ ADC convert the analog signal generated by analog baseband circuit to digital signal. The digital filter is composed by decimation filter and channel filter to eliminate interference signal. The channel filter is composed by maximum 128TAP coefficients FIR filter which coefficients can be set arbitrarily to design the frequency characteristic freely.
  The output sampling rate is different by a path of the selected decimation filter and the maximum sampling rate is 192kHz when the reference clock of 24.576MHz is used. The DC NULL is composed by DC offset calibration and Real-time DC Offset Canceller (RDOC) to cancel the DC offset on the baseband signal.
  The COMPLEX MIXER is used for the frequency conversion between Low IF and Zero IF. The parallel-serial interface for ADC serially outputs the digital baseband signal by serial. By received signal strength, the AGC adjusts the PGA gain. Refer 13.8 Digital Receiving Circuits (ADC, DIGITAL FILTER, RSSI, AGC, ADC P/S IF) for detail.

- Receiver Signal Strength Indicator (RSSI)
  The RSSI outputs the receiver signal strength by 8bit digital data. The 8bit data is confirmed by reading via SPI. The value of RSSI can be output from ADSDO pin or STATUS pin with synchronizing to ADFS. Refer 13.8.15 RSSI Function for detail.

- FM detection circuit (FM DETECTOR, DETDAC, SMF)
  The FM DETECTOR demodulates the received FM signal. The demodulated signal is converted to analog signal by 12-bit DA (DETDAC) converter and is smoothed by the SMF with Fc=64kHz and is output from DETOUT pin. And the demodulated signal can be output as digital serial output

through the ADSDOI, ADSCLK and ADFS pins by a register setting. The output rate is same with the front digital filter. The FM DETECTOR also incorporates noise squelch function1 and noise squelch function2 and output the calculation result to NSQ1 and NSQ2 pins as High/Low signal respectively. Refer 13.8.13 FM Detection Function for detail.

- Data generator circuit for transmitter (MOD S/P IF, MODDAC, SMF)
  The MODDAC is 12-bit DA convertor and converts the digital baseband signal serially input to the MOD S/P IF to the analog baseband signal. The SMF (SMOOTHING FILTER) is a low pass filter which smoothen the DAC output (Fc=20kHz). These circuits are supposed to be used to generate the transmitter data when the direct modulation is executed to external VCO. Refer 13.9 Transmit Data Generation Circuit (MODDAC, SMF) for detail.

- Pre-amp circuit (DRIVER AMP)
  This circuit amplifies and outputs the signal divided by N by LOCAL DIVIDER. When the direct modulation is executed to external VCO, this circuit is supposed to be used as transmitter signal output. Refer 13.10 Transmit Preamplifier Circuit (DRIVER AMP) for detail.

- Internal low voltage generator circuit (LDO)
  This circuit generates 1.96V voltage from external 3V voltage source (PLLVDD) to a receiver digital circuit, a digital control circuit and a part of local oscillating circuit. It is possible to operate these circuits without using the LDO by suppling an external power supply to VREF1 pin. Refer 13.11 Internal Low Voltage Generator Circuit (LDO) for detail.

- Reference voltage generator (VREF)
  This circuit generates the reference voltage for each block.

- Digital control circuit (DIGITAL CONTROL)
  - Register write/read by 4-wire serial interface (CSN, SCLK, SDI, SDO pins)
  - Input hardware reset signal (RSTN pin)
  - The state of PLL (LD pin)
  - Output internal state (STATUS pin)

6. Pin Configurations and Functions

6.1. Pin Configurations

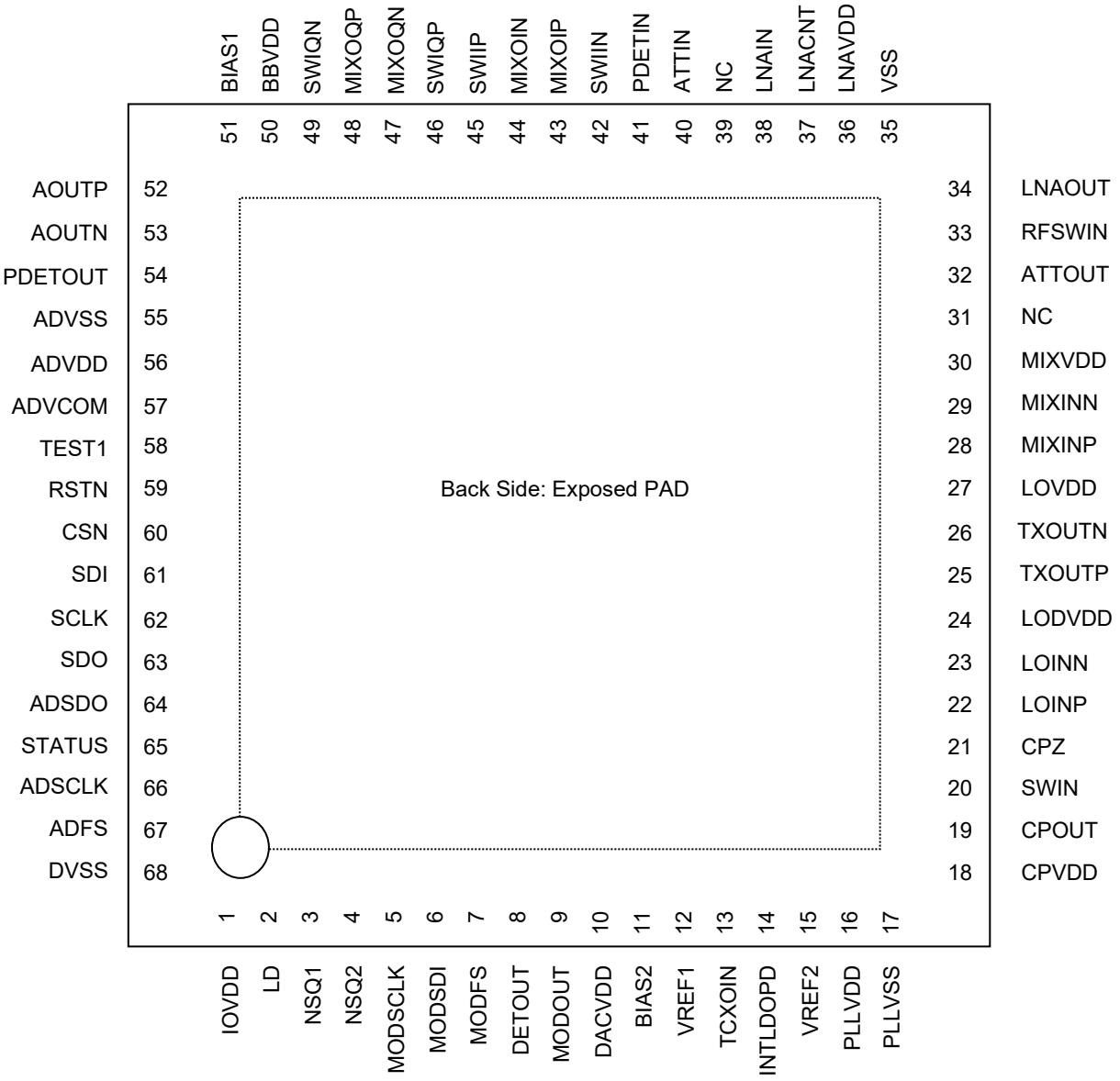


Figure 2 Pin Configurations (68-pin QFN0808, Top View)

6.2. Pin Functions

AI: Analog Input Pin, AO: Analog Output Pin, DI: Digital Input Pin, DO: Digital Output Pin,
P: Power Supply Pin, G: Ground Pin

All digital input pins must not be allowed to float.
Refer to 15.1 Reference Evaluation Board for the external element constant.

Pin#	Pin Name	I/O	Power Down State * 1	Function
1	IOVDD	P	-	Power Supply for Digital Interface Circuit
2	LD	DO	Low	Lock Detection Flag Output "L" : Unlock "H" : Lock
3	NSQ1	DO	Low	Noise Squelch Detection Flag Output 1
4	NSQ2	DIO	Low	Noise Squelch Detection Flag Output 2 * 2
5	MODSCLK	DI	Hi-Z	Clock Input for Modulation Data Interface
6	MODSDI	DI	Hi-Z	Data Input for Modulation Data Interface
7	MODFS	DI	Hi-Z	Frame Sync Input for Modulation Data Interface
8	DETOUT	AO	Hi-Z	FM Detection Signal Output
9	MODOUT	AO	Hi-Z	Modulation Signal for Transmission Output
10	DACVDD	P	-	Analog Power Supply for DETDAC and MODDAC
11	BIAS2	AI	Hi-Z	Resistor Connecting Pin for Charge Pump Current Setting Connect this pin to VSS via a 27kΩ resistor.
12	VREF1 * 3	AO	-	Stabilization Capacitor Connecting Pin for LDO Connect this pin to VSS via a 10μF capacitor.
		P	-	Digital Power Supply for Digital Circuit
13	TCXOIN	AI	Hi-Z	Reference Clock Input Connect a 100pF capacitor to this pin The pin capacitance is 3pF.
14	INTLDOPD	DI	Hi-Z	Internal LDO Disable Signal Input
15	VREF2	AO	-	Capacitor Connecting Pin for Noise Attenuation of Reference Voltage (VBG) Connect this pin to VSS via a 0.47μF capacitor.
16	PLLVDD	P	-	Analog Power Supply for LDO, N-DIVIDER and CLOCKRATE CONVERTER
17	PLLVSS	G	-	Analog Ground for LDO, N-DIVIDER and CLOCKRATE CONVERTER
18	CPVDD	P	-	Power Supply for Charge Pump
19	CPOUT	AO	Hi-Z * 4	Charge Pump Output
20	SWIN	AI	Hi-Z * 5	Resistor Connecting Pin for Fast Lock
21	CPZ	AI	Hi-Z * 5	Capacitor Connecting Pin for Loop Filter
22	LOINP	AI	Hi-Z	Local Positive Input
23	LOINN	AI	Hi-Z	Local Negative Input

24	LODVDD	P	-	Analog Power Supply for Local Divider
25	TXOUTP	AO	Hi-Z * 6	Driver Amplifier Positive Output
26	TXOUTN	AO	Hi-Z * 6	Driver Amplifier Negative Output
27	LOVDD	P	-	Analog Power Supply for Receiver Local Amplifier and Driver Amplifier
28	MIXINP	AI	350Ω Pull down	MIXER Positive Input
29	MIXINN	AI	350Ω Pull down	MIXER Negative Input
30	MIXVDD	P	-	Analog Power Supply for MIXER
31	NC	-	-	Non-Connection Connect to VSS.
32	ATTOUT	AO	11kΩ Pull down	ATT Output
33	RFSWIN	AI	Hi-Z	RF Switch Input
34	LNAOUT	AO	Hi-Z * 6	LNA Output
35	VSS	G	* 7	Ground
36	LNAVDD	P	-	Analog Power Supply for LNA and ATT
37	LNACNT	AI	Hi-Z	LNA Matching Adjustment Pin
38	LNAIN	AI	100kΩ Pull down	LNA Input
39	NC	-	-	Non-Connection Connect to VSS.
40	ATTIN	AI	101kΩ Pull down	ATT Input
41	PDETIN	AI	100kΩ Pull down	RF Power Detection Circuit Input
42	SWIIN	AI	100kΩ Pull down	Ich MIXER Switch Negative Input
43	MIXOIP	AO	100kΩ Pull down	Ich MIXER Positive Output
44	MIXOIN	AO	100kΩ Pull down	Ich MIXER Negative Output
45	SWIIP	AI	100kΩ Pull down	Ich MIXER Switch Positive Input
46	SWIQP	AI	100kΩ Pull down	Qch MIXER Switch Positive Input
47	MIXOQN	AO	100kΩ Pull down	Qch MIXER Negative Output
48	MIXOQP	AO	100kΩ Pull down	Qch MIXER Positive Output
49	SWIQN	AI	100kΩ Pull down	Qch MIXER Switch Negative Input
50	BBVDD	P	-	Analog Power Supply for Base Band Circuit and PDET
51	BIAS1	AI	Hi-Z	Current regulating resistor connection pin Connect this pin to VSS via a 47kΩ resistor.
52	AOUTP	AO	Hi-Z	Receiving Analog Baseband Signal Positive Output
53	AOUTN	AO	Hi-Z	Receiving Analog Baseband Signal Negative Output

54	PDETOUT	AO	Hi-Z	RF Power Detection Circuit Output
55	ADVSS	G	-	Analog Ground for ADC
56	ADVDD	P	-	Analog Power Supply for ADC
57	ADVCOM	AO	VSS	Stabilizing Capacitor Connecting Pin for ADC
58	TEST1	DI	100kΩ Pull down	TEST Mode Setting Pin Connect to VSS.
59	RSTN	DI	Hi-Z	Hardware Reset Signal Input The AK2404 is reset by “L” input of 1μs or more.
60	CSN	DI	Hi-Z	Chip Select Input for Register Access Interface
61	SDI	DI	Hi-Z	Data Input for Register Access Interface
62	SCLK	DI	Hi-Z	Clock Input for Register Access Interface
63	SDO	DO	Hi-Z	Data Output for Register Access Interface
64	ADSDO	DO	Low	Data Output for Receiving Data Interface
65	STATUS	DO	Low	Status Output for Receiving Data Interface
66	ADSCLK	DO	Low	Clock Output for Receiving Data Interface
67	ADFS	DO	Low	Frame Sync Output for Receiving Data Interface
68	DVSS	G	-	Digital Ground for Digital Interface Circuit and Digital Circuit
-	TAB	G	-	Exposed pad on the bottom surface of the package must be connected to VSS

Notes:
* 1. It corresponds to the state of RSTN pin=“L” or the state each block is power down by the power control register described in the chapter 13.1 Power Control.
* 2. When <Address0x30>AGC_KPSEL bit = “1”, it works as AGC_KEEP pin (DI). Refer to 13.8.12 AGC KEEP Function for detail. Even when used as DI, the initial value of this pin is DO, so pay attention to the polarity of the connected port. If necessary, handle it appropriately, such as adding a pull-down resistor.
* 3. When INTLDOPD pin = ”L”, the internal LDO works. When INTLDOPD pin = “H”, input the power supply voltage from external source to the VREF1 pin without using internal LDO. Refer to 13.11 Internal Low Voltage Generator Circuit (LDO) for detail.
* 4. Though the initial state is Hi-Z, the <Address0x16>CPO_PDST bits can switch the output state during power down. Refer to 13.7 PLL SYNTHESIZER for detail.
* 5. When <Address0x6E>PD_SYNTH_N bit = “0”, the switch of loop filter selector is OFF. Refer to 13.7 PLL SYNTHESIZER.
* 6. Power supply must be supplied via an inductor since this pin is open drain/corrector pin.
* 7. Internally connected to the TAB.

6.3. Handling of Unused Pins

Unused input / output pins must be handled appropriately by making the following settings.

■ Without using the PLL SYNTHESIZER

Pin#	Pin Name	I/O	Handling	Note
11	BIAS2	AI	Open	
16	PLLVDD	P	Supply Voltage	
17	PLLVSS	G	Connect to VSS	
18	CPVDD	P	Supply Voltage	
19	CPOUT	AO	Open	
20	SWIN	AI	Open	The same handling is also adopted in the case of that PLL SYNTHESIZER is used but the fast lock function is not used.
21	CPZ	AI	Open	Connection is required if the PLL SYNTHESIZER is used but the fast lock function is not used. Refer to 13.7 PLL SYNTHESIZER for detail.

The power must be supplied to the PLLVDD/CPVDD pins even when not using the PLL SYNTHESIZER.
When the PLL SYNTHESIZER is not used, the RDOC function can not be used.

■ Without using the LNA

Pin#	Pin Name	I/O	Handling	Note
33	RFSWIN	AI	Open	
34	LNAOUT	AO	Connect to LNAVDD	
36	LNAVDD	P	Supply Voltage	
37	LNACNT	AI	Connect to VSS	
38	LNAIN	AI	Open	

The power must be supplied to the LNAVDD pin even when not using the LNA.

■ Without using the ATT

Pin#	Pin Name	I/O	Handling	Note
32	ATTOUT	AO	Open	
33	RFSWIN	AI	Open	
36	LNAVDD	P	Supply Voltage	
40	ATTIN	G	Open	

The power must be supplied to the LNAVDD pin even when not using the ATT. If the LNA is connected to the MIXER, do not use the RFSWIN pin and connect the LNAOUT pin to the MIXINP and MIXINN pins via a matching circuit.

■ Without using the PDET

Pin#	Pin Name	I/O	Handling	Note
41	PDETIN	AI	Open	
50	BBVDD	P	Supply Voltage	
54	PDETOUT	AO	Open	

The power must be supplied to the BBVDD pin even when not using the PDET.

■ Without using MODDAC

Pin#	Pin Name	I/O	Handling	Note
5	MODSCLK	DI	Connect to VSS	
6	MODSDI	DI	Connect to VSS	
7	MODFS	DI	Connect to VSS	
9	MODOUT	AO	Open	
10	DACVDD	P	Supply Voltage	

The power must be supplied to the DACVDD pin even when not using the MODDAC.

■ Without using DRIVER AMP

Pin#	Pin Name	I/O	Handling	Note
25	TXOUTP	AO	Open	In the case of single-ended output, connect unused pin to VDD.
26	TXOUTN	AO	Open	
27	LOVDD	P	Supply Voltage	

The power must be supplied to the LOVDD pin even when not using the DRIVER AMP.

■ Without using FM detection circuit

Pin#	Pin Name	I/O	Handling	Note
8	DETOUT	AO	Open	

The power must be supplied to the DACVDD pin even when not using the FM detection circuit.

■ Without using corresponding function

Pin#	Pin Name	I/O	Handling	Note
2	LD	DO	Open	Including the case of not using lock detection function.
3	NSQ1	DO	Open	
4	NSQ2	DIO	Open	
52	AOUTP	AO	Open	
53	AOUTN	AO	Open	
65	STATUS	DO	Open	

7. Absolute Maximum Ratings

(DVSS=PLLVSS=ADVSS=VSS=0V; * 8)

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage	* 9	VDD1	-0.3	+3.6	V
	IOVDD pin	IOVDD	-0.3	+3.6	V
	VREF1 pin * 10	VREF1	-0.3	+2.3	V
Applied Analog Input Voltage		V_{AIN}	-0.3	VDD1+0.3	V
Applied Digital Input Voltage		V_{DIN}	-0.3	IOVDD+0.3	V
Applied Input Current (except Power Supply pins)		I_{IN}	-10	+10	mA
Maximum LNAIN Input Level * 11		V_{LNAIN}		2.4	Vp-p
Maximum ATTIN Input Level		ATTPOW		+10	dBm
Maximum MIXIN Input Level* 12		MIXPOW1		+14	dBm
Maximum LOIN Input Level * 13		LOPOW		+14	dBm
Maximum PDETIN Input Level		PDETPOW		+10	dBm
Storage Temperature Range		T_{stg}	-55	125	ºC

Notes:

* 8. All voltages are with respect to ground. The DVSS, PLLVSS, ADVSS and VSS must be connected to the same ground.
* 9. The VDD1 means PLLVDD, CPVDD, LODVDD, LOVDD, MIXVDD, LNAVDD, BBVDD, ADVDD, DACVDD pins.
* 10. When supplying the voltage to VREF1 pin externally, set INTLDOPD pin = “H”.
* 11. This is the AC amplitude specification without DC bias at the LNAIN pin.
* 12. This specification includes the matching circuit connected to the MIXINP and MIXINN pins.
* 13. This specification includes the matching circuit connected to the LOINP and LOINN pins.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

8. Recommended Operating Conditions

(DVSS=PLLVSS=ADVSS=VSS=0V;* 14)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Temperature Range	Ta	-40		85	ºC
Power Supply Voltage	VDD1	2.7	3.0	3.45	V
	IOVDD	2.7	3.0	3.45	V
		1.7	1.8	1.9	
	VREF1	1.7	1.8	2.0	V

Note:

* 14. All voltages are with respect to ground. The DVSS, PLLVSS, ADVSS and VSS must be connected to the same ground.

9. Digital Characteristics

9.1. DC Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit
High Level Input Voltage	* 15	V_{IH1}	0.8×IOVDD			V
	* 16	V_{IH2}	0.8×PLLVDD			V
Low Level Input Voltage	* 15	V_{IL1}			0.2×IOVDD	V
	* 16	V_{IL2}			0.2×PLLVDD	V
High Level Input Current	V_{IH1}=IOVDD * 15	I_{IH1}			+10	μA
	V_{IH2}=PLLVDD * 16	I_{IH2}			+10	μA
Low Level Input Current	V_{IL1}=0V * 15	I_{IL1}	-10			μA
	V_{IL2}=0V * 16	I_{IL2}	-10			μA
High Level Output Voltage	I_{OH}=+0.5mA * 17	V_{OH}	IOVDD-0.4		IOVDD	V
Low Level Output Voltage	I_{OL}=-0.5mA * 17	V_{OL}	0.0		0.4	V

Regarding the input current, the direction in which the current flows into the IC is defined as + and the direction in which the current flows out from the IC is defined as -.
Regarding the output current, the direction in which the current flows out from the IC is defined as + and the direction in which the current flows into the IC is defined as -.

Notes:

* 15. MODSCLK, MODSDI, MODFS, RSTN, CSN, SDI, SCLK pins and NSQ2 pin at <Address0x30>AGC_KPSEL bit = “1”
* 16. INTLDOPD pin
* 17. LD, NSQ1, NSQ2, SDO, ADSDO, STATUS, ADSCLK and ADFS pins and NSQ2 pin at <Address 0x30>AGC_KPSEL bit = “0”.

9.2. System Reset

■ Hardware Reset

Parameter		Symbol	Min.	Typ.	Max.	Unit
Hardware Reset Signal Input Width	RSTN pin	t_{RSTN}	1			μs

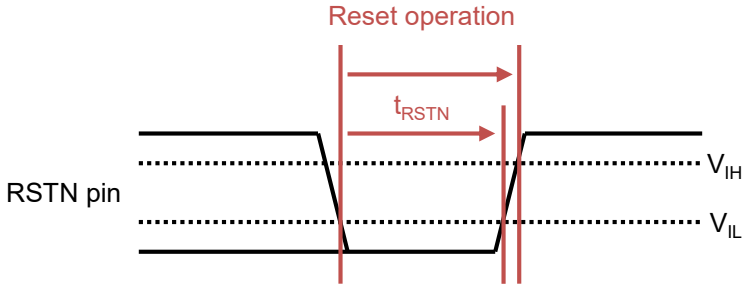


Figure 3. Hardware Reset

Hardware reset is executed by inputting “L” for 1μs or longer to the RSTN pin. All internal statuses are initialized by the hardware reset. Therefore, all operational settings should be made after this reset. For a certain reset of the device, inputs of the SCLK, the SDI and the CSN pins should be fixed to “L” or “H” during reset and reset release timings.

■ **Software Reset**

Software reset is executed by writing <Address0x7E>SRST[7:0] bits = “10101010”. All internal statuses are initialized as with the hardware reset. Therefore, all operational settings should be made after this reset. The SRST[7:0] bits will be set to “00000000” automatically after software reset is completed.

9.3. Serial Interface Timing for Register Access

Register write and read are executed via serial interface pins (CSN, SCLK, SDI and SDO pins). A serial data input to the SDI pin consists of 1 bit Read/Write instruction, 7 bits address (MSB first, A6 to A0) and 8 bits data (MSB first, D7 to D0) in one frame (16 bits). The Figure 4 shows the timing chart of the register write operation and the Figure 5 shows the timing chart of the register read operation. And the Table 2 shows the AC timing of the register write and read operation.

■ Write Access (Write Command)

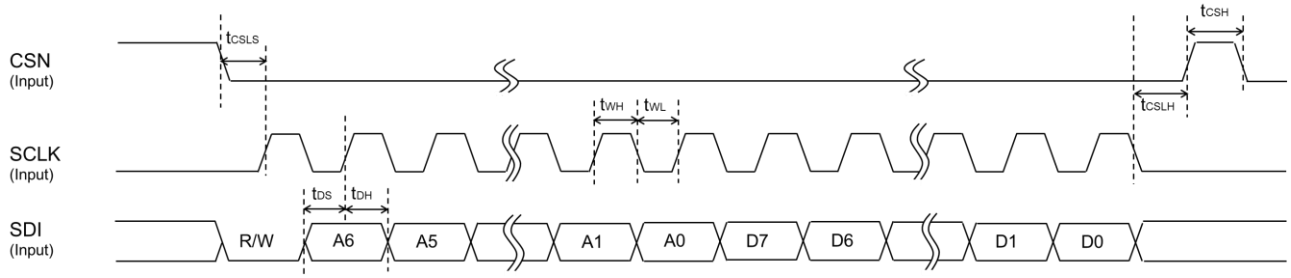


Figure 4 Interface timing for serial register write

■ Read Access (Read Command)

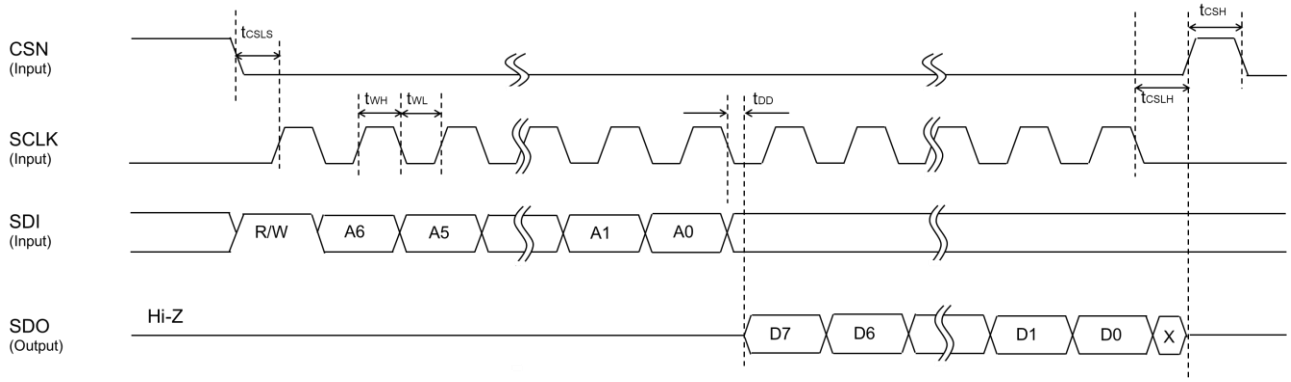


Figure 5 Interface timing for serial register read

R/W : Instruction bit controls the operation that writes data to the AK2404 or reads out data from the AK2404. When this bit is “0”, a write operation is executed. When this bit is “1”, a read operation is executed.
A6 to A0 : Register address to be accessed
D7 to D0 : Write or Read data

(1) The CSN pin should be set to “H” when not accessing to the registers. The input clock and data are ignored when the CSN pin = “H”. The serial interfaces will be activated by setting the CSN pin to “L”.

(2) In write operation, during the CSN pin = “L”, register write is executed in synchronization to a rising edge of the SCLK clock that is 16 cycles. A serial data is input to the SDI pin in the order of instruction bit, address and data. The input data is latched on the 16th rising edge of the SCLK. The CSN pin must be set to “H” every time data write is finished (note that input data will be invalid if the CSN pin becomes “H” before 16th SCLK crock count. If the clock input is kept after 16 cycles while the CSN pin = “L”, input clock and data after the 16th clock are also ignored).

(3) In read operation, instruction and address bits are received in synchronization to rising edges of first 8 SCLK clocks and the data is read out from the SDO pin in synchronization to falling edge of the 8th to 15th SCLK clocks. The CSN pin must be set to “H” every time data read is finished since a consecutive reading is not supported. The polarity of the SDO pin is output only when outputting data, and it is Hi-Z output at other timings. Also, after data output, it becomes Hi-Z output at the rising edge of the CSN pin.

9.4. Serial Interface Timing for Programmable Digital Filter Coefficient Setting

By setting the Read/Write identification bit = “0” and <Address0x42>COEF_SET bits to the specified data, the AK2404 moves to the coefficient setting mode for programmable digital filter from register writing mode. The Table 1 shows the coefficient setting mode corresponding to the specified data.

Table 1 Programmable digital filter coefficient setting mode list

R/W bit	COEF_SET[7:0] (hex)	Mode	Clock count
“0”	71	FIR Channel Filter 1 Write	2048 * 18
“0”	72	FIR Channel Filter 2 Write	2048 * 18
“0”	73	FIR Channel Filter 3 Write	2048 * 18
“0”	74	FIR Channel Filter 4 Write	2048 * 18
“0”	11	NSQ1 IIR Filter Write	160 (10 coeficients×16-bit)
“0”	12	NSQ2 IIR Filter Write	160 (10 coeficients×16-bit)
“0”	13	Out of Band Power Monitoring IIR Filter Write	160 (8 coeficients×20-bit)
“1”	F1	FIR Channel Filter 1 Read	2048 * 18
“1”	F2	FIR Channel Filter 2 Read	2048 * 18
“1”	F3	FIR Channel Filter 3 Read	2048 * 18
“1”	F4	FIR Channel Filter 4 Read	2048 * 18
“1”	91	NSQ1 IIR Filter Read	160 (10 coeficients×16-bit)
“1”	92	NSQ2 IIR Filter Read	160 (10 coeficients×16-bit)
“1”	93	Out of Band Power Monitoring IIR Filter Read	160 (8 coeficients×20-bit)

Note:

* 18. When writing and reading the coefficient of the FIR Channel Filter, if the FIR4/5 path is selected, it is 128TAP × 16-bit = 2048 clocks. When FIR3 path is selected, 64 TAP × 16-bit is repeated twice for a total of 2048 clocks.

After switching to the mode, write the coefficient data from CSN, SCLK and SDI pins according to the timings shown in Figure 6. When writing the coefficient, do not return the CSN pin to “H”, and write all data continuously in the “L” state. The Figure 6 shows an example of FIR Channel Filter (128TAP), and the coefficient data of 128TAP×16-bit=2048-bits is written continuously.

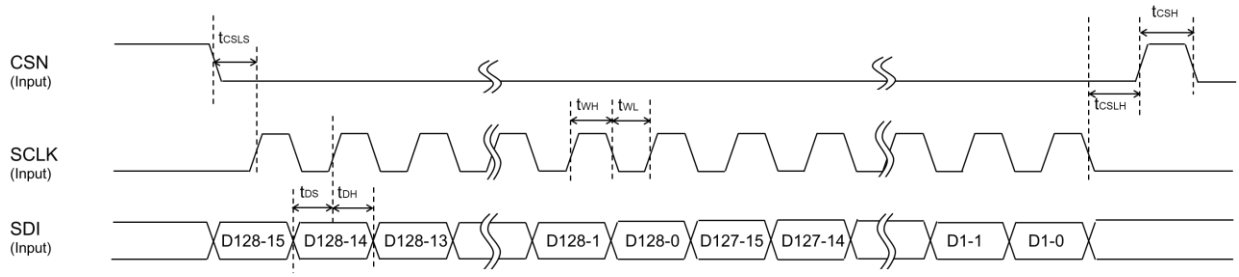


Figure 6 Interface timing for programmable digital filter coefficient write (FIR, 128TAP)

When the identification bit = “1” and the specified data is written to <Address0x42>COEF_SET bits, the mode switches from register write mode to the programmable digital filter coefficient read mode. The Table 1 shows the coefficient read mode corresponding to the specified data. After switching to the mode, read the coefficient data from CSN, SCLK, and SDO pins according to the timings shown in the Figure 7. The Figure 7 shows an example of FIR Channel Filter (128TAP), and coefficient data of 128TAP×16-bit=2048-bits is read continuously.

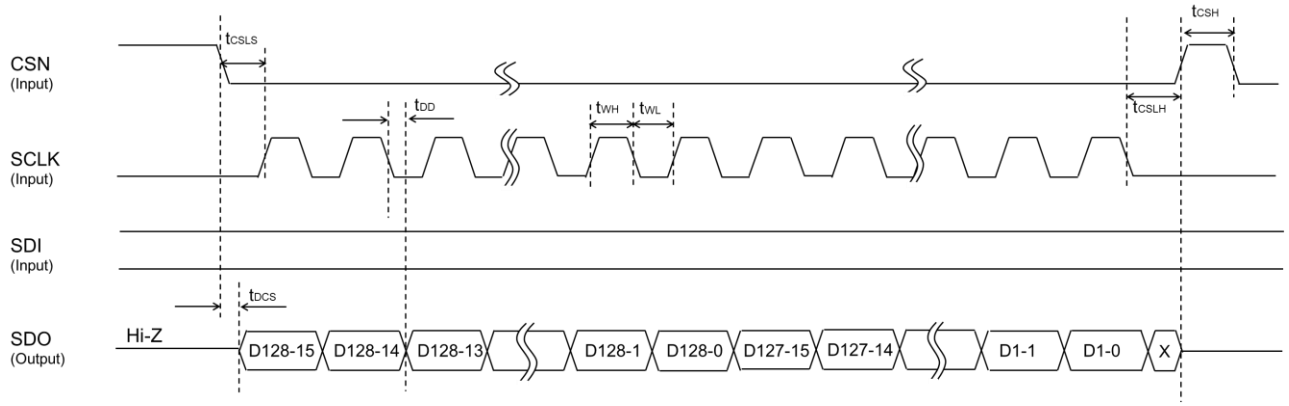


Figure 7 Interface timing for programmable digital filter coefficient read (FIR, 128TAP)

When writing/reading the coefficient, input the clock for the total number of bits of all data (described in Table 1). The programmable digital filter may not operate properly if the CSN pin is raised by inputting a clock with less or more clocks than the specified clock.

By reading back <ROpage Address0x03>R_COEFSTS_x bit (x=1, 2, 3, 4, OOB, NSQ1, NSQ2), it is possible to confirm whether writing/reading was successful or not. When R_COEFSTS_x bit = “0”, it is written/read normally. The Table 2 shows the AC timing of the programmable digital filter coefficient setting mode. For details on programmable digital filter, refer to 13.8.7 Channel Filter and 13.8.17 IIR Filter.

Table 2 AC timing of register write / read and programmable digital filter coefficient setting

Parameter		Symbol	Min.	Typ.	Max.	Unit
CSN low setup time		t_{CSLS}	50			ns
SDI setup time		t_{DS}	25			ns
SDI hold time		t_{DH}	25			ns
SCLK high time		t_{WH}	50			ns
SCLK low time		t_{WL}	50			ns
CSN low hold time		t_{CSLH}	25			ns
CSN high time		t_{CSH}	50			ns
SCLK to SDO output delay time.	20pF load	t_{DD}			45	ns
CSN to SDO output delay time	20pF load	t_{DCS}			45	ns

Digital input and output timings refer to a rising/falling signal of 0.5 × IOVDD.

9.5. Serial Interface Timing for Receiving Data and Status Output Read

The receiving data and status output are readout via serial interface that is configured with the ADFS, ADSCLK, ADSDO and STATUS pins. The data format is selected from three types of IQ 32-bit Mode, IQ 16-bit Mode and FMDET Mode by <Address0x41>ADIFSEL[1:0] bits. The Table 3 shows AC timing.

The output sampling rate (=ADFS pin output) of receiving data and status output depends on master clock (Refer to 13.6 CLOCK BUFFER+CLOCK RATE CONVERTER for the definition of f_{MCLK}), digital filter configuration set by <Address0x41>DFIL_PATH[1:0] bits and the output sampling rate division setting set by <Address0x41>RXIF_SR[1:0] bits. Refer to 13.8.18 Output Sampling Rate for detail.

The clock output from the ADSCLK pin is 64 times the output sampling rate in IQ 32-bit Mode and 32 times in both IQ 16-bit Mode and FMDET Mode. For example, when used in f_{MCLK} =24.576MHz, DFIL_PATH[1:0] bits = “01”, RXIF_SR bits = “00”, IQ 32-bit Mode, the clock frequency is 24.576MHz / 256 × 64 = 6.144MHz.

Table 3 AC timing of receiving data read

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADSCLK frequency		f_{CKA}			12.5	MHz
ADSCLK high time	20pF load	t_{WHA}	0.4 / f_{CKA}			μs
ADSCLK low time	20pF load	t_{WLA}	0.4 / f_{CKA}			μs

Digital input and output timings refer to a rising/falling signal of 0.5 IOVDD.

■ IQ 32-bit Mode

This mode uses a fast clock for 3-wire communication and is a compatible mode with the AK2401A lineup product. Set it with ADIFSEL bits = “00”. The Figure 8 shows the timing chart.

A total of 64-bit serial data is output from the ADSDO pin in synchronization with a falling edge of the ADSCLK pin. The I channel serial data is output after rising edge of the ADFS pin and the Q channel serial data is output after falling edge of ADFS pin as 32-bits data for each channel. First, 24-bits IQ data (DI23 to DI0, DQ23 to DQ0, 2's complement format, MSB first) after digital filter processes is output. Then, the internal status of RSSI and AGC is output as a status bit (S15 to S0) for 8 clocks after the last data of each “DI0” and “DQ0”. In this mode, the STATUS pin outputs “L”. Refer to 13.8.19 Status Output for detail.

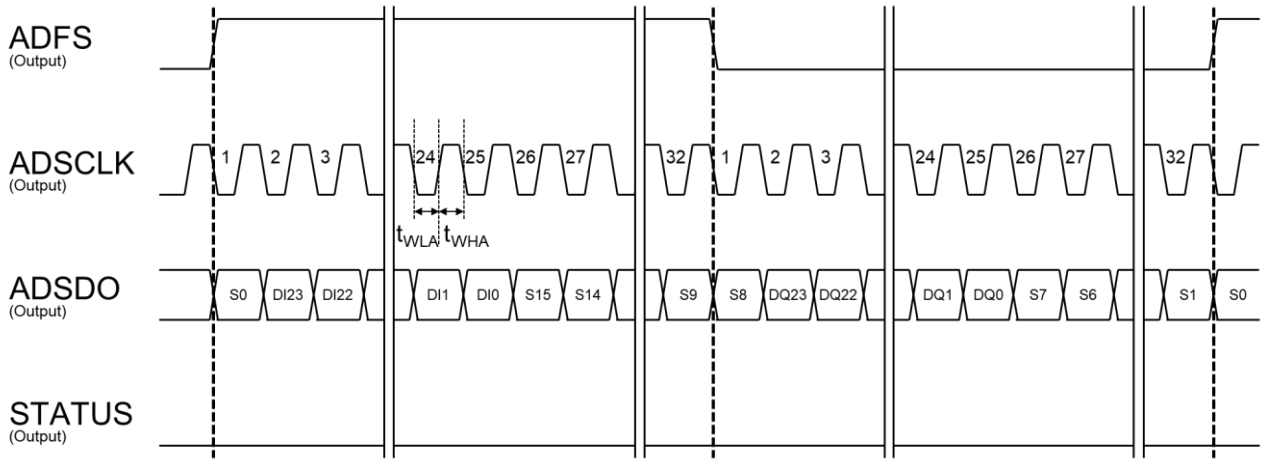


Figure 8 Interface timing for ADC data read (IQ 32-bit Mode)

■ IQ 16-bit Mode

This mode uses a slow clock for 4-wire communication. Set it with ADIFSEL bits = “01”. The Figure 9 shows the timing chart.

A 32-bit serial data is output from the ADSDO pin in synchronization with a falling edge of the ADSCLK pin. The I channel serial data is output after rising edge of the ADFS pin and the Q channel serial data is output after falling edge of ADFS pin as 16-bits data for each channel. These data are 16-bit data of I and Q channel (DI15 to DI0, DQ15 to DQ0, 2’s complement format, MSB first), and are selected by <Address0x3E>DFILOUT bits out of 24-bit data after passing the Digital Filter. The internal status of RSSI and AGC is output as a status bit (S15 to S0) from the STATUS pin. Refer to 13.8.19Status Output for detail.

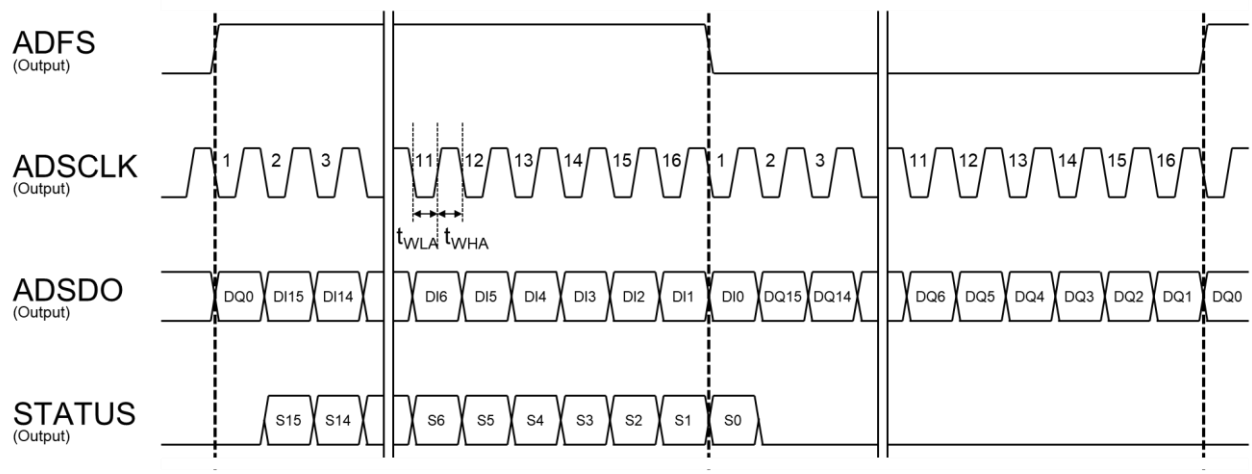


Figure 9 Interface timing for ADC data read (IQ 16-bit Mode)

■ FMDET Mode

This mode outputs the signal after FM demodulation. Set it with ADIFSEL bits = “10”. The Figure 10 shows the timing chart.

A 32-bit serial data is output from the ADSDO pin in synchronization with a falling edge of the ADSCLK pin. The FM demodulation data (DM15 to DM0, 2's complement format and MSB first) is output after rising edge of the ADFS pin as 16-bits data. After that, the internal status of RSSI and AGC is output as a status bit (S15 to S0). The STATUS pin outputs “L” in this mode. Refer to 13.8.19 Status Output for detail.

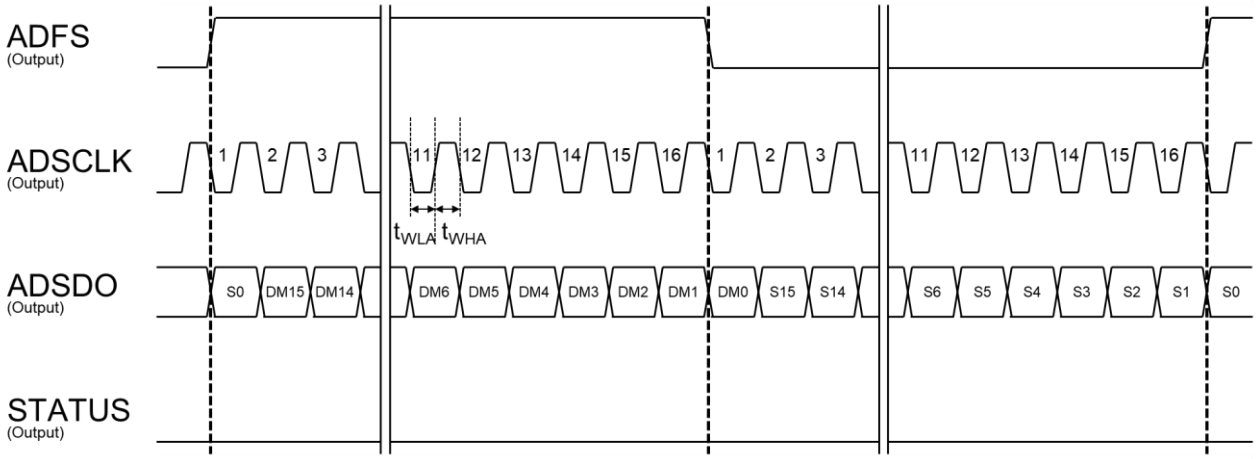


Figure 10 Interface timing for ADC data read (FMDET Mode)

9.6. Serial Interface Timing for Modulation Data Write (MOD I/F)

The modulation data write is executed via serial interface that is configured with the MODFS, MODSCLK and MODSDI pins. The Figure 11 shows the timing chart of the write operation of the modulation data and the Table 4 shows the AC timing of the write operation of the modulation data.

A total of 32-bit of serial data is input from the MODSDI pin in synchronization with the rising edge of the MODSCLK pin. The serial data consists of the Lch modulation data to be input to the OFS_MDLT section of the PLL SYNTHESIZER frequency calculation formula (described in 13.7.1 Frequency Setting) from the falling edge of the second MODSCLK pin after the falling edge of MODFS pin and the Hch modulation data to be input to MODDAC from the rising edge of the second MODSCLK pin after the rising edge of MODFS pin.
The modulation data for the Lch is 16-bit and the modulation data for Hch is 12-bit. Both are in 2's complement format and MSB first. Do not care for 4 clocks after the last modulation data “DH0” of Hch.
The input data is fixed at the rising edge of the clock that is 15 clocks after the MSB (DH11) of Hch (the rising edge of the first clock after the falling edge of the MODFS pin). It is necessary to input the additional 16 clocks as described in Figure 12 after the input data is fixed to input the final data to the MODDAC at the end of data input.
The input data is invalid if less than 16 clocks are input during the “L” or “H” interval of MODFS. And the first data is valid if the more than 16 clocks are input.

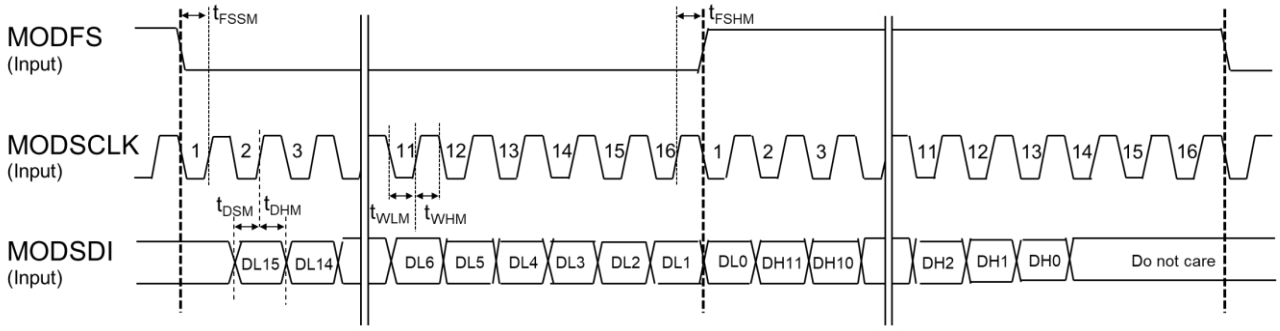


Figure 11 Interface timing for modulation data write

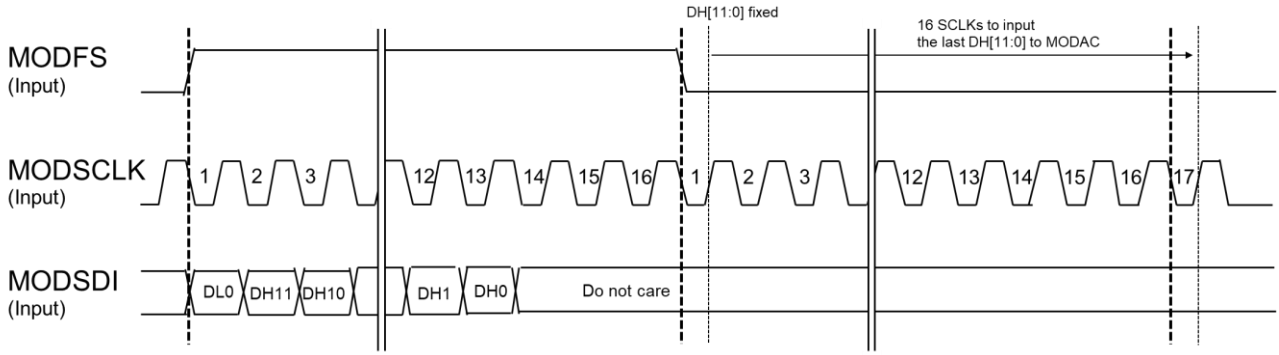


Figure 12 Interface timing for the last modulation data write

Table 4 AC timing of modulation data write

Parameter	Symbol	Min.	Typ.	Max.	Unit
MODFS frequency	f_{FSM}			96	kHz
MODFS setup time	t_{FSSM}	50			ns
MODFS hold time	t_{FSHM}	50			ns
MODSDI setup time	t_{DSM}	50			ns
MODSDI hold time	t_{DHM}	50			ns
MODSCLK high time	t_{WHM}	100			ns
MODSCLK low time	t_{WLM}	100			ns

10. Analog Characteristics

Refer to 13.1 Power Control for the setting of each operation mode.
The Reference values are not tested.
The test circuit is shown in 15.1 Reference Evaluation Board and the specification includes external circuits.

10.1. Receiving Characteristics

Unless otherwise specified, the conditions are as follows.
VDD1= 2.7 to 3.45V, IOVDD= 1.7 to 1.9V or 2.7 to 3.45V, Temperature= -40 to 85ºC

BAND1: Operating Frequency (LNA, ATT, PDET, MIXER) = 450MHz, Local Frequency = 900MHz,
<Address0x1B>DIVSEL[1:0] bits = “01” (2 div)
BAND2: Operating Frequency (LNA, ATT, PDET, MIXER) = 960MHz, Local Frequency = 960MHz,
<Address0x1B>DIVSEL[1:0] bits= “00” (no div)

10.1.1. LNA

Connecting the LNA with the ATT as shown in the 15.1 Reference Evaluation Board, the characteristics at the output at the ATTOUT pin are described. This is the characteristic evaluated in Schematic Example 2 (Figure 81 Reference Evaluation Board Example 2).

Parameter	Min.	Typ.	Max.	Unit	Description
Operating Frequency Range	45		960	MHz	
Switching Time (ATT->LNA)			50	µs	* 19
BAND1, High Power Mode, Reference Value					
Gain	14	17	20	dB	
Noise Figure		1.7	2.3	dB	
IIP3	0	5		dBm	* 20
IP1dB	-15	-7		dBm	
BAND1, Low Power Mode, Reference Value					
Gain	14	17	20	dB	
Noise Figure		1.7	2.3	dB	
IIP3	-9	-4		dBm	* 20
IP1dB	-15	-7		dBm	
BAND2, High Power Mode, Reference Value					
Gain	14	17	20	dB	
Noise Figure		2.2	2.8	dB	Reference Value
IIP3	-1	3		dBm	* 21
IP1dB	-15	-7		dBm	
BAND2, Low Power Mode, Reference Value					
Gain	14	17	20	dB	
Noise Figure		2.2	2.8	dB	
IIP3	-9	-4		dBm	* 21
IP1dB	-15	-7		dBm	

Notes:
* 19. Depends on the capacitance C1 of the matching circuit, the larger the capacitance value, the longer the time. The specified value is to connect the capacitor of 100pF specified on 15.1 Reference Evaluation Board.

* 20. Input two tone signals of 450.025MHz and 450.047MHz and measure the output signal of 450.003MHz.
* 21. Input two tone signals of 959.975MHz and 959.953MHz and measure the output signal of 959.997MHz.

10.1.2. ATT

Connecting the LNA with the ATT as shown in the 15.1 Reference Evaluation Board, the characteristics at the output at the ATTOUT pin are described. This is the characteristic evaluated in Schematic Example 2 (Figure 81 Reference Evaluation Board Example 2).

Parameter	Min.	Typ.	Max.	Unit	Description
Operating Frequency Range	45		960	MHz	
BAND1, Reference Value					
Insertion Loss	1.0	3.0	5.0	dB	ATTLVL[1:0] bits="00"
Attenuation Level * 22	4.0	6.0	8.0	dB	ATTLVL[1:0] bits="01"
	10.0	12.5	15.0	dB	ATTLVL[1:0] bits="10"
	15.0	18.5	22.0	dB	ATTLVL[1:0] bits="11"
IP1dB		20		dBm	
IIP3		30		dBm	* 23
Switching Time * 24			1	μs	
BAND2					
Insertion Loss	2.5	4.5	6.5	dB	ATTLVL[1:0] bits="00"
Attenuation Level * 22	4.5	6.5	8.5	dB	ATTLVL[1:0] bits="01"
	10.5	13	15.5	dB	ATTLVL[1:0] bits="10"
	15.5	19	22.5	dB	ATTLVL[1:0] bits="11"
IP1dB		20		dBm	Reference Value
IIP3		30		dBm	* 25
Switching Time * 24			1	μs	

Notes:
* 22. It is the relative attenuation amount from the Insertion Loss.
* 23. Input two tone signals of 450.025MHz and 450.047MHz and measure the output signal of 450.003MHz.
* 24. This specification is the switching time when switching from the LNA to the ATT and when changing ATT setting.
* 25. Input two tone signals of 959.975MHz and 959.953MHz and measure the output signal of 959.997MHz.

10.1.3. PDET

The characteristics are measured with Schematic Example 2 (Figure 81 Reference Evaluation Board Example 2) in 15.1 Reference Evaluation Board.
Set the following output offset adjustment of the PDET circuit.
<Address0x33>PDET_OFS bits = “0000” (default)
<Address0x1C> = “01101001”

Parameter	Min.	Typ.	Max.	Unit	Description
PDET					
Operating Frequency Range	45		960	MHz	
BAND1(参考値), BAND2					
Output Voltage when non modulation signal input	0.15	0.60	1.00	V	PDETIN Input=-23dBm
	0.30	0.75	1.15	V	PDETIN Input= -20dBm
	0.80	1.25	1.65	V	PDETIN Input= -10dBm
	1.30	1.75	2.15	V	PDETIN Input= 0dBm
PDET Slope1 * 26	30	50	80	mV/dB	
PDET Slope2 * 27	23	45	75	mV/dB	
PDET linearity * 28	-2.0		+2.0	dB	Reference Value
PDET Adjust Range	0.69	0.84	0.99	V	
PDET Adjust Step Size	46	56	66	mV	
PDET Additional Offset * 29	0.3	0.4	0.5	V	
Output Resistance	272	340	408	kΩ	
Load Resistance (R_L) * 30	10	100		kΩ	
Load Capacitance (C_L) * 30		10	30	pF	
Wakeup Time * 31			5	µs	Reference Value

Notes:
* 26. The PDET Slope1 is specified in the range between -23dBm and -5dBm. It is specified by 3dB step in the range between -23dBm and -20dBm and by 5dB step in the range between -20dBm and -5dBm.
* 27. The PDET Slope2 is specified in the range between -5dBm and 0dBm by 5dB step.
* 28. The output voltage at 3 points of -15dBm, -10dBm and -5dBm is linearly approximated by the least squares method, and the error to the approximate straight line at the 3 points of -23dBm, -20dBm and 0dBm is calculated. Changes of the characteristic due to changes of the temperature and the power supply voltage is not included.
* 29. The function to increase output voltage by adding offset voltage is equipped. Set <Address0x74> = 01(hex) to use this function. The characteristics of the PDET Slope and so on are not changed.
* 30. This specification is the load which the output buffer of the PDET circuit can drive.
* 31. The Wakeup Time is the time when the PDETOUT pin voltage reaches 95% of the converged value after inputting 0dBm unmodulated signal to PDETIN pin and writing the <Address0x6F> PD_PDET_N bit to “1”. It is measured under the condition of 100kΩ resistance and 10pF capacitor connected to ground as external load.

10.1.4. MIXER+PGA+AAF+ADC

The specifications are for each I channel and Q channel.
Maximum PGA Gain:
<Address0x35>PGAGAIN[5:0] bits = “000000”(+28dB)
Middle PGA Gain:
<Address0x35>PGAGAIN[5:0] bits = “011100”(0dB)

Minimum PGA Gain:
<Address0x35>PGAGAIN[5:0] bits = “110000”(-20dB)

Parameter		Min.	Typ.	Max.	Unit	Description
Operating Frequency Range		45		960	MHz	
Gain Control Range			48		dB	
Gain Control Step Size		0.7	1.0	1.3	dB	
Frequency Attenuation Characteristics (Normalized at 1kHz) RX_LPF_FC bit = “0” Low Cutoff Mode * 32, * 33	20kHz	-2	0	+1	dB	Maximum PGA Gain
	100kHz		-11		dB	
	500kHz		-74		dB	
	20kHz	-2	0	+1	dB	Middle PGA Gain
	100kHz		-3		dB	
	500kHz		-53		dB	
	20kHz	-2	0	+1	dB	Minimum PGA Gain
	100kHz		-3		dB	
	500kHz		-53		dB	
Frequency Attenuation Characteristics (Normalized at 1kHz) RX_LPF_FC bit = “1” High Cutoff Mode * 32, * 33	40kHz	-2	0	+1	dB	Maximum PGA Gain
	100kHz		-7		dB	
	500kHz		-68		dB	
	40kHz	-2	0	+1	dB	Middle PGA Gain
	100kHz		-3		dB	
	500kHz		-53		dB	
	40kHz	-2	0	+1	dB	Minimum PGA Gain
	100kHz		-3		dB	
	500kHz		-53		dB	
BAND1, High Power Mode, Reference Value						
Maximum Gain		38	42	46	dB	
Minimum Gain		-10	-6	-2	dB	
SSB Noise Figure (Zero IF) * 34			18.5	23.0	dB	Maximum PGA Gain
SSB Noise Figure (Low IF) * 35			17.5	22.0	dB	Maximum PGA Gain
Blocking SSB Noise Figure (Low IF) +10dBm, +1MHz or -1MHz * 35			37	42	dB	Maximum PGA Gain LOIN Input=0dBm
Blocking SSB Noise Figure (Low IF) +10dBm, +10MHz or -10MHz * 35			32	39	dB	Maximum PGA Gain LOIN Input=0dBm
IIP3 * 36		19	24		dBm	Middle PGA Gain
In-Band IIP2 * 37		66	80		dBm	Middle PGA Gain
Out-Band Δ1MHz IIP2 * 38		66	80		dBm	Maximum PGA Gain
Out-Band Δ10MHz IIP2 * 39		66	80		dBm	Maximum PGA Gain
Input P1dB		-28	-22		dBm	Maximum PGA Gain
Local Leak * 44			-78		dBm	LOIN Input=0dBm
BAND1, Low Power Mode, Reference Value						

Maximum Gain	38	42	46	dB	
Minimum Gain	-10	-6	-2	dB	
SSB Noise Figure (Zero IF) * 34		18.5	23.0	dB	Maximum PGA Gain
SSB Noise Figure (Low IF) * 35		17.5	22.0	dB	Maximum PGA Gain
Blocking SSB Noise Figure (Low IF) +10dBm, +1MHz or -1MHz * 35		40	45	dB	Maximum PGA Gain LOIN Input=0dBm
Blocking SSB Noise Figure (Low IF) +10dBm, +10MHz or -10MHz * 35		35	42	dB	Maximum PGA Gain LOIN Input=0dBm
IIP3 * 36	17	22		dBm	Middle PGA Gain
In-Band IIP2 * 37	66	80		dBm	Middle PGA Gain
Out-Band Δ1MHz IIP2 * 38	66	80		dBm	Maximum PGA Gain
Out-Band Δ10MHz IIP2 * 39	66	80		dBm	Maximum PGA Gain
Input P1dB	-28	-22		dBm	Maximum PGA Gain
Local Leak * 44		-78		dBm	LOIN Input=0dBm
BAND2, High Power Mode					
Maximum Gain	37	41	45	dB	
Minimum Gain	-11	-7	-3	dB	
SSB Noise Figure (Zero IF) * 34		18.5	23.0	dB	Maximum PGA Gain
SSB Noise Figure (Low IF) * 35		17.5	22.0	dB	Maximum PGA Gain
Blocking SSB Noise Figure (Low IF) +10dBm, +1MHz or -1MHz * 35		40	45	dB	Maximum PGA Gain LOIN Input=0dBm Reference value
Blocking SSB Noise Figure (Low IF) +5dBm, +10MHz or -10MHz * 35		31	36	dB	Maximum PGA Gain LOIN Input=0dBm
Blocking SSB Noise Figure (Low IF) +10dBm, +10MHz or -10MHz * 35		36	41	dB	Maximum PGA Gain LOIN Input=0dBm Reference value
IIP3 * 40	16.5	21.5		dBm	Maximum PGA Gain LOIN Input=0dBm
In-Band IIP2 * 41	55	70		dBm	Middle PGA Gain LOIN Input=0dBm
Out-Band Δ1MHz IIP2 * 42	53	70		dBm	Maximum PGA Gain LOIN Input=0dBm
Out-Band Δ10MHz IIP2 * 43	53	70		dBm	Maximum PGA Gain LOIN Input=0dBm
Input P1dB	-28	-22		dBm	Maximum PGA Gain
Local Leak * 44		-70		dBm	LOIN Input=0dBm
BAND2, Low Power Mode					
Maximum Gain	37	41	45	dB	
Minimum Gain	-11	-7	-3	dB	
SSB Noise Figure (Zero IF) * 34		18.5	23.0	dB	Maximum PGA Gain
SSB Noise Figure (Low IF) * 35		17.5	22.0	dB	Maximum PGA Gain
Blocking SSB Noise Figure (Low IF) +10dBm, +1MHz or -1MHz * 35		45	50	dB	Maximum PGA Gain LOIN Input=0dBm Reference value

Blocking SSB Noise Figure (Low IF) +5dBm, +10MHz or -10MHz * 35		36	41	dB	Maximum PGA Gain LOIN Input=0dBm
Blocking SSB Noise Figure (Low IF) +10dBm, +10MHz or -10MHz		41	46	dB	Maximum PGA Gain LOIN Input=0dBm Reference value
IIP3 * 40	15	20		dBm	Maximum PGA Gain LOIN Input=0dBm
In-Band IIP2 * 41	55	70		dBm	Middle PGA Gain LOIN Input=0dBm
Out-Band Δ1MHz IIP2 * 42	53	70		dBm	Maximum PGA Gain LOIN Input=0dBm
Out-Band Δ10MHz IIP2 * 43	53	70		dBm	Maximum PGA Gain LOIN Input=0dBm
Input P1dB	-28	-22		dBm	Maximum PGA Gain
Local Leak * 44		-70		dBm	LOIN Input=0dBm
BAND1, High Power Mode					
I/Q Gain Imbalance			0.5	dB	
I/Q Phase Imbalance			3	deg	LOIN Input=0dBm
Phase Adjust Range * 45	7	13.5	20	deg	
Phase Adjust Step Size * 45	0		0.5	deg	
BAND1, Low Power Mode					
I/Q Gain Imbalance			0.5	dB	
I/Q Phase Imbalance			3	deg	LOIN Input=0dBm
Phase Adjust Range * 45	12	18	24	deg	
Phase Adjust Step Size * 45	0		0.5	deg	
BAND2, High Power Mode, Reference Value					
I/Q Gain Imbalance			0.5	dB	
I/Q Phase Imbalance			3	deg	LOIN Input=0dBm
Phase Adjust Range * 45	20	30	37	deg	
Phase Adjust Step Size * 45	0		1.0	deg	
BAND2, Low Power Mode, Reference Value					
I/Q Gain Imbalance			0.5	dB	
I/Q Phase Imbalance			3	deg	LOIN Input=0dBm
Phase Adjust Range * 45	17	22	27	deg	
Phase Adjust Step Size * 45	0		1.0	deg	

Notes:

* 32. The Frequency Attenuation Characteristics are those of MIXER+PGA+AAF, not including the ADC.
* 33. The Frequency Attenuation Characteristics includes the effect of the external circuit elements connected to the MIXER described in Figure 80.
* 34. This is calculated from an integration value of 300Hz to 4kHz output noise. The pass band of the channel filter is set to more than 4kHz at this time.
* 35. This is measured in the condition with operating the down-conversion complex mixer (<Address 0x45>DWMIX_OFF bit = “0”) as described in 13.8.2 Complex Mixer. The frequency of the NCO (Low IF frequency) is 12.375kHz (<Address0x43>DELTA1F[7:0] bits = 21(hex)). It is calculated by integrated noise value from 300Hz to 4kHz. The pass band of the channel filter is set to more than 4kHz at this time.

* 36. Input a two-tone signal at 450.025MHz(+25kHz) and 450.047MHz(+47kHz) and measure the output signal at 3kHz. And input a two-tone signal at 449.975MHz(-25kHz) and 449.953MHz(-47kHz) and measure the output signal at 3kHz.
* 37. Input a two-tone signal at 450.00525MHz(+5.25kHz) and 450.00725MHz(+7.25kHz) and measure the output signal at 2kHz. And input a two-tone signal at 449.99475MHz(-5.25kHz) and 449.99275MHz(-7.25kHz) and measure the output signal at 2kHz.
* 38. Input a two-tone signal at 451MHz(+1MHz) and 451.002MHz(+1.002MHz) and measure the output signal at 2kHz. And input a two-tone signal at 449MHz(-1MHz) and 448.998MHz(-1.002MHz) and measure the output signal at 2kHz.
* 39. Input a two-tone signal at 460MHz(+10MHz) and 460.002MHz(+10.002MHz) and measure the output signal at 2kHz. And input a two-tone signal at 440MHz(-10MHz) and 439.998MHz(-10.002MHz) and measure the output signal at 2kHz.
* 40. Input a two-tone signal at 960.025MHz(+25kHz) and 960.047MHz(+47kHz) and measure the output signal at 3kHz. And input a two-tone signal at 959.975MHz(-25kHz) and 959.953MHz (-47kHz) and measure the output signal at 3kHz.
* 41. Input a two-tone signal at 960.00525MHz(+5.25kHz) and 960.00725MHz(+7.25kHz) and measure the output signal at 2kHz. And input a two-tone signal at 959.99475MHz(-5.25kHz) and 959.99275MHz(-7.25kHz) and measure the output signal at 2kHz.
* 42. Input a two-tone signal at 961MHz(+1MHz) and 961.002MHz(+1.002MHz) and measure the output signal at 2kHz. And input a two-tone signal at 959MHz(-1MHz) and 958.998MHz(-1.002MHz) and measure the output signal at 2kHz.
* 43. Input a two-tone signal at 970MHz(+10MHz) and 970.002MHz(+10.002MHz) and measure the output signal at 2kHz. And input a two-tone signal at 950MHz(-10MHz) and 949.998MHz(-10.002MHz) and measure the output signal at 2kHz.
* 44. The specification is at the single input port of BULUN connected to MIXINP and MIXINN pins.
* 45. The <Address0x1D>PH_ADJ_LP[6:0] bits and <Address0x1E>PH_ADJ_HP[6:0] bits are used to adjust the phase.

10.1.5. LOCAL DIVIDER(RX)

Parameter		Min.	Typ.	Max.	Unit	Description
LOIN Input Level		-5		+5	dBm	
Output Frequency Range	no div	760		960	MHz	4 levels by <Address0x1B> DIVSEL[1:0] bits
	2 div	90		960	MHz	
	4 div	45		480	MHz	
	8 div	45		240	MHz	

10.1.6. PLL SYNTHESIZER

BIAS2 pin=27kΩ

Parameter	Min.	Typ.	Max.	Unit	Description
N DIVIDER					
Operating Frequency Range	100		1920	MHz	
PHASE FREQUENCY DETECTOR(PFD)					
Phase Detector Frequency (f_{PFD})	1		25	MHz	
CHARGE PUMP(CP)					
Maximum CP Current		2560		µA	32 levels by <Address0x14, 0x15>
Minimum CP Current		80		µA	

NOISE CHARACTERISTICS					
Normalized Phase Noise		-210		dBc/Hz	* 46 Reference value

Notes:

* 46. It is calculated by the following formula with measuring in-band phase noise when PLL loop is locked. TCXOIN=24.576MHz, f_{PFD}=24.576MHz and Fractional-N operation are assumed. This specification is for when <Address0x14>CP_POLA bit = “0”.
$FoM = CN_{PLL} - 10\times\log_{10}(f_{PFD}) - 20\times\log_{10}(f_{OUT}/f_{PFD})$
FoM(Figure of Merit) : Normalized Phase Noise, CN_{PLL}: In-band Phase Noise

10.1.7. RSSI

Parameter		Min.	Typ.	Max.	Unit	Description
RSSI code <ROpage Address0x06> R_RSSI[7:0] bits Read Back	LNA Input=-120dBm	8	22	36	Dec	LNA operation <Address0x30> PGA_AGCON bit = "1" <Address0x4D> RSSI_OFST bits = 00(hex)
	LNA Input=-50dBm	148	162	176	Dec	

10.1.8. CLOCK BUFFER+CLOCK RATE CONVERTER

Parameter	Min.	Typ.	Max.	Unit	Description
TCXOIN Input Sensitivity	0.4		2	Vp-p	
TCXOIN Input Frequency Range	10	18.432 19.2 24.576	25	MHz	* 47
CLOCK RATE CONVERTER Output Frequency Range		18.432 24.576		MHz	* 47 * 48

* 47. It is recommended for the AK2404 to use 18.432MHz or 24.576MHz as the master clock frequency (f_{MCLK}) of digital circuit. If another frequency is used, warn that the frequency characteristic, the setting frequency of NCO and various setting time of digital circuit which are described later are changed. And warn that the output sampling rate of received data described in 13.8.18 Output Sampling Rate is also related to the master clock frequency.

* 48. The translation rate of the CLOCK RATE CONVERTER is set by TCXO_SEL bits. Refer to 13.6 CLOCK BUFFER+CLOCK RATE CONVERTER

10.1.9. DETDAC+SMF

Parameter		Min.	Typ.	Max.	Unit	Description
Resolution			12		bit	
Sampling Frequency				96	kHz	
Load Resistance (R_L)		10	100		kΩ	
Load Capacitance (C_L)			50	100	pF	
DC Characteristics						
DNL				1	code	
INL				2	code	
Output DC Level	code = 7FF(hex)	1.92	2.12	2.32	V	
	code = 800(hex)	0.57	0.77	0.97	V	
AC Characteristics						
Output Level * 49		1.15	1.35	1.55	Vp-p	
Reference Level * 49		1.35	1.45	1.55	V	
S/N * 49		66	72		dB	
SINAD * 49		59	65		dB	
SMF Frequency Characteristics	1kHz	-1	0	1	dB	
	64kHz	-10	-3	1	dB	
	128kHz	-35	-20	-5	dB	

* 49. RL= 100kΩ, CL= 50pF, fs= 96kHz, Input code: full scale 1kHz sine wave, Integrated Noise bandwidth:300Hz to 48kHz, Observed DETOUT pin

10.2. Transmission Characteristics

Unless otherwise specified, the conditions are as follows.
VDD1= 2.7 to 3.45V, IOVDD= 1.7 to 1.9V or 2.7 to 3.45V, Temperature= -40 to 85ºC

10.2.1. MODDAC+SMF

Parameter		Min.	Typ.	Max.	Unit	Description
Resolution			12		bit	
Sampling Frequency				96	kHz	
Load Resistance (R_L)		10	100		kΩ	
Load Capacitance (C_L)			50	100	pF	
DC Characteristics						
DNL				1	code	
INL				2	code	
Output DC Level	code = 7FF(hex)	1.92	2.12	2.32	V	<Address0x21> MODDAC_AG bits="00"
	code = 800(hex)	0.57	0.77	0.97	V	<Address0x21> MODDAC_AG bits="00"
AC Characteristics						
Output Level * 50		1.15	1.35	1.55	Vp-p	<Address0x21> MODDAC_AG bits="00"
Reference Level * 50		1.35	1.45	1.55	V	
SMF Gain * 50			0		dB	MODDAC_AG bits="00"
		-8	-6	-4	dB	MODDAC_AG bits="01"
		-14	-12	-10	dB	MODDAC_AG bits="10"
S/N * 50		66	72		dB	
SINAD * 50		59	65		dB	
SMF Frequency Characteristics	1kHz	-1	0	1	dB	
	20kHz	-12	-4	1	dB	
	100kHz	-64	-44	-24	dB	

* 50. RL= 100kΩ, CL= 50pF, fs= 96kHz, Input code: full scale 1kHz sine wave,
Integrated Noise bandwidth:300Hz to 48kHz, Observed MODOUT pin

10.2.2. LOCAL DIVIDER(TX)+DRIVER AMP

Parameter		Min.	Typ.	Max.	Unit	Description
LOIN Input Level		-5		+5	dBm	
Output Frequency Range	no div	760		960	MHz	4 levels by <Address0x1B> DIVSEL[1:0] bits
	2 div	90		960	MHz	
	4 div	45		480	MHz	
	8 div	45		240	MHz	
Output Power * 51			+2		dBm	4 levels by <Address0x22> TXOLV[1:0] bits
			-1		dBm	
			-4		dBm	
			-10		dBm	
Phase Noise * 52	10kHz		-132		dBc/Hz	TXOLV[1:0] bits = "11" LOIN Input=0dBm Reference value
	100kHz		-143		dBc/Hz	
	1MHz		-151		dBc/Hz	
	10MHz		-155	-150	dBc/Hz	

* 51. The matching condition of the test circuit is adjusted to a wide frequency range.
* 52. This specification is the output phase noise of TXOUTP and TXOUTN pins when the local signal is input from an external signal source via the LOINP and LOINN pins.

10.3. Current Consumption

Unless otherwise specified, the conditions are as follows.
VDD1= 2.7 to 3.45V, IOVDD= 1.7 to 1.9V or 2.7 to 3.45V, Temperature = -40 to 85ºC
f_{MCLK} = 24.576MHz (Refer to 13.6 CLOCK BUFFER+CLOCK RATE CONVERTER for the definition of the f_{MCLK}.)
The drive current of the digital output pin is not included.
Connect the INTLDOPD pin to VSS to power up the LDO circuit.

■ Current Consumption of Each Function

The block numbers described in the Operation Block correspond to the description numbers of "Current Consumption of Each Block" and the block numbers described in 13.1 Power Control.

Parameter	Operation Block	Min.	Typ.	Max.	Unit	Description
BIAS ONLY	[1], [14]		1.5	2.2	mA	
PLL ONLY	[1], [3], [5], [14]		11	17	mA	
RX operation Low Power Mode	[1], [3], [5], [9], [10], [11], [13], [14]		87	119	mA	* 53
RX operation High Power Mode	[1], [3], [5], [9], [10], [11], [13], [14]		109	149	mA	* 54
TX operation +2dBm Output	[1], [2], [3], [5], [12], [13], [14]		60	81	mA	* 55

* 53. <Address0x1B>DIVSEL [1:0] bits = "01", <Address0x1A>LPMODE_LNA bit = "1", <Address0x1B>HPMODE_LOBLK bit = "0", <Address0x75>I_PGA [1:0] bits = "01", <Address0x75>I_AAF bit = "0", MIXER output frequency = 1kHz
* 54. DIVSEL[1:0] bits = "01", LPMODE_LNA bit = "0", HPMODE_LOBLK bit = "1", I_PGA[1:0] bits = "01", I_AAF bit = "0" , MIXER output frequency = 1kHz
* 55. DIVSEL[1:0] bits = "01", <Address0x22>TXOLV[1:0] bits = "11",

■ Current Consumption of Each Block (Reference Value)

Parameter			Min.	Typ.	Max.	Unit	Description
VREF				0.6		mA	[1]
MODDAC				5.5		mA	[2]
PLL SYNTHESIZER				8.5		mA	[3]
CLOCK RATE CONVERTER				6		mA	[4]
CLOCK BUFFER				1		mA	[5]
DETDAC				5		mA	[6]
PDET				11		mA	[7]
ATT				0		mA	[8]
LNA	High Power Mode			18		mA	[9]
	Low Power Mode			5.5		mA	
ADC+DIGITAL				28		mA	[10]
MIXER+PGA+AAF +LOCAL DIVIDER(RX)	High Power Mode	no div		41		mA	[11] + [13]
		2 div		50		mA	
		4 div		54		mA	
		8 div		57		mA	
	Low Power Mode	no div		34		mA	
		2 div		40		mA	
		4 div		44		mA	
		8 div		47		mA	
DRIVER AMP	(+2dBm)			29		mA	[12]
	(-1dBm)			20		mA	
	(-4dBm)			14		mA	
	(-10dBm)			7.5		mA	
LOCAL DIVIDER(TX)	no div			9		mA	[13]
	2 div			15		mA	
	4 div			20		mA	
	8 div			23		mA	
STANDBY				1		mA	[14]

■ Current consumption of each block on the VREF1 pin (Reference value)

The current in VREF1 pin (1.8V) of the current described in Current Consumption of Each Block is as follows. Refer to this when using in the external supply mode of INTLDO pin = “H”.

Parameter	Min.	Typ.	Max.	Unit	Description
PLL SYNTHESIZER		1.5		mA	[3]
CLOCK RATE CONVERTER		6		mA	[4]
CLOCK BUFFER		1		mA	[5]
DIGITAL		25		mA	[10]

11. Standard Characteristics Example

The evaluation data assuming various wireless communication standards are prepared as application note. Please inquire separately.

12. Operating Sequence

12.1. Power-up Sequence

The AK2404 has an LDO for low power supply voltage circuit as well as external supply voltage (VDD1, IOVDD). Also, as described in 13.11 Internal Low Voltage Generator Circuit (LDO) by inputting “H” to INTLDOPD pin, the external power supply voltage is supplied to VREF1 pin without using the internal LDO. The power-up sequences when using the internal LDO and when supplying voltage to VREF1 pin externally are shown below. The VDD1 covers PLLVDD, CPVDD, LODVDD, LOVDD, MIXVDD, LNAVDD, BBVDD, ADVDD, DACVDD pins as defined in 7 Absolute Maximum Ratings.

AKM shall not be liable for any operation other than the power-up sequence described in this data sheet.

12.1.1. Using Internal LDO

If the internal LDO is used, connect the INTLDOPD pin to VSS. The “L” input of the RSTN pin (hardware reset) is used to initialize the internal circuit when the power supplies (VDD1, IOVDD) are turned on. Therefore, the RSTN pin must be held to “L” until VREF1 pin and VREF2 pin outputs stabilize after the power supplies (VDD1 and IOVDD) are turned on. The stabilization time of the VREF1 pin and VREF2 pin outputs depend on external capacitance of the VREF1 pin and VREF2 pin, and is up to 10ms when 100pF and 10µF are connected in parallel to VREF1 and 0.47µF is connected to VREF2 pin.

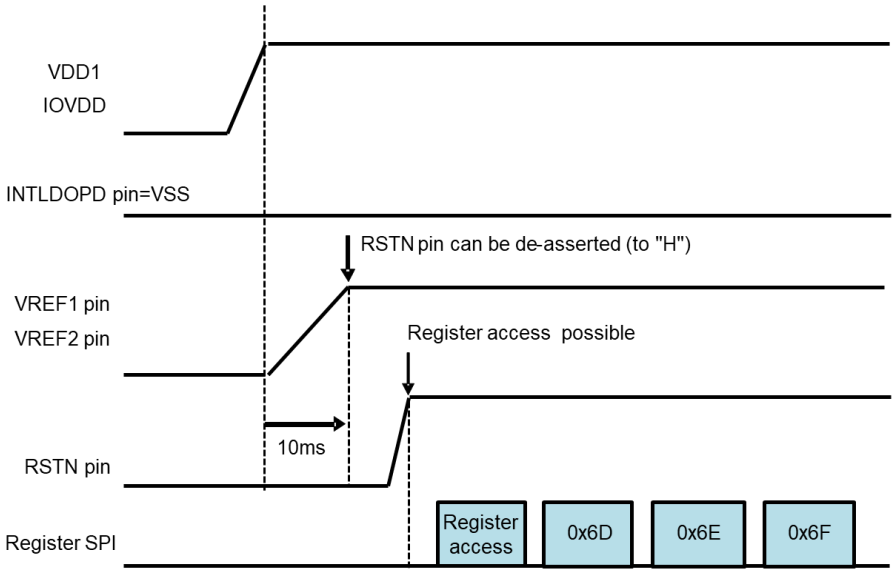


Figure 13 Power-up sequence (using internal LDO)

1. Set the RSTN pin to “L” and turn on the power supplies (VDD1 and IOVDD) with the INTLDOPD pin = VSS. The IOVDD must be turn on before or at the same time with the PLLVDD. It is not necessary to consider the power-up sequence except the PLLVDD and IOVDD, but it is recommended to turn on all power supplies at the same time. Supply the power supply voltage to unused blocks, and use the register to power down. The VREF1 pin and VREF2 pin described in 2 will be turned on at the same time as the PLLVDD is turned on.

2. After the power supplies (VDD1 and IOVDD) are turned on, the VREF1 pin and VREF2 pin are

turned on up to 10ms later, enabling the RSTN pin to be turned on.

3. When the RSTN pin is set to “H”, the register writing is enabled.

4. Write arbitrary registers. The <Address0x6D>PD_REF_N bit must be turned on earlier than the <Address0x6F>PD_RX_N bit as described in 13.1 Power Control.

12.1.2. Supplying voltage to VREF1 pin externally

If the power voltage is supplied to the VREF1 pin externally without using the internal LDO, connect the INTLDOPD pin to the PLLVDD. The “L” input of the RSTN pin (hardware reset) is used to initialize the internal circuit when the power supplies (VDD1, IOVDD and VREF1) are turned on. Therefore, the RSTN pin must be held to “L” until the VREF2 pin output stabilizes after the power supplies (VDD1, IOVDD and VREF1) are turned on. The stabilization time of the VREF2 pin output depends on external capacitance of the VREF2 pin, and is up to 10ms when the capacitor of 0.47µF is connected to the VREF2 pin.

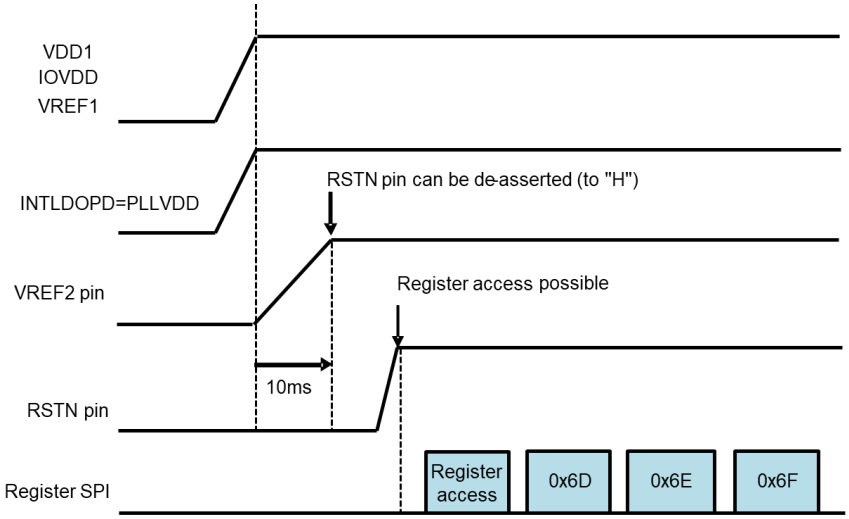


Figure 14 Power-up sequence (external power supply to VREF1 pin)

1. Set the RSTN pin to “L” and turn on the power supplies (VDD1, IOVDD and VREF1) with the INTLDOPD pin = PLVDD. The IOVDD must be turn on before or at the same time with the PLLVDD. It is not necessary to consider the power-up sequence except the PLLVDD and IOVDD, but it is recommended to turn on all power supplies at the same time. Supply the power supply voltage to unused blocks, and use the register to power down.

2. After the power supplies (VDD1, IOVDD and VREF1) are turned on, the VREF2 pin is turned on up to 10ms later, enabling the RSTN pin to be turned on.

3. When the RSTN pin is set to “H”, the register writing is enabled.

4. Write arbitrary registers. The <Address0x6D>PD_REF_N bit must be turned on earlier than the <Address0x6F>PD_RX_N bit as described in 13.1 Power Control.

12.2. Power-up Sequence of the PLL Synthesizer

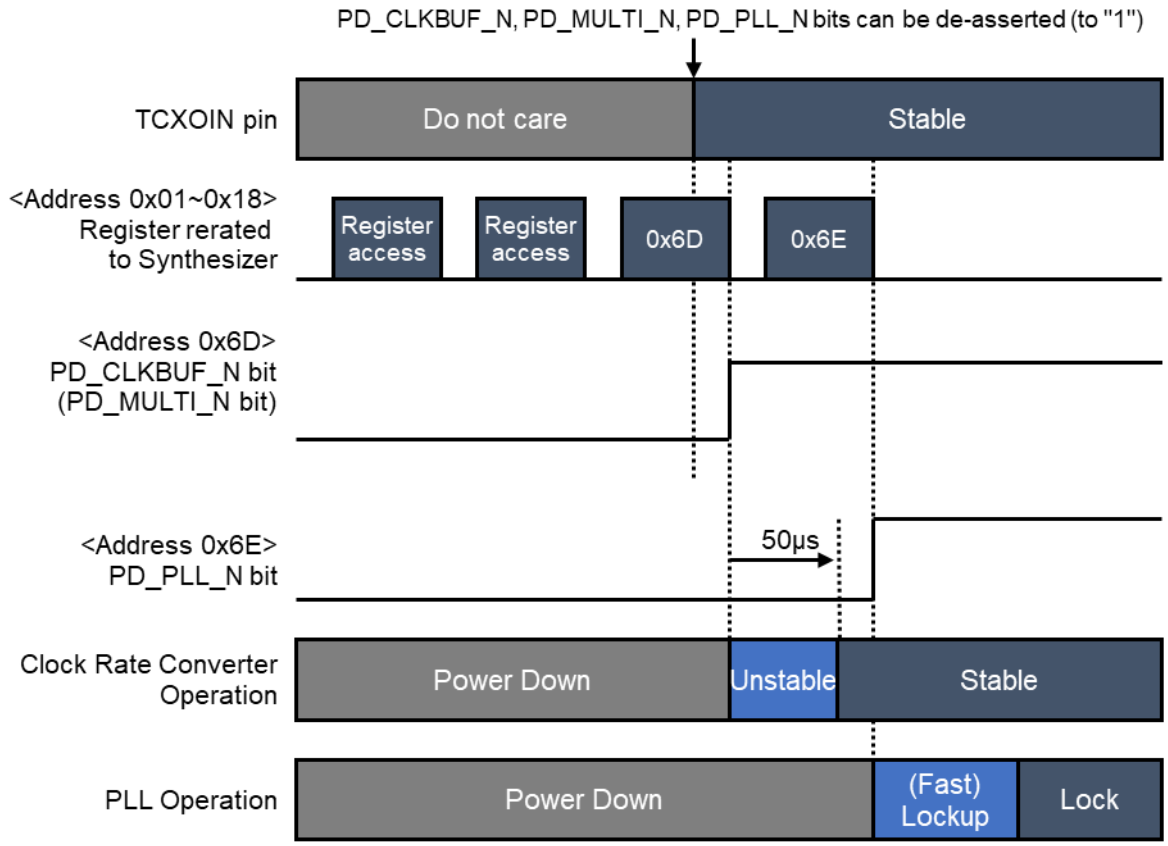


Figure 15 Power-up Sequence of the PLL Synthesizer

The PLL SYNTHESIZER starts the lock operation by writing <Address0x6E>PD_PLL_N bit = “1”. Set the registers related to the PLL SYNTHESIZER in advance.

Set <Address0x6D>PD_CLKBUF_N bit = “1” after the reference clock input from TCXOIN pin is stable. Set <Address0x6D>PD_MULTI_N bit = “1” at the same time if the CLOCK RATE CONVERTER is used. Then, after the stabilization time of 50µs has elapsed, write PD_PLL_N bit = “1” and turn on PLL SYNTHESIZER. Refer to 13.1 Power Control for more information on the power control.

The PLL SYNTHESIZER starts lock up operation after 256/f_{PFD} (about 11µs when f_{PFD}=24.576MHz) triggered by writing PD_PLL_N bit = “1”. At that time, if <Address0x16>FASTEN bit = “1”, the fast lock up counter operates and the fast lock up operation is performed. Refer to 13.7.3 Fast Lock Function.

The LD pin is set to unlock state (“L”) during the PLL SYNTHESIZER is turned off with PD_PLL_N bit = “0”. Refer to 13.7.4 Lock Detection for detail.

12.3. Power-up Sequence of the Receiver

To turn on the receiver, write “1” to <Address0x6F>PD_RX_N bit and PD_ADC_N bit when 50ms has elapsed after setting <Address0x6D>PD_REF_N bit = “1” and when the PLL generating the local signal is locked. Then, execute calibration to eliminate the DC offset.

The calibration starts by writing “1” to Address 0x24> OFSCAL1 and OFSCAL2 bits. If OFSCAL1 and OFSCAL2 bits are set to “1” simultaneously, analog calibration is executed first, then the digital calibration is automatically executed. If the calibration is executed separately, execute the analog block (OFSCAL1) first, then execute the digital block (OFSCAL2).

The Figure 16 shows the operation sequence of the power-up of the receiver. For more information, including the CAL time (2), refer to 13.8.8 DC Offset .

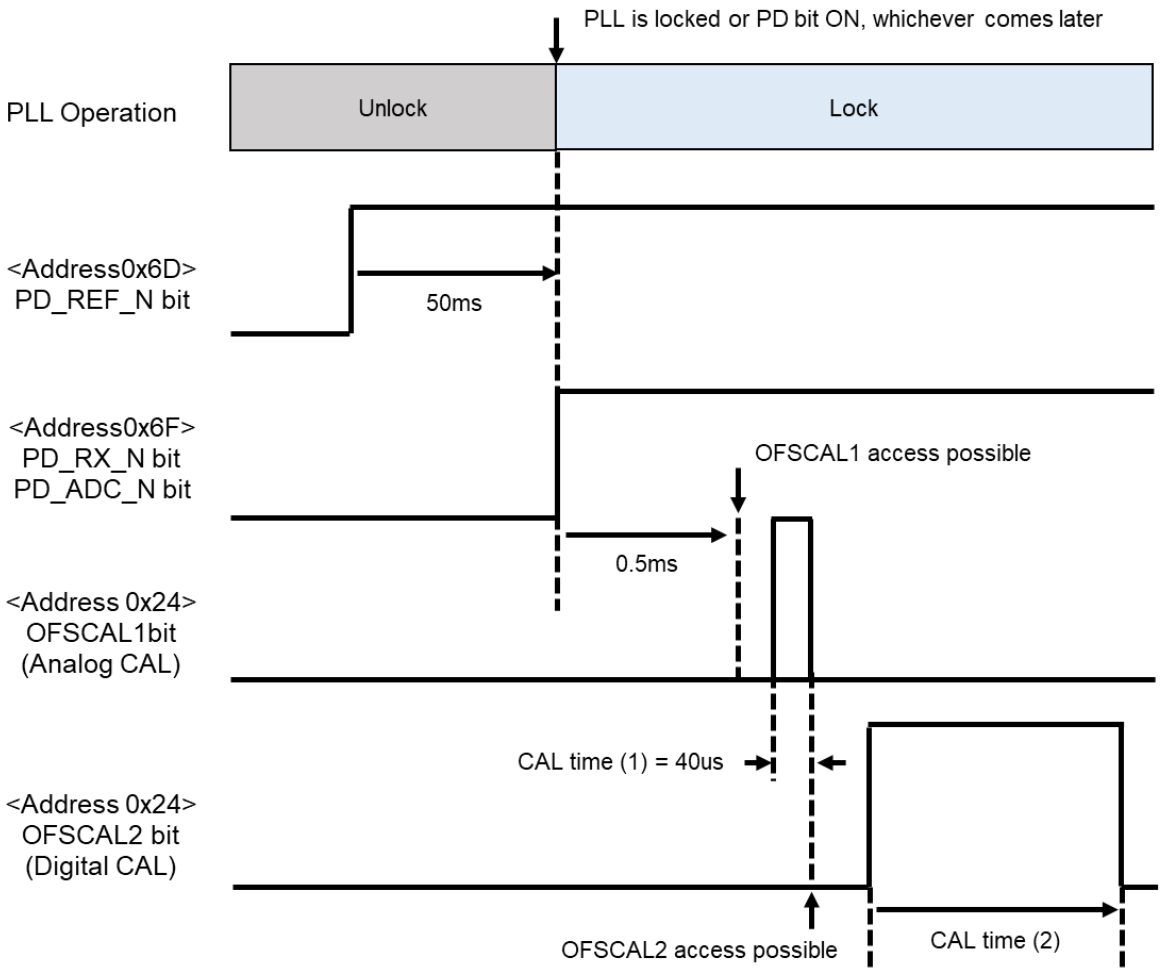


Figure 16 Power-up sequence of the Receiver

13. Functional Description

13.1. Power Control

The power management of the AK2404 is controlled by <Address0x6D to 6F> power down register and INTLDOPD pin. The Figure 17 shows 14 blocks that are controlled by these settings. Writing “1" to the register powers up the corresponding block. The LDO circuit is powered up by inputting “L” to the INTLDOPD pin and powered down by inputting “H”.

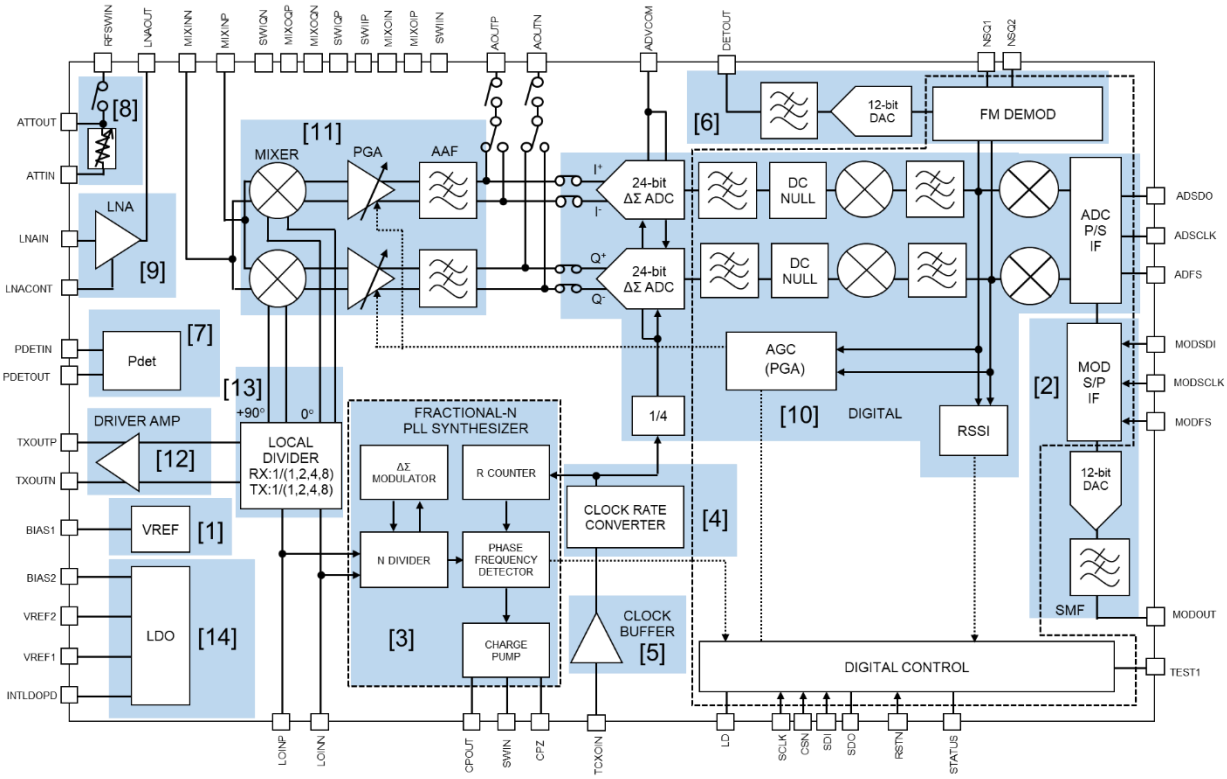


Figure 17 Power Management Block

Table 5 Power Management Block and Control Method

Control Method	Name	Power Management Block													
		[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]	[11]	[12]	[13]	[14]
Pin	INTLDOPD pin														●
Register	PD_REF_N	●													
Register	PD_MODDAC_N		●												
Register	PD_PLL_N			●											
Register	PD_MULTI_N				●										
Register	PD_CLKBUF_N					●									
Register	PD_TX_N												●	●	
Register	PD_DETDAC_N						●								
Register	PD_PDET_N							●							
Register	PD_ATT_N								●						
Register	PD_LNA_N									●					
Register	PD_ADC_N										●				
Register	PD_RX_N											●		●	

* 56. The blocks of [7] to [13] should be powered up after the block of [1] (VREF) is powered up. Also, at the power down, the block of [1] should be powered down after the blocks of [7] to [13] are powered down.
* 57. The LOCAL DIVIDER of [13] is controlled by PD_RX_N bit or PD_TX_N bit. It operates by setting "1" in either register.

13.1.1. Power Control Logic of the LNA and ATT

The LNA and ATT do not power up at the same time. According to the truth table of the Table 6, the LNA and ATT are controlled by the register setting. When both PD_LNA_N bit and PD_ATT_N bit are set to "1", only the ATT becomes power-up.

Table 6 Power control logic of the LNA and ATT

PD_LNA_N	PD_ATT_N	Power Control
0	0	Both of LNA and ATT are off state.
0	1	Only ATT is active.
1	0	Only LNA is active.
1	1	Only ATT is active.

13.2. Operation Mode Setting

The operation mode and control registers of the AK2404 are shown in the Table 7.

Table 7. Operation Mode and Control Register

Operation Mode	Control Register	Polarity	Controlled Block
High Power Mode	<Address0x1A> LPMODE_LNA bit	0	[9]LNA
Low Power Mode		1	
Low Power Mode	<Address0x1B> HPMODE_LOBLK bit	0	[13]LOCAL DIVIDER(RX)
High Power Mode		1	
Low Cutoff Mode	<Address0x1A> RXLPF_FC bit	0	[11]PGA
High Cutoff Mode		1	
I_PGA bits = "00"	<Address0x75> I_PGA bits	00	[11]PGA
I_PGA bits = "01"		01	
I_PGA bits = "10"		10	
I_PGA bits = "11"		11	
I_AAF bit = "0"	<Address0x75> I_AAF bit	0	[11]AAF
I_AAF bit = "1"		1	

13.3. Level Diagram

13.3.1. Level Diagram of Analog Receiving Circuit

The Figure 18 shows the level diagram of the analog receiving circuit when setting <Address0x30> PGA_AGCON bit = “1” (during AGC operation). Refer to 13.8.10 for detail about AGC function.

The AGC operates so that the ADC input level becomes the set value of <Address0x36>AGCTGT bits and the PGA gain is changed to expand the dynamic range of the system. The PGA gain for the LNA input depends on the AGCTGT bits set, and the level diagram when AGCTGT bits = “0000” (+6dBm) is described here. The gain of MIXER+PGA+AAF is described with the value of BAND1.

To operate the ATT when a system detects strong input can reduce the input level of the MIXER and improve the distortion characteristics. The level diagrams are shown here when -30dBm input with <Address0x33>ATTLVL bits = “00”(-4dB) setting and +10dBm input with <Address0x33>ATTLVL bits = “11”(-22dB) setting.

The full-scale level of 24-bit ΔΣ ADC is 1.7 x (ADVDD:3.0V) = 5.1Vp-p, and the maximum input level is +18.1dBm when converted by 50Ω.

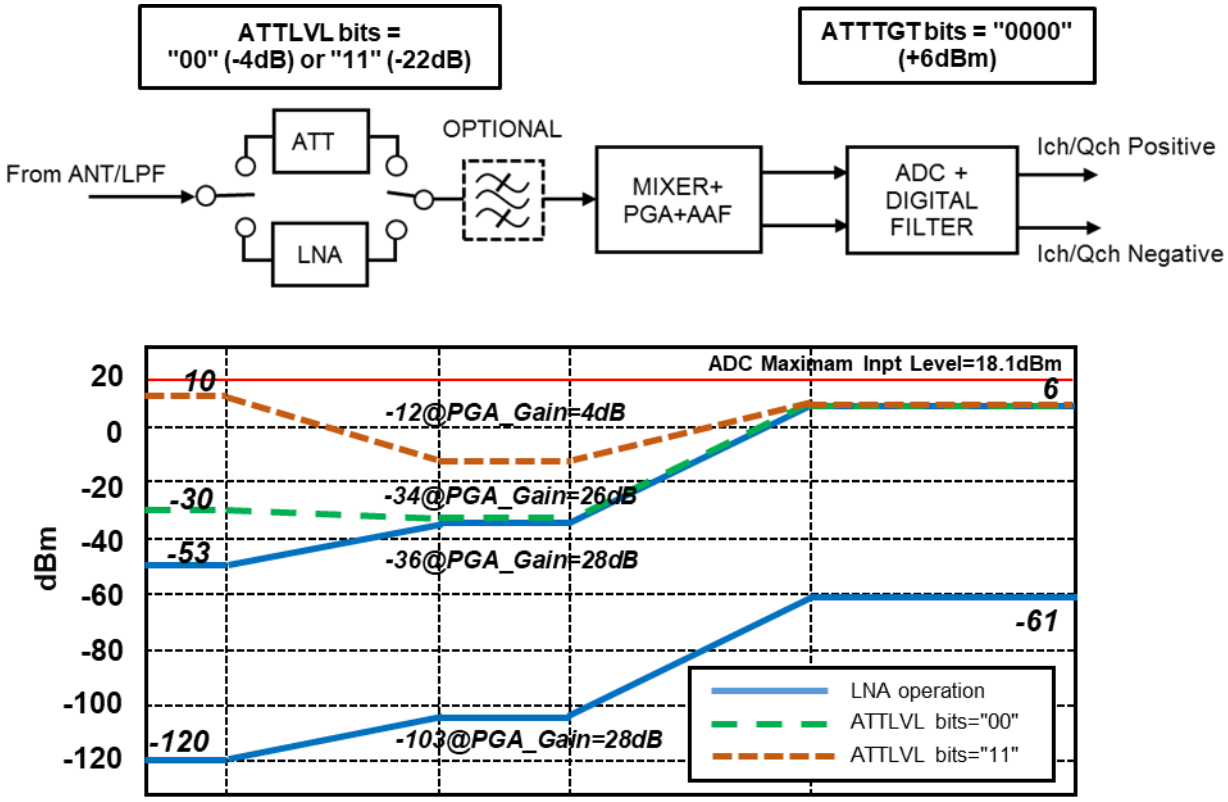


Figure 18 Level Diagram of Analog Receiving Circuit

13.3.2. Level Diagram of Digital Receiving Circuit

The Figure 19 shows the level diagram of digital receiving circuit. The maximum input level of the 24-bit ΔΣ ADC is +18.1dBm (=1.7 × VDD1[Vp-p]), which is -7dB FS for 24-bit Full Scale. If the input level exceeds this maximum level, clipping occurs. The received signal is attenuated 6dB in the decimation filter block. Therefore, set the DC gain of the channel filter to +6dB so that the total gain of the digital receiving circuit is 0dB. Since the channel filter consists of a programmable FIR filter, the DC gain is determined by the coefficient and bit adjustment settings. Refer to 13.8.7 Channel Filter for detail.

The RDOC (Real-time DC Offset Canceller) is optimized for a condition that the total gain of the digital filter is 0dB.

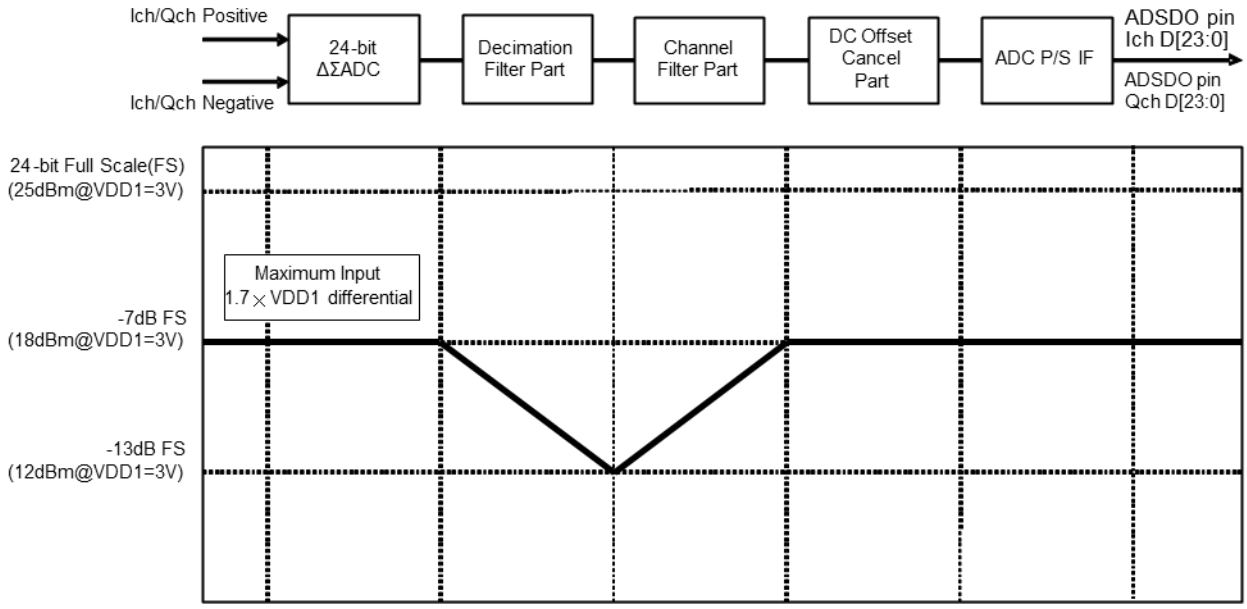


Figure 19 Level Diagram of Digital Receiving Circuit

13.4. Analog Receiving Circuits (LNA, ATT, PDET, MIXER, PGA, AAF)

13.4.1. LNA, ATT

The LNA amplifies the received RF signal with low noise. And the ATT attenuates the received RF signal. The LNA and ATT are located in parallel and one of them becomes active. Refer to 13.1 Power Control for detail.

The matching circuit is required for the input of the LNA. The input and output of the ATT is matched to 50Ω internally. When the LNA is active, the impedance at input and output of the ATT appears Hi-Z because the ATT is off. Therefore, the LNA is not influenced. And when the ATT is active, the impedance of input and output of the LNA appears Hi-Z because the LNA is off state. Therefore, the ATT is not influenced. The Figure 20 shows the impedance state when the LNA is active and the Figure 21 shows the impedance state when the ATT is active.

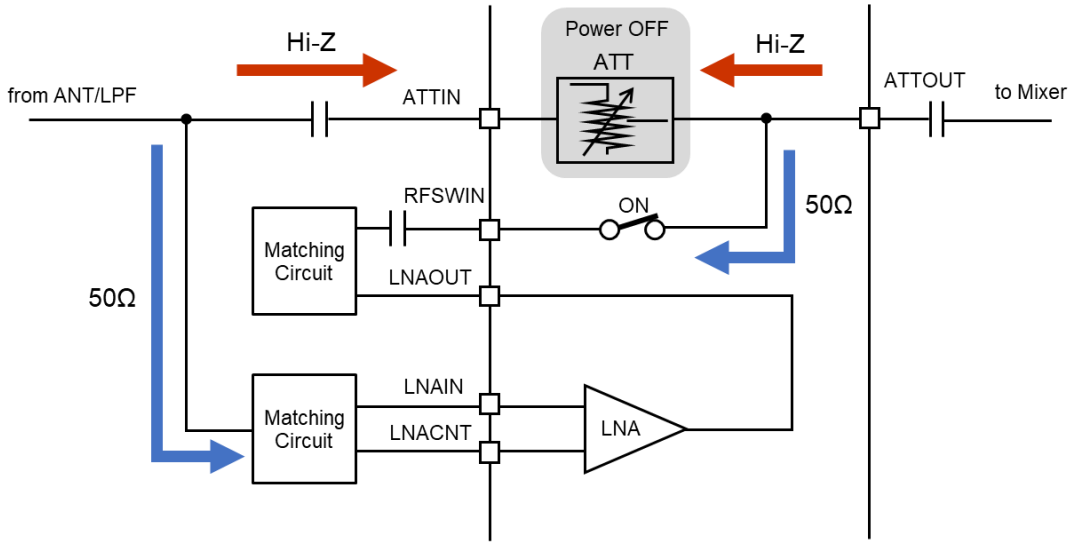


Figure 20 Impedance state when the LNA is active

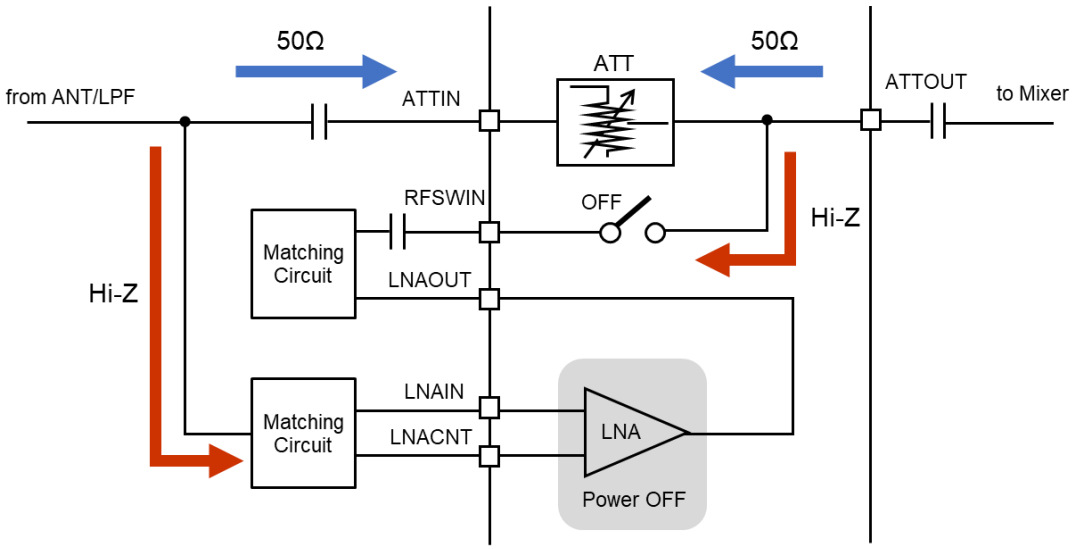


Figure 21 Impedance state when the ATT is active

■ LNA

The LNA has two operation mode of High Power Mode and Low Power Mode which have different current and analog characteristics. These modes are set by <Address0x1A>LPMODE_LNA bit. The High Power Mode improves the linearity but increases the current.

The Figure 22 shows the equivalent circuit of the input of the LNA. The C1 of the DC cut capacitor is required because the LNAIN pin is DC biased internally. The LNACONT pin is connected to the ground via source inductance LS. The C2 and LG is matching element for impedance conversion. The element value for impedance matching can be calculated by following equation and procedure if the frequency condition is different from the condition described in 15 External Circuit.

$$Z_{in} = sL_S + sL_G + \frac{1}{sC_2} + \frac{L_S g_m}{C_2} \quad (g_m: \text{transconductance of transistor}) \qquad \ldots(13.1)$$

$$\therefore \mathrm{Re} : \frac{L_S g_m}{C_2} = 50[\Omega] \qquad \ldots(13.2)$$

$$\therefore \mathrm{Im} : \omega_0 L_S + \omega_0 L_G - \frac{1}{\omega_0 C_2} = 0[\Omega] \quad (\omega_0: \text{center angular frequency}) \qquad \ldots(13.3)$$

From equation 13.2,

$$C_2 = \frac{L_S g_m}{50} \qquad \ldots(13.4)$$

From equation 13.3,

$$L_G = \frac{1}{\omega_0^2 C_2} - L_S \qquad \ldots(13.5)$$

As shown in the Figure 22, the input impedance Z_{in} can be expressed by the equation 13.1. The source inductance LS should be determined first for the impedance matching. The gain tends to decrease with increasing the LS, and increase with decreasing the LS. Refer the value described in 15 External Circuit as an initial value.
Then the value of C2 can be calculated by the equation 13.4 after determining LS. Specifically, adjust the C2 while measuring the S11 so that the real part becomes 50Ω. Finally, the value of LG can be calculated by the equation 13.5 after determining the value of LS and C2. Specifically, adjust the LG while measuring the S11 so that the imaginary part becomes 0Ω. Determine the value after thorough evaluation because of the influence by parasitic components of the elements and the board.

The g_m means the transconductance of internal transistor. When the power mode is switched by the LPMODE_LNA bit, the value of the gm at the Low Power Mode is smaller than that at the High Power Mode. Therefore, be careful that the optimal matching value is different by LNA power mode.

And as described in 7 Absolute Maximum Ratings, if the amplitude at LNA pin is larger than 2.4Vp-p, add the protection diode to limit the input amplitude. The LD is an inductance to cancel the mismatch of input matching by the parasitism of the diode. Add this inductance, if needed.

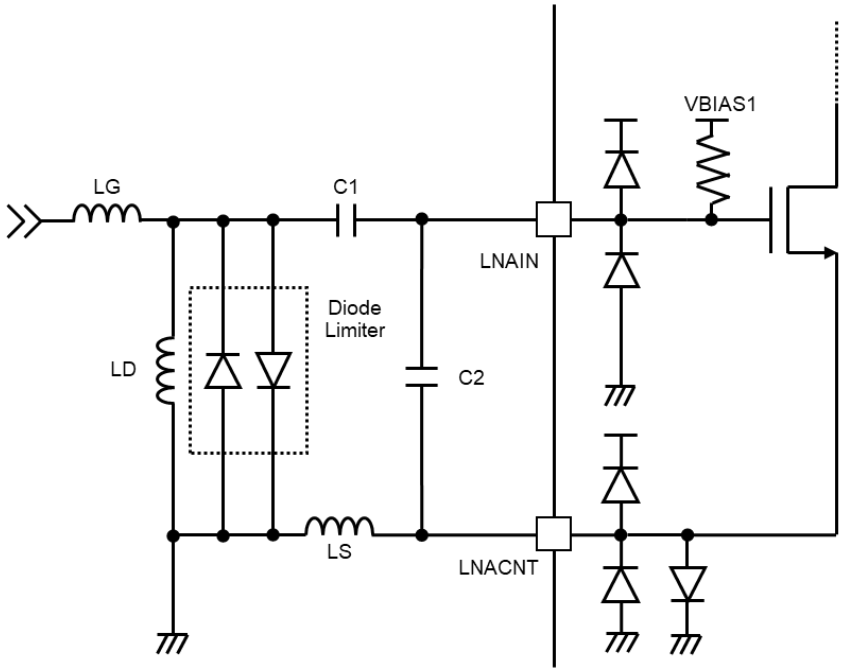


Figure 22 Equivalent Circuit for LNA Input Block

The Figure 23 shows the equivalent circuit of the LNA output. Supply the DC voltage to the LANOUT pin via an inductance L1 from the VDD1, because this pin is open-drain output. And connect load resistance RL in parallel. Though the electrical characteristic is specified under the condition of connecting the load resistance of 200Ω in standard, it is possible to change the resistance value if needed. The C4 is a capacitor for DC cut. The L1 and C4 are also used as the matching element to convert impedance. If the LNA and ATT are switched for use, execute the impedance matching by considering a selector switch between RFSWIIN pin and ATTOUT pin.

It is possible to mount the external filter between the LNA and MIXER according to the requirement for image suppression characteristic.

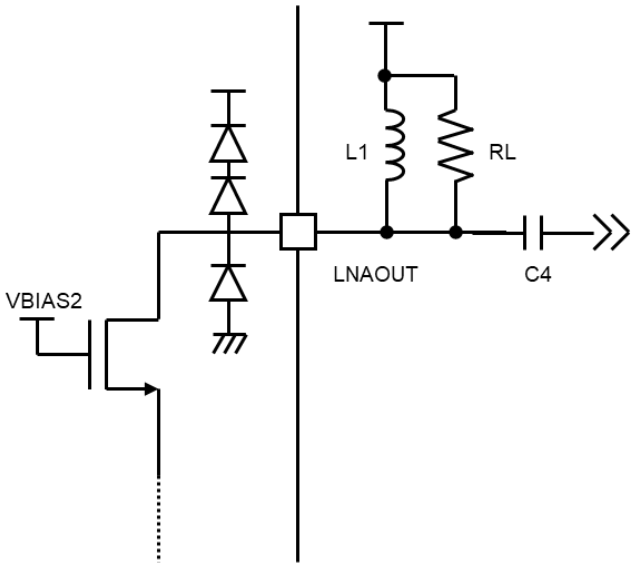


Figure 23 Equivalent Circuit for LNA Output Block

■ **ATT**

The amount of ATT attenuation is switched by <Address0x33>ATTLVL[1:0] bits in 4 steps at 6dB steps based on Insertion Loss.

■ **Switching Time (ATT -> LNA)**

When switching from the ATT to LNA by using AGC and so on, the Switching Time depends on the capacitance value of the C1 for DC cut described in 15.1 Reference Evaluation Board. The Figure 24 shows the relationship between the capacitance value of the C1 and the Switching Time. The C1 is recommended to use the capacitor of 100pF for the BAND1(450MHz) and BAND2(960MHz) specified at the analog characteristics, and the Switching Time is about 30µs in this case. On the other hand, when the frequency is getting lower, the capacitance of the C1 needs to be increased. For example, when receiving the signal of the VHF band or the specified minimum frequency of 45MHz, if the C1 is 1000pF to pass the signal, the Switching Time is about 300µs.

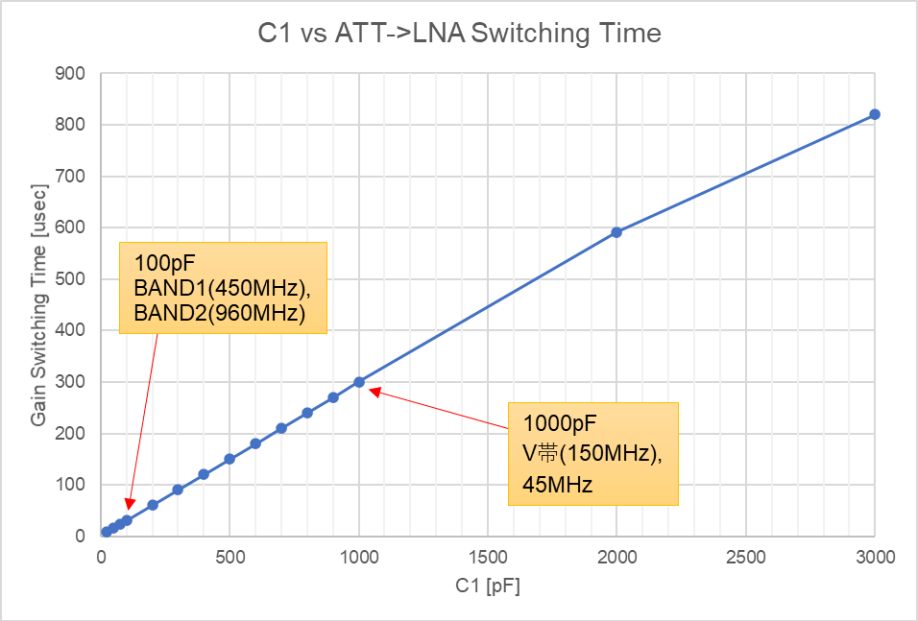


Figure 24 Relationship between the capacitance value of C1 and setup time of the LNA

13.4.2. PDET

The PDET circuit is a power detection circuit for RF signal. The Figure 25 shows the block diagram. This is ON/OFF controlled by <Address0x6F>PD_PDET_N bit.

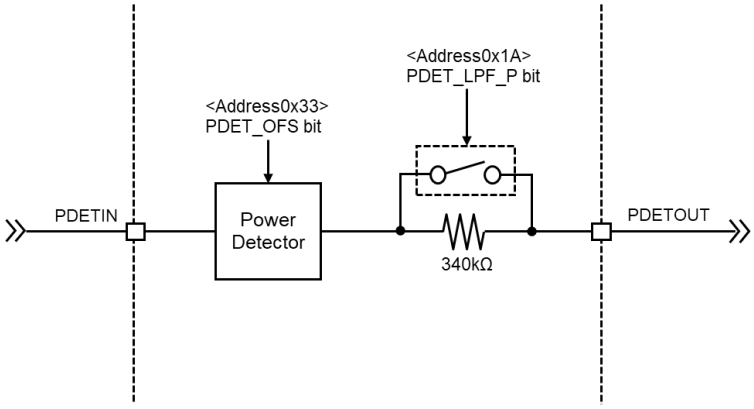


Figure 25 PDET circuit block diagram

The PDET circuit outputs a voltage from the PDETOUT pin corresponding to the input signal level on the PDETIN pin. The input impedance of the PDETIN pin is Hi-Z. The input signal level can be in the range of -23dBm to 0dBm when the capacitor described in 15.1 Reference Evaluation Board is connected in series to the PDETIN pin. And an offset voltage can be added to power detection voltage and be adjusted the output level in the range of -392mV to +448mV (4bit 56mV/step, accuracy of 1.12dB in input conversion for input level ranging from -23dBm to -5dBm). When adjusting, input -15dBm signal and set the PDET_OFS bits so that the output voltage from the PDETOUT pin becomes to 1.05V. The function to add offset voltage to increase Output Voltage is equipped. Set <Address0x74> = 01(hex) to use this function. The Output Voltage is increased by 0.4V if this function is used. The characteristics of the PDET Slope and so on do not change.

A resistor of 340kΩ is connected to the output of the Power Detector. This resistor is enabled by setting <Address0x1A>PDET_LPF_P bit = “1” and is bypassed when set to “0”. If the modulation signal with power fluctuation like π/4 DQPSK is received, compose a RC low pass filter by a capacitor connected between PDETOUT pin and VSS and this internal resistance to suppress the fluctuation.

13.4.3. MIXER

The Figure 26 shows the polarity of the quadrature demodulator. The Ich phase is designed to advance 90 degrees relative to the Qch phase.

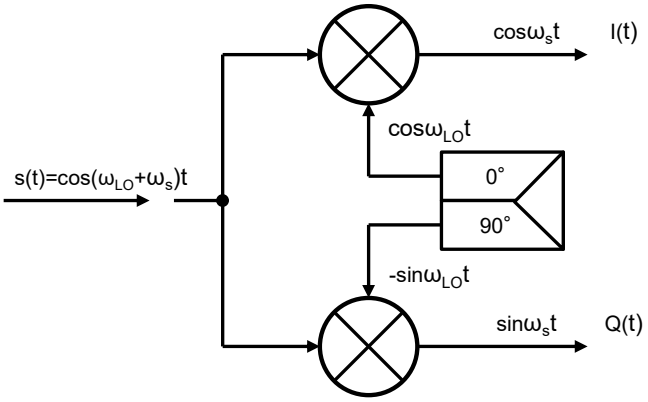


Figure 26 Polarity of Quadrature Demodulator

The Figure 27 shows the input equivalent circuit of the MIXER. The input impedance is designed to 50Ω. However, adjust the matching by LM and CM3. And convert the input signal to the differential signal by the balun and connect the CM1 and CM2 of the DC cut capacitor to the MIXINP and MIXINN pins.

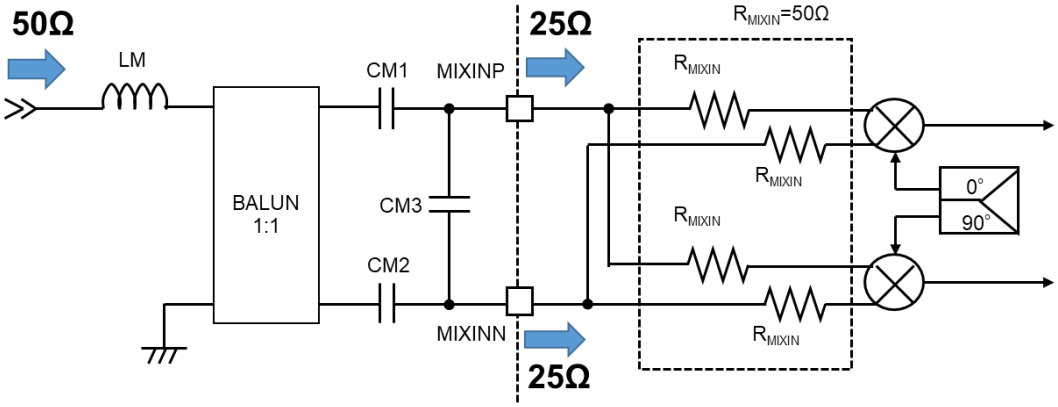
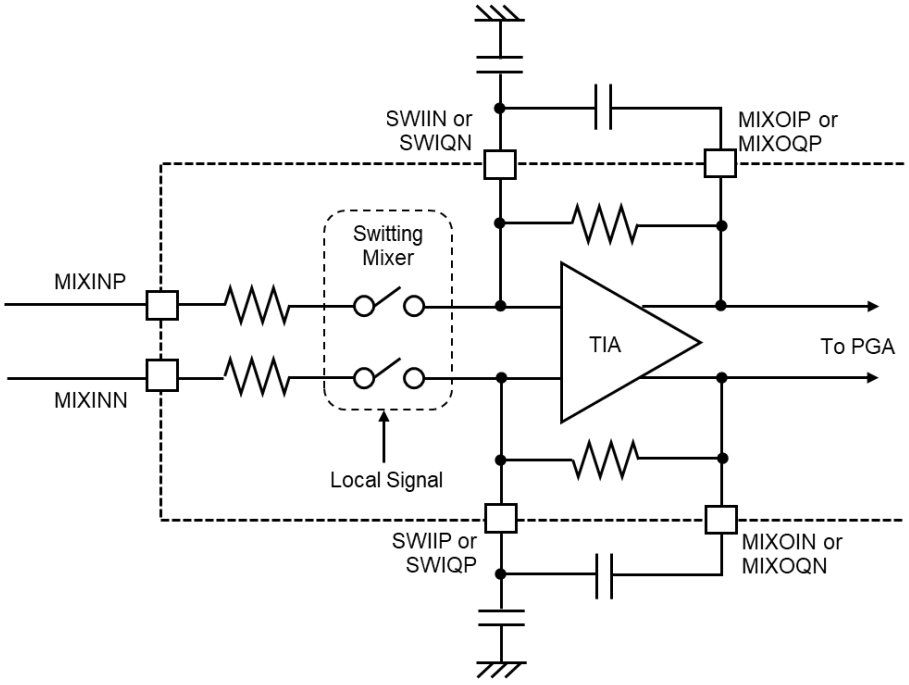


Figure 27 Equivalent Circuit for MIXER Input Block

The MIXER composes a LPF by connecting the external capacitors to the SWIIP, SWIIN, SWIQP, SWIQN, MIXOIP, MIXOIN, MIXOQP and MIXOQN pins. Connect the capacitors of the CMS1 to CMS8 described in the Table 64 on 15.1 Reference Evaluation Board. In this case, the cut off frequency is 141kHz.



※ Only Ich or Qch side is drawn in the block diagram.
Figure 28 Equivalent Circuit for MIXER LPF Block

13.4.4. PGA, AAF

The PGA and AAF consist of active filter by using the operational amplifiers. The current of the operational amplifier can be switched by <Address0x75> I_PGA bits and I_AAF bits. The linearity of each block can be improved by increasing the current.

The Figure 29 shows the frequency characteristics of the analog filter composed by the MIXER, PGA and AAF. The cutoff frequency (Fc) of the PGA can be switched by <Address0x1A> RXLPF_FC bit. When RXLPF_FC bit = “0”, the Fc is set to 45kHz and when RXLPF_FC bit = “1”, the Fc is set to 90kHz. And the Fc of the PGA shifts to a high frequency side as the gain is lower. The Fc of the AAF is 100kHz. The frequency characteristics in the Figure 29 are the result of combining MIXER, PGA (at the maximum gain) and the AAF. The gain is normalized based on 1kHz.

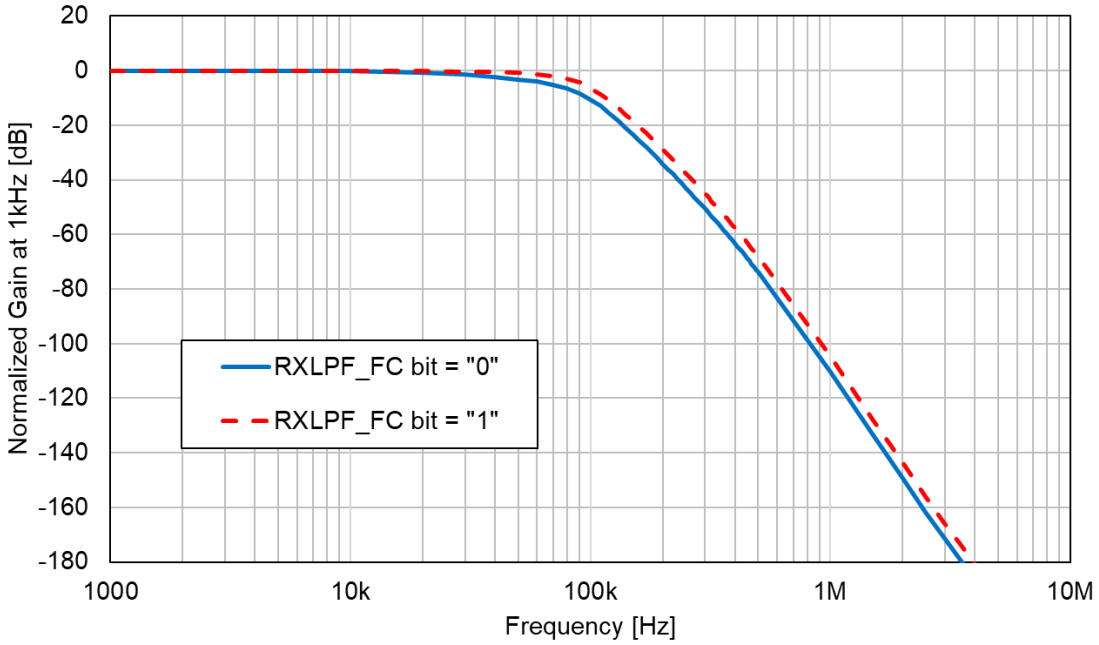


Figure 29 Analog Filter Frequency Characteristics (Maximum PGA Gain Setting)

13.4.5. Switching of the Output Path of the Analog Baseband Signal

The signal path of the AAF output can be switched by <Address0x1A>IQ_SEL, ANA_PATH, and MAIN_PATH bits. Normally, the path between AAF and ADC is connected by setting MAIN PATH bit = “1” and the paths between AAF and the AOUTP pin, and AAF and the AOUTN pin are open by setting ANA_PATH bit = “0”. In this case, the AOUTP pin and the AOUTN pin must be opened.

The receiving analog baseband signal can be taken out with differential output from the AOUTP and AOUTN pins by setting ANA_PATH bit = “1” to connect the AAF to the AOUTP and AOUTN pins. In this case, the IQ_SEL bit controls whether the Ich or Qch data is output. Connect the DC cut capacitors to the AOUTP and AOUTN lines because the AOUTP and AOUTN pins are internally DC biased. Then, measure these signals with Hi-Z.

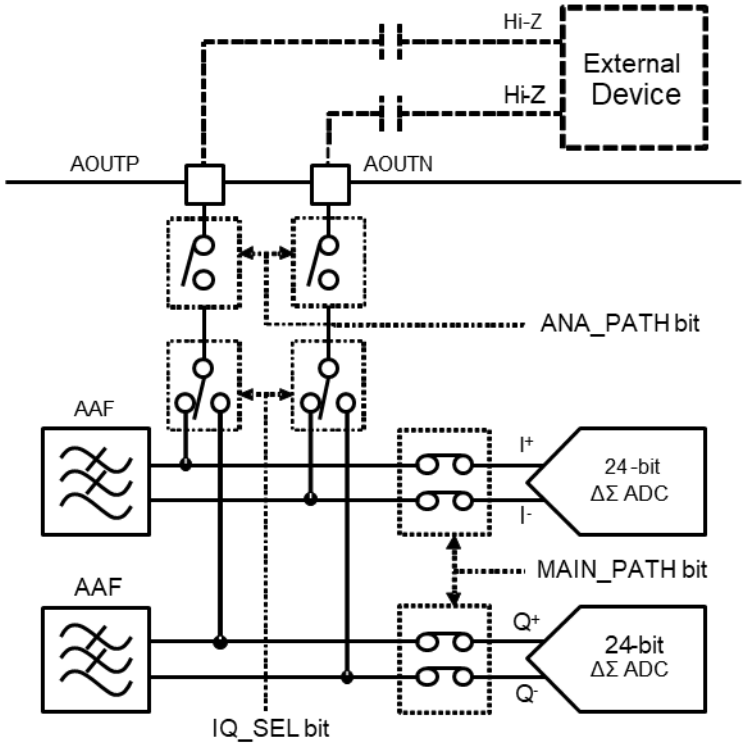


Figure 30 Output Path of the Analog Baseband Signal

13.5. LOCAL DIVIDER

13.5.1. LOCAL DIVIDER

The LOCAL DIVIDER consists of the local dividers and poly phase filter and the number of dividing is selected by <Address0x1B>DIVSEL bits. The Figure 31 shows the block diagram.

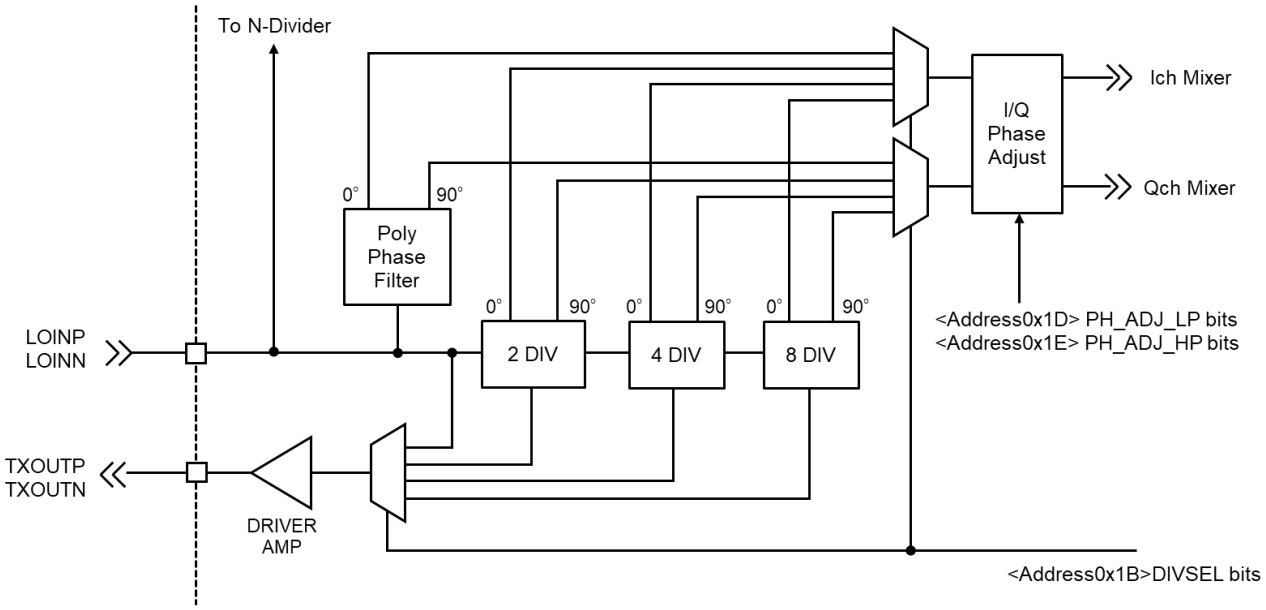


Figure 31 LOCAL DIVIDER Block Diagram

When setting the DIVSEL bits = “00”, the input frequency is used without dividing. During the receiving, the local signal input from the LOINP and LOINN pins is converted to I and Q signals with 90 degree phase difference by the poly phase filter and are input to the Mixer. Warn that the bandwidth of the poly phase filter is between 760MHz and 960MHz. During transmission, the local signal is amplified by the DRIVER AMP to the signal power set in <Address0x22>TXOLV bits and output from the TXOUTP and TXOUTN pins.

When setting the DIVSEL[1:0] bits = “01”, “10” or “11”, the local signal input from the LOINP and LOINN pins is respectively divided by 2, 4 or 8 by the local divider. In this case, during the transmission, the amplified signal is output as it is, and during the receiving, the converted to I and Q signals with 90 degree phase difference are output.

The LOCAL DIVIDER during receiving operation has two operating modes of High Power Mode and Low Power Mode that have different analog characteristics and power consumptions. And these modes are set by <Address0x1B>HPMODE_LOBLK bit. The High Power Mode set by HPMODE_LOBLK bit = “1” improves the phase noise but increases the power consumption of the LOCAL DIVDER compared with the Low Power Mode set by HPMODE_LOBLK bit = “0”.

13.5.2. Phase Calibration

The AK2404 has a calibration function that corrects orthogonal difference of 90 degrees phase shifter. Depending on the local input frequency, signal level and 2nd harmonic level, the 90 degrees phase shifter changes the orthogonality. In this case, the phase imbalance may be improved by adjusting the phase with <Address0x1D>PH_ADJ_LP[6:0] bits and <Address0x1E>PH_ADJ_HP[6:0] bits.

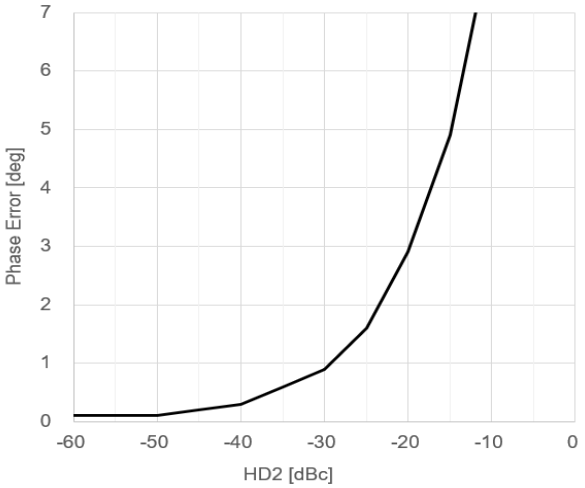
The Figure 32 shows the effect of the 2nd order harmonic of the local signal on the orthogonality. The graph (a) shows the phase imbalance versus the 2nd order harmonic of the local signal when the phase imbalance is adjusted by ideal local signal (the distortion of the local signal < -60dBc). And the graph (b)

shows the output S/N (Hum & Noise Ratio) after the FM demodulation for the phase imbalance. It is recommended to suppress the phase imbalance less than one degree because the S/N degrades when the orthogonality of the I and Q phase is not enough. The graph (c) and (d) compare the phase imbalance versus the input power of the local signal when the 2nd order harmonic of the local signal is -50dBc and -20dBc. And the graph (e) and (f) compare the phase imbalance versus input frequency of the local signal when the 2nd order harmonic of the local signal is -50dBc and -20dBc. As shown in the graphs, the variation of the phase imbalance versus various parameter becomes smaller by suppressing the 2nd order harmonic of the local signal.

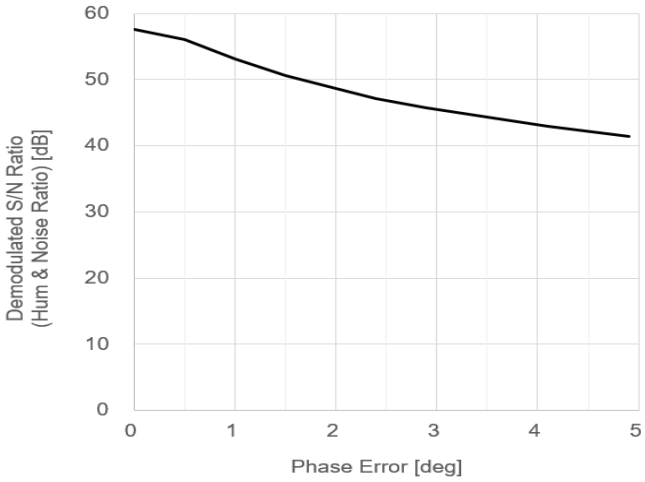
■ How to calibrate the phase

1. At first, insert a LPF between the VCO and the LOIN pin to attenuate the 2nd order harmonic. It is recommended to suppress the 2nd order harmonic to -40dBc or less.

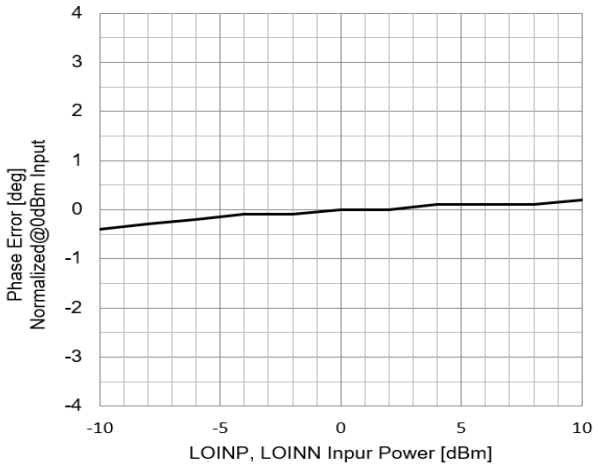
2. Set the LOIN input level and LOIN input frequency to the used conditions and determine the calibration value. One way to measure the phase imbalance is to set the CW output state. Measure the phase difference between I and Q output when the CW signal of LO+1kHz is input as RF signal, and determine the calibration value that is closed to 90 degree.



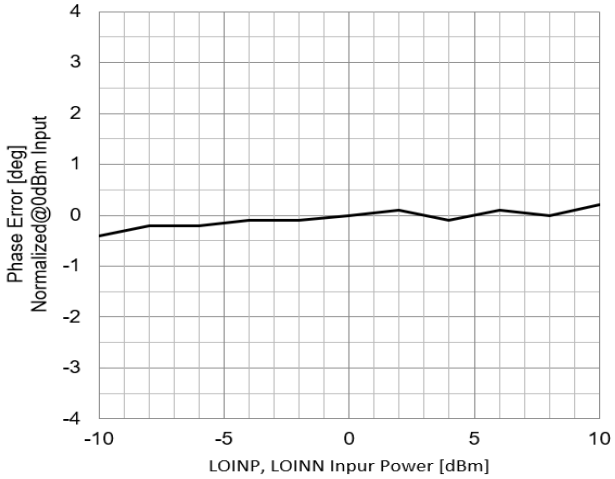
(a) LOIN=900MHz, 0dBm



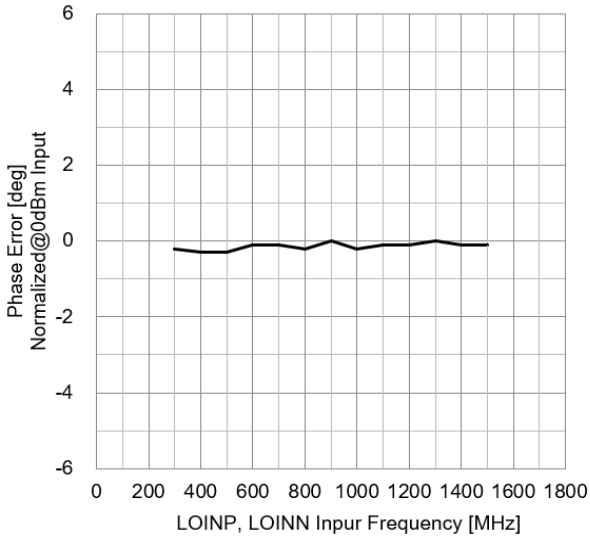
(b) LOIN=900MHz, 0dBm



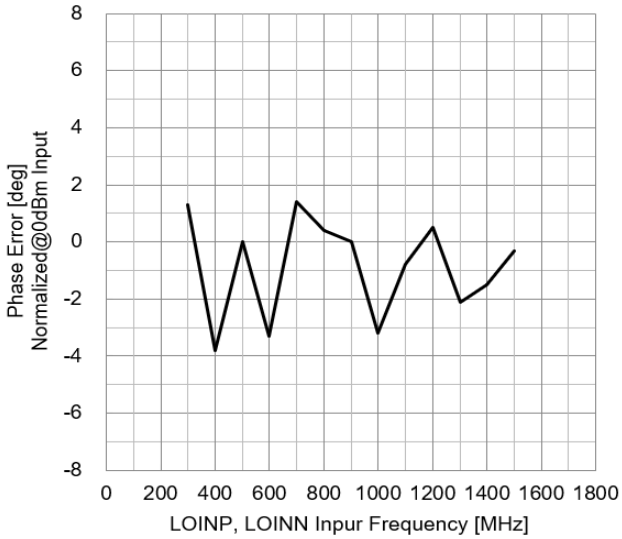
(c) LOIN=900MHz, HD2=-50dBc



(d) LOIN=900MHz, HD2=-20dBc



(e) LOIN=0dBm, HD2=-50dBc



(f) LOIN=0dBm, HD2=-20dBc

Figure 32 The I/Q phase orthogonality and measurement example of various parameters
(LO is divided by 2)

13.6. CLOCK BUFFER+CLOCK RATE CONVERTER

The block diagram of the CLOCK BUFFER and CLOCK RATE CONVERTER is shown in the Figure 33. Input the clipped sine wave to the TCXOIN pin via the DC cut capacitor by AC coupling. Refer to 10.1.8 CLOCK BUFFER+CLOCK RATE CONVERTER about the specification of the clipped sine wave. The TCXO is assumed as the input source. Warn that it is not designed to assume the clock like generated by an MCU.

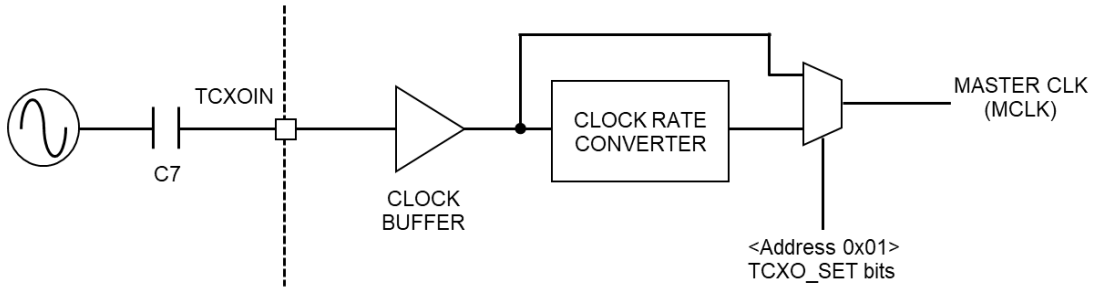


Figure 33 CLOCK BUFFER and CLOCK RATE CONVERTER Block Diagram

The CLOCK RATE CONVERTER converts the input frequency of the TCXOIN pin and the converted signal is used for the internal master clock (MCLK). Unless otherwise specified, the digital circuit in the AK2404 operates at the frequency of the master clock (f_{MCLK}). Note that it is not the TCXO frequency (f_{TCXO}). If the CLOCK RATE CONVERTER is not used, $f_{TCXO} = f_{MCLK}$.

The CLOCK RATE COVERTER executes the frequency conversion by multiplying the TCXOIN frequency and then dividing it. The Table 8 shows the converted frequency by the CLOCK RATE CONVERTER and the output frequency of the multiplier. Set <Address0x01>TCXO_SET bits according to the used TCXO frequency. The CLOCK RATE CONVERTER is turned off at the setting of TCXO_SET bits =0, 3(dec) because the TCXO input frequency is used as it is. Note that the spurious characteristics may be degraded by the frequency component which occurs during multiplication if the CLOCK RATE CONVERTER is used by the setting except of TCXO_SET bits = 0, 3(dec).

When using frequencies other than 3 types of 18.432MHz, 19.2MHz, 24.576MHz for TCXOIN, select the frequency which is closer to TCXO_SET bits = 0 or 3(dec) due to the effect of the operation of the digital circuit in the later stage. Note that the normal operation is not guaranteed if any other conversion table is selected (when the CLOCK RATE CONVERTER operates).

Table 8 CLOCK RATE CONVERTER Table

TCXO_ SET[2:0]	TCXOIN Input Frequency [MHz]	CLOCK RATE CONVERTER Output Frequency. [MHz]	Multiplier Output Frequency [MHz]
0	24.576	24.576	-
1	24.576	18.432	368.64
2	24.576	18.432	663.552
3	18.432	18.432	-
4	18.432	24.576	368.64
5	18.432	24.576	442.368
6	19.2	18.432	460.8
7	19.2	24.576	614.4

13.7. PLL SYNTHESIZER

The AK2404 has a ΔΣ fractional-N PLL synthesizer. The PLL synthesizer integrates a ΔΣ modulator, a divider for reference clock, a phase frequency detector, a charge pump and an N-divider, composing a PLL with an external loop filter and VCO.

The charge pump has two types of current, the normal type (<Address0x14>CPFINE[4:0] bits) and the fast lock type (<Address0x15>CPFAST[4:0] bits) which can be set in 32 steps. The PLL can achieve the fast lock by switching two types of charge pump current set by an internal timer. The PLL has a switch to switch the loop filter constant which is switched by the internal timer. The charge pump current can be calculated by the equation below set by the value of 5-bit of the CPFINE[4:0] and CPFAST[4:0] bits and the resistance connected to the BIAS2 pin. The sample configuration is shown in the Table 9. Connect a resistor of 27kΩ to the BIAS2 pin.

Charge Pump Current [μA] = I_{CP_MIN} × (Setting Value + 1)
I_{CP_MIN} [μA] = 2160 / Resistor Connected to the BIAS2 pin [kΩ]

Table 9 Charge Pump Current

CPFAST CPFINE decimal	CP current [μA] at BIAS2 pin=27kΩ
0	80
1	160
2	240
3	320
. . .	. . .
28	2320
29	2400
30	2480
31	2560

And the output state of the charge pump at power-down can be set from 3 types of Hi-Z, “H” and “L” by <Address0x16>CPO_PDST bits.

The Figure 34 shows an example of the charge pump configuration and an external loop filter configuration. The loop filter must be connected to three pins of CP, SWIN and CPZ. The CPZ pin must be connected to the intermediate node between the RS2 resistor and the CS2 capacitor even if the fast lock function is not used. In this case, the RS2 resistor should be connected to the CP pin and the CS2 capacitor should be connected to the ground.
During the fast lock operation, the RS2 and RS’2 resistors are connected in parallel internally by the internal switch. Calculate the loop bandwidth and phase margin at the fast lock using the parallel resistance values of the RS2 and RS’2 resistors. The ON resistance of the internal switch is about 150Ω.

Due to the circuit configuration of the charge pump in the AK2404, the lock up time tends to be shorter when the loop filter voltage is increased compared to when it is decreased (it turns to be opposite when <Address0x14 CP_POLA bit = “1” is set). During fast lock operation, the same operation is performed in the up direction and down direction, so set the timer time of the fast lock function appropriately.

Since the AK 2404 is primarily intended for use in narrow band applications, the constants on the 15.1 Reference Evaluation Board are designed to have a loop bandwidth of approximately 1 kHz to reduce phase noise on adjacent channels approximately 12.5 kHz away. A third order loop filter is used in order to suppress fractional noise which becomes larger more than 1MHz offset.

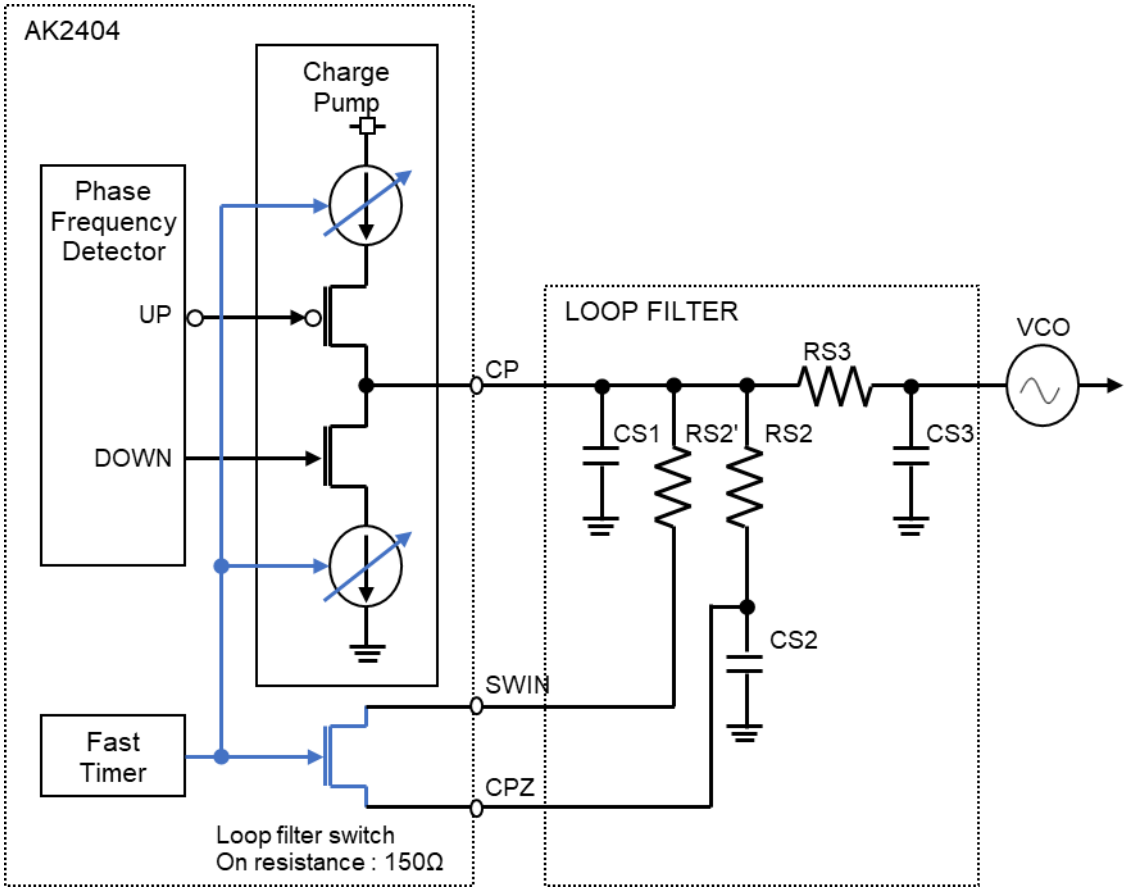


Figure 34 Example of the Charge Pump Configuration and External filter

13.7.1. Frequency Setting

The setting frequency f_{VCO} of PLL SYNTHESIZER is calculated by the following equation.

$$f_{VCO}=f_{PFD} \times \left(\mathrm{INT}+\frac{\mathrm{FRAC}}{\mathrm{MOD}}+\frac{\mathrm{DEN\_RATIO} \times (\mathrm{OFS\_FINE} + \mathrm{OFS\_MDLT} + pol \times \mathrm{OFS\_RDOC})}{\mathrm{OFS\_DEN}}\right) \quad \text{(Eq. 13.1)}$$

f_{PFD} : PFD input frequency (Phase Detector Frequency)
INT : Integer Portion of Dividing Value
Set the range of 28 ≤ INT ≤ 1920(dec) (unsigned, 11bit)
FRAC : Numerator for Fractional Portion of Dividing Value
Set the range of 0 ≤ FRAC < MOD(dec) (unsigned, 23bit)
MOD : Denominator for Fractional Portion of Dividing Value
Set the range of 2 ≤ MOD ≤ 8388607(dec) (unsigned, 23bit)
DEN_RATIO : Step ratio of Frequency Offset Value to correct LO DIVIDER frequency division (1, 2, 4 or 8)
OFS_FINE : Numerator for Frequency Offset Value to be used for the AFC and so on.
Set the range of -32768 (8000(hex)) to +32767 (7FFF(hex)) (signed, 16bit)
OFS_MDLT : Numerator for Frequency Offset Value to be used for the modulation data of Lch input from the MOD I/F
Set the range of -32768 (8000(hex)) to +32767 (7FFF(hex)) (signed, 16bit)
Valid only when <Address0x21>MOD_ENABLE[1] bit = “1”
Refer to 13.7.5 Frequency Offset Adjustment and Modulation function about the relationship between the OFST_MDLT and modulation function.
OFS_RDOC : Numerator for Frequency Offset Value to be used for the RDOC function
Set the range of -32768 (8000(hex)) to +32767 (7FFF(hex)) (signed, 16bit)
Valid only when <Address0x68>RDOC_FM bit = “1”
Refer to 13.8.9 RDOC Function about the relationship between the OFS_RDOC and RDOC.
OFS_DEN : Denominator for Frequency Offset Value
1 or more, and set within the formula to be described later (unsigned, 23bit).
pol : The coefficient that sets the polarity of OFS_RDOC, set by the RDOC function.
+1 or -1

The following settings are valid only when FRAC > 0 or <Address0x12>DSM_AT_INT bit = “1” where the ΔΣ modulator is valid.

$$\frac{\mathrm{FRAC}}{\mathrm{MOD}}+\frac{\mathrm{DEN\_RATIO} \times (\mathrm{OFS\_FINE} + \mathrm{OFS\_MDLT} + pol \times \mathrm{OFS\_RDOC})}{\mathrm{OFS\_DEN}}$$

The frequency offset value range has the following restrictions due to the restriction of the ΔΣ modulator.

$$\left|\frac{\mathrm{DEN\_RATIO} \times (\mathrm{OFS\_FINE} + \mathrm{OFS\_MDLT} + pol \times \mathrm{OFS\_RDOC})}{\mathrm{OFS\_DEN}}\right| < 0.5$$

An example of frequency setting is shown below. For example, to achieve f_{VCO} = 910.0375MHz and frequency resolution (ch pitch) = 125Hz at f_{PFD} = 24.576MHz, set as follows.

INT = floor(f_{VCO} / f_{PFD}) (* The “floor” means truncate.)
= floor(910.0375 / 24.576)
= 37

MOD = f_{PFD}/(ch pitch)
= 24,576,000 / 125
= 196608

FRAC = ((fvco / fPFD) – INT) × MOD
= ((910.0375 / 24.576) – 37) × 196608
= 5804

f_{VCO} = 24.576 × (37 + (5804 / 196608) + (0 / 8388607))
= 910.0375… [MHz]

13.7.2. Re-lockup Event

When the following events occur, the formula of the frequency calculation is recalculated and ΔΣ modulator is reset.

- When <Address0x6E>PD_PLL_N bit is set to “1” from “0”.
- When <Address0x11>INT[7:0] bits is set with PD_PLL_N bit = “1”.

Setting INT[7:0] bits before canceling power down (when PD_PLL_N bit = “0” is set) is not considered the event. Setting the registers related to the PLL synthesizer (<Address0x01 to 0x18>) must be finished before the re-lockup event. If re-lockup event is generated by writing the <Address0x11>INT[7:0] bits, write the <Address0x11> after setting the above PLL synthesizer related registers except the <Address 0x11>.

The fast lock operation described in 13.7.3 Fast Lock Function starts after the reset of ΔΣ modulator is completed, if the <Address0x16>FASTEN bit = “1” is set. And it is prohibited to update the frequency (generating a new re-lockup event) from the generation of the re-lockup event until the completion of the ΔΣ modulator reset and fast lock operation. It takes time of (30 to 31) × t_{DIVCLK} from the generation of the re-lockup event until the reset of ΔΣ modulator. ($t_{DIVCLK} \cong 1 / f_{PFD}$)

13.7.3. Fast Lock Function

The AK2404 has a fast lock function to realize fast PLL lock-up. Setting FASTEN bit="1" enables the fast lock function. The fast lock timer starts when a re-lockup event occurs as described in 13.7.2 Re-lockup Event.

By the fast lock function, the loop filter switch is turned on during the timer period set by the <Address0x13>FAST_TIME[7:0] bits and the charge pump current for the fast lock set by the CPFAST[4:0] bits becomes active. After the timer period is completed, the loop filter switch is turned off and the normal charge pump current set by the CPFINE[4:0] bits becomes active and it returns normal state. The timing chart of the fast lock function is shown in the Figure 35. The following formula is used to calculate the period of fast lock function. The Table 10 shows the example of the setting.

Timer Period = (1 / f_{PFD}) × (1023 + 1024 × FAST_TIME[7:0] bits)

Table 10 Fast Lock-up Period

FAST_TIME decimal	Duration [µs] at f_{PFD}=24.576MHz	Duration [µs] at f_{PFD}=18.432MHz
0	42	56
1	83	111
2	125	167
3	167	222
4	208	278
5	250	333
. . .	. . .	. . .
251	10,500	14,000
252	10,542	14,056
253	10,583	14,111
254	10,625	14,167
255	10,667	14,222

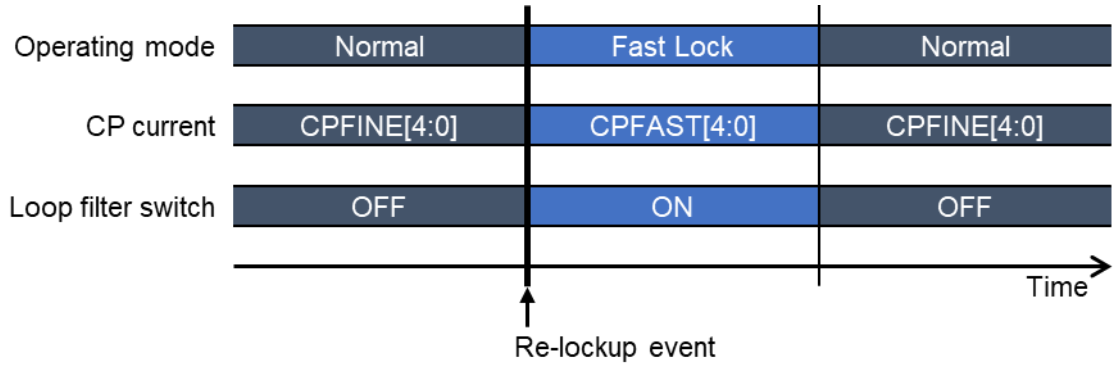


Figure 35 Fast Lock Function Sequence

13.7.4. Lock Detection

The AK2404 has a lock detection function to detect the lock or unlock state of the PLL. The lock detection function detects the phase error at the PFD output and outputs the lock detection signal from the LD pin according to the internal logic. The lock detection circuit outputs “H” during the PLL is locked state and outputs “L” during the PLL is unlocked state. And it is unlocked state (“L”) during the PLL is power down by setting the PD_PLL_N bit = “0”. When the LDSEL[1:0] bits = “11" is set, the LD pin outputs “H” regardless of PLL lock/unlock. The detection count N, which corresponds to the sensitivity setting of the lock detect circuit described later, can be set in the register. The detection count from the unlock state to the lock detection can be set by the <Address0x17>LD_LOCKCNT[7:0] bits, and the detection count from the lock state to the unlock detection can be set by the <Address0x18> LD_UNLOCKCNT[7:0] bits. All “0 ” is prohibited for both LD_LOCKCNT bits and LD_UNLOCKCNT bits. The Reference Clock in the following description is the master clock frequency (f_{MCLK}) described in 13.6 CLOCK BUFFER+CLOCK RATE CONVERTER. It indicates the TCXO frequency when the CLOCK RATE CONVERTER is not used and the CLOCK RATE COVERTER output frequency when the CLOCK RATE CONVERTER is used.

The internal logic differs according to the set value of <Address0x16>LD_MODE bit and <Address0x09>PLL_R bits, and it is as follows.

■PLL_R=1

The LD pin becomes “H” (lock) if the phase error is detected N times consecutively below the half clock ($T_{MCLK}/2$) of the master clock. In this state, the LD pin becomes “L” (unlock) if the phase error of $T_{MCLK}/2$ or more is detected N times consecutively. That means that the maximum phase error $phase_{max}$ at lock is $T_{MCLK}/2$. The Figure 36 shows the timing of the lock detection signal.

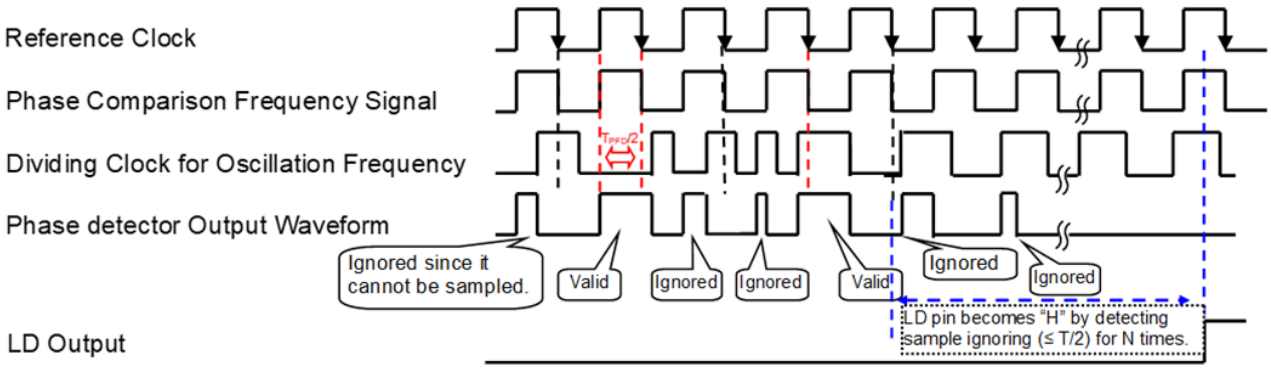


Figure 36 Lock Detection Circuit Timing (PLL_R=1)

■PLL_R=2

The LD pin becomes “H” (lock) if the phase error is detected N times consecutively below one clock (T_{MCLK}) of the master clock. In this state, the LD pin becomes “L” (unlock) if the phase error of T_{MCLK} or more is detected N times consecutively. That means that the maximum phase error $phase_{max}$ at lock is T_{MCLK}. The Figure 37 shows the timing of the lock detection signal.

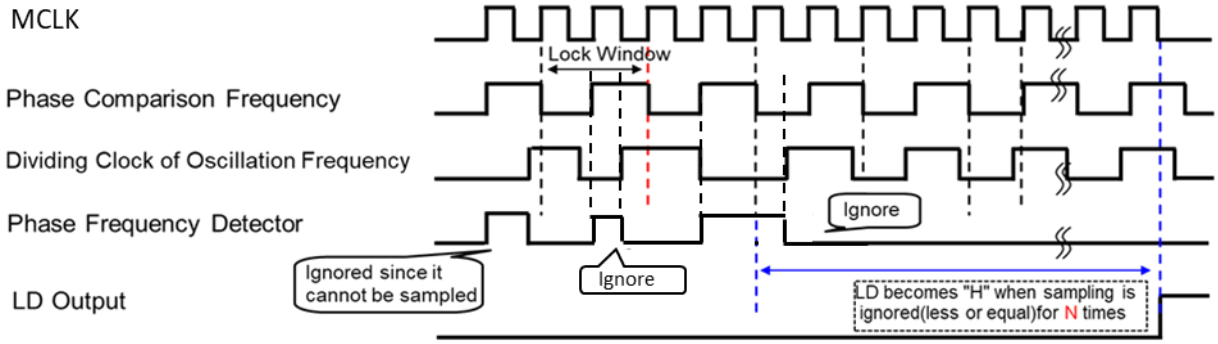


Figure 37 Lock Detection Circuit Timing (PLL_R=2)

■LD_MODE=0, PLL_R≥3

The LD pin becomes “H” (lock) if the phase error is detected N times consecutively below one clock (T_{MCLK}) of the master clock. In this state, the LD pin becomes “L” (unlock) if the phase error of T_{MCLK} or more is detected N times consecutively. That means that the maximum phase error $phase_{max}$ at lock is T_{MCLK}. The Figure 38 shows the timing of the lock detection signal. The minimum frequency of the LOINP and LOINN pins capable to use under the condition of LD_MODE=0 depends on the frequency of the master clock. And there is a restriction below about the LOIN input frequency period T_{LO} and master clock period T_{MCLK}.

$$T_{MCLK} > T_{LO} \times 11$$

Converted to frequency, it is as follows.

$$f_{LO} > f_{MCLK} \times 11$$

Note that the lock detection function does not operate normally if a signal less than the minimum input frequency is input. When the lower frequency is input to the LOINP and LOINN pins, lock detection function can be used by setting LD_MODE=1.

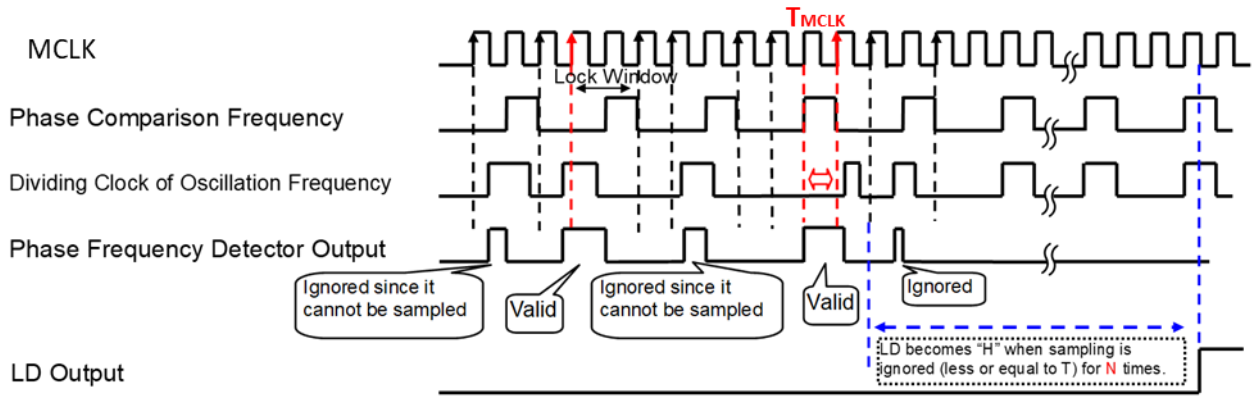


Figure 38 Lock Detection Circuit Timing (LD_MODE=0, PLL_R≥3)

■LD_MODE=1, PLL_R≥5

The LD pin becomes "H" (lock) if the phase error is detected N times consecutively below three clocks ($3\times T_{MCLK}$) of the master clock. In this state, the LD pin becomes "L" (unlock) if the phase error of $3\times T_{MCLK}$ or more is detected N times consecutively. That means that the maximum phase error $phase_{max}$ at lock is $3\times T_{MCLK}$. The Figure 39 shows the timing of the lock detection signal. When using with LD_MODE=1, note that the lock detection function does not operate normally when PLL_R= 3 to 4 is set.

As shown in the Figure 39, the lock window of $T_{MULT}\times 5$ width is generated based on the rising edge of the output from the phase comparator. And it detects whether the rising edge of the clock which is generated by dividing the frequency of the VCO is in the lock window or not.

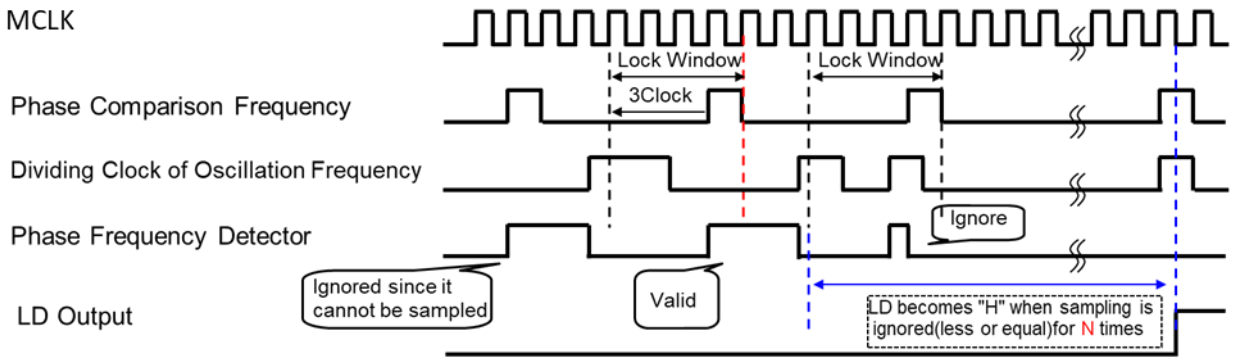


Figure 39 Lock Detection Circuit Timing (LD_MODE=1, PLL_R≥5)

13.7.5. Frequency Offset Adjustment and Modulation function

The PLL SYNTHESIZER has the functions to adjust the frequency offset and to perform the frequency modulation. Use the frequency offset value set by the OFS_DEN item in the frequency setting formula shown in (13.1). The equation (13.9) shows the VCO frequency deviation Δf_{VCO} set by the frequency offset value. Set <Address0x12> DSM_AT_INT bit to “1” when using this function.

$$\Delta f_{VCO} = f_{PFD} \times \left(\frac{\text{DEN\_RATIO} \times (\text{OFS\_FINE} + \text{OFS\_MDLT} + pol \times \text{OFS\_RDOC})}{\text{OFS\_DEN}} \right) \quad \ldots (13.9)$$

The Figure 40 shows the circuit configuration of the frequency offset adjustment and modulation function.

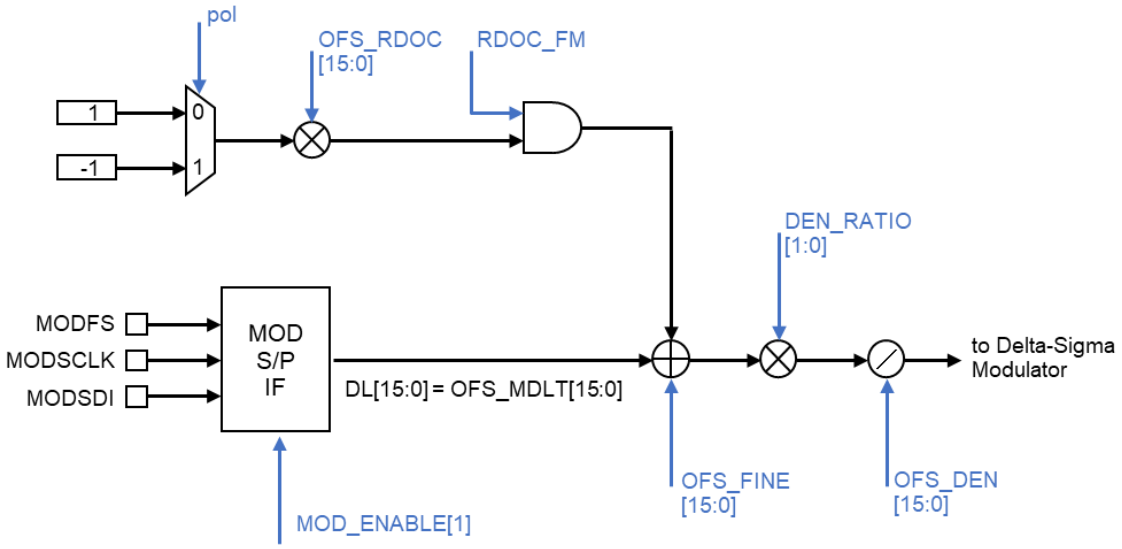


Figure 40 Frequency Offset and Modulation Configuration

The frequency offset value can be input by the three types listed in the Table 11.

Table 11 Frequency Offset and Modulation Parameter

Signal	Access	Main purpose
OFS_MDLT[15:0]	MOD I/F	FM/FSK modulation
OFS_FINE[15:0]	Register I/F <Address0x04 to 05>	Auto Frequency Control
OFS_RDOC[15:0]	Register I/F <Address0x02 to 03>	RDOC

When the MOD I/F is used, set <Address0x21> MOD_ENABLE[1] bit to “1”.
When the MOD_ENABLE[1] bit is set to “0”, the previous input data is kept.
When the value of the MOD_ENABLE[1] bit is changed, stop the access to the MOD I/F. (Fix MODSCLK to "L".)

The modulation signal is calculated by the following procedure.

1. Add OFS_MDLT and OFS_FINE
2. Add OFS_RDOC when <Address0x65>RDOC_FM bit = “1”
3. Multiply the set value of <Address0x01>DEN_RATIO bits
4. Divides by <Address0x06 to 08>OFS_DEN bits and adds it to the frequency set value

The modulated signal is recalculated when the re-calculation event defined below occurs.

- When re-lockup event occurs (Refer to chapter 13.7.2.)
- When MOD I/F data is fixed (Refer to chapter 9.6.)
- When writing to <Address0x05>OFS_FINE[7:0] bits
- When writing to <Address0x03>OFS_RDOC[7:0] bits
- When writing to <Address0x08>OFS_DEN[7:0] bits
- When writing to <Address0x21>MOD_ENABLE[1] bit
- When writing to <Address0x65>RDOC_FM bit
- When the *pol* polarity is changed

Reconfiguration of the modulated signal (generation of a new recalculation event) is prohibited from the occurrence of the recalculation event until the recalculation of the modulated signal is completed. It takes time of (30 to 31) × t_{DIVCLK} to recalculate the modulation signal. ($t_{DIVCLK} \cong 1 / f_{PFD}$)
And it takes time of (34 to 35) × t_{DIVCLK} from the time when the data is fixed in the MOD I/F until it is reflected in the frequency setting.

13.8. Digital Receiving Circuits (ADC, DIGITAL FILTER, RSSI, AGC, ADC P/S IF)

The block diagram of digital receiving circuit is shown in the Figure 41. The AK2404 is basically used in LOW_IF. The analog baseband signal generated in the analog receiving circuit is converted to the digital data oversampled by 64 times (at data rate=MCLK/256) by a 24-bit ΔΣ ADC. Then, the data is decimated with decreasing the ΔΣ noise and the data is input to the channel filter to remove the interfere wave after converted to the ZERO_IF data by a complex mixer. And it is possible to adjust the gain for the purpose to compensate the IQ gain mismatch during the frequency conversion. The signal level after passing the channel filter is stored to registers by the RSSI function. It can be confirmed by readback of the register by the SPI or confirmed by the serial output of the status bit. The desired signal is output from the parallel-serial interface of the ADC as the digital baseband signal. At that time, it is possible to up-convert to the LOW_IF data by the complex mixer at the later stage and output the data. The output sampling rate depends on the configuration of the selected digital filter.

The DC offset cancellation can be executed by the PRE_HPF when the LOW_IF is used. Because the NCO frequency component (Δ1) is output on the output of the complex mixer when the DC offset is not removed, it is necessary to remove it by the channel filter. It is not recommended to use the POST HPF or RDOC.

When the ZERO_IF is used, select either the POST_HPF or RDOC for the desired wave to cancel the DC offset superimposed on the baseband signal. When receiving the signal of the modulation type like the QPSK and QAM which amplitude is varied, the RDOC is not effective. Use the POST_HPF to remove the DC offset when receiving such signals.

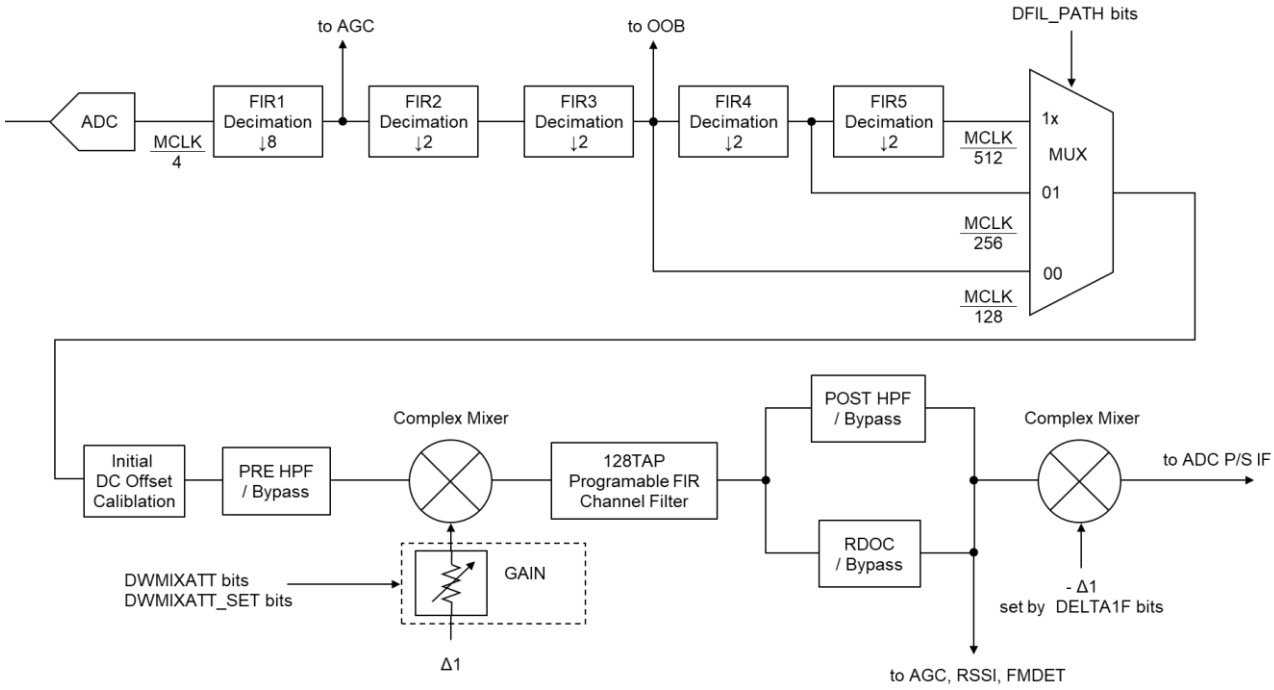


Figure 41 Digital Receiving Block Diagram

13.8.1. ADC

The ADC is a 24-bit ΔΣ ADC. The master clock (MCLK) which is converted from the reference clock input from the TCXOIN pin by the CLOCK RATE CONVERTER is divided by four to be used for the operating clock of the ADC.

The full scale is specified by ADVDD ×1.7 [Vp-p_dif] and the 0dBFS of the level diagram is +18.1dBm (when ADVDD = 3.0V) when it is considered by 50Ω conversion.

13.8.2. Complex Mixer

The AK2404 has the complex mixers. The complex mixers are located at former and later of the channel filter and execute frequency conversion by multiplying the local signal generated by the NCO by Ich or Qch data. The complex mixer at the former stage is used to down-convert the LOW_IF signal to the ZERO_IF signal. And the complex mixer at the later stage is used to up-convert the ZERO_IF signal to the LOW_IF signal. The complex mixer suppresses the image signal superimposed on the desired wave at the down and up conversion. It is possible to by-pass each mixer by setting <Address0x45>DWMIX_OFF bit = “1” or UPMIX_OFF bit = “1”.

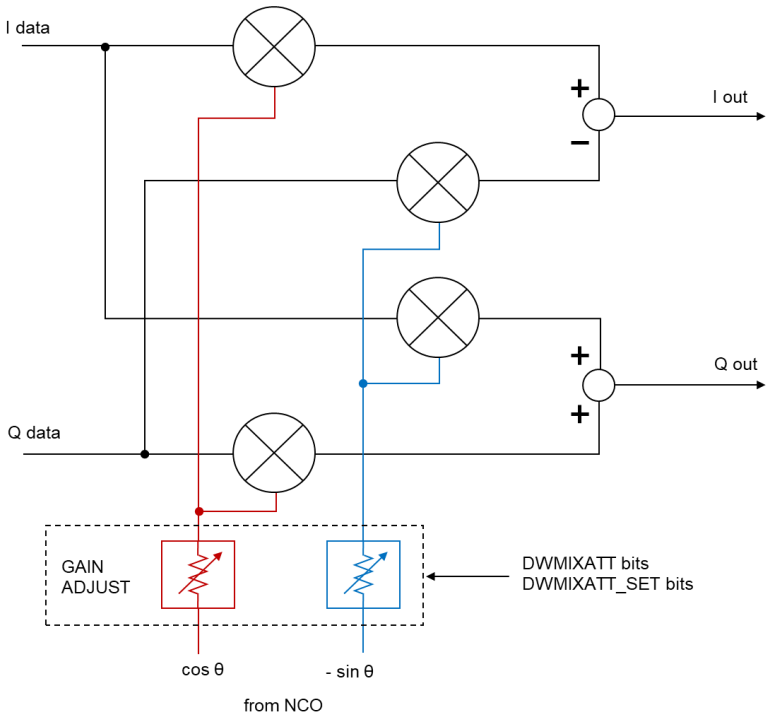


Figure 42 Complex Mixer (Down Convert)

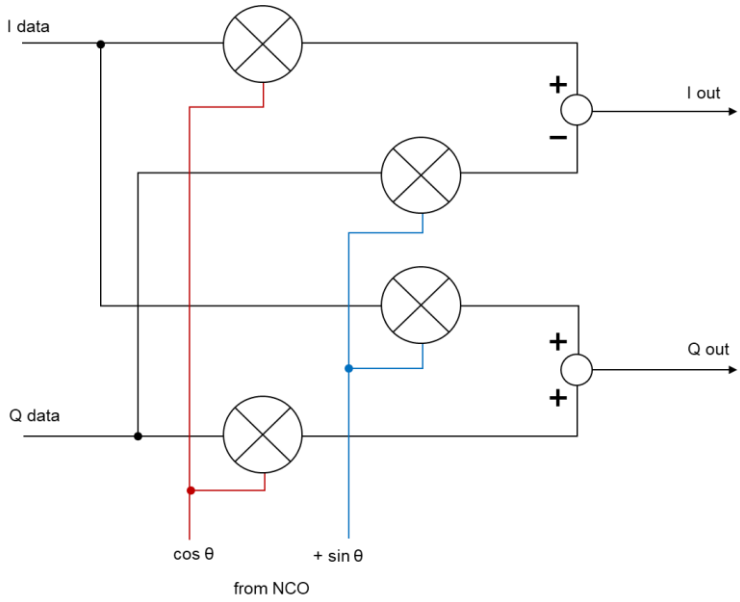


Figure 43 Complex Mixer (UP Convert)

■Gain Adjusting Function

The complex mixer before the channel filter has a function to adjust a gain to correct the gain error of the I/Q signal. The gain adjustment is executed by attenuating the amplitude of local signal of either Ich or Qch. The attenuation is calculated by the equation below according to the setting of <Address0x47 to 0x48>DWMIXATT[13:0] bits. The Figure 44 shows a graph of the attenuation versus the set value of the DWMIXATT bits.

$$Attenuation\ Level = 20 \times \log\left(\frac{1}{2^{14}} \times DWMIXATT\ bits\right)\ [dB]$$

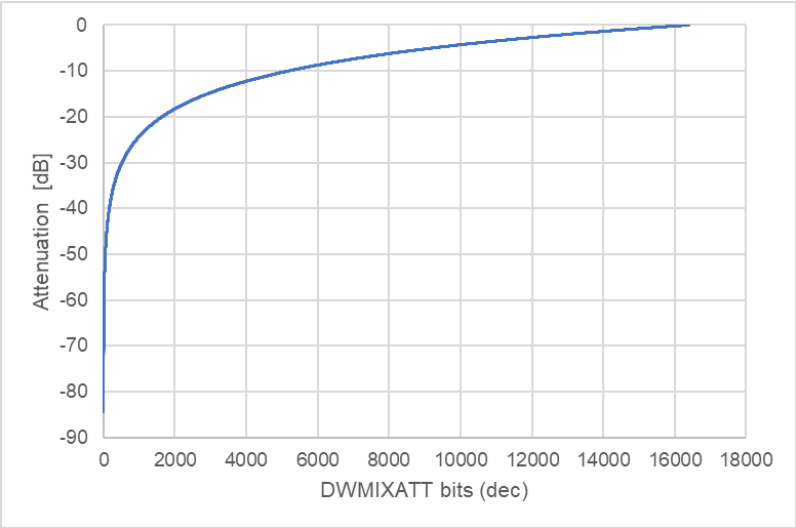


Figure 44 Gain Adjustment versus DWMIXATT bits

The gain adjustment function is controlled by <Address0x48>DWMIXATT_SEL bits. The gain of Ich is attenuated by setting DWMIXATT_SET bits = “01” and the gain of Qch DWMIXATT_SET bits = “10”. If the value of “00” or “11” is set, the gain adjustment function is turned off.

13.8.3. Out of Band Power Monitoring Function

The AK2404 has a function to detect the power of out of band and can detect the interference wave at the higher side (Rside) and the lower side (Lside) of the desired wave. The Figure 45 shows the block diagram. The signal from the FIR3 is frequency converted by a complex mixer after being removed the DC offset by an initial DC Offset Calibration circuit. The local frequency of the complex mixer is calculated from a frequency Δ1 set by <Address0x43>DELTA1F bits and Δ2 set by <Address0x44>DELTA2F bits. Then, the noise in the higher frequency region is suppressed by a programmable third order IIR filter (LPF) and the signal is output by 8-bit digital data after being detected the signal power by a RSSI circuit (chapter 13.8.15). The detected power can be read back by <ROpage Address0x07>R_OOBL_RSSI bits and <ROpage Address0x08> R_OOBR_RSSI bits. And the difference between the desired wave and RSSI value can be output as a status signal by setting <Address0x3E>STS_RSSI_SEL bits = “01” or “1x”.

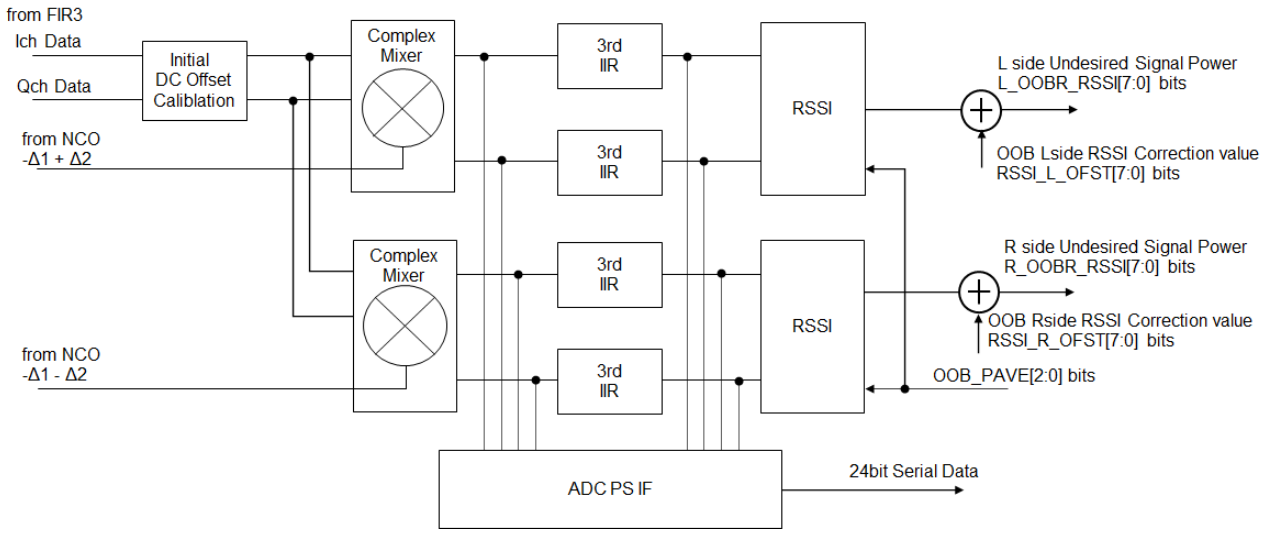


Figure 45 Out of Band Power Monitoring Block Diagram

The DC offset component of the received signal input to the Out of Band Power Monitoring circuit is converted to the local frequency component at the output of complex mixer. Therefore, it is possible to reduce the DC offset component by the Initial DC Offset Calibration so that the DC offset component does not affect to the result of power detection at the RSSI. And the IIR filter at later stage can further suppress the component converted to the local frequency. The internal node in the Out of Band Power Monitoring circuit can be observed by setting <Address 0x79>RXDTO bits. The output of complex mixer is confirmed by setting RXDTO bits = “0110(R side)” or “0111(L side)” and the output of third order IIR filter is confirmed by setting RXDTO bits = “1000(R side)” or “1001(L side)”. Both of them are serially output from ADFS, ADSCLK and ADSDO pins. It is possible to confirm the frequency conversion of complex mixer, frequency characteristic of third order IIR filter and the result of Initial DC Offset Calibration and so on by these settings. Refer to 13.8.20 Test Output Function of Internal Node for detail.

The Out of Band Power Monitoring circuit operates with the frequency of MCLK/128. The RSSI for Out of Band Power Monitoring averages the power calculated at this frequency. The average count is set by <Address0x50>OOB_PAVE[2:0] bits.

Table 12 Average Number of RSSI for Out of Band Power Monitoring

OOB_PAVE			Average Number
[2]	[1]	[0]	
0	0	0	1 data
0	0	1	2 data
0	1	0	4 data
. . .	. . .	. . .	. . .
1	1	0	64 data
1	1	1	128 data

13.8.4. NCO

The Numerically Controlled Oscillator (NCO) generates the local frequency of complex mixer. The local frequency is calculated by Δ1 (= <Address0x43>DELTA1F[7:0] bits), Δ2 (= <Address 0x44> DELTA2F[7:0] bits) and MCLK frequency. The local frequency of the complex mixer described in the chapter 13.8.2 uses Δ1 and the local frequency of the complex mixer for the Out of Band Power Monitoring circuit described in the chapter 13.8.3 uses -Δ1+Δ2 (L side) and -Δ1-Δ2 (R side). The Table 13 shows the frequency of Δ1 and Δ2 calculated by DELTA*F bits and the Table 14 shows the local frequency of Out of Band Power Monitoring circuit calculated by Δ1 and Δ2. The resolution and setting range of frequency shown in the Table 13 and Table 14 become half by setting <Address0x45>NCO_SET bit = "1".

MCLK = 24.576MHz : LO Frequency = DELTA*F[7:0] × 375.00 [Hz]
MCLK = 18.432MHz : LO Frequency = DELTA*F[7:0] × 281.25 [Hz]

Table 13 LO Frequency of Complex Mixer

Δ1, Δ2	MCLK = 24.576MHz	MCLK = 18.432MHz	Unit
127	47,625.00	35,718.75	Hz
126	47,250.00	35,437.50	
. . .	. . .	. . .	
44	16,500.00	12,375.00	
. . .	. . .	. . .	
33	12,375.00	9,281.25	
. . .	. . .	. . .	
1	375.00	281.25	
0	DC Output	DC Output	
-1	-375.00	-281.25	
. . .	. . .	. . .	
-67	-25,125.00	-18,843.75	
. . .	. . .	. . .	
-127	-47,625.00	-35,718.75	

Table 14 LO Frequency of Out of Band Power Monitoring Block

Δ1+Δ2, Δ1-Δ2	MCLK = 24.576MHz	MCLK = 18.432MHz	Unit
254	95,250.00	71,437.50	Hz
. . .	. . .	. . .	
1	375.00	281.25	
0	DC Output	DC Output	
-1	-375.00	-281.25	
. . .	. . .	. . .	
-254	-95,250.00	-71,437.50	

The frequency setting is loaded by <Address0x45>ROM_UPDATE[1:0] bits after setting local frequency by Δ1 and Δ2. The ROM_UPDATE bits automatically returns to zero after setting.

Table 15 ROM_UPDATE Function

ROM_UPDATE		Function
[1]	[0]	
0	0	Not update
0	1	Update the NCO frequency Δ1 of main path
1	0	Update the NCO frequency (Δ1±Δ2) of Out of Band Power Monitoring
1	1	Update all NCO frequency

13.8.5. Decimation Filter

The block diagram of receiving filter circuit is shown below. After passing through the ΔΣ ADC, the operating frequency of the receiving signal is gradually decreased while the ΔΣ noise is attenuated by the decimation filter. The output of FIR3, FIR4 and FIR5 can be selected by setting <Address0x41> DFIL_PATH[1:0] bits.

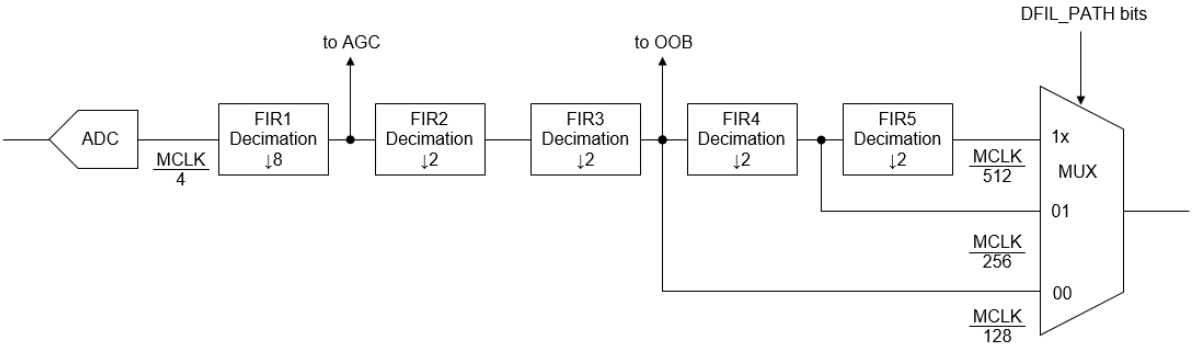
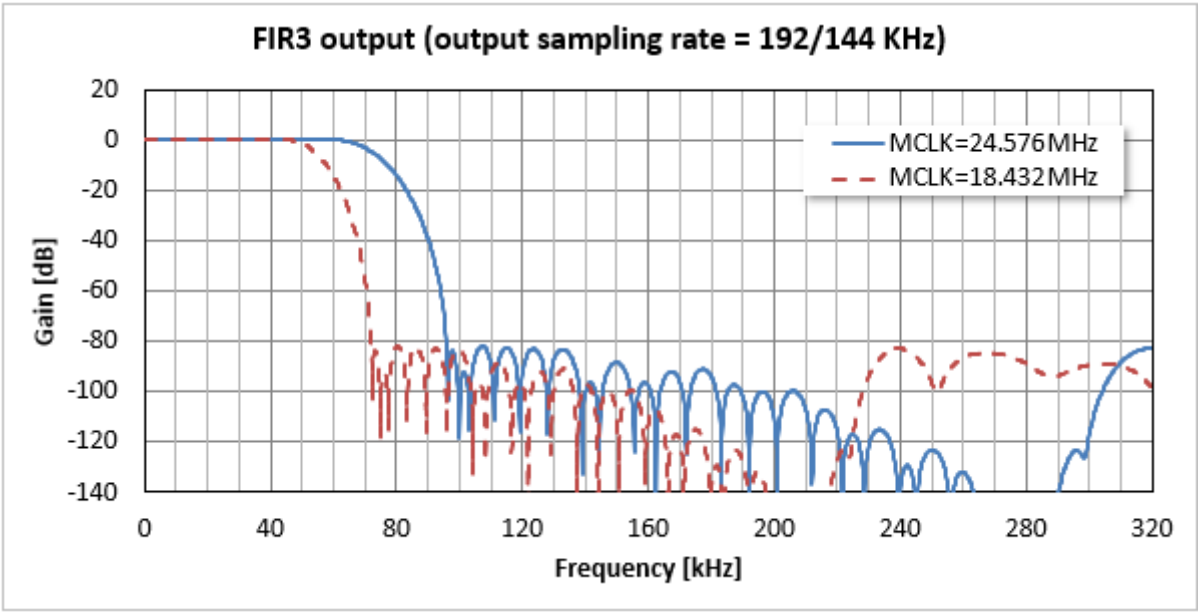
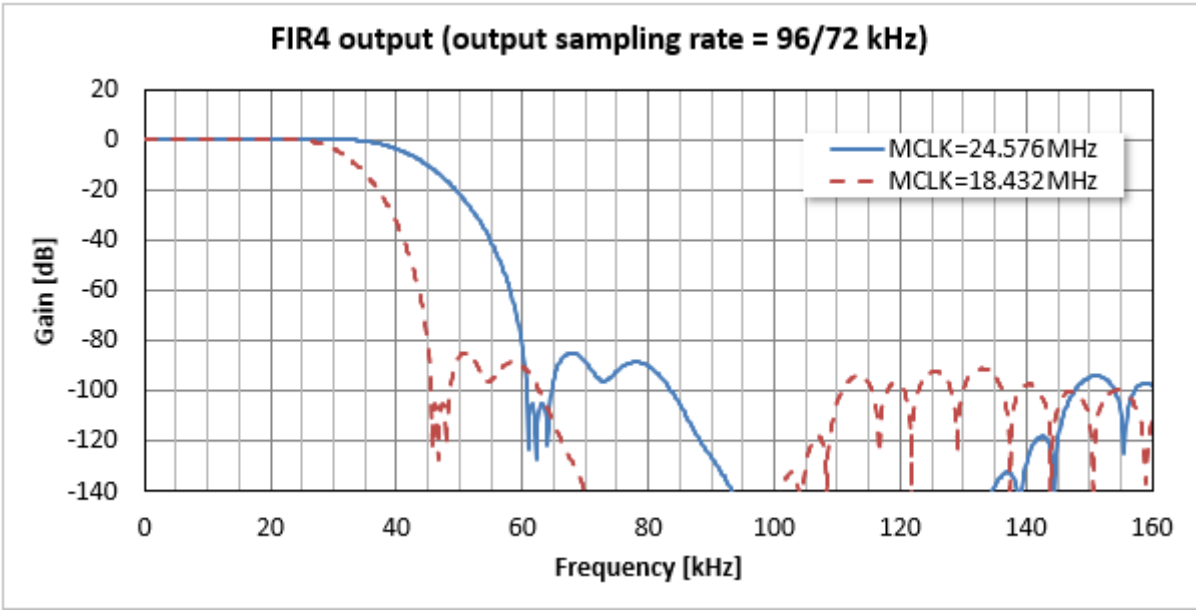


Figure 46 Decimation Filter Block Diagram





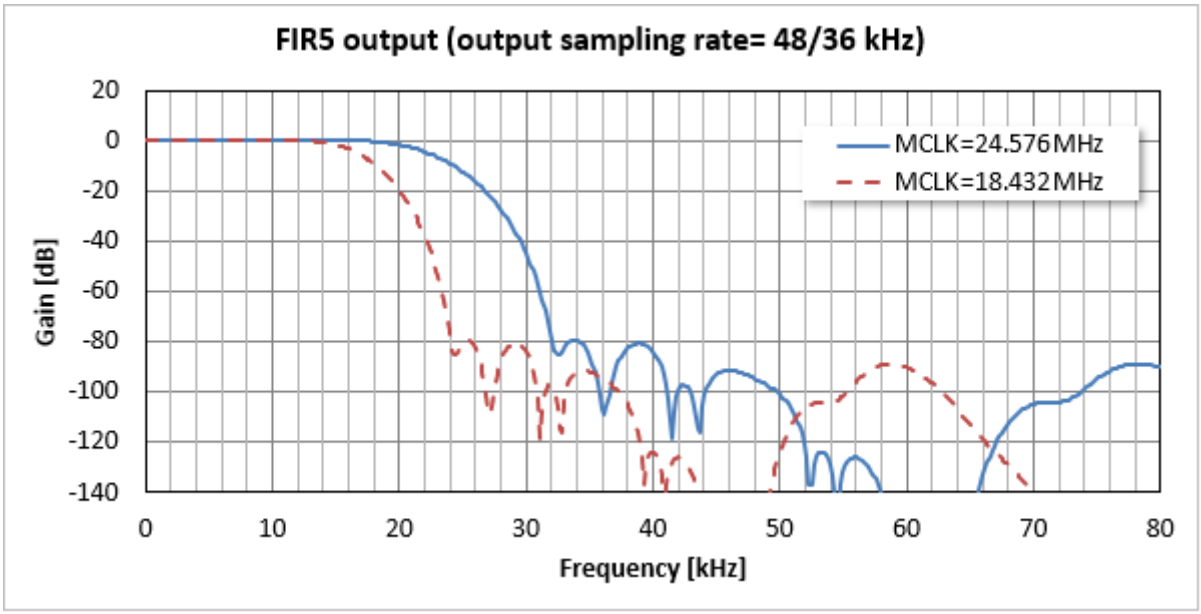


Figure 47 Decimation Filter Frequency Characteristics

13.8.6. HPF

The HPFs are placed at three locations in total. One is placed in front of the AGC circuit for offset removal, and the other two are placed in front of each of the two complex mixers.

■ AGCHPF

The AGCHPF located at later of the FIR1 can be used by setting “1” to <Address0x34>AGCHPFSEL bit. The high pass filter consists of a first order IIR and its cut off frequency is switched by <Address 0x34>AGCHPF_FC[3:0] bits. The Table 16 shows the frequency characteristics. And the cutoff frequency of the AGCHPF is also changed by setting of <Address0x41>DFIL_PATH[1:0] bits because the output signal of the FIR1 is decimated at the operating frequency of the channel filter by the AGCHPF.

Table 16 AGCHPF Cutoff Frequency

AGCHPF_FC				Gain [dB]	Cutoff Frequency						
					MCLK=24.576MHz			MCLK=18.432MHz			Unit
[3]	[2]	[1]	[0]		DFIL_PATH[1:0] bits			DFIL_PATH[1:0] bits			
					2’b00	2’b01	2’b1X	2’b00	2’b01	2’b1X	
0	0	0	0	0.00	0.9	0.5	0.2	0.7	0.4	0.2	Hz
0	0	0	1	0.00	1.9	0.9	0.5	1.4	0.7	0.4	
0	0	1	0	0.00	3.7	1.9	0.9	2.8	1.4	0.7	
0	0	1	1	0.00	7.5	3.7	1.9	5.6	2.8	1.4	
0	1	0	0	0.00	15.0	7.5	3.7	11.2	5.6	2.8	
0	1	0	1	0.00	29.9	15.0	7.5	22.4	11.2	5.6	
0	1	1	0	0.01	59.9	29.9	15.0	44.9	22.5	11.2	
0	1	1	1	0.02	119.9	59.9	30.0	89.9	45.0	22.5	
1	0	0	0	0.03	240.2	120.1	60.1	180.2	90.1	45.0	
1	0	0	1	0.07	482.4	241.2	120.6	361.8	180.9	90.4	
1	0	1	0	0.14	972.3	486.2	243.1	729.2	364.6	182.3	
1	0	1	1	0.28	1975.5	987.7	493.9	1481.6	740.8	370.4	
1	1	X	X	0.56	4078.0	2039.0	1019.5	3058.5	1529.2	764.6	

X:Do not care

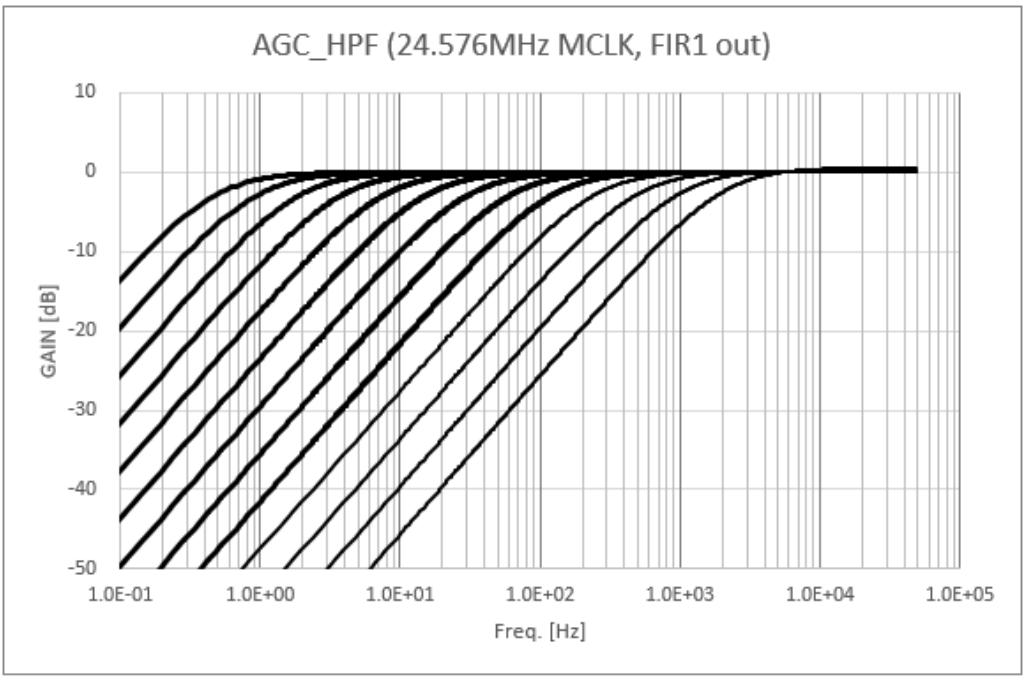


Figure 48 AGCHPF Frequency Characteristics (DFIL_PATH bits = “01”)

■ PRE_HPF

The PRE_HPF located in front of the complex mixer for the down conversion (LOW_IF -> ZERO_IF) can be used by setting <Address0x46>PRE_HPFSEL[1:0] bits. When setting “01” to PRE_HPFSEL[1:0] bits, the PRE_HPF consists of the first order IIR filter and when setting “1x” to PRE_HPFSEL[1:0] bits, the PRE_HPF consists of the second order IIR filter. The cut off frequency can be switched by <Address0x46>PRE_HPF_FC[3:0] bits. The Table 17 shows the frequency characteristics of the first order HPF and Table 18 shows the frequency characteristics of the second order HPF. The cut off frequency is also changed by <Address0x41>DFIL_PATH[1:0] bits because the PRE_HPF operates at the operating frequency of the channel filter.

Table 17 1st order PRE_HPF Cutoff Frequency

PRE_HPF_FC				Gain [dB]	Cutoff Frequency						Unit
					MCLK=24.576MHz			MCLK=18.432MHz			
					DFIL_PATH[1:0] bits			DFIL_PATH[1:0] bits			
[3]	[2]	[1]	[0]		2’b00	2’b01	2’b1X	2’b00	2’b01	2’b1X	
0	0	0	0	0.00	0.9	0.5	0.2	0.7	0.4	0.2	Hz
0	0	0	1	0.00	1.9	0.9	0.5	1.4	0.7	0.4	
0	0	1	0	0.00	3.7	1.9	0.9	2.8	1.4	0.7	
0	0	1	1	0.00	7.5	3.7	1.9	5.6	2.8	1.4	
0	1	0	0	0.00	15.0	7.5	3.7	11.2	5.6	2.8	
0	1	0	1	0.00	29.9	15.0	7.5	22.4	11.2	5.6	
0	1	1	0	0.01	59.9	29.9	15.0	44.9	22.5	11.2	
0	1	1	1	0.02	119.9	59.9	30.0	89.9	45.0	22.5	
1	0	0	0	0.03	240.2	120.1	60.1	180.2	90.1	45.0	
1	0	0	1	0.07	482.4	241.2	120.6	361.8	180.9	90.4	
1	0	1	0	0.14	972.3	486.2	243.1	729.2	364.6	182.3	
1	0	1	1	0.28	1975.5	987.7	493.9	1481.6	740.8	370.4	
1	1	0	0	0.56	4078.0	2039.0	1019.5	3058.5	1529.2	764.6	
1	1	0	1	1.16	8692.4	4346.2	2173.1	6519.3	3259.7	1629.8	
1	1	1	X	2.5	19707.5	9853.8	4926.9	14780.6	7390.3	3695.2	

X:Do not care

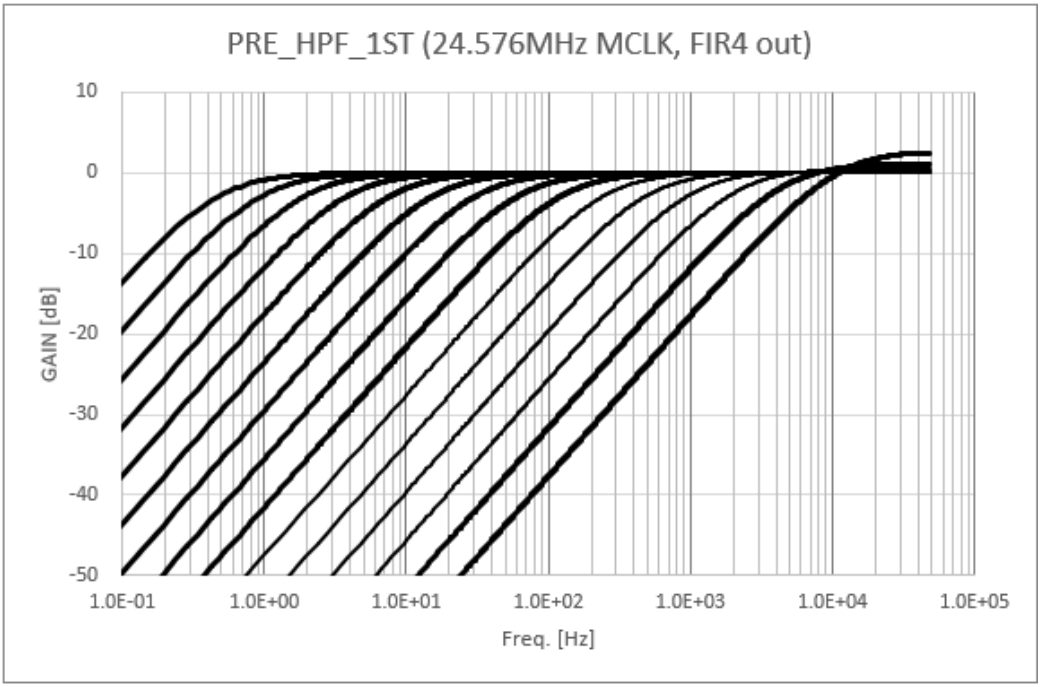


Figure 49 1st order PRE_HPF Frequency Characteristics (DFIL_PATH bits = “01”)

Table 18 2nd order PRE_HPF Cutoff Frequency

PRE_HPF_FC				Gain [dB]	Cutoff Frequency						Unit
					MCLK=24.576MHz			MCLK=18.432MHz			
					DFIL_PATH[1:0] bits			DFIL_PATH[1:0] bits			
[3]	[2]	[1]	[0]		2'b00	2'b01	2'b1X	2'b00	2'b01	2'b1X	
0	0	0	0	0.00	0.9	0.5	0.2	0.7	0.4	0.2	Hz
0	0	0	1	0.00	1.9	0.9	0.5	1.4	0.7	0.4	
0	0	1	0	0.00	3.7	1.9	0.9	2.8	1.4	0.7	
0	0	1	1	0.00	7.5	3.7	1.9	5.6	2.8	1.4	
0	1	0	0	0.00	15.0	7.5	3.7	11.2	5.6	2.8	
0	1	0	1	0.01	30.0	15.0	7.5	22.5	11.2	5.6	
0	1	1	0	0.02	60.0	30.0	15.0	45.0	22.5	11.3	
0	1	1	1	0.03	120.4	60.2	30.1	90.3	45.1	22.6	
1	0	0	0	0.07	242.1	121.1	60.5	181.6	90.8	45.4	
1	0	0	1	0.14	490.1	245.0	122.5	367.5	183.8	91.9	
1	0	1	0	0.27	1004.0	502.0	251.0	753.0	376.5	188.3	
1	0	1	1	0.55	2109.8	1054.9	527.4	1582.3	791.2	395.6	
1	1	0	0	1.11	4684.1	2342.0	1171.0	3513.1	1756.5	878.3	
1	1	0	1	2.32	11868.2	5934.1	2967.0	8901.1	4450.6	2225.3	
1	1	1	X	5.00	46530.2	23265.1	11632.6	34897.7	17448.8	8724.4	

X:Do not care

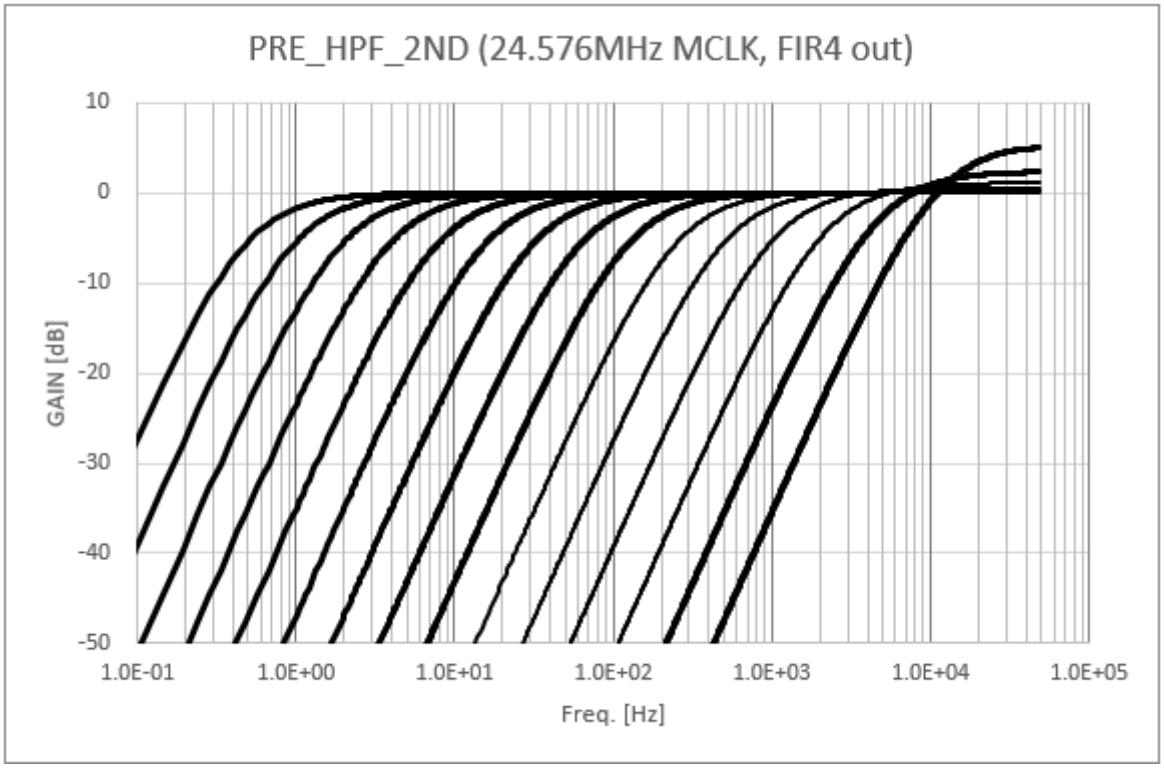


Figure 50 2nd order PRE_HPF Frequency Characteristics (DFIL_PATH bits = "01")

■ POST_HPF

The POST_HPF located in front of the complex mixer for the up conversion (ZERO_IF -> LOW_IF) can be used by setting “1” to <Address0x5F>POST_HPFSEL. The high pass filter consists of a first order IIR filter and the cut off frequency can be switched by <Address0x5F>POST_HPF_FC[3:0] bits. The Table 19 shows the frequency characteristics. The cut off frequency is also changed by <Address0x41>DFIL_PATH[1:0] bits because the POST_HPF operates at the operating frequency of the channel filter. The POST_HPF cannot be used at the same time with the RDOC function described in the chapter 13.8.9. Use the POST_HPF by setting “0” to <Address0x62>RDOC_ON bit.

Table 19 POST_HPF Cutoff Frequency

POST_HPF_FC				Gain [dB]	Cutoff Frequency						Unit
					MCLK=24.576MHz			MCLK=18.432MHz			
					DFIL_PATH[1:0] bits			DFIL_PATH[1:0] bits			
[3]	[2]	[1]	[0]		2’b00	2’b01	2’b1X	2’b00	2’b01	2’b1X	
0	0	0	0	0.00	0.9	0.5	0.2	0.7	0.4	0.2	Hz
0	0	0	1	0.00	1.9	0.9	0.5	1.4	0.7	0.4	
0	0	1	0	0.00	3.7	1.9	0.9	2.8	1.4	0.7	
0	0	1	1	0.00	7.5	3.7	1.9	5.6	2.8	1.4	
0	1	0	0	0.00	15.0	7.5	3.7	11.2	5.6	2.8	
0	1	0	1	0.00	29.9	15.0	7.5	22.4	11.2	5.6	
0	1	1	0	0.01	59.9	29.9	15.0	44.9	22.5	11.2	
0	1	1	1	0.02	119.9	59.9	30.0	89.9	45.0	22.5	
1	0	0	0	0.03	240.2	120.1	60.1	180.2	90.1	45.0	
1	0	0	1	0.07	482.4	241.2	120.6	361.8	180.9	90.4	
1	0	1	0	0.14	972.3	486.2	243.1	729.2	364.6	182.3	
1	0	1	1	0.28	1975.5	987.7	493.9	1481.6	740.8	370.4	
1	1	X	X	0.56	4078.0	2039.0	1019.5	3058.5	1529.2	764.6	

X:Do not care

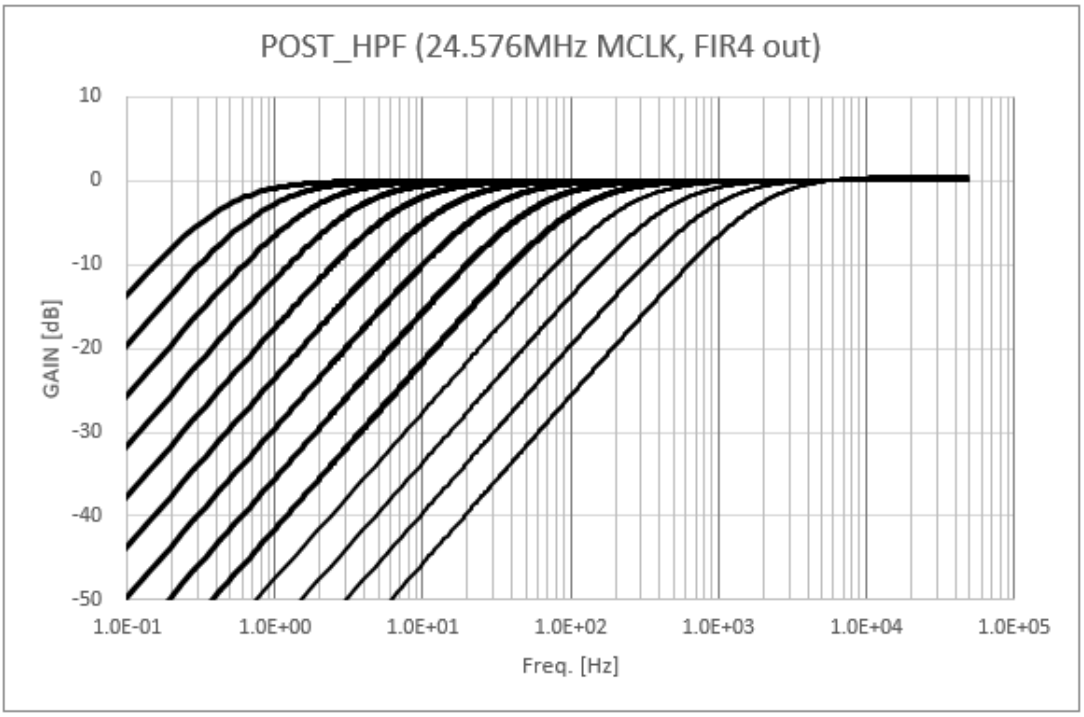
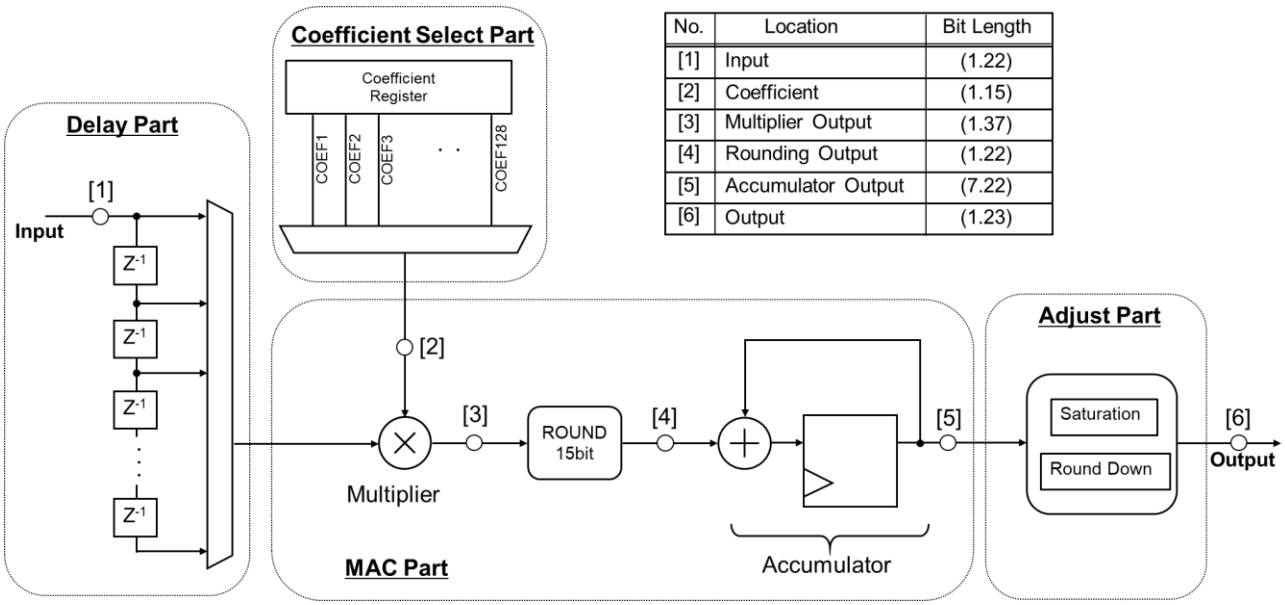


Figure 51 POST_HPF Frequency Characteristics(DFIL_PATH bits = “01”)

13.8.7. Channel Filter

The channel filter is a programmable FIR filter which can be set by arbitrary coefficients. Four filter characteristics can be set by setting <Address0x4A>CHCOEF_SEL[1:0] bits. The Figure 52 shows the block diagram of the programmable FIR. The filter consists of the Delay Part, the Coefficient Select Part, the MAC part (Multiplier and Accumulator) and the Adjust Part (bit adjustment). The table shown in the Figure 52 shows the bit length at points [1] to [6]. Regarding the notation of the bit length, for example, bit length (1.22) indicates a total 23-bit configuration of 1 bit to the left of the decimal point and 22 bits to the right of the decimal point.



No.	Location	Bit Length
[1]	Input	(1.22)
[2]	Coefficient	(1.15)
[3]	Multiplier Output	(1.37)
[4]	Rounding Output	(1.22)
[5]	Accumulator Output	(7.22)
[6]	Output	(1.23)

Figure 52 Programmable FIR Filter Block Diagram

■Constraint of the coefficient

The constraint of the coefficient is shown below.

Bit Number	Bit	16
Input Range	Dec	+32767 to -32767
	Hex	7FFFh to 8001h (* 58)
Maximum Value of Total of Coefficient	Dec	262143 (2^18-1)
Maximum Value of Total of Absolute Coefficient	Dec	524287 (2^19-1)

Note:
* 58. Setting “8000(hex)” is prohibited.

The number of taps which can be input is restricted as following by the setting of <Address0x41> DFIL_PATH[1:0] bits.

DFIL_PATH[1:0]	Total number of TAP
“00”	64 (TAP1 to TAP64)
“01” , “1X”	128 (TAP1 to TAP128)

■Adjust Part

The saturation processing and round down processing are executed after the output of the Accumulator. The saturation processing is executed for the ACCOUT[28:0] (bit length (7.22)) at [5] in the Figure 52 output from the Accumulator. The saturation processing is executed by the setting of <Address0x4A>PFIL_SAT[2:0] bits and bit adjustment is executed to make the output bit length to be 24-bit. First the saturation processing and then round down is executed. The adjustment is executed to make the output to be 24-bit because the bit length changes after the saturation processing. If the bit length exceeds 24-bit after the saturation processing, it is adjusted to 24-bit by the round down of the excess bits. And if the bit length is less than 24-bit after the saturation processing, it is adjusted to 24-bit by filling missing LSB side with “0”.

Table 20 Channel filter output bit adjustment

PFIL_SAT			Saturation processing	Round down bit	ACCOUT bit	Gain
[2]	[1]	[0]				
0	0	0	2-bit	3-bit	ACCOUT [26:3]	× 1/8
0	0	1	3-bit	2-bit	ACCOUT [25:2]	× 1/4
0	1	0	4-bit	1-bit	ACCOUT [24:1]	× 1/2
0	1	1	5-bit	0-bit	ACCOUT [23:0]	× 1
1	0	0	6-bit	0-bit	ACCOUT [22:0], 1’d0	× 2
1	0	1	7-bit	0-bit	ACCOUT [21:0], 2’d0	× 4
1	1	0	8-bit	0-bit	ACCOUT [20:0], 3’d0	× 8
1	1	1	9-bit	0-bit	ACCOUT [19:0], 4’d0	× 16

The operation order is described below based on the actual configuration example.

Operation Example)

The “coef” below is a coefficient calculated by such as the MATLAB and the total is approximately 1.

FIR3 path
<Address0x41> DFIL_PATH[1:0] = 2’d0
<Address0x4A> PFIL_SAT[2:0] = 3’d5

OUT = IN × [coef × 2^16] / (2^15) × 4

FIR4 path
<Address0x41> DFIL_PATH[1:0] = 2’d1
<Address0x4A> PFIL_SAT[2:0] = 3’d4

OUT = IN × [coef × 2^17] / (2^15) × 2

FIR5 path
<Address0x41> DFIL_PATH[1:0] = 2’d2
<Address0x4A> PFIL_SAT[2:0] = 3’d3

OUT = IN × [coef × 2^18] / (2^15) × 1

■Writing/Reading coefficients

Three pins of CSN, SCLK and SDI are used to write/read the coefficients of programmable FIR filter. It is possible to hold four kinds of the coefficients by setting <Address0x42>COEF_SET[7:0] bits. Refer to 9.4 Serial Interface Timing for Programmable Digital Filter Coefficient Setting for the writing AC timing. The writing or reading all coefficients of 128TAP must be executed continuously during the CSN pin is "L". When the writing or reading all coefficients of 128TAP is finished and CSN pin is set to "H", the burst mode of the writing or reading the coefficients is finished and normal writing or reading of the registers becomes capable. If the FIR3 path is selected and only 64TAP are used, write the same coefficients twice to write the coefficients of 128TAP. The Figure 53 shows the timing chart of writing and reading the coefficients of the programmable FIR filter and the Figure 54 shows the block diagram to hold the coefficients.

The writing operation moves to the burst writing mode after <Address0x42>COEF_SET[7:0] bits= "7x(hex)" (x=1, 2, 3, 4) is set, and the CSN pin is set to "H" once and then the CSN pin is set to "L". The reading operation moves to the burst reading mode after <Address0x42>COEF_SET[7:0] bits= "Fx(hex)" (x=1, 2, 3, 4) is set, and the CSN pin is set to "H" once and then the CSN pin is set to "L".

And it is possible to confirm whether the writing or reading is correctly executed or not by <ROpage Address 0x03> R_COEFSTS_x bit (x=1, 2, 3, 4, OOB, NSQ1, NSQ2) after completing the writing or reading the coefficients. Input the clocks of 16[bit]×128[TAP] = 2048[clock] to the SCLK pin during the burst writing or reading mode of the coefficients. At that time in the AK2404, the number of input clocks are counted while the CNS pin is set to "L" in the burst mode. When the CSN pin is set to "H", if the number of clocks is less than 2048 clocks or more than 2048 clocks, R_COEFSTS_x bit is set to "1" regarded as the writing is not executed correctly. If the burst writing or reading mode of the coefficients is completed with 2048 clocks, R_COEFSTS_x bit is set to "0" regarded as the writing is executed correctly. The initial value of R_COEFSTS_x bit is "1" and is set to "0" only when the writing or reading of the coefficients is correctly completed.

The coefficients are once stored to the internal registers when the burst writing mode is completed. The coefficients are loaded to the programmable filter when one of four kinds of coefficients is selected by <Address0x4A>CHCOEF_SEL[1:0] bits and <Address0x4A>COEFLOAD bit = "1" is set. The COEFLOAD bit automatically returns to "0" after the coefficients are loaded. Write "1" to COEFLOAD bit after when the clock is input by setting "1" to <Address0x6D>PD_CLKBUF_N bit. Set COEFLOAD bit = "1" again when <Address0x6F>PD_ADC_N bit = "1" is set, <Address0x4A>CHCOEF_SEL bits is changed or <Address0x41>DFIL_PATH bits is changed.

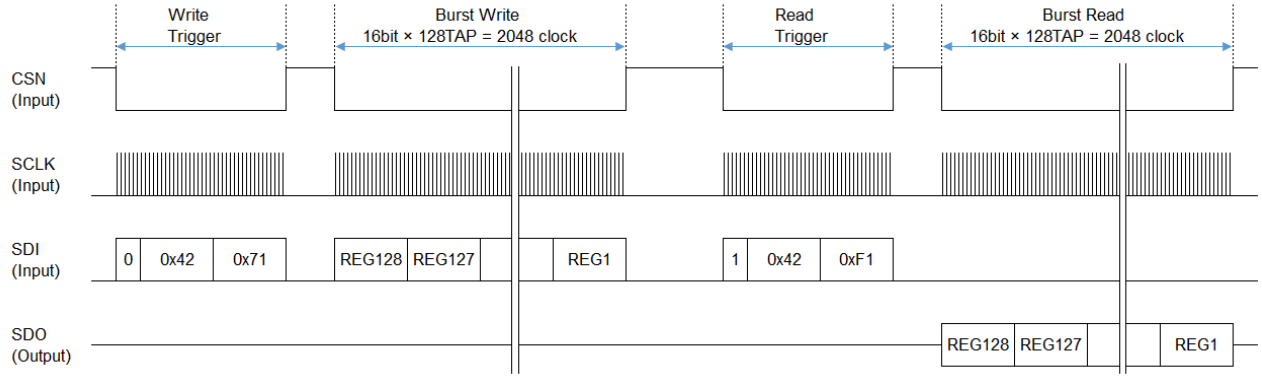


Figure 53 Programmable FIR Filter Coefficient Write/Read Timing Chart

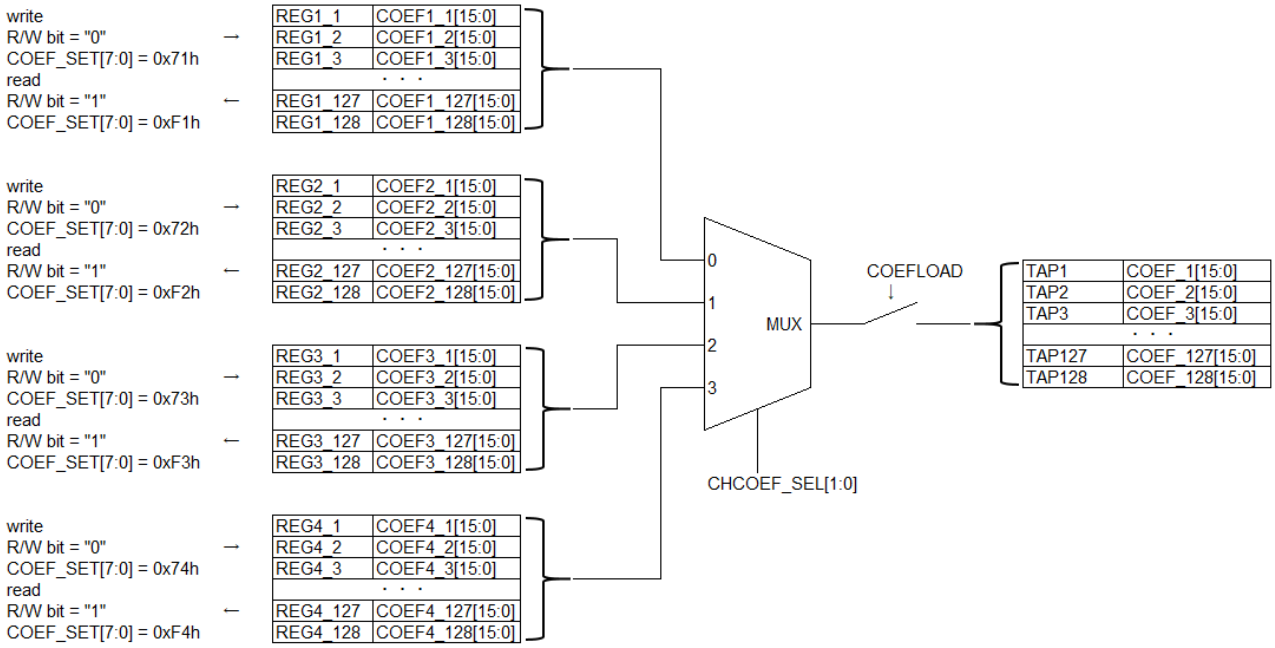


Figure 54 Programmable FIR Filter Coefficient Write/Read Block Diagram

13.8.8. DC Offset Calibration

The DC offset calibration is executed by the receiving analog circuit and receiving digital circuit. The DC offset calibration of the receiving analog circuit is executed by the MIXER and the DC offset calibration of the receiving digital circuit is executed by the main path (output of the last stage of the Decimation filter), AGC block and Out of Band Power Monitoring control block in the receiving digital circuit.

Refer to 12.3 Power-up Sequence of the Receiver or the operating sequence of the DC offset calibration.

■ DC Offset Calibration of Analog Block (MIXER)

The DC offset calibration of the analog block is executed by the MIXER. The calibration starts when setting “1” to <Address0x24>OFSCAL1 bit and it takes 40μs to complete (CAL Time(1)). The OFSCAL1 bit automatically return to “0” after the calibration is completed. The result of the calibration is initialized by the hardware reset or software reset.

The result of the calibration is read from the following registers.
<ROpage Address0x10>R_OFSTA_I bits : Ich DC offset calibration code
<ROpage Address0x11>R_OFSTA_Q bits : Qch DC offset calibration code

■ DC Offset Calibration of Digital Block

The DC offset calibration is executed by the main path, AGC block and Out of Band Power Monitoring control block. The calibration starts when setting “1” to <Address0x24>OFSCAL2 bit. The calibration is executed by calculating the time average of the output from the Decimation Filter, input of the AGC or input of the Out of Band Power Monitoring circuit and subtracting it from each data. The Table 21, Table 22 and Table 23 show each calibration time. The calibration is simultaneously executed at the three parts, the main path, AGC and Out of Band Power Monitoring control block. And the calibration is executed by switching the PGA gain repeatedly (wait -> Minimum PGA Gain -> wait -> Maximum PGA Gain). The OFSCAL2 bit automatically returns to “0” after all calibrations are completed. Therefore, the DC offset calibration time (CALTIME(2)) of the digital block is limited by the time of the longest calibration.

The <Address0x27>FIROFS_AVE bits sets the average processing time during the calibration of the receiving main path. Because the sampling frequency changes due to the filter path selected by the

<Address0x41>DFIL_PATH[1:0] bits, the calibration time also changes. The Table 21 shows the calibration time of the receiving main path when the reference clock of 18.432MHz or 24.576MHz is used.

Table 21 Calibration time of Main Path

DFIL_PATH	FIROFS_AVE		CAL Time (Main Path)		
	[1]	[0]	18.432MHz	24.576MHz	Unit
00	0	0	3.4	3.3	ms
	0	1	3.9	3.7	
	1	0	4.8	4.3	
	1	1	6.6(default)	5.7(default)	
01	0	0	3.9	3.7	
	0	1	4.8	4.3	
	1	0	6.6	5.7	
	1	1	10.1(default)	8.3(default)	
1X	0	0	4.8	4.3	
	0	1	6.6	5.7	
	1	0	10.1	8.3	
	1	1	17.2(default)	13.7(default)	

Similarly for the calibration of the AGC control block, the <Address0x27>AGCOFS_AVE bits sets the average processing time during the calibration. The calibration time changes due to the fiter path selected by the DFIL_PATH[1:0] bits. The Table 22 shows the calibration time of the AGC when the reference clock of 18.432MHz or 24.576MHz is used.

Table 22 Calibration time of AGC

DFIL_PATH	AGCOFS_AVE		CAL Time (AGC Path)		
	[1]	[0]	18.432MHz	24.576MHz	Unit
00	0	0	3.4	3.3	ms
	0	1	3.9	3.7	
	1	0	4.8	4.3	
	1	1	6.6(default)	5.7(default)	
01	0	0	3.9	3.7	
	0	1	4.8	4.3	
	1	0	6.6	5.7	
	1	1	10.1(default)	8.3(default)	
1X	0	0	4.8	4.3	
	0	1	6.6	5.7	
	1	0	10.1	8.3	
	1	1	17.2(default)	13.7(default)	

The <Address0x27>FIROFS_AVE bits sets the average processing time during the calibration of the Out of Band Power Monitoring control block. The Table 23 shows the calibration time of the Out of Band Power Monitoring control block when the reference clock of 18.432MHz or 24.576MHz is used.

Table 23 Calibration time of Out of Band Power Monitoring control block

FIROFS_AVE		CAL Time (Out of band)		
[1]	[0]	18.432MHz	24.576MHz	Unit
0	0	3.4(default)	3.3(default)	ms
0	1	3.9	3.7	
1	0	4.8	4.3	
1	1	6.6	5.7	

The result of the calibration can be read from the following registers.

<ROpage Address0x12 to 0x17>R_OFSTD_I[23:0], R_OFSTD_Q[23:0] bits: main path
<ROpage Address0x18 to 0x1D>R_OFSTD_OOBI[23:0], R_OFSTD_OOBQ[23:0] bits: Out of Band Power Monitoring control block
<ROpage Address0x1F to 0x20, 0x22 to 0x23>R_AGCOFS_I[15:0], R_AGCOFS_Q[15:0] bits: AGC Control block

The calibration is calculated for each gain of the PGA and the result for the gain set at the time of readback is read out.
The result of the calibration is initialized by the hardware reset or software reset.

13.8.9. RDOC Function

The POST_HPF or Real-time DC Offset Canceler (RDOC) can be selected to cancel the DC offset when the ZERO_IF is used. The RDOC is the function to follow the varying DC offset at real time during receiving and always cancel the DC offset. The RDOC function is effective when receiving signal of the modulation type without amplitude fluctuation like the FM or FSK. It is possible to read back the amount of the DC offset cancelled by the RDOC from <ROpage Address0x24 to 0x26> R_RDOC_I bits and <ROpage Address0x27 to 0x29> R_RDOC_Q bits.

■RDOC setting
The following registers are for the RDOC operation setting. Set all registers to the initial value.

Register	Address	Initial Value
RDOC_1	0x62 D6	“1”
RDOC_2	0x62 D4-D3	“10”
RDOC_3	0x62 D2-D1	“01”
RDOC_4	0x63 D6	“0”
RDOC_5	0x63 D5-D4	“00”
RDOC_6	0x63 D2-D1	“00”
RDOC_7	0x63 D0	“0”
RDOC_8	0x64 D6-D4	“010”
RDOC_9	0x64 D2-D1	“00”
RDOC_10	0x64 D0	“0”
RDOC_11	0x65 D7-D6	“11”
RDOC_12	0x65 D5-D4	“11”
RDOC_13	0x65 D2-D1	“00”
RDOC_14	0x65 D0	“0”
RDOC_15	0x66 D7-D6	“11”
RDOC_16	0x6B D7-D0	“00101010”
RDOC_17	0x6C D7-D0	“00001010”
RDOC_18	0x66 D1-D0	“00”
RDOC_19	0x67 D4	“0”
RDOC_20	0x67 D2-D1	“00”
RDOC_21	0x67 D0	“0”
RDOC_22	0x68 D2-D1	“00”
RDOC_23	0x69 D6-D5	“00”
RDOC_24	0x69 D4-D3	“00”
RDOC_25	0x69 D2-D0	“101”
RDOC_26	0x6A D7-D0	“00001001”

■Control function of the local frequency offset (OFS_RDOC)
Set <Address0x68>RDOC_FM bit = “1” when receiving non-modulated signal (CW) like the analog radio with FM modulation. This function automatically controls to add the offset frequency to the local signal relative to the receiving signal so that the frequency of local signal and receiving signal do not match. And when detecting that the local signal and receiving signal match, the polarity of the offset frequency is switched. The offset frequency is set by <Address0x02-0x03>OFS_RDOC bits and it is recommended to set 150Hz with the frequency after the LOCAL DIVIDER division.

The operating state of this function is output from the LD pin by setting <Address0x16>LD_RDOC bit = “1”. When the LD pin = “L”, the value of set by OFS_RDOC bits is set to the synthesizer and when the LD pin = “H”, the offset frequency set by OFS_RDOC bits with opposite polarity is set to the synthesizer. The lock detection signal is not output at that time.

Turn off this function by setting RDOC_FM bit = “0” and OFS_RDOC bits=all 0 when the non-modulated signal (CW) is not received like the digital radio with FSK modulation.

13.8.10. AGC Function

The AK2404 has a AGC (Auto Gain Control) function. When the AK2404 receives a strong signal, the AGC controls PGA gain so that the input level of the ADC converges to the desired target level without exceeding the full-scale range. The AGC start to operate by setting <Address0x30>PGA_AGCON bit = “1”. It is possible to set the gain by <Address0x35>PGAGAIN[5:0] bits manually when setting <Address 0x30> PGA_AGCON bit = “0”.

The Figure 55 shows the AGC block diagram, the Figure 56 through Figure 58 shows the flowchart of the AGC and the Figure 59 show the timing chart during the AGC operation. The AGC has following related registers and operates according to the set values. Refer the chapter 14.6 AGC for detail.

<Address0x38>AGCTIM[3:0] bits : Interval to calculate and judge the signal power
<Address0x38>AGCTRW[3:0] bits : Wait time after gain switching
<Address0x35>PGAGAIN[5:0] bits : PGA gain setting
<Address0x36>AGCMAX[2:0] bits : Maximum allowable gain variation in one AGC operation
<Address0x36>AGCTGT[3:0] bits : Target value of ADC input signal power convergence level
<Address0x37>AGCHYS[1:0] bits : Hysteresis width for signal power convergence level
<Address0x37>AGCLIM[5:0] bits : Maximum gain limit setting for PGA

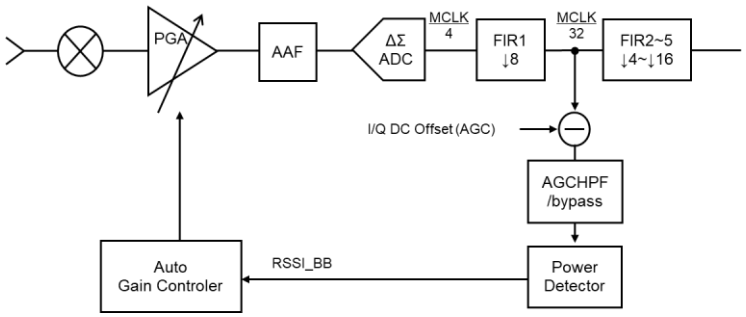


Figure 55 AGC Block Diagram

The AGC operation is described according to the numbers [1] to [5] in the main flowchart shown in the Figure 56.

[1] AGC ON/OFF
Set the PGA_AGCON bit = “1” to start the AGC operation, as described earlier.

[2] AGCKEEP process
When the AGC starts operation, it judges the AGC KEEP function. The AGC KEEP function refers the function which pauses the AGC operation by the register control or pin control and this judgement is executed first. The Figure 57 shows the flowchart of AGCKEEP process. For the AGC KEPP function, the timing of changing the PGA gain depends on the setting of <Address0x30>AGC_KPMODE bit. Refer the chapter 13.8.12 AGC KEEP Function for detail.

[3] Transient response waiting time
The AGC waits for the time set by AGCTRW bits after starting operation. It also waits for the same time when it starts the next calculation after calculating the PGA gain. This is the waiting time which takes into account the transient response time after start-up the receiving or after switching the gain.

[4] Power detection
After waiting for the convergence of the transient response of the received signal, the AGC detects the signal power at every time set by AGCTIM bits. The signal power detection circuit is located in front of the programable FIR filter and detects the signal power passed the analog filter and input to the ADC. The RSSI_BB executes same operation as in 13.8.15 RSSI Function. The result of the power detection of the RSSI_BB is possible to read back by the <ROpage Address0x0A>R_RSSI_BB bits. This value is updated at every time set by AGCTIM bits.

[5] PGA GAIN operation processing

The Figure 58 shows the flowchart of the PGA GAIN operation processing. The AGC calculates the PGA gain to keep the ADC input level constant. At this time, the AGC adjusts the PGA gain to define the convergence range as the upper limit of the convergence is (AGCTGT bits + AGCHYS bits) and the lower limit of the convergence is (AGCTGT bits - AGCHYS bits) and to keep the ADC input level within this range. If the detected power is higher than the upper limit, the PGA gain is decreased and if it is lower than the lower limit, the PGA gain is increased. At this time, the amount of gain variation in one calculation is limited to the maximum value set in AGCMAX bits. And the maximum value of the PGA is limited by AGCLIM bits.

After the AGC function is turned on, the AGC repeats the operation of [2] to [5]. Even after the receiving signal level becomes stable and the gain variation is stopped, the AGC internally executes the power detection and judgement at every waiting time set by AGCTRW bits and AGCTIM bits. Therefore, if the receiving signal level changes, the follow-up operation is executed again according to the detection level. It is possible to confirm the timing when the AGC changed the PGA gain by status bit output from the STATUS pin (Refer to 13.8.19 Status Output.).

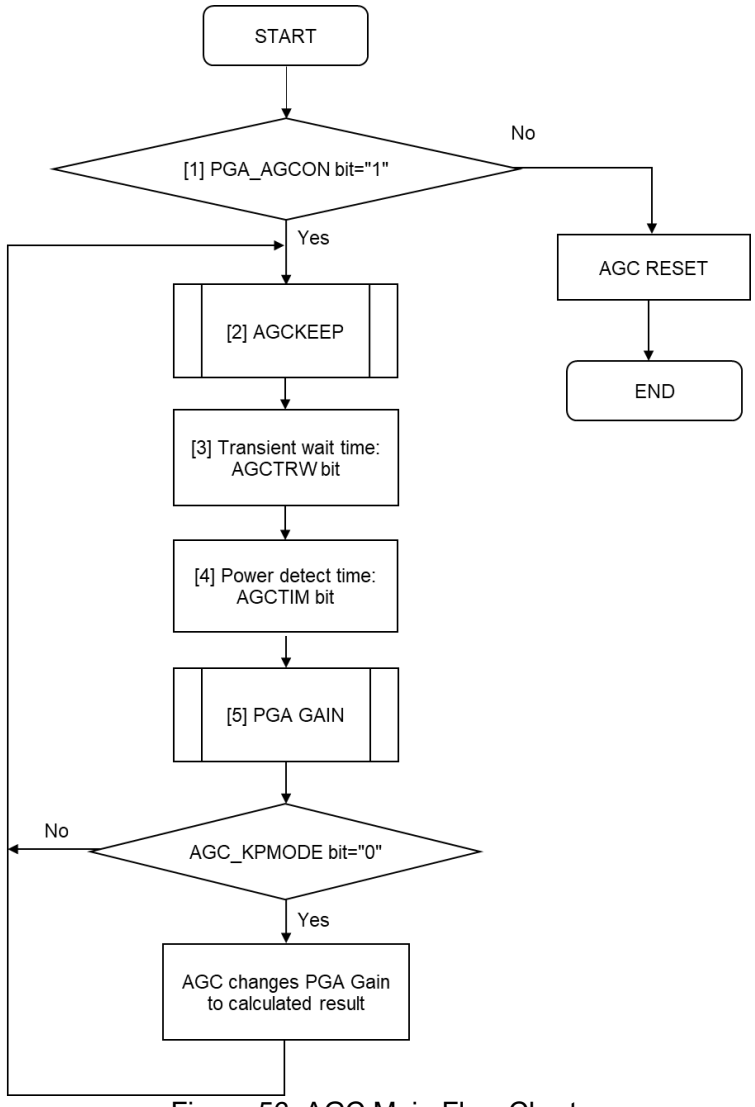


Figure 56 AGC Main Flow Chart

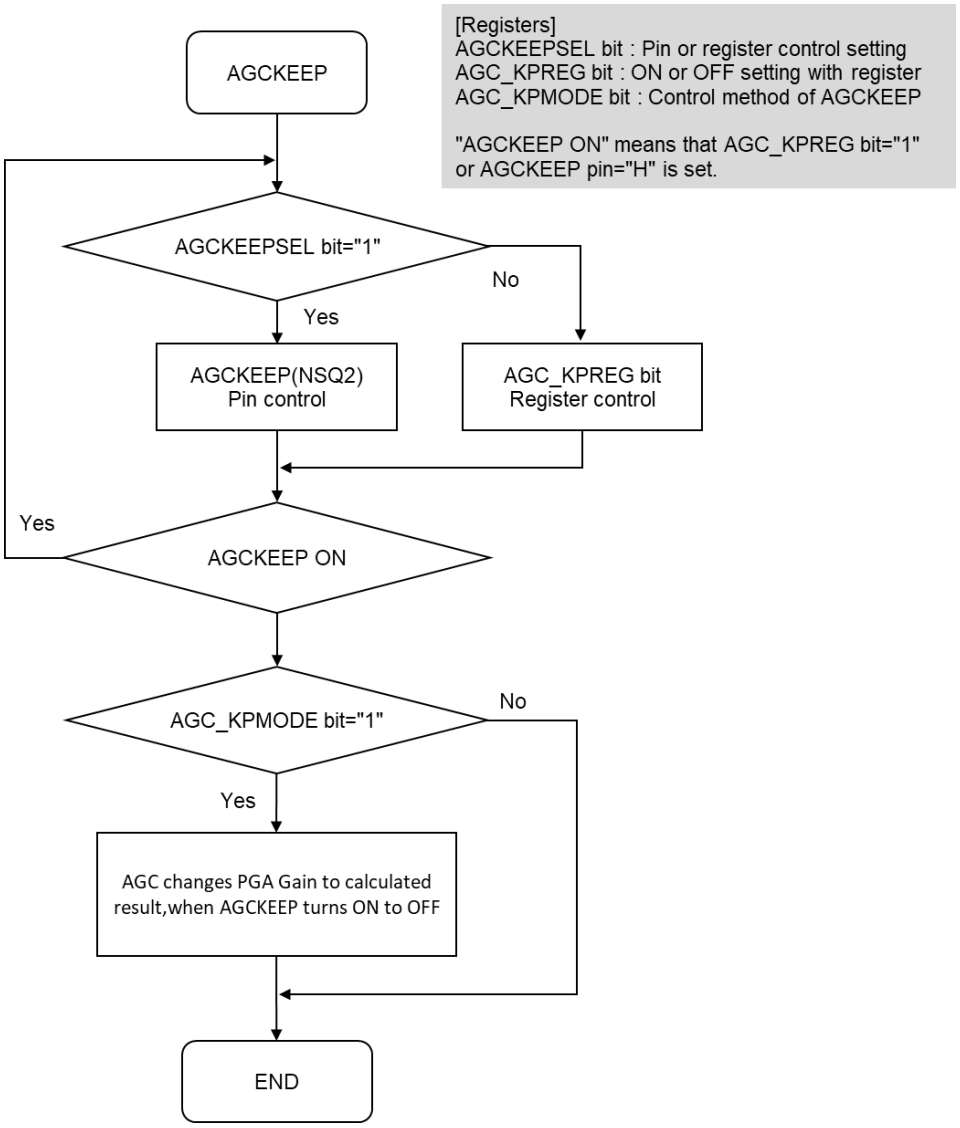


Figure 57 AGC Sub Frow Chart (AGCKEEP)

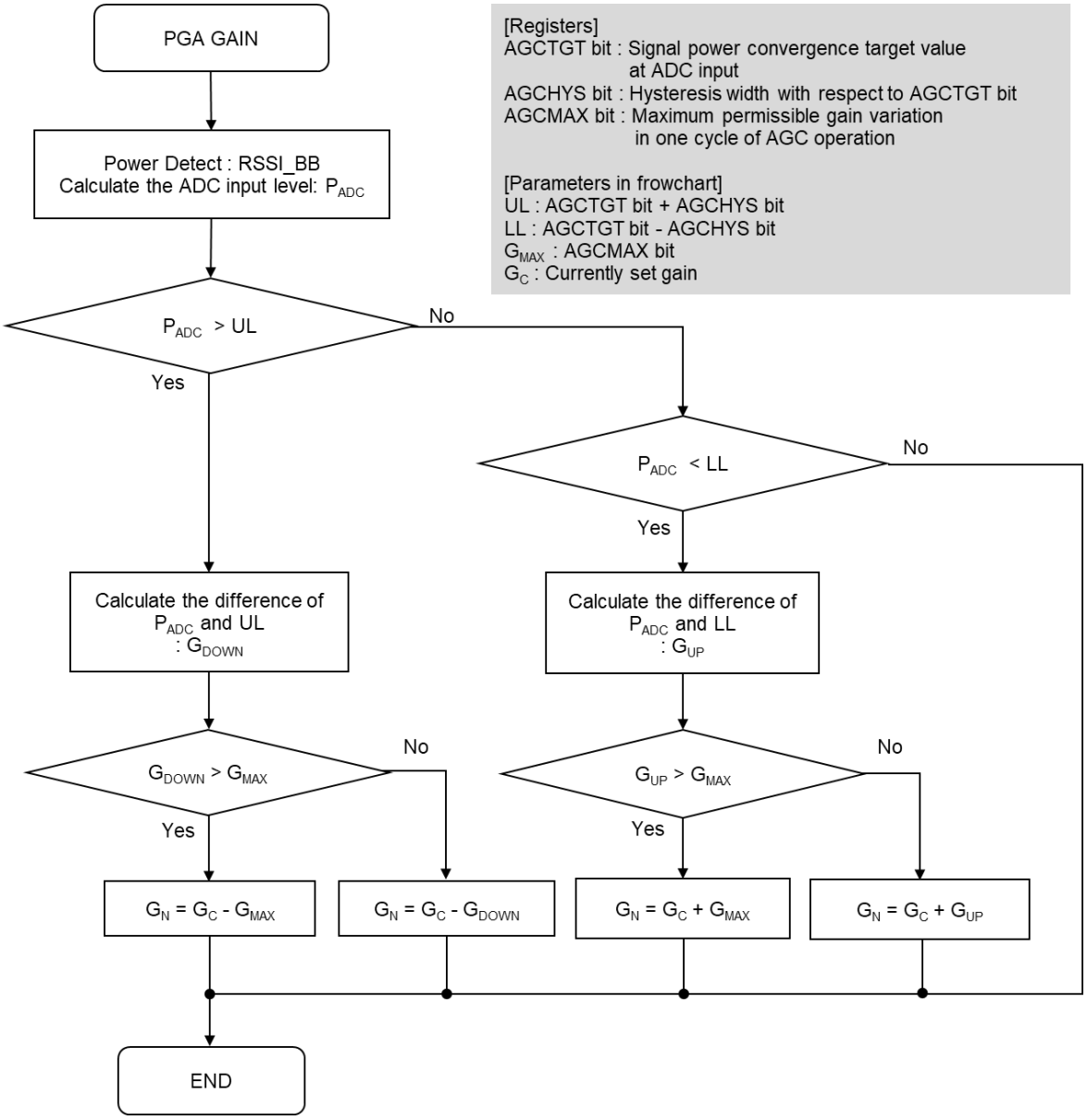
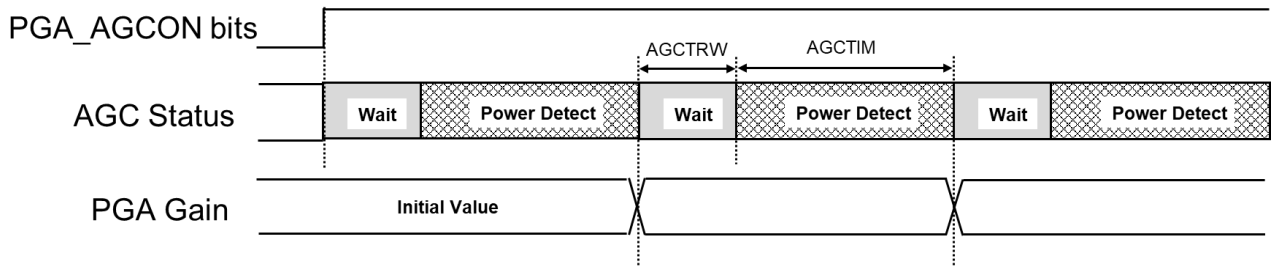


Figure 58 AGC Sub Frow Chart (PGA GAIN)



Wait : Period set by AGCTRW bits
Power Detect : Period set by AGCTIM bits
PGA Gain Initial Value : PGAGAIN bits Setting

Figure 59 AGC Operation Timing Chart

13.8.11. Digital Output AGC Function

The digital output AGC function refers to the function which automatically switches the 16-bit serial output from the 24-bit digital filter output based on the received signal level detected by the RSSI in the AGC.

It is necessary to set <Address0x41>ADIFSEL[1:0] bits = “01” (IQ 16-bit Mode) and to operate the AGC (PGA_AGCON bit = “1”) to use this function. The digital output AGC function becomes available by setting <Address0x3E>DAGC_ON bit = “1”.

The digital output AGC function compares the threshold set by <Address0x3E>DAGC_HYS[1:0] bits and <Address0x3F>DAGC_TH[7:0] with the result calculated by the RSSI located after the channel filter, and switches [1] 16-bit of the MSB side and [2] the output bits set by <Address0x3E> DFILOUT[2:0] bits (Table 24).

The timing to switch the digital AGC output depends on the AGC setting because the digital AGC function operates at the same time with the AGC of PGA. Refer to 13.8.10 for detail. The AGC KEEP function is applied to this control as well. When <Address0x30>AGC_KPMODE bit = “0” is set, the output bit is switched at the timing of the RSSI calculation under the condition that the AGC KEEP function is off. When AGC_KPMODE bit = “1” is set, the output bit is switched at the timing when the AGC KEEP function is turned from “ON” to “OFF” based on the RSSI result lastly calculated before the timing when the AGC KEEP function is turned from “OFF” to “ON”. Refer to the chapter 13.8.12 for detail of the AGC KEEP function.

When outputting, the MSB side is saturated and the LSB side is truncated. The Figure 60 shows an example of the output bit configuration. This example shows the configuration when [2] DFILOUT[2:0] bits = “101” is set. When the AGC function is turned off by setting PGA_AGCON bit = “0” or when the digital output AGC function is turned off by setting DAGC_ON bit= “0”, the output bit is fixed to the output bit set by DFILOUT bits of [2].

Table 24 Digital Filter Output bit Setting

DFILOUT			Output bit
[2]	[1]	[0]	
0	0	0	ADCOUT[23:8]
0	0	1	ADCOUT[22:7]
0	1	0	ADCOUT[21:6]
0	1	1	ADCOUT[20:5]
1	0	0	ADCOUT[19:4]
1	0	1	ADCOUT[18:3]
1	1	0	ADCOUT[17:2]
1	1	1	ADCOUT[16:1]

The Figure 61 shows the operation when the output bit is switched. When the RSSI calculation result is greater than or equal to the set value of DAGC_TH[7:0], the [1] side is selected for the output bit. When the RSSI calculation result is less than or equal to the value of subtracting the hysteresis width set by DAGC_HYS[1:0] bits from the value set by DAGC_TH[7:0] bits, the [2] side is selected for the output bit. Read back <ROpage Address 0x04> R_DAGC_STS or check the AGC status bit S7 (refer to the chapter 13.8.19 Status Output) output from the STATUS pin to find out whether the digital output AGC is in [1] or [2] state.

Figure 60 Digital Filter Output bit Structure (eg. DFILOUT bits= “101”)

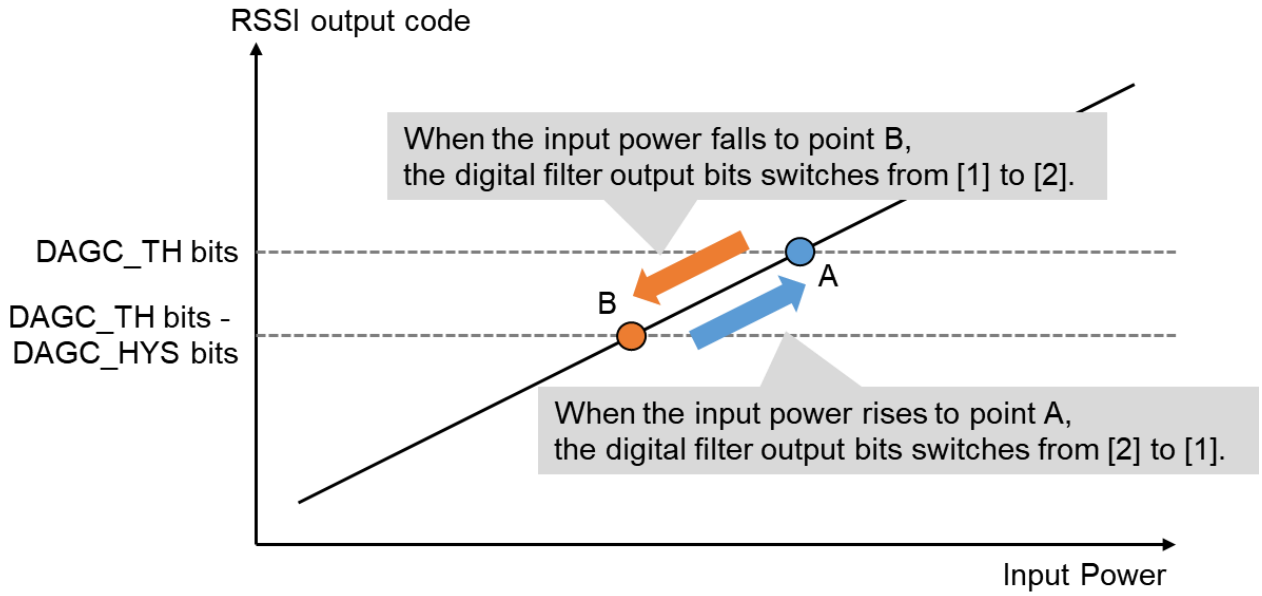
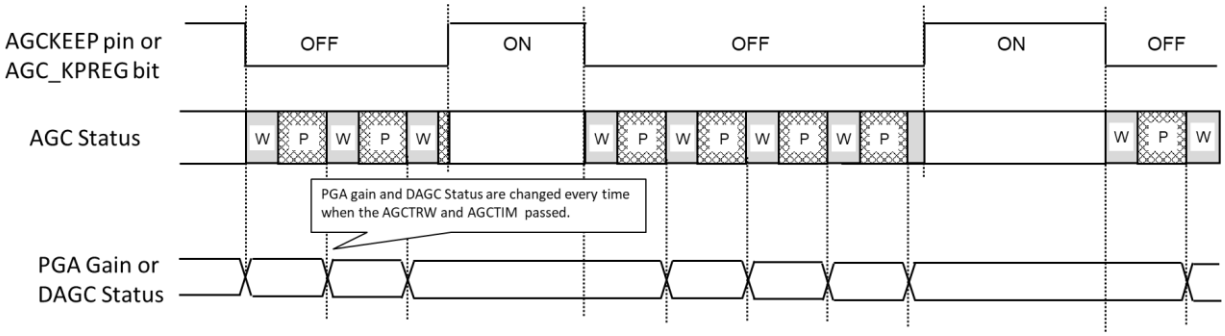


Figure 61 Output bit Transition with Digital Output AGC Function

13.8.12. AGC KEEP Function

The AK2404 has a gain retention function. By turning on this function, the AGC keeps the PGA gain and status of the digital AGC during the AGC operation and stops the operation. This function is controlled by <Address0x30>AGC_KPREG bit or AGC_KEEP pin.
The <Address0x30>AGC_KEEP_SEL bit switches the register control or pin control. The AGC_KEEP pin (input pin) is used with the NSQ2 pin (output pin) and is initially set to the NSQ2 pin. When setting AGC_KEEP_SEL bit = “1”, the NSQ2 pin switches to the input pin and operates as the AGC_KEEP pin. When AGC_KPREG bit = “1” or AGC_KEEP pin = “H” is set, the AGC keep function is turned on. The AGC KEEP function changes the gain change and hold operation according to the setting of the <Address0x30>AGC_KPMODE bit. The detail of the AGC_KPMODE bit is described below.

■ AGC_KPMODE bit= “0”
If the AGC keep function is not enabled, the AGC calculates and judges the power every time set by AGCTIM and AGCTRW bits, and changes the PGA gain and the output bit status of the digital output AGC. If the AGC keep function is turned from “OFF” to “ON”, the status of the PGA gain and the output bit status of the digital AGC are held at that time. The AGC does not operate and does not calculate and judge the power while the AGC keep function is set to “ON”. And the counter which counts the time set by AGCTIM and AGCTRW bits is cleared. If the AGC KEEP function is changed from “ON” to “OFF” again, the AGC operation is restarted with initial value of the held operation state. The Figure 62 shows the timing chart.



W : Wait (Period set by AGCTRW bits)
P : Power Detect (Period set by AGCTIM bits)

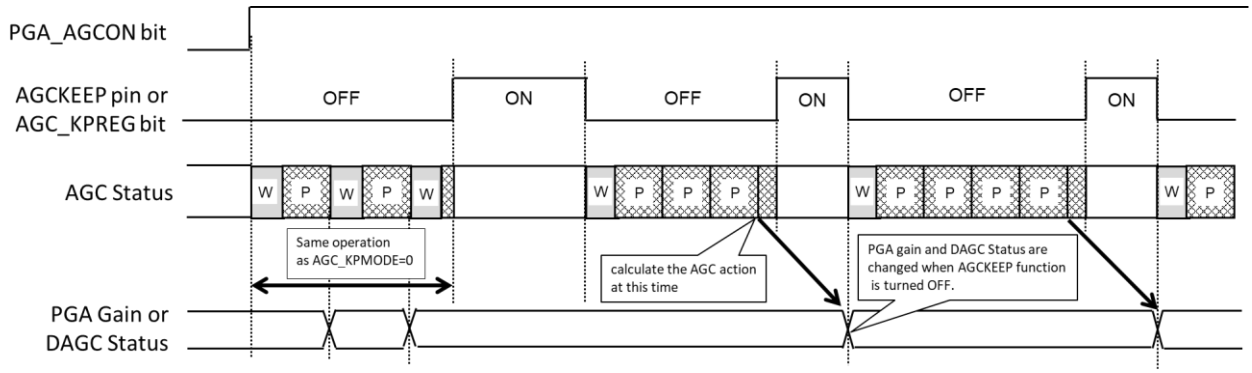
Figure 62 AGC operation when AGC_KPMODE bit = “0” is set.

■ AGC_KPMODE bit = “1”

After the AGC starts to operate, the AGC operation changes before and after the AGC is turned from “ON” to “OFF” for the first time. Before the AGC KEEP function is turned from “ON” to “OFF” for the first time, the AGC calculates and judges the power every time set by AGCTIM and AGCTRW bits, and changes the PGA gain and the output bit status of the digital output AGC. (The same operation is executed as AGC_KPMODE bit = “0” until the AGC KEEP is turned to “ON” for the first time.)

The operation is as follows, once the AGC KEEP function is turned from “ON” to “OFF”. The PGA gain and the output bit status of the digital output AGC change only when the AGC KEEP function changes from “ON” to “OFF”. The PGA gain and the output bit status of the digital output AGC do not change during the AGC KEEP function is “OFF”, but the power is detected every time set by the AGCTIM bits. The PGA gain and the output bit status of the digital output AGC are calculated by the power detected at the last “OFF” state before the AGC KEEP function is changed from “OFF” to “ON”, and the operation results are held. At the timing when the AGC KEEP function is changed from “ON” to “OFF” again, the calculation results retained at the time of the previous changeover from “OFF” to “ON” are reflected. The Figure 63 shows the timing chart.

The update timing of <ROpage Address0x09-0B>>R_RSSI_BB is the timing when the AGC KEEP function is changed from “OFF” to “ON”.



W : Wait (Period set by AGCTRW bits)
P : Power Detect (Period set by AGCTIM bits)

Figure 63 AGC operation when AGC_KPMODE bit = “1” is set.

13.8.13. FM Detection Function

The AK2404 has an FM detection circuit. The FM detection circuit consists of a DAC, a SMF and noise squelch circuits (NSQ1 and NSQ2). The Figure 64 shows the whole block diagram. The FM receive signal is FM demodulated after passing the ADC and the digital filter by the FM demodulator circuit using digital signal processing. The demodulated signal is output with 24-bit and added a value of the <Address0x56 to 0x58>IF_OFST[23:0] bits to adjust the DC offset. Then the <Address0x54> FMDET_G[1:0] bits is used to adjust the bits according to the maximum frequency deviation of the FM signal, and then the signal is output in 16-bit. The data signal is then truncated to the lower 4bits, converted to an analog signal by a 12-bit DAC, and the folded component is removed by a SMF (Smoothing Filter) and output from the DETOUT pin. And it is also possible to output the bit adjusted 16-bit demodulated signal as digital serial data from the ADFS, ADSCLK, and ADSDO pins by setting <Address0x41>ADIFSEL bits = "10". The NSQ1 and NSQ2 have a signal processing function by the programmable filter which coefficients can be set arbitrarily. Refer to 13.8.16 Noise Squelch Function about the noise squelch function.

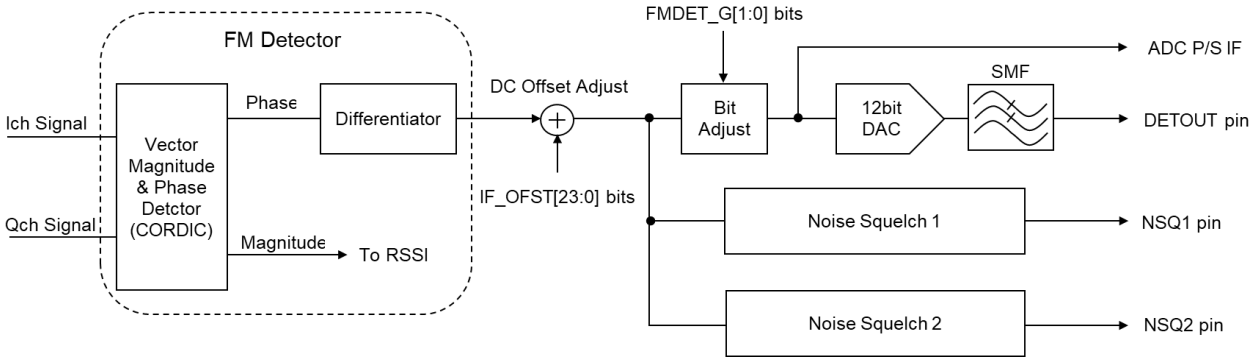


Figure 64 FM Detector Block Diagram

13.8.14. DETDAC, SMF Function

The DETDAC consists of a 12-bit DAC and can output three kinds of signals as shown in Table 25 by setting <Address0x54>RSSI_DETOUT and REG_DETOUT bits. The converted analog signal is input to the SMF and then is output from the DETOUT pin. The Figure 65 shows the frequency characteristic of the SMF. Note that depending on the sampling rate of the DETDAC, the folded noise generated during the D-A conversion can not be sufficiently attenuated. Add an external LPF if needed.

Table 25 DETDAC function

REG_DETOUT	RSSI_DETOUT	DETDAC function
0	0	FM demodulation output
0	1	RSSI output
1	X	General Purpose DAC

■ FM demodulation output

The FM demodulation output refers to the function which outputs the digital modulated signal from the FM demodulated circuit as the analog signal from the DETDAC. Adjust the output level with FMDET_G[1:0] bits so that the desired maximum frequency deviation is represented. When the LOW-IF signal is input to FM detection circuit, the IF frequency is FM demodulated as DC Offset. Remove it by IF_OFST bits.

■ RSSI output

When setting RSSI_DETOUT bit = "1", the DETDAC outputs the RSSI operation result as analog output. Refer to the chapter 13.8.15 RSSI Function for detail.

■ General Purpose DAC

When setting REG_DETOUT bit = “1”, the data written to <Address0x5D>DET_DC[7:0] bits is input to the DETDAC and is output from the DETOUT pin. At this time, the DET_DC bits are input to the 8-bit of the MSB side of the 12-biit DAC and the 4-bit of the LSB side is filled with “0”.

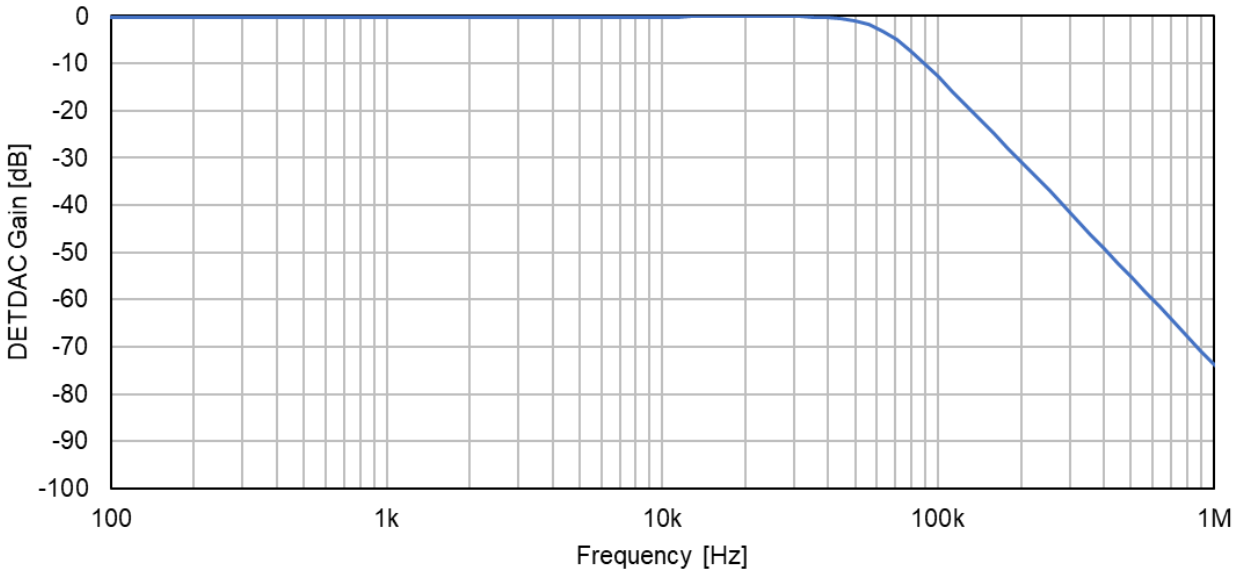


Figure 65 DETDAC SMF Frequency Characteristics

13.8.15. RSSI Function

The RSSI function provides two types of output: digital and analog.

■ Digital Output RSSI

The Figure 66 shows the block diagram of the RSSI function. The input level is detected for the signal passed the channel filter by the power detection circuit and is output as the LOG converted code. (If the DC offset calibration and RDOC function are used, the power is detected for the signal level corrected by these functions.) After that, the average processing is executed at the operating frequency of the programmable FIR filter which sampling rate is set by <Address0x41>RXIF_SR bit = “00”. The number of sampling to average is set by <Address0x4C>RSSIAVE[2:0] bits.

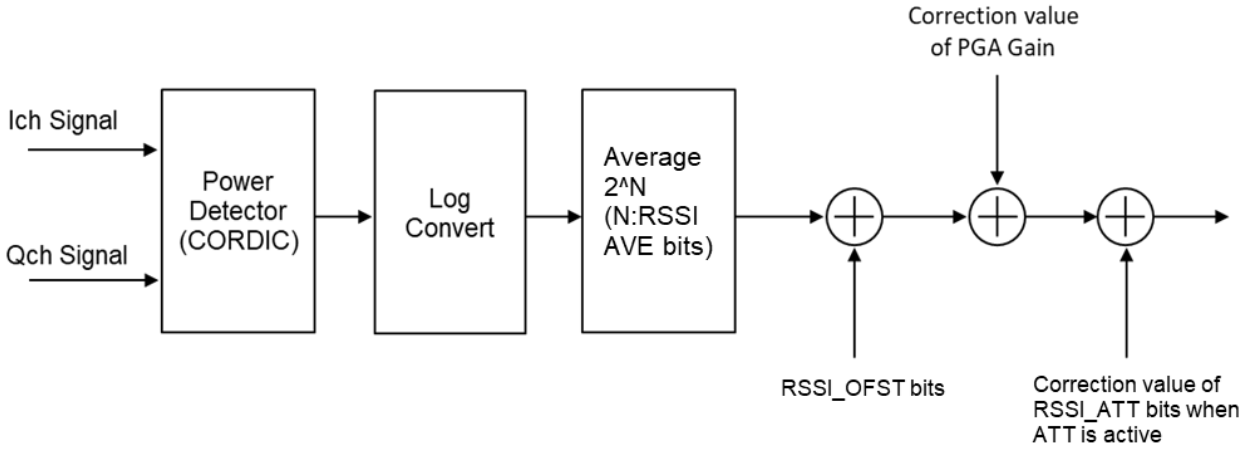


Figure 66 RSSI Block Diagram

The formula below shows the relation between the RSSI output code and the input power to the AK2404. The formula assumes that the LNA is used and that each block gain from the LNA to the RSSI circuit is typical value. And the gain of MIXER+PGA+AAF+ADC is assumed that the High Power Mode in the Band 1 is used and that the total gain is 59dB (including the matching circuit). The resolution of the RSSI code is 0.5dB/code.

RSSI code (dec) = 2 × LNA Input Level [dBm] + RSSI_OFST bits + 262

LNA Input Level [dBm] = (RSSI code (dec) - RSSI_OFST bits - 262) / 2

When the PGA gain is changed by the AGC or register setting, the RSSI corrects the output value by the changed gain. And when the ATT operates instead of the LNA, the value set by <Address0x4E> RSSI_ATT bits is added to the RSSI result as a correction value. Adjust the correction value appropriately by the amount of the ATT attenuation set by <Address0x33>ATTLVL bits. The <Address 0x4D>RSSI_OFST bits adds an offset to the operation result of the RSSI. For example, adjust by the RSSI_OFST bits when the gain deviates from the typical value, the Low Power Mode is used for MIXER+PGA+AAF+ADC or the dynamic range of the RSSI is expected to be adjusted.

The RSSI characteristic in the Figure 67 shows the characteristic when the total gain is typical value. Note that the saturation characteristic of gain at the input level above P1dB or the effect of noise on the RSSI at the input level close to the noise floor are not considered.

The digital output RSSI can be read from the <ROpage Address 0x06>R_RSSI bits. And it can be read as serial data synchronized with received data from the ADSDO pin or STATUS pin. Refer to the chapter 13.8.19 Status Output for detail.

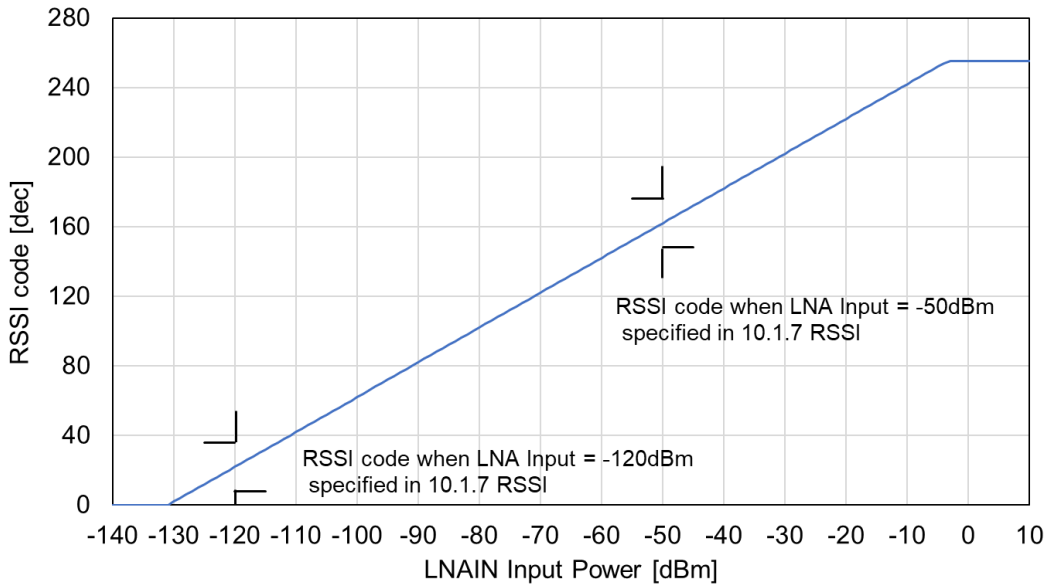


Figure 67 RSSI特性

■ Analog Output RSSI

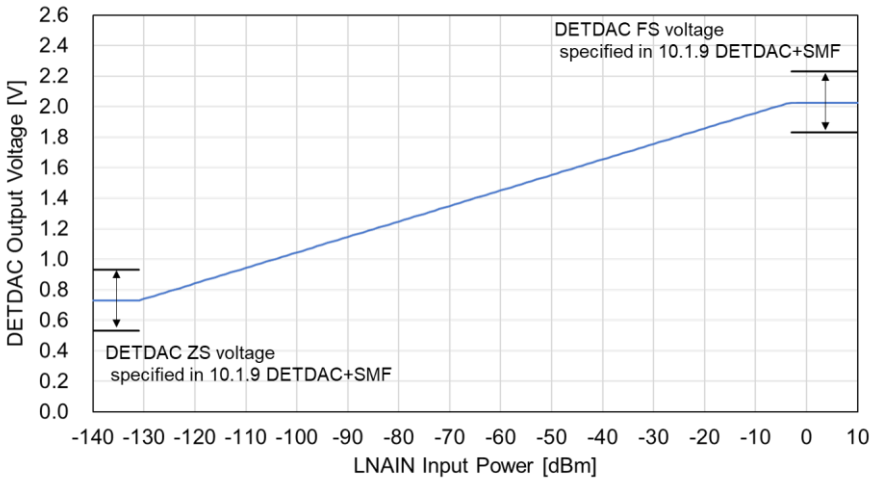
As described in the chapter 13.8.14 DETDAC, SMF Function, the operation result of the RSSI is output in analog format from the DETDAC when setting <Address0x54>RSSI_DETOUT bit = “1”. The data input to the DETDAC (DETDAC_IN[11:0]) is as follows and is calculated in straight binary.

- If RSSIDAC_LOLIM[7:0] × 16 < (RSSI[7:0] + DET_DC[7:0]) × 16,
  DETDAC_IN[11:0] = (RSSI[7:0] + DET_DC[7:0]) × 16

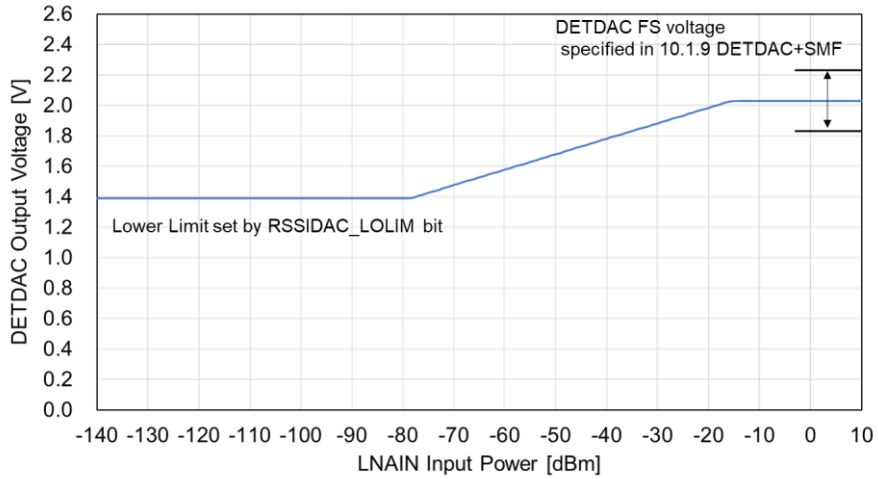
- If (RSSI[7:0] + DET_DC[7:0]) × 16 ≤ RSSIDAC_LOLIM[7:0] × 16,
  DETDAC_IN[11:0] = RSSIDAC_LOLIM[7:0] × 16

Here, the RSSI[7:0] means the RSSI code after the correction of RSSI_OFST bits, RSSI_ATT bits and PGA gain in the Figure 66. The <Address0x55>RSSIDAC_LOLIM[7:0] bits sets the lower limit of RSSI input to the DETDAC. The <Address0x5D>DET_DC bits in this function is added to the RSSI[7:0] as an offset value. And the saturation processing is executed if the calculated result of an input data is less than or equal to 0 or greater than or equal to 4095(dec).

The Figure 68 shows an example of input/output characteristic of the analog output RSSI. (This case is what the RSSI code in the digital part is calculated on the assumption that the gain of receiving analog part is typical.) Refer to the chapter 13.8.15 RSSI Function about the RSSI of digital part.



(a) RSSIDAC_LOLIM bits=0(dec), DET_DC bits=0(dec)



(b) RSSIDAC_LOLIM bits=130(dec), DET_DCbits=19(dec)

Figure 68 RSSI DAC Output Voltage

13.8.16. Noise Squelch Function

The noise squelch function detects the noise level, which is output when there is no signal to the FM detection circuit. The AK2404 has two noise squelch circuits (NSQ1 and NSQ2), which operate by setting <Address0x59>NSQ1_ON bit = “1” and <Address0x5B>NSQ2_ON bit = “1” respectively. The block diagram is shown in the Figure 69 (the NSQ1 and NSQ2 are the same circuit). The noise squelch function uses the programmable 4th order IIR filter to detect the noise level from the FM received signal demodulated by the FM detection circuit. After that, the noise level is converted to demodulated noise power by the full-wave rectification, averaging and LOG conversion circuits. The converted noise power is judged as “H/L” and output from the NSQ1 or NSQ2 pins.

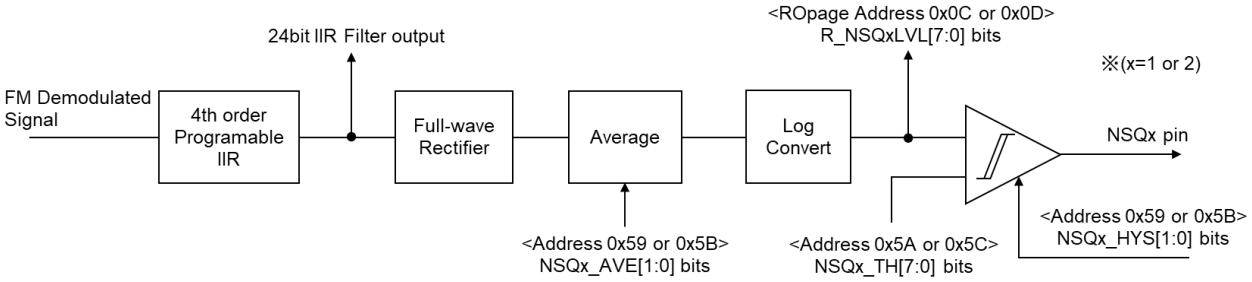


Figure 69 Noise Squelch Circuit Block Diagram

Set the coefficients of BPF or HPF to the 4th order IIR filter. The frequency characteristic of the filter can be verified by setting <Address0x79>RXDTO bits = “1011” to test output via serial signal from the ADFS, ADSDO and ADSCLK. The number of averaging is set by <Address0x59>NSQ1_AVE[1:0] bits and <Address0x5B>NSQ2_AVE[1:0] bits.

The 8-bit signal power after LOG conversion can be read from <ROpage Address 0x0C> R_NSQ1LVL[7:0] bits and <ROpage Address0x0D>R_NSQ2LVL[7:0] bits. The calculated 8-bit output code is compared with <Address0x5A>NSQ1_TH[7:0] bits or <Address0x5C>NSQ2_TH[7:0] bits by the next stage comparator, and judged as “H/L” and output from the NSQ1 or NSQ2 pins. The “H/L” transition of the comparison output is calculated by the following formula with the hysteresis operation set by <Address0x59>NSQ1_HYS bits and <Address0x5B>NSQ2_HYS bits. If the NSQ1_TH or NSQ2_TH is set by a value less than the hysteresis width, the “H->L” comparison value becomes to “0”.

L → H : R_NSQxLVL bits > NSQx_TH bits
H → L : R_NSQxLVL bits ≤ NSQx_TH bits – NSQx_HYS Setting Value (x= 1 or 2)

To use this function in an actual system, first verify the FM demodulated noise level in the no input state and the noise level at FM signal reception by the R_NSQxLVL bits, and then set the NSQx_TH bits to an appropriate value. The noise power changes as 0.25dB/code.

13.8.17. IIR Filter

A 3rd order programmable filter is equipped in the Out of Band Power Monitoring function and a 4th order programmable filter is equipped in the noise squelch function (NSQ). The filter type (LPF, BPF, HPF) can also be designed freely because the coefficients are arbitrarily set. The Figure 70 shows the filter block diagram in the Out of Band Power Monitoring and the Figure 71 shows the filter block diagram in the NSQ. Set the coefficients with 20-bit (2.18) format for the Out of Band Power Monitoring and 16-bit (2.14) format for the NSQ.

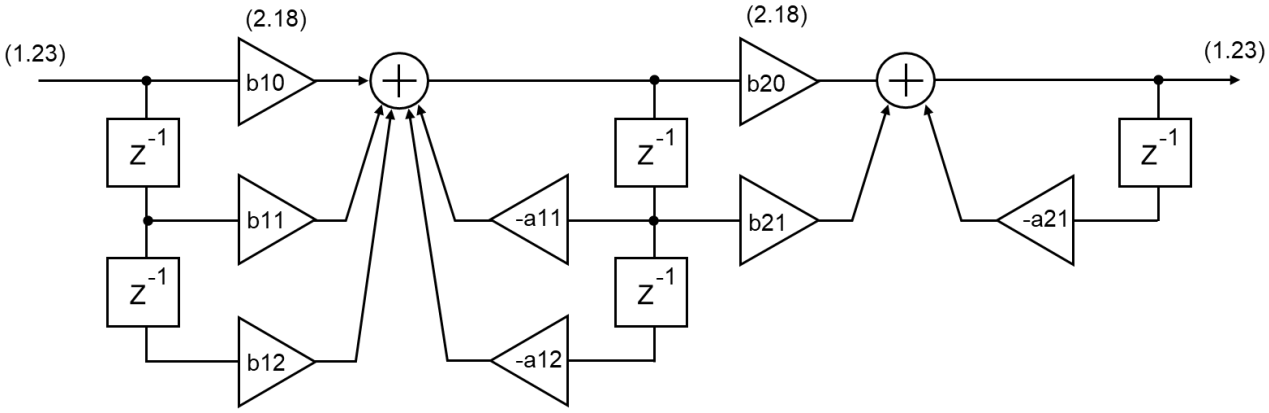


Figure 70 IIR Filter for Out of Band Power Monitoring Block Diagram

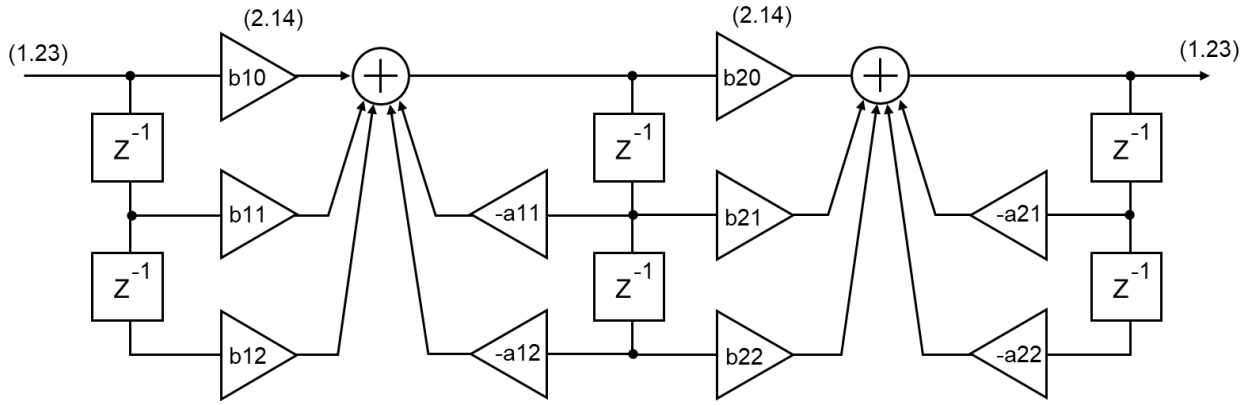


Figure 71 IIR Filter for NSQ Block Diagram

The following pages shows examples of coefficients setting and the frequency characteristics. These setting examples do not guarantee a system characteristic. Design and use an appropriate filter for the system in use. It is recommended that the minimum cut off frequency is greater than or equal to 1kHz if the LPF is used.

■ Example of Out of Band Power Monitoring IIR LPF
Sampling Rate = 192kHz

Table 26 Coefficient of Out of Band Power Monitoring IIR LPF

Coef.	Fc=1.0kHz		Fc=2.5kHz		Fc=6.25kHz	
	DEC	HEX	DEC	HEX	DEC	HEX
B10	50	00032	303	0012F	1780	006F4
B11	99	00063	606	0025E	3561	00DE9
B12	50	00032	303	0012F	1780	006F4
A11	515573	7DDF5	502022	7A906	466033	71C71
A12	-253705	C20F7	-241562	C5066	-213809	CBCCF
B20	4895	0131F	11956	02EB4	28314	06E9A
B21	4895	0131F	11956	02EB4	28314	06E9A
A21	253703	3DF07	241529	3AF79	213347	34163

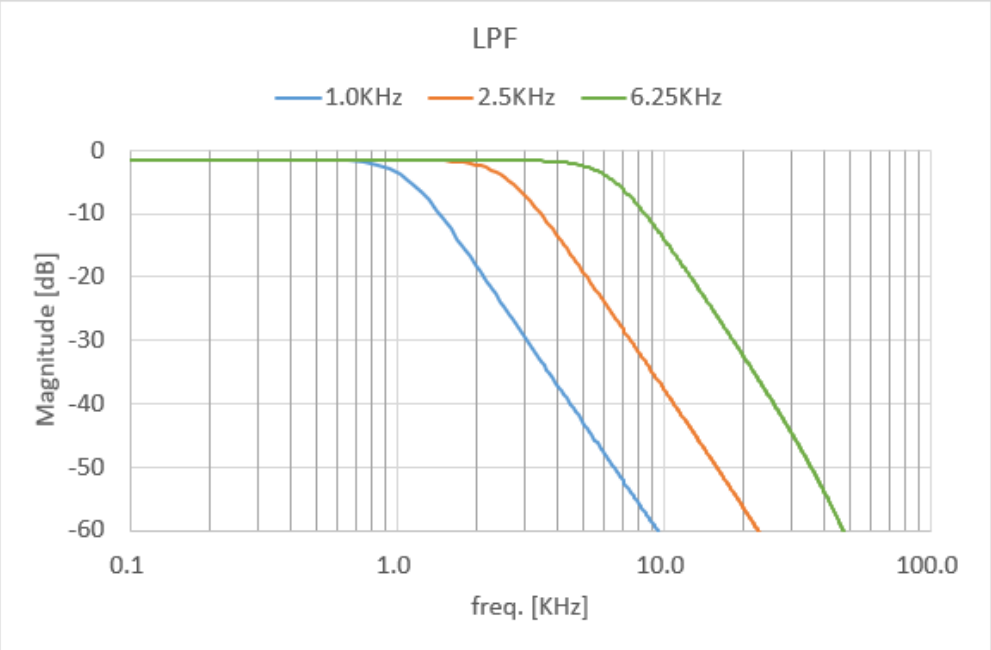


Figure 72 Out of Band Power Monitoring IIR LPF Filter Frequency Characteristics

■ Example of NSQ IIR BPF
Sampling Rate = 96kHz

Table 27 Coefficient of NSQ IIR BPF

Coef.	Center Frequency = 20kHz		Center Frequency = 25kHz		Center Frequency = 30kHz	
	DEC	HEX	DEC	HEX	DEC	HEX
B10	575	023F	594	0252	579	0243
B11	0	0000	0	0000	0	0000
B12	-575	FDC1	-594	FDAE	-579	FDBD
A11	6700	1A2C	-600	FDA8	-10635	D675
A12	-14918	C5BA	-14931	C5AD	-14909	C5C3
B20	1320	0528	1265	04F1	1319	0527
B21	0	0000	0	0000	0	0000
B22	-1302	FAEA	-1265	FB0F	-1319	FAD9
A21	9513	2529	-3497	F257	-13338	CBE6
A22	-14953	C597	-14940	C5A4	-14962	C58E

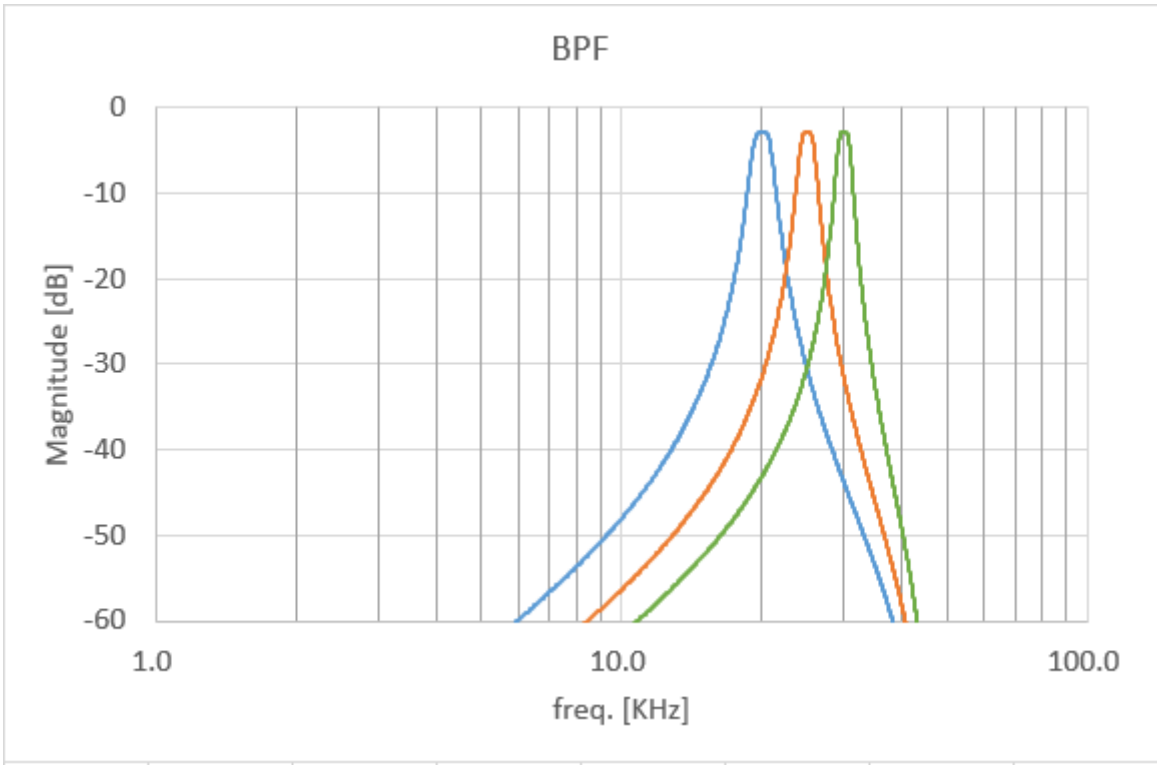


Figure 73 NSQ IIR BPF Filter Frequency Characteristics

■ Example of NSQ IIR HPF
Sampling Rate = 96kHz

Table 28 Coefficient of NSQ IIR HPF

Coef.	Fc = 20kHz		Fc = 25kHz		Fc = 30kHz	
	DEC	HEX	DEC	HEX	DEC	HEX
B10	3706	0E7A	2677	0A75	2004	07D4
B11	-7412	E30C	-5355	EB15	-4008	F058
B12	3706	0E7A	2677	0A75	2004	07D4
A11	6192	1830	-1551	F9F1	-9264	DBD0
A12	-7540	E28C	-7329	E35F	-7875	E13D
B20	6574	19AE	5181	143D	3460	0D84
B21	-13149	CCA3	-10362	D786	-6919	E4F9
B22	6574	19AE	5181	143D	3460	0D84
A21	4482	1182	-1115	FBA5	-6765	E593
A22	-932	FC5C	-666	FD66	-1294	FAF2

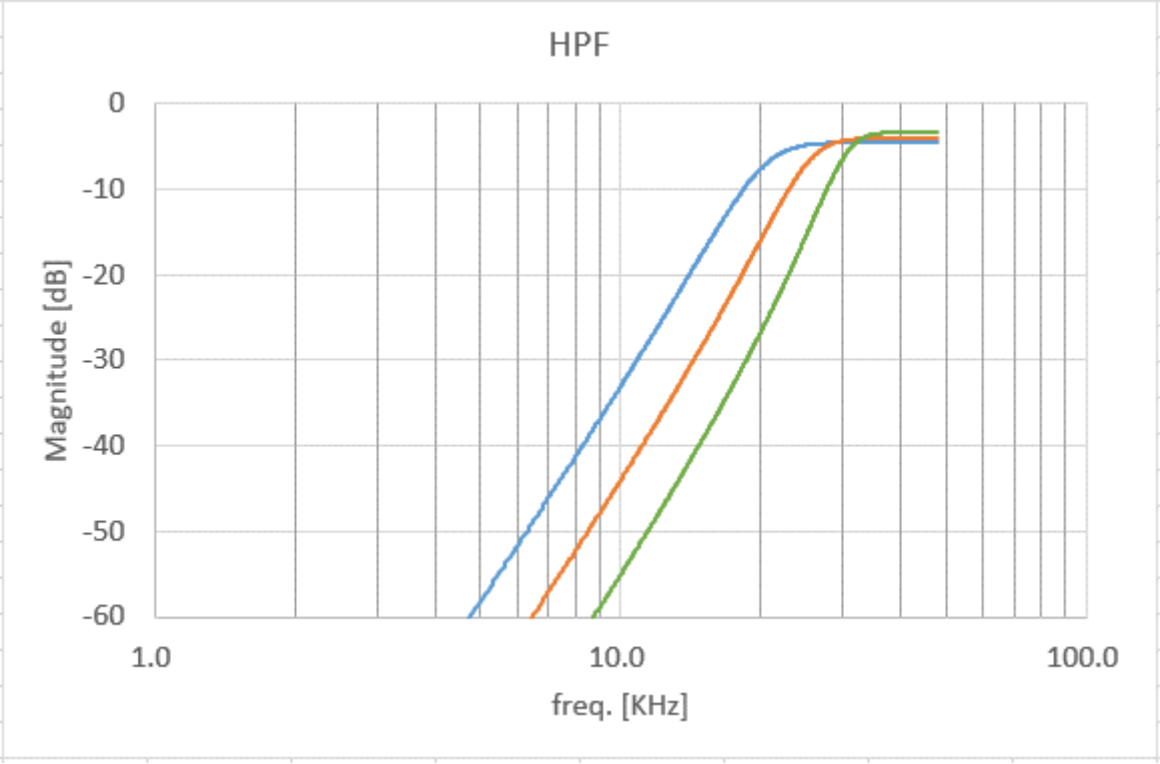


Figure 74 NSQ IIR HPF Filter Frequency Characteristics

13.8.18. Output Sampling Rate

Since the channel filter operates at different frequency according to the setting by <Address0x41> DFIL_PATH[1:0] bits, the output sampling rate is different at each setting. And the sampling rate can be output at a speed reduced to 1/2 or 1/4 of the initial setting by setting <Address0x41>RXIF_SR[1:0] bits. The Table 29 shows the output sampling rate for each filter setting.

Table 29 Output Sampling Rate

DFIL_PATH		Output Sampling Rate		
[1]	[0]	RXIF_SR=00 (default)	RXIF_SR=01 (1/2 rate)	RXIF_SR=1X (1/4 rate)
0	0	MCLK/128	Prohibited	Prohibited
0	1	MCLK/256	MCLK/512	MCLK/1024
1	X	MCLK/512	MCLK/1024	MCLK/2048

13.8.19. Status Output

As described in 9.5 Serial Interface Timing for Receiving Data and Status Output Read, the AK2404 outputs the operating status of the RSSI and AGC as status bits synchronized with the received data. The Figure 75, Figure 76 and Figure 77 show the timing chart again.

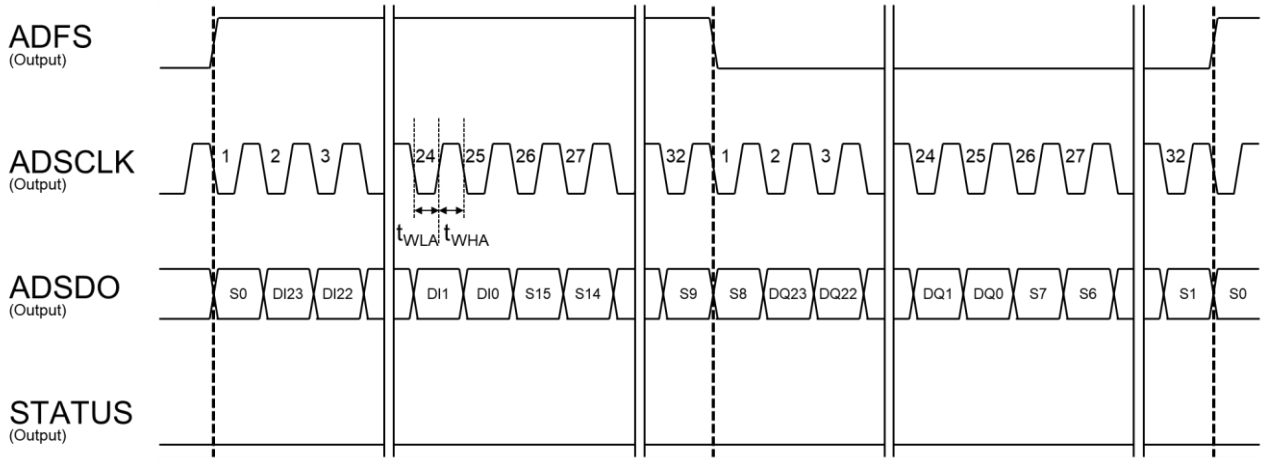


Figure 75 Interface timing for ADC data read (IQ 32-bit Mode)

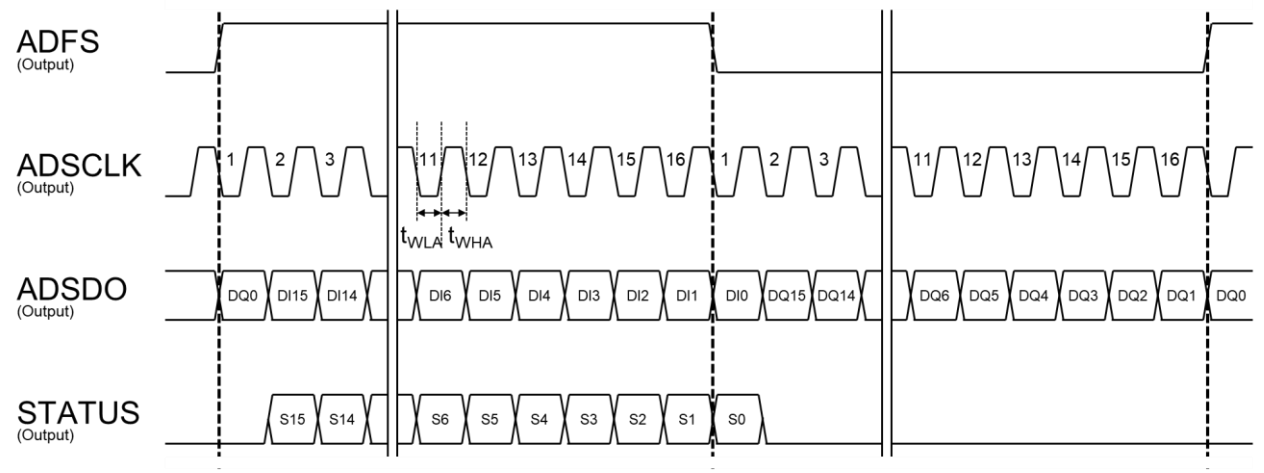


Figure 76 Interface timing for ADC data read (IQ 16-bit Mode)

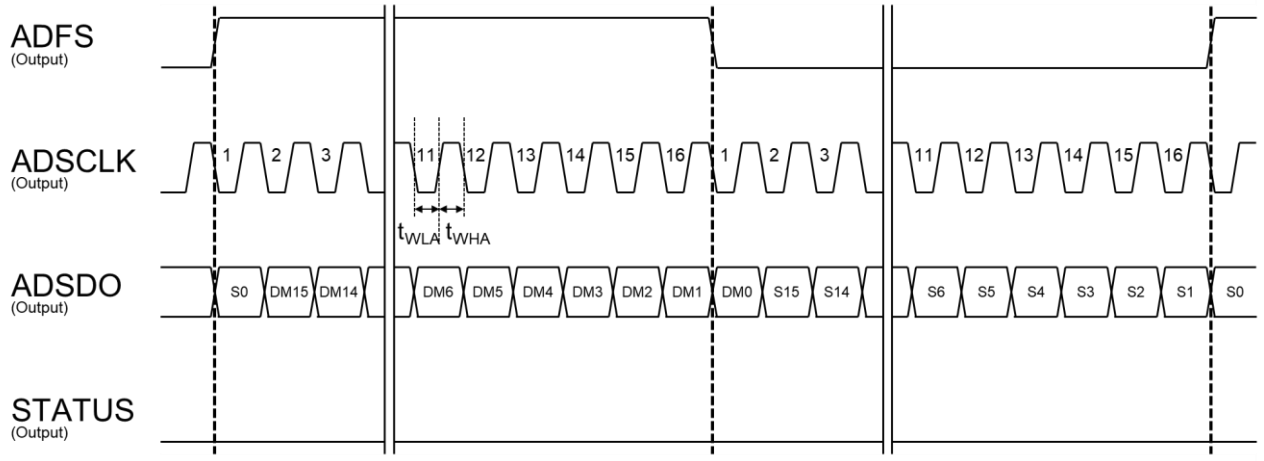


Figure 77 Interface timing for ADC data read (FMDET Mode)

The details of status bits are as follows. The S7, S1 and S0 output the status bits only when the corresponding AGC operates and output “0” when the AGC does not operate.

S15 to S8 : RSSI
The calculated results of the RSSI are output. The value to be output is set by <Address0x3E> STS_RSSI_SEL bits as follows. However, if the subtraction result is less than 0 code, the 0 code is output.

“00” : <ROpage Address0x06>R_RSSI bits
“01” : <ROpage Address0x07>R_OOBL_RSSI bits minus R_RSSI bits
“1x” : <ROpage Address0x08>R_OOBR_RSSI bits minus R_RSSI bits

S7 : Digital Output AGC Status
This status determines the operating status of the digital output AGC. “0” is output during outputting the LSB side of the received data and “1” is output during outputting the MSB side. This status bit is only effective when <Address0x3E>DAGC_ON bit = “1” is set and outputs the same value as read back value of the <ROpage Address0x04>R_DAGC_STS bit.

S6 : Status to indicate LNA and ATT operation
This status determines whether the current status is operating in the LNA or ATT. “0” is output when the LNA operates and “1” is output when the ATT operates. “0” is output when both of the LNA and ATT are powered down. The same value is output as read back value of the <ROpage Address0x04> R_ATT_STS bit.

S5 to S3 : If <Address0x6F>PD_ATT_N bit = “0” and PD_LNA_N bit = “1”, “0” is output. “1” is output for other setting.

S2 : “0” is output.

S1 : PGA Gain increasing Flag
“1” is output when the PGA gain is increased. The interval to output “1” is one sample of the output sampling rate. The timing to output “1” depends on the setting of <Address0x30>AGC_KPMODE bits. This status bit is valid only when the <Address0x30>PGA_AGCON bit = “1” is set.

When AGC_KPMODE bit = “0”
“1” is output at the timing when the gain is changed.

When AGC_KPMODE bit = “1”
“1” is output if it is judged that the gain is changed at the timing of changing to AGC_KEEP pin = “H” or AGC_KPREG bit = “1”. The actual gain change is reflected in the PGA gain setting when change to AGC_KEEP pin = “L” or AGC_KPREG bit = “0” next.

S0 : PGA Gain Decreasing Flag
“1” is output when the PGA gain is decreased. The interval to output “1” is same as the PGA gain increasing flag S1. This status bit is effective only when <Address0x30>PGA_AGCON bit = “1” is set.

13.8.20. Test Output Function of Internal Node

Setting <Address0x79>RXDTO bits outputs the internal node of the receiving digital circuit to the ADFS, ADSCLK and ADSDO pins by 3-wired serial format (Table 30). This function is intended for debugging purpose.

Table 30 Test Output Setting of Receiving Path

RXDTO (dec)	TESTOUT	Data format	DFIL_PATH		
			00	01	1x
0	Normal output	24-bit signed I/Q	128	256	512
1	FIR3 output	**23-bit** signed I/Q	128	256	512
2	FIR4 output	**23-bit** signed I/Q	256	512	1024
3	FIR5 output	**23-bit** signed I/Q	512	1024	2048
4	OFSCAL output (main path)	24-bit signed I/Q	128	256	512
5	Complex mixer (Low_IF -> Zero_IF) output	24-bit signed I/Q	128	256	512
6	Out of Band Power Monitoring Rside complex mixer output	24-bit signed I/Q	128	256	512
7	Out of Band Power Monitoring Lside complex mixer output	24-bit signed I/Q	128	256	512
8	Out of Band Power Monitoring Rside IIR output	24-bit signed I/Q	128	256	512
9	Out of Band Power Monitoring Lside IIR output	24-bit signed I/Q	128	256	512
10	OFSCAL output (Out of Band Power Monitoring path)	24-bit signed I/Q	128	256	512
11	NSQ IIR output	24-bit signed I:NSQ1, Q:NSQ2	128	256	512
12	Not assign (“0” output)	-	128	256	512
13	Not assign (“0” output)	-	128	256	512
14	Not assign (“0” output)	-	128	256	512
15	Not assign (“0” output)	-	128	256	512

The test outputs for the decimation filter are executed by setting RXDTO bits = 0 to 3(dec). At this time, set the <Address0x41>DFIL_PATH bits to the filter to be desired to output. The test outputs after DC offset calibration are provided by setting RXDTO bits = 4,10(dec). It is possible to verify that the DC offset is removed as intended.
The complex mixer (Low_IF -> Zero_IF) is test output by setting RXDTO bits = 5(dec). For example, since the system DC offset is down converted to the NCO frequency (Δ1), it is possible to verify that the frequency conversion is executed as intended.
The complex mixer and IIR of the Out of Band Power Monitoring are test output by setting RXDTO bits = 6 to 9(dec). It is possible to verify the frequency conversion by the NCO frequency (Δ1±Δ2) and the frequency characteristic after setting the IIR coefficient.
The IIR of the NSQ is test output by setting RXDTO bits = 11(dec). It is possible to verify the frequency characteristic after setting the IIR coefficient. Since the NSQ is a signal after FM demodulation, the frequency characteristic can be observed by executing the FFT for the FM demodulated noise at no input.

This function becomes effective when the <Address0x41>ADIFSEL[1:0] bits are set to “00” or “01”. If ADIFSEL bits = “01” is set, the data which is less than 24-bit is formatted to 24-bit by extending the bit on the MSB side and then the 16-bit selected by the <Address0x3E>DFILOUT[2:0] bits is output. The saturation processing is executed on the MSB side and truncation processing is executed on the LSB side at output. At this time, the digital AGC described in 13.8.11 Digital Output AGC Function becomes invalid.

The output sampling rate depends on the DFIL_PATH setting and the frequency is calculated by dividing the master clock (f_{MCLK}) by the value on the column of the DFIL_PATH in the Table 30. It is possible to output at a speed reduced to 1/2 or 1/4 by setting the <Address0x41>RXIF_SR[1:0] bits same with the normal output. At this time, note the folded components of the signal due to the aliasing and execute a setting.

13.9. Transmit Data Generation Circuit (MODDAC, SMF)

The AK2404 has a 12-bit DAC (MODDAC) and the data is input via the MOD S/P IF. It is used for the VCO direct modulation and also be able to compose the two-point modulation with the PLL synthesizer modulation function described in 13.7.5 Frequency Offset Adjustment and Modulation function. The Figure 78 shows the block diagram of the MODDAC.

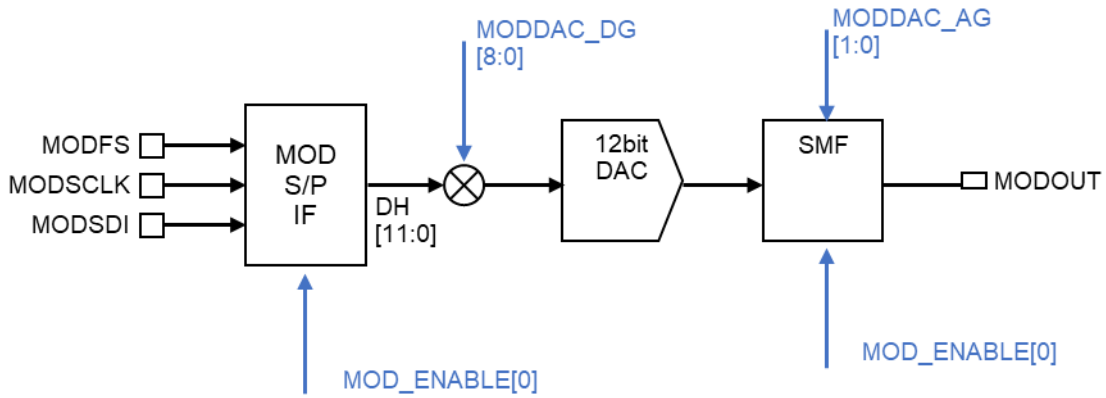


Figure 78 MODDAC Configuration

The input data to the MODDAC is enabled when setting <Address0x21>MOD_ENABLE[0] bit = "1". When the MOD_ENABLE[0] bit is set to "0", the previous input data is retained and the MODOUT pin becomes Hi-Z output.

The Hch signal input from the MOD I/F described in chapter 9.6 is input to the MODDAC and converted to an analog signal after the gain is adjusted in the range of 0.25 time to 1 time by setting <Address 0x20 to 21> MODDAC_DG[8:0] bits. The gain is calculated by the following formula. And the Table 31 shows the setting example.

$$MODDAC\ Digital\ Gain\ = \begin{cases} 20\log\left(\dfrac{MODDAC\_DG+1}{512}\right)\ [dB] & if\ 127 \le MODDAC\_DG \le 511 \\ 20\log\ (0.25)\ \ [dB] & if\ 0 \le MODDAC\_DG < 127 \end{cases}$$

Table 31 MODDAC Digital Gain

MODDAC_DG (dec)	Input Gain	Unit
0	-12.0412	dB
1	-12.0412	
・・・	・・・	
127	-12.0412	
128	-11.9736	
129	-11.9065	
・・・	・・・	
509	-0.034	
510	-0.01698	
511	0	

It takes 16 × $t_{MODSCLK}$ from the time the MOD I/F data is fixed until the MODDAC receives the data. The $t_{MODSCLK}$ is the period of the MODSCLK. And stop the access to the MOD I/F when changing the value of MOD_ENABLE[0] bit and MODDAC_DG bits. (Fix the MODSCLK pin to “L”.)

The converted analog signal is input to the Smoothing Filter (SMF) to attenuate the folded noise generated during D-A conversion, and then output from the MODOUT pin. It is possible to adjust the SMF gain with the setting of <Address0x21>MODDAC_AG[1:0] bits as described in the Table 32. The Figure 79 shows the frequency characteristic of the SMF.

Table 32 MODDAC Output Gain

MODDAC_AG		Output Gain	Unit
[1]	[0]		
0	0	0	dB
0	1	-6	
1	0	-12	
1	1	Prohibited	

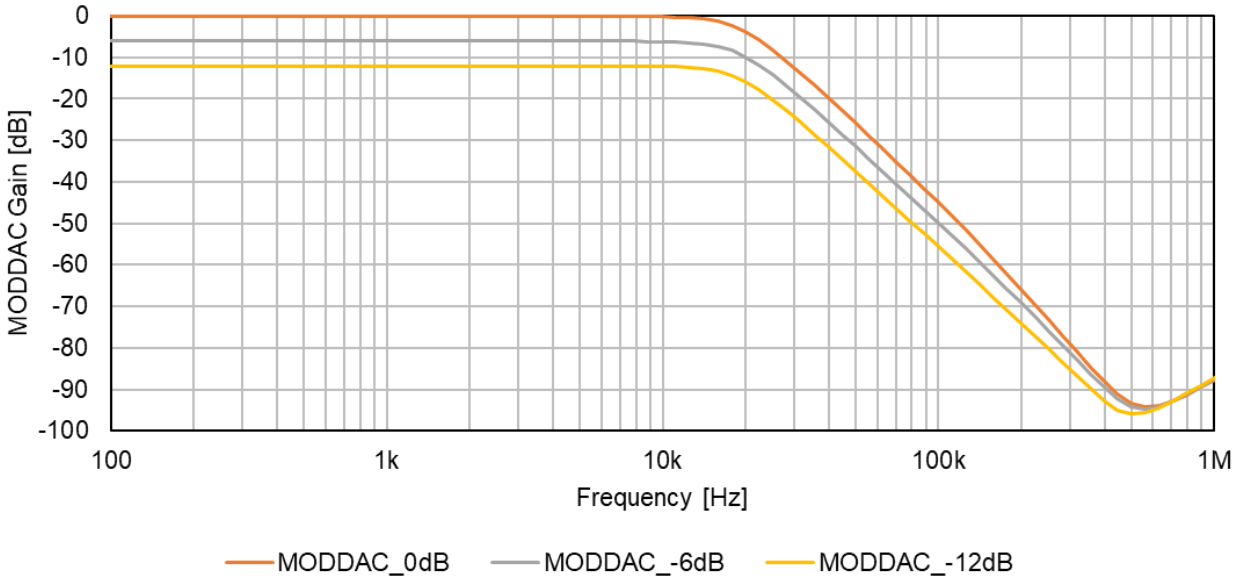


Figure 79 MODDAC SMF Frequency Characteristics

13.10. Transmit Preamplifier Circuit (DRIVER AMP)

The transmit preamplifier circuit (DRIVER AMP) amplifies and outputs a signal divided by N with the LOCAL DIVIDER. It is assumed to be used as a transmit signal output if the configuration is to execute the modulation to the external VCO. The output level is set by the <Address0x22>TXOLV bits. The external parts are the values when the parts shown in the chapter 15 External Circuit are used. Warn that the phase noise deteriorates at low output level setting.

13.11. Internal Low Voltage Generator Circuit (LDO)

The AK2404 has internal low voltage generator circuit (LDO). The internal LDO is enabled or disabled by the INTLDOPD pin. Refer to the chapter 12.1 Power-up Sequence or details of the startup sequence of each mode. The INTLDOPD pin is assumed to be fixed at “H” (PLLVDD) or “L” (VSS) according to the purpose to use. The use to switch the polarity after power-up is not assumed.

The internal LDO is used when setting INTLDOPD pin=”L”. Connect the VREF1 pin to VSS via the 10μF capacitor if the internal LDO is used. Since the internal LDO is used for the internal circuit in the AK2404, do not use it to supply the power for the external elements except the AK2404.

If the INTLDOPD pin = “H” is set, the power supply voltage is externally supplied to the VREF1 pin without using the internal LDO. Refer to 8 Recommended Operating Conditions for the recommended supplied voltage and refer to 10.3 Current Consumption for details of the power consumption during power supply.

14. Register Map and Detailed Description

14.1. Register Map

■ CLOCK/PLL

Name	Address	D7	D6	D5	D4	D3	D2	D1	D0
TCXO / *K	0x01	DEN_RATIO[1:0]		X	X	X	TCXO_SET[2:0]		
OFS_ RDOC	0x02	OFS_RDOC[15:8]							
	0x03	OFS_RDOC[7:0]							
OFS_ FINE	0x04	OFS_FINE[15:8]							
	0x05	OFS_FINE[7:0]							
OFS_ DEN	0x06	X	OFS_DEN[22:16]						
	0x07	OFS_DEN[15:8]							
	0x08	OFS_DEN[7:0]							
PLL_R	0x09	PLL_R[7:0]							
FRAC	0x0A	X	FRAC[22:16]						
	0x0B	FRAC[15:8]							
	0x0C	FRAC[7:0]							
MOD	0x0D	X	MOD[22:16]						
	0x0E	MOD[15:8]							
	0x0F	MOD[7:0]							
INT	0x10	X	X	X	X	DUM_L	INT[10:8]		
	0x11	INT[7:0]							
DSM	0x12	TEST_1[3:0]				X	X	X	DSM_AT _INT
FAST	0x13	FAST_TIME[7:0]							
CP	0x14	CP_ POLA	CPOF[1:0]		CPFINE[4:0]				
	0x15	X	X	X	CPFAST[4:0]				
PLL	0x16	CPO_PDST[1:0]		FASTEN	CPHIZ	LD_ MODE	LD_ RDOC	LD_SEL[1:0]	
LDCNT	0x17	LD_LOCKCNT[7:0]							
	0x18	LD_UNLOCKCNT[7:0]							
DUMMY	0x19	X	X	X	X	X	X	X	X

■ ANALOG

RX	0x1A	PDET_ LPF_P	X	X	RXLPF_ FC	IQ_SEL	ANA_ PATH	MAIN_ PATH	LPMODE _LNA
LOCAL1	0x1B	X	X	X	HPMODE _LOBLK	X	X	DIVSEL[1:0]	
	0x1C	X	TEST_2[2:0]			TEST_3[1:0]		TEST_4[1:0]	
PHASE ADJ	0x1D	X	PH_ADJ_LP[6:0]						
	0x1E	X	PH_ADJ_HP[6:0]						
LOCAL2	0x1F	X	X	X	X	TEST_5[1:0]		TEST_6[1:0]	
TX	0x20	MODDAC_DG[8:1]							
	0x21	MODDAC _DG[0]	X	X	X	MODDAC_AG[1:0]		MOD_ENABLE[1:0]	
	0x22	X	X	X	X	X	X	TXOLV[1:0]	
DUMMY	0x23	X	X	X	X	X	X	X	X

■ OFCAL

OFCAL	0x24	CAL RFPD	X	OFS2REG[1:0]		X	X	OFSCAL2	OFSCAL1
	0x25	X	X	OFSTA_I[5:0]					
	0x26	X	X	OFSTA_Q[5:0]					
OFCAL _DIG	0x27	X	X	X	X	FIROFS_AVE[1:0]		AGCOFS_AVE[1:0]	
	0x28	OFSTD_I[23:16]							
	0x29	OFSTD_I[15:8]							
	0x2A	OFSTD_I[7:0]							
	0x2B	OFSTD_Q[23:16]							
	0x2C	OFSTD_Q[15:8]							
	0x2D	OFSTD_Q[7:0]							
DUMMY	0x2E	X	X	X	X	X	X	X	X

■ AGC

PDET & AGC	0x2F	AGC_KPDLY[7:0]							
	0x30	X	X	X	AGC_ KPMODE	AGC_ KPREG	AGC_ KPSEL	DUM_L	PGA_ AGCON
	0x31	X	X	X	X	X	X	X	X
	0x32	X	X	X	X	X	X	X	X
	0x33	PDET_OFS[3:0]				X	X	ATTLVL[1:0]	
AGC _DIG	0x34	AGCHPF_FC[3:0]				X	X	AGCHPF _KEEP	AGCHPF SEL
	0x35	X	X	PGAGAIN[5:0]					
	0x36	X	AGCMAX[2:0]			AGCTGT[3:0]			
	0x37	AGCHYS[1:0]		AGCLIM[5:0]					
	0x38	AGCTIM[3:0]				AGCTRW[3:0]			
	0x39	DUM_H	X	X	X	X	X	X	X
	0x3A	X	X	X	X	X	X	X	X
	0x3B	X	X	X	X	X	X	X	X
	0x3C	X	X	X	X	X	X	X	X
	0x3D	X	X	X	X	X	X	X	X
	0x3E	STS_RSSI_SEL[1:0]		DFILOUT[2:0]			DAGC _HYS[1:0]		DAGC _ON
	0x3F	DAGC_TH[7:0]							
DUMMY	0x40	X	X	X	X	X	X	X	X

■ DIGITAL

DIG_ MODE	0x41	X	X	ADIFSEL[1:0]		RXIF_SR[1:0]		DFIL_PATH[1:0]
DFIL_ SET	0x42	COEF_SET[7:0]						
NCO MIXER	0x43	DELTA1F[7:0]						
	0x44	DELTA2F[7:0]						
	0x45	NCO_ SET	X	X	X	UPMIX_ OFF	DWMIX_ OFF	ROM_UPDATE[1:0]
PRE_ HPF	0x46	PRE_HPF_FC[3:0]				X	PRE_HP F_KEEP	PRE_HPFSEL[1:0]
MIXER_ ATT	0x47	DWMIXATT[13:6]						
	0x48	DWMIXATT[5:0]						DWMIXATT_SET[1:0]
DUMMY	0x49	X	X	X	X	X	X	X	X
CH FILTER	0x4A	X	PFIL_SAT[2:0]			X	CHCOEF_SEL[1:0]		COEF LOAD
DUMMY	0x4B	X	X	X	X	X	X	X	X

■ DIGITAL (continue)

RSSI	0x4C	X	X	X	X	X	RSSI_AVE[2:0]		
	0x4D	RSSI_OFST[7:0]							
	0x4E	RSSI_ATT[7:0]							
DUMMY	0x4F	X	X	X	X	X	X	X	X
Output of Outband Power Monitoring	0x50	X	X	X	X	OOB_PAVE[2:0]			OOB_ON
	0x51	RSSI_L_OFST[7:0]							
	0x52	RSSI_R_OFST[7:0]							
DUMMY	0x53	X	X	X	X	X	X	X	X
FMDET	0x54	X	RSSI_DETOUT	REG_DETOUT	X	X	X	FMDET_G[1:0]	
	0x55	RSSIDAC_LOLIM[7:0]							
	0x56	IF_OFST[23:16]							
	0x57	IF_OFST[15:8]							
	0x58	IF_OFST[7:0]							
NSQ	0x59	NSQ1_HYS[1:0]		NSQ1_AVE[1:0]		X	X	X	NSQ1_ON
	0x5A	NSQ1_TH[7:0]							
	0x5B	NSQ2_HYS[1:0]		NSQ2_AVE[1:0]		X	X	X	NSQ2_ON
	0x5C	NSQ2_TH[7:0]							
FMDET2	0x5D	DET_DC[7:0]							
DUMMY	0x5E	X	X	X	X	X	X	X	X
POST_HPF	0x5F	POST_HPF_FC[3:0]				X	X	POST_HPF_KEEP	POST_HPFSEL
DUMMY	0x60	X	X	X	X	X	X	X	X
	0x61	X	X	X	X	X	X	X	X
RDOC	0x62	X	RDOC_1	RDOC_KEEP	RDOC_2[1:0]		RDOC_3[1:0]		RDOC_ON
	0x63	X	RDOC_4	RDOC_5[1:0]		X	RDOC_6[1:0]		RDOC_7
	0x64	X	RDOC_8[2:0]			X	RDOC_9[1:0]		RDOC_10
	0x65	RDOC_11[1:0]		RDOC_12[1:0]		X	RDOC_13[1:0]		RDOC_14
	0x66	RDOC_15[1:0]		X	X	X	X	RDOC_18[1:0]	
	0x67	X	X	X	RDOC_19	X	RDOC_20[1:0]		RDOC_21
	0x68	X	X	X	X	X	RDOC_22[1:0]		RDOC_FM
	0x69	X	RDOC_23[1:0]		RDOC_24[1:0]		RDOC_25[2:0]		
	0x6A	RDOC_26[7:0]							
	0x6B	RDOC_16[7:0]							
	0x6C	RDOC_17[7:0]							

■ DIGITAL (continue)

PD	0x6D	X	X	X	PD_ MULTI_N	X	PD_CLK BUF_N	PD_REF_N	X
	0x6E	X	X	X	X	X	PD_MOD DAC_N	PD_PLL_N	PD_TX_N
	0x6F	X	DUM_L	PD_DET DAC_N	PD_ PDET_N	PD_ATT_N	PD_LNA_N	PD_ ADC_N	PD_RX_N

■ PDET ADDITIONAL OFFSET

PDET	0x74	DUM_L	DUM_L	DUM_L	DUM_L	DUM_L	DUM_L	DUM_L	PDET_O FF

■ PRE TEST FUNCTION

CURRENT	0x75	X	I_AAF	I_PGA[1:0]		X	X	X	TEST_7
RESERV ED	0x76	X	X	X	X	X	X	X	X
	0x77	X	X	X	X	X	X	X	X
	0x78	X	X	X	X	X	X	X	X
DEBUG	0x79	X	X	X	X	RXDTO[3:0]			
	0x7A	X	X	X	X	X	X	X	X

■ SOFTWARE RESET & PAGE

PAGE	0x7D	PAGE[7:0]
SOFT RESET	0x7E	SRST[7:0]

■ READ BACK ONLY (ROpage : PAGE bits = 46(hex))

DUMMY	0x01	X	X	X	X	X	X	X	X
	0x02	X	X	X	X	X	X	X	X
READ COEF	0x03	X	R_COEF STS_OOB	R_COEF STS_NSQ2	R_COEF STS_NSQ1	R_COEF STS4	R_COEF STS3	R_COEF STS2	R_COEF STS1
STATUS	0x04	R_DAGC _STS	R_ATT _STS	X	X	X	X	X	X
DUMMY	0x05	X	X	X	X	X	X	X	X
READ RSSI	0x06	R_RSSI[7:0]							
READ OOB_L	0x07	R_OOBL_RSSI[7:0]							
READ OOB_R	0x08	R_OOBR_RSSI[7:0]							
DUMMY	0x09	X	X	X	X	X	X	X	X
RSSI_BB	0x0A	R_RSSI_BB[7:0]							
DUMMY	0x0B	X	X	X	X	X	X	X	X
READ NSQ1	0x0C	R_NSQ1LVL[7:0]							
READ NSQ2	0x0D	R_NSQ2LVL[7:0]							
READ PGA	0x0E	X	X	R_PGA[5:0]					
DUMMY	0x0F	X	X	X	X	X	X	X	X

■ READ BACK ONLY (ROpage, continue)

READ ANA OFST	0x10	X	X	R_OFSTA_I[5:0]					
	0x11	X	X	R_OFSTA_Q[5:0]					
READ DIG OFST_I	0x12	R_OFSTD_I[23:16]							
	0x13	R_OFSTD_I[15:8]							
	0x14	R_OFSTD_I[7:0]							
READ DIG OFST_Q	0x15	R_OFSTD_Q[23:16]							
	0x16	R_OFSTD_Q[15:8]							
	0x17	R_OFSTD_Q[7:0]							
READ DIG OFST_I (OOB)	0x18	R_OFSTD_OOBI[23:16]							
	0x19	R_OFSTD_OOBI[15:8]							
	0x1A	R_OFSTD_OOBI[7:0]							
READ DIG OFST_Q (OOB)	0x1B	R_OFSTD_OOBQ[23:16]							
	0x1C	R_OFSTD_OOBQ[15:8]							
	0x1D	R_OFSTD_OOBQ[7:0]							
READ AGC OFST_I	0x1E	X	X	X	X	X	X	X	X
	0x1F	R_AGCOFS_I[15:8]							
	0x20	R_AGCOFS_I[7:0]							
READ AGC OFST_Q	0x21	X	X	X	X	X	X	X	X
	0x22	R_AGCOFS_Q[15:8]							
	0x23	R_AGCOFS_Q[7:0]							
READ RDOC OFST_I	0x24	R_RDOC_I[23:16]							
	0x25	R_RDOC_I[15:8]							
	0x26	R_RDOC_I[7:0]							
READ RDOC OFST_Q	0x27	R_RDOC_Q[23:16]							
	0x28	R_RDOC_Q[15:8]							
	0x29	R_RDOC_Q[7:0]							

* X : Do not care

14.2. Special Register Access

The registers at the following addresses have restrictions on writing.

■ **<Address0x04 to 0x05>OFS_FINE bits**
This register must be written to both of <Address0x04, 0x05>. And this register becomes effective at the timing when the <Address0x05> is written.

■ **<Address0x06 to 0x08>OFS_DEN bits**
This register must be written to all <Address0x06, 0x07, 0x08>. And this register becomes effective at the timing when the <Address0x08> is written.

■ **<Address0x09 to 0x11> PLL frequency setting related registers**
The <Address0x09 - 0x11> are registers related to the PLL frequency setting. It is necessary to write to all <Address0x09, 0x0A, 0x0B, 0x0C, 0x0D, 0x0E, 0x0F, 0x10, 0x11> when the frequency is set. And this register becomes effective at the timing when the <Address0x11> is written.

■ **<Address0x28 to 0x2A>OFSTD_I bits**
This register must be written to all <Address0x28, 0x29, 0x2A>. And this register becomes effective at the timing when the <Address0x2A> is written.

■ **<Address0x2B to 0x2D>OFSTD_Q bits**
This register must be written to all <Address0x2B, 0x2C, 0x2D>. And this register becomes effective at the timing when the <Address0x2D> is written.

■ **<Address0x47 to 0x48> DWMIXATT bits**
This register must be written to all <Address0x47, 0x48>. And this register becomes effective at the timing when the <Address0x48> is written.

14.3. CLOCK/PLL

Also refer to the chapter 13.7 PLL SYNTHESIZER.

14.3.1. <0x01>TCXO / *K

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x01	DEN_RATIO[1:0]		X	X	X	TCXO_SET[2:0]			W/R
Initial value	0	1				0	0	0	

DEN_RATIO[1:0] : Coefficient setting multiplied to the frequency offset value
The coefficient which is multiplied to the frequency offset value used for the frequency offset function of the PLL synthesizer is set. This function is assumed to be used for correcting the number of division of the LO DIVIDER. The Table 33 shows the coefficient set by the register.

Table 33 DEN_RATIO

DEN_RATIO		Coefficient
[1]	[0]	
0	0	1
0	1	2 (default)
1	0	4
1	1	8

TCXO_SET[2:0] : Frequency Conversion Setting with the CLOCK RATE CONVERTER
The input frequency to the TCXOIN pin can be frequency converted by the CLOCK RATE CONVERTER, which is used as internal master clock. Refer to 13.6 CLOCK BUFFER+CLOCK RATE CONVERTER for detail of this setting.

14.3.2. <0x02 to 08>OFS_RDOC/OFS_FINE/OFS_DEN

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x02	OFS_RDOC[15:8]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x03	OFS_RDOC[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x04	OFS_FINE[15:8]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x05	OFS_FINE[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x06	X	OFS_DEN[22:16]							W/R
Initial value		1	1	1	1	1	1	1	
0x07	OFS_DEN[15:8]								W/R
Initial value	1	1	1	1	1	1	1	1	
0x08	OFS_DEN[7:0]								W/R
Initial value	1	1	1	1	1	1	1	1	

OFS_RDOC[15:0] : Numerator Setting of the Frequency Offset Value (used for RDOC function)
Set this register in the range of -32768 (8000 (hex)) to +32767 (7FFF (hex)) with signed 16-bit. This register is only valid when setting <Address0x68>RDOC_FM bit = “1”. And refer to the chapter 13.8.9 RDOC Function about the relation between the OFS_RDOC and RDOC function.

OFS_FINE[15:0] : Numerator Setting for the Frequency Offset Value (used for AFC)
Set this register in the range of -32768 (8000 (hex)) to +32767 (7FFF (hex)) with signed 16-bit.

OFS_DEN[22:0] : Denominator Setting of the Frequency Offset Value
Set the denominator of the frequency offset value used for the frequency offset function of the PLL synthesizer. Set this register greater than or equal to 1 with unsigned 23-bit.

14.3.3. <0x09>PLL_R

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x09	PLL_R[7:0]								W/R
Initial value	0	0	0	0	0	0	0	1	

PLL_R : Divider Setting of R COUNTER
It is possible to set in the range of 1 (no divide) to 255 (divided by 255). The R COUNTER prohibits the setting of R=0. And when <Address0x16>LD_MODE bit = “0”, use under condition of $T_{MCLK} > T_{LO} \times 11$, where T_{MCLK} is the master clock and T_{LO} is the period of the input frequency of the LOIN. When <Address0x16>LD_MODE bit = “1”, setting of R = 3 or 4 is prohibited. When <Address0x16> LD_MODE bit = “1”, there are no restrictions on the master cock and LOIN frequency. Refer to the chapter 13.7.4 Lock Detection for detail.

14.3.4. <0x0A to 11>FRAC/MOD/INT

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x0A	X	FRAC[22:16]							W/R
Initial value		0	0	0	0	0	0	0	
0x0B	FRAC[15:8]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x0C	FRAC[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x0D	X	MOD[22:16]							W/R
Initial value		0	0	0	0	0	0	0	
0x0E	MOD[15:8]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x0F	MOD[7:0]								W/R
Initial value	0	0	0	0	0	0	0	1	
0x10	X	X	X	X	DUM_L	INT[10:8]			W/R
Initial value					0	0	0	0	
0x11	INT[7:0]								W/R
Initial value	0	0	1	0	0	0	0	0	

Set <Address0x10>DUM_L bit = “0”.

FRAC[22:0] : Setting the numerator of the fractional part of the division value
Set in the range of 0 ≤ FRAC < MOD(dec) with unsigned 23-bit.

MOD[22:0] : Setting the denominator of the fractional part of the division value
Set in the range of 2 ≤ MOD ≤ 8388607(dec) with unsigned 23-bit.

INT[10:0] : Setting the integer part of the division value
Set in the range of 28 ≤ INT ≤ 1920(dec) with unsigned 11-bit.

Set <Address0x10>DUM_L bit = “0”.

14.3.5. <0x12>DSM

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x12	TEST_1[3:0]				X	X	X	DSM_AT_INT	W/R
Initial value	0	0	1	0				1	

The <Address0x12>TEST_1[3:0] bits is test register. Set the initial value.

DSM_AT_INT :
When the FRAC=0 and the PLL synthesizer operates in the integer division, whether the ΔΣ operates or not is set by this register. Normally set DSM_AT_INT bit = “1”.

“0” : The ΔΣ modulator stops during the integer division operation.
“1” : The ΔΣ modulator operates during the integer division operation (default).

14.3.6. <0x13>FAST

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x13	FAST_TIME[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	

FAST_TIME[7:0] : Setting the fast timer lock function
Set the timer of the fast lock function. The loop filter switch is turned on only during the period set by the timer and the charge pump current for the fast lock set by the <Address0x15>CPFAST[4:0] bits becomes enabled. Refer to the chapter 13.7.3 Fast Lock Function for detail.

14.3.7. <0x14 to 15>CP

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x14	CP_POLA	CPOF[1:0]		CPFINE[4:0]					W/R
Initial value	0	0	0	0	0	0	0	0	
0x15	X	X	X	CPFAST[4:0]					W/R
Initial value				0	0	0	0	0	

CP_POLA : Setting the polarity of the charge pump
Set the polarity of the charge pump.

“0” : Positive (default)
“1” : Negative

CPOF[1:0] : Setting the phase offset adjustment of the phase frequency comparator
The phase noise and spurious characteristics is affected by providing the offset to the phase of the signal input to the phase frequency comparator in the PLL synthesizer during frequency lock. The characteristic may be improved by optimizing the condition. Normally set CPOF[1:0] bits = “00”.

Table 34 CPOF bits

CPOF		Phase Offset	Unit
[1]	[0]		
0	0	0 (default)	%
0	1	-11	
1	0	-20	
1	1	-27	

CPFINE[4:0] : Setting the charge pump current during normal operation
Set the charge pump current. Refer to the chapter 13.7 PLL SYNTHESIZER for detail.

CPFAST[4:0] : Setting the charge pump current during fast lock
Set the charge pump current during fast lock. Refer to the chapter 13.7 PLL SYNTHESIZER for detail. Also, refer to the chapter 13.7.3 Fast Lock Function for detail about the fast lock function.

14.3.8. <0x16>PLL

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x16	CPO_PDST[1:0]		FASTEN	CPHIZ	LD_MODE	LD_RDOC	LD_SEL[1:0]		W/R
Initial value	0	0	1	0	0	0	0	0	

CPO_PDST[1:0] : Setting the charge pump output at power down
Set the status of the charge pump output during power down. This register is effective only when the PLL and charge pump circuit are powered down with <Address0x6E>PD_PLL_N bit = “0”. Setting of CPO_PDST bits = “11” is prohibited. Normally set CPO_PDST[1:0] bits = “00”.

Table 35 CPO_PDST bits

CPO_PDST		CP Output Status
[1]	[0]	
0	0	Hi-Z (default)
0	1	“H” level
1	0	“L” level
1	1	Prohibited

FASTEN : Setting the fast lock function enable
Set enable or disable of the high-speed pull-in operation during the frequency convergence of the synthesizer.
“0” : High-speed pull-in disabled
“1” : High-speed pull-in enabled (default)

CPHIZ : Setting the charge pump output Tri-State
Set the charge pump output to Tri-State. Normally set CPHIZ bit = “0”.
“0” : Normal output (default)
“1” : Tri-State

LD_MODE : Setting the mode switching of the lock detection function
Set the mode switching of the lock detection. According to the used mode, there are different constraints under the operating condition of the lock detection circuit. Refer to the chapter 13.7.4 Lock Detection for detail.
“0” : Constrain on the master clock frequency period and LOIN frequency period condition (default)
“1” : Constrain on the division condition by the <Address0x09>PLL_R bits

LD_RDOC : Setting to switch the function of LD pin
Set the function of the LD pin (lock detection pin). Refer to the chapter 13.7.4 Lock Detection for the detail of the lock detection operation when “0” is set. And refer to the chapter 13.8.9 RDOC Function for the detail of the polarity output of the OFS_RDOC frequency switching when “1” is set. Normally set LD_RDOC bit = “0”.
“0” : Lock detect (default)
“1” : Polarity output of the OFS_RDOC frequency switching

LD_SEL[1:0] : Setting the judgement mode of the lock detection

When setting LD_RDOC bit = “0”, the judgement mode of the frequency lock output to the LD pin can be selected. “H” is output when corresponding circuit locks to the set frequency. Normally set LD_SEL[1:0] bits = “00”.

Table 36 Setting the judgement mode of the lock detection

LD_SEL		Signal to be Monitored
[1]	[0]	
0	0	PLL & CLOCK RATE CONVERTER lock (default)
0	1	PLL lock
1	0	CLOCK RATE CONVERTER lock
1	1	“H” fixed

14.3.9. <0x17 to 18>LDCNT

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x17	LD_LOCKCNT[7:0]								W/R
Initial value	0	0	1	1	1	1	1	1	
0x18	LD_UNLOCKCNT[7:0]								W/R
Initial value	0	0	1	1	1	1	1	1	

LD_LOCKCNT[7:0] : Setting the lock detection accuracy
LD_UNLOCKCNT[7:0] : Setting the unlock detection accuracy
Set the number of judgement in the lock / unlock detection mode. Both of LD_LOCKCNT bits and LD_UNLOCKCNT bits prohibit the setting of all 0. Refer to the chapter 13.7.4 Lock Detection for detail.

14.4. ANALOG

14.4.1. <0x1A>RX

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x1A	PDET_LPF_P	X	X	RXLPF_FC	IQ_SEL	ANA_PATH	MAIN_PATH	LPMODE_LNA	W/R
Initial value	0			0	0	0	1	0	

PDET_LPF_P : Setting the switching of the PDET output resistor
Set whether the resistor with 340kΩ located at the output of the power detection circuit in the PDET is bypassed or not.
"0" : Bypassing the resistor (default)
"1" : Not bypassing the resistor

RXLPF_FC : Setting the cut off frequency of the receive analog low pass filter
Set the cut off frequency of the PGA consisting of a 1st order low pass filter with variable gain. Refer to the chapter 13.4.4 PGA, AAF about the frequency characteristic.
"0" : Low Cutoff Mode (default)
"1" : High Cutoff Mode

IQ_SEL : I/Q setting for receive analog baseband signal output
Set whether to output Ich or Qch for the receive analog baseband signal output from AOUTP and AOUTN pins when setting <Address0x1A>ANA_PATH bit = "1".
"0" : Ich (default)
"1" : Qch

ANA_PATH : Enable setting for receive analog baseband signal output function
The AAF output signal is output from the AOUTP and AOUTN pins when setting "1". The selection of Ich or Qch is executed by the <Address0x1A>IQ_SEL bit. Normally set ANA_PATH bit = "0".
"0" : AOUTP, AOUTN pins Hi-Z (default)
"1" : AOUTP, AOUTN pins output receive analog baseband signal.

MAIN_PATH : Setting the receive analog baseband output
Set whether to connect the AAF output and ADC input. Normally set MAIN_PATH bit = "1".
"0" : Disconnect AAF output and ADC input
"1" : Connect AAF output and ADC input (default)

LPMODE_LNA : Setting the operation mode of the receive analog circuit (LNA)
Set the operation mode of the receive analog circuit (LNA) to two different operation modes with different current consumption. Refer to the chapter 10.1.1 LNA for the reception performance in each operation mode.
"0" : High Power Mode (default)
"1" : Low Power Mode

14.4.2. <0x1B to 1C,1F>LOCAL

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x1B	X	X	X	HPMODE_LOBLK	X	X	DIVSEL[1:0]		W/R
Initial value				0			0	1	
0x1C	X	TEST_2[2:0]			TEST_3[1:0]		TEST_4[1:0]		W/R
Initial value		0	0	0	0	0	0	0	
0x1F	X	X	X	X	TEST_5[1:0]		TEST_6[1:0]		W/R
Initial value					0	0	0	0	

Though <Address0x1C>TEST_2, TEST_3, TEST_4 bits are test registers, set 69(hex) to this address. These registers adjust the temperature characteristics and slope of the PDET. And the characteristics in the 10.1.3 PDET are due to this setting. Note that <Address0x1F> is described in this term and the order of address is back and forth.

HPMODE_LOBLK : Setting high blocking mode of the LO block

Set the current consumption mode of the LO block. Refer to 10.1.4 MIXER+PGA+AAF+ADC for the reception performance in each operation mode.

"0" : Low Power Mode (default)

"1" : High Power Mode

DIVSEL[1:0] : LOCAL Divider分周設定

Set the division for the LOCAL DIVIDER.

Table 37 LOCAL DIVER division setting

DIVSEL		LOCAL DIVER division setting
[1]	[0]	
0	0	No div
0	1	2 div (default)
1	0	4 div
1	1	8 div

14.4.3. <0x1D to 1E>PHASE ADJ

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x1D	X	PH_ADJ_LP[6:0]							W/R
Initial value		1	0	0	0	0	0	0	
0x1E	X	PH_ADJ_HP[6:0]							W/R
Initial value		1	0	0	0	0	0	0	

Refer to the chapter 13.5.2 Phase Calibration for detail.

PH_ADJ_LP[6:0] : I/Q quadrature phase adjustment (Low Power MODE)
PH_ADJ_HP[6:0] : I/Q quadrature phase adjustment (High Power MODE)

This register enables fine adjustment of the quadrature phase of I/Q. When setting <Address 0x1B>HPMODE_LOBLK = 0, the PH_ADJ_LP bits is effective, and when setting <Address 0x1B>HPMODE_LOBLK = 1, the PH_ADJ_HP bits is effective. The phase adjustment range follows the table below. With the code 64(dec) as center, increasing the code shifts the phase of Qch side in minus direction, and decreasing the code shifts the phase of the Ich side in minus direction. Note that the range and accuracy of the phase adjustment vary depending on the frequency and power mode. When compared in the same power mode, the adjustment range of higher frequency becomes wide, but the

adjustment accuracy becomes coarse. On the other hand, the adjustment range of lower frequency becomes narrow, but the adjustment accuracy becomes fine.

Table 38 Phase adjustment range (960MHz)

PH_ADJ_LP PH_ADJ_HP (dec)	HPM		LPM		Unit
	I ch	Q ch	I ch	Q ch	
0	15.0	0	11.0	0	Δdeg
1					
2	14.8	0	10.8	0	
3	14.5	0	11.7	0	
. . .	. . .	. . .	. . .	. . .	
62	0.5	0	0.3	0	
63	0.2	0	0.2	0	
64	0	0	0	0	
65	0	0.2	0	0.2	
66	0	0.5	0	0.4	
. . .	. . .	. . .	. . .	. . .	
125	0	14.5	0	10.7	
126	0	14.8	0	10.8	
127	0	15.0	0	11.0	

Table 39 Phase adjustment range (450MHz)

PH_ADJ_LP PH_ADJ_HP (dec)	HPM		LPM		Unit
	I ch	Q ch	I ch	Q ch	
0	6.8	0	9.0	0	Δdeg
1					
2	6.6	0	8.9	0	
3	6.5	0	8.7	0	
. . .	. . .	. . .	. . .	. . .	
62	0.2	0	0.3	0	
63	0.1	0	0.1	0	
64	0	0	0	0	
65	0	0.1	0	0.1	
66	0	0.2	0	0.3	
. . .	. . .	. . .	. . .	. . .	
125	0	6.5	0	8.7	
126	0	6.6	0	8.9	
127	0	6.8	0	9.0	

14.4.4. <0x20 to 22>TXOLV

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x20	MODDAC_DG[8:1]								W/R
Initial value	1	1	1	1	1	1	1	1	
0x21	MODDAC_DG[0]	X	X	X	MODDAC_AG[1:0]		MOD_ENABLE[1:0]		W/R
Initial value	1				0	0	0	0	
0x22	X	X	X	X	X	X	TXOLV[1:0]		W/R
Initial value							1	1	

MODDAC_DG[8:0] : Setting digital gain of the MODDAC
Set the gain adjustment of the input data to the MODDAC in the range of 0.25 to 1. Refer to the chapter 13.9 Transmit Data Generation Circuit (MODDAC, SMF).

MODDAC_AG[1:0] : Setting the analog gain of the MODDAC
Set the gain adjustment of the output signal from the MODDAC at the SMF part. Refer to the chapter 13.9 Transmit Data Generation Circuit (MODDAC, SMF) for detail.

MOD_ENABLE[1:0] : Enable setting of MODDAC I/F and MODDAC
This setting enables the writing of the modulation data using the MOD I/F.
Setting <Address0x21>MOD_ENABLE[0] bit = “1” enables to input the data to the MODDAC. And setting MOD_ENABLE[0] bit = “0” sets the MODOUT pin Hi-Z. Refer to the chapter 13.9 Transmit Data Generation Circuit (MODDAC, SMF) for detail.

Setting <Address0x21>MOD_ENABLE[1] bit = “1” enables to input a value to the OFS_MDLT which is the frequency offset of the synthesizer. And if MOD_ENABLE[1] bit = “0” is set, the OFS_MDLT holds the previous set value. Refer to the chapter 13.7.5 Frequency Offset Adjustment and Modulation function for detail.

Refer to the chapter 9.6 Serial Interface Timing for Modulation Data Write (MOD I/F) about the timing of the MODDAC and OFS_MDLT.

TXOLV[1:0] : Setting the output power of the driver amplifier
Set the output power of the driver amplifier. Refer to the chapter 13.10 Transmit Preamplifier Circuit (DRIVER AMP) for detail.

Table 40 Output power of the driver amplifier

TXOLV		Output power of the driver amplifier	Unit
[1]	[0]		
0	0	-10	dBm
0	1	-4	
1	0	-1	
1	1	2 (default)	

14.5. OFCAL

14.5.1. <0x24 to 26>OFCAL

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x24	CALRFPD	X	OFS2REG[1:0]		X	X	OFSCAL2	OFSCAL1	W/R
Initial value	1		0	0			0	0	
0x25	X	X	OFSTA_I[5:0]						W/R
Initial value			1	0	0	0	0	0	
0x26	X	X	OFSTA_Q[5:0]						W/R
Initial value			1	0	0	0	0	0	

Refer to the chapter 13.8.8 DC Offset Calibration for detail.

CALRFPD : Power down setting of the LNA/ATT during the initial DC offset calibration of the analog part (MIXER)

If “1” is written to this register, the LNA/ATT are powered down during the initial DC offset calibration of the analog part (MIXER). The power down is executed from the time when <Address0x24>OFSCAL1 bit = “1” is written until the completion of the calibration and the power on is automatically executed after the calibration is completed. If <Address0x6F>PD_LNA_N bit = “1” and PD_ATT_N bit = “1” are set, the corresponding blocks are powered on according to the truth table described in the Table 6 in 13.1.1 Power Control Logic of the LNA and ATT

“0” : The LNA/ATT are not powered down during the initial DC offset calibration of the analog part.

“1” : The LNA/ATT are powered down during the initial DC offset calibration of the analog part. (default)

OFS2REG[1:0] : Switching the DC offset correction value to the external input

Instead of using the calibration result obtained by the OFSCAL2 bit for the DC offset correction values of the channel filter, the set values of <Address0x28 to 0x2D> are added to the received signal as the correction values for the Ich and Qch respectively and output. The OFS2REG[0] bit and OFS2REG[1] bit switch the correction values of the offset calibration on the main path and the Out of Band Power Monitoring path respectively.

“0” : use the calibration result for the correction value (default)

“1” : use the register set value for the correction value

OFSCAL2 : Start trigger of the initial DC offset calibration for the digital part (channel filter + AGC + Out of Band Power Monitoring block)

Writing “1” starts the DC offset calibration for the digital part (channel filter + AGC + Out of Band Power Monitoring block). It automatically returns to “0” after the calibration is completed.

OFSCAL1 : Start trigger of the initial DC offset calibration for the analog part (MIXER)

Writing “1” starts the DC offset calibration for the analog part. It automatically returns to “0” after the calibration is completed.

OFSTA_I[6:0] : DC offset correction value of the I ch
OFSTA_Q[6:0] : DC offset correction value of the Q ch

Writing to this register enables to set the DC offset calibration value of the analog part (MIXER) by manual. Note that the calibration result is overwritten if this register is written after the calibration using the OFSCAL1 bit.

14.5.2. <0x27 to 2D>OFCAL_DIG

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x27	X	X	X	X	FIROFS_AVE[1:0]		AGCOFS_AVE[1:0]		W/R
Initial value					1	1	1	1	
0x28	OFSTD_I[23:16]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x29	OFSTD_I[15:8]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x2A	OFSTD_I[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x2B	OFSTD_Q[23:16]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x2C	OFSTD_Q[15:8]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x2D	OFSTD_Q[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	

Refer to the chapter 13.8.8 DC Offset Calibration for detail.

FIROFS_AVE[1:0] : Setting the average time of the DC offset calibration (main path and Out of Band Power Monitoring)
Set the time of averaging processing of the DC offset calibration for the main path and Out of Band Power Monitoring path.

AGCOFS_AVE[1:0] : Setting the average time of the DC offset calibration (AGC)
Set the time of averaging processing of the DC offset calibration for the AGC path.

OFSTD_I[23:0] : DC offset correction value of Ich
OFSTD_Q[23:0] : DC offset correction value of Qch
Use these registers if the DC offset correction values of the main path and the Out of Band Power Monitoring path are desired to set arbitrarily. The correction values of these registers are enabled instead of using the initial calibration result if <Address0x24>OFS2REG[x] (x= 0 or 1) bit = “1” is set.

14.6. AGC

14.6.1. <0x2F to 33>PDET & AGC

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x2F	AGC_KPDLY[7:0]								W/R
Initial value	0	1	0	0	0	0	0	1	
0x30	X	X	X	AGC_KPMODE	AGC_KPREG	AGC_KPSEL	DUM_L	PGA_AGCON	W/R
Initial value				0	0	0	0	0	
0x33	PDET_OFS[3:0]				X	X	ATTLVL[1:0]		W/R
Initial value	0	0	0	0			0	0	

Refer to the chapter 13.8.10 AGC Function and 13.8.12 AGC KEEP Function for detail. Set <Address 0x30>DUM_L bit = “0”.

AGC_KPDLY[7:0] : AGC_KEEP Signal Delay Setting

The AGC_KEEP signal is delayed by this register in order to adjust the AGC calculation timing within the IC. The group delay of the received signal path is assumed. The following set value is recommended according to the setting of <Address0x41>DFIL_PATH bits.

Table 41 Recommended value of AGC_KPDLY bits

DFIL_PATH		AGC_KPDLY bits Recommended value (dec)
[1]	[0]	
0	0	33
0	1	65 (default)
1	X	

AGC_KPMODE : Setting of the operation mode of the AGCKEEP function

Set the operation mode of the AGC KEEP function. Refer to the chapter 13.8.12 AGC KEEP Function for detail.

AGC_KPREG : Register control of the AGC KEEP function

The ON/OFF of the AGC KEEP function is controlled by this register if <Address0x30>AGC_KPSEL bit = “0” is set.

“0” : AGC KEEP function OFF (default)

“1” : AGC KEEP function ON

AGC_KPSEL : Switch the control method of the AGC_KEEP function

Switch the control method of the AGC KEEP function.

“0” : controlled by the AGC_KPREG bit (default)

“1” : controlled by the AGCKEEP(NSQ2) pin

PGA_AGCON : ON/OFF setting of the AGC function for the PGA

Set the ON/OFF of the AGC function for the PGA. The PGA gain is changed by the RSSI value (RSSI_BB) calculated by the AGC. Normally set PGA_AGCON bit= “1”. If PGA_AGCON bit = “1” is set, set <Address0x39>DUM_H bit = “1”.

“0” : The AGC function of the PGA is OFF. (default)

“1” : The AGC function of the PGA is ON.

PDET_OFS[3:0] : Setting the output offset voltage adjustment of the PDET circuit

Set the offset voltage added to the voltage output from the PDETOUT pin.

Table 42 Output offset voltage of the PDET circuit

PDET_OFS				Offset Voltage	Unit
[3]	[2]	[1]	[0]		
1	0	0	0	+448	mV
1	0	0	1	+392	
1	0	1	0	+336	
. . .				. . .	
1	1	1	1	+56	
0	0	0	0	0 (default)	
0	0	0	1	-56	
. . .				. . .	
0	1	0	1	-280	
0	1	1	0	-336	
0	1	1	1	-392	

ATTLVL[1:0] : Attenuation setting of the ATT

Set the amount of attenuation. This is the relative value from the insertion loss at the setting of ATTLVL bits = “00”.

Table 43 Setting of the ATT attenuation

ATTLVL		Attenuation Level	Unit
[1]	[0]		
0	0	0 (default)	dB
0	1	6	
1	0	12	
1	1	18	

14.6.2. <0x34 to 3F>AGC_DIG

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x34	AGCHPF_FC[3:0]				X	X	AGCHPF_KEEP	AGCHPFSEL	W/R
Initial value	0	0	0	0			0	0	
0x35	X	X	PGAGAIN[5:0]						W/R
Initial value			0	0	0	0	0	0	
0x36	X	AGCMAX[2:0]			AGCTGT[3:0]				W/R
Initial value		1	1	1	0	0	0	0	
0x37	AGCHYS[1:0]		AGCLIM[5:0]						W/R
Initial value	0	0	0	0	0	0	0	0	
0x38	AGCTIM[3:0]				AGCTRW[3:0]				W/R
Initial value	1	0	0	0	1	0	0	0	
0x39	DUM_H	X	X	X	X	X	X	X	W/R
Initial value	0								
0x3E	STS_RSSI_SEL[1:0]		DFILOUT[2:0]			DAGC_HYS[1:0]		DAGC_ON	W/R
Initial value	0	0	1	0	0	0	0	0	
0x3F	DAGC_TH[7:0]								W/R
Initial value	1	0	0	0	0	0	0	0	

Refer to the chapter 13.8.10 AGC Function, 13.8.11 Digital Output AGC Function and 13.8.12 AGC KEEP Function for detail. If <Address0x30>PGA_AGCON bit= “1” is set, set <Address0x39>DUM_H bit = “1”.

AGCHPF_FC[3:0] : Cut off frequency setting of the HPF for the AGC

Set the cut off frequency of the HPF for the AGC. Refer to the chapter 13.8.6 HPF for detail.

AGCHPF_KEEP : AGC_KEEP function and AGCHPF linkage setting

This function enables the AGC KEEP function to operate in conjunction with the AGCHPF. Setting “1” to this register holds the internal state of the AGCHPF if the AGC KEEP function is ON, and the AGCHPF performs calculations in this state.
When the AGC KEEP function is turned off, the AGCHPF operation starts again.

“0” : The AGC KEEP function and AGCHPF are not linked. (default)
“1” : The AGC KEEP function and AGCHPF are linked.

AGCHPFSEL : Setting ON/OFF of the HPF for the AGC

The HPF for the AGC is located at the previous stage of the AGC circuit. This register sets ON/OFF of the HPF for the AGC.

“0” : HPF1 OFF (default)
“1” : HPF1 ON

PGAGAIN[5:0] : Gain setting of the PGA

Set the gain both of the Ich and Qch.
■ If <Address0x30>PGA_AGCON bit = “0” is set,
the AGC function turns OFF and this register sets the PGA gain.
■ If <Address0x30>PGA_AGCON bit = “1” is set,
the AGC start to operate with the initial value set by the PGAGAIN[5:0] bits.
Normally set PGAGAIN bits = “000000”.

Table 44 Gain setting of the PGA

PGAGAIN						Gain	Unit
[5]	[4]	[3]	[2]	[1]	[0]		
0	0	0	0	0	0	28 (default)	dB
0	0	0	0	0	1	27	
0	0	0	0	1	0	26	
0	0	0	0	1	1	25	
. . .						. . .	
0	1	1	0	1	1	1	
0	1	1	1	0	0	0	
0	1	1	1	0	1	-1	
. . .						. . .	
1	0	1	1	1	1	-19	
1	1	0	0	0	0	-20	
1	1	0	0	0	1	Prohibited	
1	1	0	0	1	0		
1	1	0	0	1	1		
1	1	0	1	0	0		
1	1	0	1	0	1		
1	1	0	1	1	0		
1	1	0	1	1	1		
1	1	1	X	X	X		

AGCMAX[2:0] : Maximum allowable gain change in a single AGC operation
Set the maximum allowable gain change in a single AGC operation.

Table 45 Maximum allowable gain change of the AGC operation

AGCMAX			Maximum allowable gain change	Unit
[2]	[1]	[0]		
0	0	0	Prohibited	dB
0	0	1	1	
0	1	0	2	
0	1	1	4	
1	0	0	8	
1	0	1	16	
1	1	0	32	
1	1	1	48 (default)	

AGCTGT[3:0] : Target value of signal convergence level of the AGC
Set the target of convergence level of the AGC.

Table 46 Target value of signal convergence level of the AGC

AGCTGT				Convergence level	Unit
[3]	[2]	[1]	[0]		
0	0	0	0	6 (default)	dBm
0	0	0	1	4	
0	0	1	0	2	
0	0	1	1	0	
0	1	0	0	-2	
0	1	0	1	-4	
0	1	1	0	-6	
0	1	1	1	-8	
1	0	0	0	-10	
1	0	0	1	-12	
1	0	1	0	-14	
1	0	1	1	-16	
1	1	0	0	-18	
1	1	0	1	-20	
1	1	1	0	-22	
1	1	1	1	-24	

AGCHYS[1:0] : Hysteresis width for the signal power convergence level of the AGC

When the current receiving signal level is converged within the judgement level of this setting for the convergence target level of the AGC set by <Address0x36>AGCTGT bits, the AGC is considered to be converged and the gain change is stopped.

Table 47 Hysteresis width for the signal power convergence level of the AGC

AGCHYS		Convergence level	Unit
[1]	[0]		
0	0	-2 <, < +2 (default)	dB
0	1	-4 <, < +4	
1	0	-8 <, < +8	
1	1	-16 <, < +16	

AGCLIM[5:0] : Upper limit setting of the PGA gain

The upper limit of the PGA gain is set by this register. The PGA gain is saturated by the set value of this register regardless of the AGC operation. The set value is same as the Table 44 Gain setting of the PGA.

AGCTIM[3:0] : Time setting to calculate and judge the signal power of the AGC

Set the time to calculate and judge the signal power of the AGC. The power calculation and judgement time is calculated by the equation 14.1. And the Table 48 shows the count number. The operating frequency of the programmable FIR filter is changed by the setting of <Address0x41>DFIL_PATH bits. For more information about the operating frequency of the programmable FIR filter, refer to the chapter 13.8.5 Decimation Filter.

Power calculation and judgement time=operating period of the programmable FIR filter x count number …(14.1)

Table 48 Count number of signal power calculation and judgement of the AGC

AGCTIM				Count number
[3]	[2]	[1]	[0]	
0	0	0	0	2
0	0	0	1	4
0	0	1	0	8
0	0	1	1	16
0	1	0	0	32
0	1	0	1	64
0	1	1	0	128
0	1	1	1	256
1	0	0	0	512 (default)
1	0	0	1	1024
1	0	1	0	2048
1	0	1	1	4096
1	1	0	0	Prohibited
1	1	0	1	Prohibited
1	1	1	0	Prohibited
1	1	1	1	Prohibited

AGCTRW[3:0] : Standby time setting of the AGC power detection

Set the standby time from the timing of gain change of the PGA until the next power detection starts in AGC operation. The standby time is calculated by the equation 14.2. And the Table 49 shows the count number.

Standby time of the power detection=operating period of the programmable FIR filter x count number … (14.2)

Table 49 Standby time setting of AGC power detection

AGCTRW				Count number
[3]	[2]	[1]	[0]	
0	0	0	0	2
0	0	0	1	4
0	0	1	0	8
0	0	1	1	16
0	1	0	0	32
0	1	0	1	64
0	1	1	0	128
0	1	1	1	256
1	0	0	0	512 (default)
1	0	0	1	1024
1	0	1	0	2048
1	0	1	1	4096
1	1	X	X	Prohibited

STS_RSSI_SEL[1:0] : Selection of the status output S15 to S8 (RSSI)

The data of S15 to S8 (RSSI) output from the STATUS pin is switched. However, if the result of the subtraction is less than 0 code, the 0 code is output.

"00" : <ROpage Address0x06>R_RSSI bits (default)

"01" : <ROpage Address0x07>R_OOBL_RSSI bits minus R_RSSI bits

"1x" : <ROpage Address0x08>R_OOBR_RSSI bits minus R_RSSI bits

DFILOUT[2:0] : Setting the digital filter output bit

If the digital output AGC function is set to ON, the output bit is selected when the digital output AGC function judges the LSB side. And if the digital output AGC function is set to OFF and the 16-bit data is output with <Address0x41>ADIFSEL bits = "01", the bit selected by this register is output.

Refer to the chapters 13.8.11 Digital Output AGC and 13.8.20 Test Output Function of Internal Node for detail.

DAGC_HYS[1:0] : Setting the hysteresis width of the threshold of the digital output AGC function

Set the hysteresis width for the threshold of the digital AGC function.

Table 50 Hysteresis width of the digital output AGC function

DAGC_HYS		Switching threshold (0.5dB/code)	Unit
[1]	[0]		
0	0	4 (default)	code
0	1	8	
1	0	16	
1	1	32	

DAGC_TH[7:0] : Setting the judgement threshold of the digital output AGC function

Set the threshold of the digital output AGC function. The set value is calculated by the same equation as RSSI code described in the chapter 13.8.15 RSSI Function.

The MSB side is selected as the output bit if the calculation result of the RSSI is greater than or equal to the set value of DAGC_TH[7:0] bits. The LSB side (DFIL_OUT bits setting side) is selected as the output bit if the calculation result of the RSSI is less than or equal to the value obtained by subtracting the hysteresis width set by DAGC_HYS[1:0] bits from the value set by DAGC_TH[7:0] bits.

DAGC_ON : Setting ON/OFF for the digital output AGC function

"0" : Digital output AGC function OFF (default)

"1" : Digital output AGC function ON

14.7. DIGITAL

14.7.1. <0x41>DIG_MODE

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x41	X	X	ADIFSEL[1:0]		RXIF_SR[1:0]		DFIL_PATH[1:0]		W/R
Initial value			0	0	0	0	0	1	

ADIFSEL[1:0] : Setting the output data format

Set the data format output to the ADFS, ADSCLK, ADSDO and STATUS pins. Refer to the chapter 9.5 Serial Interface Timing for Receiving Data and Status Output Read for detail.

Table 51 Output Data Format

ADIFSEL		Output Data Format
[1]	[0]	
0	0	IQ 32-bit Mode (default)
0	1	IQ 16-bit Mode
1	0	FMDET Mode
1	1	Prohibited

RXIF_SR[1:0] : Setting the output sampling rate

Set the sampling rate output to the ADFS, ADSCLK, ADSDO and STATUS pins. Refer to the chapter 13.8.18 Output Sampling Rate for detail.

DFIL_PATH[1:0] : Setting the output path of the decimation filter

Select the output path of the decimation filter.

Table 52 Decimation Filter Output Path

DFIL_PATH		Decimation Filter Output Path
[1]	[0]	
0	0	FIR3 out
0	1	FIR4 out (default)
1	X	FIR5 out

14.7.2. <0x42>DFIL_SET

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x42	COEF_SET[7:0]								W
Initial value	-	-	-	-	-	-	-	-	

Refer to the chapters 9.4 Serial Interface Timing for Programmable Digital Filter Coefficient Setting and 13.8.17 IIR Filter for detail.

COEF_SET[7:0] : Setting the write/read of the coefficients of the programmable digital filter

<Address0x42>COEF_SET[7:0] bits sets the coefficients write/read mode of the digital filter, which can set the coefficients arbitrarily. The value written to the COEF_SET[7:0] bits selects the switching of writing and reading or filter type.

14.7.3. <0x43 to 45>NCO MIXER

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x43	DELTA1F[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x44	DELTA2F[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x45	NCO_SET	X	X	X	UPMIX_OFF	DWMIX_OFF	ROM_UPDATE[1:0]		W/R
Initial value	0				0	0	0	0	

Refer to the chapter 13.8.4 NCO for detail.

DELTA1F[7:0] : LO frequency setting of the main path (Δ1)
DELTA2F[7:0] : LO frequency setting of the Out of Band Power Monitoring path (Δ2)
Set the output frequency from the NCO. The calculation of Δ1±Δ2 is executed for the Out of Band Power Monitoring path.

If TCXO = 24.576MHz LO frequency = DELTA*F[7:0] × 375.00 [Hz]
If TCXO = 18.432MHz LO frequency = DELTA*F[7:0] × 281.25 [Hz]

NCO_SET : Resolution setting of LO frequency
If "1" is set, the resolution and output range of the output frequency from the NCO become half.
If TCXO = 24.576MHz LO frequency = DELTA*F[7:0] × 187.500 [Hz]
If TCXO = 18.432MHz LO frequency = DELTA*F[7:0] × 140.625 [Hz]

UPMIX_OFF : Setting off the complex mixer (Zero_IF to Low_IF)
If "1" is set, the frequency conversion is not executed by the complex mixer (Zero_IF to Low_IF) and bypassed.

DWMIX_OFF : Setting off the complex mixer (Low_IF to Zero IF)
If "1" is set, the frequency conversion is not executed by the complex mixer (Low_IF to Zero_IF) and bypassed.

ROM_UPDATE[1:0] : Update setting of the LO frequency
Setting this register loads the frequency setting of DELTA1F[7:0] and DELAT2F[7:0] bits to a circuit. This register automatically returns to zero after setting.

14.7.4. <0x46>PRE_HPF

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x46	PRE_HPF_FC[3:0]				X	PRE_HPF_KEEP	PRE_HPFSEL[1:0]		W/R
Initial value	0	0	0	0		0	0	0	

Refer to the chapter 13.8.6 HPF about this setting for detail.

PRE_HPF_FC[3:0] : Setting the cut off frequency of the PRE_HPF
Set the cut off frequency of the PRE_HPF.

PRE_HPF_KEEP : Linking setting of PRE_HPF and AGC KEEP function
This function enables to link the AGC KEEP function and PRE_HPF. Setting "1" to this register holds the internal state of the PRE_HPF if the AGC KEEP function is ON, and the PRE_HPF performs calculations in this state. The PRE_HPF starts to operate again if the AGC KEEP function is turned OFF.
"0" : AGC KEEP and PRE_HPF are not linked. (default)
"1" : AGC KEEP and PRE_HPF are linked.

PRE_HPFSEL[1:0]：Setting ON/OFF of the PRE_HPF

Set ON/OFF of the PRE_HPF. The filter order of the PRE_HPF can be selected between 1st order or 2nd order.

Table 53 PRE_HPF Set

PRE_HPFSEL		Function
[1]	[0]	
0	0	PRE_HPF OFF (default)
0	1	PRE_HPF ON (IIR 1次)
1	X	PRE_HPF ON (IIR 2次)

14.7.5. <0x47 to 48>MIXER_ATT

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x47	DWMIXATT[13:6]								W/R
Initial value	1	1	1	1	1	1	1	1	
0x48	DWMIXATT[5:0]						DWMIXATT_SET[1:0]		W/R
Initial value	1	1	1	1	1	1	0	0	

Refer to the chapter 13.8.2 Complex Mixer about this setting for detail.

DWMIXATT [13:0]：Setting the complex mixer gain adjustment

The gain of the complex mixer is set if DWMIXATT_SET [1:0] bits is set to “01” or “10”. Setting “all 0” is prohibited.

DWMIXATT_SET [1:0]：Setting ON/OFF of the complex mixer gain adjustment function

Set ON/OFF of the complex mixer adjustment function. The gain adjustment is executed by attenuating the local signal of either Ich or Qch.

Table 54 Setting ON/OFF of the complex mixer gain adjustment function

DWMIXATT_SET		Output Data Format
[1]	[0]	
0	0	OFF (default)
0	1	Attenuating Ich
1	0	Attenuating Qch
1	1	OFF

14.7.6. <0x4A>CH FILTER

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x4A	X	PFIL_SAT[2:0]			X	CHCOEF_SEL[1:0]		COEF LOAD	W/R
Initial value		0	0	0		0	0	0	

For more information about this setting, refer to the chapters 9.4 Serial Interface Timing for Programmable Digital Filter Coefficient Setting, 13.8.7 Channel Filter and 13.8.17 IIR Filter.

PFIL_SAT[2:0]：Saturation setting of the channel filter output

Set the saturation process and truncation of the channel filter output.

Table 55 Programable Filter Saturation Set

PFIL_SAT			Saturation process	Truncation bit	Gain
[2]	[1]	[0]			
0	0	0	2-bit	3-bit	× 1/8
0	0	1	3-bit	2-bit	× 1/4
0	1	0	4-bit	1-bit	× 1/2
0	1	1	5-bit	0-bit	× 1
1	0	0	6-bit	0-bit	× 2
1	0	1	7-bit	0-bit	× 4
1	1	0	8-bit	0-bit	× 8
1	1	1	9-bit	0-bit	× 16

CHCOEF_SEL[1:0] : Selection setting of the channel filter coefficient

Select one of the four coefficient sets.

Table 56 Channel Coefficient Select

CHCOEF_SEL		Function
[1]	[0]	
0	0	FIR Channel Filter 1 (default)
0	1	FIR Channel Filter 2
1	0	FIR Channel Filter 3
1	1	FIR Channel Filter 4

COEFLOAD : Loading the coefficient of the programmable FIR filter

The coefficients selected by <Address0x4A>CHCOEF_SEL[1:0] are loaded to the programmable FIR filter. The value of this register automatically returns to “0” after the coefficients are loaded. Set <Address0x6D>PD_CLKBUF_N bit = “1” and input the clock, then write “1” to this register.

14.7.7. <0x4C to 4E>RSSI

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x4C	X	X	X	X	X	RSSI_AVE[2:0]			W/R
Initial value						0	0	0	
0x4D	RSSI_OFST[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x4E	RSSI_ATT[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	

Refer to the chapter 13.8.15 RSSI Function for detail.

RSSI_AVE[2:0] : Setting the averaging count of the RSSI

Set the averaging count of the power detected by the RSSI circuit and sampled at the operating frequency of the programmable FIR filter set by <Address0x41>DFIL_PATH bits. The averaging count is calculated by 2^N, where N is set by RSSI_AVE.

RSSI_OFST[7:0] : Correction value of the RSSI (signed)

Set the correction value of the RSSI. The value of adding the correction value set by this register to the calculated result of the received signal power is output as the calculation result of the RSSI. Use this

function for gain compensation of signal loss in the stage before the LNA or between the LNA and MIXER. The valid setting range is -128 to +127 (code).

RSSI_ATT[7:0] : RSSI correction linked to the LNA/ATT switching

This register is used to correct the attenuation when the LNA is switched to the ATT for the calculation result of the RSSI circuit. The value of adding the correction value set by this register to the calculated result of the received signal power is output as the calculation result of the RSSI. Set the MSB to "0". The valid setting range is 0 to +127 (code). This setting is enabled only when the ATT operates.
For example, if the LNA gain is 17dB and the insertion loss of the ATT is 4dB, the gain change is -4-17=-21dB. In this case, set RSSI_ATT bits = 42(dec). Note that normal operation is not guaranteed with a set value that deviates greatly from the gain change amount. Also, refer to the Table 57.

Table 57 RSSI_ATT Setting Example

ATTLVL		RSSI_ATT (dec)
[1]	[0]	
0	0	42
0	1	54
1	0	66
1	1	78

14.7.8. <0x50 to 52> Out of Band Power Monitoring

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x50	X	X	X	X	OOB_PAVE[2:0]			OOB_ON	W/R
Initial value					0	0	0	0	
0x51	RSSI_L_OFST[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x52	RSSI_R_OFST[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	

Refer to the chapter 13.8.3 Out of Band Power Monitoring Function for detail.

OOB_PAVE[2:0] : Setting averaging count of Out of Band Power Monitoring RSSI

Set the averaging count of the power detected by the RSSI circuit of the out of band power monitoring circuit and sampled at the operating frequency of the FIR3 decimation filter (MCLK/128). The averaging count is calculated by 2^N, where N is set by OOB_AVE.

OOB_ON : Setting ON/OFF of the Out of Band Power Monitoring function

Set ON/OFF of the out of band power monitoring function.

"0" : Out of Band Power Monitoring function OFF (default)
"1" : Out of Band Power Monitoring function ON

RSSI_L_OFST[7:0] : Correction value of Out of Band Power Monitoring Lside RSSI (signed)

Set the correction value of the RSSI to detect the interference wave at low frequency side (Lside) in the out of band power monitoring circuit. The value of adding the correction value set by this register to the calculated result of the received signal power is output as the calculation result of the RSSI. Use this function for gain compensation of signal loss in the stage before the LNA or between the LNA and MIXER. The valid setting range is -128 to +127 (code).

RSSI_R_OFST[7:0] : Correction value of Out of Band Power Monitoring Rside RSSI (signed)

Set the correction value of the RSSI to detect the interference wave at high frequency side (Rside) in the out of band power monitoring circuit. The value of adding the correction value set by this register to the calculated result of the received signal power is output as the calculation result of the RSSI. Use this function for gain compensation of signal loss in the stage before the LNA or between the LNA and MIXER. The valid setting range is -128 to +127 (code).

14.7.9. <0x54 to 58>FMDET

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x54	X	RSSI_DETOUT	REG_DETOUT	X	X	X	FMDET_G[1:0]		W/R
Initial value		0	0				0	0	
0x55	RSSIDAC_LOLIM[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x56	IF_OFST[23:16]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x57	IF_OFST[15:8]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x58	IF_OFST[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	

Refer to the chapter 13.8.13 FM Detection Function and 13.8.15 RSSI Function for detail.

RSSI_DETOUT：Output setting of RSSI data to DETDAC
The RSSI data is output to the DETDAC by this setting. The output data is controlled by <Address 0x55>RSSIDAC_LOLIM[7:0] and <Address0x5D>DET_DC[7:0].

REG_DETOUT：Output setting of register data to DETDAC
The setting of <Address0x5D>DET_DC is output to the DETDAC as MSB data by this register setting. This register has priority over the RSSI_DETOUT bit.

FMDET_G[1:0]：bit adjustment of FM demodulation output
The FM detection circuit converts the frequency deviation of the FM modulated signal to the amplitude level and outputs to the DETDAC. This register setting enables to adjust the bit of the demodulated output (= adjustment of the output amplitude gain) and change the maximum frequency deviation for the DAC to output at full scale. The bit set by this register is output with serial if <Address0x41> ADIFSEL[1:0] = “10” is set.

Table 58 Maximum frequency deviation of the FM demodulated output by FMDET_G bits

FMDET_G		Maximum frequency deviation possible to output
[1]	[0]	
0	0	1/512 of MCLK frequency (default)
0	1	1/1024 of MCLK frequency
1	0	1/2048 of MCLK frequency
1	1	1/4096 of MCLK frequency

Calculation example)
The maximum frequency deviation that the DAC can represent when the MCLK frequency is 24.576MHz.
FMDET_G[1:0] = “00” ：24.576MHz / 512 = 48kHz

RSSIDAC_LOLIM[7:0]：Setting the lower limit of DETDAC output for RSSI (unsigned)

This register is enabled if <Address0x54>RSSI_DETOUT bit = “1” is set. Set the lower limit when the RSSI is output to the DETDAC.

IF_OFST[23:0]：DC offset adjustment of FM demodulation output (signed)
The DC offset of the FM demodulation output is adjusted. The FM demodulation circuit performs calculation with 24-bit and the value set by this register is added to the result of FM demodulation. If the IF signal is input to the FM demodulation circuit, a DC offset equal to the IF frequency is occurred at the FM demodulation output. Setting the correction value to this register can remove the DC offset in advance.

14.7.10. <0x59 to 5C>NSQ

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x59	NSQ1_HYS[1:0]		NSQ1_AVE[1:0]		X	X	X	NSQ1_ON	W/R
Initial value	0	0	0	0				0	
0x5A	NSQ1_TH[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	
0x5B	NSQ2_HYS[1:0]		NSQ2_AVE[1:0]		X	X	X	NSQ2_ON	W/R
Initial value	0	0	0	0				0	
0x5C	NSQ2_TH[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	

Refer to the chapter 13.8.16 Noise Squelch Function for detail.

NSQ1_HYS[1:0]：Setting the hysteresis width of NSQ1
Set the hysteresis width for the set value of <Address0x5A>NSQ1_TH[7:0] bits.

Table 59 NSQ1 Hysteresis Set

NSQ1_HYS		Hysteresis width	Unit
[1]	[0]		
0	0	4 (default)	Code
0	1	8	
1	0	16	
1	1	32	

NSQ1_AVE[1:0]：Setting the average count of output power of NSQ1 function
Set the averaging count of the output power if the noise squelch function 1 is turned ON by setting <Address0x59>NSQ1_ON bit = “1”. The moving average is used for the calculation and the data update rate is every 4 data.

Table 60 NSQ1 Average Set

NSQ1_AVE		Moving average data count
[1]	[0]	
0	0	8 (default)
0	1	16
1	0	32
1	1	64

NSQ1_TH[7:0]：Setting the threshold to judge the output power of NSQ1 function

Set the threshold to judge the output power if the noise squelch function 1 is turned ON by setting <Address0x59>NSQ1_ON bit = “1”. Comparing the value set by this register with the average value of the output power, and if the output power is larger, “H” is output from the NSQ1 pin.

NSQ2_HYS[1:0] : Setting the hysteresis width of NSQ2

Set the hysteresis width for the set value of <Address0x5C>NSQ2_TH[7:0] bits.

Table 61 NSQ2 Hysteresis Set

NSQ2_HYS		Hysteresis width	Unit
[1]	[0]		
0	0	4 (default)	Code
0	1	8	
1	0	16	
1	1	32	

NSQ2_AVE[1:0] : Setting the average count of output power of NSQ2 function

Set the averaging count of the output power if the noise squelch function 2 is turned ON by setting <Address0x5B>NSQ2_ON bit = “1”. The moving average is used for the calculation and the data update rate is every 4 data.

Table 62 NSQ2 Average Set

NSQ2_AVE		Moving average data count
[1]	[0]	
0	0	8 (default)
0	1	16
1	0	32
1	1	64

NSQ2_TH[7:0] : Setting the threshold to judge the output power of NSQ2 function

Set the threshold to judge the output power if the noise squelch function 2 is turned ON by setting <Address0x5B>NSQ2_ON bit = “1”. Comparing the value set by this register with the average value of the output power, and if the output power is larger, “H” is output from the NSQ2 pin.

14.7.11. <0x5D>FMDET2

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x5D	DET_DC[7:0]								W/R
Initial value	0	0	0	0	0	0	0	0	

Refer to the chapter 13.8.14 DETDAC, SMF Function for detail.

DET_DC[7:0] : External setting of DETDAC

The value set by this register can be output to the DETDAC by setting <Address0x54>REG_DETOUT bit = “1”. Though the DETDAC is 12-bit, this register is applied as the MSB data and the 4-bit on the LSB side are filled with 0. Note that this register is set with 2’s complement data.

14.7.12. <0x5F>POST_HPF

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x5F	POST_HPF_FC[3:0]				X	X	POST_HPF_KEEP	POST_HPFSEL	W/R
Initial value	0	0	0	0			0	0	

Refer to the chapter 13.8.6 HPF for detail.

POST_HPF_FC[3:0] : Setting the cut off frequency of the POST_HPF
Set the cut off frequency of the POST_HPF.

POST_HPF_KEEP : Linking setting of POST_HPF and AGC KEEP function
It is possible to operate with linking the AGC KEEP function and POST_HPF by this function. Setting "1" to this register holds the internal state of the POST_HPF if the AGC KEEP function is ON, and the POST_HPF performs calculations in this state. The POST_HPF starts to operate again if the AGC KEEP function is turned OFF.

"0" : The AGC KEEP and POST_HPF are not linked. (default)
"1" : The AGC KEEP and POST_HPF are linked.

POST_HPFSEL[1:0] : Setting ON/OFF of POST_HPF
Set ON/OFF of the POST_HPF.

"0" : POST_HPF OFF (default)
"1" : POST_HPF ON

14.7.13. <0x62-6B>RDOC

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x62	X	RDOC_1	RDOC_KEEP	RDOC_2[1:0]		RDOC_3[1:0]		RDOC_ON	W/R
Initial value		1	0	1	0	0	1	0	
0x63	X	RDOC_4	RDOC_5[1:0]		X	RDOC_6[1:0]		RDOC_7	W/R
Initial value		0	0	0		0	0	0	
0x64	X	RDOC_8[2:0]			X	RDOC_9[1:0]		RDOC_10	W/R
Initial value		0	1	0		0	0	0	
0x65	RDOC_11[1:0]		RDOC_12[1:0]		X	RDOC_13[1:0]		RDOC_14	W/R
Initial value	1	1	1	1		0	0	0	
0x66	RDOC_15[1:0]		X	X	X	X	RDOC_18[1:0]		W/R
Initial value	1	1					0	0	
0x67	X	X	X	RDOC_19	X	RDOC_20[1:0]		RDOC_21	W/R
Initial value				0		0	0	0	
0x68	X	X	X	X	X	RDOC_22[1:0]		RDOC_FM	W/R
Initial value						0	0	0	
0x69	X	RDOC_23[1:0]		RDOC_24[1:0]		RDOC_25[2:0]			W/R
Initial value		0	0	0	0	1	0	1	
0x6A	RDOC_26[7:0]								W/R
Initial value	0	0	0	0	1	0	0	1	
0x6B	RDOC_16[7:0]								W/R
Initial value	0	0	1	0	1	0	1	0	
0x6C	RDOC_17[7:0]								W/R
Initial value	0	0	0	0	1	0	1	0	

Refer to the chapter 13.8.9 RDOC Function for detail.

Set the initial value to all registers about the operation setting register of the RDOC as the table below.

Register	Address	Initial value
RDOC_1	0x62 D6	“1”
RDOC_2	0x62 D4-D3	“10”
RDOC_3	0x62 D2-D1	“01”
RDOC_4	0x63 D6	“0”
RDOC_5	0x63 D5-D4	“00”
RDOC_6	0x63 D2-D1	“00”
RDOC_7	0x63 D0	“0”
RDOC_8	0x64 D6-D4	“010”
RDOC_9	0x64 D2-D1	“00”
RDOC_10	0x64 D0	“0”
RDOC_11	0x65 D7-D6	“11”
RDOC_12	0x65 D5-D4	“11”
RDOC_13	0x65 D2-D1	“00”
RDOC_14	0x65 D0	“0”
RDOC_15	0x66 D7-D6	“11”
RDOC_16	0x6B D7-D0	“00101010”
RDOC_17	0x6C D7-D0	“00001010”
RDOC_18	0x66 D1-D0	“00”
RDOC_19	0x67 D4	“0”
RDOC_20	0x67 D2-D1	“00”
RDOC_21	0x67 D0	“0”
RDOC_22	0x68 D2-D1	“00”
RDOC_23	0x69 D6-D5	“00”
RDOC_24	0x69 D4-D3	“00”
RDOC_25	0x69 D2-D0	“101”
RDOC_26	0x6A D7-D0	“00001001”

RDOC_KEEP：Linking setting of AGC KEEP function and RDOC

It is possible to operate with linking the AGC KEEP function and RDOC by this function. Setting “1” stops the operation of the RDOC if the AGC KEEP function is turned ON. At this time, the calculated DC offset is held. The RDOC starts to operate again if the AGC KEEP function is turned OFF.

“0”：The AGC KEEP and RDOC are not linked. (default)

“1”：The AGC KEEP and RDOC are linked.

RDOC_ON : Setting ON/OFF of the RDOC function

Set ON/OFF of the RDOC.

“0”：RDOC OFF (default)

“1”：RDOC ON

RDOC_FM : Setting ON/OFF of automatic switching of positive and negative of the local frequency offset

Setting “1” to this register automatically switches the polarity (positive or negative) of the local frequency offset set by <Address0x02 to 0x03>OFS_RDOC[15:0] bits. The <Address0x12>DSM_AT_INT bit must be set to “1” if the RDOC_FM bit is set to “1”. The setting of RDOC_FM bit = “1” and DSM_AT_INT bit = “0” is prohibited.

“0”：does not switch the polarity (positive or negative) of frequency (default)

“1”：switches the polarity (positive or negative) of frequency

14.7.14. <0x6D-6F> PD

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x6D	X	X	X	PD_MULTI_N	X	PD_CLKBUF_N	PD_REF_N	X	W/R
Initial value				0		0	0		
0x6E	X	X	X	X	X	PD_MODDAC_N	PD_PLL_N	PD_TX_N	W/R
Initial value						0	0	0	
0x6F	X	DUM_L	PD_DETDAC_N	PD_PDET_N	PD_ATT_N	PD_LNA_N	PD_ADC_N	PD_RX_N	W/R
Initial value		0	0	0	0	0	0	0	

Control power-down of each block. Refer to the chapter 13.1 Power Control for detail.
Set <Address0x6F>DUM_L bit = “0”.

14.8. PDET ADDITIONAL OFFSET

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x74	DUM_L	DUM_L	DUM_L	DUM_L	DUM_L	DUM_L	DUM_L	PDET_OFF	W/R
Initial value	0	0	0	0	0	0	0	0	

Set <Address0x74>DUM_L bit = “0”.

PDET_OFF : Setting to increase PDET Output Voltage
This is the function to increase the PDET Output Voltage. Refer to the chapter 13.4.2 PDET for detail.

“0”：default (default)
“1”：Increase PDET Output Voltage by 0.4V

14.9. PRE TEST FUNCTION

14.9.1. <0x75>CURRENT

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x75	X	I_AAF	I_PGA[1:0]		X	X	X	TEST_7	W/R
Initial value		0	0	1				0	

The <Address0x75>TEST_7 bit is test register. Set the initial value.

I_AAF : Current adjustment of the AAF

Adjust the current of the AAF. Refer to the chapter 13.4.4 PGA, AAF.

"0" : default

"1" : +100%

I_PGA : Current adjustment of the PGA

Adjust the current of the PGA. Refer to the chapter 13.4.4 PGA, AAF.

Table 63 PGA Current Set

I_PGA		Current adjustment [%]
[1]	[0]	
0	0	-25%
0	1	0% (default)
1	0	+25%
1	1	+114%

14.9.2. <0x79 to 7A>DEBUG

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x79	X	X	X	X	RXDTO[3:0]				W/R
Initial value					0	0	0	0	
0x7A	X	X	X	X	X	X	X	X	W/R
Initial value									

RXDTO[3:0] : Setting test output of receive path

The internal node of the receiving digital circuit is output to ADFS, ADSCLK and ADSDO pins with 3-wire serial. This function is assumed for debugging purposes. Refer to the chapter 13.8.20 Test Output Function of Internal Node for detail.

14.10. SOFTWARE REST & PAGE

14.10.1. <0x7D>PAGE

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x7D	PAGE[7:0]								W
Initial value	0	0	0	0	0	0	0	0	

PAGE[7:0] : Setting the page
Writing 46(hex) to PAGE bits can move to the Read Only Page.

14.10.2. <0x7E>SOFT RESET

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x7E	SRST[7:0]								W
Initial value	0	0	0	0	0	0	0	0	

SRST[7:0] : Software reset
The software reset is executed by writing SRST bits = AA(hex). This register automatically returns to zero after completing the software reset. For more information about the software reset, refer to the chapter 9.2 System Reset.

14.11. READ BACK ONLY

14.11.1. <0x03>READ COEF

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x03	X	R_COEFSTS_OOB	R_COEFSTS_NSQ2	R_COEFSTS_NSQ1	R_COEFSTS4	R_COEFSTS3	R_COEFSTS2	R_COEFSTS1	R
Initial value		1	1	1	1	1	1	1	

R_COEFSTS_OOB : Error status of the writing or reading the filter coefficients of the Out of Band Power Monitoring
R_COEFSTS_NSQ2 : Error status of the writing or reading the filter coefficients of the NSQ2
R_COEFSTS_NSQ1 : Error status of the writing or reading the filter coefficients of the NSQ1
R_COEFSTS4 : Error status of the writing or reading the filter coefficients of the channel filter FIR4
R_COEFSTS3 : Error status of the writing or reading the filter coefficients of the channel filter FIR3
R_COEFSTS2 : Error status of the writing or reading the filter coefficients of the channel filter FIR2
R_COEFSTS1 : Error status of the writing or reading the filter coefficients of the channel filter FIR1

If the number of input clocks are greater or less than the specified counts during the burst writing or reading of the digital filter coefficients, it is judged that the writing or reading is not executed normally, and the “1” is written to this register. The status of this register is valid for the filter that has been written or read just before the access.

“0” : The writing or reading is performed normally.
“1” : The writing or reading is not performed normally. (default)

14.11.2. <0x04>STATUS

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x04	R_DAGC_STS	R_ATT_STS	X	X	X	X	X	X	R
Initial value	0	0							

Refer to the chapter 13.8.19 Status Output for detail.

R_DAGC_STS : Digital output AGC status
R_ATT_STS : Status to determine whether LNA or ATT is operating

14.11.3. <0x06 to 0B>READ RSSI

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x06	R_RSSI[7:0]								R
Initial value	0	0	0	0	0	0	0	0	
0x07	R_OOBL_RSSI[7:0]								R
Initial value	0	0	0	0	0	0	0	0	
0x08	R_OOBR_RSSI[7:0]								R
Initial value	0	0	0	0	0	0	0	0	
0x0A	R_RSSI_BB[7:0]								R
Initial value	0	0	0	0	0	0	0	0	

R_RSSI[7:0] : RSSI result of desired wave
The RSSI result of desired wave can be read back. Refer to the chapter 13.8.15 RSSI Function for detail.

R_OOBL_RSSI[7:0] : Result of the RSSI of interference wave at lower frequency
The RSSI result of interference wave at lower frequency can be read back. Refer to the chapter 13.8.3 Out of Band Power Monitoring Function for detail.

R_OOBR_RSSI[7:0] : Result of the RSSI of interference wave at higher frequency
The RSSI result of interference wave at higher frequency can be read back. Refer to the chapter 13.8.3 Out of Band Power Monitoring Function for detail.

R_RSSI_BB[7:0] : RSSI result of desired and interference wave
The RSSI result of desired and interference wave for use in AGC circuit calculation can be read back. Refer to the chapter 13.8.10 AGC Function for detail.

14.11.4. <0x0C to 0D>READ NSQ

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x0C	R_NSQ1LVL[7:0]								R
Initial value	0	0	0	0	0	0	0	0	
0x0D	R_NSQ2LVL[7:0]								R
Initial value	0	0	0	0	0	0	0	0	

Refer to the chapter 13.8.16 Noise Squelch Function for detail.

R_NSQ1LVL[7:0] : Output power measurement result of the NSQ1 function
The average value of the measured output power can be read back if the noise squelch 1 function is turned ON.

R_NSQ2LVL[7:0] : Output power measurement result of the NSQ2 function
The average value of the measured output power can be read back if the noise squelch 2 function is turned ON.

14.11.5. <0x0E>READ PGA

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x0E	X	X	R_PGA[5:0]						R
Initial value			0	0	0	0	0	0	

R_PGA[5:0] : PGA gain
The gain set in the PGA can be read back if the address of this register is written to. The AGC calculation result is read back if <Address0x30>PGA_AGCON bit = “1” is set. The value set by <Address0x35>PGAGAIN[5:0] bits is read back if PGA_AGCON bit = “0” is set.

14.11.6. <0x10 to 11>READ ANA OFST

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x10	X	X	R_OFSTA_I[5:0]						R
Initial value			1	0	0	0	0	0	
0x11	X	X	R_OFSTA_Q[5:0]						R
Initial value			1	0	0	0	0	0	

Refer to the chapter 13.8.8 DC Offset Calibration for detail.

R_OFSTA_I[5:0] : DC offset calibration result of the analog part (MIXER Ich)
R_OFSTA_Q[5:0] : DC offset calibration result of the analog part (MIXER Qch)
It is possible to read back the DC offset calibration result of the analog part (MIXER) executed by setting <Address0x24>OFSCAL1 bit = “1”.

14.11.7. <0x12 to 17>READ DIG OFST

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x12	R_OFSTD_I[23:16]								R
Initial value	0	0	0	0	0	0	0	0	
0x13	R_OFSTD_I[15:8]								R
Initial value	0	0	0	0	0	0	0	0	
0x14	R_OFSTD_I[7:0]								R
Initial value	0	0	0	0	0	0	0	0	
0x15	R_OFSTD_Q[23:16]								R
Initial value	0	0	0	0	0	0	0	0	
0x16	R_OFSTD_Q[15:8]								R
Initial value	0	0	0	0	0	0	0	0	
0x17	R_OFSTD_Q[7:0]								R
Initial value	0	0	0	0	0	0	0	0	

Refer to the chapter 13.8.8 DC Offset Calibration for detail.

R_OFSTD_I[23:0] : DC offset calibration result of the digital part (main path Ich)
R_OFSTD_Q[23:0] : DC offset calibration result of the digital part (main path Qch)
It is possible to read back the DC offset calibration result of the digital part (main path) executed by setting <Address0x24>OFSCAL2 bit = “1”.

14.11.8. <0x18 to 1D>READ DIG OFST (OOB)

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x18	R_OFSTD_OOBI[23:16]								R
Initial value	0	0	0	0	0	0	0	0	
0x19	R_OFSTD_OOBI[15:8]								R
Initial value	0	0	0	0	0	0	0	0	
0x1A	R_OFSTD_OOBI[7:0]								R
Initial value	0	0	0	0	0	0	0	0	
0x1B	R_OFSTD_OOBQ[23:16]								R
Initial value	0	0	0	0	0	0	0	0	

0x1C	R_OFSTD_OOBQ[15:8]								R
Initial value	0	0	0	0	0	0	0	0	
0x1D	R_OFSTD_OOBQ[7:0]								R
Initial value	0	0	0	0	0	0	0	0	

Refer to the chapter 13.8.8 DC Offset Calibration for detail.

R_OFSTD_OOBI[23:0] : DC offset calibration result of the Out of Band Power Monitoring path (Ich)
R_OFSTD_OOBQ[23:0] : DC offset calibration result of the Out of Band Power Monitoring path (Qch)
It is possible to read back the DC offset calibration result of the out of band power monitoring path executed by setting <Address0x24>OFSCAL2 bit = “1”.

14.11.9. <0x1E to 23>READ AGC OFST

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x1E	X	X	X	X	X	X	X	X	R
Initial value									
0x1F	R_AGCOFS_I[15:8]								R
Initial value	0	0	0	0	0	0	0	0	
0x20	R_AGCOFS_I[7:0]								R
Initial value	0	0	0	0	0	0	0	0	
0x21	X	X	X	X	X	X	X	X	R
Initial value									
0x22	R_AGCOFS_Q[15:8]								R
Initial value	0	0	0	0	0	0	0	0	
0x23	R_AGCOFS_Q[7:0]								R
Initial value	0	0	0	0	0	0	0	0	

Refer to the chapter 13.8.8 DC Offset Calibration for detail.

R_AGCOFS_I[15:0] : DC offset calibration result of the AGC circuit (Ich)
R_AGCOFS_Q[15:0] : DC offset calibration result of the AGC circuit (Qch)
It is possible to read back the DC offset calibration result of the AGC circuit executed by setting <Address0x24>OFSCAL2 bit = “1”.

14.11.10. <0x24 to 29>READ RDOC

Address	D7	D6	D5	D4	D3	D2	D1	D0	W/R
0x24	R_RDOC_I[23:16]								R
Initial value	0	0	0	0	0	0	0	0	
0x25	R_RDOC_I[15:8]								R
Initial value	0	0	0	0	0	0	0	0	
0x26	R_RDOC_I[7:0]								R
Initial value	0	0	0	0	0	0	0	0	
0x27	R_RDOC_Q[23:16]								R
Initial value	0	0	0	0	0	0	0	0	
0x28	R_RDOC_Q[15:8]								R

Initial value	0	0	0	0	0	0	0	0	
0x29	R_RDOC_Q[7:0]								R
Initial value	0	0	0	0	0	0	0	0	

Refer to the chapter 13.8.9 RDOC Function for detail.

R_RDOC_I[23:0] : DC offset correction value of the RDOC circuit (Ich)
R_RDOC_Q[23:0] : DC offset correction value of the RDOC circuit (Qch)
It is possible to read back the amount of DC offset cancelled by the RDOC circuit when <Address0x62> RDOC_ON bit = “1” is set.

15. External Circuit

15.1. Reference Evaluation Board

The schematic example, parts list and layout diagram of the standard evaluation board used for the evaluation are shown below. The characteristics listed in the chapter 10.1.1 LNA, 10.1.2 ATT and 10.1.3 PDET are evaluated by the Schematic Example 2.

■ Schematic Example 1

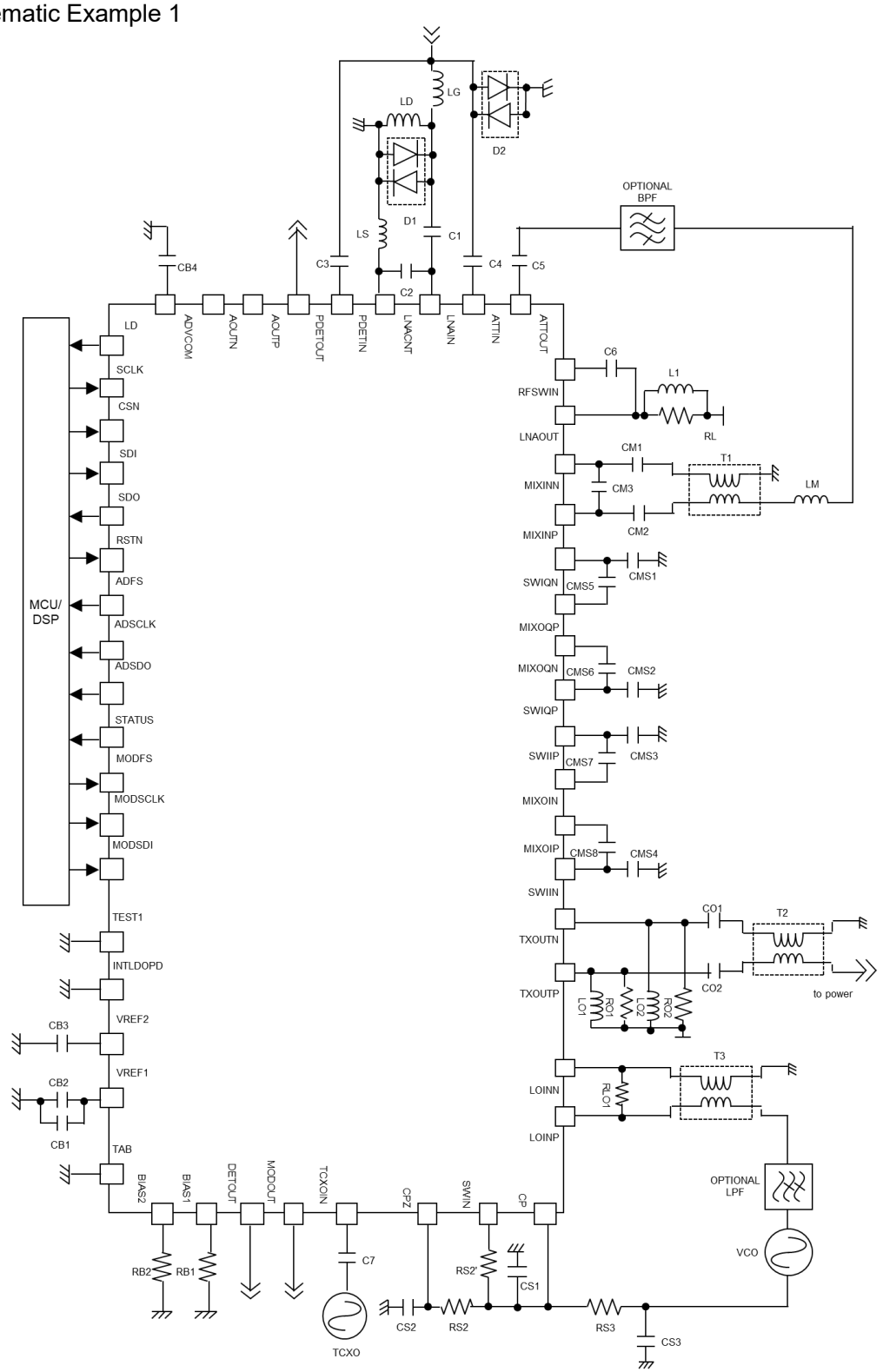


Figure 80 Reference Evaluation Board Example 1

■ Schematic Example 2

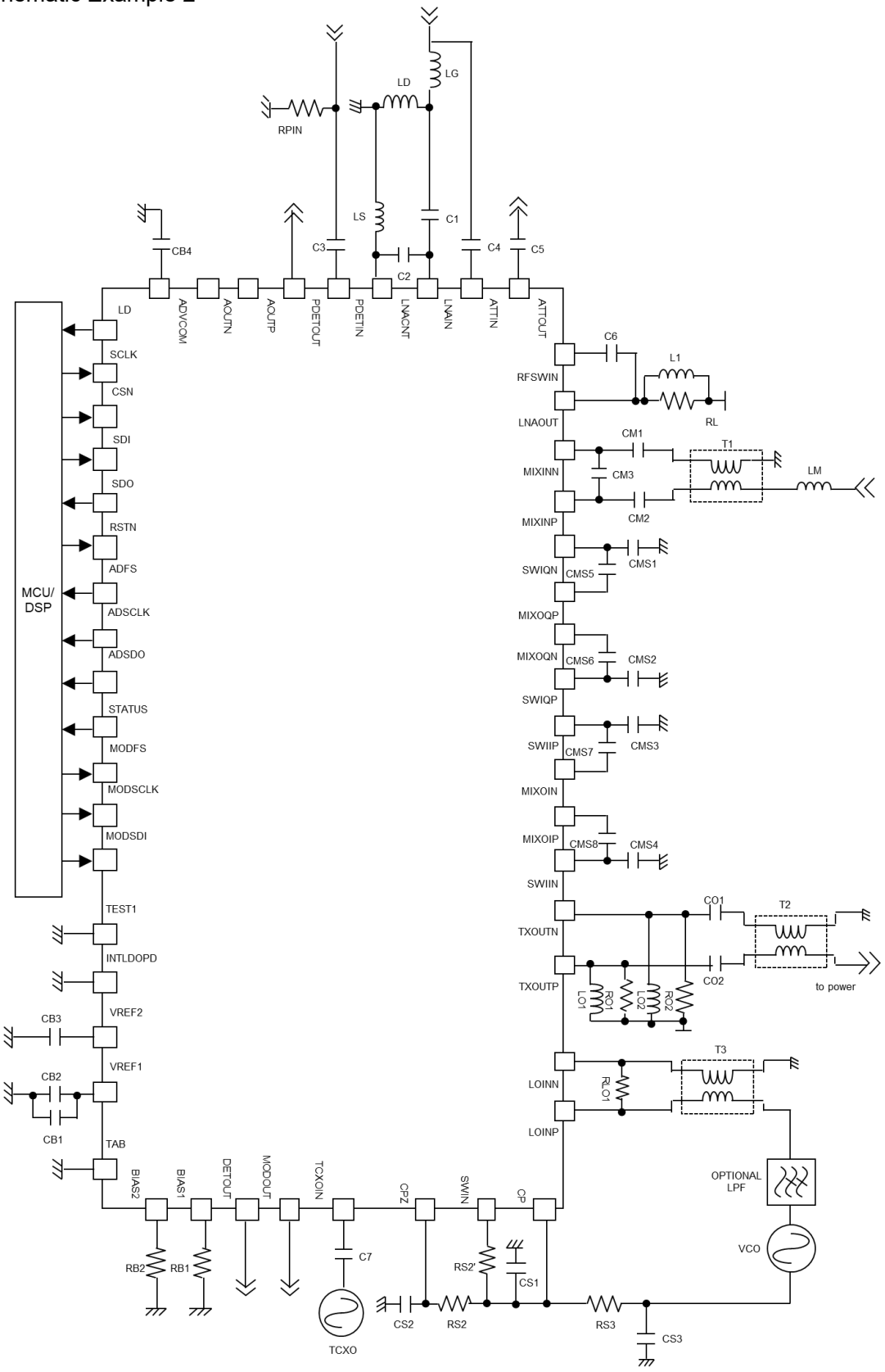


Figure 81 Reference Evaluation Board Example 2

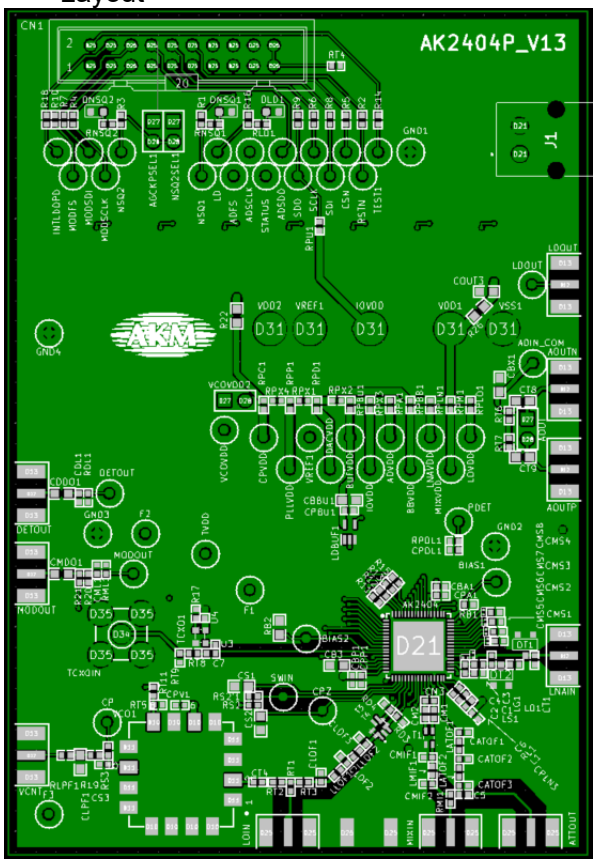
■ Parts list

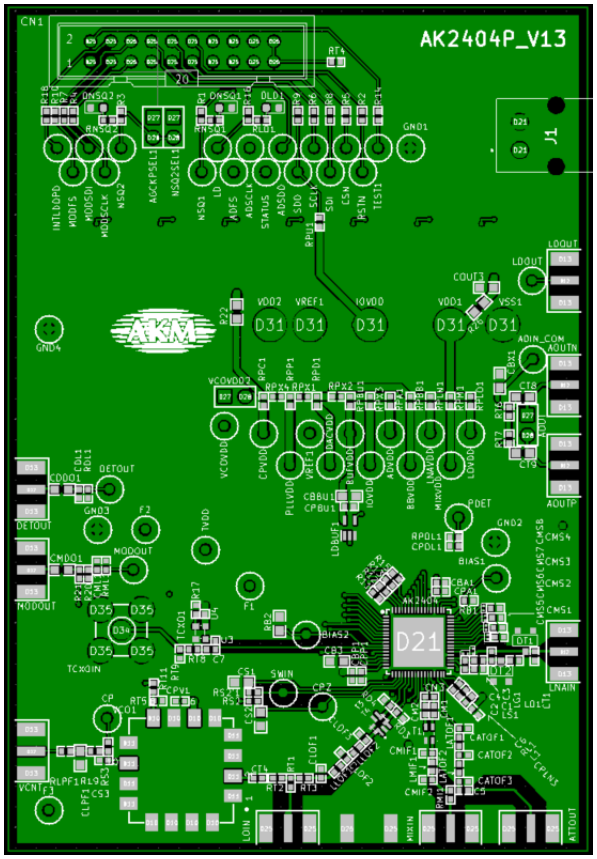
Table 64. Parts List for External Circuit Connection

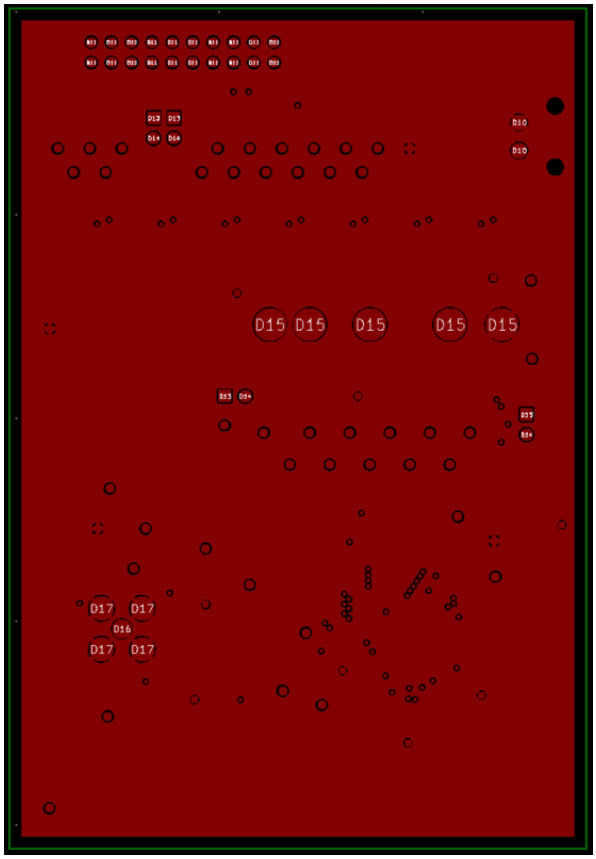
Ref.	Value	Description	Ref.	Value	Description
LG	100pF	LNAIN=450MHz High Power Mode	C3	0.5pF	DC Cut (C3: ±0.03pF product recommended)
LS	2.4nH		C4	100pF	
C2	3.0pF		C5	100pF	
C1	100pF		C7	100pF	
LD	-		T2	1:1	DXW21HN5011B
D1, D2	-		RO1	27Ω	TXOUT Wideband Matching
LG	100pF	LNAIN=450MHz Low Power Mode	RO2	27Ω	
LS	2.4nH		LO1	120nH	
C2	1.6pF		LO2	120nH	
C1	100pF		CO1	1nF	
LD	-		CO2	1nF	
D1	-		RS2	-	LOOP FILTER
RL	200Ω	LNAOUT=450MHz (RL: ±1% product recommended)	RS2’	-	
L1	22nH		RS3	-	
C6	5.0pF		CS1	-	
T1	1:1	DXW21HN5011B	CS2	-	
CM1	1nF	MIXIN Wideband Matching	CS3	-	
CM2	1nF		T3	1:1	DXW21HN5011B
CM3	1.6pF		RLO1	51Ω	LOIN Wideband Matching
LM	3.9nH				
CMS1	0.047μF	±5% product recommended	CB1	10μF	
CMS2	0.047μF		CB2	100pF	
CMS3	0.047μF		CB3	0.47μF	
CMS4	0.047μF		CB4	2.2μF	
CMS5	2700pF	±5% product recommended	RPIN	51Ω	PDETIN Matching
CMS6	2700pF				
CMS7	2700pF				
CMS8	2700pF				
RB1	47kΩ	±1% product recommended			
RB2	27kΩ	±1% product recommended	-	-	

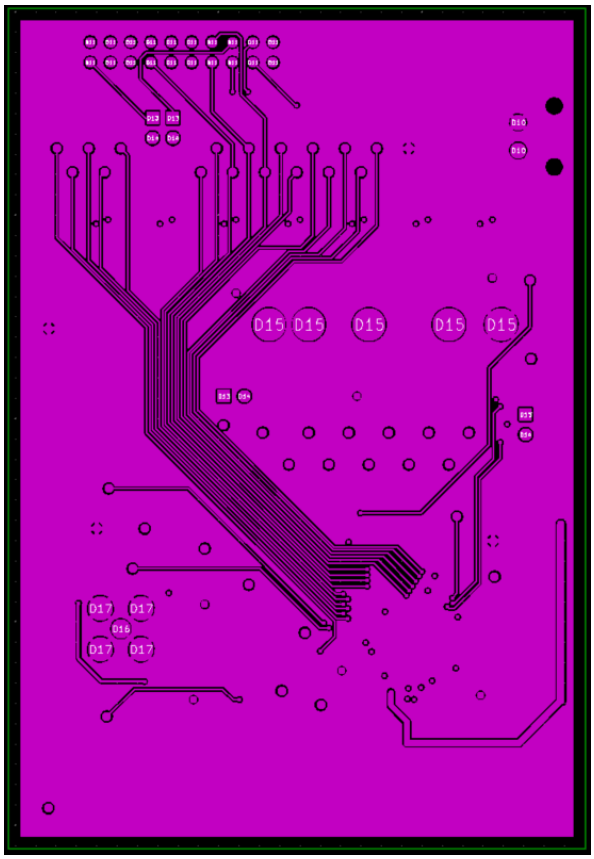
* The examples of matching circuit at the frequency except 450MHz are prepared in the application note. Please inquire separately.
* The AKM evaluation board uses the coil inductors.
* The AKM evaluation board uses the SMP1330-005LF for the diode D1 and D2.

■ Layout



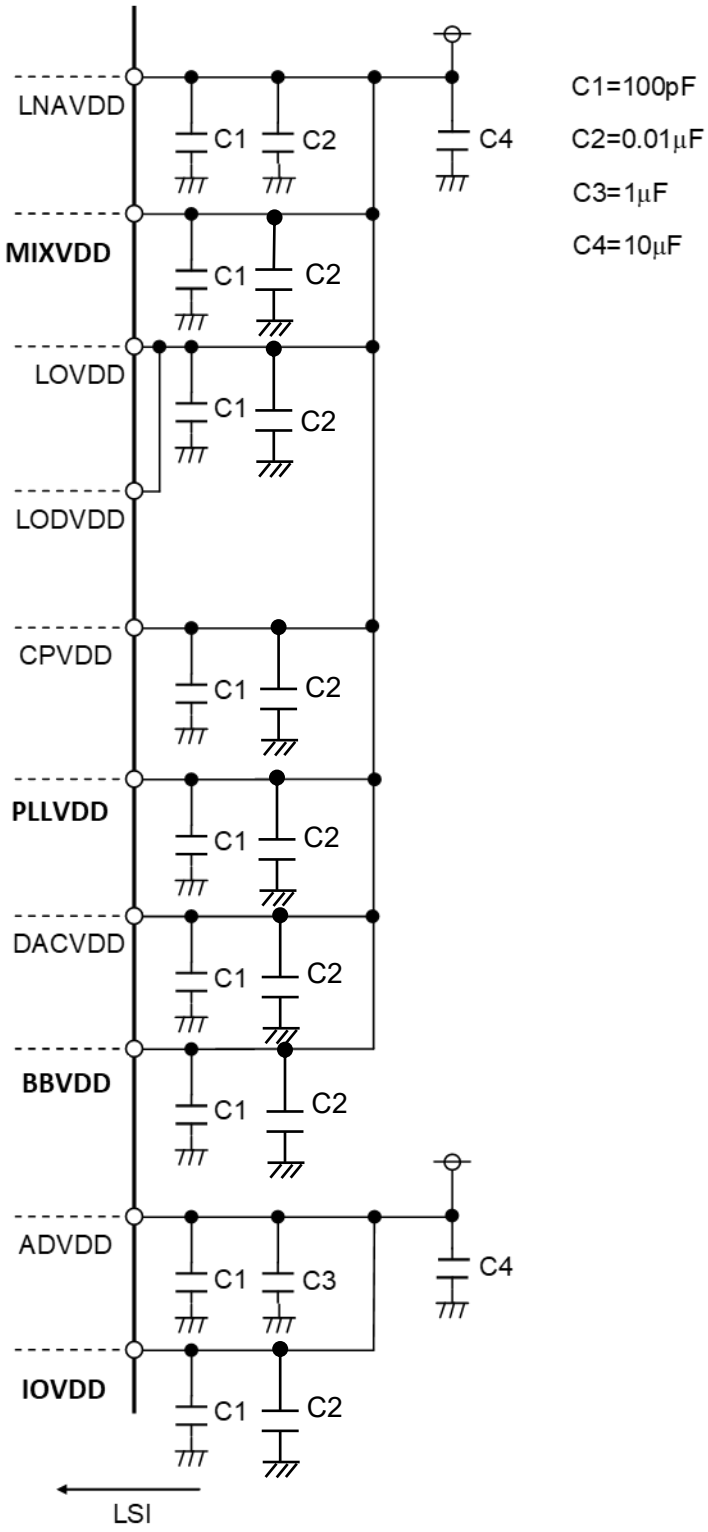






15.2. Power pins and ground pins

Connect the capacitors between VDD and VSS pins as shown in the figure below to remove the ripple, noise, and so on included in the power. The capacitors should be placed at the shortest distance between both pins for best results.

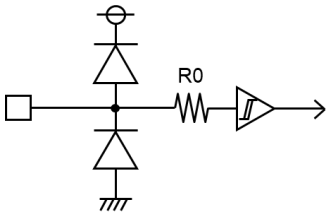
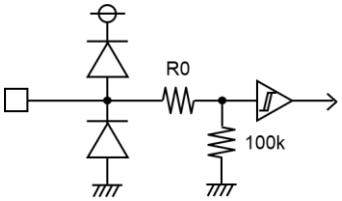
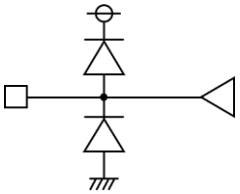
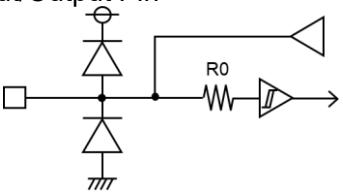
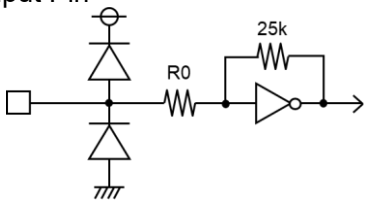
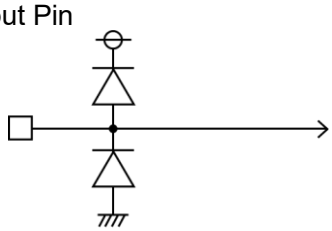
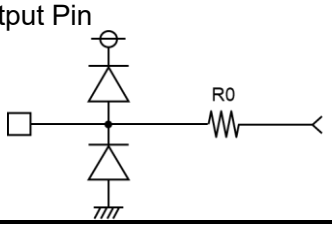


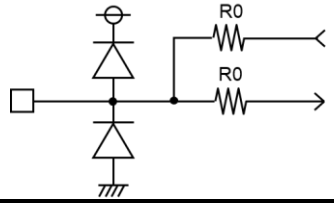
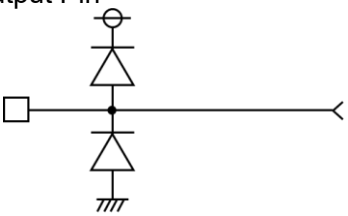
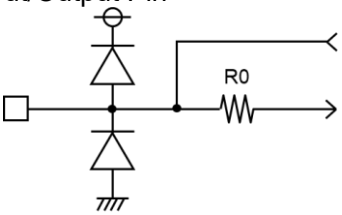
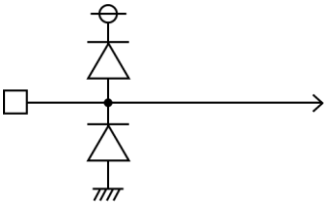
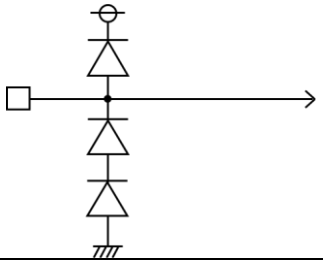
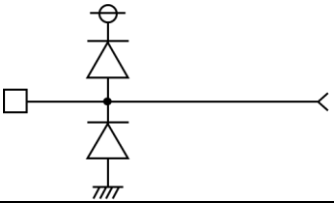
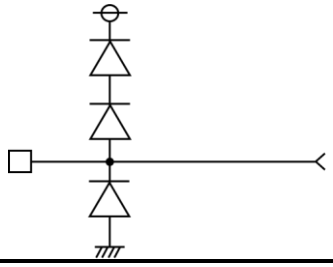
15.3. Board design

The following is a board design guideline confirmed under the conditions of our evaluation board, and is not intended to specify the layout pattern or guarantee the characteristics of the customer's board.

- Connect the exposed pad at the center of back side to the low impedance analog ground. If the exposed pad is not connected and left open, the operation may become unstable.
- The 24-bit ΔΣ ADC divides the reference clock input from the TCXOIN pin by 4 and uses it. If the CLOCK RATE CONVERTER is used, the output of the CLOCK RATE CONVERTER is divided by 4 and used. Therefore, the clock frequency used for the ΔΣ ADC and its harmonic components go around the input of the LNA and causes reception sensitivity suppression when using the AK2404 with that frequency selected as the RF frequency. Therefore, if the used RF frequency is a multiple of the clock frequency used for the ΔΣ ADC, evaluate its capability thoroughly to use. The impact can be mitigated by paying attention to the points listed below with our evaluation board.
- Do not separate each VSS but connect them to the same analog ground. The analog ground improves the spurious characteristic by taking a wider ground plane and making it low impedance.
- The exposed pad in the center of the back side and each VSS pin are shorted in the top layer of the board to improve the spurious characteristic.
- The power pins need to be cared so that the spurious does not go around to the LNA because the ADVDD and IOVDD are the main source of the spurious. In addition to a 100pF decoupling capacitor connected to each power supply pin, an additional capacitor of 0.01μF is connected to the LNAVDD pin and an additional capacitor of 1μF is connected to the ADVDD pin. The digital signal line of the ADSCLK and the power source line of the LNAVDD should be separated as much as possible to ensure isolation.
- Each power supply pin is wired from the LDO and so on with low impedance without connecting a ferrite beads and so on in series. Only for the LNAVDD pin, connecting a resistor of 1Ω in series may improve the spurious characteristic.
- The spurious characteristic is deteriorated by the harmonic noise of the ADSCLK, ADSDO and ADFS pins. Connect dumping resistors of 100Ω in series to these pins. The digital signal lines should be wired in the inner layer.
- The decoupling capacitors, especially the ceramic capacitors of small capacity, should be mounted as close to the AK2404 as possible.
- Use a balun which matches the used frequency band for the balun connected to the TXOUTP and TXOUTN pins. A separate power supply is necessary via an inductor if a balun without the center tap is used because the TXOUTP and TXOUTN pins are open collector.
- Since the capacitors connected to the VREF1 and VREF2 pins with ground are used to stable the internal circuit, mount the capacitors of specified value.
- Do not open all digital input pins.

16. LSI interface circuit

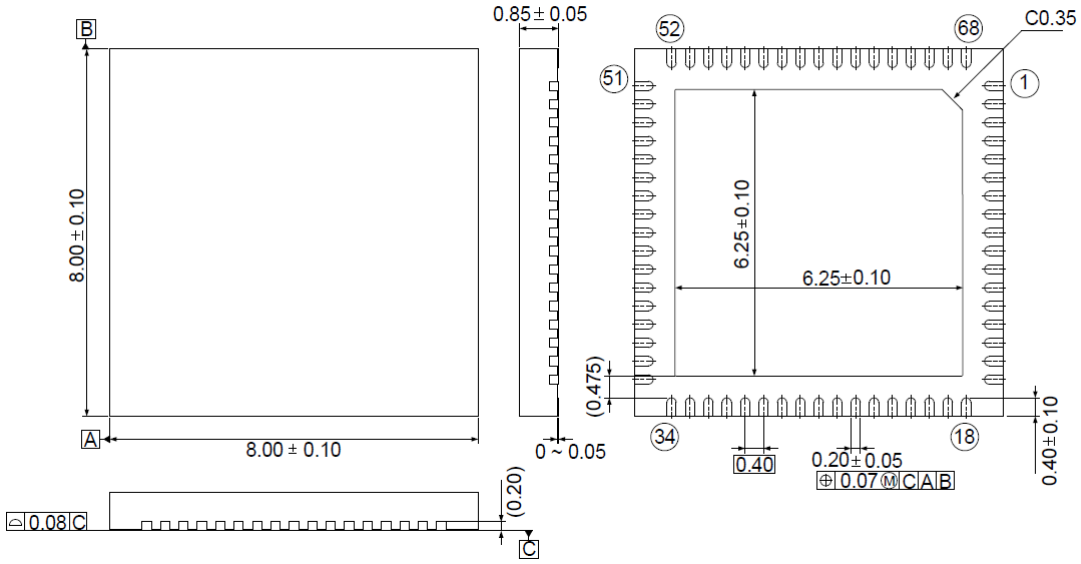
Pin#	Name	I/O	R0[Ω]	Function
5	MODSCLK	I	300	Digital Input Pin 
6	MODSDI	I	300	
7	MODFS	I	300	
14	INTLDOPD	I	300	
59	RSTN	I	300	
60	CSN	I	300	
61	SDI	I	300	
62	SCLK	I	300	
58	TEST1	I	300	Digital Input Pin Pull-Down 
2	LD	O		Digital Output Pin 
3	NSQ1	O		
63	SDO	O		
64	ADSDO	O		
65	STATUS	O		
66	ADSCLK	O		
67	ADFS	O		
4	NSQ2	IO		Digital Input/Output Pin 
13	TCXOIN	I	300	Analog Input Pin 
20	SWIN	I		Analog Input Pin 
21	CPZ	I		
42	SWIIN	I		
45	SWIIP	I		
46	SWIQP	I		
49	SWIQN	I		
52	AOUTP	O	300	Analog Output Pin 
53	AOUTN	O	300	

54	PDETOUT	O	300	Analog Output Pin 
43	MIXOIP	O		Analog Output Pin 
44	MIXOIN	O		
47	MIXOQN	O		
48	MIXOQP	O		
8	DETOUT	O	300	Analog Input/Output Pin 
9	MODOUT	O	300	
11	BIAS2	I	300	
12	VREF1	O	300	
15	VREF2	O	300	
19	CPOUT	O	300	
51	BIAS1	I	300	
57	ADVCOM	O	300	
28	MIXINP	I		RF Input Pin 
29	MIXINN	I		
33	RFSWIN	I		
37	LNACNT	I		
38	LNAIN	I		
40	ATTIN	I		
22	LOINP	I		RF Input Pin 
23	LOINN	I		
41	PDETIN	I		
32	ATTOUT	O		RF Output Pin 
25	TXOUTP	O		RF Output Pin 
26	TXOUTN	O		
34	LNAOUT	O		

17. Package

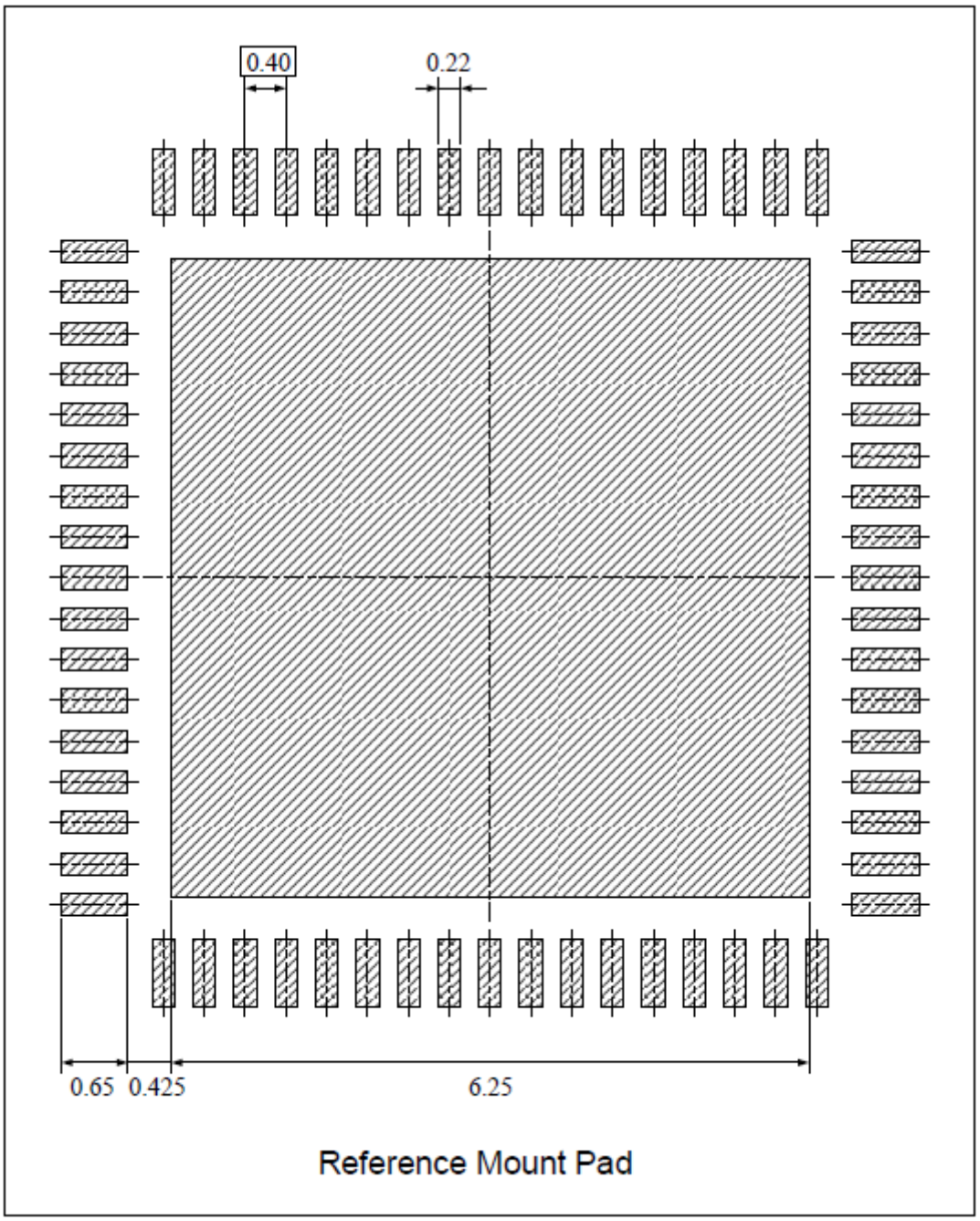
17.1. Output Dimensions

68-pin QFN 8.0mm x 8.0mm x 0.85mm, 0.4mm pitch
(Unit:mm)



Connect the exposed pad in the center of back side to the VSS.

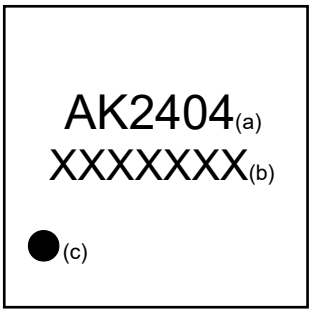
17.2. Pad Dimensions (for reference)



The exposed pad on the back of the package should be connected to the VSS.

The recommended Land-pattern is described above, however, please note that the most suitable dimension for mounting-pad will vary according to following conditions, :Materials of PCB, Kind of soldering paste, soldering method, accuracy of soldering machine, so on.
So, for your actual design for Land-pattern, you should optimize it to your actual condition.

17.3. Marking



a: Product number : AK2404
b: Date code : XXXXXXX
c: 1 pin marking: ●

18. Ordering Guide

AK2404 68-pin QFN (8.0mm x 8.0mm x 0.85mm, 0.4mm pitch)
AKD2404 AK2404 evaluation board

19. Revision history

Date (Y/M/D)	Revision	Reason	Page	Contents
2022/10/12	00	Initial version		
2022/10/18	01	Correction		Corrected errors across all pages.
2022/10/18	01	Correction	164	Added date to the Date section of the Initial version of the Revision history.
2022/10/20	02	Correction		Corrected datasheet number in footer
2023/02/17	03	Correction	105	Correction of S5-S3 output description
2023/04/17	04	Notation correction	1	Specify the standards in which the blocking characteristic of 100dB is achieved. Deleted the description of “the highest level in the industry”.

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