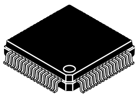
MC33772C

Battery cell controller IC

Rev. 4.1 — 6 March 2026 **Product data sheet**



1 General description

The MC33772C is a SMARTMOS lithium-ion battery cell controller IC designed for automotive applications, such as hybrid electric (HEV) and electric vehicles (EV) along with industrial applications, such as energy storage systems (ESS) and uninterruptible power supply (UPS) systems.

The device performs ADC conversions of the differential cell voltages and current, as well as battery coulomb counting and battery temperature measurements. The information is transmitted to MCU using one of the microcontroller interfaces: serial peripheral interface (SPI) or isolated daisy chain communication interface [also referred as transformer physical layer (TPL)] which supports both capacitive and inductive isolation between nodes of the IC. The product is AEC-Q100 qualified and operates up to 125 °C ambient temperature.

2 Features

- 5.0 V ≤ V_{PWR} ≤ 30 V operation, 40 V transient
- 3 to 6 cells management
- Isolated 2.0 Mbit/s differential communication or 4.0 Mbit/s SPI
- Addressable on initialization
- Bi-directional transceiver to support up to 63 nodes in daisy chain
- 0.8 mV total voltage measurement error
- Synchronized cell voltage/current measurement with coulomb count
- Averaging of cell voltage measurements
- Total stack voltage measurement
- Seven GPIO/temperature sensor inputs
- 5.0 V at 5.0 mA reference supply output
- Automatic over/undervoltage and temperature detection routable to fault pin
- Integrated sleep mode over/undervoltage and temperature monitoring
- Onboard 300 mA passive cell balancing with diagnostics
- Hot plug capable
- Detection of internal and external faults, as open lines, shorts, and leakage
- Designed to support ISO 26262, up to ASIL D safety system
- Fully compatible with the MC33771C and the MC33664
- Qualified in compliance with AEC-Q100

3 Simplified application diagram

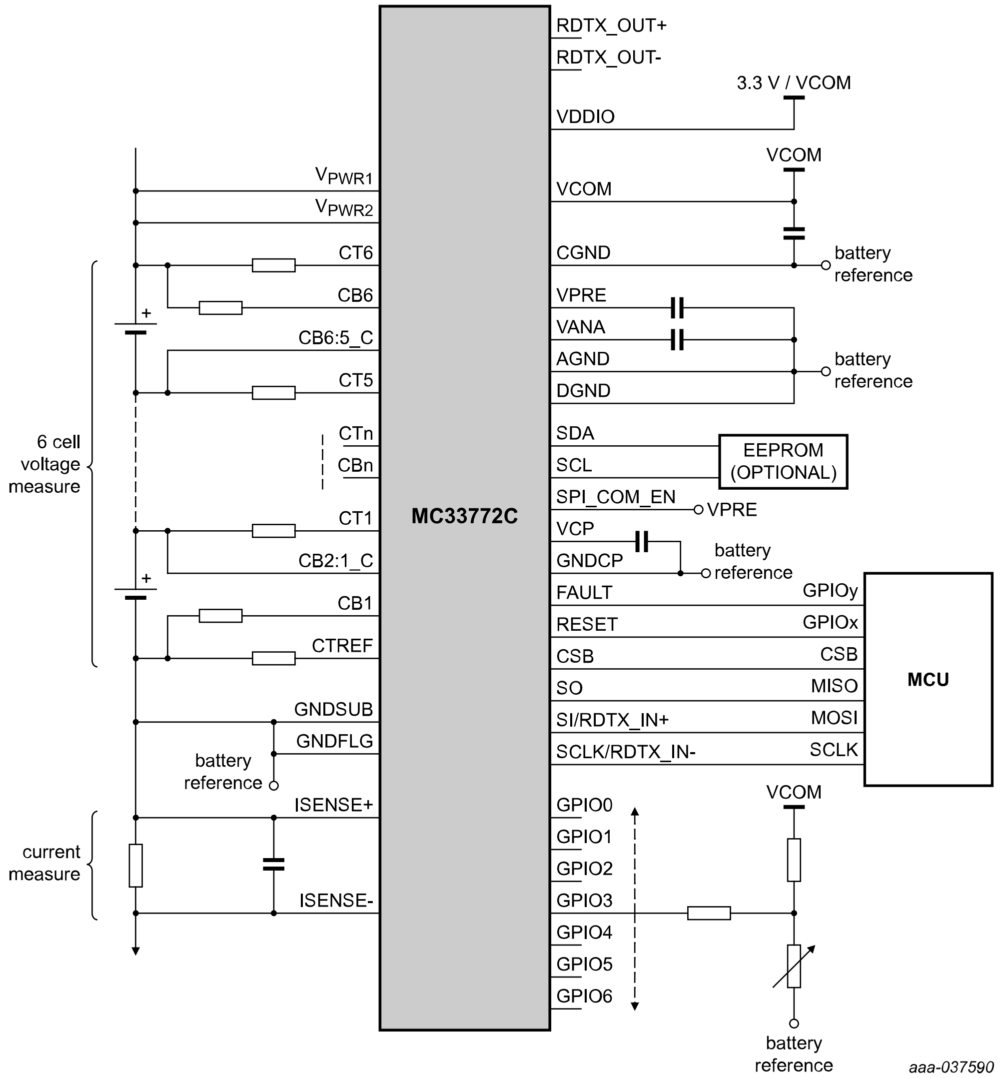


Figure 1. Simplified application diagram, SPI use case

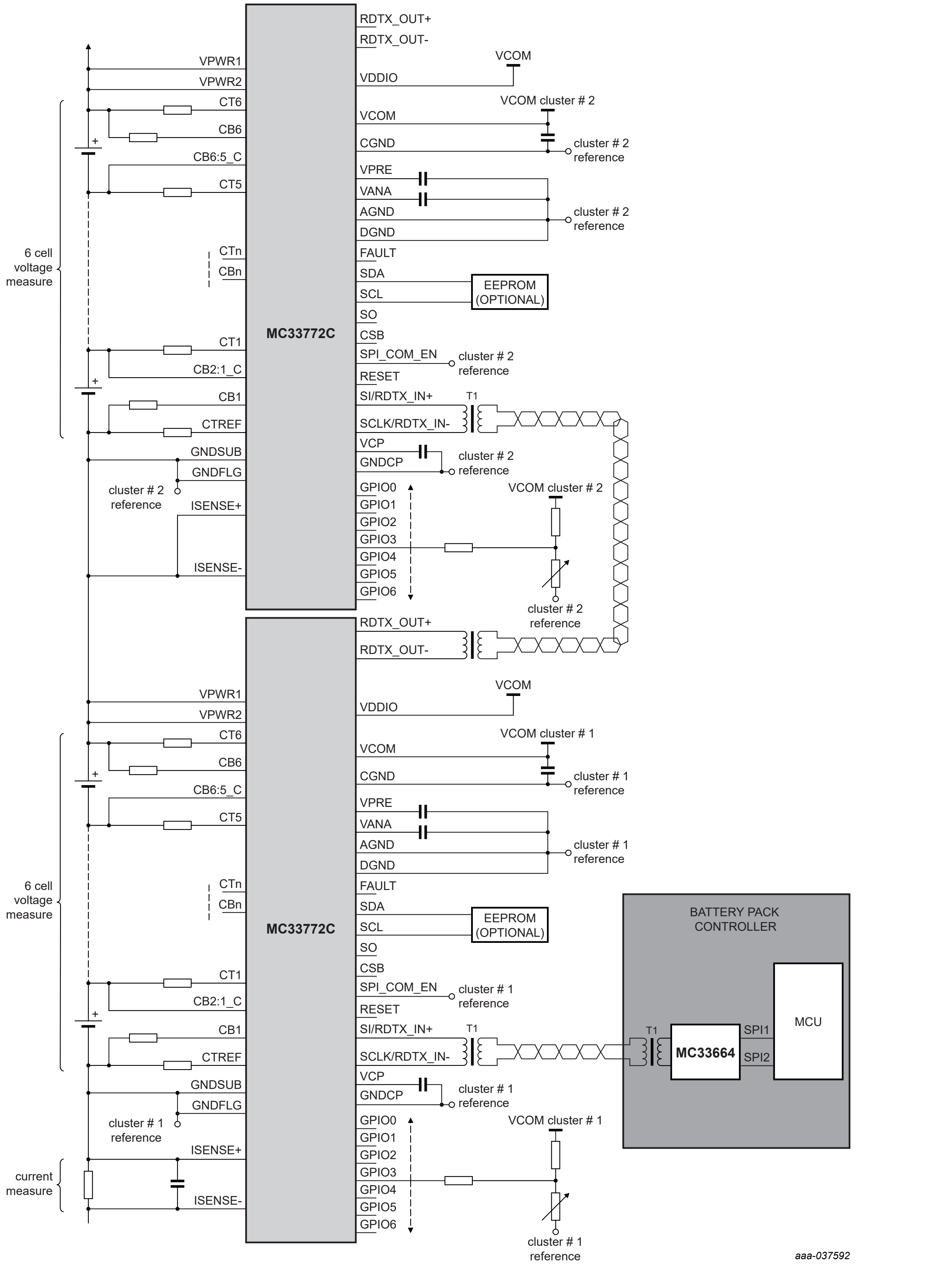


Figure 2. Simplified application diagram, TPL use case

4 Applications

- Automotive: 12 V and high-voltage battery packs
- E-bikes, e-scooters, drones
- Energy storage systems
- Uninterruptible power supply (UPS)
- Battery junction box

5 Ordering information

5.1 Part numbers definition

MC33772C x y z AE/R2

Table 1. Part number breakdown

Code	Option	Description
x	T	x = T (TPL communication type)
y	A	y = A (Advanced)
	C	y = C (Current)
	P	y = P (Premium)
z	0	z = 0 (0 channels)
	1	z = 1 (3 to 6 channels)
	2	z = 2 (3 to 4 channels)
	AE	Package suffix
	R2	Tape and reel indicator

5.2 Part numbers list

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com.

Table 2. Advanced orderable part table

Package type is 48-pin LQFP-EP

Orderable part	Number of channels	OV/UV	Precision GPIO as temperature channels and OT/UT	Current channel or coulomb count
TPL differential communication protocol				
MC33772CTA1AE	3 to 6	Yes	Yes	No
MC33772CTA2AE	3 to 4	Yes	Yes	No

Table 3. Premium orderable part table

Package type is 48-pin LQFP-EP

Orderable part	Number of channels	OV/UV	Precision GPIO as temperature channels and OT/UT	Current channel or coulomb count
TPL differential communication protocol with current measurement option				
MC33772CTP1AE	3 to 6	Yes	Yes	Yes
MC33772CTP2AE	3 to 4	Yes	Yes	Yes

Table 4. Current orderable part table

Package type is 48-pin LQFP-EP

Orderable part	Number of channels	OV/UV	Precision GPIO as temperature channels and OT/UT	Current channel or coulomb count
TPL differential communication protocol				
MC33772CTC0AE	0	No	Yes	Yes
MC33772CTC1AE	1	No	Yes	Yes

Note: *To order parts in tape and reel, add an R2 suffix to the part number.*

6 Block diagram

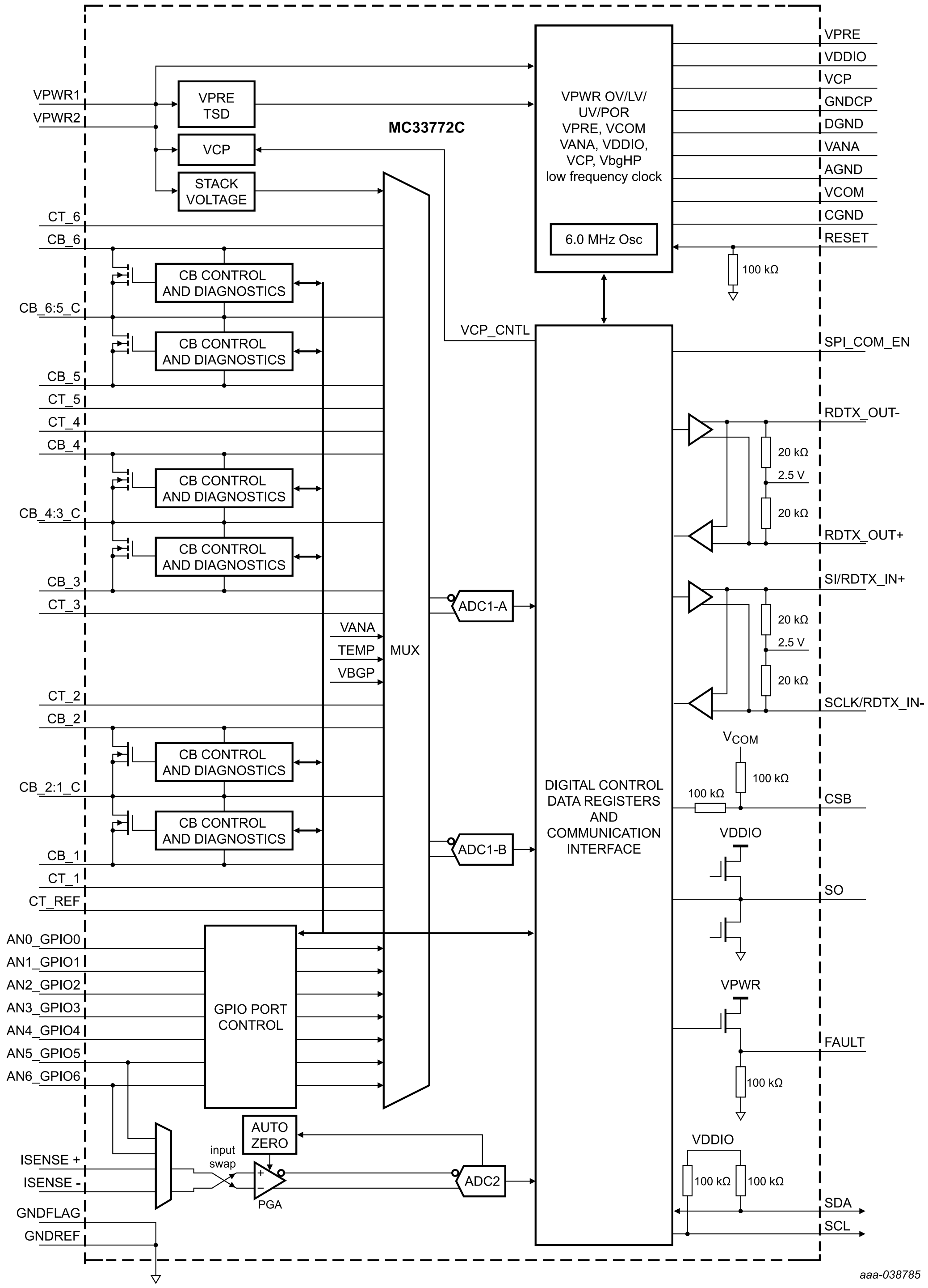


Figure 3. Simplified internal block diagram

7 Pinning information

7.1 Pinout diagram

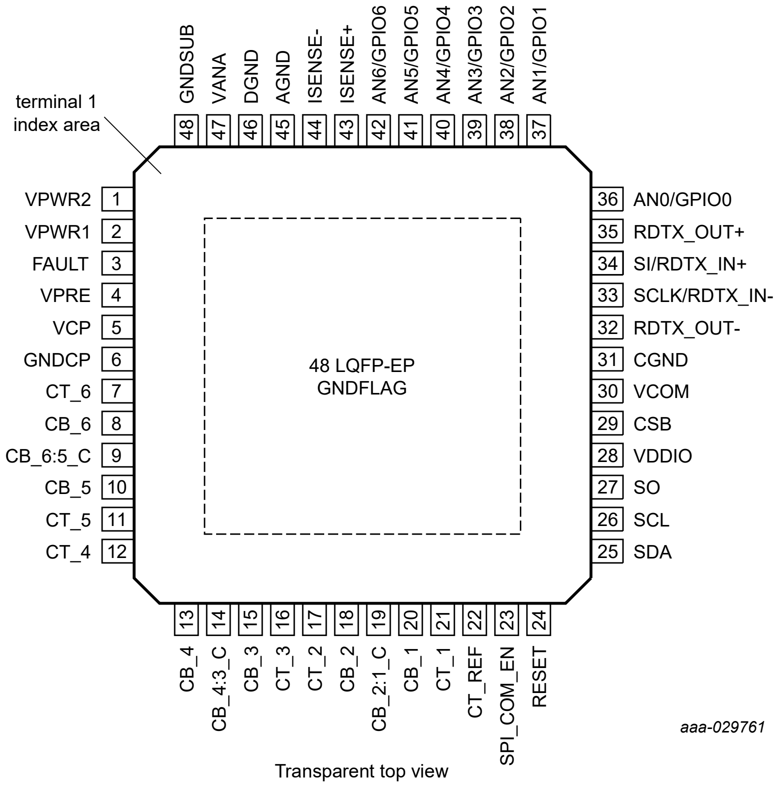


Figure 4. Pinout diagram

7.2 Pin definitions

Table 5. Pin definitions

Pin number	Pin name	Pin function	Definition
1	VPWR2	Input	Power supply input to the MC33772C
2	VPWR1	Input	Power supply input to the MC33772C
3	FAULT	Output	Fault output dependent on user defined internal or external faults. If not used, it must be left open
4	VPRE	Output	Pre-regulator voltage. Connect to a 470 nF capacitor
5	VCP	Output	Charge pump. Decouple with a 10 nF capacitor
6	GNDCP	Ground	Charge pump capacitor ground
7	CT_6	Input	Cell terminal pin 6 input. Terminate to LPF resistor
8	CB_6	Output	Cell balance driver. Terminate to cell 6 cell balance load resistor
9	CB_6:5_C	Output	Cell balance 6:5 common. Terminate to cell 6 and 5 common pin
10	CB_5	Output	Cell balance driver. Terminate to cell 5 cell balance load resistor
11	CT_5	Input	Cell terminal pin 5 input. Terminate to LPF resistor
12	CT_4	Input	Cell terminal pin 4 input. Terminate to LPF resistor
13	CB_4	Output	Cell balance driver. Terminate to cell 4 cell balance load resistor

Table 5. Pin definitions*...continued*

Pin number	Pin name	Pin function	Definition
14	CB_4:3_C	Output	Cell balance 4:3 common. Terminate to cell 4 and 3 common pin
15	CB_3	Output	Cell balance driver. Terminate to cell 3 cell balance load resistor
16	CT_3	Input	Cell terminal pin 3 input. Terminate to LPF resistor
17	CT_2	Input	Cell pin 2 input. Terminate to LPF resistor
18	CB_2	Output	Cell balance driver. Terminate to cell 2 cell balance load resistor
19	CB_2:1_C	Output	Cell balance 2:1 common. Terminate to cell 2 and 1 common pin
20	CB_1	Output	Cell balance driver. Terminate to cell 1 cell balance load resistor
21	CT_1	Input	Cell pin 1 input. Terminate to LPF resistor
22	CT_REF	Input	Cell terminal REF input. Terminate to LPF resistor
23	SPI_COM_EN	Input	SPI communication enable input. Wire to VPRE to use SPI communication, else wire to ground to use TPL communication
24	RESET	Input	RESET is an active high input. RESET has an internal pull down. If not used, it can be shorted to GND
25	SDA	I/O	I^2C data
26	SCL	I/O	I^2C clock
27	SO	Output	SPI serial output
28	VDDIO	Input	IO voltage for I^2C and SPI interfaces. Voltage level corresponding to logic 1 will be the same as VDDIO
29	CSB	Input	SPI active low chip select. If not used, it must be shorted to ground
30	VCOM	Output	Communication regulator output. Decouple with 2.2 µF to CGND
31	CGND	Ground	Communication decoupling ground, terminate to GNDSUB
32	RDTX_OUT−	I/O	TPL receive/transmit output negative
33	SCLK/RDTX_IN-	I/O	SPI clock or TPL receive/transmit input negative
34	SI/RDTX_IN+	I/O	SPI serial input or TPL receive/transmit input positive
35	RDTX_OUT+	I/O	TPL receive/transmit output positive
36	AN0 GPIO0	I/O	General purpose input/output
37	AN1 GPIO1	I/O	General purpose input/output
38	AN2 GPIO2	I/O	General purpose input/output
39	AN3 GPIO3	I/O	General purpose input/output
40	AN4 GPIO4	I/O	General purpose input/output
41	AN5 GPIO5	I/O	General purpose input/output
42	AN6 GPIO6	I/O	General purpose input/output
43	ISENSE+	Input	Current measurement input +
44	ISENSE−	Input	Current measurement input −
45	AGND	I/O	Analog ground, terminate to GNDSUB
46	DGND	I/O	Digital ground, terminate to GNDSUB
47	VANA	Output	Precision ADC analog supply. Decouple with 47 nF capacitor to AGND
48	GNDSUB	Ground	Ground reference for device, terminate to reference of battery cluster
49	GNDFLAG	Ground	Exposed pad, terminate to lowest potential of the battery cluster and to heat dissipation area of PCB

8 General product characteristics

8.1 Ratings and operating requirements relationship

The operating voltage range pertains to the VPWR pins referenced to the AGND pins.

Table 6. Ratings vs. operating requirements

Fatal range Permanent failure may occur	Lower limited operating range No permanent failure, but IC functionality is not guaranteed	Normal operating range 100 % functional	Upper limited operating range	Fatal range Permanent failure may occur
V_{PWR} < −0.3 V	5.0 V ≤ V_{PWR} ≤ 6.0 V (SPI) 6.4 V ≤ V_{PWR} ≤ 7.0 V (TPL) **Reset range:** –0.3 V ≤ V_{PWR} ≤ 5.0 V (SPI) –0.3 V ≤ V_{PWR} ≤ 6.4 V (TPL) **POR with V_{PWR} falling:** 4.8 V ≤ V_{PWR} < 5.0 V (SPI) 6.1 V ≤ V_{PWR} < 6.4 V (TPL) **POR with V_{PWR} rising:** 5.6 V ≤ V_{PWR} < 6.0 V (SPI) 6.6 V ≤ V_{PWR} < 7.0 V (TPL)	6.0 V ≤ V_{PWR} ≤ 30 V (SPI) 7.0 V ≤ V_{PWR} ≤ 30 V (TPL)	30 V < V_{PWR} ≤ 40 V **IC parameters might be out of specification. Detection of V_{PWR} overvoltage is functional**	40 V < V_{PWR}
	Handling range - No permanent failure			

In both upper and lower limited operating range, no information can be provided about IC performance. Only the detection of V_{PWR} overvoltage is guaranteed in the upper limited operating range.

Performance in normal operating range is guaranteed only if there is a minimum of three battery cells in the stack.

8.2 Maximum ratings

Table 7. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings might cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min	Max	Unit
Electrical ratings				
VPWR1, VPWR2	Supply input voltage	–0.3	40	V
CT6	Cell terminal voltage	−0.3	40	V
VPWR to CT6	Voltage across VPWR1,2 pins pair and CT6 pin	−10	10	V
CT_N to CT_{N-1}	Cell terminal differential voltage [1]	−0.3	6.7	V
$CT_{N(CURRENT)}$	Cell terminal input current	—	±500	µA
CB_N to $CB_{N:N-1\_C}$ $CB_{N:N-1\_C}$ to CB_{N-1}	Cell balance differential voltage	—	10	V
CB_{N-1} to CT_{N-1}	Cell balance input to cell terminal input	−10	+10	V
VISENSE	ISENSE+ and ISENSE– pin voltage	−0.5	2.5	V
VCOM	Maximum voltage may be applied to VCOM pin from external source	—	5.8	V
VANA	Maximum voltage may be applied to VANA pin	—	3.1	V

Table 7. Maximum ratings...*continued*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings might cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min	Max	Unit
VPRE	Maximum voltage which may be applied to VPRE pin from external source	—	7.0	V
VCP	Maximum voltage which may be applied to VCP pin from external source	—	14	V
VDDIO	Maximum voltage which may be applied to VDDIO pin from external source	—	5.8	V
V_{GPIO0}	GPIO0 pin voltage	–0.3	6.5	V
V_{GPIOx}	GPIOx pins (x = 1 to 6) voltage	–0.3	VCOM + 0.5	V
V_{DIG}	Voltage I^2C pins (SDA, SCL)	–0.3	VDDIO + 0.5	V
V_{RESET}	RESET pin	–0.3	6.5	V
V_{CSB}	CSB pin	–0.3	6.5	V
$V_{SPI\_COMM\_EN}$	SPI_COMM_EN	–0.3	7.0	V
V_{SO}	SO pin	–0.3	VDDIO + 0.5	V
$V_{GPIO5,6}$	Maximum voltage for GPIO5 and GPIO6 pins used as current input	−0.3	2.5	V
FAULT	Maximum applied voltage to pin	−0.3	7.0	V
$I_{pin\_unpowered}$	Input current in a pin when the device is unpowered	−2	2	mA
V_{COMM}	Maximum voltage to pins RDTX_OUT+, RDTX_OUT–, SI/RDTX_IN+, CLK/RDTX_IN–	−10	10	V
V_{ESD1}	ESD voltage Human body model (HBM) Charge device model (CDM) Charge device model corner pins (CDM)	 — — —	 ±2000 ±500 ±750	V
V_{ESD2}	ESD voltage (VPWR1, VPWR2, CTx, CBx, GPIOx, ISENSE+, ISENSE–, RDTX_OUT+, RDTX_OUT–, SI/RDTX_IN+, SCLK/ RDTX_ IN–) [2] Human body model (HBM)	—	±4000	V
V_{ESD3}	ESD voltage (CTREF, CTx, CBx, GPIOx, ISENSE+, ISENSE−, RDTX_ OUT+, RDTX_OUT−, SI/RDTX_IN+, SCLK/ RDTX_IN−) [3] IEC 61000-4-2, Unpowered (Gun configuration: 330 Ω / 150 pF) HMM, Unpowered (Gun configuration: 330 Ω / 150 pF) ISO 10605:2009, Unpowered (Gun configuration: 2 kΩ / 150 pF) ISO 10605:2009, Powered (Gun configuration: 2 kΩ / 330 pF)	 — — — —	 ±8000 ±8000 ±8000 ±8000	V

[1] Adjacent CT pins may experience an overvoltage that exceeds their maximum rating during OV/UV functional verification test or during open line diagnostic test. Nevertheless, the IC is completely tolerant to this special situation.
[2] ESD testing is performed in accordance with the human body model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
[3] These voltage values can be sustained only if ESD caps are used as described in Section 13.2.

8.3 Thermal characteristics

Table 8. Thermal ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings might cause a malfunction or permanent damage to the device.

Symbol	Description (rating)		Min	Max	Unit
Thermal ratings					
 T_A T_A T_J	Operating temperature Ambient (SPI application) Ambient (TPL application) Junction[1]		 –40 –40 –40	 +125 +105 +150	°C
T_{STG}	Storage temperature		−55	+150	°C
T_{PPRT}	Peak package reflow temperature	[2] [3]	—	260	°C
Thermal resistance and package dissipation ratings					
$R_{\Theta JB}$	Junction-to-board (bottom exposed pad soldered to board) 48 LQFP EP	[4]	—	11	°C/W
$R_{\Theta JA}$	Junction-to-ambient, natural convection, single-layer board (1s) 48 LQFP EP	[5] [6]	—	72	°C/W
$R_{\Theta JA}$	Junction-to-ambient, natural convection, four-layer board (2s2p) 48 LQFP EP	[5] [6]	—	30	°C/W
$R_{\Theta JCTOP}$	Junction-to-case top (exposed pad) 48 LQFP EP	[7]	—	24	°C/W
$R_{\Theta JCBOTTOM}$	Junction-to-case bottom (exposed pad) 48 LQFP EP	[8]	—	0.98	°C/W
ΨJT	Junction to package top, natural convection	[9]	—	4	°C/W

[1] The user must ensure that the average maximum operating junction temperature (Tj) is not exceeded.
[2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
[3] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.
[4] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[5] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[6] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
[7] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1), with the cold plate temperature used for the case temperature.
[8] Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
[9] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

8.4 Electrical characteristics

Table 9. Static and dynamic electrical characteristics

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
Power management					
$V_{PWR(FO)}$	Supply voltage Full parameter specification (SPI application) Full parameter specification (TPL application)	 6.0 7.0	 — —	 30 30	V
I_{VPWR}	Supply current (base value) Normal mode, cell balance OFF, ADC inactive, SPI communication inactive, IVCOM = 0 mA Normal mode, cell balance OFF, ADC inactive, TPL communication inactive, IVCOM = 0 mA	 — —	 6.0 8.0	 7.0 — 10 —	mA
$I_{VPWR(TPL\_TX1)}$	Supply current adder when TPL communication active with only one device in daisy chain	—	—	8.3	mA
$I_{VPWR(TPL\_TX1/TX2)}$	Supply current adder when TPL communication active with multiple devices in daisy chain [1]	—	—	10	mA
$I_{VPWR(CBON)}$	Supply current adder to set all 6 cell balance switches ON	—	2.0	—	mA
$I_{VPWR(ADC)}$	Delta supply current to perform ADC conversions (addend) [2] ADC1-A,B continuously converting ADC2 continuously converting	 — —	 4.7 1.0	 7.0 — 2.0 —	mA
$I_{VPWR(SS)}$	Supply current in sleep and idle modes, communication inactive, cell balance off, oscillator monitor on, cyclic measurement off [3]				
	SPI mode (T_A = 25 °C)	—	32	—	µA
	SPI mode (−40 °C ≤ T_A ≤ 85 °C)	—	—	60	
	SPI mode (T_A = 125 °C)	—	42	80 —	
	TPL mode (T_A = 25 °C)	—	75	—	
	TPL mode (−40 °C ≤ T_A ≤ 85 °C)	—	—	100	
	TPL mode (T_A = 125 °C)	—	—	138	
$I_{VPWR(CKMON)}$	Clock monitor current consumption	—	5	8 —	µA
V_{VPWR_CT}	Voltage drop across CT6 and VPWR without accuracy degradation	−0.5	—	0.5	V
$V_{PWR(OV\_FLAG)}$	V_{PWR} overvoltage fault threshold (flag)	31 —	— 33.5	36 —	V
$V_{PWR(LV\_FLAG)}$	V_{PWR} low-voltage warning threshold (flag)	7.5 —	— 7.8	8.1 —	V

Table 9. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
$V_{PWR(UV\_POR)}$	V_{PWR} undervoltage shutdown threshold (POR), falling VPWR SPI mode TPL mode	4.8 — 6.1 —	— 4.9 — 6.25	5.0 — 6.4 —	V
$V_{PWR(UV\_RIS)}$	V_{PWR} undervoltage shutdown threshold (POR), rising VPWR SPI mode TPL mode	5.6 — 6.6 —	— 5.8 — 6.8	6.0 — 7.0 —	V
$t_{VPWR(FILTER)}$	V_{PWR} OV, LV filter	—	50	—	µs
VPRE power supply					
VPRE	Pre-regulator voltage range - decouple with 470 nF SPI mode, ILoad = 15 mA SPI mode, ILoad = 15 mA, 5.0 V ≤ VPWR < 6.0 V TPL mode, ILoad = 70 mA	5.6 — 4.9 4.9 6.3 —	— 5.75 — — — 6.5	5.9 — — — 6.7 —	V
$V_{PRE(UV\_TH)}$	PRE undervoltage threshold leading to a reset	4.0 —	4.25	4.5 —	V
VCP power supply					
VCP	Charge pump voltage range	2 × V_{PRE} – 2 2 × V_{PRE} – 2	— —	2 × V_{PRE} 2 × V_{PRE}	V
$V_{CP(UV\_TH)}$	Undervoltage threshold for VCP minus VPRE	0.9 —	1.5	2.2 —	V
VDDIO power supply					
V_{DDIO}	IO supply for I²C and SPI interfaces - voltage range	3.1 —	— 4.15	5.2 —	V
VCOM power supply					
V_{COM}	VCOM output voltage	4.9 —	5.0	5.2 —	V
I_{VCOM}	VCOM output current allocated for external use	—	— —	5.0 5.0	mA
$V_{COM(UV)}$	VCOM undervoltage fault threshold	4.2 —	4.4	4.6 —	V
V_{COM_HYS}	VCOM undervoltage hysteresis	—	100	—	mV
$t_{VCOM(FLT\_TIMER)}$	VCOM undervoltage fault timer	—	10	—	µs
$t_{VCOM(RETRY)}$	VCOM fault retry timer	—	10	—	ms
$V_{COM(OV)}$	VCOM overvoltage fault threshold	5.4 5.4	— —	5.9 5.9	V

Table 9. Static and dynamic electrical characteristics...*continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
$I_{LIM(OC)}$	VCOM current limit in TPL mode VCOM current limit SPI mode	65 65 35 35	— — — —	140 140 140 140	mA
$R_{VCOM(SS)}$	VCOM sleep mode pulldown resistor	1.0 —	2.0	5.0 —	kΩ
t_{VCOM}	VCOM rise time (CL = 2.2 µF ceramic X7R only) [4]	—	— —	400 400	µs
VANA power supply					
V_{ANA}	VANA output voltage (not used by external circuits) Decouple with 47 nF X7R 0603 or 0402	 2.6 —	 2.65	 2.7 —	V
$V_{ANA(UV)}$	VANA undervoltage fault threshold	2.28 —	2.4	2.5 —	V
V_{ANA_HYS}	VANA undervoltage hysteresis	—	50	—	mV
$V_{ANA(FLT\_TIMER)}$	VANA undervoltage fault timer	—	11	—	µs
$V_{ANA(OV)}$	VANA overvoltage fault threshold	2.77 —	2.8	2.85 —	V
$t_{VANA(RETRY)}$	VANA fault retry timer	—	10	—	ms
$I_{LIM(OC)}$	VANA current limit	5.0 5	— —	10 10	mA
R_{VANA_RPD}	VANA sleep mode pull-down resistor	—	1.0	—	kΩ
t_{VANA}	VANA rise time (CL = 47 nF ceramic X7R only) [4]	—	— —	100 100	µs
ADC1-A, ADC1-B					
$CTn_{(LEAKAGE)}$	Cell terminal input leakage current	—	10	100 —	nA
CT_N	Cell terminal input current during conversion	—	50	—	nA
R_{PD}	Cell terminal open load detection pulldown resistor	850 —	950	1250 —	Ω
V_{VPWR_RES}	VPWR terminal measurement resolution	—	2.44148	—	mV/LSB
V_{VPWR_RNG}	VPWR terminal measurement range SPI application TPL application	 6.0 7.0	 — —	 36 36	V
$VPWR_{TERM\_ERR}$	VPWR terminal measurement accuracy [5]	−0.5	—	0.5	%
V_{CT_RNG}	ADC differential input voltage range for CTn to CTn-1 [6]	0.0	—	4.85	V
$V_{CT\_ANx\_RES}$	Cell voltage and ANx resolution in 15-bit MEAS_xxxx registers	—	152.58789	—	µV/LSB
$V_{ANx\_RATIO\_RES}$	ANx resolution in 15-bit MEAS_xxxx registers in ratiometric mode	—	VCOM × 30.51758	—	
V_{ERR}	Cell voltage measurement error [7] [8] 0.1 V ≤ V_{CELL} ≤ 4.85 V, –40 °C ≤ T_A ≤ 105 °C (or –40 °C ≤ T_J ≤ 125 °C)	 -5.5 —	 ±0.7	 5.5 —	mV

Table 9. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
V_{ERR_1}	Cell voltage measurement error [7] [8] 0 V ≤ V_{CELL} ≤ 1.5 V, –40 °C ≤ T_A ≤ 60 °C (or –40 °C ≤ T_J ≤ 85 °C)	−1.5 —	±0.4	1.5 —	mV
V_{ERR_2}	Cell voltage measurement error [7] [8] 1.5 V ≤ V_{CELL} ≤ 2.7 V, –40 °C ≤ T_A ≤ 60 °C (or –40 °C ≤ T_J ≤ 85 °C)	−2.0 —	±0.4	2.0 —	mV
V_{ERR_3}	Cell voltage measurement error [7] [8] 2.7 V ≤ V_{CELL} ≤ 3.7 V, –40 °C ≤ T_A ≤ 60 °C (or –40 °C ≤ T_J ≤ 85 °C)	−2.0 —	±0.5	2.0 —	mV
V_{ERR_4}	Cell voltage measurement error [7] [8] 3.7 V ≤ V_{CELL} ≤ 4.3 V, –40 °C ≤ T_A ≤ 60 °C (or –40 °C ≤ T_J ≤ 85 °C)	−2.8 —	±0.7	2.8 —	mV
V_{ERR_5}	Cell voltage measurement error [7] [8] 1.5 V ≤ V_{CELL} ≤ 4.5 V, –40 °C ≤ T_A ≤ 105 °C (or –40 °C ≤ T_J ≤ 125 °C)	–4.5 —	±0.7	4.5 —	mV
V_{ERR_A}	Cell voltage measurement error [7] [9] After aging, 0.1 V ≤ V_{CELL} ≤ 4.85 V, –40 °C ≤ T_A ≤ 105 °C (or –40 °C ≤ T_J ≤ 125 °C)	–8.0	±0.8	8.0	mV
V_{ERR_1A}	Cell voltage measurement error [7] [9] After aging, 0 V ≤ V_{CELL} ≤ 1.5 V, –40 °C ≤ T_A ≤ 60 °C (or –40 °C ≤ T_J ≤ 85 °C)	–2.0	±0.5	2.0	mV
V_{ERR_2A}	Cell voltage measurement error [7] [9] After aging, 1.5 V ≤ V_{CELL} ≤ 2.7 V, –40 °C ≤ T_A ≤ 60 °C (or –40 °C ≤ T_J ≤ 85 °C)	–2.5	±0.5	2.5	mV
V_{ERR_3A}	Cell voltage measurement error [7] [9] after aging, 2.7 V ≤ V_{CELL} ≤ 3.7 V, −40 °C ≤ T_A ≤ 60 °C (or −40 °C ≤ T_J ≤ 85 °C)	−3.2	±0.4	3.2	mV
V_{ERR_4A}	Cell voltage measurement error [7] [9] after aging, 3.7 V ≤ V_{CELL} ≤ 4.3 V, −40 °C ≤ T_A ≤ 60 °C (or −40 °C ≤ T_J ≤ 85 °C)	−3.9	±0.7	3.9	mV
V_{ERR_5A}	Cell voltage measurement error [7] [9] after aging, 1.5 V ≤ V_{CELL} ≤ 4.5 V, –40 °C ≤ T_A ≤ 105 °C (or –40 °C ≤ T_J ≤ 125 °C)	–6.0	±0.7	6.0	mV
V_{ANx_ERR}	Magnitude of ANx error in the entire measurement range: [7] [9] Ratiometric measurement Absolute measurement, input in the range [1.0, 4.5] V Absolute measurement, input in the range [0, 4.85] V for −40 °C < T_A < 60 °C Absolute measurement after soldering and aging, input in the range [0, 4 85] V for −40 °C < T_A < 105 °C	−16 −10 −8.0 −11	— — — —	16 10 8.0 11	mV
t_{VCONV}	Single channel net conversion time 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	— — — —	6.77 9.43 14.75 25.36	— — — —	μs

Table 9. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
V_{V_NOISE}	Conversion noise 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	 — — — —	 1800 1000 600 400	 — — — —	μVrms
ADC2/current sense module					
V_{INC}	ISENSE+/ISENSE− input voltage (reference to AGND)	−300	—	300	mV
V_{IND}	ISENSE+/ISENSE− differential input voltage range	−150	—	150	mV
$V_{ISENSEX(OFFSET)}$	ISENSE+/ISENSE− input voltage offset error [10]	—	—	0.5	μV
$I_{SENSEX(BIAS)}$	ISENSE+/ISENSE− input bias current	−100	—	100	nA
$I_{SENSE(DIF)}$	ISENSE+/ISENSE− differential input bias current	−5.0	—	5.0	nA
$I_{GAINERR}$	ISENSE error including nonlinearities [11]	−0.5	—	0.5	%
I_{ISENSE_OL}	ISENSE open load injected current [12]	109 —	130	151 —	μA
V_{ISENSE_OL}	ISENSE open load detection threshold	340 —	460	600 —	mV
V_{2RES}	Current sense user register resolution	—	0.6	—	μV/LSB
V_{PGA_SAT}	PGA saturation half-range Gain = 256 Gain = 64 Gain = 16 Gain = 4	 — — — —	 4.9 19.5 78.1 150	 — — — —	mV
V_{PGA_ITH}	Voltage threshold for PGA gain increase Gain = 256 Gain = 64 Gain = 16 Gain = 4	 — — — —	 — 2.344 9.375 37.50	 — — — —	mV
V_{PGA_DTH}	Voltage threshold for PGA gain decrease Gain = 256 Gain = 64 Gain = 16 Gain = 4	 — — — —	 4.298 17.188 68.750 —	 — — — —	mV
t_{AZC_SETTLE}	Time to perform auto-zero procedure after enabling the current channel	—	200	—	μs
t_{ICONV}	ADC conversion time including PGA settling time 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	 — — — —	 19.00 21.67 27.00 37.67	 — — — —	μs
V_{I_NOISE}	Noise at 16-bit conversion [10]	—	3.01	—	μVrms
V_{I_NOISE}	Noise error at 13-bit conversion	—	8.33	—	μVrms
ADC_{CLK}	ADC2 and ADC1-A,B clocking frequency	5.7 —	6.0	6.3 —	MHz

Table 9. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
Diagnostic thresholds					
V_{OL_DETECT}	Cell terminal open load V detection threshold 1.5 V ≤ VCELL ≤ 2.7 V 2.5 V ≤ VCELL ≤ 3.7 V 2.5 V ≤ VCELL ≤ 4.3 V	 — — —	 50 100 150	 — — —	mV
V_{LEAK}	Cell terminal leakage detection level [12]	–15	—	15	mV
V_{REF_DIAG}	ISENSE diagnostic reference with PGA having gain 4	123.5	—	129.5	mV
V_{OFF_DIAG}	ISENSE diagnostic common mode offset voltage [13]	—	—	37.2	μV
V_{REF_ZD}	Precision diagnostic zener reference for cell voltage channel functional verification [7]	4.45	—	4.85	V
V_{CVFV}	Cell voltage channel functional verification allowable error in CT verification measurement [12]	–22	—	6	mV
V_{BGP}	Band gap reference used in ADC1-A,B functional verification	—	1.18	—	V
$ADC1a_{FV}$, $ADC1b_{FV}$	ADC1-A and ADC1-B functional verification (maximum tolerance between ADC1-A, B and diagnostic reference 1.5 V ≤ VCELL ≤ 4.3 V)	–5	—	5	mV
CTx_UV_TH	Undervoltage functional verification threshold in diagnostic mode 1.5 V ≤ VCELL ≤ 2.7 V 2.5 V ≤ VCELL ≤ 3.7 V 2.5 V ≤ VCELL ≤ 4.3 V	 390 650 1200	 — — —	 — — —	mV
CTx_OV_TH	Overvoltage functional verification threshold in diagnostic mode 1.5 V ≤ VCELL ≤ 2.7 V 2.5 V ≤ VCELL ≤ 3.7 V 2.5 V ≤ VCELL ≤ 4.3 V	 — — —	 — — —	 1800 3500 4000	mV
Cell balance drivers					
$V_{DS(CLAMP)}$	Cell balance driver VDS active clamp voltage	10 —	11	12 —	V
$V_{OUT(FLT\_TH)}$	Output fault detection voltage threshold Balance off (open load) Balance on (shorted load)	 0.3 —	 0.55	 0.75 —	V
R_{PD_CB}	Output OFF open load detection pull-down resistor Balance off, open load detect disabled	 1.7 —	 2.0	 2.9 —	kΩ
$I_{OUT(LKG)}$	Output leakage current Balance off, open load detect disabled at V_{DS} = 4.0 V	 —	 —	 1.0	μA
$R_{DS(on)}$	Drain-to-source on resistance I_{OUT} = 300 mA, T_J = 125 °C I_{OUT} = 300 mA, T_J = 25 °C I_{OUT} = 300 mA, T_J = −40 °C	 — — —	 — 0.5 0.4	 0.80 — —	Ω
I_{LIM_CB}	Driver current limitation (shorted resistor)	310	—	950	mA

Table 9. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
t_{ON}	Cell balance driver turn on [14] R_L = 15 Ω	—	350	450 —	μs
t_{OFF}	Cell balance driver turn off [14] R_L = 15 Ω	—	200	—	μs
$t_{BAL\_DEGLICTH}$	Short/open detect filter time	19 —	20	42.1 —	μs
Internal temperature measurement					
IC_TEMP1_ERR	IC temperature measurement error	−3.0	—	3.0	K
IC_TEMP1_RES	IC temperature resolution	—	0.032	—	K/LSB
TSD_TH	Thermal shutdown	155 —	170	185 —	°C
TSD_HYS	Thermal shutdown hysteresis	5.0 —	10	12.2 —	°C
Default operational parameters					
$V_{CTOV(TH)}$	Cell overvoltage threshold (8 bits)	0.0	4.2	5.0	V
$V_{CTOV(RES)}$	Cell overvoltage threshold resolution	—	19.53125	—	mV/LSB
$V_{CTUV(TH)}$	Cell undervoltage threshold (8 bits)	0.0	2.5	5.0	V
$V_{CTUV(RES)}$	Cell undervoltage threshold resolution	—	19.53125	—	mV/LSB
$V_{GPIO\_OT(TH)}$	GPIOx configured as ANx input overtemperature threshold from POR	—	1.16	—	V
$V_{GPIO\_OT(RES)}$	Overtemperature voltage threshold resolution	—	4.8828125	—	mV/LSB
$V_{GPIO\_UT(TH)}$	GPIOx configured as ANx input undertemperature threshold from POR	—	3.82	—	V
$V_{GPIO\_UT(RES)}$	Undertemperature voltage threshold resolution	—	4.8828125	—	mV/LSB
General purpose input/output GPIOx					
V_{IH}	Input high-voltage (3.3 V compatible) [15]	2.0	—	—	V
V_{IL}	Input low-voltage (3.3 V compatible) [15]	—	—	1.0	V
V_{HYS}	Input hysteresis [15]	—	100	—	mV
I_{IL}	Input leakage current Pins 3-state, V_{IN} = V_{COM} or AGND	−100	—	100	nA
I_{IDL}	Differential input leakage current GPIO 5,6 GPIO 5,6 configured as digital inputs for current measurement	−30	—	30	nA
V_{OH}	Output high-voltage I_{OH} = −0.5 mA	V_{COM} − 0.8	—	—	V
V_{OL}	Output low-voltage I_{OL} = +0.5 mA	—	—	0.8	V
V_{ADC}	Analog ADC input voltage range for ratiometric measurements	AGND	—	V_{COM}	V
$V_{OL(TH)}$	Analog input open pin detect threshold [16]	0.1 —	0.15	0.23 —	V
R_{OPENPD}	Internal open detection pull-down resistor [17]	3.8 —	5.0	6.2 —	kΩ

Table 9. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
t_{GPIO0_WU}	GPIO0 WU de-glitch filter	47 —	50	85 —	µs
t_{GPIO0_FLT}	GPIO0 daisy chain de-glitch filter both edges	19 —	20	48 —	µs
t_{GPIO2_SOC}	GPIO2 convert trigger de-glitch filter	1.9 —	2.0	2.1 —	µs
t_{GPIOx_DIN}	GPIOx configured as digital input de-glitch filter	2.5	—	5.6	µs
Reset input					
V_{IH_RST}	Input high-voltage (3.3 V compatible)	2.0	—	—	V
V_{IL_RST}	Input low-voltage (3.3 V compatible)	—	—	1.0	V
V_{HYS}	Input hysteresis	—	0.6	—	V
$t_{RESETFLT}$	RESET de-glitch filter	—	100	—	µs
R_{RESET_PD}	Input logic pull down (RESET)	—	100	—	kΩ
SPI_COM_EN input					
V_{IH}	Input high-voltage (3.3 V compatible)	2.0	—	—	V
V_{IL}	Input low-voltage (3.3 V compatible)	—	—	1.0	V
V_{HYS}	Input hysteresis	—	450	—	mV
Digital interface					
V_{FAULT_HA}	FAULT output (high active, I_{OH} = 1.0 mA) FAULT output (high active, I_{OH} = 1.0 mA), SPI mode, 5.0 ≤ VPWR < 6.0 V	3.9 — 2.9	4.9 —	6.0 — 6.0	V
I_{FAULT_CL}	FAULT output current limit	3.0	—	25	mA
R_{FAULT_PD}	FAULT output pulldown resistance	—	100	—	kΩ
V_{IH_COMM}	Voltage threshold to detect the input as high SI/RDTX_IN+, SCLK/RDTX_IN–, CSB, SDA, SCL (NOTE: needs to be 3.3 V compatible)	—	—	2.0	V
V_{IL_COMM}	Voltage threshold to detect the input as low SI/RDTX_IN+, SCLK/RDTX_IN–, CSB, SDA, SCL	0.8	—	—	V
V_{HYS}	Input hysteresis SI/RDTX_IN+, SCLK/RDTX_IN−, CSB, SDA, SCL	—	100	—	mV
I_{LOGIC_SS}	Sleep state input logic current CSB	−100	—	100	nA
R_{SCLK_PD}	Input logic pulldown resistance (SCLK/RDTX_IN–, SI/RDTX+)	—	20	—	kΩ
R_{I_PU}	Input logic pullup resistance to V_{COM} (CSB, SDA, SCL)	—	100	—	kΩ
I_{SO_TRI}	3-state SO input current 0 V to V_{COM}	−2.0	—	2.0	µA
V_{SO_HIGH}	SO high-state output voltage with $I_{SO(HIGH)}$ = −2.0 mA	V_{DDIO} − 0.4	—	—	V
V_{SO_LOW}	SO, SDA, SLK low-state output voltage with $I_{SO(HIGH)}$ = −2.0 mA	—	—	0.4	V
CSB_{WU_FLT}	CSB wake-up de-glitch filter, low to high transition	—	50	65 —	µs

Table 9. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
System timing					
t_{CELL_CONV}	Time needed to acquire all 6 cell voltages and the current after an on demand conversion [18] 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	 38 — 53 — 84 — 144 —	 41 57 89 152	 43 — 60 — 93 — 160 —	μs
t_{SYNC}	V/I synchronization time [18] ADC1-A,B at 13 bit, ADC2 at 13 bit ADC1-A,B at 14 bit, ADC2 at 13 bit ADC1-A,B at 15 bit, ADC2 at 13 bit ADC1-A,B at 16 bit, ADC2 at 13 bit	 — — — —	 41.39 42.71 47.37 95.14	 — — — —	μs
t_{SYNC}	V/I synchronization time [18] ADC1-A,B at 13 bit, ADC2 at 14 bit ADC1-A,B at 14 bit, ADC2 at 14 bit ADC1-A,B at 15 bit, ADC2 at 14 bit ADC1-A,B at 16 bit, ADC2 at 14 bit	 — — — —	 46.73 48.05 50.71 92.47	 — — — —	μs
t_{SYNC}	V/I synchronization time [18] ADC1-A,B at 13 bit, ADC2 at 15 bit ADC1-A,B at 14 bit, ADC2 at 15 bit ADC1-A,B at 15 bit, ADC2 at 15 bit ADC1-A,B at 16 bit, ADC2 at 15 bit	 — — — —	 57.39 58.71 61.37 87.14	 — — — —	μs
t_{SYNC}	V/I synchronization time [18] ADC1-A,B at 13 bit, ADC2 at 16 bit ADC1-A,B at 14 bit, ADC2 at 16 bit ADC1-A,B at 15 bit, ADC2 at 16 bit ADC1-A,B at 16 bit, ADC2 at 16 bit	 — — — —	 78.73 80.05 82.71 88.02	 — — — —	μs
$t_{VPWR(READY)}$	Time after VPWR connection for the IC to be ready for initialization	—	—	5.0	ms
$t_{WAKE-UP}$	Power up duration	—	—	440	μs
t_{WAKE_DELAY}	Time between wake pulses	500 —	600	700 —	μs
t_{NOWUP}	Time, starting from the first SOM received, to go back to Sleep/Idle mode time after receiving incomplete TPL bus wake-up sequence	— —	—	1.3 1.3	ms
t_{IDLE}	Idle timeout after POR	54 —	60	66 —	s
$t_{BALANCE}$	Cell balance timer range	0.5	—	511	min
t_{CYCLE}	Cyclic acquisition timer range	0.0	—	8.5	s
t_{FAULT}	Fault detection to activation of fault pin Normal mode	 —	 —	 56	μs
t_{DIAG}	Diagnostic mode timeout	0.047	1.0	8.5	s

Table 9. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
t_{EOC}	SOC to data ready (includes post processing of data) [18] 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	 140 — 190 — 291 — 494 —	 148 201 307 520	 156 — 211 — 323 — 546 —	µs
t_{SETTLE}	Time after SOC to begin converting with ADC1-A,B [18]	11.67 —	12.28	12.90 —	µs
t_{CLST_TPL}	Time needed to send an SOC command and read back 6 cell voltages, 7 temperatures, 1 current, and 1 coulomb counter with TPL communication working at 2.0 Mbit/s and ADC1-A,B configured as follows (with ADC_CFG[AVG] = 0): 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	— — — —	0.79 0.85 0.95 1.16	— — — —	ms
t_{CLST_SPI}	Time needed to send an SOC command and read back 6 cell voltages, 7 temperatures, 1 current, and 1 coulomb counter with SPI communication working at 4.0 Mbit/s and ADC1-A,B configured as follows (with ADC_CFG[AVG] = 0): 13-bit resolution 14-bit resolution 15-bit resolution 16-bit resolution	— — — —	0.48 0.54 0.64 0.86	— — — —	ms
$t_{I2C\_DOWNLOAD}$	Time to download EEPROM calibration after POR	—	—	1.0	ms
t_{I2C_ACCESS}	EEPROM access time, EEPROM write (depends on device selection)	—	5.0	—	ms
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx}$ = 00	450 —	500	550 —	µs
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx}$ = 01	0.90 —	1.0	1.10 —	ms
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx}$ = 10	9 —	10	11 —	ms
$t_{WAVE\_DC\_BITx}$	Daisy chain duty cycle off time $t_{WAVE\_DC\_BITx}$ = 11	90 —	100	110 —	ms
$t_{WAVE\_DC\_ON}$	Daisy chain duty cycle on time	450 —	500	550 —	µs
t_{COM_LOSS}	Time out to reset the IC in the absence of communication	—	1024	—	ms

Table 9. Static and dynamic electrical characteristics*...continued*

Characteristics noted under conditions: 6.0 V ≤ V_{PWR} ≤ 30 V (SPI mode) or 7.0 V ≤ V_{PWR} ≤ 30 V (TPL mode), −40 °C ≤ T_A ≤ 125 °C (SPI mode) or –40 °C ≤ T_A ≤ 105 °C (TPL mode), GND = 0 V, unless otherwise stated. Typical values refer to V_{PWR} = 24 V, T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
SPI interface					
t_{TD}	Sequential data transfer delay in SPI mode (N) [19]	1.0	—	—	µs
F_{SCK}	SCLK frequency	—	—	4.0	MHz
t_{SCK_H}	SCLK high time (A) [19]	125	—	—	ns
t_{SCK_L}	SCLK high time (B) [19]	125	—	—	ns
t_{SCK}	SCLK period (A+B) [19]	250	—	—	ns
t_{FALL}	SCLK falling time	—	—	15	ns
t_{RISE}	SCLK rising time	—	—	15	ns
t_{SET}	SCLK setup time (O) [19]	20	—	—	ns
t_{HOLD}	SCLK hold time (P) [19]	20	—	—	ns
t_{SI_SETUP}	SI setup time (F) [19]	40	—	—	ns
t_{SI_HOLD}	SI hold time (G) [19]	40	—	—	ns
t_{SO_VALID}	SO data valid, rising edge of SCLK to SO data valid (I) [19]	—	—	40	ns
t_{SO_EN}	SO enable time (H) [19]	—	—	40	ns
$t_{SO\_DISABLE}$	SO disable time (K) [19]	—	—	40	ns
t_{CSB_LEAD}	CSB lead time (L) [19]	100	—	—	ns
t_{CSB_LAG}	CSB lag time (M) [19]	100	—	—	ns
TPL interface (MCU)					
t_{MCU_RES}	Time between two consecutive message request transmitted by MCU [20]	4.0	—	—	µs
t_{WU_Wait}	Time the MCU shall wait after sending first wake-up message per MC33772C IC [21]	0.75	—	—	ms
TPL interface (MC33772C)					
t_{TPL_TD}	Sequential data transfer delay in TPL mode [22][23]	3.8 —	4.0	4.25 —	µs
t_{TPL}	Transmit pulse duration	—	208	—	ns
t_{port_delay}	Port delay introduced by each repeater in MC33772C [24]	—	—	0.95	µs
t_{RES}	Slave response after read command [23][25]	4.0 —	5.0	9 —	µs
$V_{RDTX\ INTH}$	Differential receiver threshold	480 —	580	680 —	mV
t_{EOM}	Message timeout duration [26]	238 —	250	—	µs

[1] The current consumption due to communication is valid with minimum 8 nodes in the daisy chain.

[2] Use of ADC1-A,B can be performed with a duty cycle of t_{EOC}/period (µs). For example, SYS_CFG1[CYCLIC_TIMER] = 010, corresponding to 100000 µs period, and ADC_CFG[ADC1_A_DEF] = ADC_CFG[ADC1_B_DEF] = 11, corresponding to 16 bits and therefore t_{EOC} = 520 µs, given a duty cycle of 0.0052 (or ROM). When an ADC is configured in continuous mode, the duty cycle is equal to 1, resulting in high-current consumption.

[3] To calculate the current consumption in sleep mode, the following formula has to be used: $I_{SLEEP\_MODE} = (1 - \tau_{NORMAL}) \cdot I_{VPWR(SS)} + \tau_{NORMAL} \cdot [I_{VPWR} + I_{VPWR(ADC)}] + I_{VPWR(CBON)}$ (not zero only if SYS_CFG1[CB_DRVEN] = 1), where $\tau_{NORMAL} = (t_{VCOM} + t_{EOC})$/period (µs), where t_{EOC} depends on the selected number of bits for the ADCs (see ADC_CFG[ADC1_A_DEF, ADC1_B_DEF, ADC2_DEF] fields) and period (µs) depends on SYS_CFG1[CYCLIC_TIMER], as explained in note [1]. Evidently $I_{SLEEP\_MODE} = I_{VPWR(SS)}$ only if no conversion is requested in sleep mode (for example, SYS_CFG1[CYCLIC_TIMER] = 000) and if the cell balancing is OFF.

[4] 5 % to 95 % rise time

[5] Parameter $VPWR_{TERM\_ERR}$ is guaranteed if GPIO[0..1] are set in analog inputs (GPIO_CFG1[GPIO0_CFG] = 0b0x and GPIO_CFG1[GPIO1_CFG] = 0b0x). The $VPWR_{TERM\_ERR}$ is degraded to typical ±0.8 % if GPIO0 or GPIO1 is set to digital IO mode (GPIO_CFG1[GPIO0_CFG] = 0b1x or GPIO_CFG1[GPIO1_CFG] = 0b1x).

[6] ADC1-A/B may clamp when the voltage of the Cellx or ANx is over 4.85 V.

[7] The cell voltage error includes all internal errors, for example; ADC offset, gain error, INL and DNL are included. Current measurement is not active when measuring the cell voltage. Single shot measurements are affected by noise, which has zero mean and standard deviation given by V_{V_NOISE} and is not included in the cell voltage error. In order to reduce it, SW implemented IIR or FIR low-pass filters may be used; example, a moving average, whose length is N samples, has output standard deviation $V_{OUTPUT\_NOISE} = V_{V\_NOISE}$ /sqrt(N). Performance can be granted only if ADC1-A,B are configured at 16-bits resolution (ADC_CFG[ADC1_A_DEF] =ADC_CFG[ADC1_B_DEF] = 11) and if -100 mV ≤ CTREF - GND ≤ 100 mV.

[8] Inaccuracies from soldering or aging are not included.

[9] Inaccuracies from soldering (MSL3 preconditioning) and aging (after 3000 h HTOL at T_A = 125 °C) are included.

[10] Offset error is considered at PGA inputs, with PGA gain being set to 256. Both PGA inputs are grounded (shorted together with SYS_DIAG[I_MUX]=11). The offset value, guaranteed by design, does not include the noise, which is considered to be averaged. The noise is characterized by V_{I_NOISE} and is also with PGA gain set to 256 and PGA inputs shorted together (with SYS_DIAG[I_MUX]=11).

[11] Performance can be granted only if the ADC2 is configured at the best resolution, namely, ADC_CFG[ADC2_DEF] = 11.

[12] Setting the SYS_DIAG[ISENSE_OL_DIAG] bit to logic 1 causes the injection of the current I_{ISENSE_OL} in both ISENSE ± pins, so if the shunt is disconnected, in one or both of the input pins there is an increased voltage due to charging of external capacitors. Comparison to the threshold V_{ISENSE_OL} detects the open fault.

[13] Diagnostic threshold when the PGA inputs are shorted together, the PGA gain is set at 256 and the ADC2 is configured at 16 bit.

[14] Cell balance drivers performance can be granted if the cell voltage is greater than 1.1 V.

[15] For GPIO0 configured as wake-up, transition time must be shorter than 100 µs.

[16] Out of range band should be considered for the GPIOs external components design to avoid false open pin detection.

[17] During internal open detection, an internal pull up current of 10 µA typical is generated in the pin.

[18] See the ADC conversion sequence in Figure 10

[19] See the timing diagram in Figure 5

[20] It is the time which MCU shall wait for sending new message request to MC33772C.

[21] The waiting time for MCU after transmitting the first wake-up message is dependent on the number of MC33772C in daisy chain. If the number of nodes in daisy chain is N, then the total waiting time for MCU after sending first wake-up message is $N{*}t_{WU\_Wait}$

[22] t_{TPL_TD} is the time between two consecutive response messages at the node which is initiating transmission. This time could vary when measured at other forwarding nodes in daisy chain.

[23] See the waveforms diagram in Figure 28

[24] The expected waiting time for MCU, to get the response from MC33772C is dependant on number of MC33772C used in daisy chain. The repeater of each node imposes a delay of t_{port_delay} for both request and response. Example: if 24, MC33772C ICs are used in a daisy chain, the last node (24th MC33772C) receives the request in (24*0.95)µs = 22.8 µs.

[25] t_{RES} is the time between request received and response transmitted by the slave device, which is addressed in the read command. This time could vary when measured at other forwarding nodes in daisy chain.

[26] The EOM timeout counter starts/restarts after reception of SOM. This means that the maximum length of allowed message frame is t_{EOM}. If a valid EOM is not received in this time frame, the message frame is discarded and the device is ready for new reception.

8.5 Timing diagrams

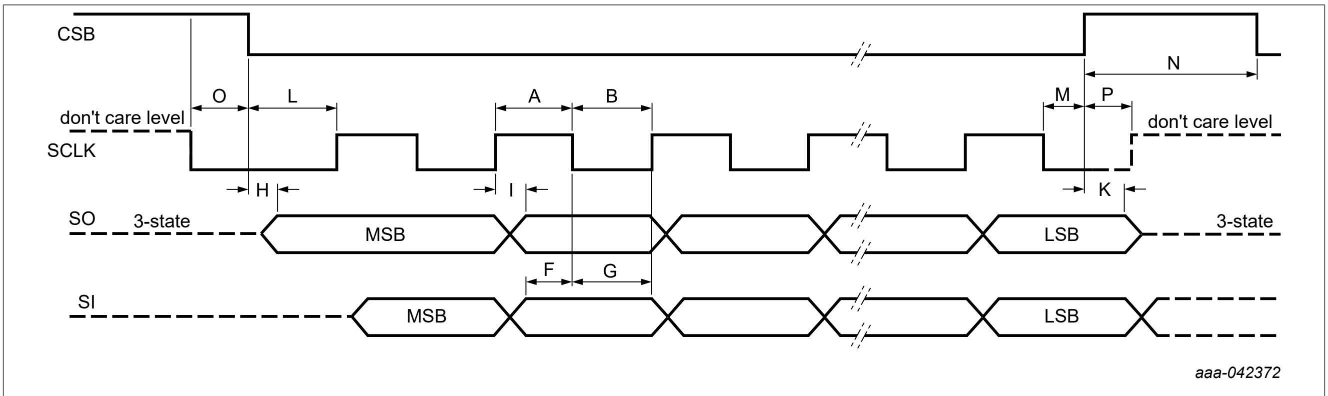


Figure 5. Low-voltage SPI interface timing

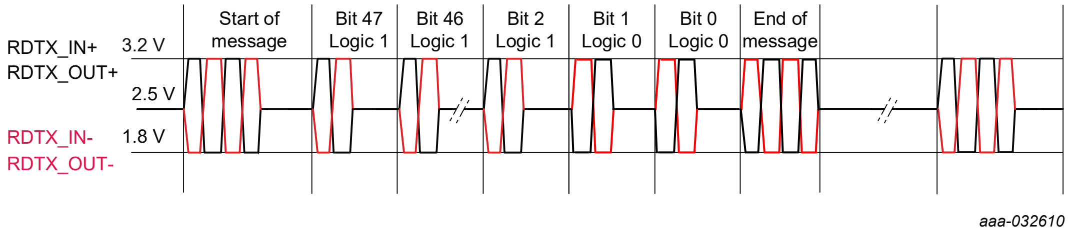


Figure 6. Transformer communication signaling

9 Functional description

9.1 Introduction

The MC33772C contains all circuit blocks necessary to perform synchronized battery voltage measurements, battery voltage/current measurement, coulomb counting, cell temperature measurement and integrated cell balancing. These features along with high speed communication make the MC33772C ideal for automotive Lithium-ion battery monitoring. In addition to the battery management functions, the MC33772C is designed to monitor many internal and external functions to validate the integrity of the measurements and the measurement system. The following section describes in detail the features, functions and modes of operation of the device. Table 10 summarizes the IC measurement capability depending on the operating mode. Following terms, phrasings and conventions are used in this document:

- User: this word denotes the battery pack controller, including at least one MCU, where the intelligence of the system is located. The pack controller uses one or more MC33772C to sense the physical quantities of a battery.
- User parameter (or simply parameter): it is a datum memorized in the IC registers that is readable or writable by the user and is denoted by an identifier within square brackets preceded by a prefix, for example, REGISTER_NAME[FIELD_NAME], where REGISTER_NAME is the symbol for the intended register and FIELD_NAME is the symbol for the parameter itself, which is, in general, a portion of the 16-bit register data.
- Channel: it is a signal, which can be measured. There are external channels, for example, cell voltages and temperatures, and internal channels, for example, die temperature, and voltage diagnostic references.
- Conversion: this word denotes an analog to digital conversion performed by an ADC and is often meant as measurement of a given channel.
- Sequence: this term denotes a scan of channels that enter some multiplexers to be routed to the ADCs according to a certain sequence. During the scan, each ADC performs subsequent data conversions, where each conversion affects a predetermined channel. Sequences are necessary because the number of channels is much greater than the number of ADCs.
- Cyclic measurement: this means the bank of ADCs perform sequences autonomously, for example, with no intervention requested to the user. The user has to do a single programming of an internal timer by providing it with the period value. Then the timer provides the periodic trigger starting each measurement sequence. For example, the period may be 100 ms, while the sequence duration is order of magnitudes shorter. The main purpose of performing cyclic measurements is to carry out automatic comparisons of some measured channels against predefined tunable thresholds, so some fault bits can be set accordingly. Fault bits are readable by the user by accessing the proper fault registers through the ordinary communication channel; or the fault bits may be used to assert the FAULT pin, for the safety information be propagated to the user through the fault line of daisy chained devices.
- On-demand measurement: this means the bank of ADCs perform a sequence when triggered by a SOC command, where SOC means start of conversion. Typically, the user periodically sends a SOC command followed by the reading of the measured values of the most important channels, namely all cell voltages, temperatures and current.

Table 10. Working mode versus measurements

Operating mode	On-demand measurements	Voltage/temperature cyclic measurements	Current measurement	Coulomb counter	Reference
Normal mode	Available	Available, if SYS_CFG1[CYCLIC_TIMER] ≠ 0	Available and running continuously if enabled by setting SYS_CFG1[I_MEAS_EN] = 1	Available and running continuously if enabled by setting SYS_CFG1[I_MEAS_EN] = 1 Exception: when the device transitions from sleep to normal mode, it is frozen until it is read and reset by the user	Section 9.3.4
Diagnostic mode	Available	Not available	Available and running continuously if enabled by setting SYS_CFG1[I_MEAS_EN] = 1	Available and running continuously if enabled by setting SYS_CFG1[I_MEAS_EN] = 1	Section 9.3.6
Sleep mode	Not available	Available, if SYS_CFG1[CYCLIC_TIMER] ≠ 0	Available if enabled by setting SYS_CFG1[I_MEAS_EN] = 1, timing depends on SYS_CFG1[CYCLIC_TIMER] (it must be ≠ 0)	Available if enabled by setting SYS_CFG1[I_MEAS_EN] = 1, timing depends on SYS_CFG1[CYCLIC_TIMER] (it must be ≠ 0)	Section 9.3.5
other modes	Not available	Not available	Not available	Not available	

9.2 Power supplies and reset

9.2.1 Decoupling of power supplies

The recommended decoupling of power supplies is shown in Figure 7 The capacitors should be placed close to the IC pins.

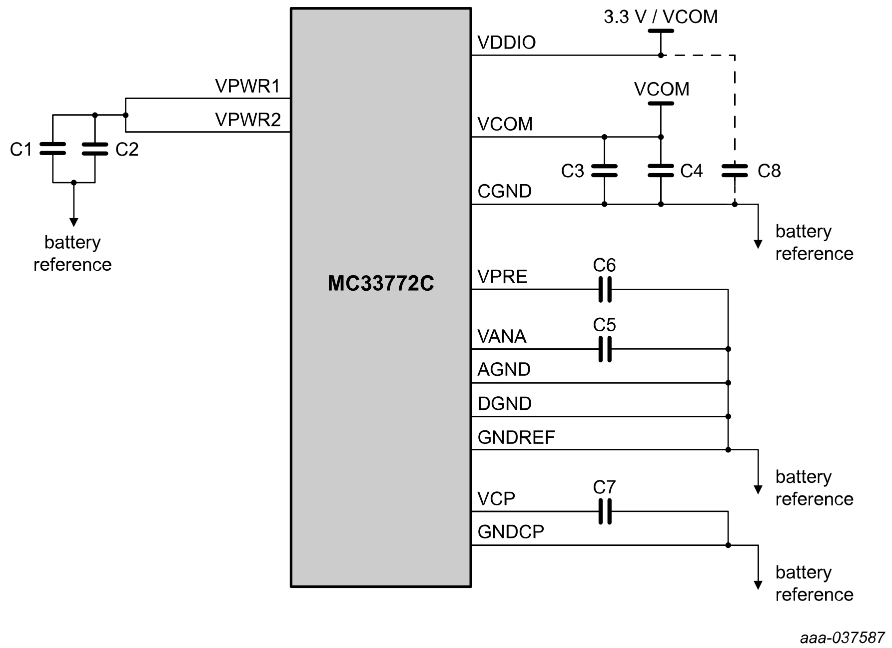


Figure 7. Recommended decoupling of power supplies

Table 11. Recommended capacitor values for power supply decoupling

ID	Value	Units	Comments
C1	220	nF	
C2	1	nF	
C3	2.2	µF	Ceramic capacitor
C4	220	pF	
C5	47	nF	Ceramic capacitor
C6	470	nF	
C7	10	nF	
C8	100	nF	Only necessary for 3.3 V SPI applications where VDDIO is not connected to VCOM

9.2.2 VPWR overvoltage, low-voltage

The MC33772C incorporates comparators to monitor VPWR pins for overvoltage and low-voltage conditions. In the event the voltage on VPWR pin is above the overvoltage threshold $V_{PWR(OV\_Flag)}$ for greater than the $t_{VPWR(Filter)}$ period, the overvoltage fault flag is set in FAULT1_STATUS[VPWR_OV_FLT].

When unmasked by FAULT_MASK1[MASK_12_F], the FAULT1_STATUS[VPWR_OV_FLT] bit sets the FAULT output pin high. An overvoltage condition on the VPWR pin does not cause the MC33772C to perform a shutdown. The pack controller may clear the FAULT1_STATUS[VPWR_OV_FLT] bit when V_{PWR} returns to the normal operating range by writing logic 0 to the FAULT1_STATUS[VPWR_OV_FLT] bit.

When unmasked by FAULT_MASK1[MASK_11_F], a low-voltage condition on VPWR pin causes the FAULT1_STATUS[VPWR_LV_FLT] bit to be set. The FAULT1_STATUS[VPWR_LV_FLT] bit may be cleared when the normal operating range voltage resumes on the VPWR pin and by writing logic 0 to the FAULT1_STATUS[VPWR_LV_FLT] bit.

9.2.3 VCOM supply

The VCOM supply is a linear regulator used to supply power for communication, GPIOx, SPI interface, external temperature sensor reference, and optional external EEPROM.

The VCOM supply is monitored by the MC33772C for undervoltage. Excessive load on the VCOM pin activates VCOM current limit causing an undervoltage fault condition to occur. During the event, the FAULT2_STATUS[VCOM_UV_FLT] fault bit is set and the regulator enters $t_{VCOM(RETRY)}$ shutdown/retry strategy.

Undervoltage shutdown of the VCOM supply directly affects communication, GPIO outputs and external temperature measurements. In addition to setting the individual fault bits for each ANx/GPIO, multiple faults may be set in the FAULTx_STATUS register.

Faults may be cleared by the pack controller when communication resumes. VCOM also has a comparator that monitors for overvoltage. In the event the voltage on VCOM becomes greater than $V_{COM(OV)}$, the FAULT2_STATUS[VCOM_OV_FLT] fault flag is set.

9.2.4 VANA supply

The VANA supply is an internal 2.5 V supply used by the MC33772C for analog control. No circuits other than the decoupling capacitor should be terminated to the VANA pin. The VANA supply is monitored by the MC33772C for undervoltage. External load on the VANA pin activates the VANA current limit causing an undervoltage fault condition to occur. During the event, the FAULT2_STATUS[VANA_UV_FLT] fault bit is set and the regulator enters $t_{VANA(retry)}$ shutdown/retry strategy.

Undervoltage shutdown of the VANA supply directly affects the performance of the analog to digital converters generating fault condition. Additionally, VANA is monitored by the ADC converter for an overvoltage condition each time a conversion sequence is performed. In the event VANA exceeds the $V_{ANA(OV)}$ threshold, the FAULT2_STATUS[VANA_OV_FLT] is set.

9.2.5 VPRE supply

The VPRE supply is an internal pre-regulator supply that sources power to low-voltage sections of the MC33772C. VPRE is the input supply to the VCOM and VANA regulators. The VPRE pin can only be connected to the decoupling capacitor and, in case the SPI communication mode needs to be selected, to one end of the 10 kΩ resistor, whose other end is connected to SPI_COM_EN.

9.2.6 VCP supply

The VCP is an internal power supply generated by a doubler charge pump that is fed by VPRE. The VCP pin can only be connected to a 10 nF decoupling capacitor. The other end of such capacitor must be connected to its dedicated ground, namely GNDCP.

9.2.7 VDDIO supply

The VDDIO is an external power supply that enters the IC through a pin having the same name. The purpose of it is supplying power to the SPI and I^2C interfaces at 3.3 V or 5.0 V, depending on the input voltage. In 5.0 V applications, the VDDIO pin can be shorted to the VCOM pin, eliminating the use of an external supply.

9.2.8 Power on reset (POR)

The MC33772C has two sources of power on reset (POR) in the IC system. An undervoltage condition on the VPWR pin causes the MC33772C to reset. Upon returning from undervoltage, the MC33772C performs a POR.

The second source of potential POR occurs during transient conditions when the internal digital logic supply voltage drops below the critical threshold where logic states cannot be guaranteed. In this case, the MC33772C performs a power on reset.

Power on reset is indicated by the FAULT1_STATUS[POR] bit. In the event of a POR, all registers in the MC33772C are set to their power on reset state and the FAULT pin becomes active.

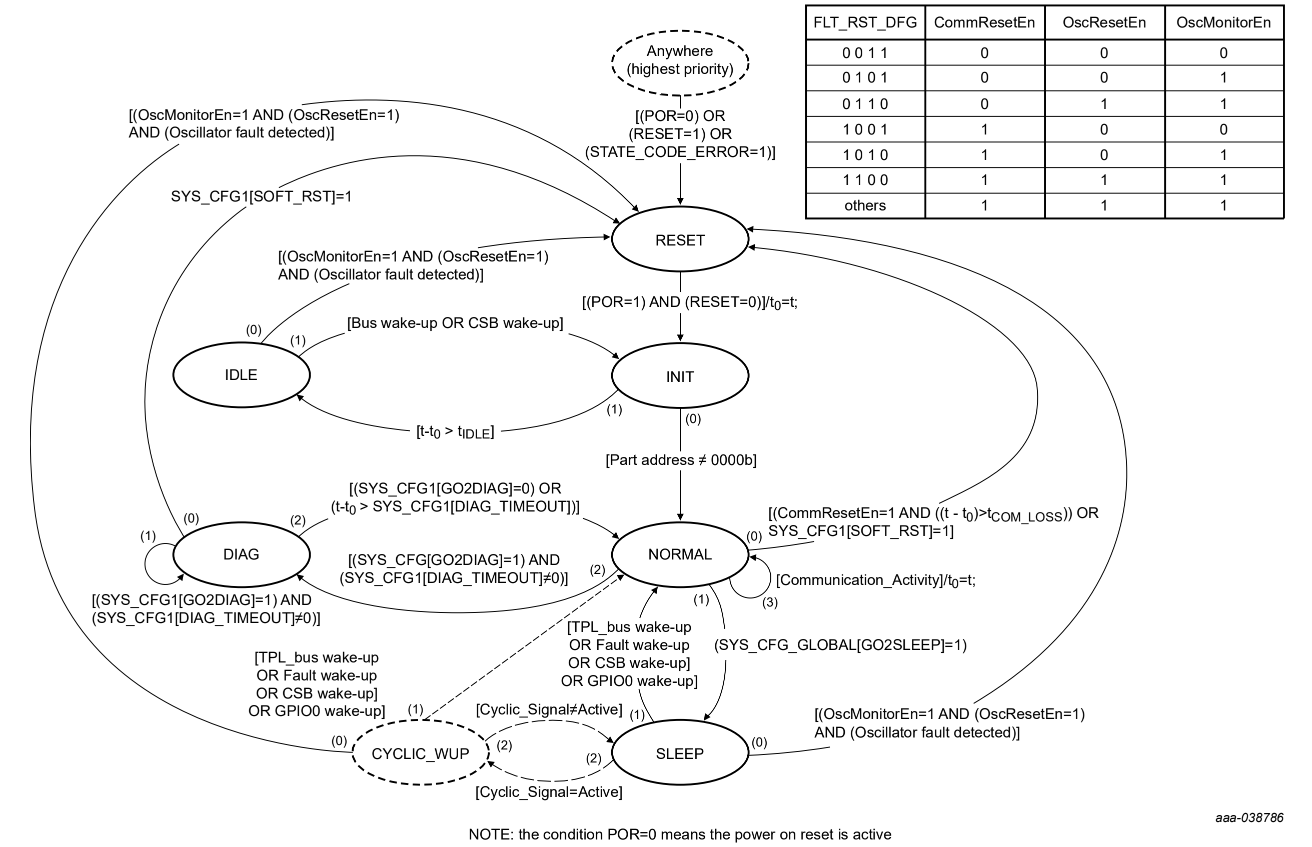
9.2.9 Hardware and software reset

An active high on the RESET pin for greater than the $t_{RESETFLT}$ filter time causes the MC33772C to reset. Software resets are performed when the MC33772C receives a message written to the SYS_CFG1[SOFT_RST] bit. Hardware and software resets are indicated by the status of the FAULT1_STATUS[RESET_FLT] bit, and the FAULT pin becomes active. After a HW or SW reset, it is necessary to wait for the time interval $t_{VPWR(READY)}$ before being possible to reprogram the part.

9.3 Modes of operation

From Reset mode, the MC33772C must be initialized with a cluster ID before the device is allowed to enter Normal mode. After initialization, the MC33772C enters Normal mode. In Normal mode the device is in full operation performing the necessary safety functions as well as on-demand conversions. When commanded to Sleep mode, the device will have reduced current consumption. Diagnostic mode provides a method for diagnosing the integrity of many safety functions as well as internal or external faults that may have occurred. If properly configured, if there is no traffic during Normal mode on the bus during t_{COM_LOSS}, the MC33772C will reset.

In the event the device is powered up and not initialized, the MC33772C enters the low-power Idle mode after a t_{IDLE} timeout period. Detecting a wake-up pattern transfers the MC33772C to the initialization state Init where the CID can be programmed. In Figure 8, an integer number enclosed in round brackets close to a transition arc indicates the priority of such a state transition in case the conditions are verified at the same time. The lower the number is, the higher is the priority, so if several conditions are true at the same time, the one with lowest priority number determines the state transition; a boolean condition is enclosed between square brackets. A list of actions after the state transition condition is preceded by the slash symbol. Symbol "t" represents the absolute time, symbol t_0 stays for a variable having the dimension of time.



FLT_RST_DFG	CommResetEn	OscResetEn	OscMonitorEn
0 0 1 1	0	0	0
0 1 0 1	0	0	1
0 1 1 0	0	1	1
1 0 0 1	1	0	0
1 0 1 0	1	0	1
1 1 0 0	1	1	1
others	1	1	1

Figure 8. Operating mode state diagram

Table 12. Power supply mode operation

	Normal/Init mode	Diagnostic mode	Cyclic Wake-up	Sleep/Idle mode
Supplies active	VCOM = ON, VANA = ON, VPRE = ON, VCP = ON	VCOM = ON, VANA = ON, VPRE = ON, VCP = ON	VCOM = ON (during cycle), VANA = ON (during cycle), VPRE = ON, VCP = ON	VCOM = 0, VANA = 0, VPRE = ON, VCP = ON
Communication	Communication enabled	Communication enabled	Communication enabled (during cycle)	Wake-up function only

9.3.1 Reset mode

The table in Figure 8 provides information about the mapping between all possible values of the SYS_CFG2[FLT_RST_CFG] field, which may be written and read by the user, and the corresponding values of the following internal bits, which are not user readable:

- CommResetEN: If it is equal to 1, the IC reset due to a communication timeout in Normal mode is enabled, else it is disabled
- OscResetEN: If it is equal to 1, the IC reset due to the detection of a defective oscillator in Sleep mode is enabled, else it is disabled
- OscMonitorEN: If it is equal to 1, the oscillator monitoring is enabled, else it is disabled

The value "others" readable in the column labeled as SYS_CFG2[FLT_RST_CFG] refers to values that are different from those listed above.

The registers are reset to their default values, except some bits of the FAULT1_STATUS register.

9.3.2 Idle mode

The MC33772C enters Idle mode from Init mode when the communication bus is not active for the t_{IDLE} time period. While the MC33772C is in Idle mode, no messages are recognized, only a valid wake-up sequence lets the device transition from Idle mode to Init mode. When the MC33772C is configured as a SPI interface and enters Idle mode, the device transitions from Idle mode to Init mode if CSB duration is larger than CSB_{WU_FLT} maximum value, otherwise the pulse will be considered as a glitch and then filtered.

9.3.3 Init mode

After a Power On Reset (POR) or Reset (Soft RST or pin RESET), the MC33772C enters Init mode. The MC33772C's cluster ID is 0 (unassigned CID). All registers, except the Init register, are read-only. In Init mode, any unassigned MC33772C does not forward any message and responds (if needed) only on the side that received a request. The user has to assign a Cluster ID between 1 and 63, to enter Normal mode. This assignment is mandatory for both SPI and TPL communication. If the assignment of a Cluster ID is not performed within the t_{IDLE} timeout, Idle mode will be entered to reduce current consumption.

9.3.4 Normal mode

In Normal mode, on reception of a valid message, the MC33772C executes the commanded operation. Device configuration registers control the operating characteristics of the MC33772C and are all programmed while the device is in Normal mode. Once programmed, the MC33772C performs safety operations like overvoltage and undervoltage in the background without further instruction from the pack controller[1].

To accomplish the safety operations in Normal mode, the MC33772C performs a cyclic conversion sequence at the programmed timed interval. In the event the MC33772C receives an on-demand conversion request from the pack controller during a cyclic conversion, the device stops the cyclic conversion and immediately starts the on-demand conversion cycle. Halting the cyclic conversion and performing the on-demand conversion allows all MC33772C devices in the system to achieve synchronized measurements. From Normal mode, the MC33772C may be commanded to Sleep mode or Diag mode. If instructed by a proper value of the SYS_CFG2[FLT_RST_CFG] field, the part automatically resets whenever the communication is absent for longer than t_{COM_LOSS}.

1 The cyclic measurement is disabled by default. Cyclic measurement can be activated by writing to SYS_CFG1[CYCLIC_TIMER].

9.3.5 Sleep mode

Sleep mode provides a method to significantly reduce battery current and the overall quiescent current of the battery management system. In Sleep mode, the overvoltage, undervoltage, overtemperature, undertemperature, and overcurrent circuitry can remain cyclically active[2], as well as the monitoring of V_{PWR}.

Based on the CYCLIC_TIMER setting, the MC33772C may continue performing cyclic conversions in Sleep mode. This is the meaning of the dotted bubble labeled as CYCLIC_WUP in the state diagram shown in Figure 8. The permanence time in the CYCLIC_WUP transient state is really short; it is basically the time needed to turn on the VCOM power supply and to acquire 20 channels.

In the event a conversion value is greater than or less than the threshold value and the particular wake-up/fault is unmasked, the MC33772C performs a bus wake-up and can activate the FAULT pin.

To instruct the MC33772C to enter the Sleep mode, the user sets the SYS_CFG_GLOBAL[GO2SLEEP] bit to logic 1. If the communication type is TPL, only a global write command can be used, while in case of pure SPI communication, a local write command is necessary. In case the ADCs are performing acquisition (for a single sample or an average of N samples), the transition is delayed until the ongoing sequence is completed. It means that a single sample will be correctly acquired while an average will be potentially interrupted; in this latter case MEAS_CELLx registers cannot be updated (DATA_RDY bit stays at 0 until the completion of the next average).

Exit from Sleep mode is possible if one of the following occurs:

- Upon detection of a bus wake-up sequence, in TPL mode only
- By transitioning the CSB pin from low state to high state (shortly referred to as CSB wake-up)
- Upon detection of at least one out of a certain number of fault conditions (see FAULT1_STATUS, FAULT2_STATUS and FAULT3_STATUS along with their associated wake-up mask registers WAKEUP_MASK1, WAKEUP_MASK2 and WAKEUP_MASK3)[3]
- Depending on the content of SYS_CFG2[FLT_RST_CFG] field, it is possible to set the OscResetEn variable to 1. This causes a reset if the oscillator monitor function detects a clock malfunction, signaled by the FAULT2_STATUS[OSC_ERR] = 1
- Wake-up by GPIO0

The CSB wake-up capability implies some system considerations when SPI communication is used. Assuming the CSB line is pulled up to the same power supply used by the MCU, when the MCU commands the MC33772C to go to sleep and then the MCU itself goes to sleep, both devices sleep until the time the MCU wakes up. However, when this happens, the MC33772C wakes up because the CSB line transitions from low state to high state. To avoid this behavior, the MCU has to take care to force the CSB line to the high state during the entire sleep time.

9.3.6 Diagnostic mode

In Diagnostic mode, the system controller has extended control of the MC33772C in order to execute performance integrity checks of the device. It is critical to note that when the MC33772C is in Diagnostic mode, cyclic conversions are halted and OV/UV/OT/UT detection is not performed automatically. To perform OV/UV/OT/UT or any other protection feature that requires a conversion, an on-demand conversion message must be sent by the pack controller.

To prevent the MC33772C from remaining in diagnostic mode without automatic OV/UV/OT/UT detection, a protection DIAG_TIMEOUT timer has been implemented. In the event of the timeout, the MC33772C reverts to Normal mode and sets the bit FAULT3_STATUS[DIAG_TO_FLT] to logic 1.

2 The cyclic measurement is disabled by default. Cyclic measurement can be activated by writing to SYS_CFG1[CYCLIC_TIMER].

3 The wake-up performed by MC33772C under the detection of internal fault is disabled by default. It can be activated by writing to registers WAKEUP_MASK1, WAKEUP_MASK2 and WAKEUP_MASK3.

To enter diagnostic mode, the user must set the SYS_CFG1[GO2DIAG] bit to logic 1. To exit diagnostic mode, the user must clear the SYS_CFG1[GO2DIAG] bit.

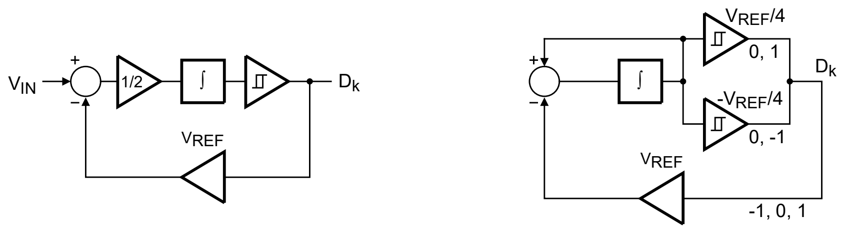
Note: *If cyclic acquisition is enabled, before transitioning to diagnostic mode, the cyclic acquisition needs to be disabled. Disabling of cyclic acquisition and GO2DIAG should be two separate commands sent by MCU.*

9.4 Analog to digital converters ADC1-A, ADC1-B, ADC2

At the heart of the MC33772C are three hybrid ADCs using a 6.0 MHz clock and having two modes of operation, called *phases*:

- Incremental phase: it is necessary to compute the most significant bits. During this first phase, the ADC operates as shown in Figure 9 (left part). It appears equal to a 1st order ΣΔ, but it has no memory, as the initial state is always 0.
- The second phase, referred to as cyclic phase, is needed to extract the least significant bits. During this phase, the converter is blind to the input (but not to the reference) and performs the conversion of the residual error.

This ADC, which is built around a switched capacitor integrator, is much faster than a ΣΔ, an essential feature when the input comes from a multiplexer and the channel switching has to be very fast. There is no decimation downstream the ADC.



The output of the integrator V_N at the end of the incremental phase is given by:

$$V_N = \frac{N \,.\, V_{IN} - V_{REF} \,.\, \sum_{k=1} D_k}{2}$$

The integrator is updated at each cycle. The current output of the integrator, V_k, is linked to the previous one, V_{k-1}, by the following relationship.

$$V_k = 2 \,.\, V_{k-1} - D_{k-1} \,.\, V_{REF}$$

aaa-027851

Figure 9. ADC converter: incremental phase (left) and cyclic phase (right)

The ADC architecture affords the user the flexibility to select the speed vs. accuracy. Conversion resolution setting for ADC1-A, ADC1-B and ADC2 are programmable from 13 to 16 bits (see Section 11.7). ADC1-A and ADC1-B settings must be equal to each other.

9.4.1 High precision voltage reference

To guarantee the accuracy of all ADC conversion data, the MC33772C integrates a high precision fully compensated voltage reference.

9.4.2 Measurement sequence

The MC33772C performs on-demand differential measurements of external inputs and internal measurements using three ADC converters for measurement, calibration, and diagnostics. Once the device is initialized, on-demand conversions are initiated by writing to the ADC_CFG[SOC] convert register or a GPIO2 input trigger.

The ADC_CFG register contains the conversion parameters for ADC1-A, ADC1-B, and ADC2 converters and the start conversion bit for synchronization. Writing a logic 1 to the SOC bit initiates the conversion sequence. Conversions in progress may be interrupted by reinitiating a new conversion. Measurements for each ADC converters in the MC33772C have a predefined measuring sequence. Voltage conversions coming from ADC1-A and ADC1-B are synchronized with free running current measurements performed by ADC2.

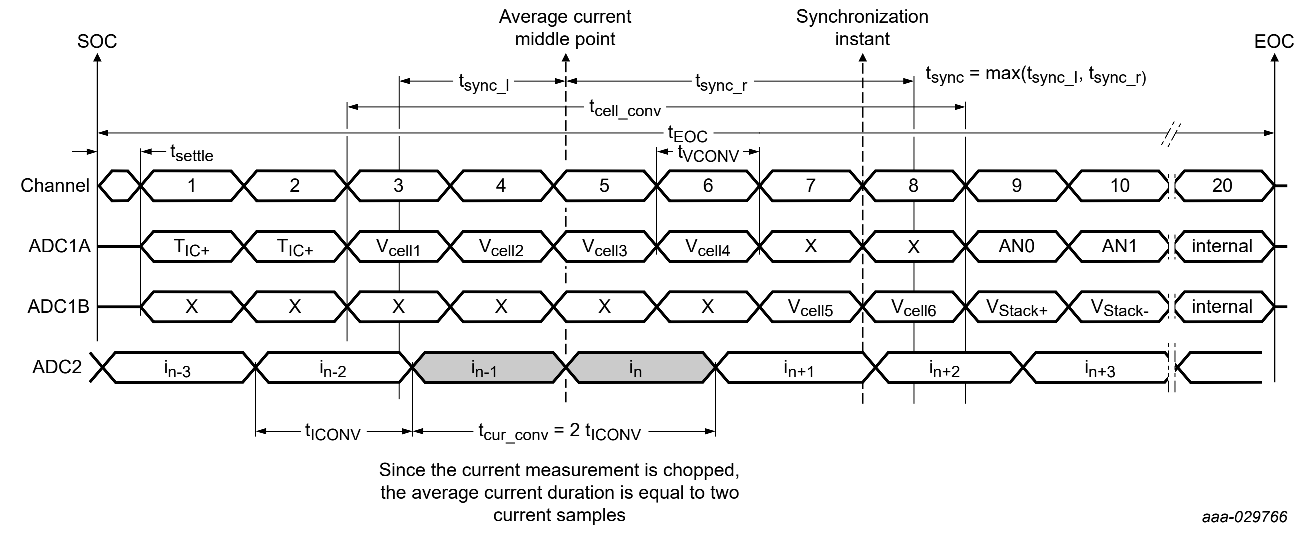


Figure 10. ADC conversion sequence in normal mode

Immediately after receipt of a conversion request, there is a dead time t_{SETTLE}, after which ADC1-A and ADC1-B converters start their conversion sequence. Voltage conversions of ADC1-A and ADC1-B run asynchronously with the current measurements performed by ADC2 as shown in Figure 10.

At time t_{CELL_CONV}, all voltage and current samples are frozen and then post-elaborated. Offset is measured and canceled, a multiplicative correction with a gain depending on the IC die temperature is performed. The completion of the entire sequence, whose length is equal to 20 time slots, occurs at time t_{EOC}. All results are stored into user registers and their associated data ready bits are set to Logic 1. Channels identified as "internal" are used for calibration purposes and are performed at each conversion sequence. Information on how the data is tagged and stored is provided in Section 10. On-demand conversions are not only used for storing measurement results in user registers, but also for OV/UV/OT/UT comparisons.

The MC33772C features a synchronized voltage and current measurements for each requested conversion. Synchronization point is after the 7th channel, that is, at this time the IC takes a snapshot of the latest two chopped conversions of the current signal, the average of which is calculated to get rid of the current offset.

The meaning of the time t_{SYNC} is the maximum value of two time intervals, t_{SYNC_L} and t_{SYNC_R}, where:

- t_{SYNC_L} is the time interval between the middle point of the first voltage conversion and the instant corresponding to middle point of the latest valid average current value
- t_{SYNC_R} is the time interval between the previously mentioned instant and the middle point of the eighth converted channel

Table 13 shows how the user channels are mapped in the 20 available time slots per ADC. Symbols Vbg_tj_a and Vbg_tj_b correspond, respectively, to contents of MEAS_VBG_DIAG_ADC1A and MEAS_VBG_DIAG_ADC1B registers. They represent the measurements of the same diagnostic band gap.

Table 13. ADC conversion sequence multiplexer inputs

ADC conversion	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
ADC1-A	IC temp	IC temp	Cell 1	Cell 2	Cell 3	Cell 4			AN0	AN1	AN2	AN3	AN4	AN5	AN6	Vbg_tj_a	internal	internal	internal	internal
ADC1-B							Cell 5	Cell 6	Stack	Stack	internal	VANA	Vbg_tj_b	internal	internal	internal	internal	internal	internal	internal

In addition to on-demand conversions requests, the MC33772C provides timing control for cyclic measurements, that is, conversions occurring with no need for the pack controller to repeatedly send SOC commands.

Cyclic measurements are useful for automatic OV/UV/OT/UT check. The user may select the cycle period by programming register SYS_CFG1[CYCLIC_TIMER]. The effective duration of a cyclic sequence is given by the t_{EOC} parameter. A cyclic sequence does not affect the content of the measurement registers (namely, of registers MEAS_xxxx), while it has effect on the content of CELL_OV_FLT, CELL_UV_FLT, AN_OT_UT_FLT and FAULTx_STATUS registers.

An undervoltage on VANA might alter the functioning of the ADC. This could result in the detection of nonexistent faults. Therefore, if FAULT2_STATUS[VANA_UV_FLT] is set, the following faults should be ignored:

- FAULT1_STATUS[VPWR_OV_FLT]
- FAULT1_STATUS[AN_UT_FLT]
- FAULT1_STATUS[CT_OV_FLT]
- FAULT2_STATUS[VANA_OV_FLT]
- FAULT2_STATUS[ADC1_A_FLT]
- FAULT2_STATUS[ADC1_B_FLT]
- FAULT3_STATUS[VCP_UV]

9.4.2.1 Voltage averaging

The MC33772C provides a feature of on-demand, on-chip voltage averaging. Using this feature, cell terminal voltage, Vstack voltage, and VrefA and VrefB voltages can be averaged for a configured number of samples. Averaging makes the measurement data more robust to noise, the averaging feature acts as a digital low pass filter. The on-chip averaging feature of MC33772C reduces the MCU load by performing the averaging on-chip and also reducing the number of communication frames to be exchanged between master and slave.

After initialization of MC33772C, averaging can be triggered by configuring the ADC_CFG register as described in Section 11.7. The number of samples to be averaged is chosen by writing to bit-field ADC_CFG[AVG] and accumulation of samples to be averaged is initiated by setting bit-field ADC_CFG[SOC] to logic 1 or by triggering GPIO2 input. Once the averaging is started the MC33772C accumulates the configured number of samples and divides the accumulated value by the number of configured samples. The final value is updated in MEAS_CELLxx registers.

Ongoing accumulation of samples can only be interrupted by the GO2SLEEP and GO2DIAG commands. However, the averaging can be restarted with a new SOC command. On reception of a new SOC command, the MC33772C discards the ongoing measurement (accumulation) and starts the new measurement. It is to be noted that the feature of voltage averaging is not available for cyclic measurement.

In Normal mode, during ongoing averaging the device can interrupt the voltage averaging and change its mode of operation. However, the GO2SLEEP and GO2DIAG commands have certain priority over averaging. The MC33772C performing averaging is able to transition to Sleep or Diagnostic mode on reception of a valid GO2SLEEP or GO2DIAG command but only after completion of the ongoing sequence of measurement.

9.4.3 Measurement processing

After all channels are converted, they need to be post-processed. Three operations are performed before the final value is available:

- Offset compensation
- Gain compensation
- Temperature compensation

This can be seen in Table 14. The columns labeled as "Gain comp.?" and "By…" show if the input signals are gain compensated (yes/no) and by which gain. For instance, GCF_c1 stays for a gain, which may be calculated by using GCF_room_c1, GCF_hot_c1 and GCF_cold_c1 variables specified in Table 89. In this table, attributes "cold" and "hot" refer to –40 °C and 89 °C respectively, and attribute room refers to 25 °C. A gain mayor may not depend on the temperature (column "Temp. comp.?" may attain the value yes or no). If a gain depends on the IC temperature, there are three scalar gains. For instance, GCF_cold_cx, GCF_room_cx, GCF_hot_cx represent respectively the delta gain compensation values at cold (−40 °C) room (+25 °C) and hot (+89 °C) temperature of the die. They are used to calculate, by delta gain compensation, the actual value of gain at any temperature.

ADC2 works with GCF_ix (x = 4, 16, 64, 256), depending on the current gain used by the PGA. See Table 89. The value of a gain is centered on the targeted channel resolution, so it is of the form 1 + DG. Therefore, DG is centered on zero and is represented in two's complement. In the IC, only the DG part of the gain needs to be stored. See Table 15.

Table 14. Gain compensation

Measured channel	No.	Offset comp.?	Gain comp.?	By...	Temp. comp.?	Result stored in...	...checked by...	... in the range of	
By ADC1-A									
ICTEMP1	1	Chopper	Yes	GCF_IcTemp	No	MEAS_IC_TEMP			
ICTEMP1	2	Chopper	Yes	GCF_IcTemp	No	MEAS_IC_TEMP			
CT1	3	Yes	Yes	GCF_c1	Yes	MEAS_CELL1	IC	CT1_UV_TH	CT1_OV_TH
CT2	4	Yes	Yes	GCF_c2	Yes	MEAS_CELL2	IC	CT2_UV_TH	CT2_OV_TH
CT3	5	Yes	Yes	GCF_c3	Yes	MEAS_CELL3	IC	CT3_UV_TH	CT3_OV_TH
CT4	6	Yes	Yes	GCF_c4	Yes	MEAS_CELL4	IC	CT4_UV_TH	CT4_OV_TH
Unused	7								
Unused	8								
AN0	9	Yes	Yes	GCF_ANx_ratio [1]	No[1]	MEAS_AN0	IC	AN0_UT_TH	AN0_OT_TH
AN1	10	Yes	Yes	GCF_ANx_ratio [1]	No[1]	MEAS_AN1	IC	AN1_UT_TH	AN1_OT_TH
AN2	11	Yes	Yes	GCF_ANx_ratio [1]	No[1]	MEAS_AN2	IC	AN2_UT_TH	AN2_OT_TH
AN3	12	Yes	Yes	GCF_ANx_ratio [1]	No[1]	MEAS_AN3	IC	AN3_UT_TH	AN3_OT_TH
AN4	13	Yes	Yes	GCF_ANx_ratio [1]	No[1]	MEAS_AN4	IC	AN4_UT_TH	AN4_OT_TH
AN5	14	Yes	Yes	GCF_ANx_ratio[1]	No[1]	MEAS_AN5	IC	AN5_UT_TH	AN5_OT_TH
AN6	15	Yes	Yes	GCF_ANx_ratio[1]	No[1]	MEAS_AN6	IC	AN6_UT_TH	AN6_OT_TH
V_{BG_TJ}	16	Yes	Yes	GCF_Vbgtj1	Yes	MEAS_VBG_DIAG_ADC1A	IC	Internal reference	
Reserved	17								
Reserved	18								
Reserved	19								
Reserved	20								
By ADC1-B									
Unused	1								
Unused	2								
Unused	3								
Unused	4								
Unused	5								
Unused	6								
CT5	7	Yes	Yes	GCF_c5	Yes	MEAS_CELL5	IC	CT5_UV_TH	CT5_OV_TH
CT6	8	Yes	Yes	GCF_c6	Yes	MEAS_CELL6	IC	CT6_UV_TH	CT6_OV_TH
Stack	9	Chopper	Yes	GCF_stack	No	MEAS_STACK			
Stack	10	Chopper	Yes	GCF_stack	No	MEAS_STACK			
Reserved	11								
VANA	12	Yes	Yes	GCF_c1	Yes	ADC1_B_RESULT	IC		VANA_OV_TH
V_{BG_TJ}	13	Yes	Yes	GCF_Vbgtj2	Yes	MEAS_VBG_DIAG_ADC1B	IC	Internal reference	
Reserved	14								
Reserved	15								
Reserved	16								
Reserved	17								
By ADC2									
ISENSE	1	Chopper	Yes	GCF_i4-256	Yes	MEAS_I	IC		TH_ISENSE_H

Table 14. Gain compensation_...continued_

Measured channel	No.	Offset comp.?	Gain comp.?	By...	Temp. comp.?	Result stored in...	...checked by...	... in the range of	
ISENSE	2	Chopper	Yes	GCF_i4-256	Yes	MEAS_I	IC		TH_ISENSE_H

[1] It is assumed that all ANx have been programmed as ratiometric; in case a certain ANx is programmed as an absolute input, the gain GCF_ANx_ratio gets replaced by GFC_c1 and the 'No' value contained in the column labeled 'Temp. comp.?' is replaced by a 'Yes'.

9.5 Cell terminal voltage measurement

Cell terminal voltages are monitored differentially, level shifted and multiplexed to the ADC1-A and ADC1-B converters. Conversion results of the cells are available in MEAS_CELLx registers.

Unused cell terminal (CTx) inputs may be terminated as described in Section 13.2.2. Overvoltage and undervoltage of unused inputs should be disabled through the OV_UV_EN[CTx_OVUV_EN] bits to prevent the input from triggering fault events. Conversions performed on unused inputs result in nearly zero ADC values.

The differential measurement of each cell terminal input is designed to function in conjunction with external anti-aliasing filter (see Section 13.2).

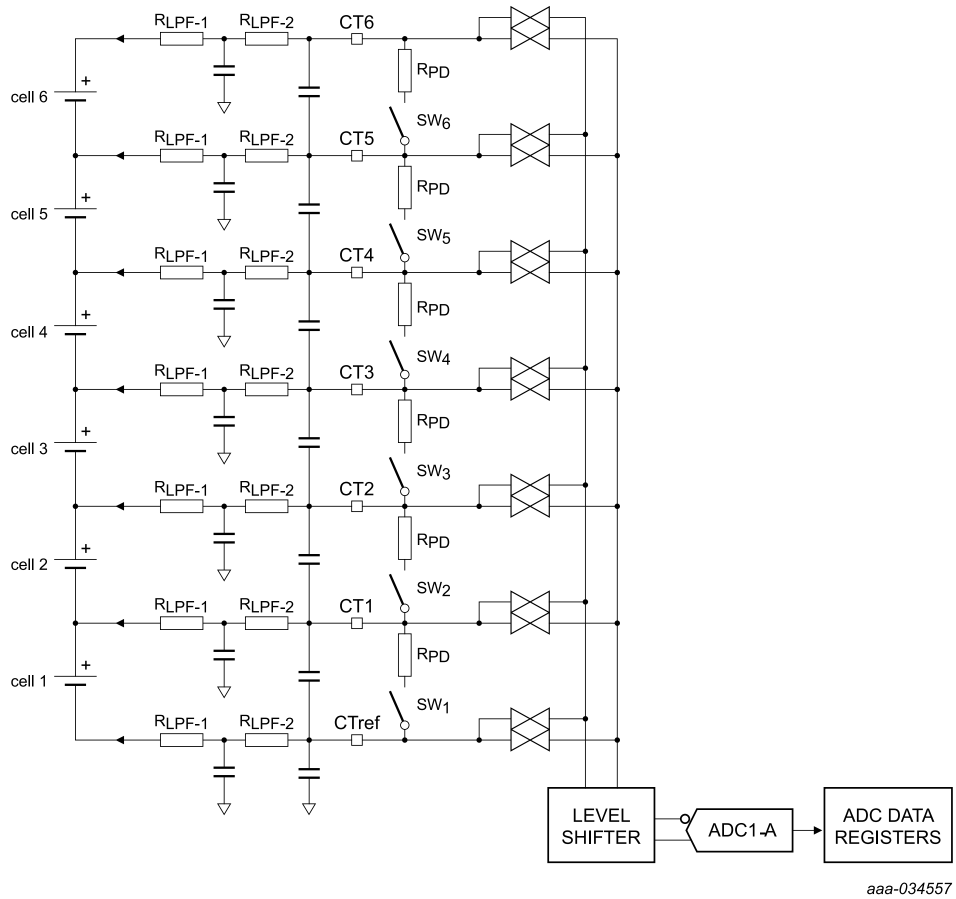


Figure 11. ADC1-A voltage measurement chain

9.6 Current measurement

Current measurement channel features 16-bit ADC with an automatic programmable gain amplifier (PGA) allowing the user to accurately measure current from −1500 A to 1500 A (the actual range is in terms of voltage and is given by min and max of V_{IND}) with a 6.0 mA resolution (in terms of voltage it is V_{2RES}) when using a single 100 µΩ shunt resistor. The current channel includes automatic gain selection, redundant measurement path, and internal diagnostics.

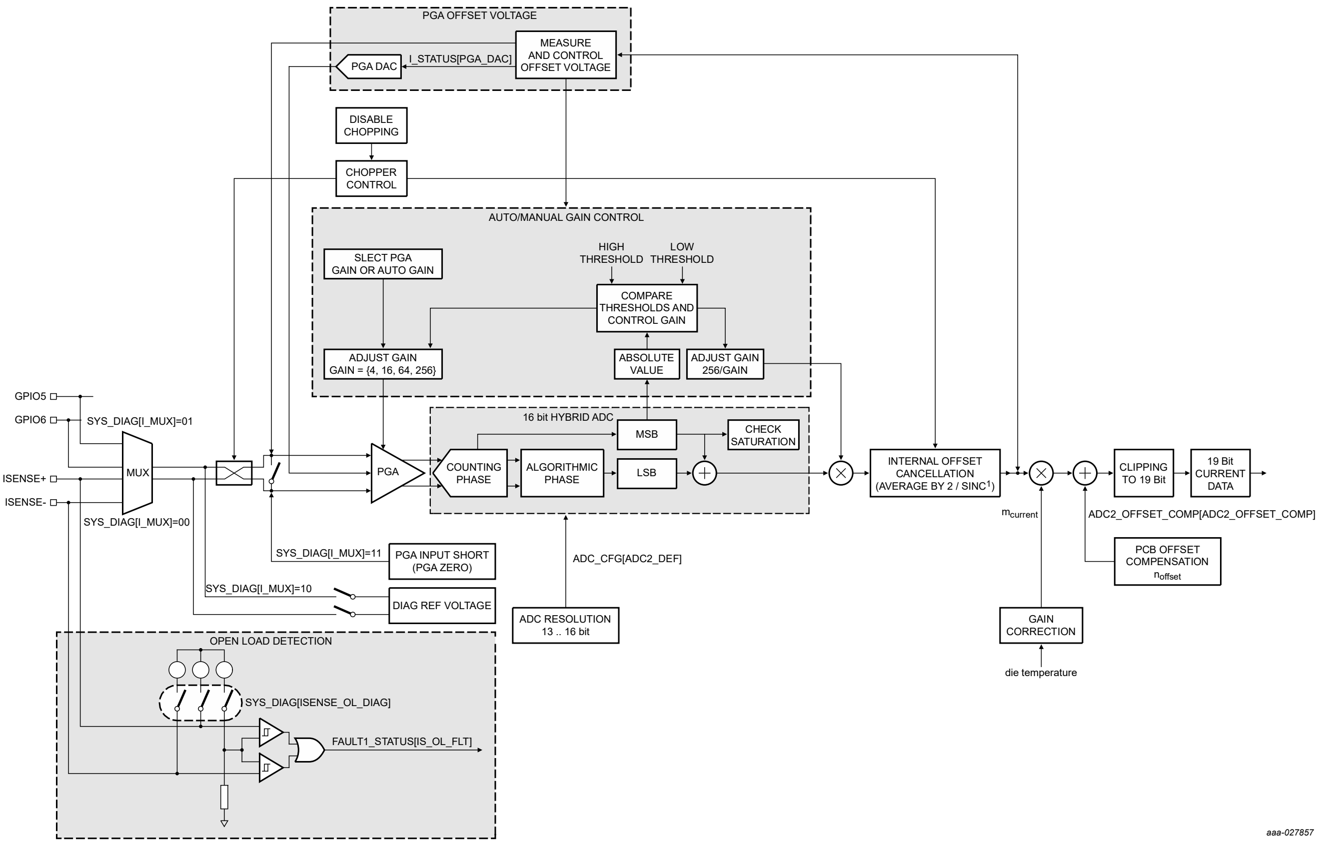


Figure 12. Current measurement channel

From initialization, the current measurement chain is disabled. The MCU controller must enable the measurement chain by setting the SYS_CFG1[I_MEAS_EN] bit to logic 1, to initiate continuous current conversions. Current measurement conversions for coulomb counting are performed continuously in Normal and Diagnostic modes, while in Sleep mode they occur periodically and the period is given by SYS_CFG1[CYCLIC_TIMER].

Note: *The conversion command ADC_CFG[SOC] must be sent at least 27 µs after SYS_CFG1[I_MEAS_EN] is enabled.*

The Current Acquisition Channel fulfills accuracy and dynamic range requirement through:

- The Auto-Zero Compensation feature is guaranteeing the PGA dynamic range.
- A chopper function is ensuring a reduced offset introduced by the acquisition Chain.

The automatic auto-zero compensation for the PGA is performed each time the current measurement channel gets enabled. The time to perform the procedure is given by the parameter t_{AZC_SETTLE}.

To minimize the offset introduced by the acquisition chain, the chopper sends alternatively and repetitively, the ISENSE+/– differential inputs and the ISENSE–/+ differential inputs (reverse input pair) to the PGA differential inputs. Downstream the ADC2, a digital post-processor computes the difference between the current sample and the past sample and divided it by 2. Therefore, the offset introduced by the acquisition chain is cancelled.

Conversion result of current channel will be stored into MEAS_ISENSE1[MEAS_I_MSB] and MEAS_ISENSE2[MEAS_I_LSB] with a resolution of V_{2RES}, which remains the same regardless of the PGA Gain setting.

Note: *A conversion started with an ADC_CFG[AVG] bit-field set to a non-zero value would result in the toggling of MEAS_ISENSE1[DATA_RDY] and MEAS_ISENSE2[DATA_RDY] between 0 and 1 for each voltage measurement sequence, unless the configured number of sequences are completed. At the end of averaging, the bit MEAS_ISENSEx[DATA_RDY] is stable at the end of last sequence.*

The PGA gain of the current acquisition channel (4, 16, 64, 256) can either be set in a manual or an automatic mode. The setting of the PGA gain in manual or automatic mode can be performed by configuring ADC_CFG[PGA_GAIN] register.

The setting of the PGA gain in automatic mode will also be performed by the automatic gain control. Automatic gain control allows the device to obtain the most appropriate gain setting for the amplifier input signal level. In automatic gain control mode, the conversion result is digitally compared with internally programmed thresholds. See Figure 13.

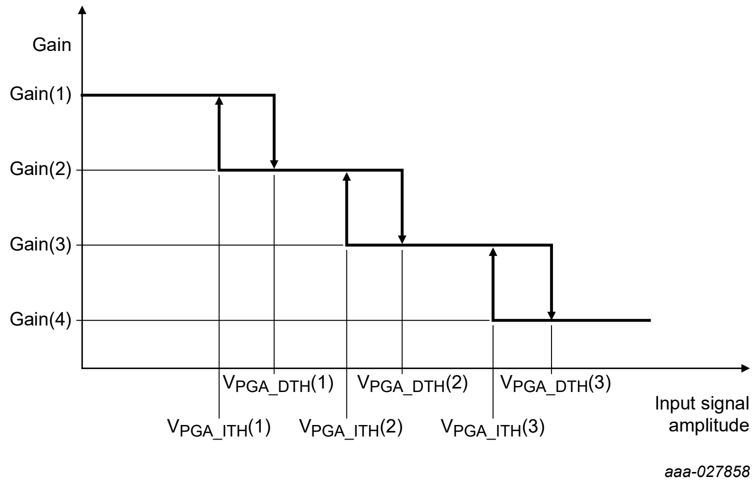


Figure 13. Current measurement channel (gain vs. input signal amplitude)

PGA auto-gain is implemented by applying a hysteresis to each threshold. Saturation of the ADC is reported by the flag MEAS_ISENSE2[ADC2_SAT]. A PGA setting change between two chopped measurements is reported by the flag MEAS_ISENSE2[PGA_GCHANGE] to indicate reduced accuracy for the resulting measurement value. An external low-pass filter is required to prevent an over range event within the PGA. Such event may happen if the time derivative of the current signal is so high that it causes the voltage drop across the ISENSE +/- terminals to exceed the maximum allowed slope value of ±4 V/s. The way this limit on the slope has to be understood is the following: if the battery current changes like a large ideal step, the output signal of the input filter must have a slope whose absolute value must not exceed the aforementioned value. So, this limit only applies to large signals, that is, it does not apply, for example, to a sinusoidal current signal having small amplitude but very large frequency, because a small signal normally does not require a change in the gain value. Large signal signifies that the signal magnitude is so high that the PGA gain is required to be switched to a value different from the currently used one.

ADC2, dedicated to the current measurement channel, performs continuous conversions in Normal and Diagnostic modes. Receiving an on-demand conversion request, the most recent current measurement obtained before the last cell voltage gets converted is stored in MEAS_ISENSE1 and MEAS_ISENSE2 registers, so synchronizing the current with all voltages within the t_{SYNC} window.

The current measurement channel includes a sleep mode wake-up feature. In Sleep mode, the PGA gain is constantly equal to 256 and each cyclic current measurement result is compared with the current wake-up threshold TH_ISENSE_OC register. Three out of four current values above the threshold trigger a system wake-up and activate the fault output when the wake-up enable bit is set.

Note: *If current sense is active (SYS_CFG1[I_MEAS_EN]=1) during sleep mode, cyclic acquisition should not be set to continuous mode (SYS_CFG1[CYCLIC_TIME]=001).*

9.6.1 Gain correction of the current channel

The following is a detailed explanation of the gain correction of the current channel.

- *Room temperature delta gains*:
  GCF_ix (for x = 4, 16, 64, 256 representing all possible PGA gains) with resolution 0.09765625 %, spanning the range (-256…+255).0.09765625 %
- *Cold temperature delta gains*:
  GCF_cold_ix (for x = 4, 16, 64, 256 representing all possible PGA gains) with resolution 0.09765625 %, spanning the range (-16…+15).0.09765625 %
- *Hot temperature delta gains*:
  GCF_hot_ix (for x = 4, 16, 64, 256 representing all possible PGA gains) with resolution 0.09765625 %, spanning the range (-16…+15).0.09765625 %

In contrast to i_gain_x, which is represented by a 9-bit word, GCF_hot_ix and GCF_cold_ix are represented by a reduced number of bits (5) and therefore their range is 16 times smaller than the one at room temperature, because the resolution is the same for all gains. Basically GCF_hot_ix and GCF_cold_ix can only additively correct the i_gain_x respectively in hot and cold conditions. This becomes clear by considering the gain temperature dependency, which is as follows:

If (temperature T is higher than T_room) Then // T is the IC temperature

gain_selected = GCF_hot_ix

Else

gain_selected = GCF_cold_ix

EndIf

DG = GCF_ix + (gain_selected * k(T)) // where k(T) is a stored function, such that: 0 ≤k(T) ≤ 1, k(T_room) = 0 and k(T_cold) = k(T_hot) = 1

Gain = 1 + DG

Table 15. Gain format

Gain = 1 + DG (DG)	Representation: 2's complement (number of bits)	Min (%)	Max (%)	Resolution (%)
GCF_room_cx (odd cell)	10	−6.2500	6.2378	0.01221
GFC_room_c(x+1)vs(x) (even cell vs odd cell)	4 for x = 1 2 for x ≠ 1	–0.098 for x = 1 –0.024 for x ≠ 1	0.085 for x = 1 0.012 for x ≠ 1	0.01221
GFC_cold_cx (odd cell) (cold temp vs room)	7 for x = 1 6 for x ≠ 1	–0.781 for x = 1 –0.391 for x ≠ 1	0.769 for x = 1 0.378 for x ≠ 1	0.01221
GFC_cold_c(x+1)vs(x) (even cell vs odd cell)	6 for x = 1 2 for x ≠ 1	–0.391 for x = 1 –0.024 for x ≠ 1	0.378 for x = 1 0.012 for x ≠ 1	0.01221
GFC_hot_cx (odd cell) (hot temp vs room)	7 for x = 1 6 for x ≠ 1	–0.781 for x = 1 –0.391 for x ≠ 1	–0.769 for x = 1 –0.378 for x ≠ 1	0.01221
GFC_hot_c(x+1)vs(x) (even cell vs odd cell)	5 for x = 1 3 for x ≠ 1	–0.195 for x = 1 –0.049 for x ≠ 1	0.183 for x = 1 0.037 for x ≠ 1	0.01221
GFC_Vbgtj1-2 (diagnostic voltage reference)[1]	8	−3.1250	3.1006	0.02441
GFC_i4-256 (current)	9	−25.0000	24.9023	0.09766
GFC_stack (stack voltage)	7	−3.1250	3.0762	0.04883

Table 15. Gain format*...continued*

Gain = 1 + DG (DG)	Representation: 2's complement (number of bits)	Min (%)	Max (%)	Resolution (%)
GCF_ANx_ratio (ANx ratio)	5	−1.5625	1.4648	0.09766
GCF_IcTemp (IC temperature)	4	−3.1250	2.7344	0.39063

[1] This gain compensation factor is relative to GCF_c1.

9.7 Coulomb counting

All conversions of ADC2 increment the internal coulomb counter, referred to as COULOMB_CNT, which represents the discrete integral of ADC2 samples, where the time index can only take positive integer values. COULOMB_CNT is copied to registers COULOMB_CNT1, COULOMB_CNT2. In addition to this, the MC33772C provides the number of accumulated samples in register CC_NB_SAMPLES, which represents the elapsed time expressed in integer units. The coulomb counter registers COULOMB_CNT1, COULOMB_CNT2 and CC_NB_SAMPLES are reset by writing the ADC_CFG[CC_RST] reset bit.

The registers CC_NB_SAMPLES/COULOMB_CNT1/COULOMB_CNT2 are updated if a write command has been done on one of these 3 registers (updated at next read) or if a read/write command has been done on another register (updated at next read). If the 3 registers are read in loop without any write or read command on other registers, their values are not updated.

In the event an overflow occurs in either COULOMB_CNT or CC_NB_SAMPLES, the CC_OVR_FLT bit is set and, when unmasked, the FAULT pin is activated. The coulomb count value is impacted by conversions performed during diagnosis of the current measurement chain.

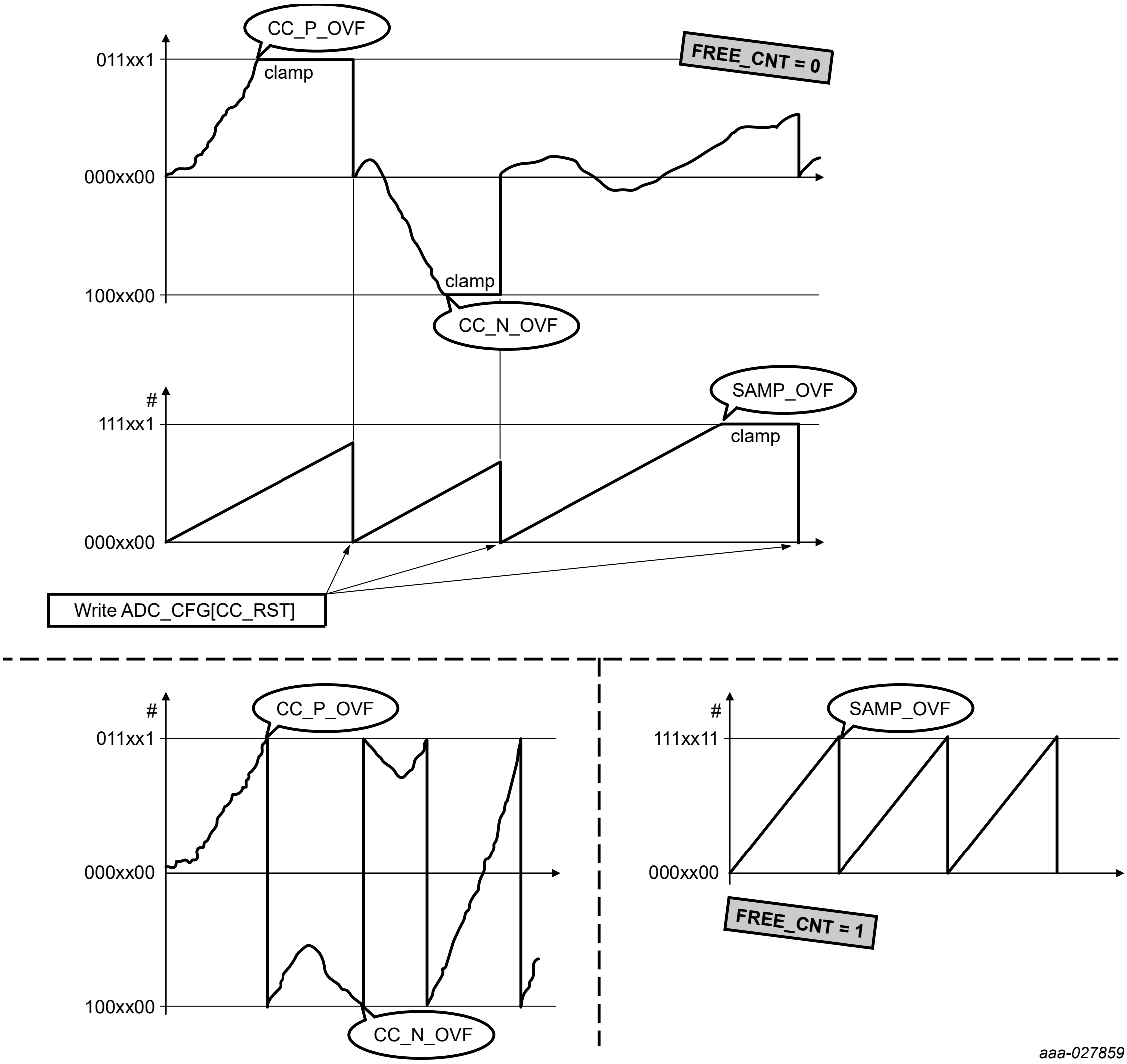


Figure 14. Coulomb counter different behaviors

The COULOMB_CNT is an integer whose associated resolution is V_{2RES}, therefore, COULOMB_CNT·V_{2RES} gives μV. If the shunt resistance R_{SHUNT} is expressed in μΩ, then COULOMB_CNT·V_{2RES} / R_{SHUNT} gives A.

The coulomb counting feature allows the pack controller to compute the average current. Value of R_{SHUNT} is only owned by the pack controller. By assuming two snapshots of the above mentioned registers are taken at two consecutive times T_{k-1} and T_k, the ratio $Iav_k = (ACC_k – ACC_{k-1}) / (N_k – N_{k-1})$ provides the average value of the current during the time interval $(T_k – T_{k-1})$, where ACC_k and ACC_{k-1} are the values of the quantity COULOMB_CNT·V_{2RES} / R_{SHUNT} respectively at times T_k and T_{k-1}, and N_k and N_{k-1} are the values of CC_NB_SAMPLES corresponding to the same two instants. To get an electric charge, the pack controller needs to multiply the ratio Iav_k by $(T_k – T_{k-1})$ to get an electric charge.

Reading one of the three user registers (COULOMB_CNT1, COULOMB_CNT2, CC_NB_SAMPLES) triggers the MC33772C to copy the content of the coulomb counter internal registers into these three user registers. The content of the coulomb counter user registers is updated only when an address different from $2D, $2E, and $2F is read, and then one or more of the registers (COULOMB_CNT1, COULOMB_CNT2, CC_NB_SAMPLES) are read again.

It is important to reset the entire coulomb counter status each time the type of input source is changed. In fact, the coulomb counter integrates not only the current signal, but also other possible diagnostic inputs.

If the bit ADC2_OFFSET_COMP[CC_RST_CFG] is set to logic 1, reading any coulomb counter register (from @ $2D to @ $2F) also resets the coulomb counter.

The coulomb counter can behave in two different ways: clamping mode (by setting ADC2_OFFSET_COMP[FREE_CNT] = 0) and rollover mode (by setting ADC2_OFFSET_COMP[FREE_CNT] = 1): see Figure 14.

Flags ADC2_OFFSET_COMP[CC_P_OVF] and ADC2_OFFSET_COMP[CC_N_OVF] respectively signal an occurred overflow or an occurred underflow in the coulomb counter accumulator; they can be reset to zero by writing a logic 0 in those bits.

The flag ADC2_OFFSET_COMP[SAMP_OVF] signals an occurred overflow of the number of samples. It can be reset to zero by writing a Logic 0 in it. Any kind of occurring overflow is reflected in the content of the FAULT3_STATUS[CC_OVR_FLT] bit as well.

If ADC2 is enabled (SYS_CFG1[I_MEAS_EN] = 1) AND cyclic measurement is active (SYS_CFG1[CYCLIC_TIMER] ≠ 0), the coulomb counter is calculated also in sleep mode. If so, each time the device is entering into Cyclic Wake-Up mode at the period equal of the cyclic timer configured according to SYS_CFG1[CYCLIC_TIMER], the current will be measured, with PGA gain set to 256, and integrated in the Coulomb Counter. The number of samples accumulated in the Coulomb Counter will also be incremented by 1.

If any fault condition occurs by these operations, depending on the fault and wake-up mask configuration, the device is awakened and the fault line is activated, including the case where the coulomb counter crosses the threshold TH_COULOMB_CNT, which is specific to Sleep mode and produces the setting of both ADC2_OFFSET_COMP[CC_OVT] and FAULT3_STATUS[CC_OVR_FLT] bits.

When the device transitions from Sleep mode to Normal mode, the coulomb counter is frozen until it is read and reset by the user, and the acquisition speed is turned from the configured one (by the cyclic timer SYS_CFG1[CYCLIC_TIMER]) to continuous.

TYPE A (free running mode with explicit reset):

CONFIGURATION instructions:

1. SYS_CFG1[IMEAS_EN] = 1; // Enable the current measurement
2. ADC2_OFFSET_COMP[FREE_CNT] = 1; // Select the free running mode
3. ADC2_OFFSET_COMP[CC_RST_CFG] = 0; // Do not reset to zero upon read

RESET instructions:

1. write ADC_CFG[CC_RST] = 1; // Reset to zero:
2. COULOMB_CNT = COULOMB_CNT_old = CC_NB_SAMPLES_old = Time = Time_old = 0; // Variables initialization

NORMAL USE instructions:

1. Time = get_abs_time(); // Get the absolute time
2. Read registers COULOMB_CNT1, COULOMB_CNT2 and CC_NB_SAMPLES;
3. COULOMB_CNT = (COULOMB_CNT1, COULOMB_CNT2); // Concatenate MSB and LSB
4. I_AVG = (COULOMB_CNT - COULOMB_CNT_old)/(CC_NB_SAMPLES -CC_NB_SAMPLES_old); // This is average current
5. DELTA_Q = I_AVG * (Time – Time_old); // This delta charge may be accumulated in a different variable
6. COULOMB_CNT_old = COULOMB_CNT;
7. CC_NB_SAMPLES_old = CC_NB_SAMPLES;
8. Time_old = Time;
9. Read any register different from COULOMB_CNT1, COULOMB_CNT2 and CC_NB_SAMPLES
10. Jump to step 1

TYPE B (free running mode with implicit reset):

CONFIGURATION instructions:

1. SYS_CFG1[IMEAS_EN] = 1; // Enable the current measurement
2. ADC2_OFFSET_COMP[FREE_CNT] = 1; // Select the free running mode
3. ADC2_OFFSET_COMP[CC_RST_CFG] = 1; // Reset to zero upon read

RESET instructions:

1. ADC_CFG[CC_RST] = 1; // Reset to zero
2. Time = Time_old = 0; // Variables initialization

NORMAL USE instructions:

1. Time = get_abs_time(); // Get the absolute time
2. Read registers COULOMB_CNT1, COULOMB_CNT2 and CC_NB_SAMPLES;
3. COULOMB_CNT = (COULOMB_CNT1, COULOMB_CNT2); // Concatenate MSB and LSB
4. I_AVG = COULOMB_CNT/CC_NB_SAMPLES; // This is average current
5. DELTA_Q = I_AVG *(Time-Time_old); // This delta charge may be accumulated in a different variable
6. Time_old = Time;
7. Read any register different from COULOMB_CNT1, COULOMB_CNT2 and CC_NB_SAMPLES
8. Jump to step 1

9.8 GPIOx port control and diagnostics

For user flexibility, the MC33772C has seven GPIO to support voltage measurements referenced to GND - typically coming from NTC based circuits used to extract temperature information, e.g. that of cells - or to drive external circuits. All GPIOs may be individually configured as digital inputs or output ports, wake-up inputs, convert trigger inputs, ratiometric analog inputs with reference to VCOM, or analog inputs with absolute measurements, as shown in Table 16. With the exception of the GPIO0, no external voltage must be applied on GPIOx pins when the device is off or in Sleep mode.

Table 16. GPIO port configurations

GPIO port	GPIO			ANx		ISENSE (diagnostic mode only)
	Standard GPIO	Wup and daisy chain	Convert trigger	Absolute	Ratiometric	
0	x	x	—	x	x	—
1	x	—	—	x	x	—
2	x	—	x	x	x	—
3	x	—	—	x	x	—
4	x	—	—	x	x	—
5	x	—	—	x	x	x
6	x	—	—	x	x	x

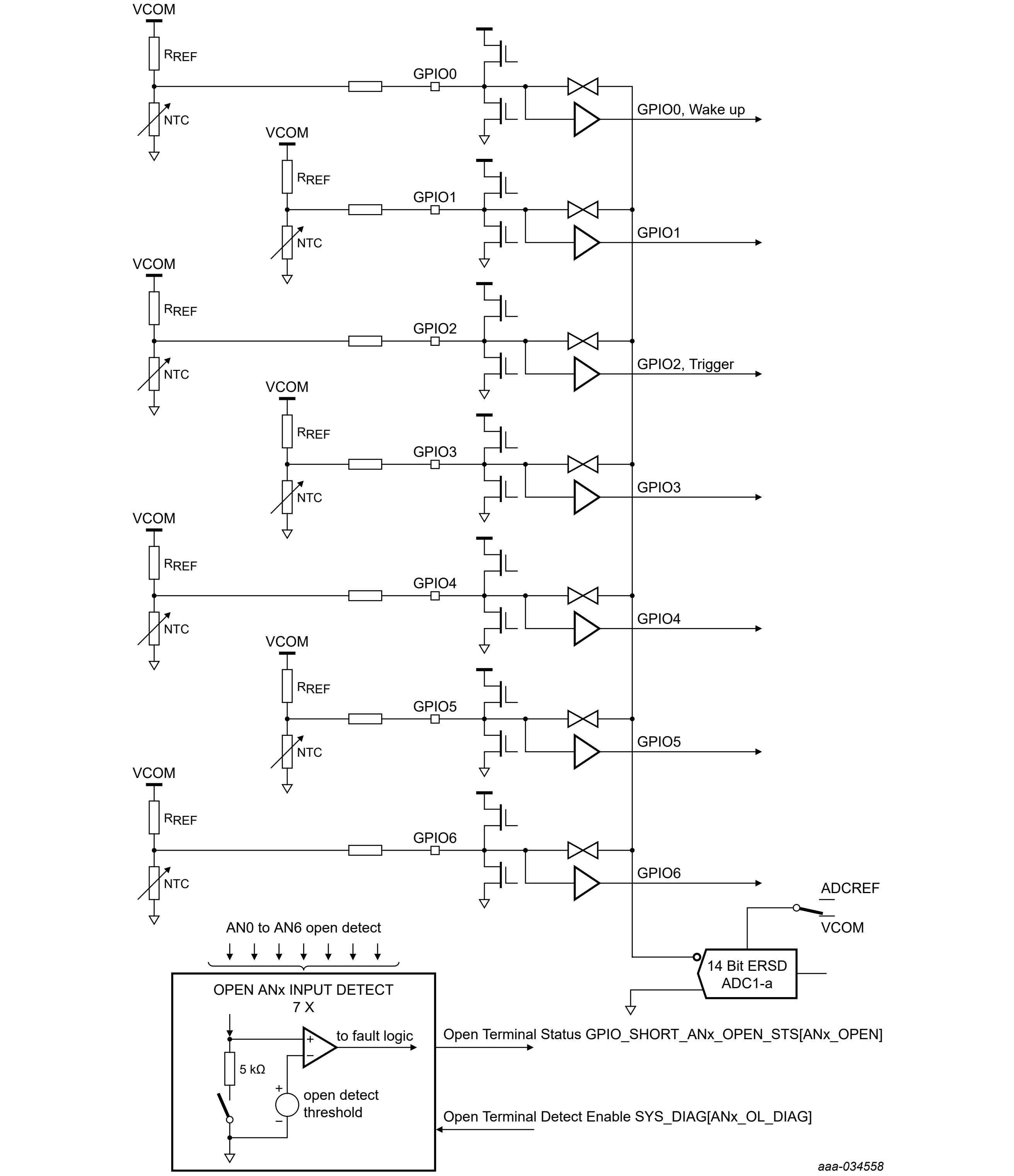


Figure 15. GPIO internal input structure

9.8.1 GPIOx used as digital I/O

Setting the GPIO_CFG1[GPIOx_CFG] bits to 10 or 11 configures the specific port as an input or output. Pins configured as outputs are driven high or low by writing to the GPIO_CFG2 register. Status of the ports, regardless of the digital configuration, is provided in the GPIO_STS register, which is a feedback of the actually commanded output.

Ports configured as GPIO outputs are diagnosed by the MC33772C. An output state GPIO_STS[GPIOx_ST], which is opposite of the commanded state GPIO_CFG2[GPIOx_DR], is considered to be shorted. Each short fault bit GPIO_SHORT_ANx_OPEN_STS[GPIOx_SH] associated with each GPIOx is OR wired to the FAULT2_STATUS[GPIO_SHORT_FLT] bit. Each GPIO_SHORT_ANx_OPEN_STS[GPIOx_SH] bit when unmasked activates the FAULT pin.

9.8.2 GPIO0 used as wake-up input or fault pin activation input

Setting the GPIO_CFG1[GPIO0_CFG] bits to 10 is used to configure a GPIO0 port as an input. To program GPIO0 as wake-up input, the user must set the GPIO_CFG2[GPIO0_WU] bit to logic 1. In this case, the device performs a wake-up on the rising or falling edge.

By setting the GPIO_CFG2[GPIO0_FLT_ACT] to logic 1, the GPIO0 port may be used to activate the FAULT pin in Normal, Sleep, and Diagnostic modes of operation. This feature allows the user to daisy chain the FAULT pin in high-voltage battery pack applications.

9.8.3 FAULT pin daisy chain operation

The FAULT pin may be programmed to provide the battery management system with a diagnostic feedback. Two behaviors are possible. One is based on logic levels: low level indicates normal condition, high level reveals a faulty condition. The other possibility is based on the heartbeat signal, a periodic signal generated by the IC to indicate normal operation, which provides a higher integrity level. The signal getting stuck to a constant level reveals a faulty condition.

Both modes can be activated in Normal mode, Sleep mode, and Diagnostic mode. The fault pin, carrying the diagnostic signal, is daisy chained to the next lower MC33772C GPIO0 port. Each MC33772C device is programmed to pass the heartbeat through to the neighboring device in the system. In this configuration, any fault that the MC33772C can automatically detect may activate the FAULT line.

To configure the MC33772C for daisy chain fault output:

1. Set GPIO0 as an input GPIO0_CFG = 10.
2. Disable wake-up on GPIO0 with GPIO0_WU = 0.
3. Set GPIO0 to propagate signal to FAULT pin with GPIO_CFG2[GPIO0_FLT_ACT] = 1.

To use the MC33772C heartbeat feature, the user must write a 1 in the SYS_CFG1[FAULT_WAVE] bit. The signaling square wave has constant on time, whereas the desired off time may be selected by writing a proper value in the SYS_CFG1[WAVE_DC_BITx] configuration field.

The usage of the fault pin is essential if the IC uses SPI communication and must provide some monitoring functionality in Sleep mode. In such use case the fault line is the only means to alert the system controller about an occurred fault, while in TPL mode, even if the IC is sleeping, it has the chance to send a wake-up signal through the bus. The fault line usage is optional in Normal and Diagnostic modes, as well as in Sleep mode and TPL configuration.

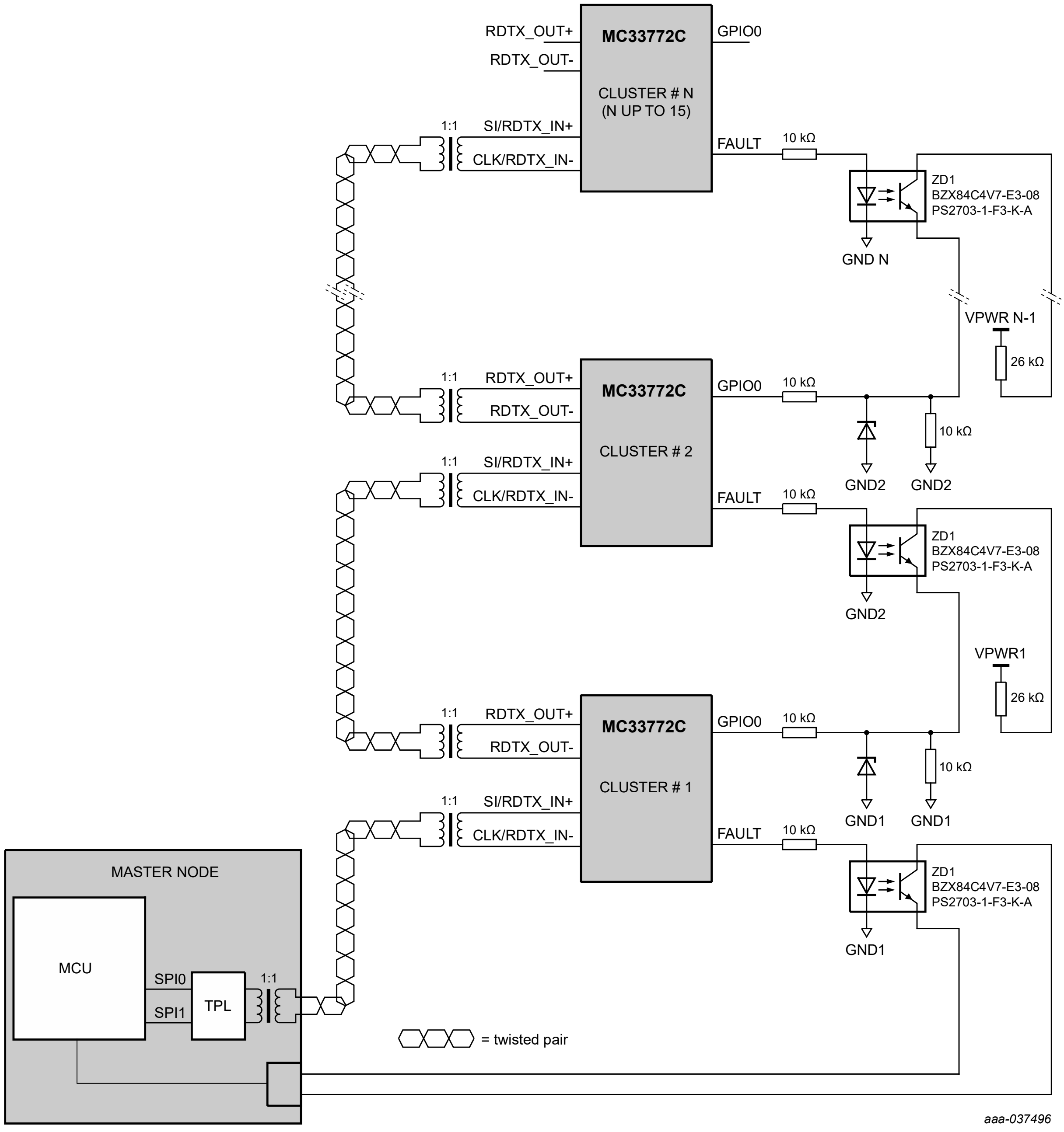


Figure 16. Heartbeat daisy chain

9.8.4 GPIO2 used as ADC trigger

The MC33772C provides a convenient method to trigger an ADC conversion from an external digital source. To use GPIO2 as an ADC trigger, configure the port as a digital input through the setting GPIO_CFG1[GPIO2_CFG] = 10 and enable the trigger through the setting GPIO_CFG2[GPIO2_SOC] = 1. With the port configured, positive edge events on GPIO_CFG2[GPIO2_SOC] triggers a start of conversion sequence.

With a GPIO2 trigger, the converter operates as programmed in the ADC_CFG[SOC] bit. The GPIO2 convert trigger feature is not available in Sleep mode.

9.8.5 GPIOx used as analog

Setting the GPIO_CFG1[GPIOx_CFG] bits to 00 or 01 configures the specific port as an analog ratiometric input (for conversion with ADC1-A using VCOM as reference voltage) or single ended input (for absolute measurement, which means using ADC1-A with its internal voltage reference in place of VCOM). GPIOs configured as analog inputs are usually used for temperature measurement. The MC33772C may be programmed to detect overtemperature and undertemperature.

To detect overtemperature and undertemperature, the generated digital value is compared to an individually programmed threshold in the TH_ANx_OT and TH_ANx_UT registers. ADC1-A results on any temperature measurement input that exceed the threshold activate the FAULT1_STATUS[AN_OT_FLT,AN_UT_FLT] bit. The conversion results for the analog inputs are available in MEAS_ANx register for the pack controller to read. GPIOs configured as single ended analog inputs can also be used to monitor voltage through external voltage divider.

9.8.6 GPIO5, GPIO6 used as ISENSE

To use GPIO5 and GPIO6 as inputs to the current sense PGA, the MC33772C must be in Diagnostic mode. As a secondary method of measuring current for functional verification, the user may connect input ports 5 and 6 as inputs to the positive and negative inputs of the PGA by setting the SYS_DIAG[I_MUX] bits to 01. This way, GPIO5 plays the role of ISENSE+ and GPIO6 plays the role of ISENSE–.

Customers using GPIO5 and GPIO6 as a secondary current measurement in diagnostic mode must command GPIO5 and GPIO6 to digital inputs by setting GPIO_CFG1[GPIO5_CFG] = 10 and GPIO_CFG1[GPIO6_CFG] = 10.

9.9 Cell balance control

The MC33772C features fully protected integrated cell balancing drivers with fault diagnostics. The cell balancing feature is active in Normal, Sleep and Diagnostic modes. The MC33772C contains registers to control and monitor cell balance drivers and cell balance fault status.

The SYS_CFG1 register contains the CB_DRVEN bit. The CB_DRVEN bit must be enabled for any of the drivers to be activated. All drivers are disabled when CB_DRVEN bit is logic 0. For cell balance drivers to be active, both the SYS_CFG1[CB_DRVEN] and the CBx_CFG[CB_EN] bits must be set to logic 1.

The individual cell balance timer is set through the CBx_CFG[CB_TIMER]. Timing parameters can be found in the register map of this specification. Each time the cell balance CBx_CFG[CB_TIMER] bit is written by the MCU controller, the MC33772C initiates the cell balance timer. It is important to explicitly mention, each time the CB_DRVEN bit is set to logic 0, then cell balancing timers get reset to 0 (the CBx_CFG[CB_TIMER] bits are unchanged) and all cell balancing MOSFETs are turned off. Before the CB_DRVEN bit is set again to logic 1, all CBx_CFG registers need to be configured again. Otherwise, a cell balancing sequence will be started with the previous settings.

The SYS_CFG1 register contains the CB_MANUAL_PAUSE bit, which, if set to logic 1, instructs the MC33772C to disable the cell balance switches. When the CB_MANUAL_PAUSE bit is set again to logic 0, the cell balance switches are restored according to the programming. However, the cell balance timers are not frozen during a manual pause. The contents of CBx_CFG[CB_TIMER] and ADC2_OFFSET_COMP[ALLCBOFF_ON_SHORT] bits must not be changed while balancing.

9.10 Internal IC temperature

Internal temperature measurement is completed automatically during each ADC conversion sequence. The MEAS_IC_TEMP register containing the IC temperature measurement may be read at any time by the pack controller. Resolution of MEAS_IC_TEMP is 32 mK/LSB.

9.11 Internal temperature fault

In addition to the digital temperature measurement register, the MC33772C is equipped with a silicon overtemperature Thermal ShutDown (TSD). In the event the silicon thermal shutdown is activated in Normal mode, the MC33772C halts all monitoring operations and enters a low-power state with the FAULT pin activated. When the die temperature returns to normal, the MC33772C resumes operation in Init mode.

In the event of an internal TSD:

1. Conversion sequence is aborted and the MC33772C stops converting
2. The FAULT2_STATUS[IC_TSD_FLT] bit is set to logic 1, implying a FAULT pin activation.
3. VCOM, VANA and VPRE are in shut down, communication gets blocked
4. All cell balance switches are disabled, all IC information except the FAULT2_STATUS[IC_TSD_FLT] bit is cleared and CB_DRVEN is cleared

Overtemperature TSD events are also detected while the MC33772C is in Sleep mode during cyclic measurements. TSD events detected during the Sleep mode cyclic measurement force the MC33772C to set the IC_TSD_FLT bit and activate the FAULT pin while remaining in Sleep mode.

When the die temperature returns to a normal level, as the IC returns in Init mode, the user shall provide the device with an address and proper parameters again.

9.12 Storage of parameters in an optional EEPROM

NXP provides parts with optimal calibration values, stored in a Read Only Memory called *fuses cell array*. It is typically neither necessary nor advised to change the standard values. Nevertheless, sometimes this might be required. An example is adjusting the gain calibration of the current channel to take into account the behavior of the external shunt resistor, due to the temperature coefficient and individual resistance deviation from the nominal value.

New calibration values may be determined in Normal mode and then stored:

- either in an external EEPROM (keeping content in case of power-down or reset event)
- or in the internal R/W memory, which is referred to as *mirror memory*. In this case, they are active until next power-down or reset event

Each time the part experiences a power-up or reset event, an initialization process (transparent to the user) takes place like hereafter:

- the mirror memory is first uploaded with the value of the *fuses cell array*
- if an EEPROM is recognized, this mirror memory gets automatically reloaded with the content of the EEPROM (overwriting the previous values). Else, the mirror memory is not modified
- the content of the mirror memory is released and propagated to the applicative part of the chip, protected by an ECC (Error Correction Code)

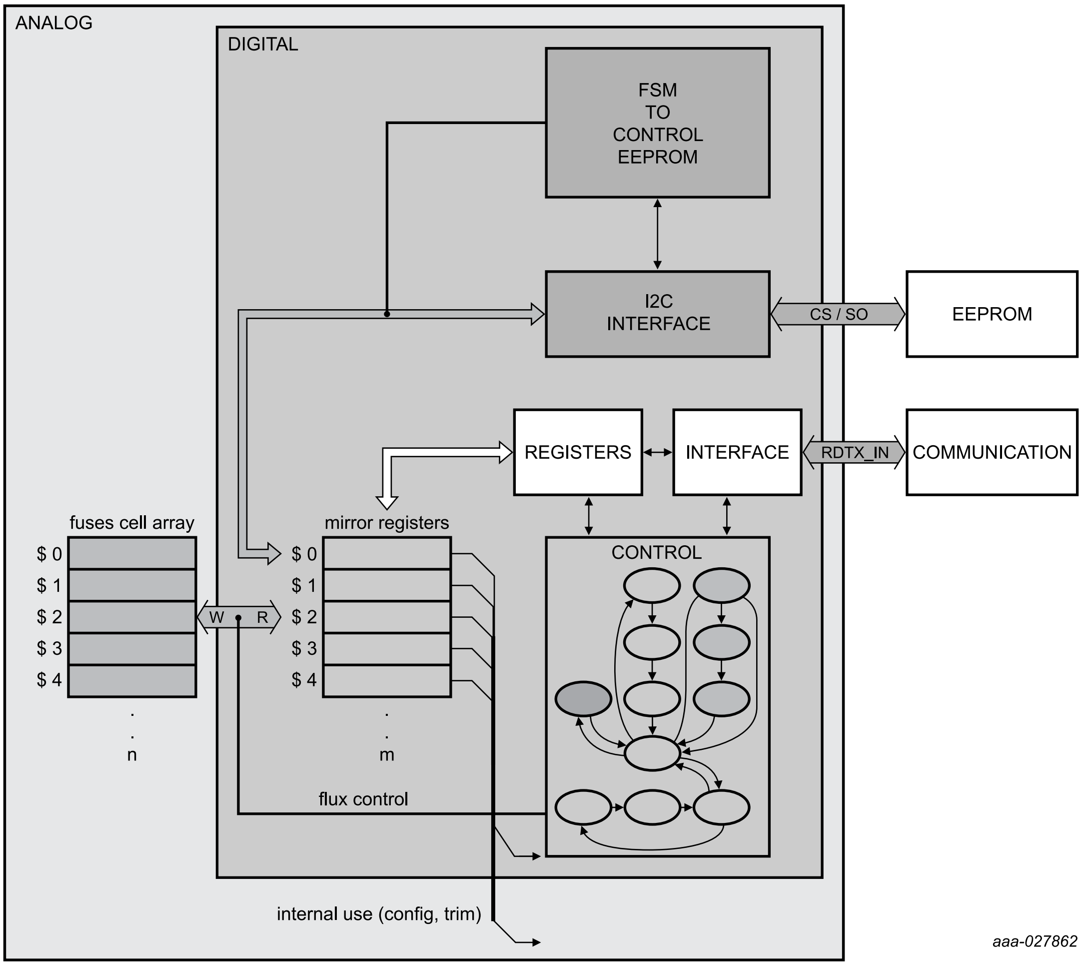


Figure 17. Memories

Because the EEPROM content is expected to overwrite the mirror memory, the space of EEPROM-addresses and the space of mirror-addresses correlate to each other. Mirror data are organized in 16-bit words, while the data of the EEPROM have been thought as bytes. As at EEPROM-address $00 there is the key value, the first calibration byte of the EEPROM must have EEPROM-address $01 and corresponds to the most significant byte of the mirror word having mirror-address $00. The second calibration byte of the EEPROM must have EEPROM-address $02 and corresponds to the least significant byte of the mirror word still having mirror-address $00, and so on.

9.12.1 Error Correction Code (ECC)

The calibration values are protected with some ECC bits, which are programmed in the *fuses cell array*. Like the calibration values, these ECC bits are loaded the same way in the mirror memory during the initialization process, to be used as a protection of the calibration data.

In case of a single error, the problem is automatically corrected, and the user is warned by the bit FUSE_MIRROR_CNTL[SEC_ERR_FLT]. In case of a double error, the problem can only be detected, and the fault flag FAULT2_STATUS[DED_ERR_FLT] is set.

If the user customizes its own calibration data, some new ECC bits must be evaluated. There are two ways for the user to evaluate by its own the new ECC bits.

1. There is a special calculation sheet the customer has to request from NXP. This sheet contains the correct values for DED_ENCODE2 and DED_ENCODE1 information, that is, ECC words used in the MC33772C to detect a single error in the data and to correct it
2. Writing the SYS_CFG2[HAMM_ENCOD] bit to logic 1, in which case the DED Hamming decoders generate the redundancy bits in DED_ENCODE1 and DED_ENCODE2 registers. See Table 84 and Table 85. However, in the normal usage, the SYS_CFG2[HAMM_ENCOD] bit has to be set at logic 0. For safety reasons, it is recommended the value of such bit is periodically checked to be at logic 0. If the bit is not at logic 0, then it must be written at logic 0 again

Once evaluated, these new ECC bits must be stored in the appropriate location:

- In the mirror memory if the customization is done there
- In the EEPROM, if the new calibration is stored there (will be downloaded at next power-up)
- In both cases, at address $0E and $0F (or EEPROM equivalent) of the fuse bank. See Table 89

9.12.2 Mirror memory

As described previously, the mirror memory can be accessed, partially in Read/Write mode, totally in Read-Only mode. This, by using the FUSE_MIRROR_DATA and FUSE_MIRROR_CNTL general registers (see Table 86 and Table 87).

The former contains the value of the data to be written into the mirror memory or to be read from it (FMR_DATA). The latter contains the address to access (FMR_ADDR) and some control fields (FSTM and FST).

Note: *FUSE_MIRROR_CNTL[FM_ADDR] enables to access addresses from $00 to $0F in Read/Write mode and addresses from $10 to $12 in Read-Only mode. See Table 89.*

To manage the mirror memory, the FSM of Figure 18 must be used.

Meaning of the states:

- To_Automatic_Read_S: transient state for slightly delaying the automatic read, after POR
- Automatic_Read_S: in this state the entire bank of fuses is automatically transferred from fuses cell array to the mirror memory
- Low_Power_S: low power state; it must be the initial and final state of a sequence of write operations. This is the state where the mechanism idles after an automatic read
- Enable_SPI_Write_S: state allows writing into the mirror memory

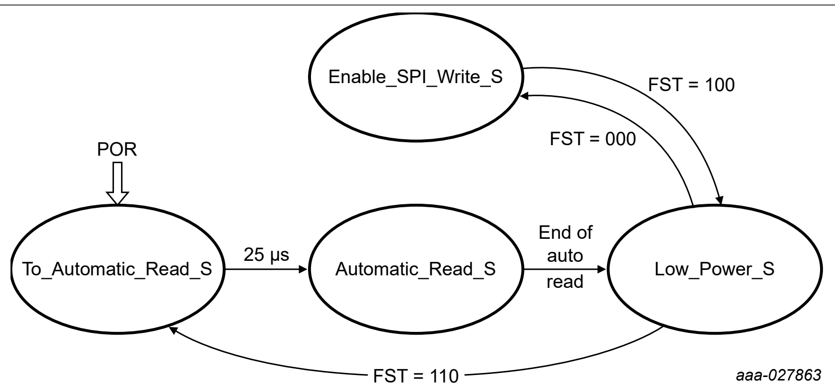


Figure 18. Mirror memory control

The read sequence may be useful, for example when the user wants to read the traceability information (serial number) contained in some specific words of the mirror memory. See Table 89.

Table 17. Sequence of read operations

Type of command	FSTM	FST	FMR_ADDR	FUSE_MIRROR_DATA
FUSE_MIRROR_CNTL[FMR_ADDR] set	0	000	00000	X
FUSE_MIRROR_DATA	X	X	X	data read at addr $0
FUSE_MIRROR_CNTL[FMR_ADDR] set	0	000	00001	X
FUSE_MIRROR_DATA	X	X	X	data read at addr $1
FUSE_MIRROR_CNTL[FMR_ADDR] set	0	000	00010	X
FUSE_MIRROR_DATA read	X	X	X	data read at addr $2

Table 18. Sequence of write operations

Type of command	FSTM	FST	FMR_ADDR	FUSE_MIRROR_DATA
FUSE_MIRROR_CNTL to enable writing	1	000	00000	X
FUSE_MIRROR_CNTL[FMR_ADDR] at $0	1	000	00000	X
FUSE_MIRROR_DATA	X	X	X	Data to be written at addr $0
FUSE_MIRROR_CNTL[FMR_ADDR] at $1	1	000	00001	X
FUSE_MIRROR_DATA	X	X	X	Data to be written at addr $1
FUSE_MIRROR_CNTL[FMR_ADDR] at $2	1	000	00010	X
FUSE_MIRROR_DATA	X	X	X	Data to be written at addr $2
FUSE_MIRROR_CNTL to low power	1	100	X	X

9.12.3 Optional EEPROM

Through the I2C interface, it is possible to link the MC33772C to an EEPROM, typically to store a customized configuration of calibration (user's final test and assembly). However, nothing prevents to use it as a generic information storage. But in all cases, the first portion of the EEPROM has to be reserved to the copy of all gains, even if this is identical to the content of the fuse cell array.

If connected, the EEPROM is automatically recognized, provided the address $00 of the EEPROM contains the proper one-byte key value, namely $CB hex.

Like for the mirror memory, the EEPROM is accessible following an indirect addressing, through the EEPROM_CTRL register. To program the EEPROM, the address and the data must be provided respectively in EEPROM_CTRL[EEPROM_ADD] and EEPROM_CTRL[DATA_TO_WRITE] fields, with the EEPROM_CTRL[RW] bit set to logic 0. The user must simply send the write command with the EEPROM address and data to be written, and set the write bit to logic 0. The MC33772C automatically writes the data to the given EEPROM address. To read data from the EEPROM, the user has to first write to the EEPROM_CTRL register, providing the address in EEPROM_CTRL[EEPROM_ADD] field, with the EEPROM_CTRL[RW] bit set to logic 1, then read in the same register to get the data in EEPROM_CTRL[READ_DATA] field.

10 Communication

The MC33772C is designed to support Serial Peripheral Interface (SPI) or Transformer Physical Layer (TPL) communication.

SPI communication uses the standard CSB to select the MC33772C and clocks data in and out using SCLK, SI, and SO. Using SPI to communicate to the MC33772C provides system isolation when used in conjunction with galvanic isolators. Serial communication is enabled using the SPI_COM_EN pin. To select SPI communication, the SPI_COM_EN pin must be terminated to the VCOM supply. Terminating the SPI_COM_EN pin to CGND pin selects TPL communication. Systems using only SPI communication to the MC33772C may leave RDTX_OUT+ and RDTX_OUT– unterminated or may short them to ground.

During initialization, each MC33772C device is assigned a specific address by the MCU by writing a non-zero value to INIT[CID] bit field. Only the MC33772C with the correct address acts upon and responds to the request from MCU. After initialization, the MCU may communicate globally to all slave devices by using a global command. No response is generated when a global command is received by each slave device in the chain.

Note: *The MC33772C supports only one communication method at a time and is determined by the state of SPI_COM_EN pin. Changing the state of the SPI_COM_EN pin after POR and VCOM is in regulation is considered a communication fault, and sets the COM_LOSS_FLT bit. The MC33772C remains in same configuration determined at POR.*

10.1 SPI communication

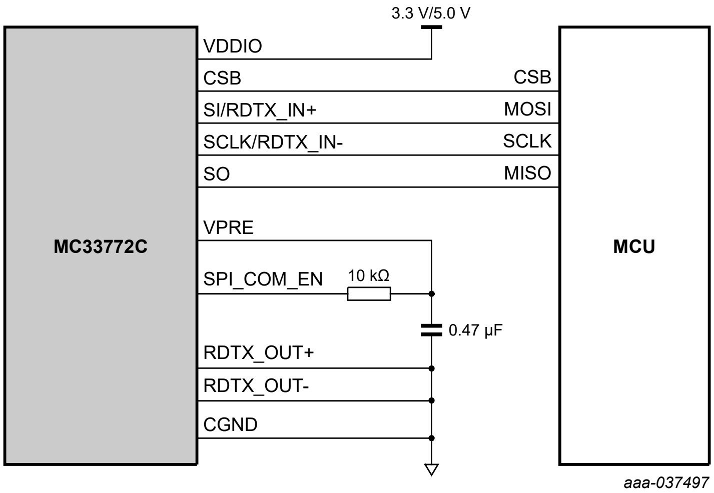


Figure 19. SPI interface termination

Note: *Supply input VDDIO accepts 3.3 V or 5.0 V to manage SPI and I2C interfaces.*

The MC33772C SPI interface is a standard SPI interface with a chip select (CSB), clock (SCLK), master in slave out (MISO), and master out slave in (MOSI). The SI/SO shifting of the data follows a first-in-first-out method, with both input and output words transferring the most significant bit (MSB) first. All SPI communication to the MC33772C is controlled by the microcontroller.

One 48-bit message frame for previously requested data is retrieved through serial out for each current serial in message sent by the MCU. For message integrity and communication robustness, each SPI transmit message consists of nine bit fields with a total of 48 bits message frame. The nine transmit fields are defined as following:

1. Register data (16 bits)
2. Request/Response (1 bit), always at 1 in the response
3. Register address (7 bits)
4. Reserved (2 bits)
5. Cluster ID (6 bits)
6. Message counter (4 bits)
7. Reserved (2 bits)
8. Command (2 bits)
9. Cyclic redundancy check (8 bits)

Messages having less or more than 48 bits, incorrect CRC, or incorrect SCLK phase are disregarded. Communication faults set the COM_ERR_FLT fault bit in the FAULT1_STATUS register and increments the COM_STATUS[COM_ERR_COUNT] register.

Note: *It is required that the SCLK input is low before the falling edge of CSB (SCLK phase).*

Table 19. SPI command format

Register data	Request/ Response	Register address	Reserved	Device address (Cluster ID)	Message counter	Reserved	Command	CRC
Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]

Information is transferred to and from the MC33772C through the read and write commands. After a power-up (POR) or RESET (pin) or SYS_CFG1[SOFT_RST], the MC33772C device only responds to the cluster ID of 00 0000b. The user must change the cluster ID of the device by writing a new cluster ID into register INIT[CID]. Subsequent read/write command must use the new cluster ID to communicate to the device. Whatever the type of transmitted message, the master has to write a logic 0 in the Request/Response bit. Any message transmitted by the user with Request/Response bit set to 1 or with wrong CID is treated as Invalid request by MC33772C.

Notes:

- *In SPI communication, global write commands are not allowed and the MC33772C responds with all bit field set to zero except message counter and correct CRC, in the subsequent message frame*
- *In SPI communication, the MC33772C responds with all bit filed set to zero except message counter and correct CRC to an invalid request from MCU*
- *In SPI communication, the MC33772C responds with all bit filed set to zero except message counter and the correct CRC to the very first MC33772C / MCU message frame*

The response message sent by MC33772C to MCU is similar to the receive message and includes the 4-bit message counter. The Message counter is a local counter to MC33772C. It is increased by one for each new response transmitted by MC33772C, this applies also to auto read generated by MC33772C for write and NOP commands. It is recommended that the MCU compares the message counter value of two consecutive responses transmitted by MC33772C, if the values are same then MCU shall treat the messages as error.

1. Register data (16 bits)
2. Request/Response (1 bit)
3. Register address (7 bits)
4. Reserved (2 bits)
5. Cluster ID (6 bits)
6. Message counter (4 bits)
7. Reserved (2 bits)
8. Command (2 bits)
9. Cyclic redundancy check (8 bit)

Table 20. SPI response format

Register data	Request/ Response	Register address	Reserved	Device address (Cluster ID)	Message counter	Reserved	Command	CRC
Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]

To initiate communication, the MCU transitions CSB from high to low. The data from the MCU is sent with the most significant bit first. The SI data is latched by the device on the falling edge of SCLK. Data on SO is changed on the rising edge of SCLK and read by MCU on the falling edge of SCLK. The SO response message is dependent on the previous command.

Falling edge of CSB initiates the following:

1. Enables the SI Input
2. Enables the SO output driver

Rising edge of CSB initiates the following operation:

1. Disables the SO driver (high-impedance)
2. Activates the received 48-bit command word allowing the MC33772C to act upon the new command

Notes:

- *The MC33772C responds to a NO_OPERATION command with a NO_OPERATION response (with increased message counter value) in the subsequent response*
- *After initialization, when writing to a register, the MC33772C responds with an auto read of the register which was written in the subsequent write request*
- *The MC33772C does not execute any command if the Request/Response bit is equal to logic 1*

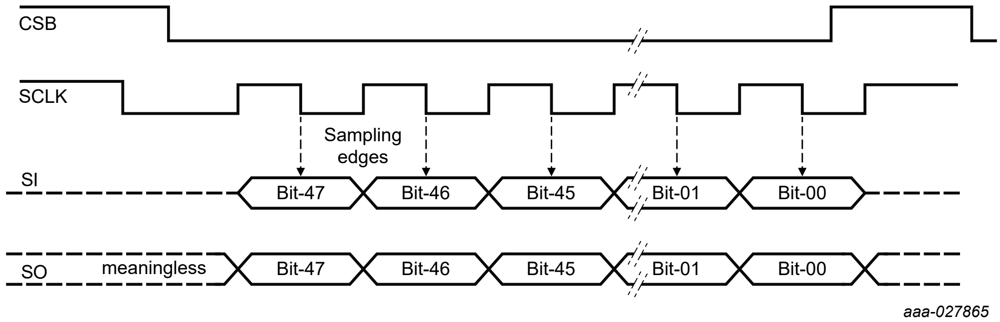


Figure 20. SPI transmission

10.2 TPL communication

High speed differential isolated communication is achieved through the use of transformer or capacitive isolation. Terminating the SPI_COM_EN pin to the CGND pin selects transformer communication. For transformer communication (TPL), an MC33664 IC is required between the MC33772C IC and the MCU, as shown in Figure 48

For TPL communication, it is recommended that the device is terminated as shown in Figure 48. Component values are given in Section 13.2.

The MC33772C IC is equipped with a bi-directional transceivers for upstream and downstream communication. The bi-directional transceiver is implemented to support up to 63 nodes in one daisy chain (CID = 00 0000b is reserved for network initialization). The message received by the receiver on one port of MC33772C is retransmitted by the transmitter of the opposite port of MC33772C. This ensures that the message is not attenuated as it propagates through the daisy chain. Each node in the daisy chain adds a delay of t_{port_delay} for forwarding messages in the daisy chain.

In TPL communication, the CSB pin may be used as a wake-up input. During Sleep mode, an edge transition of the CSB initiates the wake-up function. Alternatively, the CSB pin may be shorted to ground or software masked to prevent undesired wake-up events.

Communication between the pack controller and the MC33772C is half duplex communication with transformer isolation. Transformer physical layer in the pack controller creates a pulse phase modulated signal transmitted to the bus through the transformer. The MC33772C physical layer is equipped with a segment-based transmitter, which is used as a terminating resistor (internally) during the receive mode. The default value of terminating resistance is set to 120 Ω for impedance matching and network stability. In TPL communication, the MC33772C IC is always electrically connected to its neighbouring MC33772C ICs in a daisy chain. However, by using INIT[BUS_FW] the neighboring MC33772C can be disconnected digitally. This can be configured using INIT register.

10.2.1 TPL Encoding

The transformer physical layer (TPL) uses pulse encoded symbols for communication. The three signal pulses used for encoding positive (P,black), negative (N, red) and zero (M, black) are shown in Figure 21 .

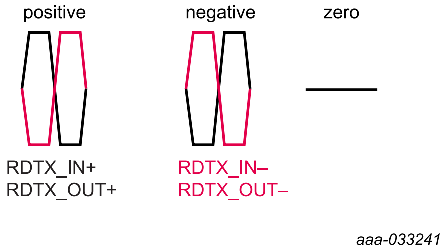


Figure 21. TPL Pulses

Start Of Message (SOM) and End Of Message (EOM) symbols are generated by the transformer driver and always occur at the start and end of the communication message. The SOM symbol and EOM symbol each contain two complete signal pulses. The SOM symbol produces a double pulse with a logic 1 phase. EOM produces a double pulse with logic 0 phase. Data pulses are single period pulse waves that indicate logic 1 or 0, based on the phase. The four symbols shown in Table 21 are used.

Table 21. TPL encoding

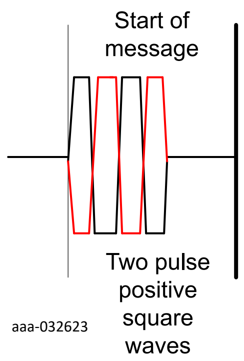
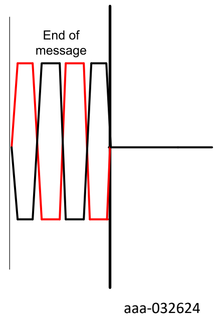
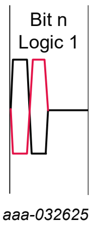
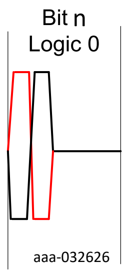
Symbols	Pulse modulation	Description
Start Of Message (SOM)	 **Figure 22. SOM**	Positive phase, double pulse (and plus pause)
End Of Message (EOM)	 **Figure 23. EOM**	Negative phase, double pulse

Table 21. TPL encoding *...continued*

Symbols	Pulse modulation	Description
Logic 1	 **Figure 24. Logic 1**	Positive phase, single pulse (and plus pause)
Logic 0	 **Figure 25. Logic 0**	Negative phase, single pulse (and plus pause)

10.2.2 Command message bit order

Same as in Section 10.1.

10.2.3 Response message bit order

Same as in Section 10.1.

10.2.4 Transformer communication format

Command and response frames are exchanged primarily between a single master and any single slave. One exception is the use of a global command, which can be transmitted from one master to multiple slaves, but includes no slave response. The purpose of the command and response transactions are to read and write to registers within the slave register map.

The command and response communication structure provides all context information required for unambiguous single-exchange transactions for extended memory applications requiring safety critical and efficient memory access.

The message structures have predefined fixed bit length frames and defined timing between transfers. To transfer data efficiently from the slave, multiple response packets may be requested by the read command. The MC33772C defines a set of fields that constitute the command and response message structure.

Transformer message format is identical to the SPI format. Command message frames consist of nine fields containing exactly 48 bits. The response structure is similar to the SPI format.

After initialization, information is transferred to and from the MC33772C through the read and write commands. On Power Up or POR, the first MC33772C device in the chain responds to address 00 0000b[4] [5]. The user must program the first device with a new address by writing to the INIT[CID] register. Programming the device

4 A slave device at POR with INIT[CID] = 00 0000b responds only at the port it received the request.
5 A slave device with CID = 00 0000b does not forward messages.

with a new address allows the pack controller to communicate and initialize the next device in the daisy chain. Subsequent read/write commands to the next device must use the new address to communicate.

All write commands sent by the master must consist of a single frame. The slave device does not generate any response to a write command from master but only acts on it. Similarly, the slave device does not generate any response nor performs any operation after receiving a valid NOP message from the master.

Read commands sent by the master may generate a single response or multiple responses depending on the parameters set in the read request. The packet size and memory start location are identified in the read command sent by the master.

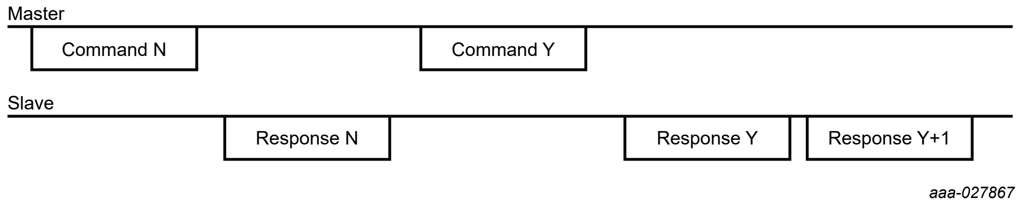


Figure 26. Bus traffic example

No response is generated by a slave MC33772C when a corrupted message is received. Confirmation that a global write command is received by the slave must be done by reading the register in which it was written.

In cases where a bus error occurs, due to induced noise or a bus fault, the slave detects bad data transfers. The MC33772C slave reacts to communication faults by setting the FAULT1_STATUS[COM_ERR_FLT] and incrementing the COM_STATUS[COM_ERR_COUNT] register.

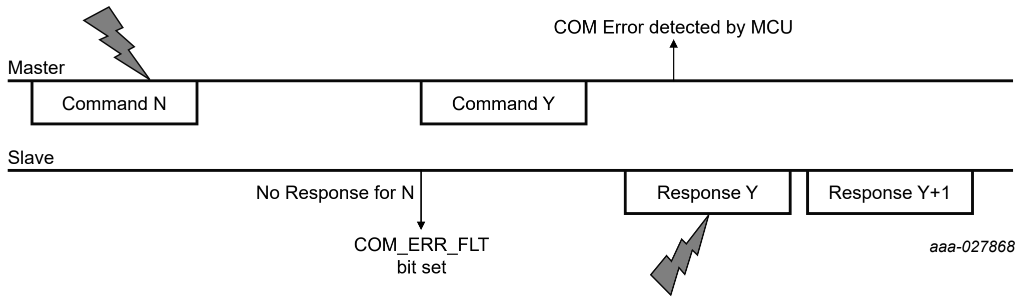


Figure 27. Bus traffic with receive error and recovery

All valid read commands sent to an individual slave provide a response. In the event a slave does not respond to a read request message, the master must assume the message was corrupted or lost. To recover from the event, the master must retransmit the message. Corrupted messages received by the master are detected through an incorrect CRC code. To recover, the master must request the data again.

10.2.5 Transformer communication timing

Command and response message frames are to be sent and received at 2.0 Mbit/s bit rate. The response to a first read request command is provided within t_{RES} of the end of the frame. However, two consecutive message responses transmitted by MC33772C IC for burst read request are separated by t_{TPL_TD} time as shown in Figure 28.

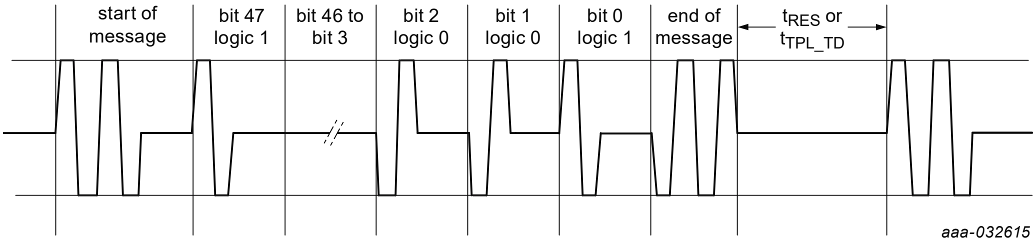


Figure 28. Transformer communication waveforms

Each sent and received message starts with Start Of Message (SOM) bit followed by a 48-bit message and ends with an End Of Message (EOM) bit.

10.2.6 Transformer communication wake-up

In TPL communication, the system wake-up can be triggered by either the MC33772C IC (wake-up due to internal event) or the pack controller (MCU). In both cases, a dedicated wake-up pulse sequence is used. The wake-up pulse sequence consists of two transmit messages of any length. The messages are separated by a delay time (t_{WAKE_DELAY}). Each message contains a SOM and EOM symbol.

10.2.6.1 MC33772C System wake-up

By default, the internal event wake-up capability of the MC33772C is disabled. When enabled and in the event the MC33772C detects a wake-up condition, the device initiates a wake-up pulse sequence on the bus to alert the pack controller. The MC33772C IC initiating the wake-up, due to an internal event, sends the wake-up sequence upstream and downstream in the daisy chain to ensure the wake-up message propagates along the entire chain to the pack controller. Each neighbouring MC33772C IC in daisy chain forwards the received wake-up sequence opposite to the direction where it received the wake-up sequence. In this process, all MC33772C devices in the daisy chain, along with the pack controller, are awoken. After the pack controller gets awoken; it is recommended the pack controller interrogate each MC33772C in the system to determine the source of the wake-up.

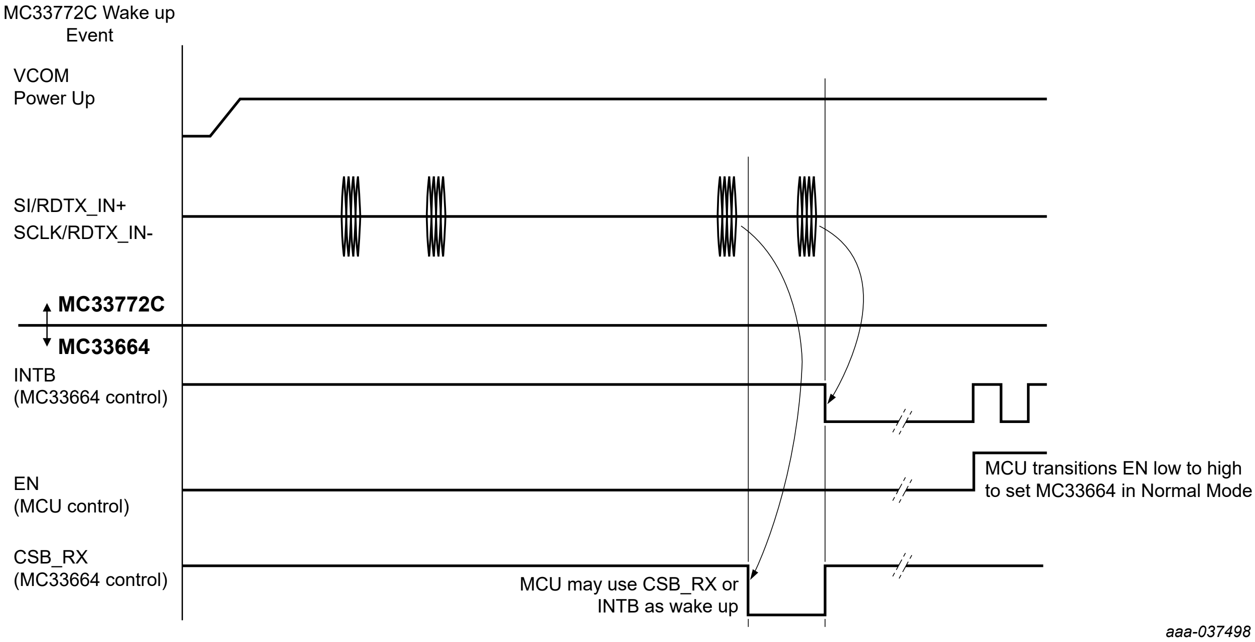


Figure 29. MC33772C system wake-up

Note: *The system wake-up performed by MC33772C IC in case of any internal event is disabled by default. This wake-up can be activated by writing to register WAKEUP_MASK1, WAKEUP_MASK2 and WAKEUP_MASK3.*

10.2.6.2 Pack controller system wake-up

The pack controller can also perform system wake-up by sending a wake-up sequence to the first MC33772C IC. The pack controller can use the CSB_TX pin of the MC33664 to generate SOM and EOM with correct timing.

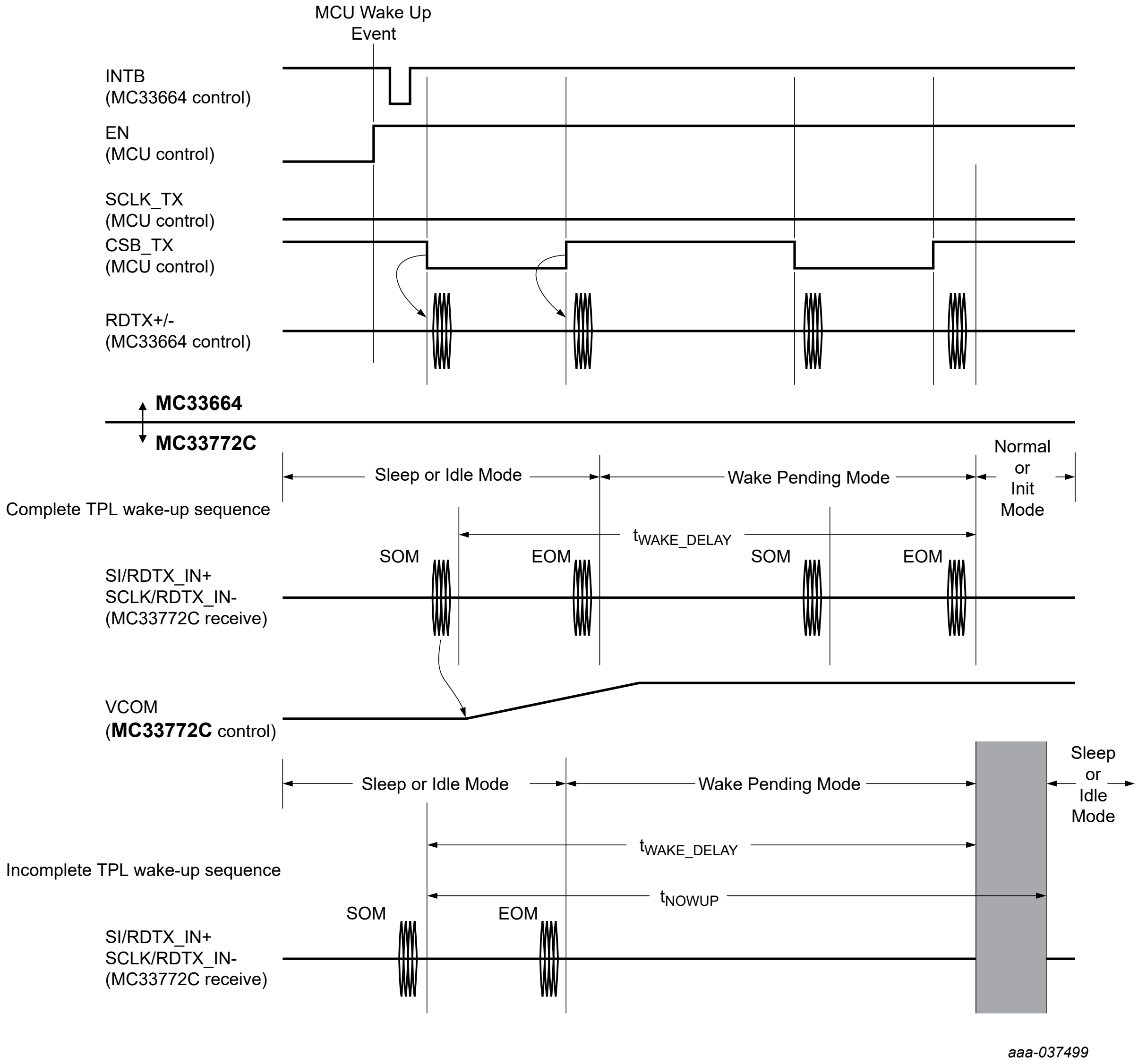


Figure 30. Pack controller system wake-up

If the device is in Sleep mode, each successive slave device awoken by the wake-up message on the bus, generates a new wake-up message for its neighbor. The message is to be transmitted in one direction only on the bus. The direction of transmission of the wake-up message on the bus is always at the opposite port of the received wake-up message. In the unlikely event of a collision, the message at the lower port (RDTX_IN) is given a higher priority than the message at the higher port (RDTX_OUT).

Note:

- *Any write message of any length can be used to generate both wake-up pulses and obtain a valid device wake-up*
- *The second wake-up message should be sent after a minimum time of tWAKE_DELAY(min) from the first SOM reception*
- *The device falls back to Sleep or Idle mode when an SOM followed by EOM is not received in tWAKE_DELAY(max)*
- *If the wake-up sequence is incomplete, then a new wake-up attempt can only be done after a tNOWUP delay (see Figure 30)*
- *The pack controller must wait for t_{WU_Wait} ms per node to communicate with the MC33772C ICs after sending the first wake-up message. For example, given that the MC33772C IC is enumerated and bus forwarding is enabled, with 10 nodes in a daisy chain the pack controller must wait 7.5 ms before communicating to MC33772C IC. The waiting time allows all the MC33772C ICs in the system to transition to Normal mode*
- *The pack controller must use only one master node to perform wake-up of devices*

10.3 CRC generation

The master and slaves calculate a CRC on the entire message using the processes detailed in this section.

The command and response CRC is fixed at 8 bits in length. The CRC is calculated using the polynomial $x^8 + x^5 + x^3 + x^2 + x + 1$ (identified by 97h – Koopman notation). To get the CRC engine into the correct state, a 11h must be clocked in before the message. This procedure corresponds to a seed value of 42h.

An example CRC encoding HW implementation is shown in Figure 31.

Note: *97h in Koopman notation corresponds to 2Fh in the MSB-first code notification.*

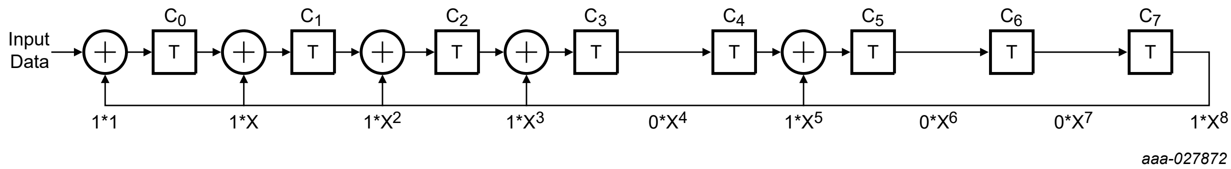


Figure 31. Command and response mode – example CRC encoder

The effect of the CRC encoding procedure is shown in the following table. The seed value is appended into the most significant bits of the shift register.

Table 22. Data preparation for CRC encoding

Seed	Register data	Request/ Response	Register address	Reserved	Cluster ID	Message counter	Reserved	Cmd
1111_1111	Bits [47:32]	Bit [31]	Bits [30:24]	Bits[23:22]	Bits[21:16]	Bits[15:12]	Bits[11:10]	Bits[9:8]

Seed…	…padded with the message to encode…	…padded with 8 zeros

1. Using a serial CRC calculation method, the transmitter rotates the seed and data into the least significant bits of the shift register
2. During the serial CRC calculation, the seed and the data bits are XOR compared with the polynomial data bits. When the MSB is logic 1, the comparison result is loaded in the register, otherwise the data bits are simply shifted. It must be noted the 48-bit message to be processed must have the bits corresponding to the CRC byte all equal to zero (00000000)
3. Once the CRC is calculated, it replaces the CRC byte initially set to all zeros and is transmitted

Following is the procedure for the CRC decoding:

1. The seed value is loaded into the most significant bits of the receive register
2. Using a serial CRC calculation method, the receiver rotates the received message and CRC into the least significant bits of the shift register in the order received (MSB first)
3. When the calculation on the last bit of the CRC is rotated into the shift register, the shift register contains the CRC check result:
   - If the shift register contains all zeros, the CRC is correct
   - If the shift register contains a value other than zero, the CRC is incorrect

CRC calculation examples:

Table 23. Command CRC calculation examples

Data 16 bit (Hex)	Request/Response bit and memory address, 8 bit (Hex)	Reserved (2 bits) and Cluster Id (6 bit), 8 bit (Hex)	Message counter, 4 bit (Hex)	Reserved (2 bits) and Command (2 bits), 4 bit (Hex)	CRC 8 bit (Hex)	Frame 48 bit (Hex)
0x0101	0x08	0x01	0x3	0x0	0x3C	0x01010801303C
0x0A0A	0x01	0x0A	0x9	0x1	0x84	0x0A0A010A9184
0x01C4	0x0F	0x02	0x1	0x2	0x26	0x01C40F021226
0x7257	0x01	0x05	0x7	0x3	0xC7	0x7257010573C7

Table 24. Response CRC calculation examples

Data 16 bit (Hex)	Request/Response bit and memory address, 8 bit (Hex)	Reserved (2 bits) and Cluster Id (6 bit), 8 bit (Hex)	Message counter 4 bit (Hex)	Reserved (2 bits) and Command (2 bits), 4 bit (Hex)	CRC 8 bit (Hex)	Frame 48 bit (Hex)
0x1101	0x89	0x01	0x3	0x0	0x26	0x110189013026
0x2002	0x89	0x05	0x9	0x0	0x7A	0x20028905907A
0x5103	0x89	0x0A	0x1	0x5	0x07	0x5103890A1507
0xFF04	0x89	0x06	0x7	0x2	0xA6	0xFF04890672A6

10.4 Commands

10.4.1 Read command and response

Read command is intended to be used for SPI and transformer interface. The read command is a local command used for retrieving data from the MC33772C device. The data field contains the number of data registers to be returned. Requesting data from registers greater than address $7F forces the device to loop the register counter back to register $00.

Table 25. Read command table

Command name	Register data		Request/ Response	Register address	Reserved	Device address (Cluster ID)	Message counter	Reserved	Command	CRC
	Bit[47:32]		Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Read command	XXXX XXXX X	NRT- 01 to 7F	0b	Register address	xxb	CID	xxxxb	xxb	01b	CRC

Table 26. Read response table

Command name	Register data	Request/ Response	Register address	Reserved	Device address (Cluster ID)	Message counter	Reserved	Command	CRC
	Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Read MsgCntr Response	Register Data	1b	Register address	00b	CID	MsgCntr	00b	01b	CRC

Table 27. Legend for read command, read response tables

Read command		Read response	
Bit[7:0]	= 8-bit CRC	Bit[7:0]	= 8-bit CRC
Bit[9:8]	= Command (01b)	Bit[9:8]	= Command field (01b)
Bit[11:10]	= Reserved (xxb)	Bit[11:10]	= Reserved (00b)
Bit[15:12]	= Message counter	Bit[15:12]	= Message counter
Bit[21:16]	= Device address (Cluster ID)	Bit[21:16]	= Device address (Cluster ID)
Bit[23:22]	= Reserved = X, don't care	Bit[23:22]	= Reserved (00b)
Bit[30:24]	= Register address	Bit[30:24]	= Register address
Bit[31]	= Request/Response = 0b (Request)	Bit[31]	= Request/Response = 1b (Response)
Bit[39:32]	= NRT, number of registers to transfer back. Max is $7F, loop back on address $00	Bit[47:32]	= Data at memory address
Bit[47:40]	= X, don’t care		

Notes:

- *The read command is a local command*
- *Requesting a read of a reserved register provides a $0000 data response*
- *Registers are read-only on devices that have not been initialized*
- *Requesting a number of NRT equal to 00 is the same as requesting 01*
- *The MsgCntr is a local counter of MC33772C IC. It is only increased by the node responding to MCU request. The node increases the value of MsgCntr by 1 with each new response transmitted by MC33772C. On saturation of this counter it restarts from 0000b*
- *The initial value of message counter is 0000b and first response transmitted by MC33772C has the message counter value set to 0000b*

10.4.2 Local write command

Unlike the read command, for which MC33772C responds with data, the write command does not generate any response. When the slave receives a valid local write command, the message is acted upon but no response is generated. Writing to read only registers does not allow the register content to be updated.

Table 28. Write command table

Command name	Register data	Request/ Response	Register address	Reserved	Device address (Cluster ID)	Message counter	Reserved	Command	CRC
	Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Write command	Register Data	0b	Register address	xxb	CID	xxxxb	xxb	10b	CRC

Table 29. Legend for write command and write response tables

Write command	
Bit[7:0]	= 8-bit CRC
Bit[9:8]	= Command (10b)
Bit[11:10]	= Reserved (xxb)
Bit[15:12]	= Message counter (xxxxb)
Bit[21:16]	= Device address (Cluster ID)
Bit[23:22]	= Reserved (xxb)
Bit[30:24]	= Register address
Bit[31]	= Request/Response = 0b
Bit[47:32]	= Register Data

Note: *Writing to reserved registers performs no operation and loads no data in the reserved register.*

10.4.3 Global write command

The global write command allows the transformer user to communicate to all devices on the bus at the same time. The global write command is useful to program all devices at the same time with values for fault threshold or to synchronize conversions for all devices on the bus. When a slave receives a valid global write command, the message is acted upon, but no response is generated.

Table 30. Global write command table

Command name	Register data	Request/ Response	Register address	Reserved	Device address (Cluster ID)	Message counter	Reserved	Command	CRC
	Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Global Write command	Register Data	0b	Register address	xxb	XX XXXXb (global)	MsgCntr	xxb	11b	CRC

Table 31. Legend for global write command table

Write command	
Bit[7:0]	= 8-bit CRC
Bit[9:8]	= Command field (11b)
Bit[11:10]	= Reserved (xxb)
Bit[15:12]	= Message counter = xxxxb (global)
Bit[21:16]	= Device address (Cluster ID) = xx xxxxb (global)
Bit[23:22]	= Reserved = xxb, Don't care
Bit[30:24]	= Register address
Bit[31]	= Request/Response = 0b
Bit[47:32]	= Register Data

10.4.4 No operation command

The No Operation (NOP) command allows the user to reset the communication time-out timer of the MC33772C. If the pack controller has no new request for MC33772C IC but does not want the MC33772C to reset (and lose its CID address), it can send a NOP command to the MC33772C IC. The NOP command does not trigger any response or operation from the MC33772C. Thus, the NOP command can be used by the pack controller like a ping to prevent the IC from resetting itself.

Table 32. No operation command table

Command name	Register data	Request/ Response	Register address	Reserved	Device address (Cluster ID)	Message counter	Reserved	Command	CRC
	Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
No operation (NOP) command	Register Data	0b	Register address	xxb	CID	xxxxb	xxb	00b	CRC

Table 33. Legend for no operation command and no operation response tables

Write command	
Bit[7:0]	= 8-bit CRC
Bit[9:8]	= Command field (00b)
Bit[11:10]	= Reserved (xxb)
Bit[15:12]	= Message counter
Bit[21:16]	= Device address (Cluster ID) = CID
Bit[23:22]	= Reserved = xxb, Don't care
Bit[30:24]	= Register address
Bit[31]	= Request/Response = 0b
Bit[47:32]	= Register Data

10.4.5 Command and response summary

Table 34. Command summary table

Command name	Register data	Request/ Response	Register address	Reserved	Device address (Cluster ID)	Message counter	Reserved	Command	CRC
	Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
NOP command	xxxx xxxxb	0b	xxx xxxxb	xxb	CID	XXXXb	XXb	00b	CRC
Read command	Number of registers	0b	Register address	xxb	CID	XXXXb	XXb	01b	CRC
Write command	Register Data	0b	Register address	xxb	CID	XXXXb	XXb	10b	CRC
Global write command	Register Data	0b	Register address	xxb	XX XXXXb	XXXXb	XXb	11b	CRC

If a device has its cluster ID (CID) equal to 00 0000b, then only its INIT register can be written by the pack controller. All the MC33772C devices have their First message from MCU controller writing to cluster ID 00 0000b. To perform a read/write operation of any register (other than INIT) of MC33772C IC, the MCU must first assign a unique address to each MC33772C device by writing to its INIT register with a suitable CID value. The process of assigning a unique CID address to each slave device by the pack controller is called *initialization*.

After initialization, each time the device receives a frame having the Request/Response bit equal to logic 1, this frame is not recognized, even though the address contained in the CID field is equal to the programmed one. In this condition, the device neither acts upon nor answers the command. This is a normal behavior, whose purpose is to avoid the device acting upon or responding to a frame generated by another slave device of the network.

Table 35. Response summary table

Command name	Register data	Request/ Response	Register address	Reserved	Device address (Cluster ID)	Message counter	Reserved	Command	CRC
	Bit[47:32]	Bit[31]	Bit[30:24]	Bit[23:22]	Bit[21:16]	Bit[15:12]	Bit[11:10]	Bit[9:8]	Bit[7:0]
Read response	Register Data	1b	Register address	00b	CID	MsgCntr	XXb	01b	CRC

10.5 I^2C communication interface

As an optional feature, the MC33772C has an integrated I^2C communication link to an external local EEPROM, which may be used to store calibration parameters defined by the user. If the EEPROM is not used, then the SCL and SDA pins must be left open. When this occurs, the FAULT1_STATUS[I2C_ERR_FLT] bit is automatically updated to logic 1. The automatic update happens even if an error bit is masked. If no EEPROM is mounted, the pack controller has to ignore the content of FAULT1_STATUS[I2C_ERR_FLT].

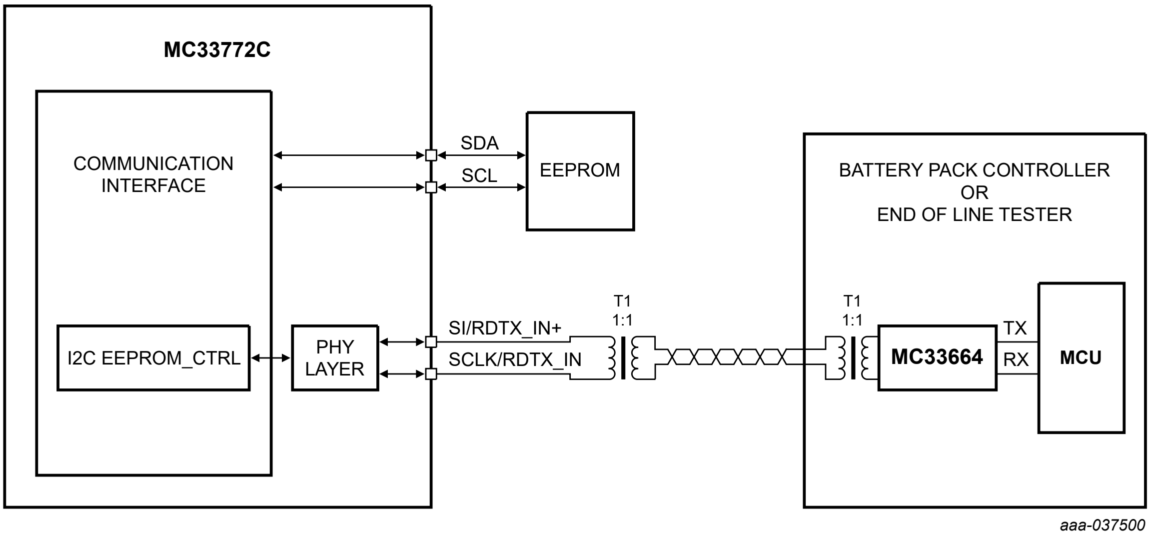


Figure 32. MC33772C calibration registers

11 Registers

11.1 Register map

Important: *Trying to access registers marked as reserved produces responses having all zeros in the data field.*

Unless otherwise stated, in all register descriptions, POR means one of the following:

- Power on reset
- Hardware reset
- Software reset
- Reset event based on SYS_CFG2[FLT_RST_CFG] register configuration

Table 36. Register table

Register		Response	Reference	Description	Notes
A[6:0]	Symbol				
$00	Reserved	Table 26		Reserved	Not readable or writeable
$01	INIT	Table 26	Section 11.2	Device initialization	Global write is forbidden for CID
$02	SYS_CFG_ GLOBAL	Table 26	Section 11.3	Global system configuration	Only accessible through a global access in transformer mode. In SPI mode it can be written by a standard write command.
$03	SYS_CFG1	Table 26	Section 11.4	System configuration	
$04	SYS_CFG2	Table 26	Section 11.5	System configuration	
$05	SYS_DIAG	Table 26	Section 11.6	System diagnostic	Writable in DIAG mode only, automatically cleared when exiting DIAG mode
$06	ADC_CFG	Table 26	Section 11.7	ADC configuration	
$07	ADC2_OFFSET_ COMP	Table 26	Section 11.8	ADC2 offset compensation	
$08	OV_UV_EN	Table 26	Section 11.9	CT measurement selection	
$09	CELL_OV_FLT	Table 26	Section 11.10	CT overvoltage fault	
$0A	CELL_UV_FLT	Table 26	Section 11.11	CT undervoltage fault	
$0B	TPL_CFG	Table 26	Section 11.12	TPL configuration for up and down Transmitter	
$0C	CB1_CFG	Table 26	Section 11.13	CB configuration for cell 1	
$0D	CB2_CFG	Table 26	Section 11.13	CB configuration for cell 2	
$0E	CB3_CFG	Table 26	Section 11.13	CB configuration for cell 3	
$0F	CB4_CFG	Table 26	Section 11.13	CB configuration for cell 4	
$10	CB5_CFG	Table 26	Section 11.13	CB configuration for cell 5	

Table 36. Register table*...continued*

Register		Response	Reference	Description	Notes
A[6:0]	Symbol				
$11	CB6_CFG	Table 26	Section 11.13	CB configuration for cell 6	
$12	Reserved	Table 26	Section 11.47	NXP reserved	
$13	Reserved	Table 26	Section 11.47	NXP reserved	
$14	Reserved	Table 26	Section 11.47	NXP reserved	
$15	Reserved	Table 26	Section 11.47	NXP reserved	
$16	Reserved	Table 26	Section 11.47	NXP reserved	
$17	Reserved	Table 26	Section 11.47	NXP reserved	
$18	Reserved	Table 26	Section 11.47	NXP reserved	
$19	Reserved	Table 26	Section 11.47	NXP reserved	
$1A	CB_OPEN_FLT	Table 26	Section 11.14	Open CB fault	
$1B	CB_SHORT_FLT	Table 26	Section 11.15	Short CB fault	
$1C	CB_DRV_STS	Table 26	Section 11.16	CB driver status	
$1D	GPIO_CFG1	Table 26	Section 11.17	GPIO configuration	
$1E	GPIO_CFG2	Table 26	Section 11.18	GPIO configuration	
$1F	GPIO_STS	Table 26	Section 11.19	GPIO diagnostic	
$20	AN_OT_UT_FLT	Table 26	Section 11.20	AN over and undertemperature	
$21	GPIO_SHORT_ ANx_OPEN_STS	Table 26	Section 11.21	Short GPIO / Open AN diagnostic	
$22	I_STATUS	Table 26	Section 11.22	PGA DAC value	
$23	COM_STATUS	Table 26	Section 11.23	Number of COM error counted	
$24	FAULT1_STATUS	Table 26	Section 11.24	Fault status	
$25	FAULT2_STATUS	Table 26	Section 11.25	Fault status	
$26	FAULT3_STATUS	Table 26	Section 11.26	Fault status	
$27	FAULT_MASK1	Table 26	Section 11.27	FAULT pin mask	
$28	FAULT_MASK2	Table 26	Section 11.28	FAULT pin mask	
$29	FAULT_MASK3	Table 26	Section 11.29	FAULT pin mask	
$2A	WAKEUP_MASK1	Table 26	Section 11.30	Wake-up events mask	
$2B	WAKEUP_MASK2	Table 26	Section 11.31	Wake-up events mask	
$2C	WAKEUP_MASK3	Table 26	Section 11.32	Wake-up events mask	
$2D	CC_NB_SAMPLES	Table 26	Section 11.33	Number of samples in coulomb counter	
$2E	COULOMB_CNT1	Table 26	Section 11.34	Coulomb counting accumulator	
$2F	COULOMB_CNT2	Table 26	Section 11.34	Coulomb counting accumulator	
$30	MEAS_ISENSE1	Table 26	Section 11.35	ISENSE measurement	
$31	MEAS_ISENSE2	Table 26	Section 11.35	ISENSE measurement	
$32	MEAS_STACK	Table 26	Section 11.36	Stack voltage measurement	

Table 36. Register table*...continued*

Register		Response	Reference	Description	Notes
A[6:0]	Symbol				
$33	Reserved	Table 26	Section 11.47	NXP reserved	
$34	Reserved	Table 26	Section 11.47	NXP reserved	
$35	Reserved	Table 26	Section 11.47	NXP reserved	
$36	Reserved	Table 26	Section 11.47	NXP reserved	
$37	Reserved	Table 26	Section 11.47	NXP reserved	
$38	Reserved	Table 26	Section 11.47	NXP reserved	
$39	Reserved	Table 26	Section 11.47	NXP reserved	
$3A	Reserved	Table 26	Section 11.47	NXP reserved	
$3B	MEAS_CELL6	Table 26	Section 11.36	Cell 6 voltage measurement	
$3C	MEAS_CELL5	Table 26	Section 11.36	Cell 5 voltage measurement	
$3D	MEAS_CELL4	Table 26	Section 11.36	Cell 4 voltage measurement	
$3E	MEAS_CELL3	Table 26	Section 11.36	Cell 3 voltage measurement	
$3F	MEAS_CELL2	Table 26	Section 11.36	Cell 2 voltage measurement	
$40	MEAS_CELL1	Table 26	Section 11.36	Cell 1 voltage measurement	
$41	MEAS_AN6	Table 26	Section 11.36	AN6 voltage measurement	
$42	MEAS_AN5	Table 26	Section 11.36	AN5 voltage measurement	
$43	MEAS_AN4	Table 26	Section 11.36	AN4 voltage measurement	
$44	MEAS_AN3	Table 26	Section 11.36	AN3 voltage measurement	
$45	MEAS_AN2	Table 26	Section 11.36	AN2 voltage measurement	
$46	MEAS_AN1	Table 26	Section 11.36	AN1 voltage measurement	
$47	MEAS_AN0	Table 26	Section 11.36	AN0 voltage measurement	
$48	MEAS_IC_TEMP	Table 26	Section 11.36	IC temperature measurement	
$49	MEAS_ VBG_ DIAG_ADC1A	Table 26	Section 11.36	ADC1-A voltage reference measurement	
$4A	MEAS_ VBG_ DIAG_ADC1B	Table 26	Section 11.36	ADC1-B voltage reference measurement	
$4B	TH_ALL_CT	Table 26	Section 11.37	CTx over and undervoltage threshold	
$4C	Reserved	Table 26	Section 11.47	NXP reserved	
$4D	Reserved	Table 26	Section 11.47	NXP reserved	
$4E	Reserved	Table 26	Section 11.47	NXP reserved	
$4F	Reserved	Table 26	Section 11.47	NXP reserved	
$50	Reserved	Table 26	Section 11.47	NXP reserved	
$51	Reserved	Table 26	Section 11.47	NXP reserved	
$52	Reserved	Table 26	Section 11.47	NXP reserved	
$53	Reserved	Table 26	Section 11.47	NXP reserved	

Table 36. Register table*...continued*

Register		Response	Reference	Description	Notes
A[6:0]	Symbol				
$54	TH_CT6	Table 26	Section 11.38	CT6 over and undervoltage threshold	
$55	TH_CT5	Table 26	Section 11.38	CT5 over and undervoltage threshold	
$56	TH_CT4	Table 26	Section 11.38	CT4 over and undervoltage threshold	
$57	TH_CT3	Table 26	Section 11.38	CT3 over and undervoltage threshold	
$58	TH_CT2	Table 26	Section 11.38	CT2 over and undervoltage threshold	
$59	TH_CT1	Table 26	Section 11.38	CT1 over and undervoltage threshold	
$5A	TH_AN6_OT	Table 26	Section 11.39	AN6 overtemperature threshold	
$5B	TH_AN5_OT	Table 26	Section 11.39	AN5 overtemperature threshold	
$5C	TH_AN4_OT	Table 26	Section 11.39	AN4 overtemperature threshold	
$5D	TH_AN3_OT	Table 26	Section 11.39	AN3 overtemperature threshold	
$5E	TH_AN2_OT	Table 26	Section 11.39	AN2 overtemperature threshold	
$5F	TH_AN1_OT	Table 26	Section 11.39	AN1 overtemperature threshold	
$60	TH_AN0_OT	Table 26	Section 11.39	AN0 overtemperature threshold	
$61	TH_AN6_UT	Table 26	Section 11.39	AN6 undertemperature threshold	
$62	TH_AN5_UT	Table 26	Section 11.39	AN5 undertemperature threshold	
$63	TH_AN4_UT	Table 26	Section 11.39	AN4 undertemperature threshold	
$64	TH_AN3_UT	Table 26	Section 11.39	AN3 undertemperature threshold	
$65	TH_AN2_UT	Table 26	Section 11.39	AN2 undertemperature threshold	
$66	TH_AN1_UT	Table 26	Section 11.39	AN1 undertemperature threshold	
$67	TH_AN0_UT	Table 26	Section 11.39	AN0 undertemperature threshold	
$68	TH_ISENSE_OC	Table 26	Section 11.40	ISENSE overcurrent threshold	
$69	TH_COULOMB_ CNT_MSB	Table 26	Section 11.41	Coulomb counter threshold (MSB)	
$6A	TH_COULOMB_ CNT_LSB	Table 26	Section 11.41	Coulomb counter threshold (LSB)	
$6B	SILICON_REV	Table 26	Section 11.42	Silicon revision	
$6C	EEPROM_CNTL	Table 26	Section 11.43	EEPROM transfer control	
$6D	DED_ENCODE1	Table 26	Section 11.44	ECC signature 1	
$6E	DED_ENCODE2	Table 26	Section 11.45	ECC signature 2	
$6F	FUSE_MIRROR_ DATA	Table 26	Section 11.46	Fuse mirror data	
$70	FUSE_MIRROR_ CNTL	Table 26	Section 11.46	Fuse mirror address	

Table 36. Register table...*continued*

Register		Response	Reference	Description	Notes
A[6:0]	Symbol				
$71	Reserved	Table 26	Section 11.47	NXP reserved	
...	Reserved	Table 26	Section 11.47	NXP reserved	
$7F	Reserved	Table 26	Section 11.47	NXP reserved	

Table 37. Mirror memory

Register		Description	Notes
A[4:0]	Name		
$00	FUSE_MIRROR_BANK0	Fuse bank 0	
$01	FUSE_MIRROR_BANK1	Fuse bank 1	
$02	FUSE_MIRROR_BANK2	Fuse bank 2	
$03	FUSE_MIRROR_BANK3	Fuse bank 3	
$04	FUSE_MIRROR_BANK4	Fuse bank 4	
$05	FUSE_MIRROR_BANK5	Fuse bank 5	
$06	FUSE_MIRROR_BANK6	Fuse bank 6	
$07	FUSE_MIRROR_BANK7	Fuse bank 7	
$08	FUSE_MIRROR_BANK8	Fuse bank 8	
$09	FUSE_MIRROR_BANK9	Fuse bank 9	
$0A	FUSE_MIRROR_BANK10	Fuse bank 10	
$0B	FUSE_MIRROR_BANK11	Fuse bank 11	
$0C	FUSE_MIRROR_BANK12	Fuse bank 12	
$0D	FUSE_MIRROR_BANK13	Fuse bank 13	
$0E	FUSE_MIRROR_BANK14	Fuse bank 14	DED_ENCODE2
$0F	FUSE_MIRROR_BANK15	Fuse bank 15	DED_ENCODE1
$10	FUSE_MIRROR_BANK16	Fuse bank 16	Traceability
$11	FUSE_MIRROR_BANK17	Fuse bank 17	Traceability
$12	FUSE_MIRROR_BANK18	Fuse bank 18	Traceability

11.2 Initialization register – INIT

Following power-up or soft POR, the MC33772C is in a reset state. In the Init mode, the user may read the registers of the MC33772C using the cluster id 00 0000b. The MC33772C must be enumerated before it acts upon to write commands.

To initialize the device, a write command has to be sent with the value of 00 0000b in the cluster Identifier field of the frame, Section 10.4.2, with the new cluster ID, that is the new address to be assigned to the node, must be written to the CID field of the INIT register. Only a device with current cluster ID of 00 0000b may be programmed to a new address. By programming the device with a new CID the device is considered enumerated. After a device has been initialized, it only acts on subsequent global write (transformer mode) or local write and responds to read commands matching the device cluster ID. Once a device has been enumerated, the CID bits in the register INIT cannot be reprogrammed unless the device receives a hard or soft reset.

The bit fields INIT[TPLx_TX_TERM] are used for preventing pins (RDTX_IN/OUT±) from floating when the MC33772Cs are connected in single ended daisy chain (without loop-back). It is to be noted that this applies only to last node in the daisy chain. Depending on which pin (RDTX_IN± or RDTX_OUT±) of last node is floating, INIT[TPLx_TX_TERM] should be set to 1. The MC33772C IC used in daisy chain communication with loop-back shall have the bit fields INIT[TPLx_TX_TERM] set to zero while for single ended daisy chain communication (without loop-back) the floating TPL port shall be set to 1.

When the bus forwarding bit INIT[BUSFW] is 0 (default):

The IC forwards all messages to its neighboring node. The IC also responds to read messages in both directions to balance current consumption for all nodes of the daisy chain.

When INIT[BUSFW] is 1:

- Normal mode: The IC does not forward any message
- Sleep mode: The IC only forwards the wake-up messages to enable all nodes in daisy chain to be activated
- The IC responds only in one direction (the direction in which it received the request). However, in case of internal fault in Sleep mode the IC sends wake-up messages in both directions on the daisy chain.

Table 38. INIT

INIT																
$01	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write								BUS_FW	TPL1_ TX_ TERM	TPL2_ TX_ TERM	CID					
Read	0	0	0	0	0	0	0									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUS_FW	Description	Bus forwarding, from one port to the opposite port and single side response to a READ request
	0	Forwarding to neighboring node and response on both sides (only if CID ≠ $00)
	1	Stop forwarding and response on single side (side at which the request was received)
	Reset condition	POR
TPL1_TX_TERM	Description	TPL transmitter termination for lower port (RDTX_IN)
	0	Disabled
	1	Enabled
	Reset condition	POR
TPL2_TX_TERM	Description	TPL transmitter termination for upper port (RDTX_OUT)
	0	Disabled
	1	Enabled
	Reset condition	POR
CID	Description	Cluster Identifier. Can be overidden by any combination different from "all zeros". Not accessible with global write
	0 0 0 0 0 0	Default
	x x x x x x	CID
	Reset condition	POR

11.3 System configuration global register SYS_CFG_GLOBAL

In TPL mode, only a global command can be used to write to register $02, while a local write is disregarded. In contrast, if using the SPI mode, only a local write to register $02 can be executed.

Table 39. SYS_CFG_GLOBAL

SYS_CFG_GLOBAL																
$02	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																GO2 SLEEP
Read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GO2SLEEP	Description	Go to sleep command
	0	Disabled
	1 (active pulse)	Device goes to Sleep mode after all conversions in progress are completed
	Reset condition	POR

11.4 System configuration register 1 – SYS_CFG1

The SYS_CFG1 register contains control bits and register settings that allow the user to adapt the MC33772C to specific applications and system requirements. Of these control bits, it is important to note the SYS_CFG1[SOFT_RST] bit is used to reset register contents of the device.

Table 40. SYS_CFG1

SYS_CFG1																
$03	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	CYCLIC_TIMER			DIAG_TIMEOUT			I_MEAS_EN	DO NOT CHANGE	CB_DRVEN	GO2DIAG	CB_MANUAL_PAUSE	SOFT_RST	FAULT_WAVE	WAVE_DC_BITx		x
Read										DIAG_ST		0				x
Reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1

CYCLIC_TIMER	Description	Timer to trigger cyclic measurements in Normal mode or Sleep mode
	0 0 0	Cyclic measure is disabled, whatever the mode
	0 0 1	Continuous measurements
	0 1 0	0.1 s
	0 1 1	0.2 s
	1 0 0	1.0 s
	1 0 1	2.0 s
	1 1 0	4.0 s
	1 1 1	8.0 s
	Reset condition	POR
DIAG_TIMEOUT	Description	Diag mode timeout. Length of time the device is allowed to be in Diag mode before being forced to Normal mode
	0 0 0	No timer, not allowed to enter Diag mode
	0 0 1	0.05 s
	0 1 0	0.1 s
	0 1 1	0.2 s
	1 0 0	1.0 s
	1 0 1	2.0 s
	1 1 0	4.0 s
	1 1 1	8.0 s
	Reset condition	POR
I_MEAS_EN	Description	Enable for current measurement chain
	0	Disabled
	1	Current measurement chain is enabled
	Reset condition	POR

Table 40. SYS_CFG1*...continued*

CB_DRVEN	Description	General enable or disable for all cell balance drivers
	0	Disabled
	1	Enabled, each cell balance driver can be individually switched on and off by CBx_CFG register
	Reset condition	POR
GO2DIAG	Description	Commands the device to Diag mode. Rewriting the GO2DIAG bit restarts the DIAG_TIMEOUT
	0	Exit Diag mode
	1	Enter Diag mode (starts timer)
	Reset condition	POR
CB_MANUAL_PAUSE	Description	Cell balancing manual pause
	0	Disabled. CB switches can be normally commanded on/off by the dedicated logic functions
	1	CB switches are forced off, CB counters are not frozen
	Reset condition	POR
DIAG_ST	Description	Identifies when the device is in Diag mode
	0	System is not in Diag mode
	1	System is in Diag mode
	Reset condition	POR
SOFT_RST	Description	Software reset
	0	Disabled
	1 (active pulse)	Active software reset
	Reset condition	POR (bit is not reset if reset was due to software reset)
FAULT_WAVE	Description	FAULT pin waveform control bit
	0	FAULT pin has high or low level behavior. FAULT pin high, fault is present. FAULT pin low indicates no fault present
	1	FAULT pin has heartbeat wave when no fault is present. Pulse high time is fixed at 500 μs
	Reset condition	POR
WAVE_DC_BITx	Description	Controls the off time of the heartbeat pulse
	0 0	500 μs
	0 1	1.0 ms
	1 0	10 ms
	1 1	100 ms
	Reset condition	POR

11.5 System configuration register 2 – SYS_CFG2

Table 41. SYS_CFG2

SYS_CFG2																
$04	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	x	x	x				FLT_RST_CFG[1]				TIMEOUT_COMM		x	w0c[2]	NUMB_ODD	HAMM_ENCOD
Read	x	x	x	PREVIOUS_STATE			FLT_RST_CFG[1]				TIMEOUT_COMM		x	VPRE_UV	NUMB_ODD	HAMM_ENCOD
Reset	0	0	0	0	0	0	1	1	0	0	1	1	0	1	0	0

PREVIOUS_STATE	Description	Information about the previous state of the device
	0 0 0	The device is coming from Init state (reset value)
	0 0 1	The device is coming from Idle state
	0 1 0	The device is coming from Normal state
	0 1 1	The device is coming from Diag state
	1 1 1	The device is coming from Sleep state
	1 1 0	The device is coming from Cyclic_WUP state
	Reset condition	POR

Table 41. SYS_CFG2*...continued*

FLT_RST_CFG	Description	Fault reset configuration[3]
	0 0 1 1	Disabled COM timeout (1024 ms) reset and OSC fault monitoring and reset
	0 1 0 1	Enabled OSC fault monitoring
	0 1 1 0	Enabled OSC fault monitoring and reset
	1 0 0 1	Enabled COM timeout (1024 ms) reset
	1 0 1 0	Enabled COM timeout (1024 ms) reset and OSC fault monitoring
	1 1 0 0	Enable COM timeout (1024 ms) reset and OSC fault monitoring and reset (reset value)
	others	Invalid, leads to enabled COM timeout (1024 ms) reset and OSC fault monitoring and reset (1100)
	Reset condition	POR
TIMEOUT_COMM	Description	No communication timeout - flag in FAULT1_STATUS[COM_LOSS] if no communication during…
	0 0	32 ms
	0 1	64 ms
	1 0	128 ms
	1 1	256 ms (reset value)
	Reset condition	POR
VPRE_UV	Description	V_{PRE} undervoltage detection
	0	No undervoltage detected (reset value)
	1	Undervoltage detected on V_{PRE}
	Reset condition	POR / Clear on write 0
NUMB_ODD	Description	Odd number of cells in the cluster (useful for open-load diagnosis)
	0	Even configuration (reset value)
	1	Odd configuration
	Reset condition	POR
HAMM_ENCOD	Description	Hamming encoders
	0	Decode - the DED Hamming decoders fulfill their job (reset value)
	1	Encode - the DED Hamming decoders generate the redundancy bits
	Reset condition	POR

[1] The GO2RESET option should not be disabled after a communication time out.
[2] w0c: write 0 to clear
[3] For more information, refer to Figure 8

11.6 System diagnostics register – SYS_DIAG

Table 42. SYS_DIAG

SYS_DIAG																
$05	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	FAULT_ DIAG			I_MUX		ISENSE_ OL_ DIAG	ANx_ OL_ DIAG	ANx_ TEMP_ DIAG	DA_DIAG	POL ARITY	CT_ LEAK_ DIAG	CT_ OV_UV	CT_OL_ ODD	CT_OL_ EVEN	CB_OL_ ODD	CB_OL_ EVEN
Read		0	0													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FAULT_DIAG	Description	FAULT pin driver command
	0	No FAULT pin drive, FAULT pin is under command of the pack controller
	1	FAULT pin is forced to high level
	Reset condition	POR
I_MUX	Description	Allows user to select between various inputs to PGA to be converted by ADC2
	0 0	(ISENSE+, ISENSE−)
	0 1	(GPIO5, GPIO6)
	1 0	Calibrated internal reference (VREF_DIAG)
	1 1	PGA zero (PGA differential inputs terminated to ground)
	Reset condition	POR

Table 42. SYS_DIAG...*continued*

ISENSE_OL_DIAG	Description	ISENSE open load diagnostic control bit. Enables or disables internal pull-up resistors on the ISENSE input pins
	0	Disabled
	1	Enabled
	Reset condition	POR
ANx_OL_DIAG	Description	ANx open load diagnostic control bit. Used to activate the pull-down on GPIO input pins
	0	Diagnostic disabled
	1	Diagnostic enabled
	Reset condition	POR
ANx_TEMP_DIAG	Description	Control bit to activate the OT/UT diagnostic on GPIOx configured as ANx ratiometric or single ended ADC input
	0	Diagnostic inactive
	1	Diagnostic active
	Reset condition	POR
DA_DIAG	Description	Cell voltage channel functional verification. Diagnostic mode function only
	0	No check
	1	Check is enabled (floating Zener conversion, ground Zener measurement added, comparison)
	Reset condition	POR
POLARITY	Description	Control bit used in terminal leakage detection. Controls the polarity between the level shifter and the ADC1-A and ADC1-B converters
	0	Noninverted
	1	Inverted
	Reset condition	POR
CT_LEAK_DIAG	Description	Control bit used in terminal leakage detection. Commands the MUX to route the CTx/CBx pin to ADC1-A,B converters. This bit must be exclusive vs. DA_DIAG
	0	Normal operation, CTx are MUXed to converter
	1	Δ between CT and CB pins are routed to the analog front end, to be converted
	Reset condition	POR
CT_OV_UV	Description	OV and UV diagnostic is enabled. This bit must be set to logic 0 when performing CT open load diagnostic
	0	OV and UV diagnostic disabled
	1	OV and UV diagnostic enabled
	Reset condition	POR
CT_OL_ODD	Description	Control bit used to control the odd numbered cell terminal open detect switches
	0	Odd switches are open
	1	Odd switches are closed (may be set only when CT_OL_EVEN is logic 0)
	Reset condition	POR
CT_OL_EVEN	Description	Control bit used to control the even numbered cell terminal open detect switches
	0	Even switches are open
	1	Even switches are closed (may be set only when CT_OL_ODD is logic 0)
	Reset condition	POR
CB_OL_ODD	Description	Control bit used to control the cell balance open load ODD detection switches
	0	ODD cell balance open load detection switches are open
	1	ODD cell balance open load detection switches are closed
	Reset Condition	POR
CB_OL_EVEN	Description	Control bit used to control the cell balance open load EVEN detection switches
	0	EVEN cell balance open load detection switches are open
	1	EVEN cell balance open load detection switches are closed
	Reset condition	POR

11.7 ADC configuration register – ADC_CFG

The ADC_CFG is used to set the conversion parameters of the three ADC converters and command the MC33772C to perform on-demand conversions in both normal and diagnostic modes.

Table 43. ADC_CFG

ADC_CFG																
$06	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	AVG				SOC	PGA_GAIN			CC_RST	x	ADC1_A_DEF		ADC1_B_DEF		ADC2_DEF	
Read					EOC_N	PGA_GAIN_S			0	x						
Reset	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	1

AVG	Description	With each conversion request, the number of samples to be averaged can be configured
	0 0 0 0	No averaging, the result is taken as is (compatibility mode)
	0 0 0 1	Averaging of 2 consecutive samples
	0 0 1 0	Averaging of 4 consecutive samples
	0 0 1 1	Averaging of 8 consecutive samples
	0 1 0 0	Averaging of 16 consecutive samples
	0 1 0 1	Averaging of 32 consecutive samples
	0 1 1 0	Averaging of 64 consecutive samples
	0 1 1 1	Averaging of 128 consecutive samples
	1 0 0 0	Averaging of 256 consecutive samples
	All other Configurations	No averaging, the result is taken as is (compatibility mode)
	Reset condition	POR
SOC	Description	Control bit to command the MC33772C to initiate a conversion sequence
	0	Disabled. Writing SOC to 0 has no effect on an ongoing conversion sequence
	1 (active pulse)	Enabled. Initiate a conversion sequence
	Reset condition	POR
EOC_N	Description	End of conversion flag
	0	Device has completed the commanded conversion
	1	Device is performing the commanded conversion
	Reset condition	POR
PGA_GAIN	Description	Define the gain of the ADC2 programmable gain amplifier
	0 0 0	4
	0 0 1	16
	0 1 0	64
	0 1 1	256
	1 x x	Automatic gain selection (internally adjusted)
	Reset condition	POR
PGA_GAIN_S	Description (bit 10)	Automatic gain mode status (information available only if SYS_CFG1[I_MEAS_EN] = 1)
	0	Fixed gain
	1	Automatic gain control
	Reset condition	POR
	Description (bit[9:8])	Report the current gain of the ADC2 programmable gain amplifier (automatically settled or not). (information available only if SYS_CFG1[I_MEAS_EN] = 1)
	0 0	4
	0 1	16
	1 0	64
	1 1	256
	Reset condition	POR
CC_RST	Description	Control bit used to reset the value of the coulomb counter to 0
	0	No action
	1 (active pulse)	Reset coulomb counter registers COULOMB_CNT1 and COULOMB_CNT2 and the CC_NB_SAMPLES registers
	Reset condition	POR

Table 43. ADC_CFG*...continued*

ADC1_A_DEF	Description	ADC1_A measurement resolution
	0 0	13 bit
	0 1	14 bit
	1 0	15 bit
	1 1	16 bit
	Reset condition	POR
ADC1_B_DEF	Description	ADC1_B measurement resolution
	0 0	13 bit
	0 1	14 bit
	1 0	15 bit
	1 1	16 bit
	Reset condition	POR
ADC2_DEF	Description	ADC2 measurement resolution
	0 0	13 bit
	0 1	14 bit
	1 0	15 bit
	1 1	16 bit
	Reset condition	POR

11.8 Current measurement chain offset compensation – ADC2_OFFSET_COMP

This register contains an 8-bit signed data (two's complement). The content of the offset compensation register is added directly to the data at the end of the channel measurement, independent on the PGA gain. Even though the current channel is fully offset compensated, the PCB HW introduces an extra offset that can be compensated by means of this data. This register provides several bits that are able to influence the behavior of the coulomb counter.

Table 44. ADC2_OFFSET_COMP

ADC2_OFFSET_COMP																
$07	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	CC_RST_CFG	FREE_CNT	w0c[1]	w0c[1]	w0c[1]	w0c[1]	x	ALLCBOFF_ON_SHORT	ADC2_OFFSET_COMP							
Read			CC_P_OVF	CC_N_OVF	SAMP_OVF	CC_OVT	x									
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CC_RST_CFG	Description	Configuration of the action linked to the read of coulomb count results
	0	No linked action
	1	Reading any CC register (from @ $2D to @ $2F) also resets the coulomb counters
	Reset condition	POR
FREE_CNT	Description	Configuration of the free running coulomb counters
	0	No free-running, coulomb counters clamp on min/max values
	1	Free-running mode. No clamp but rollover
	Reset condition	POR
CC_P_OVF	Description	Overflow indicator on the COULOMB_CNT1,2[COULOMB_CNT]
	0	No overflow
	1	COULOMB_CNT1,2[COULOMB_CNT] went in overflow
	Reset condition	POR / Clear on write 0
CC_N_OVF	Description	Underflow indicator on the COULOMB_CNT1,2[COULOMB_CNT]
	0	No underflow
	1	COULOMB_CNT1,2[COULOMB_CNT] went in underflow
	Reset condition	POR / Clear on write 0

Table 44. ADC2_OFFSET_COMP*...continued*

SAMP_OVF	Description	Overflow indicator on the CC_NB_SAMPLES
	0	No underflow
	1	CC_NB_SAMPLES went in overflow
	Reset condition	POR / Clear on write 0
CC_OVT	Description	Overthreshold indicator on the COULOMB_CNT1,2[COULOMB_CNT]
	0	No over threshold
	1	COULOMB_CNT1,2[COULOMB_CNT] went in over threshold (TH_COULOMB_CNT)
	Reset condition	POR / Clear on write 0
ALLCBOFF_ON_SHORT	Description	All CB's turn off in case of at least one short
	0	Only shorted CB's are turned off
	1	If at least one CB is shorted, all CB's are then turned off (CB_DRVEN is reset)
	Reset condition	POR
ADC2_OFFSET_COMP	Description	Offset value, signed (two's complement) with V_{2RES} resolution. It can be used to compensate for a PCB offset
	Reset condition	POR

[1] w0c: write 0 to clear

11.9 Cell select register – OV_UV_EN

The user has the option to select a common overvoltage and undervoltage threshold, or individual thresholds for each cell. To use a common threshold for all cell terminal inputs, the user must program register TH_ALL_CT and enable the common threshold bit. An individual threshold may be programmed for each cell terminal through register TH_CTx. Either threshold selection requires the CTx_OVUV_EN bit be set for the MC33772C to monitor the cell terminal input for over and undervoltage.

Table 45. OV_UV_EN

OV_UV_EN																
$08	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	COMMON_OV_TH	COMMON_UV_TH									CT6_OVUV_EN	CT5_OVUV_EN	CT4_OVUV_EN	CT3_OVUV_EN	CT2_OVUV_EN	CT1_OVUV_EN
Read			0	0	0	0	0	0	0	0						
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

COMMON_OV_TH	Description	All CTx measurement use the common overvoltage threshold register for comparison
	0	Use individual threshold register
	1	Use common threshold register
	Reset condition	POR
COMMON_UV_TH	Description	All CTx measurement use the common undervoltage threshold register for comparison
	0	Use individual threshold register
	1	Use common threshold register
	Reset condition	POR
CTx_OVUV_EN	Description	Enable or disable ADC data to be compared with thresholds for OV/UV. If disabled no OV/UV fault is set
	0	OV/UV disabled
	1	OV/UV is enabled
	Reset condition	POR

11.10 Cell terminal overvoltage fault register – CELL_OV_FLT

The CELL_OV_FLT register contains the overvoltage fault status of each cell. The CELL_OV_FLT register is updated with each cyclic conversion and each on-demand conversion from the system controller. In Normal mode, the CTx_OV_FLT bit may be cleared by writing logic 0 when overvoltage is no longer present at the cell terminal inputs.

Table 46. CELL_OV_FLT

CELL_OV_FLT																
$09	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write											w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	0	0	0	0	0	0	0	0	0	0	CT6_OV_FLT	CT5_OV_FLT	CT4_OV_FLT	CT3_OV_FLT	CT2_OV_FLT	CT1_OV_FLT
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CTx_OV_FLT	Description	CTx_OV_FLT register contains the status of the overvoltage fault for each cell terminal. Register is updated with each internal and system controller on-demand conversion cycle														
	0	No cell terminal overvoltage														
	1	Cell terminal overvoltage detected on terminal x														
	Reset condition	POR / Clear on write 0														

[1] w0c: write 0 to clear

11.11 Cell terminal undervoltage fault register – CELL_UV_FLT

The CELL_UV_FLT register contains the undervoltage fault status of each cell. The CELL_UV_FLT register is updated with each cyclic conversion and each on-demand conversion from the system controller. In Normal mode, the CTx_UV_FLT bit may be cleared by writing logic 0 when undervoltage is no longer present at the cell terminal inputs.

Table 47. CELL_UV_FLT

CELL_UV_FLT																
$0A	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write											w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	0	0	0	0	0	0	0	0	0	0	CT6_UV_FLT	CT5_UV_FLT	CT4_UV_FLT	CT3_UV_FLT	CT2_UV_FLT	CT1_UV_FLT
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CTx_UV_FLT	Description	CTx_UV_FLT register contains the status of the overvoltage fault for each cell terminal. Register is updated with each internal and system controller requested conversion cycle														
	0	No cell terminal undervoltage														
	1	Cell terminal undervoltage detected on terminal x														
	Reset condition	POR / Clear on write 0														

[1] w0c: write 0 to clear

11.12 TPL register – TPL_CFG

TPL_CFG register configures up and down transmitter. It allows the pack controller to configure transmitter drive strength based on capacitive or transformer isolation and selection of differential load termination.

Table 48. TPL_CFG

TPL_CFG																
$0B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	DO NOT CHANGE															
Read																
Reset	0	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0

Note: *The default value TPL_CFG register is set considering a transmission line of 120 Ω.*

11.13 Cell balance configuration register – CBx_CFG

The cell balance configuration register holds the operating parameters of the cell balance output drivers.

Table 49. CBx_CFG

CBx_CFG																
$0C to $19	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write							CBx_EN	CBx_TIMER								
Read	0	0	0	0	0	0	CBx_STS									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CBx_EN	Description	Cell balance enable
	0	Cell balance driver disabled
	1	Cell balance is enabled or re-launched if overwritten (restarts the timer count from zero and enables the driver)
	Reset condition	POR
CBx_STS	Description	Cell balance driver status
	0	Cell balance driver is off
	1	Cell balance driver is on
	Reset condition	POR
CBx_TIMER	Description	Cell balance timer in minutes
	000000000	0.5 minutes
	000000001	1 minute
	000000010	2 minutes
	...	
	111111111	511 minutes
	Reset condition	POR

11.14 Cell balance open load fault detection register – CB_OPEN_FLT

Table 50. CB_OPEN_FLT

CB_OPEN_FLT																
$1A	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write											w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	0	0	0	0	0	0	0	0	0	0	CB6_ OPEN_ FLT	CB5_ OPEN_ FLT	CB4_ OPEN_ FLT	CB3_ OPEN_ FLT	CB2_ OPEN_ FLT	CB1_ OPEN_ FLT
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CBx_OPEN_FLT	Description	Cell balancing open load detection – (info) Logic OR of CBx_OPEN_FLT is provided in the FAULT2_STATUS[CB_OPEN_FLT]
	0	No open load cell balance fault detected
	1	Off state open load detected
	Reset condition	POR / Clear on write 0

[1] w0c: write 0 to clear

11.15 Cell balance shorted load fault detection register – CB_SHORT_FLT

The cell balance short detection register holds the cell balance shorted load status.

Table 51. CB_SHORT_FLT

CB_SHORT_FLT																
$1B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write											w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	0	0	0	0	0	0	0	0	0	0	CB6_ SHORT_ FLT	CB5_ SHORT_ FLT	CB4_ SHORT_ FLT	CB3_ SHORT_ FLT	CB2_ SHORT_ FLT	CB1_ SHORT_ FLT
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CBx_SHORT_FLT	Description		Cell balancing shorted load fault detection – (info) CBx_SHORT_FLT Ored is provided in the FAULT2[CB_SHORT_FLT]													
	0		No shorted load fault detected													
	1		Shorted load fault detected													
	Reset condition		POR / Clear on write 0													

[1] w0c: write 0 to clear

11.16 Cell balance driver on/off status register – CB_DRV_STS

Table 52. CB_DRV_STS

CB_DRV_STS																
$1C	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	0	0	0	0	0	0	0	0	0	0	CB6_STS	CB5_STS	CB4_STS	CB3_STS	CB2_STS	CB1_STS
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CBx_STS	Description		Contains the state of the cell balance driver													
	0		Driver CBx is off													
	1		Driver CBx is on													
	Reset condition		POR													

11.17 GPIO configuration register 1 – GPIO_CFG1

The GPIO_CFG1 register programs the individual GPIO port as a ratiometric, single ended, input or output port.

Table 53. GPIO_CFG1

GPIO_CFG1																
$1D	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write			GPIO6_CFG		GPIO5_CFG		GPIO4_CFG		GPIO3_CFG		GPIO2_CFG		GPIO1_CFG		GPIO0_CFG	
Read	0	0														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIOx_CFG	Description		Register controls the configuration of the GPIO port													
	0 0		GPIOx configured as analog input for ratiometric measurement													
	0 1		GPIOx configured as analog input for absolute measurement													
	1 0		GPIOx configured as digital input													
	1 1		GPIOx configured as digital output													
	Reset condition		POR													

11.18 GPIO configuration register 2 – GPIO_CFG2

Table 54. GPIO_CFG2

GPIO_CFG2																
$1E	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write							GPIO2_SOC	GPIO0_WU	GPIO0_FLT_ACT	GPIO6_DR	GPIO5_DR	GPIO4_DR	GPIO3_DR	GPIO2_DR	GPIO1_DR	GPIO0_DR
Read	0	0	0	0	0	0										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO2_SOC	Description	GPIO2 used as ADC1_A/ADC1_B start-of-conversion. Requires GPIO2_CFG = 10
	0	GPIO2 port ADC trigger is disabled
	1	GPIO2 port ADC trigger is enabled. A rising edge on GPIO2 triggers an ADC1-A and ADC1-B conversion – only when in normal mode
	Reset condition	POR
GPIO0_WU	Description	GPIO0 wake-up capability. Valid only when GPIO0_CFG = 10
	0	No wake-up capability
	1	Wake-up on any edge, transitioning the system from sleep to normal
	Reset condition	POR
GPIO0_FLT_ACT	Description	GPIO0 activate fault output pin. Valid only when GPIO0_CFG = 10
	0	Does not activate FAULT pin when GPIO0 is configured as an input and is logic 1
	1	Activates the FAULT pin when GPIO is configured as an input and is logic 1
	Reset condition	POR
GPIOx_DR	Description	GPIOx pin drive. Ignored except when GPIOx_CFG = 11
	0	Drive GPIOx to low level
	1	Drive GPIOx to high level
	Reset condition	POR

11.19 GPIO status register – GPIO_STS

Table 55. GPIO_STS

GPIO_STS																
$1F	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write		w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]								
Read	0	GPIO6_H	GPIO5_H	GPIO4_H	GPIO3_H	GPIO2_H	GPIO1_H	GPIO0_H	0	GPIO6_ST	GPIO5_ST	GPIO4_ST	GPIO3_ST	GPIO2_ST	GPIO1_ST	GPIO0_ST
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOx_H	Description	The GPIOx_H bits detects and latches the low to high transition occurring on the GPIOx input
	0	No high state detected
	1	A high state has been detected
	Reset condition	POR / Clear on write 0
GPIOx_ST	Description	Real time GPIOx status
	0	Report GPIOx at low level
	1	Report GPIOx at high level
	Reset condition	POR

[1] w0c: write 0 to clear

11.20 Overtemperature/undertemperature fault register – AN_OT_UT_FLT

Table 56. AN_OT_UT_FLT

AN_OT_UT_FLT																
$20	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write		w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]		w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	0	AN6_OT	AN5_OT	AN4_OT	AN3_OT	AN2_OT	AN1_OT	AN0_OT	0	AN6_UT	AN5_UT	AN4_UT	AN3_UT	AN2_UT	AN1_UT	AN0_UT
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 56. AN_OT_UT_FLT*...continued*

ANx_OT	Description	Overtemperature detection for ANx – ANx_OT ored is provided in FAULT1_STATUS[AN_OT_FLT]
	0	No overtemperature fault detected
	1	Overtemperature fault detected on ANx
	Reset condition	POR / Clear on write 0 (ANx_OT is set again on next cyclic conversion or on-demand conversion if overtemperature persists)
ANx_UT	Description	Undertemperature detection for ANx – ANx_UT ored is provided in FAULT1_STATUS[AN_UT_FLT]
	0	No undertemperature fault detected
	1	Undertemperature fault detected on ANx
	Reset condition	POR / Clear on write 0 (ANx_UT is set again on next cyclic conversion or on-demand conversion if undertemperature persists)

[1] w0c: write 0 to clear

11.21 GPIO open short register – GPIO_SHORT_ANx_OPEN_STS

Table 57. GPIO_SHORT_ANx_OPEN_STS

GPIO_SHORT_ANx_OPEN_STS																
$21	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write		w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]		w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	0	GPIO6_ SH	GPIO5_ SH	GPIO4_ SH	GPIO3_ SH	GPIO2_ SH	GPIO1_ SH	GPIO0_ SH	0	AN6_ OPEN	AN5_ OPEN	AN4_ OPEN	AN3_ OPEN	AN2_ OPEN	AN1_ OPEN	AN0_ OPEN
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIOx_SH	Description	GPIOx short detection GPIOx_SH ored is provided in FAULT2_STATUS[GPIO_SHORT_FLT]
	0	No short detected
	1	Short detected, pad sense is different from pad command
	Reset condition	POR / Clear on write 0
ANx_OPEN	Description	Analog inputs open load detection. ANx_OPEN ored is provided in FAULT2_STATUS[AN_OPEN_FLT]
	0	No open load detected
	1	Open load detected on Anx
	Reset condition	POR / Clear on write 0 (ANx_OPEN is set again with open load detect switch closed and open load persists)

[1] w0c: write 0 to clear

11.22 Current measurement status register – I_STATUS

Table 58. I_STATUS

I_STATUS																
$22	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	PGA_DAC								0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PGA_DAC	Description	DAC code
	0 0 0 0 0 0 0 0	DAC code is initially all zeros
	1 1 1 1 1 1 1 1	DAC code to be provided to the PGA (for offset cancellation), calculated through an autozero phase
	Reset condition	POR

11.23 Communication status register – COM_STATUS

Table 59. COM_STATUS

COM_STATUS																
$23	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	w0c[1]															
Read	COM_ERR_COUNT								0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

COM_ERR_COUNT	Description	Number of communication errors detected
	0 0 0 0 0 0 0 0	0 communication errors have been detected
	...	
	1 1 1 1 1 1 1 1	255 communication errors have been detected. Overflow of counter sets FAULT1_STATUS[COMM_ERR_OVR_FLT]. Count remains at 255 until cleared by controller
	Reset condition	POR / Clear on write 0

[1] w0c: write 0 to clear

11.24 Fault status register 1 – FAULT1_STATUS

Table 60. FAULT1_STATUS

FAULT1_STATUS																
$24	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]				
Read	POR	RESET_ FLT	COM_ ERR_ OVR_ FLT	VPWR_ OV_FLT	VPWR_ LV_FLT	COM_ LOSS_ FLT	COM_ ERR_ FLT	CSB_ WUP_ FLT	GPIO0_ WUP_ FLT	I2C_ ERR_ FLT	IS_OL_ FLT	IS_OC_ FLT	AN_ OT_FLT	AN_ UT_FLT	CT_ OV_FLT	CT_ UV_FLT
Reset	1	0**	0*	0*	0*	0**	0*	0	0	0	0	0	0	0	0	0
Depending on the voltage conditions occurring on some pins at the IC initialization, the initial value of bits marked by a * may be flipped. Values marked ** may be flipped at reset depending on its cause (see bit descriptions).																

POR	Description	Power-On-Reset indication (POR)
	0	No POR
	1	Device has PORed
	Reset condition	POR / Clear on write 0
RESET_FLT	Description	RESET Indication (non-maskable)
	0	No reset
	1	Device has been reset through the RESET pin or by a write command setting the SYS_CFG1[SOFT_RST] or by a communication loss or an oscillator monitoring fault
	Reset condition	POR / Clear on write 0
COM_ERR_OVR_FLT	Description	Overflow indicator on the COM_STATUS[COM_ERR_COUNT]
	0	No error
	1	COM_STATUS[COM_ERR_COUNT] went in overflow
	Reset condition	POR / Clear on write 0
VPWR_OV_FLT	Description	VPWR overvoltage notification[2]
	0	No overvoltage (VPWR < VPWR(OV_FLAG)) detected
	1	Overvoltage detected (VPWR > VPWR(OV_FLAG), timing filtered)
	Reset condition	POR / Clear on write 0
VPWR_LV_FLT	Description	VPWR low-voltage notification
	0	No low-voltage (VPWR > VPWR(LV_FLAG)) detected
	1	Low-voltage detected (VPWR < VPWR(LV_FLAG), timing filtered)
	Reset condition	POR / Clear on write 0
COM_LOSS_FLT	Description	In Normal mode, each slave device must receive a local message within the programmed period or COM_LOSS_FLT flag is set
	0	No error
	1	Communication loss detected
	Reset condition	POR / Clear on write 0

Table 60. FAULT1_STATUS...*continued*

COM_ERR_FLT	Description	Communication error detected
	0	No error
	1	An error has been detected during a communication
	Reset condition	POR / Clear on write 0
CSB_WUP_FLT	Description	CBS wake-up notification
	0	No wake-up
	1	CSB wake-up detected
	Reset condition	POR / Clear on write 0
GPIO0_WUP_FLT	Description	GPIO0 wake-up notification
	0	No wake-up
	1	GPIO0 wake-up detected
	Reset condition	POR / Clear on write 0
I2C_ERR_FLT	Description	I^2C communication error during the transfer from EEPROM to the IC
	0	No Error
	1	Error detected
	Reset condition	POR / Clear on write 0
IS_OL_FLT	Description	ISENSE pins open load detected
	0	No open load detected
	1	Open load detected in one or both ISENSE pins
	Reset Condition	POR / Clear on write 0
IS_OC_FLT	Description	ISENSE overcurrent detected (Sleep mode only)
	0	No overcurrent detected
	1	Overcurrent detected from ISENSE inputs
	Reset condition	POR / Clear on write 0
AN_OT_FLT	Description	Analog input overtemperature detection
	0	No overtemperature detected
	1	Overtemperature detected in one or more of the ANx analog inputs
	Reset condition	POR / Clear on write 0 all AN_OT_UT[ANx_OT] bits
AN_UT_FLT	Description	Analog inputs undertemperature detection[2]
	0	No undertemperature detected
	1	Undertemperature detected in one or more of the ANx analog inputs
	Reset condition	POR / Clear on write 0 all AN_OT_UT[ANx_UT] bits
CT_OV_FLT	Description	Cell terminal overvoltage detection[2]
	0	No overvoltage detected
	1	Overvoltage detected in one or more of the 6 cell terminals
	Reset condition	POR / Clear on write 0 all CELL_OV[CTx_OV] bits
CT_UV_FLT	Description	Cell terminal undervoltage detection
	0	No undervoltage detected
	1	Undervoltage detection in one or more of the 6 cell terminals
	Reset condition	POR / Clear on write 0 all CELL_UV[CTx_UV] bits

[1] w0c: write 0 to clear
[2] Ignore if FAULT2_STATUS[VANA_UV_FLT] is set

11.25 Fault status register 2 – FAULT2_STATUS

Table 61. FAULT2_STATUS

FAULT2_STATUS																
$25	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]					w0c[1]	w0c[1]	w0c[1]
Read	VCOM_ OV_FLT	VCOM_ UV_FLT	VANA_ OV_FLT	VANA_ UV_FLT	ADC1_ B_FLT	ADC1_ A_FLT	GND_ LOSS_ FLT	IC_ TSD_ FLT	IDLE_ MODE_ FLT	AN_ OPEN_ FLT	GPIO_ SHORT_ FLT	CB_ SHORT_ FLT	CB_ OPEN_ FLT	OSC_ ERR_ FLT	DED_ ERR_ FLT	FUSE_ ERR_ FLT
Reset	0*	0*	0*	0*	0	0	0*	0	0	0	0	0	0	0*	0*	0**
Depending on the voltage conditions occurring on some pins at the IC initialization, the initial value of bits marked by a * may be flipped. Values marked ** may be flipped at reset depending on its cause (see bit descriptions).																

VCOM_OV_FLT	Description	VCOM overvoltage notification[2]
	0	No overvoltage detected
	1	Overvoltage has been detected on VCOM supply
	Reset condition	POR / Clear on write 0
VCOM_UV_FLT	Description	VCOM undervoltage notification
	0	No undervoltage detected
	1	Undervoltage has been detected on VCOM supply
	Reset Condition	POR / Clear on write 0
VANA_OV_FLT	Description	VANA overvoltage notification[2]
	0	No overvoltage detected
	1	Overvoltage has been detected on the VANA supply
	Reset condition	POR / Clear on write 0
VANA_UV_FLT	Description	VANA undervoltage notification
	0	No undervoltage detected
	1	Undervoltage has been detected on the VANA supply
	Reset condition	POR / Clear on write 0
ADC1_B_FLT	Description	ADC1_B fault notification[2]
	0	No fault detected
	1	ADC1_B fault (over or undervoltage has been detected on MEAS_VBG_DIAG_ADC1B)
	Reset condition	POR / Clear on write 0
ADC1_A_FLT	Description	ADC1_A fault notification[2]
	0	No fault detected
	1	ADC1_A fault (over or undervoltage has been detected on MEAS_VBG_DIAG_ADC1A)
	Reset condition	POR / Clear on write 0
GND_LOSS_FLT	Description	Loss of ground has been detected on DGND or AGND or CGND
	0	No error
	1	Loss of ground detected
	Reset condition	POR / Clear on write 0
IC_TSD_FLT	Description	IC thermal limitation notification
	0	No thermal limitation detected
	1	Thermal limitation detected
	Reset condition	POR / Clear on write 0
IDLE_MODE_FLT	Description	Idle mode notification
	0	No notification
	1	The system has transitioned through idle mode
	Reset condition	POR / Clear on write 0
AN_OPEN_FLT	Description	Analog inputs open load detection
	0	No open load detected
	1	Open load detected in one or more of the Anx analog inputs
	Reset condition	POR / Clear on write 0 all GPIO_SHORT_AN_OPEN_FLT[ANx_OPEN] bits

Table 61. FAULT2_STATUS*...continued*

GPIO_SHORT_FLT	Description	GPIO short detection
	0	No short detected
	1	Short detected in one or more of the seven GPIOs
	Reset condition	POR / Clear on write 0 all GPIO_SHORT_AN_OPEN_FLT (GPIOx_SH) bits
CB_SHORT_FLT	Description	Cell balance short-circuit detection
	0	No short-circuit detected
	1	On state short-circuit detected in one or more of the 6 cell balancing switches
	Reset condition	POR / Clear on write 0 all CB_SHORT_FLT[CBx_SHORT] bits
CB_OPEN_FLT	Description	Cell balancing open load detection
	0	No cell balance open load detected
	1	Off state open load detected in one or more of the 6 cell balancing switches
	Reset condition	POR / Clear on write 0 all CB_OPEN_FLT[CBx_OPEN] bits
OSC_ERR_FLT	Description	Low-power oscillator error
	0	No error
	1	The low-power oscillator frequency is out of range
	Reset condition	POR / Clear on write 0
DED_ERR_FLT	Description	ECC error, double error detection
	0	No error
	1	A double error has been detected in the fuses
	Reset condition	POR / Clear on write 0
FUSE_ERR_FLT	Description	Error in the loading of fuses
	0	No error
	1	The lock bit was not set after loading, meaning transfer of the fuse values is aborted
	Reset condition	POR / Clear on write 0

[1] w0c: write 0 to clear
[2] Ignore if FAULT2_STATUS[VANA_UV_FLT] is set

11.26 Fault status register 3 – FAULT3_STATUS

Table 62. FAULT3_STATUS

FAULT3_STATUS																
$26	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write		w0c[1]	w0c[1]								w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	CC_ OVR_ FLT	DIAG_ TO_FLT	VCP_UV	0	0	0	0	0	0	0	EOT_CB6	EOT_CB5	EOT_CB4	EOT_CB3	EOT_CB2	EOT_CB1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CC_OVR_FLT	Description	Overflow indicator on the COULOMB_CNT1,2[COULOMB_CNT] or CC_NB_SAMPLES
	0	No error
	1	COULOMB_CNT1,2[COULOMB_CNT] or CC_NB_SAMPLES went in overflow
	Reset condition	POR / Clear On Write 0 CC_P_OVF,CC_N_OVF, SAMP_OVF and CC_OVT
DIAG_TO_FLT	Description	Timeout of diagnostic state
	0	No timeout
	1	The system has exited itself from diagnostic state after timeout
	Reset condition	POR / Clear on write 0
VCP_UV	Description	VCP undervoltage detection[2]
	0	No undervoltage detected
	1	Undervoltage detected on VCP supply
	Reset condition	POR / Clear on write 0
EOT_CBx	Description	End of time cell balancing notification – indicates when a cell balance timer has expired and driver has been shutoff
	0	Cell balance timer has not timed out
	1	Cell balance timer has timed out
	Reset condition	POR / Clear on write 0

[1] w0c: write 0 to clear
[2] Ignore if FAULT2_STATUS[VANA_UV_FLT] is set

11.27 Fault mask register 1 – FAULT_MASK1

The FAULT_MASK1 register allows the user to selectively mask fault bits associated to the FAULT1_STATUS register. Masking a certain fault bit has the effect of preventing this bit from activating the FAULT output pin.

Table 63. FAULT_MASK1

FAULT_MASK1																
$27	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write				MASK_ 12_F	MASK_ 11_F	MASK_ 10_F	MASK_ 9_F	MASK_ 8_F	MASK_ 7_F	MASK_ 6_F	MASK_ 5_F	MASK_ 4_F	MASK_ 3_F	MASK_ 2_F	MASK_ 1_F	MASK_ 0_F
Read	0	0	0													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MASK_x_F	Description	Prevent the corresponding flags in FAULT1_STATUS to activate the FAULT pin
	0	The flag in position x activates the FAULT pin
	1	No activation
	Reset condition	POR

11.28 Fault mask register 2 – FAULT_MASK2

The FAULT_MASK2 register allows the user to selectively mask fault bits associated to the FAULT2_STATUS register. Masking a certain fault bit has the effect of preventing this bit from activating the FAULT output pin.

Table 64. FAULT_MASK2

FAULT_MASK2																
$28	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	MASK_15_F	MASK_14_F	MASK_13_F	MASK_12_F	MASK_11_F	MASK_10_F	MASK_9_F			MASK_6_F	MASK_5_F	MASK_4_F	MASK_3_F	MASK_2_F	MASK_1_F	MASK_0_F
Read								0	0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MASK_x_F	Description	Prevent the corresponding flags in FAULT2_STATUS to activate the FAULT pin
	0	The flag in position x activates the FAULT pin
	1	No activation
	Reset condition	POR

11.29 Fault mask register 3 – FAULT_MASK3

The FAULT_MASK3 register allows the user to selectively mask fault bits associated to the FAULT3_STATUS register. Masking a certain fault bit has the effect of preventing this bit from activating the FAULT output pin.

Table 65. FAULT_MASK3

FAULT_MASK3																
$29	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	MASK_15_F	MASK_14_F	MASK_13_F								MASK_5_F	MASK_4_F	MASK_3_F	MASK_2_F	MASK_1_F	MASK_0_F
Read				0	0	0	0	0	0	0						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MASK_x_F	Description	Prevent the corresponding flags in FAULT3_STATUS to activate the FAULT pin
	0	The flag in position (x) activates the FAULT pin
	1	No activation
	Reset condition	POR

11.30 Wake-up mask register 1 – WAKEUP_MASK1

The WAKEUP_MASK1 register disables wake-up events related to several FAULT1_STATUS fault bits. If a certain bit contained in the latter register is not masked by the corresponding bit of the former register, the IC transitions from Sleep mode to Normal mode.

Table 66. WAKEUP_MASK1

WAKEUP_MASK1																
$2A	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write				MASK_12_F	MASK_11_F				MASK_7_F			MASK_4_F	MASK_3_F	MASK_2_F	MASK_1_F	MASK_0_F
Read	0	0	0			0	0	0		0	0					
Reset	0	0	0	1	1	0	0	0	1	0	0	1	1	1	1	1

MASK_x_F	Description	Prevent the corresponding flags in FAULT1_STATUS to wake-up the device
	0	The flag in position (x) wakes the device up, when active
	1	No wake-up is possible by this source
	Reset condition	POR

11.31 Wake-up mask register 2 – WAKEUP_MASK2

The WAKEUP_MASK2 register disables wake-up events related to several FAULT2_STATUS fault bits. If a certain bit contained in the latter register is not masked by the corresponding bit of the former register, the IC transitions from Sleep mode to Normal mode.

Table 67. WAKEUP_MASK2

WAKEUP_MASK2																
$2B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	MASK_15_F	MASK_14_F	MASK_13_F	MASK_12_F	MASK_11_F	MASK_10_F	MASK_9_F	MASK_8_F			MASK_5_F	MASK_4_F		MASK_2_F	MASK_1_F	
Read									0	0			0			0
Reset	1	1	1	1	1	1	1	1	0	0	1	1	0	1	1	0
MASK_x_F	Description	Prevent the corresponding flags in FAULT2_STATUS to wake-up the device														
	0	The flag in position (x) wakes the device, when active														
	1	No wake-up is possible by this source														
	Reset condition	POR														

11.32 Wake-up mask register 3 – WAKEUP_MASK3

The WAKEUP_MASK3 register disables wake-up events related to several FAULT3_STATUS fault bits. If a certain bit contained in the latter register is not masked by the corresponding bit of the former register, the IC transitions from Sleep mode to Normal mode.

Table 68. WAKEUP_MASK3

WAKEUP_MASK3																
$2C	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	MASK_15_F		MASK_13_F								MASK_5_F	MASK_4_F	MASK_3_F	MASK_2_F	MASK_1_F	MASK_0_F
Read		0		0	0	0	0	0	0	0						
Reset	1	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1
MASK_x_F	Description	Prevent the corresponding flags in FAULT3_STATUS to wake-up the device														
	0	The flag in position (x) wakes the device, when active														
	1	No wake-up is possible by this source														
	Reset condition	POR														

11.33 Coulomb count number of samples register – CC_NB_SAMPLES

The CC_NB_SAMPLES register contains the 16-bit value, which represents the number of samples accumulated in the coulomb counter at the moment of copying its value to the COULOMB_CNT registers.

Table 69. CC_NB_SAMPLES

CC_NB_SAMPLES																
$2D	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	CC_NB_SAMPLES															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CC_NB_SAMPLES	Description	Number of samples accumulated for the coulomb count value														
	Reset condition	POR / ADC_CFG[CC_RST]														

11.34 Coulomb count register – COULOMB_CNT

The COULOMB_CNT register contains the current 32-bit value of the accumulated current samples. Data representation is signed two's complement, with V_{2RES} resolution. Division of ΔCOULOMB_CNT by ΔCC_NB_SAMPLES provides the average current, where the operator Δ denotes the variation over two different readings of a state. Subsequent multiplication by the corresponding elapsed time Δt provides the charge flowed out/in of the battery.

Table 70. COULOMB_CNT1

COULOMB_CNT1																
$2E	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	COULOMB_CNT_MSB															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
COULOMB_CNT_MSB	Description		Coulomb counting accumulator													
	Reset condition		POR / ADC_CFG[CC_RST]													

Table 71. COULOMB_CNT2

COULOMB_CNT2																
$2F	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	COULOMB_CNT_LSB															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
COULOMB_CNT_LSB	Description		Coulomb counting accumulator													
	Reset condition		POR / ADC_CFG[CC_RST]													

11.35 Current measurement registers – MEAS_ISENSE1 and MEAS_ISENSE2

The MEAS_ISENSEx registers contain the signed two's complement value of the battery current measured on demand.

Table 72. MEAS_ISENSE1

MEAS_ISENSE1																
$30	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	DATA_RDY	MEAS_I _MSB														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DATA_RDY	Description		This bit is set when the conversion is complete and the register is updated. The DATA_RDY bit is cleared when a request to convert is received either through the SOC or GPIO2 convert trigger													
	0		A new sequence of conversions is currently running													
	1		A data is available in MEAS_ISENSE1													
	Reset condition		POR													
MEAS_I_MSB	Description		ISENSE value, compensated in gain and temp, signed													
	Reset condition		POR													

Table 73. MEAS_ISENSE2

MEAS_ISENSE2																
$31	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write									w0c[1]	w0c[1]						
Read	DATA_RDY	0	0	0	0	0	PGA_GAIN		ADC2_SAT	PGA_GCHANGE	0	0	MEAS_I _LSB			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DATA_RDY	Description	This bit is set when the conversion is complete and the register is updated. The DATA_RDY bit is cleared when a request to convert is received either through the SOC or GPIO2 convert trigger
	0	A new sequence of conversions is currently running
	1	Data is available in MEAS_ISENSE2
	Reset condition	POR
PGA_GAIN	Description	Report the current gain of the ADC2 programmable gain amplifier (automatically settled or not)
	0 0	4
	0 1	16
	1 0	64
	1 1	256
	Reset condition	POR
ADC2_SAT	Description	ADC2 saturation information
	0	No saturation reported
	1	ADC2 has saturated during the ISENSE on-demand conversion
	Reset condition	POR / Clear on write 0
PGA_GCHANGE	Description	PGA gain change information during ISENSE on-demand conversion
	0	No gain change during ISENSE on-demand measurement; result is accurate
	1	The PGA gain has changed between the two chopped measurements
	Reset condition	POR / Clear on write 0
MEAS_I _LSB	Description	ISENSE value, compensated in gain and temp, signed
	Reset condition	POR

[1] w0c: write 0 to clear

11.36 Measurement registers – MEAS_xxxx

The MEAS_xxxx registers contain the measured values as a result of on-demand conversions. Note that the cyclic conversions leave no trace in these registers, as they are only used to update the OV/UV/OT/UT flags and other status information.

Table 74. MEAS_xxxx

MEAS_xxxx																
$32 and $3B to $4A	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	DATA_RDY	MEAS_xxxx														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DATA_RDY	Description	This bit is set when the conversion is complete and the register is updated. The DATA_RDY bit is cleared when a request to convert is received either through the SOC or GPIO2 convert trigger
	0	A new sequence of conversions is currently running
	1	A data is available in MEAS_xxxx
	Reset condition	POR
MEAS_xxxx	Description	Value is unsigned, resolution is $V_{CT\_ANx\_RES}$ independently on the selected resolution of ADC_CFG
	Reset condition	POR

11.37 Overvoltage undervoltage threshold register – TH_ALL_CT

Resolution for OV threshold and UV threshold are, respectively, $V_{CTOV(TH)}$ and $V_{CTUV(TH)}$.

Table 75. TH_ALL_CT

TH_ALL_CT																
$4B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	ALL_CT_OV_TH								ALL_CT_UV_TH							
Read																
Reset	1	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0
ALL_CT_OV_TH	Description		Overvoltage threshold setting for all cell terminals. Enabled through register OV_UV_EN													
	11010111		Default overvoltage threshold set to 4.2 V													
	Reset condition		POR													
ALL_CT_UV_TH	Description		Undervoltage threshold setting for all cell terminals. Enabled through register OV_UV_EN													
	10000000		Default undervoltage threshold set to 2.5 V													
	Reset condition		POR													

11.38 Overvoltage undervoltage threshold register – TH_CTx

Table 76. TH_CTx

TH_CTx																
$4C to $59	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	CTx_OV_TH								CTx_UV_TH							
Read																
Reset	1	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0
CTx_OV_TH	Description		Overvoltage threshold setting for individual cell terminals. OV_UV_EN[COMMON_OV_TH] bit must be logic 0 and OV_UV_EN[CTx_OVUV_EN] bit must be logic 1 to use TH_CTx register as threshold													
	11010111		Default overvoltage threshold set to 4.2 V													
	Reset condition		POR													
CTx_UV_TH	Description		Undervoltage threshold setting for individual cell terminals. OV_UV_EN[COMMON_UV_TH] bit must be logic 0 and OV_UV_EN[CTx_OVUV_EN] bit must be logic 1 to use TH_CTx register as threshold													
	10000000		Default undervoltage threshold set to 2.5 V													
	Reset condition		POR													

11.39 Overtemperature, undertemperature threshold registers – TH_ANx_OT, TH_ANx_UT

Registers TH_ANx_OT and TH_ANx_UT contain the individually programmed overtemperature and undertemperature value for each analog input.

Table 77. TH_ANx_OT

TH_ANx_OT																
$5A to $60	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write							ANx_OT_TH									
Read	0	0	0	0	0	0										
Reset	0	0	0	0	0	0	0	0	1	1	1	0	1	1	0	1
ANx_OT_TH	Description		Overtemperature threshold setting for analog input x													
	0011101101		Overtemperature default set to 1.16 V													
	Reset condition		POR													

Table 78. TH_ANx_UT

TH_ANx_UT																
$61 to $67	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write							ANx_UT_TH									
Read	0	0	0	0	0	0										
Reset	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	0
ANx_UT_TH	Description		Undertemperature threshold setting for analog input x													
	1100001110		Undertemperature default set to 3.82 V													
	Reset condition		POR													

11.40 Overcurrent threshold register – TH_ISENSE_OC

Registers TH_ISENSE_OC contains the programmed overcurrent threshold in sleep mode.

Table 79. TH_ISENSE_OC

TH_ISENSE_OC																
$68	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write					TH _ISENSE_OC											
Read	0	0	0	0												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TH_ISENSE_OC	Description		Sleep mode ISENSE overcurrent threshold, unsigned. Resolution is 1.2 μV/LSB													
	Reset condition		POR													

11.41 Over coulomb counter threshold registers – TH_COULOMB_CNT

The coulomb counter threshold in sleep mode is given by the following two registers.

Table 80. TH_COULOMB_CNT_MSB

TH_COULOMB_CNT_MSB																
$69	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	TH_COULOMB_CNT_MSB															
Read																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TH_COULOMB_ CNT_MSB	Description		Over coulomb counting accumulator threshold (MSB)													
	Reset condition		POR													

Table 81. TH_COULOMB_CNT_LSB

TH_COULOMB_CNT_LSB																
$6A	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	TH_COULOMB_CNT_LSB															
Read																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TH_COULOMB_ CNT_LSB	Description		Over coulomb counting accumulator threshold (LSB). Resolution is V_{2RES}													
	Reset condition		POR													

11.42 Silicon revision register – SILICON_REV

Table 82. SILICON_REV

SILICON_REV																
$6B	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	0	0	0	0	0	0	0	0	0	FREV				MREV		
Reset	0	0	0	0	0	0	0	0	0	F	F	F	F	M	M	M

FREV	Description	Full mask revision
	0001	Pass 1.x
	0010	Pass 2.x
	…	
	Reset condition	POR
MREV	Description	Metal mask revision
	000	Pass y.0
	001	Pass y.1
	…	
	Reset condition	POR

11.43 EEPROM communication register - EEPROM_CTRL

Table 83. EEPROM_CTRL

EEPROM_CTRL																
$6C	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	R/W	EEPROM_ADD							DATA_TO_WRITE							
Read	BUSY	ERROR	EE_PRESENT	0	0	0	0	0	READ_DATA							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

R/W	Description	Read/write bit, directs the MC33772C to read or write from EEPROM
	0	Write
	1	Read
	Reset condition	POR
EEPROM_ADD	Description	EEPROM address to read or write
	Reset condition	POR
DATA_TO_WRITE	Description	Data to be written into the EEPROM
	Reset condition	POR
BUSY	Description	Busy bit
	0	Indicates the IC has completed the EEPROM read or write operation
	1	Indicates the IC is in the process of performing the EEPROM read or write operation
	Reset condition	POR
ERROR	Description	EEPROM communication error bit.
	0	No error occurred during the communication to EEPROM
	1	An error occurred during the communication to EEPROM
	Reset condition	POR
EE_PRESENT	Description	EEPROM detection
	0	No EEPROM detected
	1	EEPROM has been detected and present
	Reset condition	POR
READ_DATA	Description	Data read in the EEPROM at address given by EEPROM_ADD
	Reset condition	POR

11.44 ECC signature 1 register

Table 84. DED_ENCODE1

DED_ENCODE1																
$6D	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	DED_HAMMING_COUT1_23_8															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DED_HAMMING_COUT1_23_8	Description	Reports the 16 MSBits to encode in the fuse matrix (ECC)														
	Reset condition	POR														

11.45 ECC signature 2 register

Table 85. DED_ENCODE2

DED_ENCODE2																
$6E	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write																
Read	DED_HAMMING_COUT_1_7_0								0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DED_HAMMING_COUT_1_7_0	Description	Report the 16 LSBits to encode in the fuse matrix (ECC)														
	Reset condition	POR														

11.46 FUSE mirror and data control

Table 86. FUSE_MIRROR_DATA

FUSE_MIRROR_DATA																
$6F	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	FMR_DATA															
Read	FMR_DATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FMR_DATA	Description	Fuse mirror data to read or write														
	Reset condition	POR														

Table 87. FUSE_MIRROR_CNTL

FUSE_MIRROR_CNTL																
$70	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	w0c[1]			FMR_ADDR									FSTM	FST		
Read	SEC_ERR_FLT	0	0	FMR_ADDR					0	0	0	0	0	FST_ST		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SEC_ERR_FLT	Description	ECC error, single error correction														
	0	No error														
	1	A single error has been detected and corrected. The IC is usable, must not be considered defective														
	Reset condition	POR / Clear on write 0														
FMR_ADDR	Description	Fuse mirror register address														
	Reset condition	POR														
FSTM	Description	Fuse state write mask. This bit controls the write access to the FST[2:0] bits														
	0	Writing in FST bits has no effect														
	1	FST bits are unlocked for writing														
	Reset condition	POR														

Table 87. FUSE_MIRROR_CNTL*...continued*

FST	Description	Fuse state control. write to this register controls the switching of the fuse state machine. Read in this register enables tracing the current state
	0 0 0	Refer to Mirror memory access for bit description
	Reset condition	POR
FST_ST	Description	Fuse state control. Read in this register enables to trace the current state
	0 0 0	Refer to Mirror memory access for bit description
	Reset condition	POR

[1] w0c: write 0 to clear

11.47 Reserved

Table 88. RESERVED

Reserved																
$00, $12 to $19, $33 to $3A, $4C to $53, $71 to $7F	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write	do not change															
Read																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.48 Fuse bank

Table 89. FUSE_BANK

Bank address	Data															
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
$00	GCF_cold_c5						GCF_room_c5									
$01	GCF_cold_c3						GCF_room_c3									
$02	GCF_hot_c5						GCF_room_c1									
$03	hot_c6vs5 [2]	GCF_hot_i4					GCF_hot_i256					GCF_cold_i256				
$04	hot_c6vs5 [1]	GCF_cold_i4					GCF_hot_i64					GCF_cold_i64				
$05	hot_c6vs5 [0]	GCF_ANx_ratio					GCF_hot_i16					GCF_cold_i16				
$06	room_c2vs1				cold_c2vs1					GCF_hot_c1						
$07	GCF_IcTemp				hot_c2vs1					GCF_cold_c1						
$08	room_c6vs5		cold_c6vs5		hot_c4vs3			cold_c4vs3		GCF_stack						
$09	GCF_cold_Vbgtj2							GCF_i256								
$0A	GCF_cold_Vbgtj1							GCF_i64								
$0B	GCF_hot_Vbgtj2							GCF_i16								
$0C	GCF_hot_Vbgtj1							GCF_i4								
$0D	GCF_room_Vbgtj2								GCF_room_Vbgtj1							
$0E	DED_ENCODE2								GCF_hot_c3						room_c4vs3	
$0F	DED_ENCODE1															
$10	Traceability															
$11	Traceability															
$12	Reserved											Traceability				

12 Safety

12.1 Safety features

MC33772C was developed as a Safety Element out of Context (SEooC). All the assumptions of use taken into account are described in the Safety Manual.

MC33772C has been developed to be ASIL-C Qualified. Nevertheless, the MC33772C can be employed within systems performing up to ASIL-D functions, because the MC33772C can support to achieve the corresponding ISO 26262 HW architectural metrics. This holds true only if the system integrator uses all safety mechanisms recommended in the Safety Manual, under the stated conditions of use and the fulfillment of the assumed general and specific requirements stated therein.

Diagnostics and safety features of the device are not described in the present document. To know about them, the user is referred to the MC33772C Safety Manual, whose information content is essential for any safety related application.

13 Typical applications

13.1 Introduction

NXP Semiconductors has developed a battery cell controller IC supporting both centralized and distributed battery management architectures. Centralized battery monitoring systems contain a controller module sensing individual differential cell voltages through a wiring harness. Distributed systems locate monitoring devices close to the lithium-ion batteries and use a communication interface to transfer data to the main controller MCU.

There are significant advantages to using transformers for isolation and communication. The most obvious benefit of the pulse transformers is the high degree of voltage isolation. Transformers specified in this document are automotive qualified and rated at 3750 Vrms. Using pulse transformers allow the NXP battery management system to achieve communication rates of 2.0 Mbit/s with very low radiated emissions.

An added benefit to the transformer daisy chain network is the ability to loop the network back to the pack controller. This feature allows the user to verify communication to each node in the daisy chain.

13.1.1 Centralized battery management system

A centralized system is comprised of a single transformer driver with a transformer or capacitive isolation between each battery cell controller IC.

The centralized battery monitoring system using capacitive isolation is shown in Figure 33.

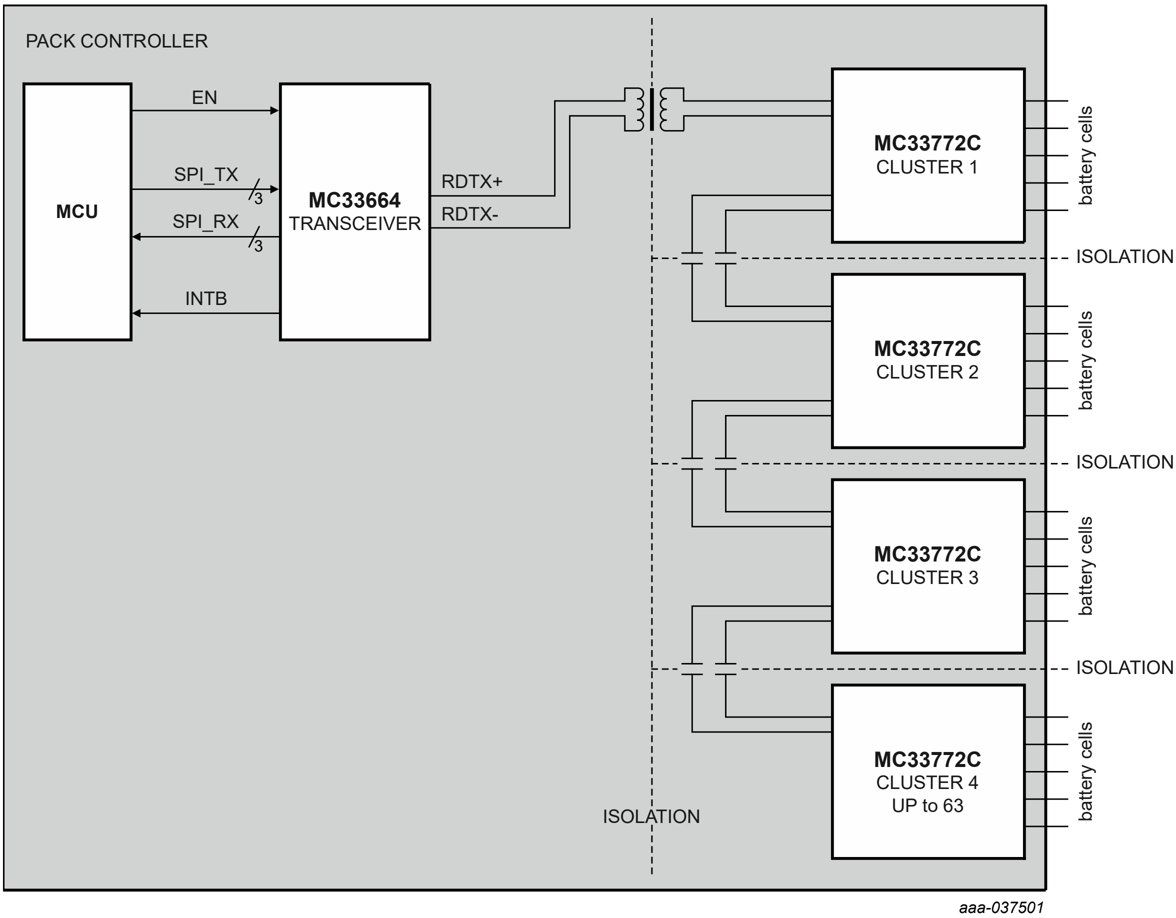


Figure 33. Centralized battery monitoring system with capacitive isolation

The centralized battery monitoring system using transformer isolation is shown in Figure 34.

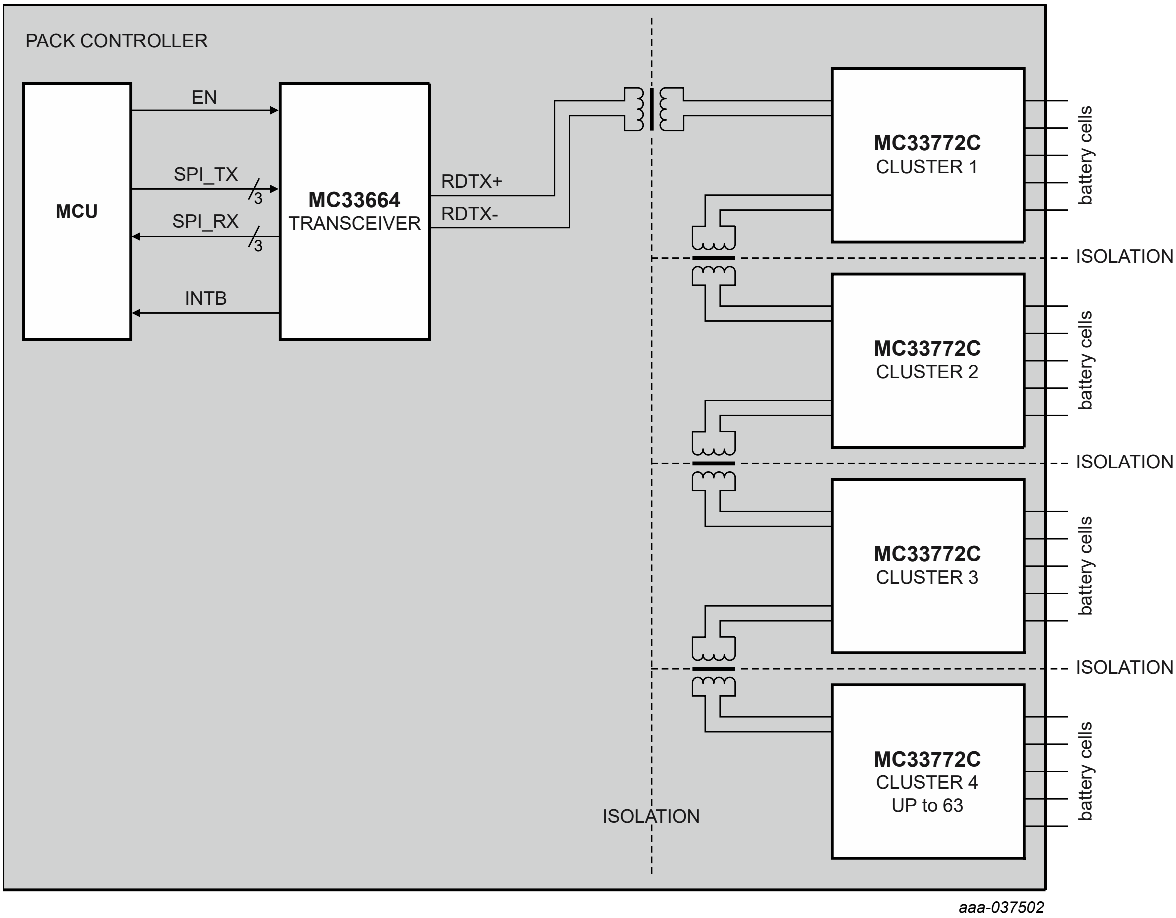


Figure 34. Centralized battery monitoring system with transformer isolation

13.1.2 Distributed battery management system

The distributed battery management solution is identical to the centralized system with an additional transformer and daisy chain cable in the pack controller and between each node.

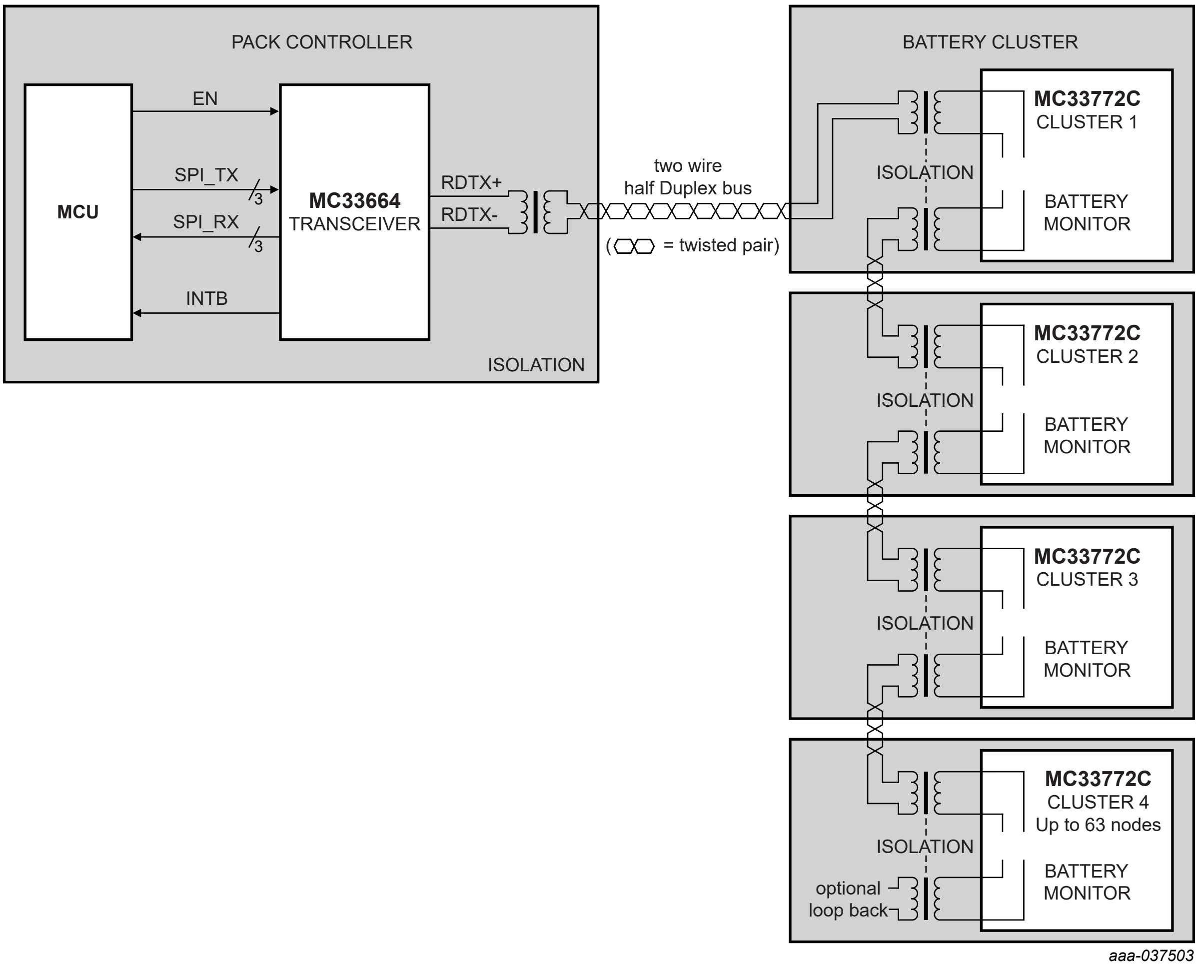


Figure 35. Distributed battery monitoring system

13.1.3 Multiple daisy chain

In a distributed system, the MC33772C ICs can be connected in multiple daisy chains. The number of daisy chains supported by the MC33772C IC is configurable with the MSB of the INIT[CID] register. Using one bit MSB of CID supports two daisy chains with up to 31 slave devices in each daisy chain. Similarly, using two bit MSB of CID supports 4 daisy chains with up to 15 slave devices in each daisy chain.

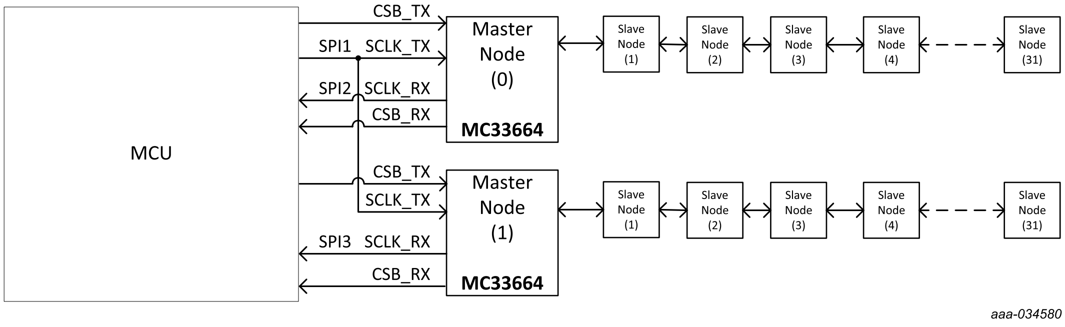


Figure 36. Example of multiple daisy chain.

13.1.4 Loop-Back daisy chain

In a distributed system, the MC33772C IC can also support a loop-back daisy chain with two master nodes connected at two SPI ports of the MCU. The slave devices are connected at each end of the master nodes as shown in the figure.

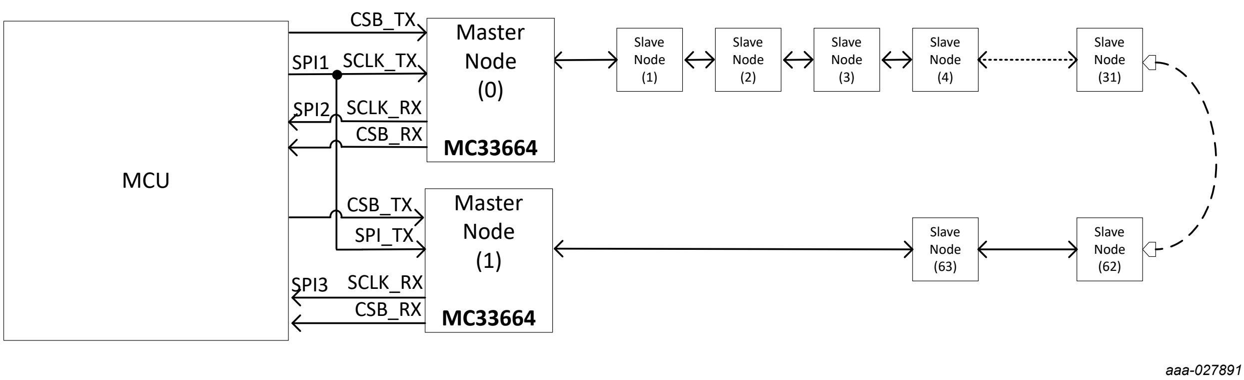


Figure 37. Example of loop-back daisy chain.

Note: *In the case of a loop-back daisy chain configuration, the MCU shall use only one master node at a time for communicating with the MC33772C IC.*

Note: *If multiple daisy chains are used in case of loop-back daisy chain communication, then two master nodes forming one complete loop are to be assigned with one daisy chain address.*

13.2 MC33772C External Components

This section provides information about recommended external components and how to select them.

13.2.1 Cell terminal filters

Figure 38 and Figure 42 show the recommended second order low-pass filters for cell voltages.

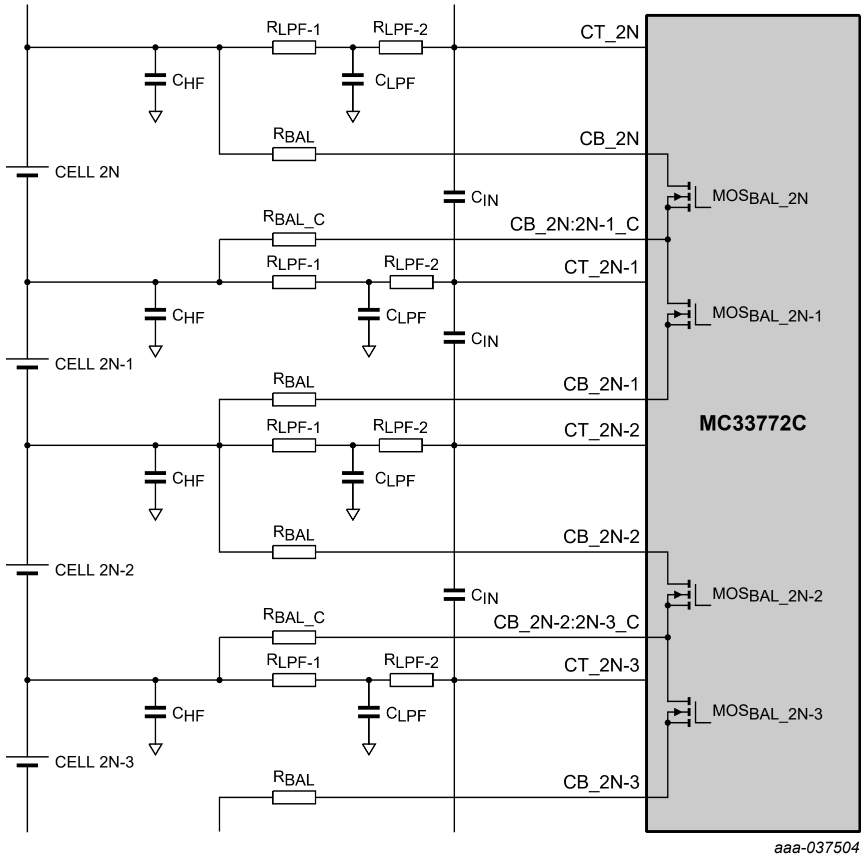


Figure 38. Second order cell terminal filters and cell balancing resistors (internal cell balancing MOSFETs are shown for clarity)

Table 90. CT filter components

ID	Value	Units	Comments
C_{HF}	0.047	μF	Value used and tested at NXP Semiconductors to withstand ESD gun and hot plug
R_{LPF-1}	3	kΩ	Value used and tested to withstand hot plug at NXP. Low-pass filter resistor R_{LPF-1} together with C_{LPF} determine the filter cut-off frequency. This value must not be changed. Component tolerance depends on the wanted accuracy for the bandwidth. See Equation 1 and Equation 2
C_{LPF}	0.1	μF	This capacitance value together with R_{LPF-1} provides 530 Hz cut-off frequency. Value used and tested to withstand hot plug at NXP. Component tolerance depends on the wanted accuracy for the bandwidth. See Equation 1 and Equation 2
R_{LPF-2}	2	kΩ	Value used and tested to withstand hot plug at NXP. This value must not be changed. No special requirement for the tolerance of this component.
C_{IN}	0.01	μF	Value used and tested to withstand hot plug at NXP. This value must not be changed. No special requirement for the tolerance of this component

Table 90. CT filter components*...continued*

ID	Value	Units	Comments
R_{BAL}	X	Ω	Any value is possible, as long as the cell balance current does not exceed 300 mA
R_{BAL_C}	$R_{BAL}/5$	Ω	Maximum value

Using the arrangement shown in Figure 38, the filter cut-off frequency in Hz, depending on the measurement time constant τ, is given by the following formula.

$$f_{cut} = 1 / (2\pi\tau) \quad (1)$$

$$\tau = R_{LPF\text{-}1}\, C_{LPF} \quad (2)$$

For noisy applications, if the CTREF voltage cannot be kept within the limits described in Table 9 footnote , a setup of dual anti-parallel Schottky diodes can be added between the CTREF battery connector pin and the module ground to limit the voltage drop amplitude in transient. These diodes should be placed close to the corresponding Rlpf-1 resistor (CT_REF pin low pass filter).

13.2.2 Unused cells

If the cluster has less than the maximum number of cells, the usage of cell terminal pins CTx and cell balancing pins CBx has to satisfy some constraints. Each external LPF block is masked as shown in Figure 39, to simplify diagrams representation. A minimum of three cells must be used. At least cells connected to CT_REF/CT1, CT1/CT2 and CT5/CT6. Unused cells must start with CT3. Stacked cells arrangements from 3 to 6 cells are described in Table 91.

Note*: For more information, refer to AN12536.*

Table 91. Stacked cells

MC33772	Stacked cells			
Cell	6	5	4	3
1	CT_REF/CT1	CT_REF/CT1	CT_REF/CT1	CT_REF/CT1
2	CT1/CT2	CT1/CT2	CT1/CT2	CT1/CT2
3	CT2/CT3	CT3/CT4	CT4/CT5	CT5/CT6
4	CT3/CT4	CT4/CT5	CT5/CT6	—
5	CT4/CT5	CT5/CT6	—	—
6	CT5/CT6	—	—	—

Note:

- *CT3 is always populated with the full Low Pass Filter*
- *Other pins that are not used are shorted directly to CT3*

As a general rule, unused CTx have to be terminated to the positive of the cell connected to CT1/CT2 . This is also valid for 3 to 4 channels version of MC33772C. As shown, several external components may be removed. Cell balancing resistors (RBAL) of unused cells are to be mounted and terminated at the positive terminal of cell 2. Resistors for hot plug protection RLPF-2 must also be mounted.

Configuration with a number of cells 3, 4 or 5 leads to an application diagram analogous to Figure 40.

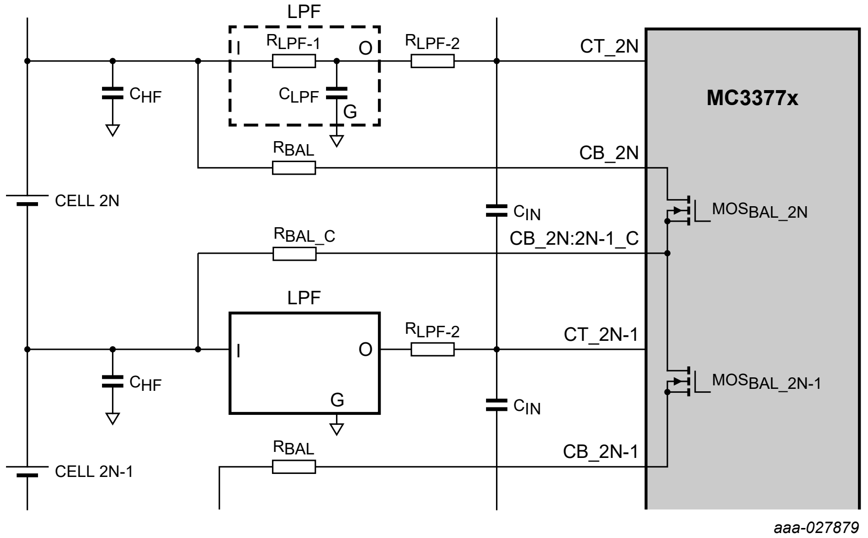


Figure 39. LPF block masking

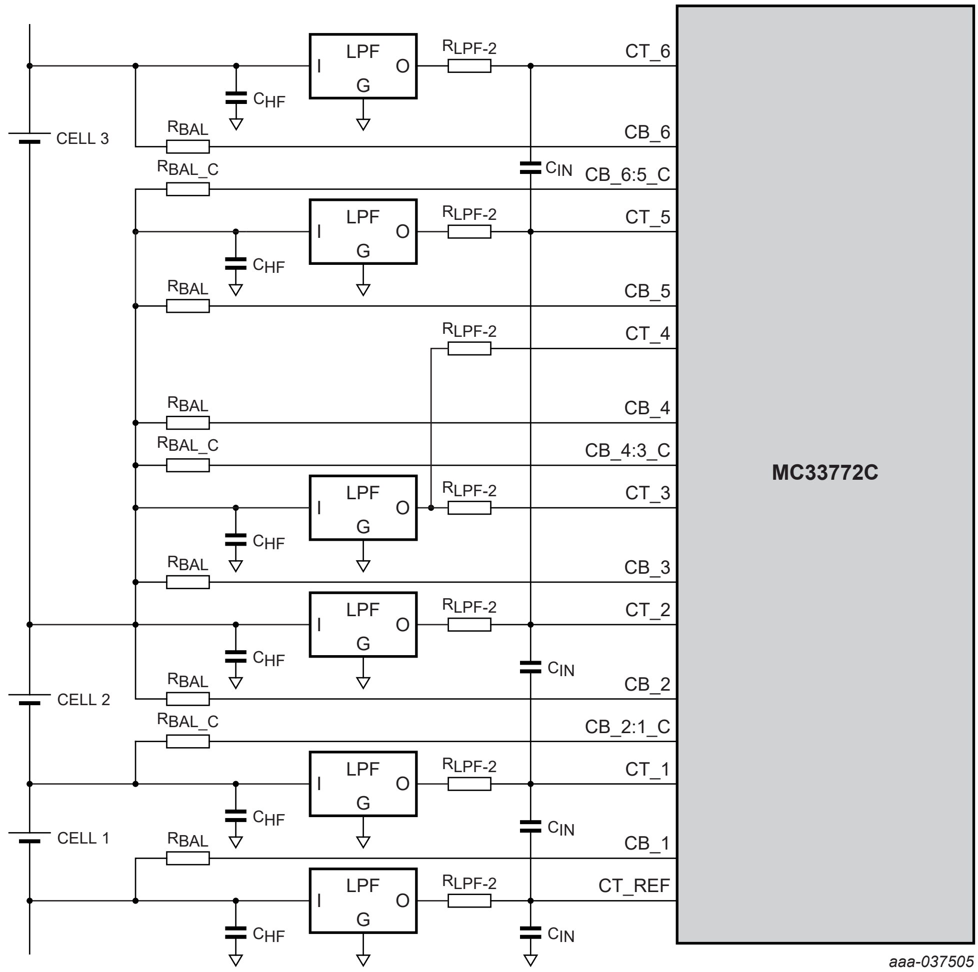


Figure 40. The three cell configuration

13.2.3 Hot plug protection

The VPWR line, shown in Figure 41, must be protected by a serial resistor in order to limit the inrush current and a parallel capacitor to filter fast voltage variation. A higher value of R_{VPWR} provides better protection. The drawback of higher R_{VPWR} is higher voltage drop. The minimum battery voltage (V_{BAT}) supplying the device through the R_{vpwr}resistor is then equal to Equation 3 . As the stack voltage is measured across VPWR1, 2 pins and ground, stack measurement is affected by such voltage drop. Furthermore, voltage drops higher than V_{VPWR_CT} have a negative impact on cell measurement accuracy.

$$\min\left(V_{\mathrm{BAT}}\right) = \max\left(V_{\mathrm{PWR(UV\_POR)}} + R_{\mathrm{vpwr}} * \left[\max\left(I_{\mathrm{VPWR(TPL\_TX)}}\right) + \max\left(I_{\mathrm{LIM\_VCOM(OC)}}\right) + \max\left(I_{\mathrm{LIM\_VANA(OC)}}\right)\right]\right) \quad (3)$$

In order to withstand hot plug, it is mandatory to use Zener diodes as shown in Figure 41 close to the VPWR line. In general, all components, whose values are given in Table 92, are mandatory to protect the IC when a connection is made to the battery pack. Changing the value of any external components listed in Table 92 may result in serious IC damage during the connection to the battery pack. Capability of the device to sustain random connection to live voltage for pins VPWRx, CT_x, CB_x, CTREF, GND, ISENSE+ and ISENSE– has been extensively evaluated. Nevertheless, the total number of random combinations related to those pins cannot be entirely tested. Therefore, despite all engineering efforts performed by NXP, it is the responsibility of the system provider to ensure safe connection to the battery pack.

Furthermore, it is the responsibility of the system provider to manage the risk of short circuits on any external components connected to the IC, including external low-pass filters. A short-circuit on the pins connected to the battery can lead to high current flowing through the IC, causing a thermal event on the PCB. The system provider must employ common practices, such as fuse protection on the VPWR line, series of capacitors on the CT pins, appropriate power rating for external resistors, or any other appropriate measure capable to mitigate hazards.

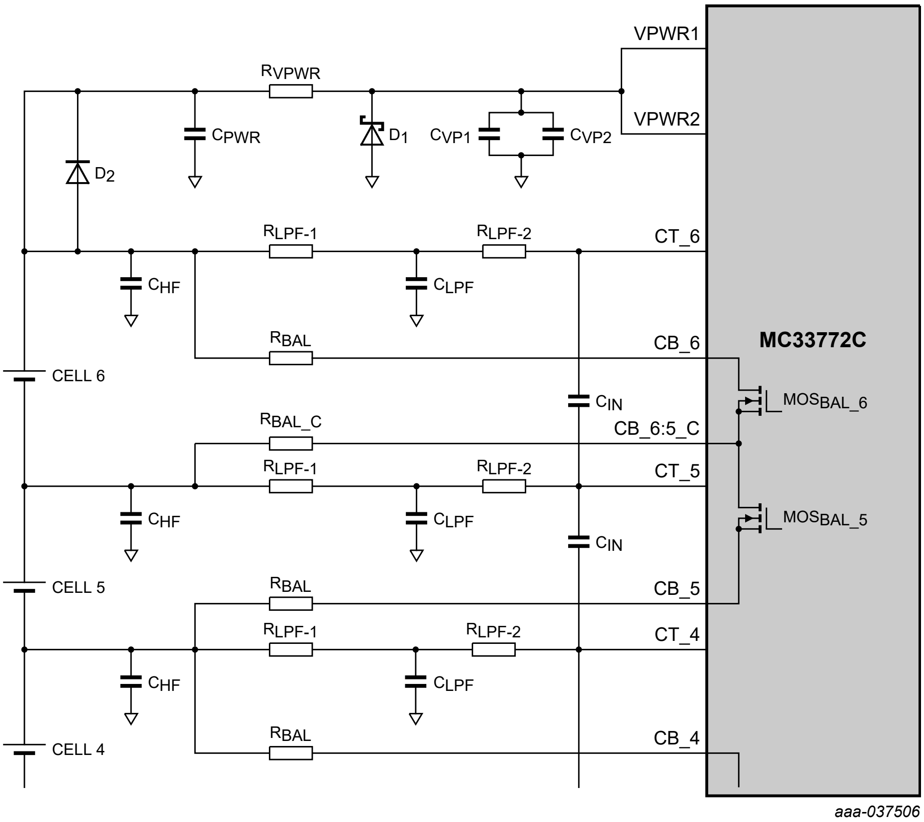


Figure 41. Top cell terminal filters and balancing resistors, VPWR1, 2 components to withstand hot plug

Table 92. Components to avoid hot plug issues

ID	Value	Units	Comments
D_2	1	A	To withstand hot plug when VPWR1/2 and CT_6 are set on different connector lines to connect to upper cell of the monitored cell stack, use specified forward current, e.g., PMEG10010ELR
D_1	39	V	To protect the IC against transient overvoltage, use the specified Zener voltage, e.g., BZT52H-B39
C_{PWR}	0.047	µF	Value used and tested at NXP to withstand hot plug. This value must not be exceeded
R_{VPWR}	6.8	Ω	Reducing the resistance value may jeopardize the hot plug capability. Power rating is 1/10 W
C_{VP1}	220	nF	To withstand hot plug, this value must not be changed
C_{VP2}	1	nF	Ceramic capacitor
R_{LPF2}	2	kΩ	To withstand hot plug, this value should not be decreased

13.2.4 Current channel filter

The current channel may be filtered as shown in Figure 42. Example component values are given in Table 93.

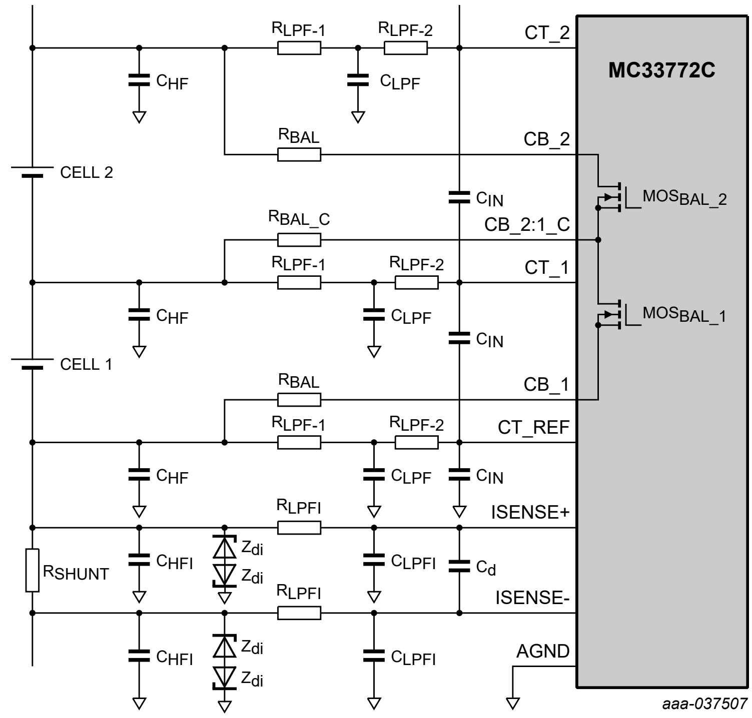


Figure 42. Bottom cell terminal filters, cell balancing components and current channel filter

Table 93. ISENSE filter components

ID	Value	Units	Comments
C_{HFI}	47	nF	This component serves to withstand ESD gun and its value must not be changed
R_{LPFI}	127	Ω	Warning: do not exceed 200 Ω. Use 5 % tolerance. Used value is to get both f_{CUTI} = 91.8 Hz and f_{ICM} = 26.67 kHz. See Equation 4, Equation 5, Equation 7, and Equation 8
C_d	6.8	µF	This example value has been chosen to get f_{CUTI} = 91.8 Hz and t_{DIAG} ≤ 31.7 ms. See Equation 4, Equation 5, and Equation 6. Use 5 % tolerance
C_{LPFI}	47	nF	Value is chosen in order to get: 91.8 Hz, t_{DIAG} ≤ 31.7 ms and f_{ICM} = 26.67 kHz. See Equation 4, Equation 5, Equation 6, Equation 7 and Equation 8. Use 5 % tolerance
ZDI	2.0	V	To protect during hot plug in case one of the ISENSE± pin is connected before GND of the device. Recommended MMSZ4679T1G

The signal cutoff frequency (in Hz) arrangement shown in Figure 42 of the current channel external filter depends on the measurement time constant τ_I given byEquation 5.

$$f_{cutI} = 1 / (2\pi\tau_I) \quad (4)$$

$$\tau_I = R_{LPFI}(C_{LPFI} + 2C_d) \quad (5)$$

The diagnostic time to detect an open from the shunt to the current filter arrangement shown in Figure 42, is given by:

$$t_{diag} = (C_{LPFI} + C_d)\frac{V_{ISENSE\text{-}OL} + |R_{shunt} I_{max}|}{I_{SENSE\text{-}OL}} \quad (6)$$

The current channel external filter arrangement shown in Figure 42 of the common mode cutoff frequency in Hz, depends on the measurement time constant τ_{Icm}, given by the following formula, whose numeric result should be selected one detected above the signal cutoff frequency.

$$f_{Icm} = 1 / (2\pi\tau_{Icm}) \quad (7)$$

$$\tau_{Icm} = R_{LPFI}\, C_{LPFI} \quad (8)$$

Above equations must be taken into account when considering the procedure to detect an open connection between ISENSE± and the input filter. Values for V_{ISENSE_OL} and I_{ISENSE_OL} are given in Table 9, values for the shunt resistance R_{SHUNT} and the maximum current I_{MAX} through it are application specific, while example values for the filter capacitors and resistors can be found in Table 93.

13.2.5 Temperature channels

Figure 43 shows usage of GPIOx as analog inputs (ANx) for temperature measurements. If not used, each GPIOx may be shorted to GND.

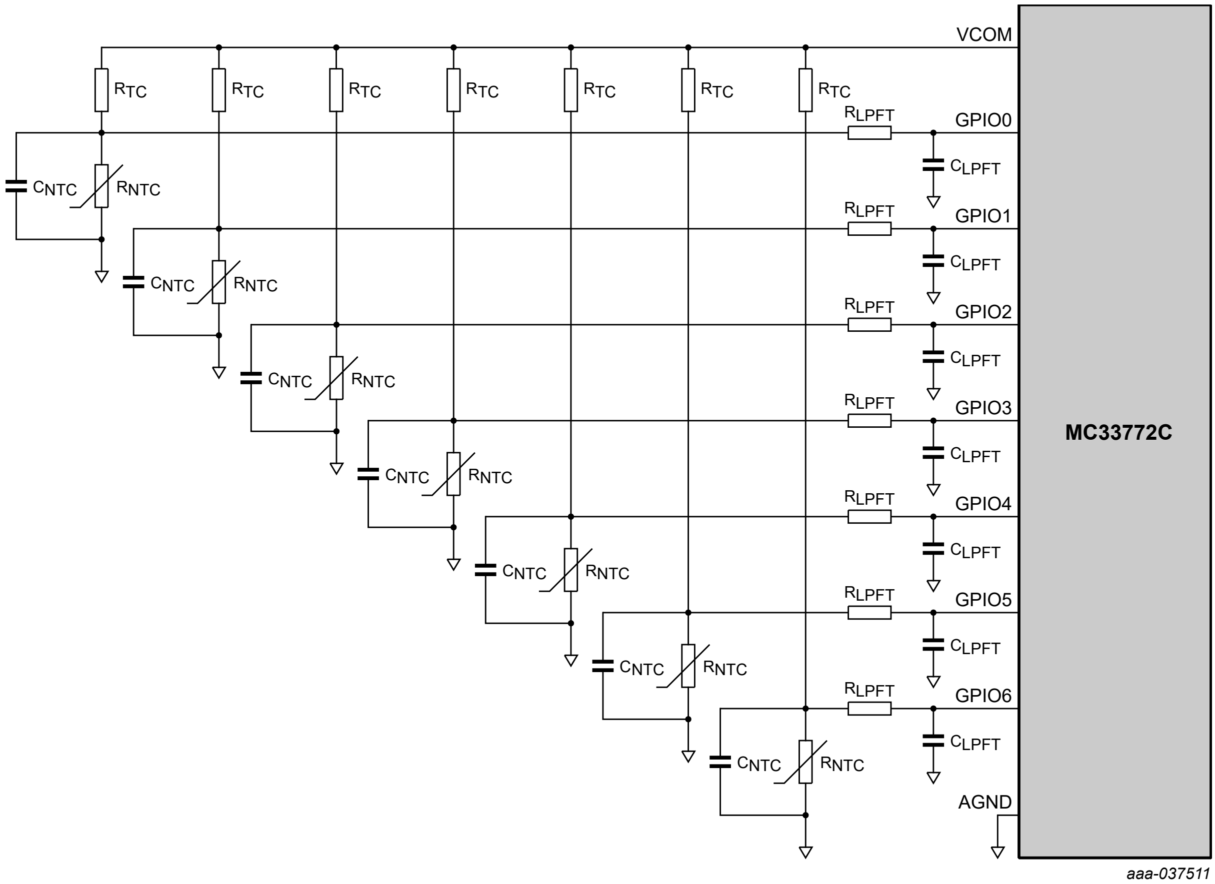


Figure 43. GPIOx used as ANx

Table 94. ANx filter components

ID	Value	Units	Comments
R_{TC}	6.8	kΩ	Component with 1 % tolerance, for accurate temperature measurement. Proposed value, together with all other proposed values, gives approximately f_{CUTT} = 10 kHz. See Equation 9, Equation 10, Equation 11, and Equation 12
R_{NTC}	10	kΩ	Nominal resistance value is given at 25 °C, tolerance must be 5 % or better
C_{NTC}	1.2	nF	This component is for ESD protection
R_{LPFT}	3.3	kΩ	Influences the channel bandwidth. See Equation 9, Equation 10, Equation 11, and Equation 12
C_{LPFT}	1.2	nF	5 % tolerance or better. Influences the channel bandwidth. See Equation 9, Equation 10, Equation 11, and Equation 12

The signal cutoff frequency (in Hz) for the arrangement shown in Figure 43 of GPIOx used as radiometric analog inputs, depends on the measurement time constant τ_T, given by the following formula. Ideally, the current channel should have the same bandwidth as cell voltage channels.

$$f_{cutT} = 1 \,/\, (2\pi\tau_T) \tag{9}$$

where,

$$\tau_T = max(\tau_1,\ \tau_2) \tag{10}$$

$$\tau_1 = (R_{LPFT} + (R_{TC}R_{NTC}) \,/\, (R_{TC} + R_{NTC}))C_{LPFT} \tag{11}$$

$$\tau_2 = C_{NTC}(R_{TC}R_{NTC}) \,/\, (R_{TC} + R_{NTC}) \tag{12}$$

In case the NTC resistor is located outside of the board and can be submitted to large EMC and ESD Gun constraints, the recommended filter for temperature is 2nd order as shown in Figure 44.

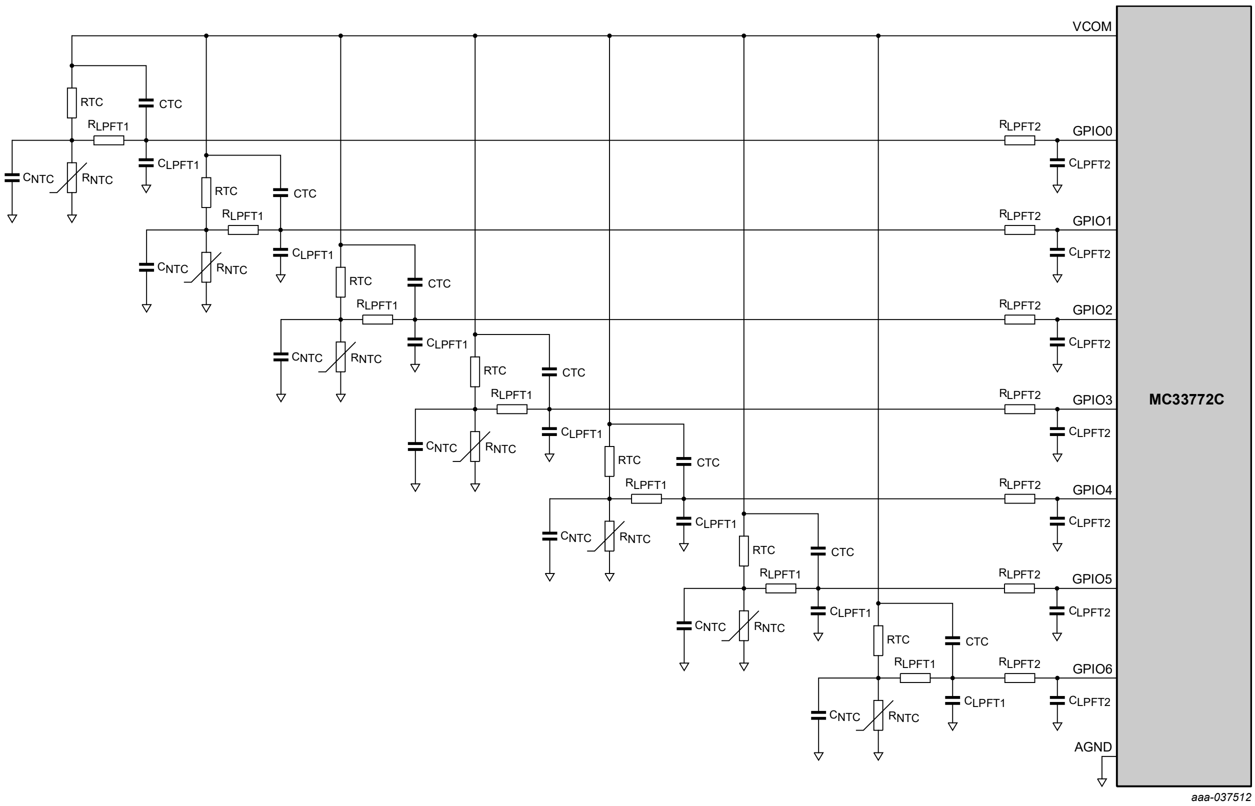


Figure 44. GPIOx used as ANX (with 2nd order filter)

Table 95. ANx second order filter components

ID	Value	Units	Comments
R_{TC}	6.8	kΩ	Component with 1 % tolerance, for accurate temperature measurement
C_{TC}	1.2	nF	
R_{NTC}	10	kΩ	Nominal resistance value is given at 25 °C, tolerance must be 5 % or better

Table 95. ANx second order filter components...*continued*

ID	Value	Units	Comments
C_{NTC}	1.2	nF	This component is for ESD protection
C_{LPFT1}	1.2	nF	5 % tolerance or better
R_{LPFT1}	3.3	kΩ	
C_{LPFT2}	1.2	nF	5 % tolerance or better
R_{LPFT2}	3.3	kΩ	

13.2.6 Centralized applications

13.2.6.1 Centralized applications - Transformer or capacitive isolation - Master node

For capacitive isolation in a centralized system the schematic is split into two segments. The first segment displays the external component of master node as shown in Figure 45. The second segment displays the external components between two MC33772C ICs as shown in Figure 46. In high voltage system applications, a high voltage isolation transformer is recommended between master node and first slave node.

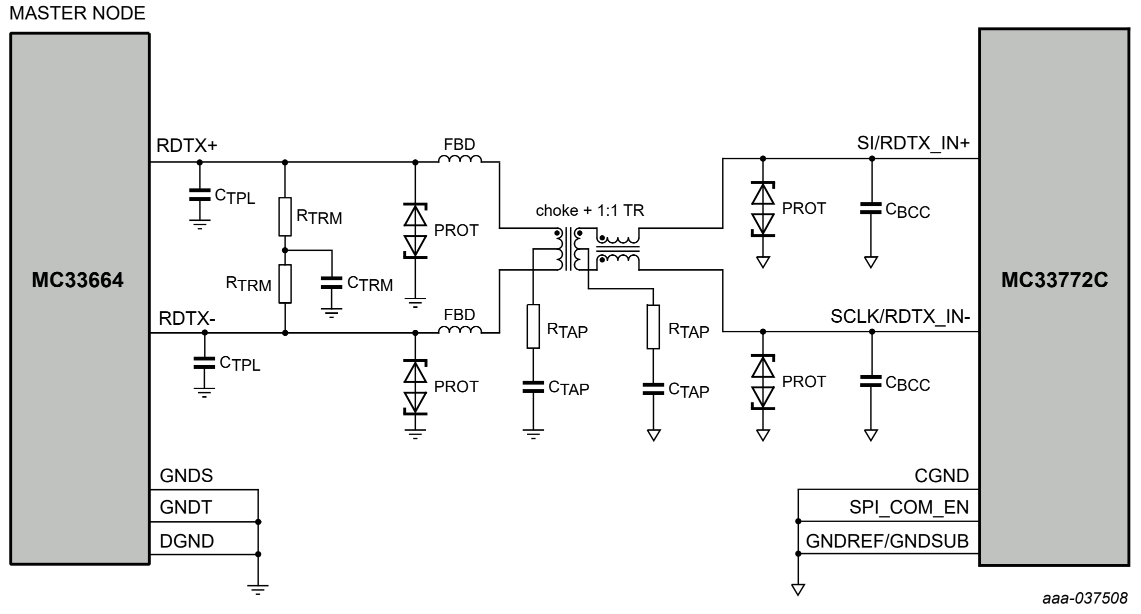


Figure 45. Master node in a centralized application with transformer isolation

Table 96. Master node components for a centralized application with transformer or capacitive isolation

ID	Value	Units	Comments
C_{TPL}	68	pF	Ceramic capacitor
C_{TRM}	4.7	nF	Ceramic capacitor for split termnination of MC33664
R_{TRM}	75	Ω	Split termination resistor for MC33664
PROT	8	V	ESD protection. Use PESD5VOV1BB or equivalent. The indicated voltage is the nominal breakdown voltage
R_{TAP}	150	Ω	Center tap resistor
C_{TAP}	10	nF	Center tap capacitor
C_{BCC}	220	pF	Ceramic capacitor

Table 96. Master node components for a centralized application with transformer or capacitive isolation...*continued*

ID	Value	Units	Comments
Choke +1:1 TR	Pulse Electronic HM2103	N/A	Single channel transformer with common mode choke
FBD	120	Ω	Ferrite Bead (optional). Use MMZ1608Y121BTD25 or equivalent

13.2.6.2 Centralized applications - Capacitive isolation - Slave node

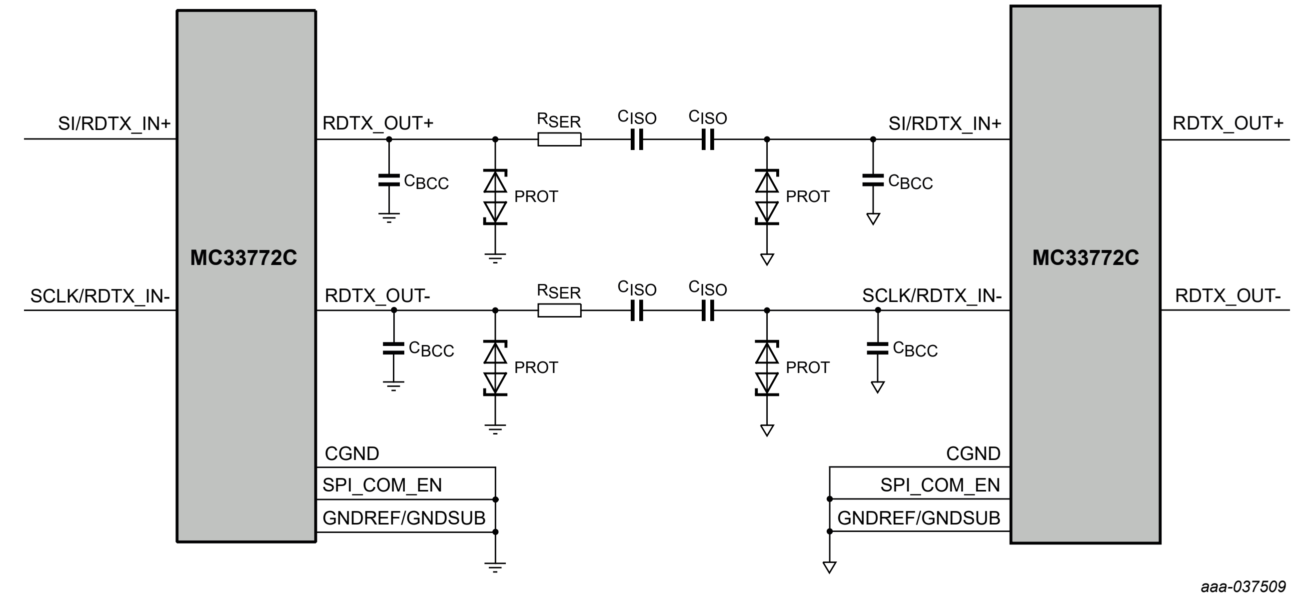


Figure 46. Slave node for a centralized application with capacitive isolation

Table 97. Slave node components for a centralized application with capacitive isolation

ID	Value	Units	Comments
C_{BCC}	22	pF	Ceramic capacitor
R_{SER}	62	Ω	Series resistance
C_{ISO}	10	nF	Isolation capacitor
PROT	8	V	ESD protection. Use PESD5V0V1BB or equivalent. The indicated voltage is the nominal breakdown voltage

13.2.6.3 Centralized applications - Transformer isolation - Slave node

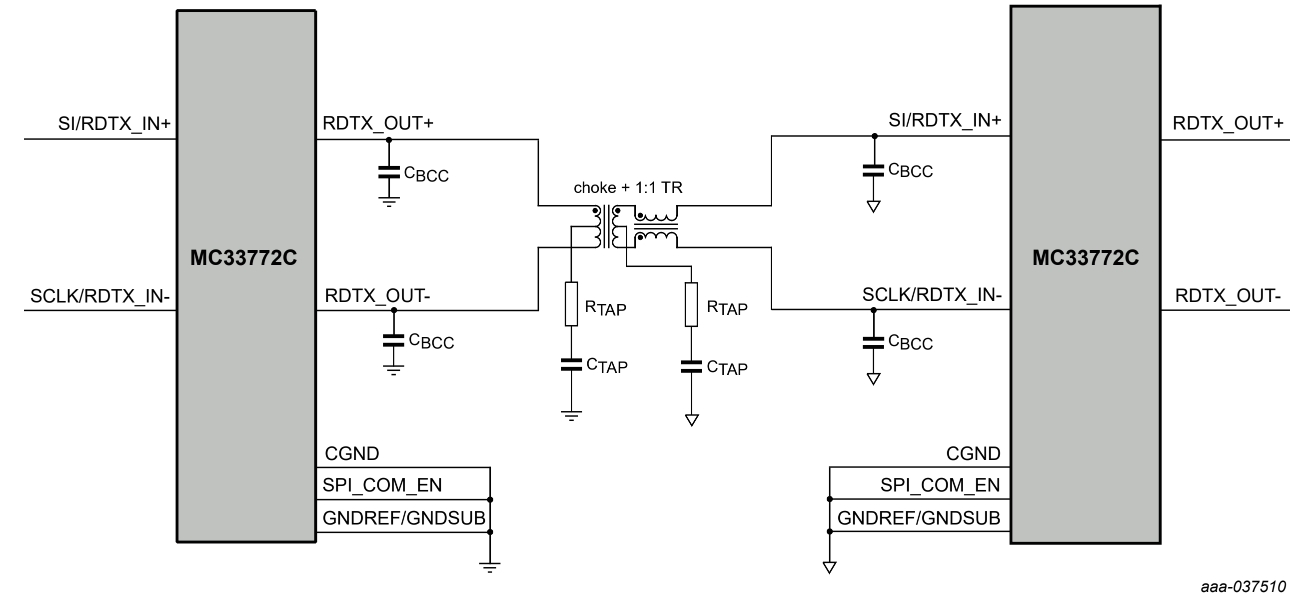


Figure 47. Slave node for a centralized application with transformer isolation

Table 98. Slave node components for a centralized application with transformer isolation

ID	Value	Units	Comments
C_{BCC}	220	pF	Ceramic capacitor
C_{TAP}	10	nF	Center tap capacitor
R_{TAP}	150	Ω	Center tap resistor

13.2.7 Distributed applications

13.2.7.1 Distributed systems - Master node

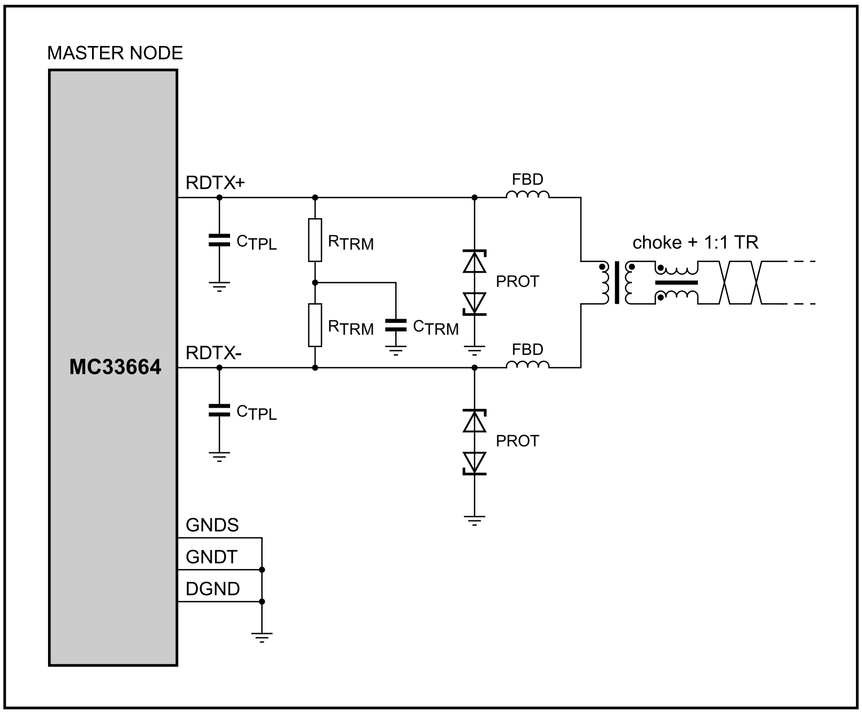


Figure 48. Master node in a distributed system (transformer isolation only)

Table 99. Master node components in a distributed system

ID	Value	Units	Comments
C_{TPL}	68	pF	Ceramic capacitor
C_{TRM}	4.7	nF	Ceramic capacitor for split termination of MC33664
R_{TRM}	75	Ω	Split termination resistor for MC33664
PROT	8	V	ESD protection. Use PESD5V0V1BB or equivalent. The indicated voltage is the nominal breakdown voltage
Choke + 1:1 TR	Pulse Electronic HM2103	N/A	Single channel transformer with common mode choke
FBD	470	Ω	Ferrite Bead (optional).Use MMZ1608Q471BTD25 or equivalent

13.2.7.2 Distributed applications - Slave node

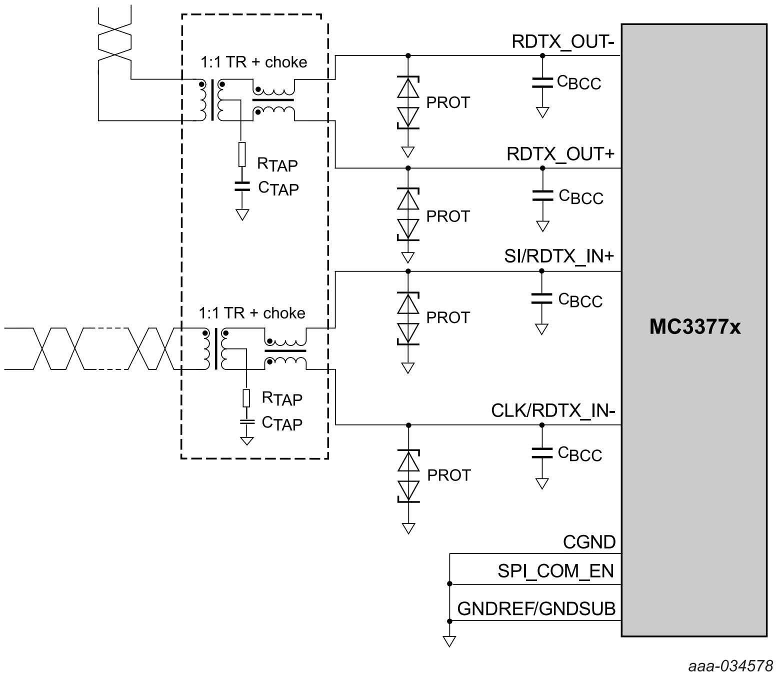


Figure 49. Slave node of a distributed application (transformer isolation only)

Table 100. Slave node components in a distributed application

ID	Value	Units	Comments
C_{BCC}	220	pF	Ceramic capacitor
PROT	8	V	ESD protection. Use PESD5V0V1BB or equivalent. The indicated voltage is the nominal breakdown voltage
C_{TAP}	10	nF	Center tap capacitor
R_{TAP}	150	Ω	Center tap resistor
1:1 TR + choke	PULSE Electronic HM2102	N/A	Dual channel transformer with common mode choke

14 MC33772CTx - Current Sense

14.1 MC33772CTC0AE

The MC33772CTC0AE part number is configured for current measurement, for instance for Battery Junction Box. It does not allow to monitor any cells, but can monitor temperatures and voltages. It can monitor the current through ISENSE ± or GPIO[5..6]. The MC33772CTC0AE can also monitor up to seven temperatures or voltages thanks to GPIO[6..0].

The MC33772CTC0AE is supporting communication through SPI or TPL. It requires a specific application schematic to connect the Analog Front End as the device will not monitor cells, so cannot be directly supplied from them.

The input voltage has to be 6 V minimum for SPI communication and 7 V minimum for TPL communication. For settings of Analog Front End, refer to Figure 50. For settings of the Current channel using ISENSE ± or GPIO[5..6], refer to ISENSE ± connection of Figure 42.

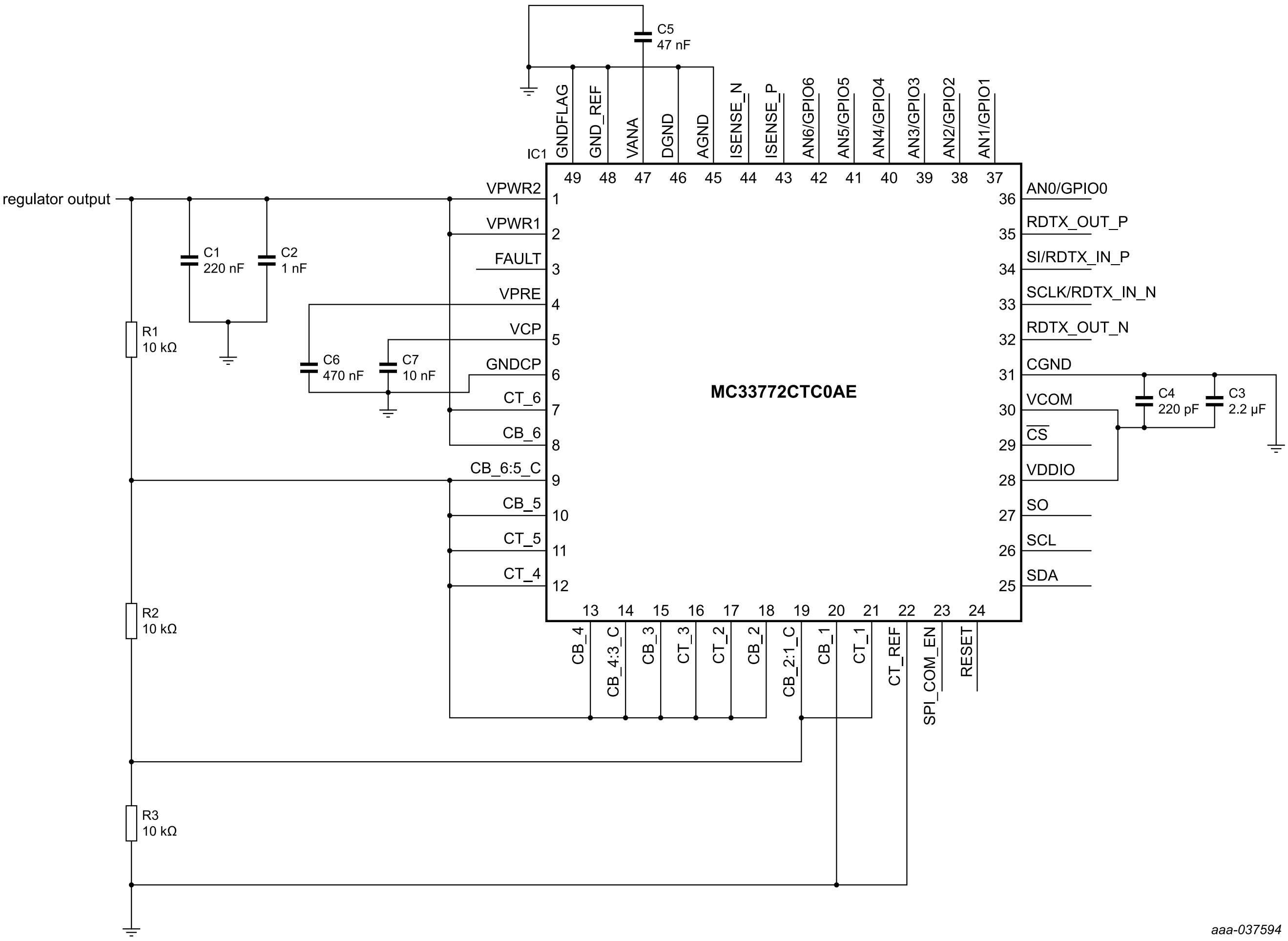


Figure 50. Analog Front End connection

14.2 MC33772CTC1AE

The MC33772CTC1AE part number is configured for current measurement, for instance for Battery Junction Box. It does not allow to monitor any cells, but can monitor temperatures and voltages. It can monitor the current through ISENSE ± or GPIO[5..6]. The MC33772CTC1AE can also monitor up to eight temperatures or voltages thanks to GPIO[6..0] and CT_1.

The MC33772CTC1AE is supporting communication through SPI or TPL. It requires a specific application schematic to connect the Analog Front End as the device will not monitor cells, so cannot be directly supplied from them.

For settings of Analog Front End, refer to Figure 51. For settings of the Current channel using ISENSE ± or GPIO[5..6], refer to ISENSE ± connection of Figure 42.

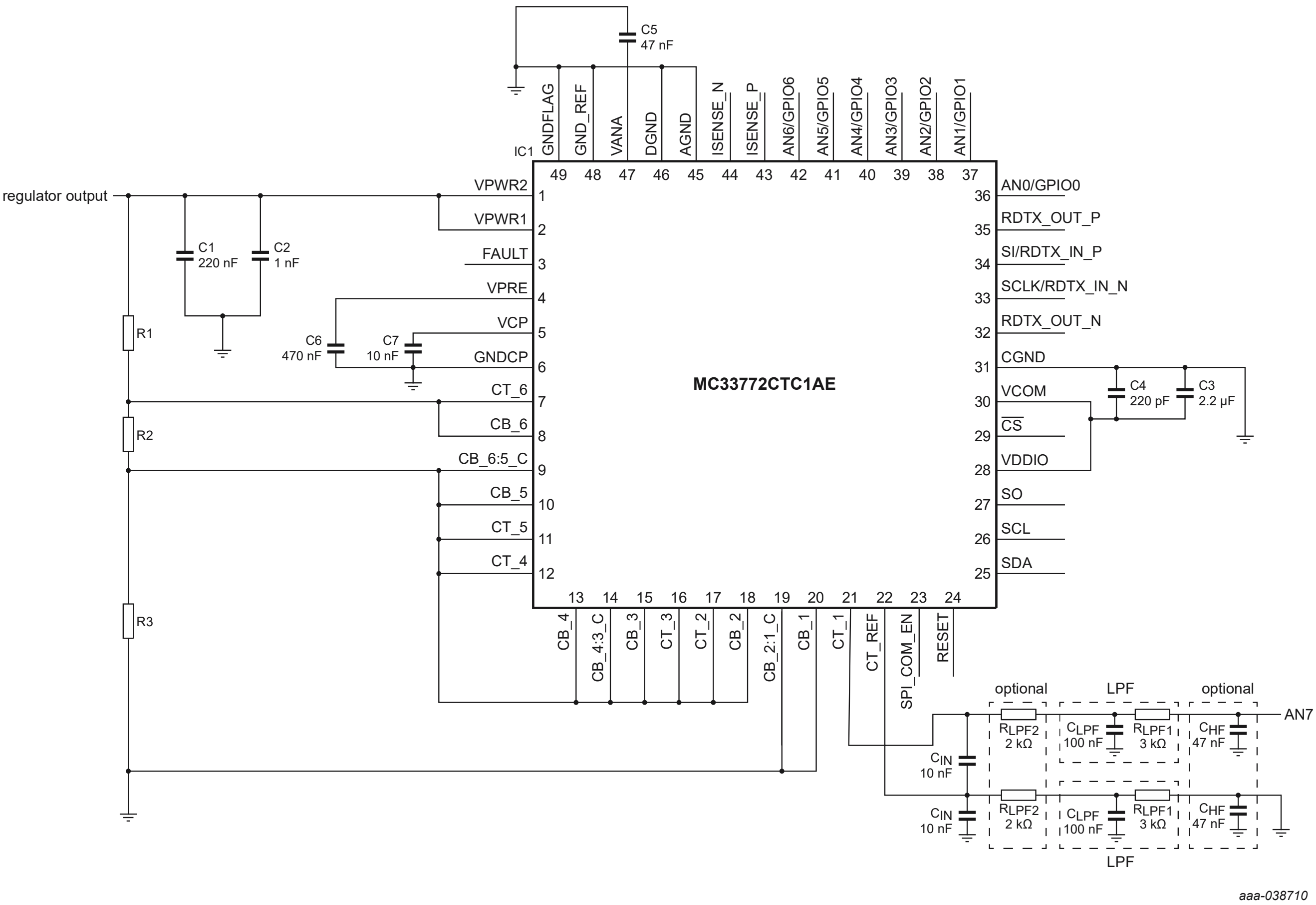


Figure 51. Analog Front End connection

The values of R1, R2 and R3 depend on the input voltage. Several values are listed in Table 101.

Table 101. Example of resistors value depending on application

Input voltage	R1	R2	R3
7 V	1 kΩ	18 kΩ	47 kΩ
12 V	4.7 kΩ	47 kΩ	47 kΩ

15 Packaging

15.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the document number of the drawings.

Table 102. Package Outline

Package	Suffix	Package outline drawing number
48-pin LQFP-EP	AE	SOT1571-1

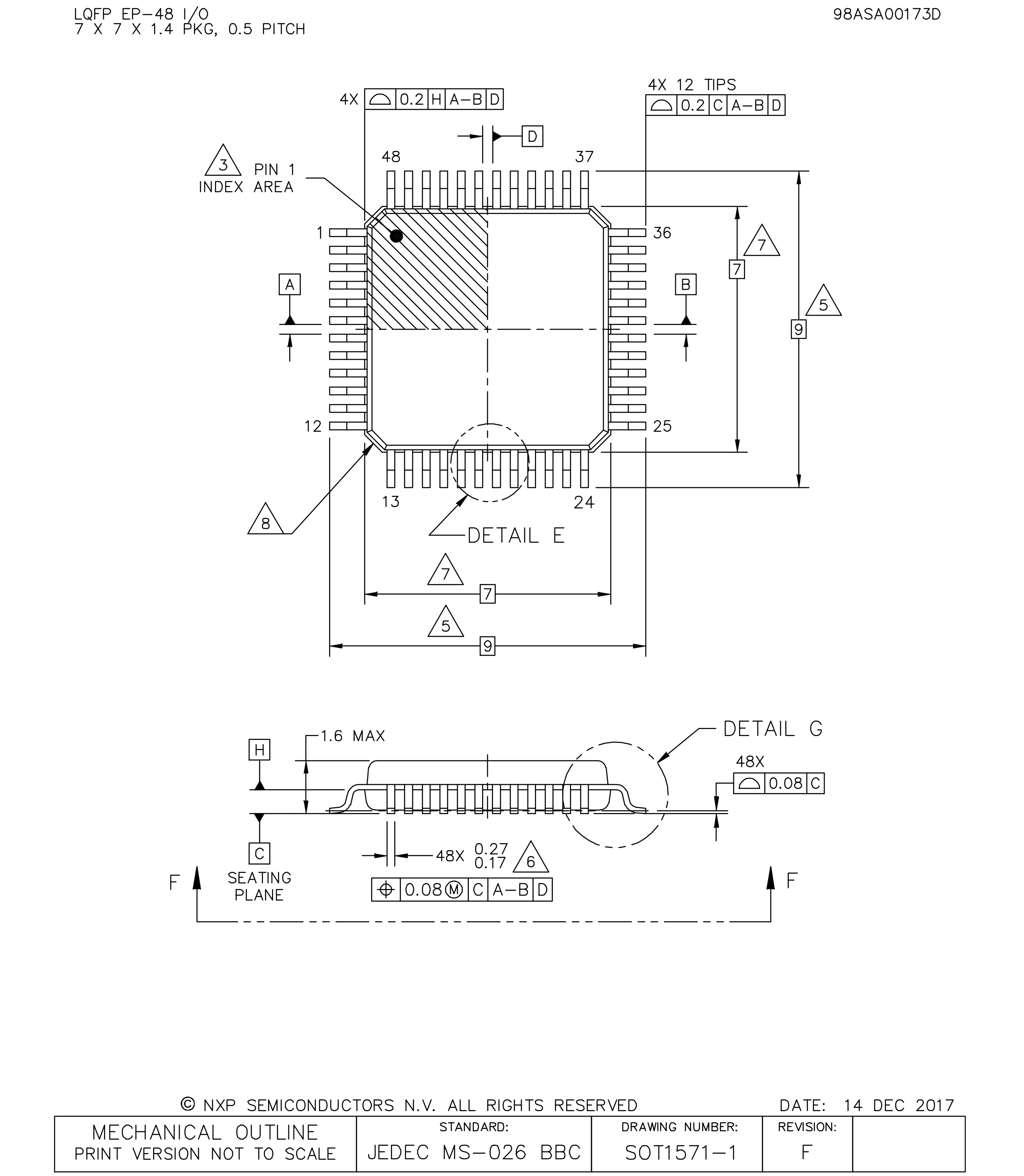
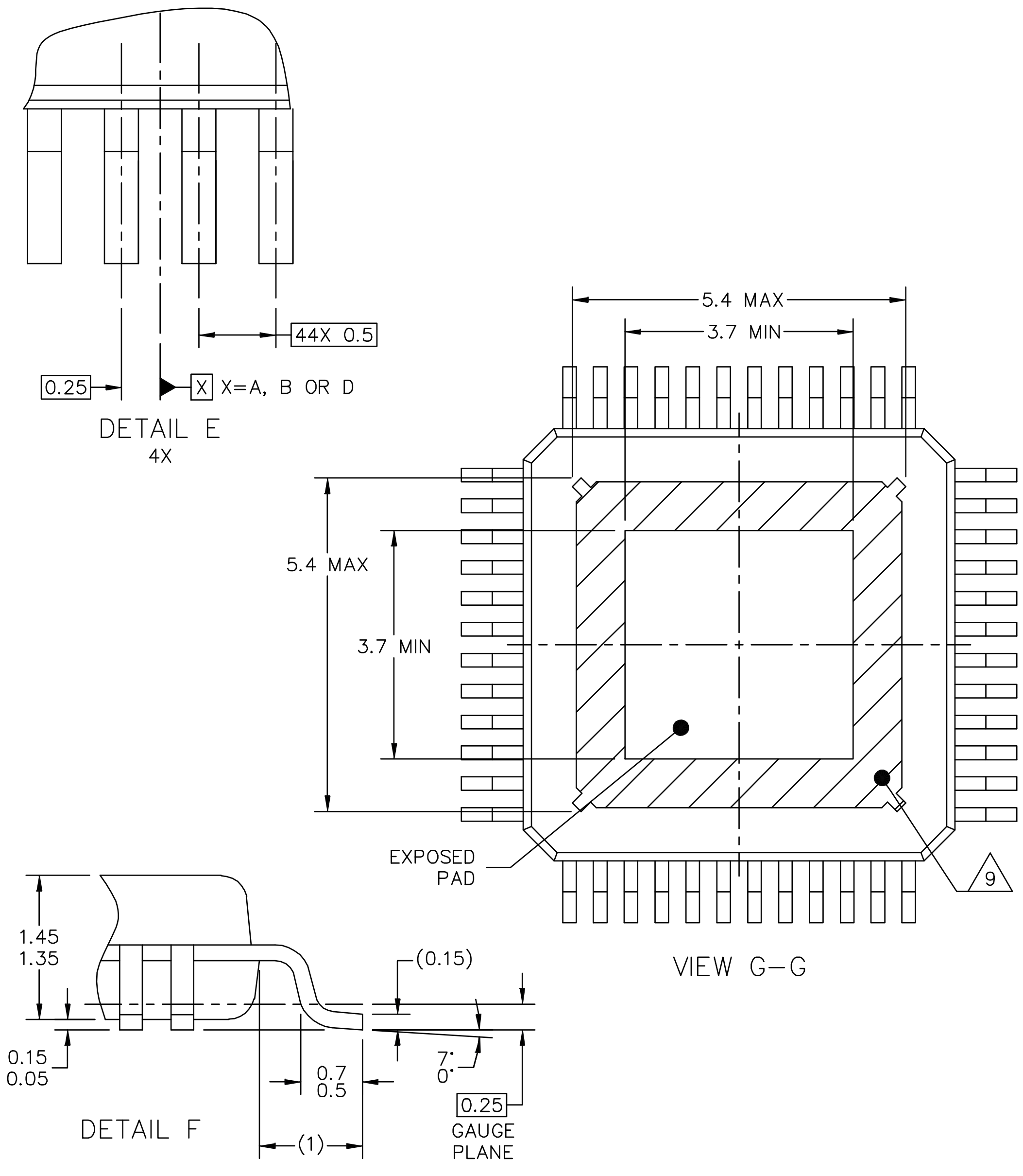


Figure 52. Package outline

LQFP EP–48 I/O
7 X 7 X 1.4 PKG, 0.5 PITCH

98ASA00173D



DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS–026 BBC	DRAWING NUMBER: SOT1571–1	REVISION: F	

Figure 53. Package outline

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 CONFIGURATION MAY VARY.
4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.
7. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

DATE: 28 AUG 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS-026 BBC	DRAWING NUMBER: SOT1571-7	REVISION: 0	

Figure 54. Package outline

16 Revision history

Table 103. Revision history

Document ID	Release date	Description
MC33772C v.4.1	05 March 2026	• Section 9.5 has been updated • Section 13.2.4 has been updated
MC33772C v.4.0	16 July 2024	• Product data sheet • Supersedes MC33772C v.3.0 • Updated status from confidential to public • Updated Revision history and Legal information to confirm with updated NXP standards
MC33772C v.3.0	04 June 2021	• Product data sheet • Supersedes MC33772C v.2.0 • Section 8.4, Table 9 – Changed $V_{ANx\_RATIO\_RES}$ typical value from VCOM * (30. 5176) to VCOM × 30.51758 – Updated min and max for parameter $ADC1a_{FV}$, $ADC1b_{FV}$ from −6.66 mV to −5 mV and from 6.66 mV to 5 mV – Added footnote 15 to parameters V_{IH}, V_{IL} and V_{HYS} regarding use of GPIO0 as wake-up – Updated duration of HTOL in footnote 9 – Added footnote 22 to t_{TPL_TD} – Added footnote 25 to t_{RES} – Removed parameters VERR33RT and VERR33RTA • Section 9.11: Modified list item number 2 and changed order of paragraphs • Section 10.4.1: Removed part of a sentence concerning content of the data field described in Table 25 • Section 11.18: Modified description of GPIOx_DR • Section 11.24: Added part to description of value 1 for bit RESET_FLT • Section 11.24 and Section 11.25 – Modified list of bits marked * – Added new mark ** • Section 11.47, Table 88: Modified table content • Section 14.2, Figure 51: Changed coloring of R_{LPF2} resistors • Several minor typo corrections throughout the document
MC33772C v.2.0	10 March 2021	• Preliminary data sheet • Supersedes MC33772C v.1.0
MC33772C v.1.0	25 August 2020	• Preliminary data sheet • Initial release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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