RAA489206

16-Cell Battery Front End

The RAA489206 is a 16-cell Battery Front End (BFE) IC, an essential component of any Battery Management System (BMS) that periodically scans battery status and the operating environment to optimize battery life and prevent catastrophic failures.

To manage the overall state of the battery pack, a differential multiplexer and 16-bit ADC allow for the accurate monitoring of cell voltage, temperature, and load current.

The RAA489206 supports I^2C, SPI, and SPI w/CRC protocols allowing customers to connect an MCU in a proprietary battery management solution.

Low current consumption with an average IDLE mode current of 200µA and a SHIP mode current of less than 18µA maximizes the storage and discharge life of a battery pack.

The RAA489206 features internal cell balancing circuitry that provides 8mA of balance current per cell. External cell balancing for higher currents is also supported.

This 16-cell high voltage BFE IC is offered in an efficient 64 Ld QFN package with a thermal pad.

Features

- High hot plug rating: 62V
- V_{CELL} accuracy: ±10mV
- I_{PACK} accuracy: ±0.2%
- 16-bit V_{CELL} and I_{PACK} measurements
- Charge/Load wakeup detection circuitry
- 4-pin GPIO port
- Integrated 3.3V regulator
- Supports I^2C, SPI, and SPIw/CRC communications

Applications

- Light electric vehicles such as e-bikes, e-scooters, and e-motorcycles
- Cordless power and gardening tools
- Home appliances
- 24V, 36V, 42V, and 48V portable battery packs
- Telecom and server farms
- Solar farms
- Energy storage systems

Contents

1. Overview

1.1 Typical Application

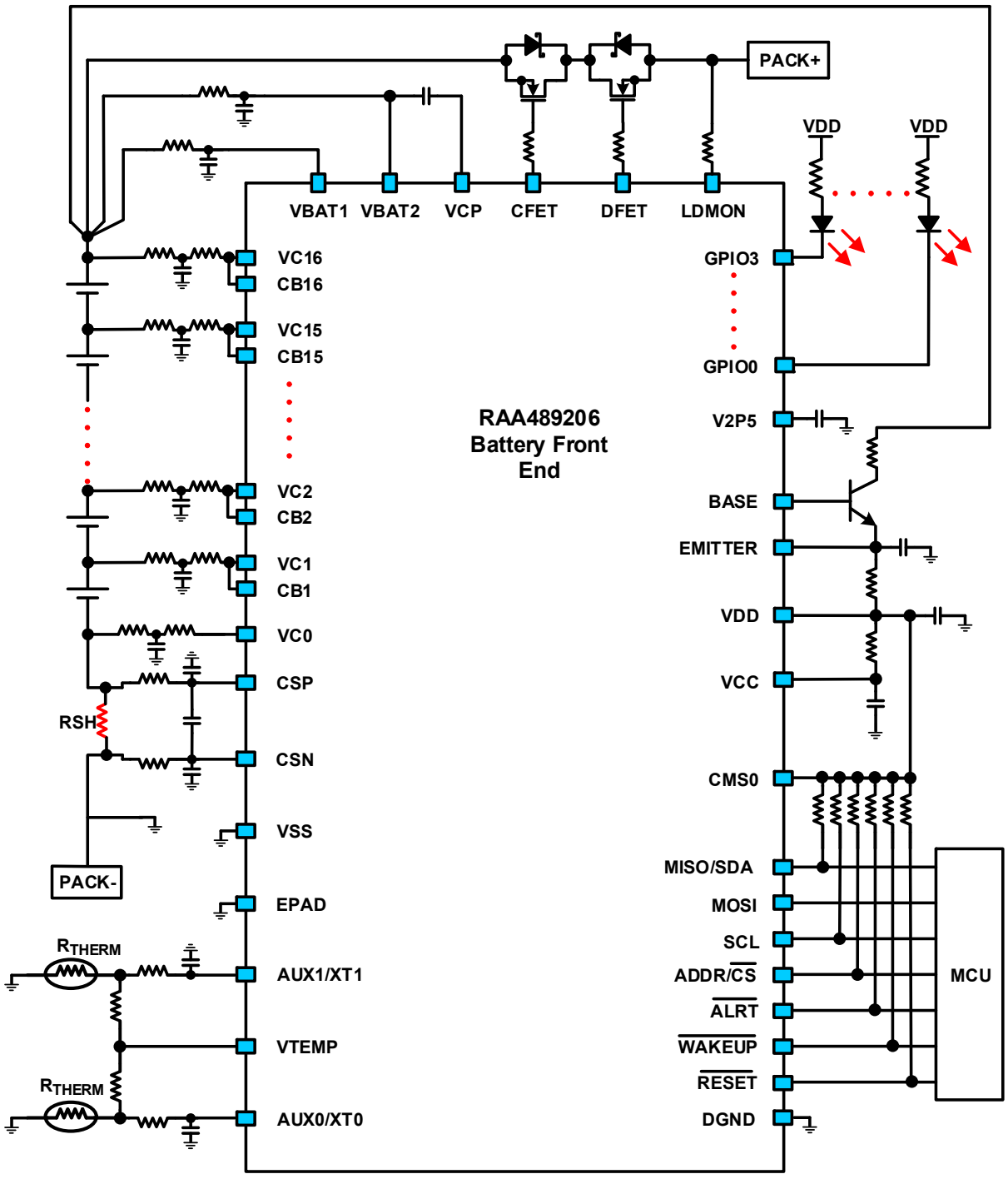


Figure 1. Typical Application

1.2 Block Diagram

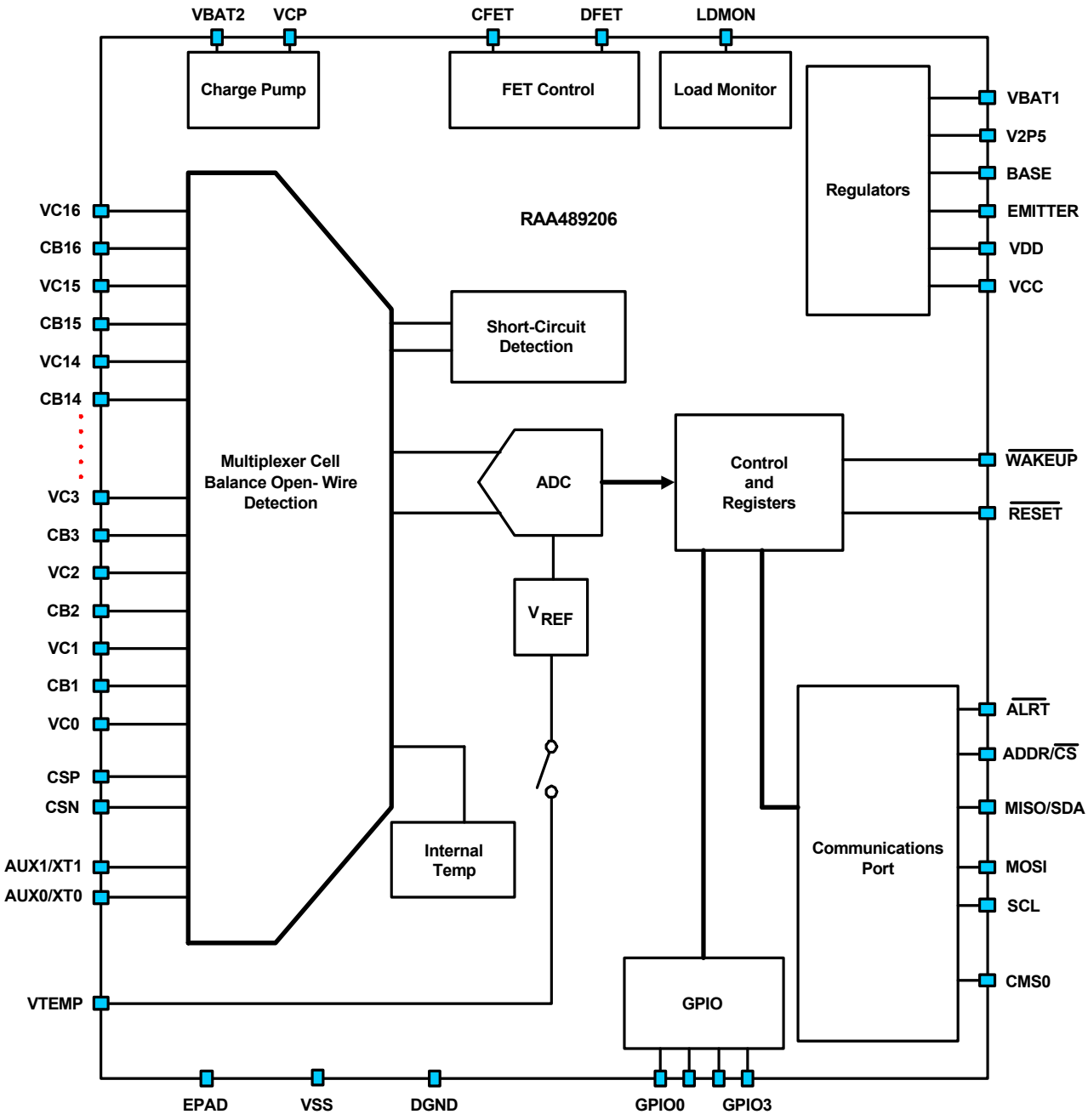
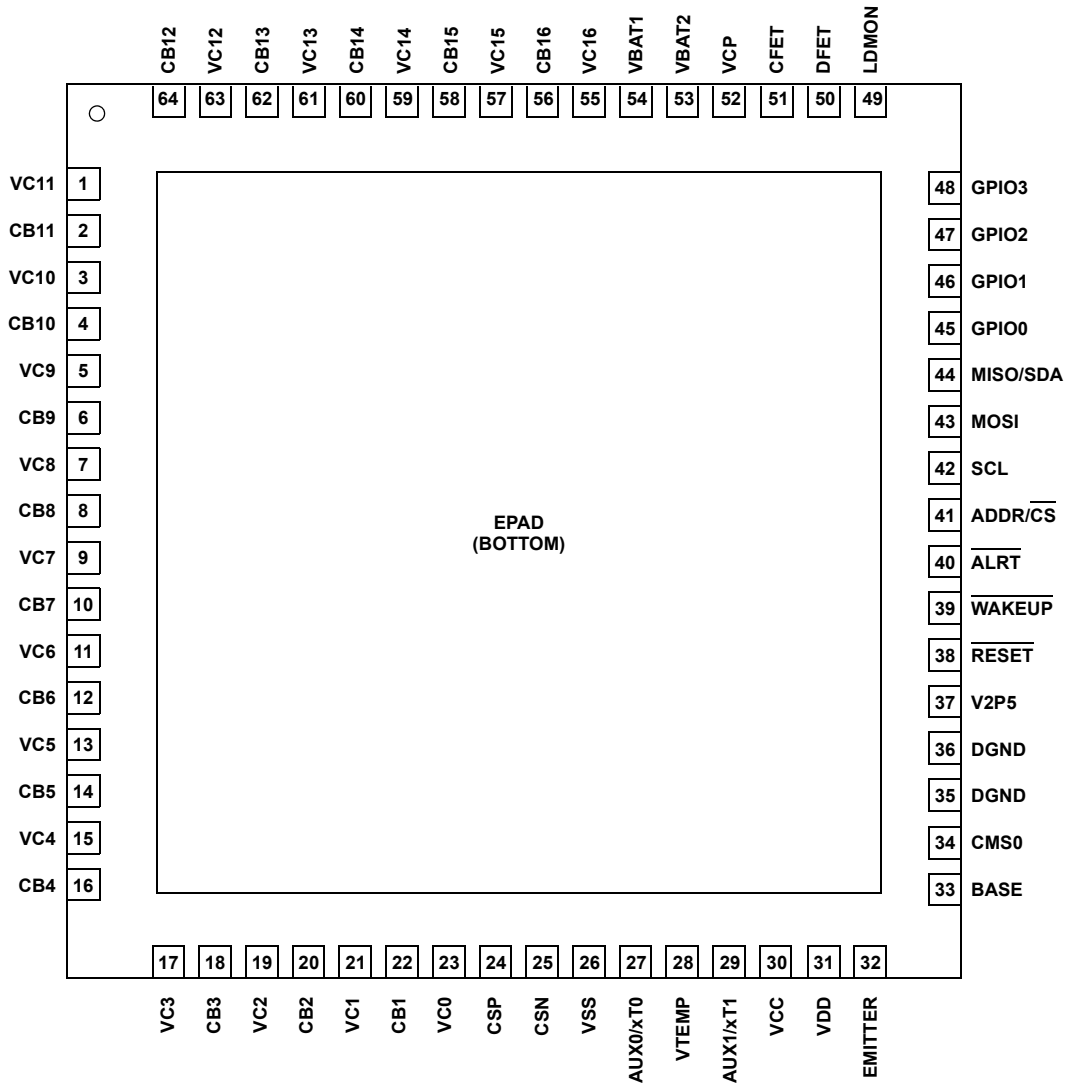


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 55, 57, 59, 61, 63	VCn (n = 0 to 16)	Battery cell voltage inputs. In an application with a 16-cell battery string, in which cell number 1 connects to the lowest voltage and cell number 16 connects to the highest voltage, VCn connects to the positive terminal of cell n and to the negative terminal of cell n+1 through external resistors (VC16 connects only to the positive terminal of Cell 16, VC0 only connects to the negative terminal of Cell 1). For applications with fewer than 16 cells, see Figure 122.
2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 56, 58, 60, 62, 64	CBn (n = 1 to 16)	Cell balancing pins. When external cell balancing FETs are used, each of these pins controls an external FET. When internal cell balancing FETs are used, these pins connect to the drains of the on-chip cell balancing transistors. See Cell Balancing Registers.
24	CSP	Current sense positive input.

Pin Number	Pin Name	Description
25	CSN	Current sense negative input.
26	VSS	Analog ground. Connect to the EPAD (electrical/thermal pad under the package).
27	AUX0/xT0	External temperature monitor or general purpose inputs. These inputs are intended for use with external resistor networks using NTC type thermistor sense elements, but can also be used as general purpose analog inputs at the discretion of the user.
29	AUX1/xT1	
28	VTEMP	Reference voltage for off-chip temperature monitoring circuit. This is a switched output that supplies a reference voltage to external circuits that include thermistors. It is enabled before starting a measurement of pins AUX0/xT0, AUX1/xT1, or VTEMP itself. It is disconnected from the pin after the measurement completes.
30	VCC	3.3V analog supply voltage input. Connect to VDD using a 10Ω resistor and connect a 1µF capacitor between this pin and VSS.
31	VDD	3.3V digital supply voltage input. Connect directly or through a current sense resistor to the emitter of the external NPN transistor, connect through a 10Ω resistor to VCC. Connect a 1µF capacitor between this pin and DGND.
32	EMITTER	Regulator source current is calculated from the measured voltage between VDD and EMITTER pins. Connect this pin to the Emitter of the external NPN. Connect a regulator current sense resistor between the EMITTER and VDD pins. Connect a 1µF capacitor between this pin and DGND.
33	BASE	Regulator control pin. Connect to the base of the external NPN transistor. Do not float.
34	CMS0	Communication protocol selection. Static input pins; do not change after power-up. See Table 75.
35	DGND	Digital ground.
36	DGND	
37	V2P5	Internal 2.5V digital supply decoupling pin. Connect a 1µF capacitor between V2P5 and DGND.
38	$\overline{\text{RESET}}$	Active low reset digital input. Connect to a logic HIGH to enable the device. Connect to a logic LOW to reset the device to its Power-On Reset (POR) default state.
39	$\overline{\text{WAKEUP}}$	Active low wakeup digital input. Connect to a logic LOW voltage level to wake up the device and transition from SHIP or LOW POWER mode to IDLE mode.
40	$\overline{\text{ALRT}}$	Open-drain, active low alert output. It is asserted under a variety of conditions to interrupt a microcontroller. See System Faults and Status.
41	ADDR/$\overline{\text{CS}}$	Chip Select input for SPI communication interface or address selection pin for I^2C communications interface.
42	SCL	Serial clock input pin for both SPI and I^2C communications interfaces.
43	MOSI	Master Output Slave Input for SPI communication interface.
44	MISO/SDA	Master Input Slave Output for SPI communication interface, or open-drain serial data I/O for I^2C communication interfaces.
45	GPIO0	General purpose digital I/Os. Open drain when used as outputs. They can be used as general purpose inputs or outputs, as status LED drivers, or as part of FET driving circuits. See 0x12 - ALRT and GPIO.
46	GPIO1	
47	GPIO2	
48	GPIO3	
49	LDMON	Load monitor input. This analog voltage monitor determines whether a normal load, short, or no load is connected to the battery pack. This pin is internally connected to the DFET pin when the DFET is off.

Pin Number	Pin Name	Description
50	DFET	Drives the gate of an external NMOS that controls the current path between the battery pack and the load. This pin is internally connected to the LDMON pin when the DFET is turned off.
51	CFET	Drives the gate of an external NMOS that controls the current path between the battery pack and the charger. This pin is internally connected to the VBAT2 pin when the CFET is turned off.
52	VCP	Charge pump output voltage. Place a capacitor between VCP and VBAT2. The charge pump provides power to FET drivers and part of the cell balancing circuits.
53	VBAT2	Power supply pin. Connect to the most positive terminal of the battery pack through dedicated filter. This pin is internally connected to the CFET pin when the CFET is turned off.
54	VBAT1	Power supply pin. Connect to the most positive terminal of the battery pack through dedicated filter.
Bottom	EPAD	Analog ground. Metal pad under the package. Connect to the VSS pin and ground plane for thermal dissipation.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter[1]	Minimum	Maximum	Unit
DGND	-0.5	+0.5	V
CSP, CSN, VC0	-1.0	+1.0	V
VBAT1, VBAT2, VCP	-0.5	+70	V
VCn (n = 13 to 16)	-0.5	+70	V
VCn (n = 9 to 12)	-0.5	+63	V
VCn (n = 6 to 8)	-0.5	+54	V
VCn (n = 2 to 5)	-0.5	+45	V
VC1	-0.5	+9	V
CBn (n = 13 to 16)	-0.5	+70	V
CBn (n = 9 to 12)	-0.5	+63	V
CBn (n = 6 to 8)	-0.5	+54	V
CBn (n = 2 to 5)	-0.5	+45	V
CB1	-1	+9	V
CBn [Internal Cell Balancing Current when active][2]		±20	mA
CFET, DFET, VCP, LDMON[2]	-0.5	+70	V
CFET	V_{BAT2} - 0.5	V_{BAT2} + 12	V
DFET	LDMON - 0.5	V_{BAT2} + 12	V
VCP	V_{BAT2} - 1.0	V_{BAT2} + 12	V
V2P5[2]	-0.5	+2.9	V
BASE, EMITTER, VCC, VDD, VTEMP, Aux0/xT0, Aux1/xT1[2]	-0.5	+6	V
SCL, MISO/SDA, MOSI, ADDR/$\overline{CS}$, GPIOx, CMS0, $\overline{ALRT}$, $\overline{RESET}$, $\overline{WAKEUP}$[3]	DGND - 0.5	DGND + 6	V
SDA, $\overline{ALRT}$, GPIOx Pull-Down Current [3]		10	mA
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2014)	1.5		kV
Charged Device Model (Tested per JS-002-2018)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

1. All voltages are specified with respect to VSS, unless otherwise noted.
2. VCP, CFET, DFET, CB[1:16], V2P5, VTEMP, and BASE pins are analog outputs and should not be driven from an external source. VCC and VDD can be driven only by the external NPN connected to the BASE and EMITTER pins.
3. $\overline{ALRT}$, GPIO0, GPIO2, GPIO3 (configure as an output) and MISO/SDA (operating as an output) pins are digital outputs. These pins should not be driven from an external source.

3.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
64 Ld QFN	24	1.1

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Continuous Power Dissipation		400	mW
Maximum Storage Temperature Range	-55	+125	°C
Maximum Junction Temperature (T_{JMAX})		+125	°C
Pb-Free Reflow Profile	see TB493		

3.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature Range (T_A)	-40	+85	°C
Junction Temperature (T_J)	-40	+95[1]	°C
V_{BAT1}, V_{BAT2} Charge Pump Enabled	12	59	V
V_{BAT1}, V_{BAT2} Charge Pump Disabled	12	64	V
CFET, DFET	V_{BAT2}	V_{BAT2} + 11	V
VCP	V_{BAT2}	V_{BAT2} + 11	V
LDMON	0	VBAT2	V
VC(n+1) - VC(n) (n = 0 to 15)	2.2	4.7	V
CB(n+1) - VC(n) (n = 0 to 15)	0	6	V
VC0	-600	300	mV
CB(n) (n = 1 to 16) [2]	$VC_{(n-1)}$	$VC_{(n-1)}$ + 5	V
CSN, DGND	-10	+10	mV
(CSP - CSN) [Current Measurement]	-600	+300	mV
VTEMP, AUX0/xT0, AUX1/xT1	0	1.22	V
EMITTER - V_{DD}	0	275	mV
SDA, $\overline{ALRT}$, GPIOx Pull-Down Current[3]		2.5	mA
GPIOx, $\overline{ALRT}$, MOSI,MISO/SDA, SCL,ADDR/$\overline{CS}$, CMS0, $\overline{WAKEUP}$, $\overline{RESET}$ [3]	0	V_{DD}	V

1. As determined by the default IOTF Threshold.
2. VCP, CFET, DFET, CB[1:16], V2P5, VTEMP, and BASE pins are analog outputs and should not be driven from an external source. VCC and VDD can be driven only by the external NPN connected to the BASE and EMITTER pins.
3. $\overline{ALRT}$, GPIO0, GPIO2, GPIO3 (configure as an output) and MISO/SDA (operating as an output) pins are digital outputs. These pins should not be driven from an external source.

3.4 Electrical Specifications

Unless otherwise specified: T_A = +25°C, V_{BAT1} = V_{BAT2} = 48V, (VC_n - VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, control registers at default, V_{SS} = DGND = 0V, cell balancing is off. Voltages are with respect to V_{SS}. External components are per Pin Functionality.[1][2][3][4][5]

Parameter	Symbol	Test Conditions	Min[6]	Typ	Max[6]	Unit
Power Supply (System Operation)						
V_{BAT} Voltage Range	V_{BAT1}, V_{BAT2}	For V_{BAT1}, V_{BAT2}	12	-	59	V
Total Average Current Consumed at VBAT1, VBAT2, VDD, and VCC Pins	I_{total}	IDLE Mode; Charge Pump On	250	330	380	µA
		IDLE Mode; Charge Pump Off	200	290	340	µA
		SCAN Mode; Charge Pump and FETs on, Current during VCell Scan	600	820	1000	µA
		SCAN Mode; Charge Pump and FETs off, Current during VCell Scan	540	760	940	µA
		LOW POWER Mode; Strong Reg on; LP REG = 1		39	200	µA
		LOW POWER Mode; Weak Reg on; LP REG = 0		10	50	µA
		SHIP Mode		5	18	µA
Cell Measurement (0x30 - 0x4F - V_{CELL} Voltage (R))						
V_{CELL} Measurement Error	V_{CELLME}	0°C to +60°C; 3V to 4.5V, Register 0x02 = 0x9C, 14 cell configuration at 4.5V.	-10		10	mV
V_{CELL} Input Leakage Current	-	Not Scanning	-0.3		0.3	µA
I_{PACK} Functional Block (0x52 - 0x53 - I_{PACK} Voltage (R))[7]						
I_{PACK} Measurement Gain Error	I_{PACK_GE}	V_{CSP} = ±200mV 0x03 = 0x9C	-0.3		0.3	%
I_{PACK} Measurement Gain Error TC	$I_{PACK\_GE\_TC}$	T = -40°C to +85°C 0x03 = 0x9C		±30		ppm/°C
I_{PACK} Measurement Offset vs Common-Mode	I_{PACK_CMRR}	V_{CMV} = ±163.84mV 0x03 = 0x9C		±1.6		µV/V
I_{PACK} Measurement Offset	I_{PACK_VOS}	0x03 = 0x9C	-100	10	+100	µV
I_{PACK} Measurement Offset TC	$I_{PACK\_VOS\_TC}$	T = -40°C to +85°C 0x03 = 0x9C		±0.3		µV/°C
I_{PACK} Input Current	I_{PACK_IC}	V_{CSP} = V_{CSN}	-15	1	+15	µA
		T = -40°C to +85°C		0.001		µA/°C
I_{PACK} Offset Current	I_{os_IC}	I_{CSP} - I_{CSN}	-7.5	0.005	+7.5	µA
		T = -40°C to +85°C		0.001		µA/°C
Zero Current Threshold	I_{Zero_THR}	Zero current threshold for charge and discharge		±200		µV

Unless otherwise specified: T_A = +25°C, V_{BAT1} = V_{BAT2} = 48V, (VC_n - VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, control registers at default, V_{SS} = DGND = 0V, cell balancing is off. Voltages are with respect to V_{SS}. External components are per Pin Functionality.[1][2][3][4][5] (Cont.)

Parameter	Symbol	Test Conditions	Min[6]	Typ	Max[6]	Unit
Short-Circuit Detectors (I_{PACK} Fault Detectors)						
Discharge Short-Circuit Hysteresis	SC_{DCHRG_Hys}			20		mV
Discharge Short-Circuit V_{OS}	SC_{DCHRG_Vos}	Difference between setting and trigger voltage		8		mV
Load Monitor Function (0x0E - Load/Charge Operations)						
Load Detection Threshold	V_{LDThr}		0.9	1.2	1.6	V
Load Detection Hysteresis	V_{LDHys}			100		mV
Load Monitor Pull-Up Resistance	R_{LDPU}	From LDMON to VBAT1 ELD[1:0] = 01	0.75	1	1.2	MΩ
		From LDMON to VBAT1 ELD[1:0] = 10	8	10	13.5	kΩ
Load Monitor External Isolation Resistor (see Block Diagram of Power FET Controls)	R_{LDISO}		200			Ω
Load Monitor Enable Delay Time	t_{LDEN}	DFET off to load detection test		256		ms
External Temperature Measurements (ETAUX Detectors)						
V_{ETAUX} Gain Error	V_{ETAUX_GE}	0V to FS	-1	±0.2	+1	%
V_{ETAUX} Gain Error TC	$V_{ETAUX\_GE\_TC}$	0V to FS		±35		ppm/°C
V_{ETAUX} Gain Error Match	$V_{ETAUX\_GE\_M}$	0V to FS		±0.25		%
V_{ETAUX} Offset	V_{ETAUX_VOS}	V_{ETAUX} = 0V		-3		mV
V_{ETAUX} Offset TC	V_{ETAUX_VOSTC}			±22		µV/°C
Maximum Capacitor Connected to xT0, xT1 (Figure 85)	C_{ETAUX}	NTC = 10kΩ			22	nF
		NTC = 100kΩ			3.9	nF
Settling Time for VTEMP before a xT0, xT1 measurement	t_{ETAUX_settle}	V_{TEMP} Turn on to xT0, xT1 measurement	3.35	4		ms
ETAUX Pull-Up Resistor	R_{ETAUX}	OW Test Internal pull-up resistors from xT0 and xT1 to VCC (AUX PULL = 1).		1.3		MΩ
ETAUX Input Current	I_{ETAUX}		-1	0.01	+1	µA
		T = -40°C to 85°C		0.001		µA/°C
ETAUX Open-Wire Threshold	$ETAUX_{owThr}$			1.146		V
Internal Temperature Sensor (Internal Temperature)						
Internal Temperature Sensor Measurement Range	IT		-40		+85	°C
Internal Temperature Sensor Output Code		25°C		0x99		Bits
Internal Temperature Sensor Resolution	IT_{STEP}			0.8		°C/LSB
Internal Temperature Error	IT_{ER}	0°C to +60°C		±5		°C

Unless otherwise specified: T_A = +25°C, V_{BAT1} = V_{BAT2} = 48V, (VC_n - VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, control registers at default, V_{SS} = DGND = 0V, cell balancing is off. Voltages are with respect to V_{SS}. External components are per Pin Functionality.[1][2][3][4][5] (Cont.)

Parameter	Symbol	Test Conditions	Min[6]	Typ	Max[6]	Unit
Regulator and V_{TEMP} (Regulator Measurements and Detectors)						
Regulation Voltage Accuracy	REG_V	At VDD Pin, no external load	3.15	3.3	3.45	V
Capacitance at the Regulator	REG_C		1			µF
V_{TEMP} Voltage Accuracy		0mA to 2mA load	1.189		1.221	V
V_{TEMP} Output Impedance				0.2		Ω
Weak Reg Voltage at VDD		SHIP or LOW POWER Mode, No Load, LP REG = 0	2.65	2.89		V
Weak Reg Drive Current Capability		SHIP or LOW POWER Mode, LP REG = 0		150		µA
BASE Pin Drive Current capability (Ext regulator NPN base drive only)	I_{BASE_drv}	LP REG = 1	1			mA
V_{VCC} Measurement Error	V_{VCC_ME}			-2.0		%
V_{VTEMP} Measurement Error	V_{VTEMP_ME}			-0.25		%
I_{REG} Measurement Gain Error	$IREG_{GE}$	EMITTER = V_{DD} + 50mV to V_{DD} + 200mV		0.025		%
I_{REG} Measurement Offset	$IREG_{VOS}$				280	µV
Time to Switch from Strong Regulator to Weak (Internal) Regulator	t_{REGSW}	Device transitions to SHIP or LOW POWER Modes		2.048		s
Regulator and V_{TEMP} Thresholds (Regulator Measurements and Detectors)						
Voltage Threshold for V_{TEMP}	$VTEMP_{Min}$			1.1		V
V_{CC} and V_{DD} Overvoltage Threshold	PG_{VDD_OV}			3.83		V
	PG_{VCC_OV}					
V_{CC} and V_{DD} Undervoltage Threshold	PG_{VDD_UV}			2.58		V
	PG_{VCC_UV}					
V_{2P5} Overvoltage Threshold	PG_{2P5V_OV}			2.84		V
V_{2P5} Undervoltage Threshold	PG_{2P5V_UV}			1.94		V
V_{BAT1} (0x20 - 0x21 - V_{BAT1} Thresholds)						
V_{BAT1} Measurement Error	V_{BAT1_ME}	25V ≤ V_{BAT1} ≤ 55V (0C to 60C)		±0.5		%
V_{BAT1} Measurement Error TC	V_{BAT1ME_TC}			±100		ppm/°C
V_{BAT1} Input Resistance	R_{VBAT1}			640		kΩ
Cell Balancing (Cell Balancing Registers)						
External Cell Balance Drive Current	I_{ECB}	CB Config = 1; CB_n output on (n = 1 to 16)	21		28	µA
External Cell Balance Leakage Current	I_{ECB_OFF}	CB Config = 1; CB_n output off (n = 1 to 16)		10		nA

Unless otherwise specified: T_A = +25°C, V_{BAT1} = V_{BAT2} = 48V, (VC_n - VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, control registers at default, V_{SS} = DGND = 0V, cell balancing is off. Voltages are with respect to V_{SS}. External components are per Pin Functionality.[1][2][3][4][5] (Cont.)

Parameter	Symbol	Test Conditions	Min[6]	Typ	Max[6]	Unit
Internal Cell Balance Pin Resistance CBn to VCn-1 (n = 1 to 16)	R_{CB_OFF}, R_{CB_ON}	CB Config= 0; CB_n output off (n = 1 to 16)		4		MΩ
		CB Config= 0; CBn output on (n = 1 to 16)		70		Ω
CB Threshold Hysteresis	V_{CBHys}			90		mV
FET Drive Control Specifications (Power FET Block)						
Average Output Voltage with Respect to V_{BAT2} at DFET and CFET Pins	V_{DFET}, V_{CFET}	12V ≤ V_{BAT2} ≤ 55V; (100µA load on Charge Pump)	8		12	V
Charge Pump Rising Voltage Threshold (To clear CPMP NRDY bit 0x65.5)	V_{pmpMin}	V_{BAT2} recommended operating range		11		V
Charge Pump Falling Voltage Threshold (To set CPMP NRDY bit 0x65.5)	$V_{pmpFall}$	V_{BAT2} recommended operating range		5.6		V
DFET Off-State Output Resistance	R_{DFOFF}	Resistance from DFET to LDMON, VCMP on		70		Ω
CFET Off-State Output Resistance	R_{CFOFF}	Resistance from CFET to V_{BAT2} VCMP on		70		Ω
DFET On-State Output Resistance	R_{DFON}	Resistance from DFET to VPMP, VCMP on		2800		Ω
CFET On-State Output Resistance	R_{CFON}	Resistance from CFET to VPMP, VCMP on		2800		Ω
Charge Pump-to-Gate Capacitance Ratio (External FETs)	C_{pmp}	C_{pmp} to (C_{DFET} + C_{CFET}) Ratio	20			Ratio
Charge Pump Peak Current	I_{SC}		200			µA
Charge Pump Start-Up Time	t_{strt}	C_{pmp} = 470nF; the time it takes to charge C_{pmp} to 10V above VBAT2		13	30	ms
Open-Wire (See Open-Wire Test)						
Open-Wire Resistance	R_{OW}	VC_n to VC_{n-1} (n = 1 to 16)		8		kΩ
Open-Wire Resistance Connection Time	t_{OW}			10		ms
Open-Wire Detection Threshold	V_{OWth1}	VC_n to VC_{n-1} (n = 1 to 16)		0.5		V
V_{BAT1} Open-Wire Detection Threshold	V_{OWth2}	VC16 - VBAT1		0.3		V
VSS Open-Wire Detection Threshold	V_{OWth3}	VC1 - VSS, VC0 - VSS		0.25		V
Input Capacitance	C_{OW}	Equivalent capacitor that can be connected to the pin			200	nF

Unless otherwise specified: T_A = +25°C, V_{BAT1} = V_{BAT2} = 48V, (VC_n - VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, control registers at default, V_{SS} = DGND = 0V, cell balancing is off. Voltages are with respect to V_{SS}. External components are per Pin Functionality.[1][2][3][4][5] (Cont.)

Parameter	Symbol	Test Conditions	Min[6]	Typ	Max[6]	Unit
System (System Operation)						
First Conversion ADC Conversion Time	ADC_{CT1}	ADC input changes or a new trigger executes		2		ms
ADC Subsequent Conversion Time	ADC_{CT2}			0.5		ms
Communication Time Out 0x1B.7:6 - Communications Timeout	t_{COM}	Maximum time allowed without receiving communication from the Host while in IDLE mode		4.096		s
LOW POWER Measurement period	t_{LPMEAS}	Time between scans in LOW POWER Mode		2.048		s
Internal 32kHz Oscillator Accuracy			-5	±1	+5	%
Internal 4MHz Oscillator Accuracy				3		%
GPIO (0x12 - ALRT and GPIO)						
GPIO Pins Low Level Output Voltage	$GPIO_{VOL}$	I_{sink} = 2mA		0.2	0.4	V
GPIO Pin High Level Input Voltage	$GPIO_{VIH}$		$0.7 x V_{DD}$			V
GPIO Pin Low Level Input Voltage	$GPIO_{VIL}$				$0.3 x V_{DD}$	V
GPIO Pull-up	R_{GPIO_PU}		2500			Ω
GPIO Pins Leakage Current High	$GPIO_{LIH}$	3.3V applied	-1		+1	uA
GPIO Pins Pulse Period	$GPIO_{pulse\_per}$	LED Drive mode		10		ms
GPIO Pins On-Time (Low)	$GPIO_{pulse\_on}$	LED Drive mode		2		ms
$\overline{CS}$/ADDR, CMS0						
Pins High Level Input Voltage	PIN_{VIH}		$0.7 x V_{DD}$			V
Pins Low Level Input Voltage	PIN_{VIL}				$0.3 x V_{DD}$	V
Pins Leakage Current	PIN_{LIH}	0V to 3.3V applied	-1		+1	µA
$\overline{ALRT}$ ($\overline{ALRT}$ Pin (40))						
$\overline{ALRT}$ Pin Low Level Output Voltage	$\overline{ALRT}_{VOL}$	I_{sink} = 2mA		0.2	0.4	V
$\overline{ALRT}$ Sink Current	$\overline{ALRT}_{IOL}$	At 0.6V		4		mA
$\overline{ALRT}$ Pin Leakage Current	$\overline{ALRT}_{LIH}$		-1		+1	µA
$\overline{ALRT}$ Pin Pulse Period	$\overline{ALRT}_{pulse\_per}$	$\overline{ALRT}$ Pulse EN = 1		10		ms
$\overline{ALRT}$ Pin On-Time	$\overline{ALRT}_{pulse\_on}$	$\overline{ALRT}$ Pulse EN = 1		2		ms
$\overline{WAKEUP}$ ($\overline{WAKEUP}$ Pin (39))						
$\overline{WAKEUP}$ Pin High Level Input Voltage	$\overline{WK}_{VIH}$		$0.7 x V_{DD}$			V

Unless otherwise specified: T_A = +25°C, V_{BAT1} = V_{BAT2} = 48V, (VC_n - VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, control registers at default, V_{SS} = DGND = 0V, cell balancing is off. Voltages are with respect to V_{SS}. External components are per Pin Functionality.[1][2][3][4][5] (Cont.)

Parameter	Symbol	Test Conditions	Min[6]	Typ	Max[6]	Unit
$\overline{\text{WAKEUP}}$ Pin Low Level Input Voltage	$\overline{WK}_{VIL}$				$0.3xV_{DD}$	V
$\overline{\text{WAKEUP}}$ Pin Leakage Current	$\overline{WK}_{LIH}$	0V to 5.5V applied	-1		+1	µA
$\overline{\text{WAKEUP}}$ Low state pulse width	$\overline{WK}_{LPw}$	Minimum detectable pulse width	100			ns
$\overline{\text{RESET}}$ (RESET Pin (38))						
$\overline{\text{RESET}}$ Pin High Level Input Voltage	$\overline{RST}_{VIH}$		$0.7xV_{DD}$			V
$\overline{\text{RESET}}$ Pin Low Level Input Voltage	$\overline{RST}_{VIL}$				$0.3xV_{DD}$	V
$\overline{\text{RESET}}$ Pin Leakage Current High	$\overline{RST}_{LIH}$	0V to 5.5V applied	-1		+1	µA
Power-On Reset Voltage at VBAT1 (Hysteresis 100mV Minimum)	V_{POR}		4		7	V
Power-On Reset Startup Time to Measurement	$t_{StartUp}$	$V_{BAT1} > V_{POR}$, $\overline{\text{RESET}}$ rising edge or soft reset to first measurement command			20	ms
Power-On Reset Communication Lockout	t_{RESET}	$V_{BAT1} > V_{POR}$, $\overline{\text{RESET}}$ rising edge or soft reset to first serial communication command activity (ACK)		200		µs
$\overline{\text{RESET}}$ Low State Pulse Width	$\overline{RST}_{LPw}$		100			ns
SPI Interface Specifications (SPI Serial Interface)						
Slave Address (7bits) No CRC	SA_{SPI}	Fixed		0001 010		Binary
Slave Address (7bits) Use CRC	SA_{SPI}	Fixed		1001 110		Binary
SCLK, MOSI, $\overline{\text{CS}}$ Input Lo Voltage	SPI_V_{IL}				$0.2xV_{DD}$	V
SCLK, MOSI, $\overline{\text{CS}}$ Input Hi Voltage	SPI_V_{IH}		$0.8xV_{DD}$			V
SCLK, MOSI, $\overline{\text{CS}}$ Input Hysteresis	SPI_V_{HYS}			$0.05xV_{DD}$		mV
SCLK, MOSI, $\overline{\text{CS}}$ Input Current	SPI_I_{IN}		-1		+1	µA
SCLK, MOSI, $\overline{\text{CS}}$ Input Capacitance	SPI_C_{IN}				10	pF
MISO Output Lo Voltage	SPI_V_{OL}	2mA Sink Current	0		0.4	V
MISO Output Hi Voltage	SPI_V_{OH}	2mA Source Current	V_{DD}-0.4V		V_{DD}	V
SCL Clock Frequency	SPI_f_{SCL}				2	MHz

Unless otherwise specified: T_A = +25°C, V_{BAT1} = V_{BAT2} = 48V, (VC_n - VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, control registers at default, V_{SS} = DGND = 0V, cell balancing is off. Voltages are with respect to V_{SS}. External components are per Pin Functionality.[1][2][3][4][5] (Cont.)

Parameter	Symbol	Test Conditions	Min[6]	Typ	Max[6]	Unit
Pulse Width of Input Spikes Suppressed	SPI_t_{IN1}	Any pulse narrower than the max spec is suppressed			50	ns
Clock High Time	SPI_t_{HIGH}		200			ns
Clock Low Time	SPI_t_{LOW}		200			ns
Enable Lag Time	SPI_t_{LAG}	Last data read clock edge to chip select high	250			ns
Time Delay Between Bytes	SPI_t_{WAIT}	Time between falling edge of the clock pulse corresponding to the last bit of any byte, and the next rising edge of the clock corresponding to the first bit of the next byte	7			µs
Slave Access Time	SPI_T_{LEAD}	Chip select low to SCLK rising edge	200			ns
Data Valid Time	SPI_t_V	Clock low to MISO valid		130	350	ns
Data Output Hold Time	SPI_t_{HO}	Data hold time after falling edge of SCL	0	115		ns
MISO Disable Time	SPI_t_{DIS}	MISO disabled following rising edge of $\overline{CS}$			240	ns
Data Setup Time	SPI_t_{SU}	Data input valid before rising edge of SCL	100			ns
Data Input Hold Time	SPI_t_{HI}	Data input to remain valid following rising edge of SCL	80			ns
MOSI Rise Time	SPI_t_R	Up to 50pF load			30	ns
MOSI Fall Time	SPI_t_F	Up to 50pF load			30	ns
I^2C Interface Specifications (I^2C Serial Interface)						
Slave Address (7bits)	SA_{I2C}	$\overline{CS}$/Addr = VDD		0011 010		Binary
		$\overline{CS}$/Addr = DGND		0001 010		Binary
SDA and SCL Input Buffer LOW Voltage	V_{IL}		-0.3		0.3xV_{DD}	V
SDA and SCL Input Buffer HIGH Voltage	V_{IH}		0.7xV_{DD}		V_{DD}+0.3	V
SDA and SCL Input Buffer Hysteresis	Hysteresis			0.05xV_{DD}		V
SDA Output Buffer LOW Voltage	V_{OL}	Sinking 2mA	0	0.02	0.4	V
Pin Leakage Current for SDA and SCL Pins	I_{leak}		-1		1	µA
SCL Frequency	f_{SCL}				400	kHz

Unless otherwise specified: T_A = +25°C, V_{BAT1} = V_{BAT2} = 48V, (VC_n - VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, control registers at default, V_{SS} = DGND = 0V, cell balancing is off. Voltages are with respect to V_{SS}. External components are per Pin Functionality.[1][2][3][4][5] (Cont.)

Parameter	Symbol	Test Conditions	Min[6]	Typ	Max[6]	Unit
Pulse Width Suppression Time at SDA and SCL Inputs	t_{IN}	Any pulse narrower than the Max value is suppressed			50	ns
SCL Falling Edge to SDA Output Data Valid	t_{AA}	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window			900	ns
Time the Bus Must be Free Before the Start of a New Transmission	t_{BUF}	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition	1300			ns
Clock LOW Time	t_{LOW}	Measured at the 30% of V_{DD} crossing	1300			ns
Clock HIGH Time	t_{HIGH}	Measured at the 70% of V_{DD} crossing	600			ns
Eighth Bit to ACK Bit Delay (Applies to reading ADC Output Data Only)	$I^2C\_t_{WAIT}$	Time between the rising edge of the clock pulse corresponding to the last bit of any byte, and the falling edge of the clock pulse corresponding to the Acknowledge bit	7			µs
START Condition Setup Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}	600			ns
START Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}	600			ns
Input Data Setup Time	$t_{SU:DAT}$	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}	100			ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window	20		900	ns
STOP Condition Setup Time	$t_{SU:STO}$	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}	600	17		ns
STOP Condition Hold Time	$t_{HD:STO}$	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}	600	45		ns
Output Data Hold Time	t_{DH}	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window	0	150		ns

Unless otherwise specified: T_A = +25°C, V_{BAT1} = V_{BAT2} = 48V, (VC_n - VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, control registers at default, V_{SS} = DGND = 0V, cell balancing is off. Voltages are with respect to V_{SS}. External components are per Pin Functionality.[1][2][3][4][5] (Cont.)

Parameter	Symbol	Test Conditions	Min[6]	Typ	Max[6]	Unit
SDA and SCL Rise Time	t_R	From 30% to 70% of V_{DD}	20+0.1xCb		300	ns
SDA and SCL Fall Time	t_F	From 70% to 30% of V_{DD}	20+0.1xCb		300	ns
Capacitive Loading of SDA or SCL	Cb	Total on-chip and off-chip	10		400	pF
SDA and SCL Bus Pull-Up Resistor Off-Chip	R_{PU}	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2kΩ~2.5kΩ For Cb = 40pF, max is about 15kΩ~20kΩ	1	4.7		kΩ
Output Buffer LOW Voltage	V_{OL}	I_{OL} = 2mA	0	0.02	0.4	V
Voltage Hysteresis	V_{hys}	I_{OL} = 2mA	0.05 xV_{DD}			V
Pin Leakage Current	I_{leak}				1	µA
Rise Time	t_{rSW}	30% to 70% of V_{DD}			150	ns
Fall Time	t_{fSW}	70% to 30% of V_{DD}			150	ns
Glitch Filtering	t_{glitch}	Pulses narrower than Min are ignored	50			ns

1. Applies to all measurements except for VTEMP, xT0, and xT1 that wait for VTEMP settling.
2. Drivers are open drain. V_{DD} is the power supply of the chip's digital IOs.
3. Pulse widths measured from the 0.3×V_{CC} crossing during the falling edge to the 0.7×V_{CC} crossing during the rising edge.
4. Timing selected to work with clock tolerances up to ±20% at both the master and the slave.
5. Values are for calculation purposes only and are not test limits. See the register descriptions in section 4 for details.
6. Compliance to datasheet limits is assured by one or more of the following methods: production test, characterization, and design. Recommended external components are listed in Pin Functionality.
7. Also see CSP and CSN Pins (24, 25) for typical circuit.

4. Typical Performance Graphs

T_A = +25°C, V_{BAT1} =V_{BAT2} = 48V, (VC_n- VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, averages = 1, V_{SS} = DGND = 0V, unless otherwise specified. Cell balancing is off.

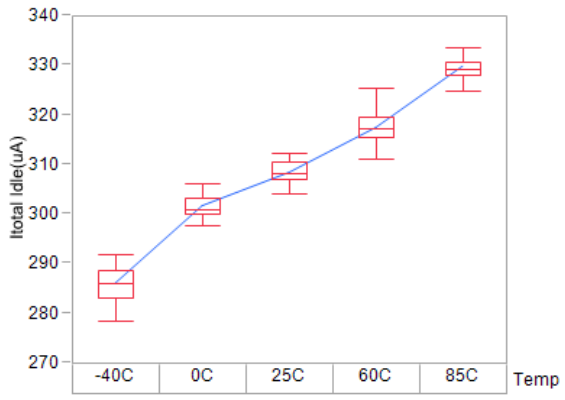


Figure 3. I_{TOT} IDLE Mode

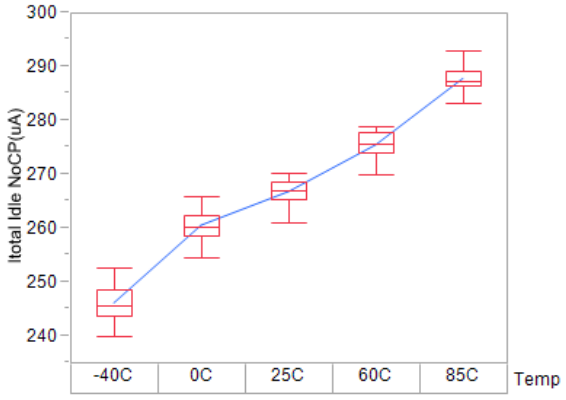


Figure 4. I_{TOT} IDLE Mode, CP Off

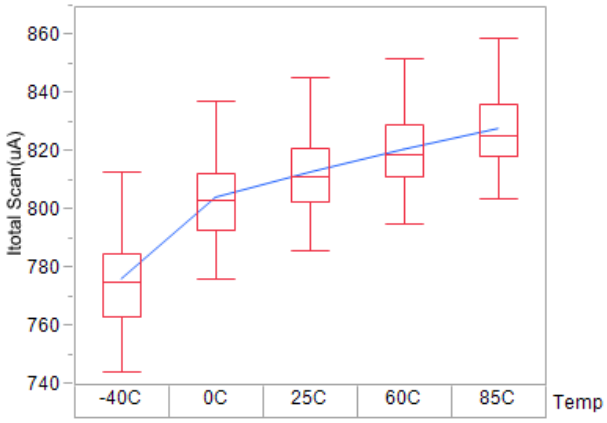


Figure 5. I_{TOT} SCAN Mode

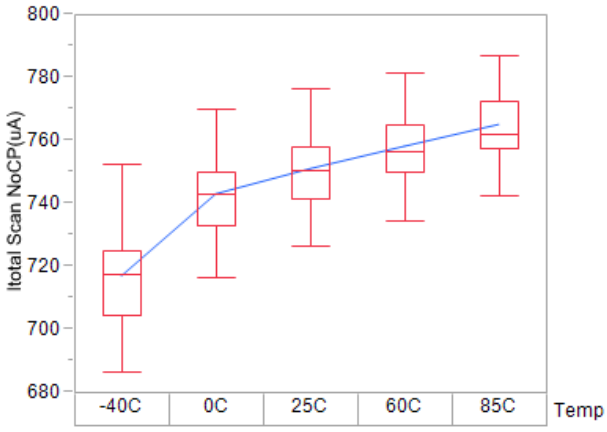


Figure 6. I_{TOT} SCAN Mode, CP Off

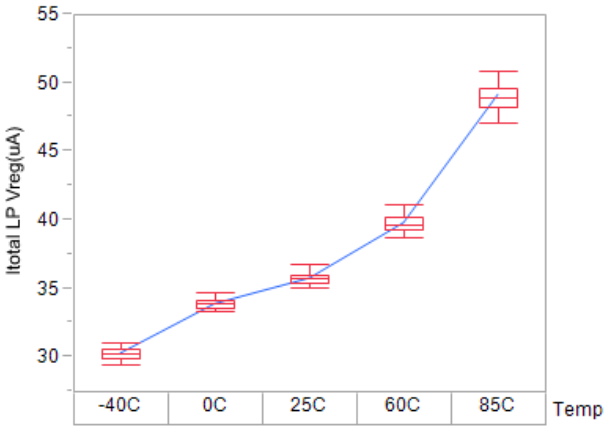


Figure 7. I_{TOT} LP Mode, LP Reg = 1

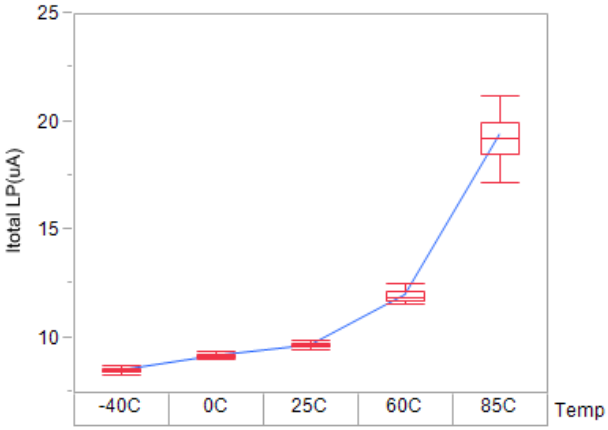


Figure 8. I_{TOT} LP Mode, LP Reg = 0

T_A = +25°C, V_{BAT1} =V_{BAT2} = 48V, (VC_n- VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, averages = 1, V_{SS} = DGND = 0V, unless otherwise specified. Cell balancing is off. (Cont.)

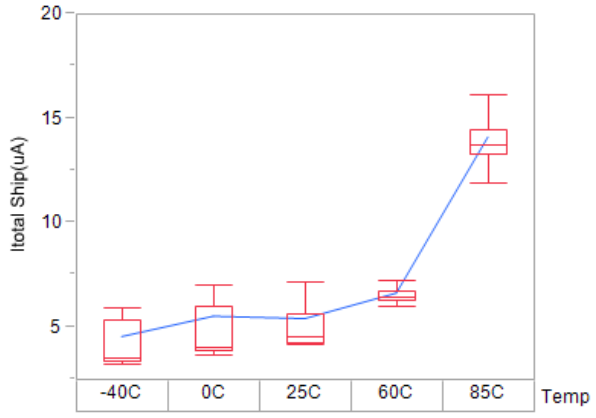


Figure 9. I_{TOT} SHIP Mode, LP Reg = 0

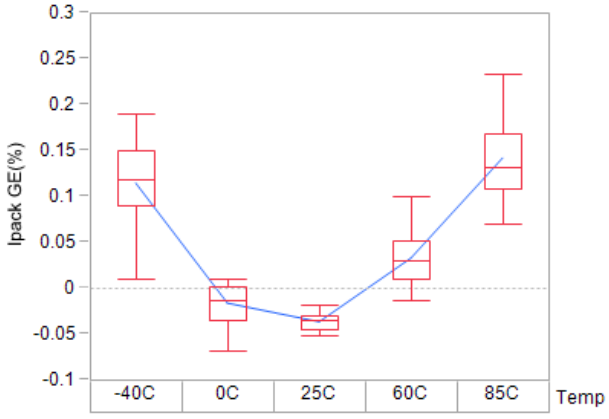


Figure 10. I_{PACK} Measurement Gain Error

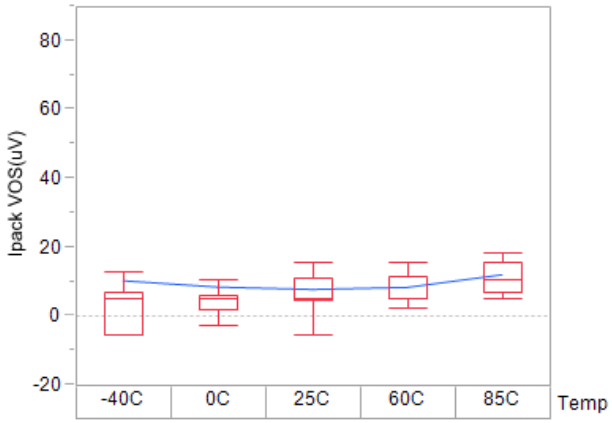


Figure 11. I_{PACK} Measurement Offset Voltage

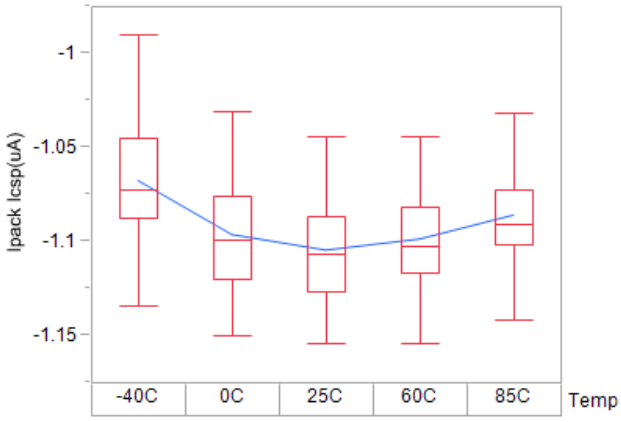


Figure 12. I_{CSP} Pin Measurement Input Current

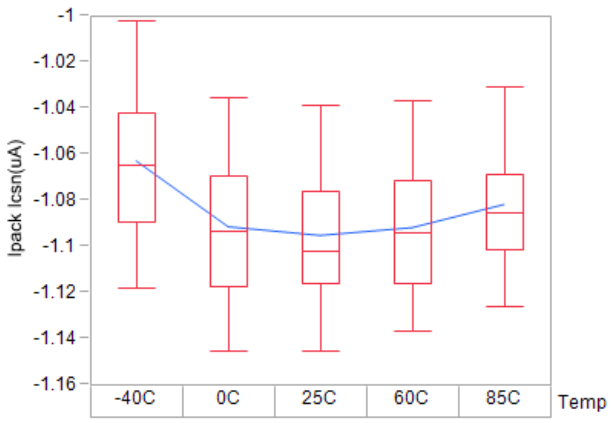


Figure 13. I_{CSN} Pin Measurement Input Current

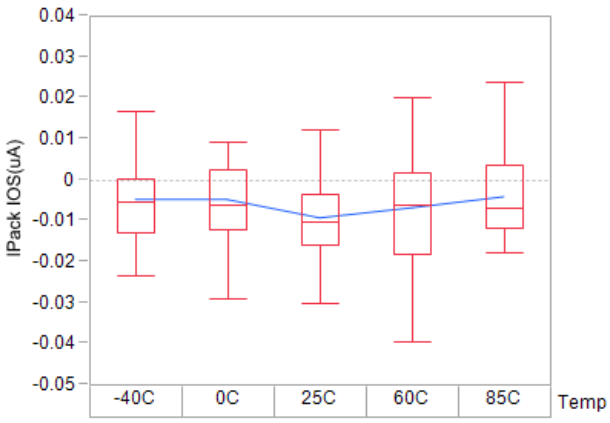


Figure 14. I_{PACK} Measurement Offset Current

T_A = +25°C, V_{BAT1} =V_{BAT2} = 48V, (VC_n- VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, averages = 1, V_{SS} = DGND = 0V, unless otherwise specified. Cell balancing is off. (Cont.)

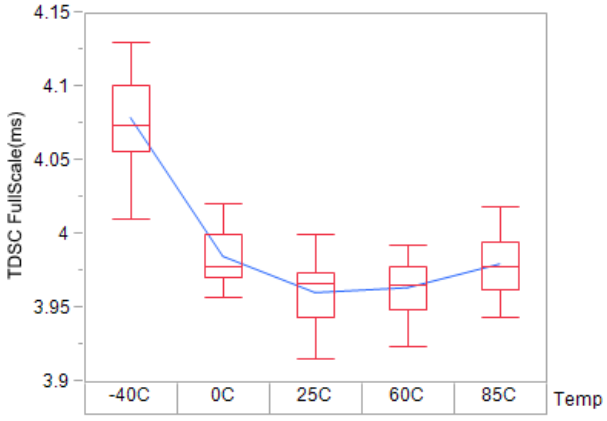


Figure 15. DSC Delay, Maximum Setting

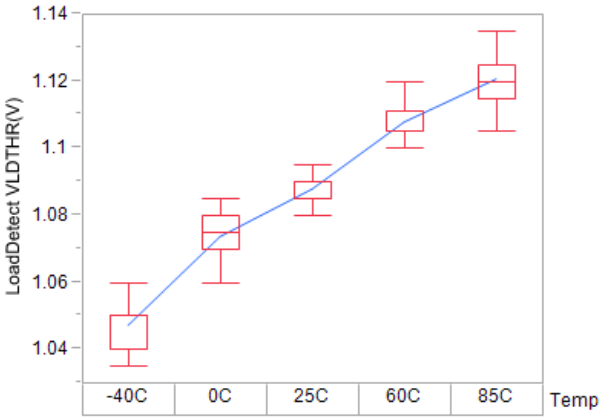


Figure 16. Load Detection Threshold

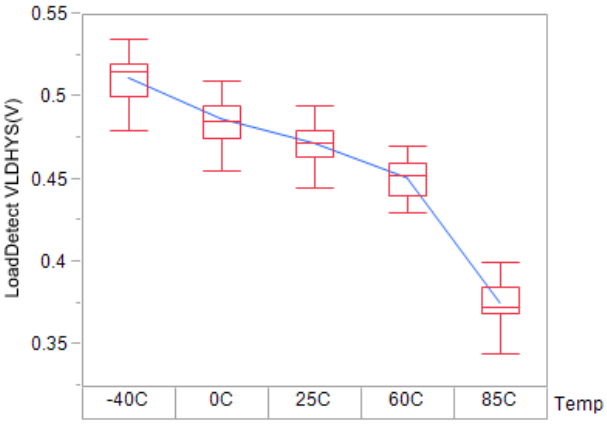


Figure 17. Load Detection Hysteresis

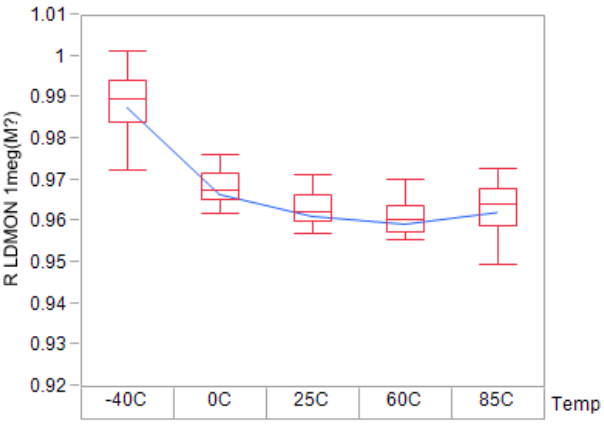


Figure 18. Load Monitor Pull-Up, ELD[1:0] = 01

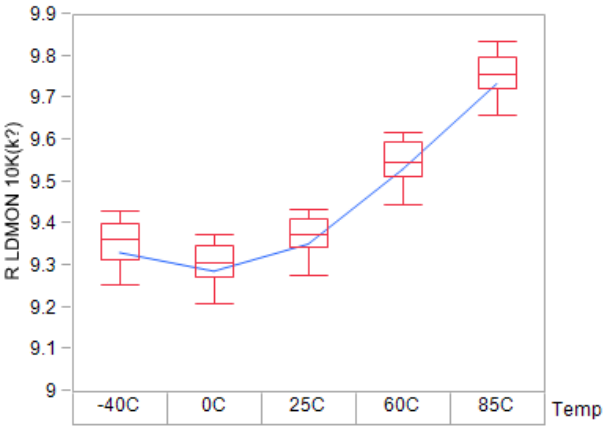


Figure 19. Load Monitor Pull-Up, ELD[1:0] = 10

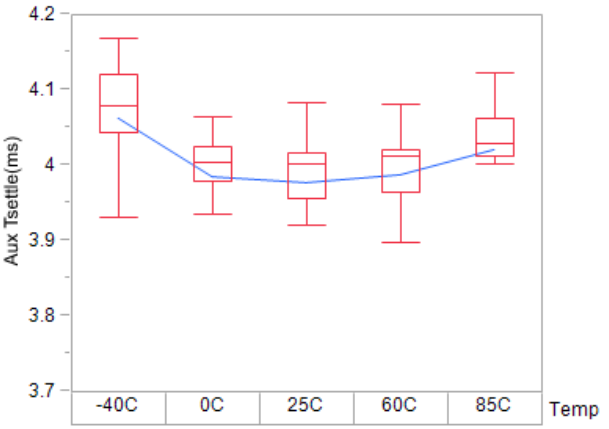


Figure 20. V_{TEMP} Settling Time

T_A = +25°C, V_{BAT1} =V_{BAT2} = 48V, (VC_n- VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, averages = 1, V_{SS} = DGND = 0V, unless otherwise specified. Cell balancing is off. (Cont.)

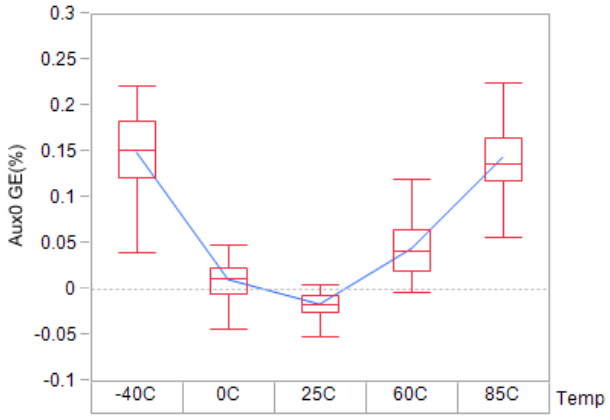


Figure 21. AUX0/xT0 Gain Error

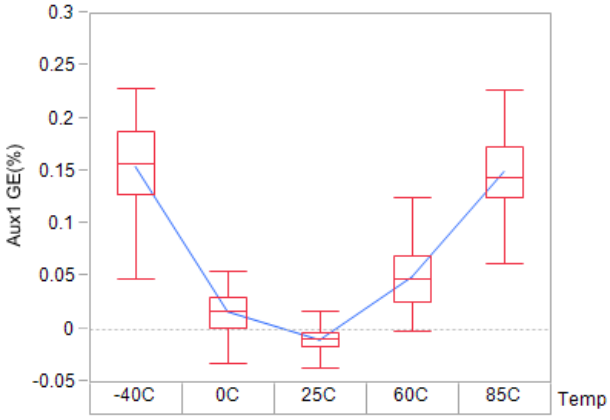


Figure 22. AUX1/xT1 Gain Error

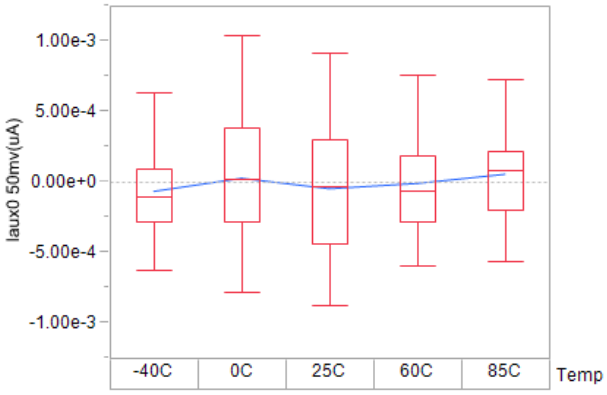


Figure 23. AUX0/xT0 Pin Input Current at 50mV

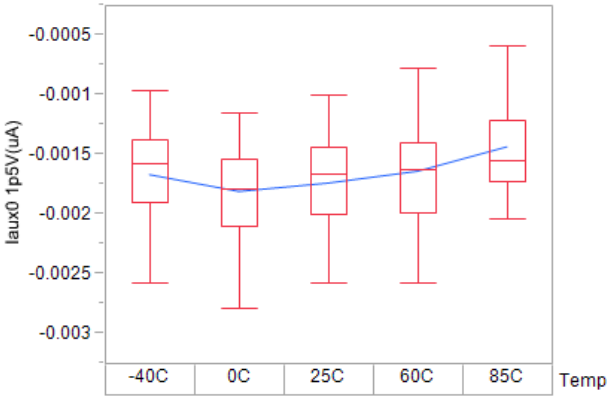


Figure 24. AUX0/xT0 Pin Input Current at 1.5V

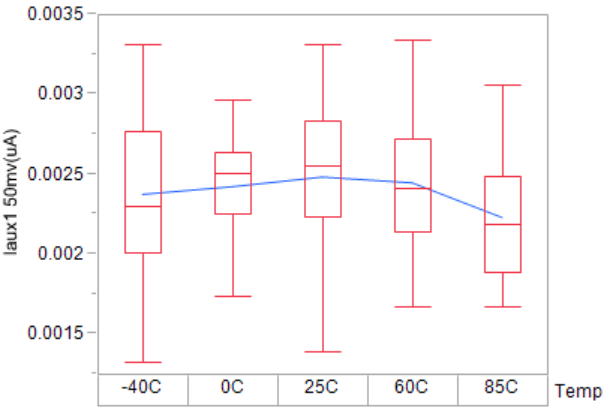


Figure 25. AUX1/xT1 Pin Input Current at 50mV

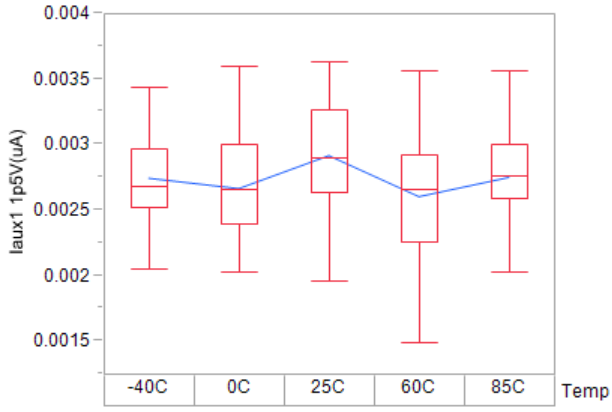


Figure 26. AUX1/xT1 Pin Input Current at 1.5V

T_A = +25°C, V_{BAT1} =V_{BAT2} = 48V, (VC_n- VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, averages = 1, V_{SS} = DGND = 0V, unless otherwise specified. Cell balancing is off. (Cont.)

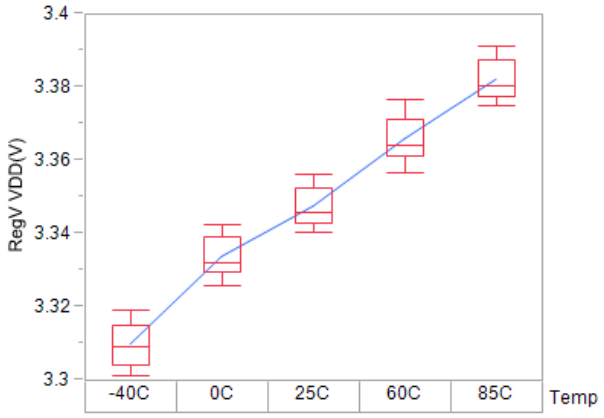


Figure 27. Regulation Voltage Accuracy

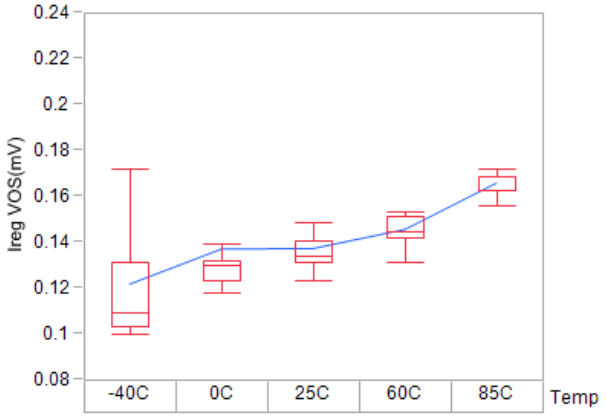


Figure 28. I_{REG} Measurement Offset

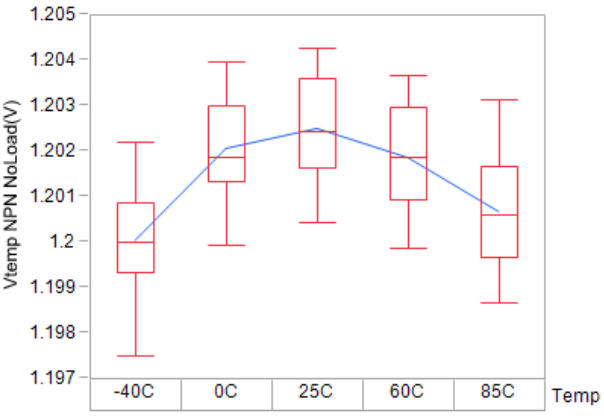


Figure 29. V_{TEMP} Voltage Accuracy (No Load)

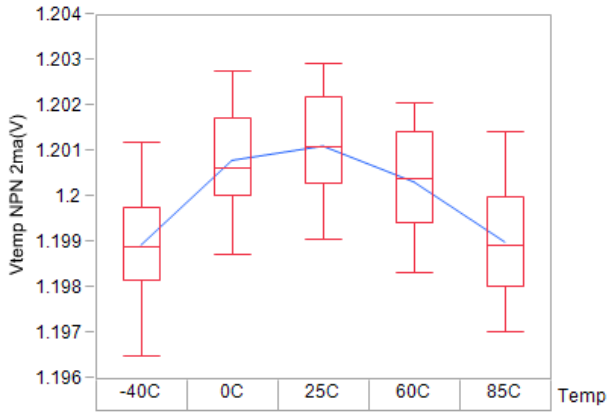


Figure 30. V_{TEMP} Voltage Accuracy (2mA Load)

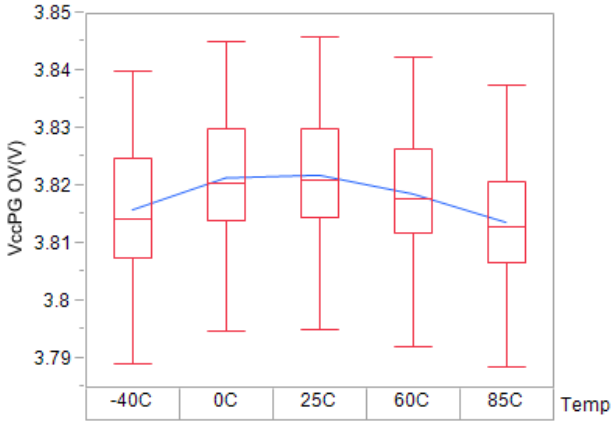


Figure 31. VCC PG OV Threshold

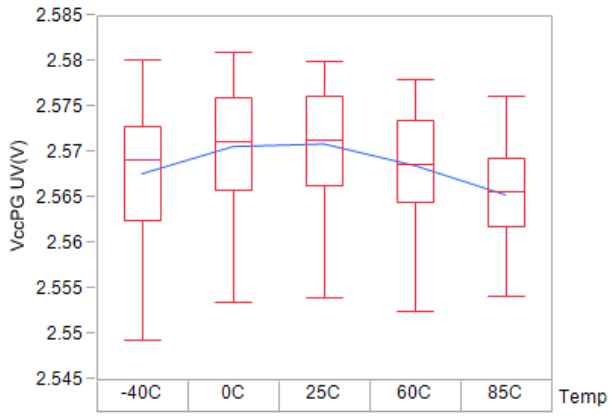


Figure 32. VCC PG UV Threshold

T_A = +25°C, V_{BAT1} =V_{BAT2} = 48V, (VC_n- VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, averages = 1, V_{SS} = DGND = 0V, unless otherwise specified. Cell balancing is off. (Cont.)

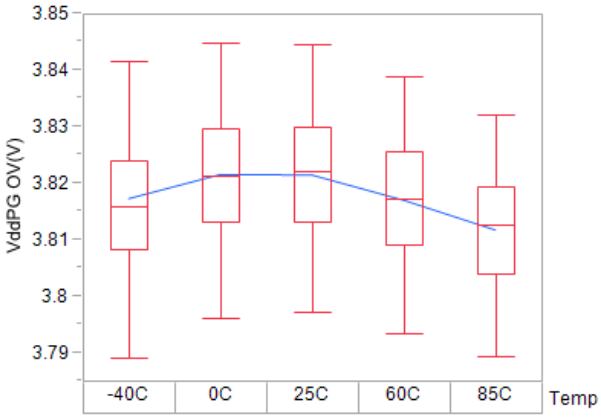


Figure 33. VDD PG OV Threshold

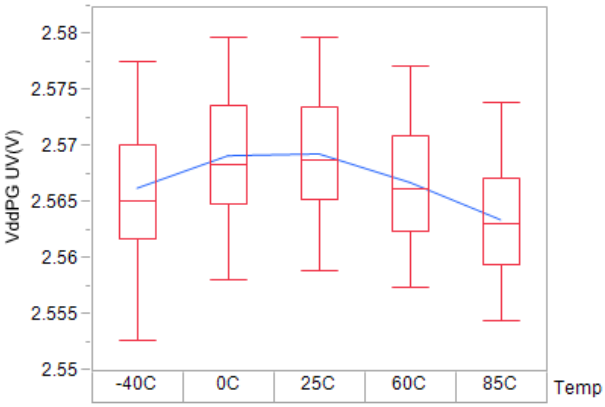


Figure 34. VDD PG OV Threshold

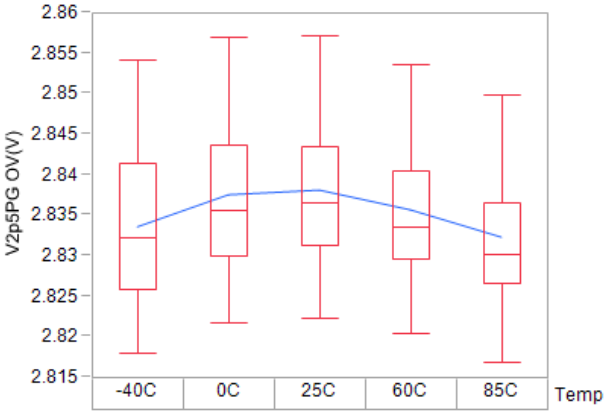


Figure 35. V2P5 PG OV Threshold

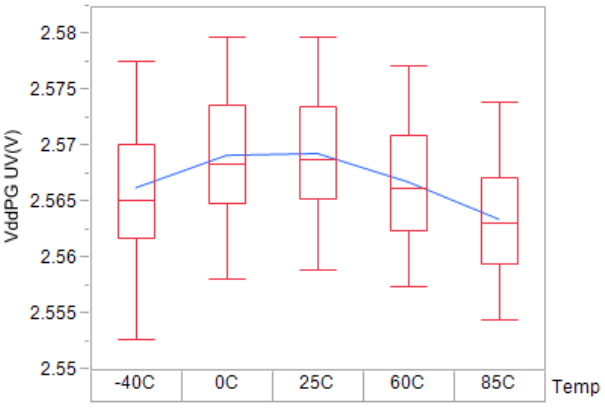


Figure 36. V2P5 PG UV Threshold

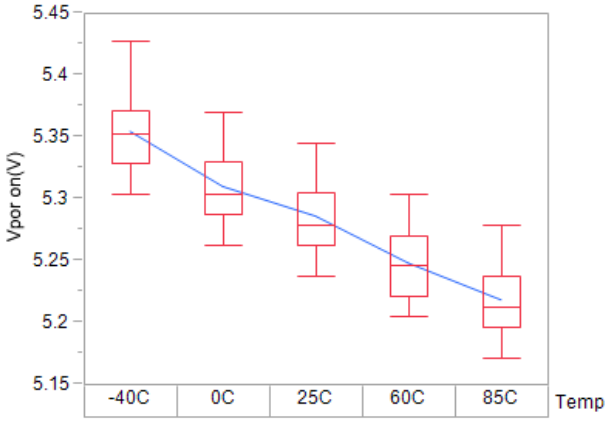


Figure 37. Power-On Reset ON Voltage (VBAT1)

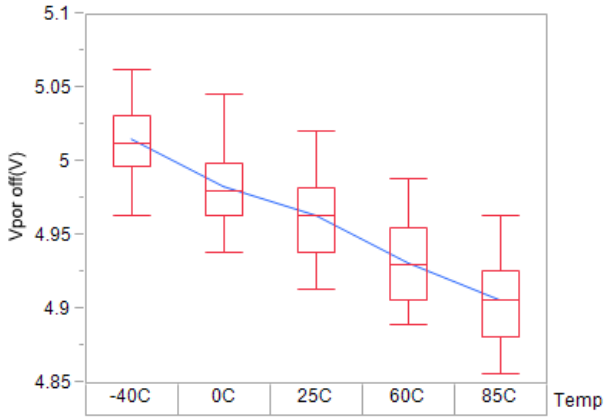


Figure 38. Power-On Reset OFF Voltage (VBAT1)

T_A = +25°C, V_{BAT1} =V_{BAT2} = 48V, (VC_n- VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, averages = 1, V_{SS} = DGND = 0V, unless otherwise specified. Cell balancing is off. (Cont.)

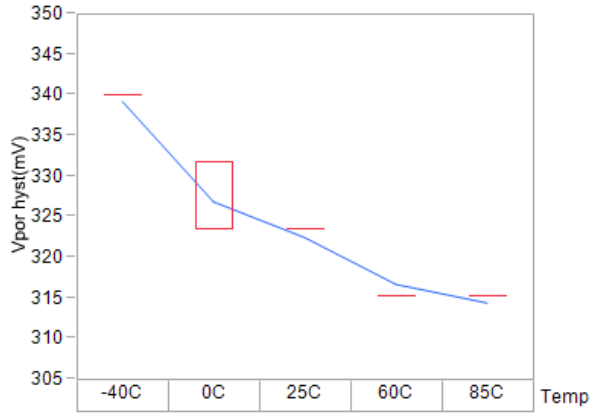


Figure 39. Power-On Reset Hysteresis

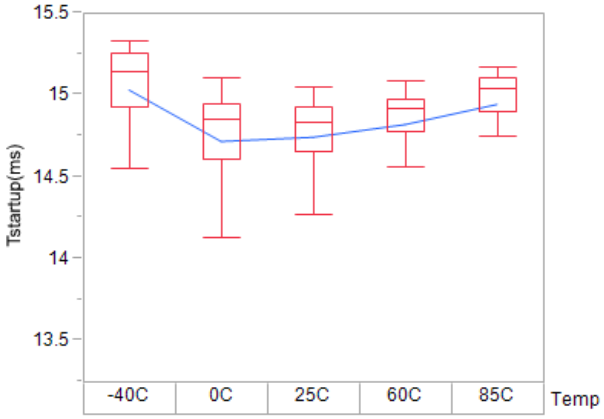


Figure 40. POR Startup Time To Measurement

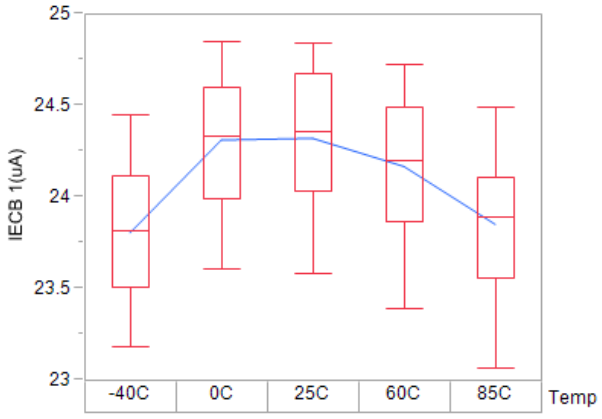


Figure 41. CB1 Pin Input Current (Active)

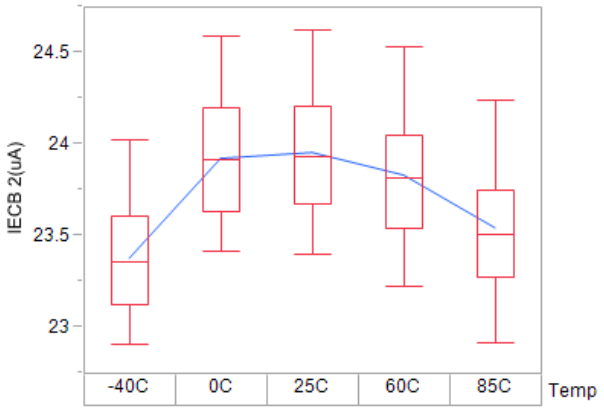


Figure 42. CB2 Pin Input Current (Active)

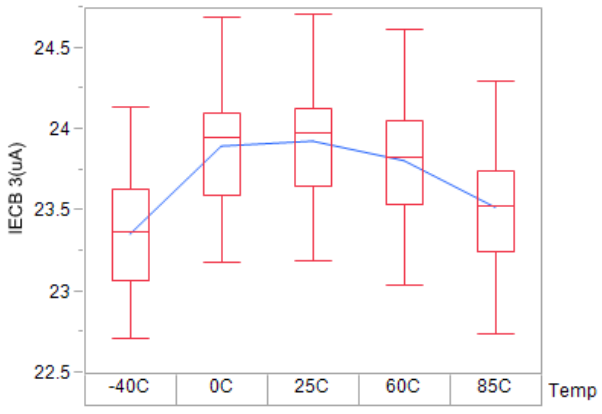


Figure 43. CB3 Pin Input Current (Active)

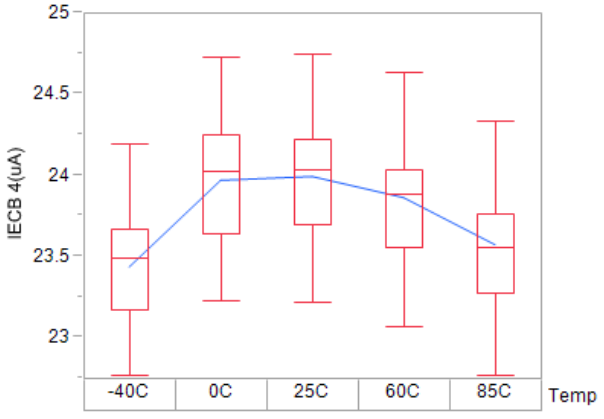


Figure 44. CB4 Pin Input Current (Active)

T_A = +25°C, V_{BAT1} =V_{BAT2} = 48V, (VC_n- VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, averages = 1, V_{SS} = DGND = 0V, unless otherwise specified. Cell balancing is off. (Cont.)

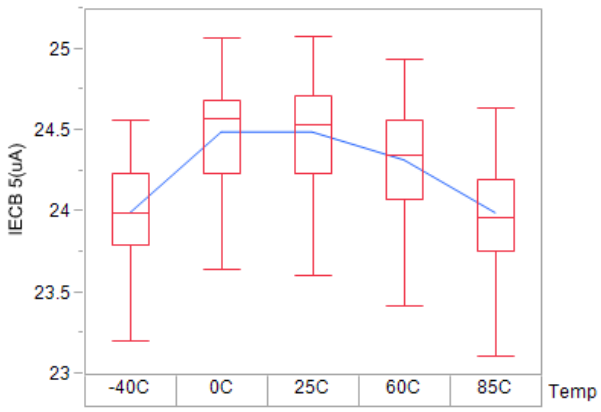


Figure 45. CB5 Pin Input Current (Active)

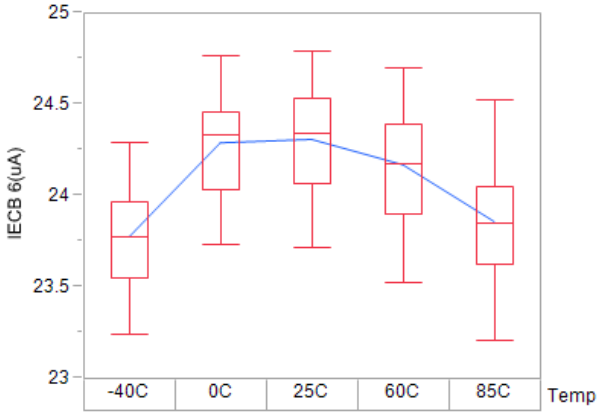


Figure 46. CB6 Pin Input Current (Active)

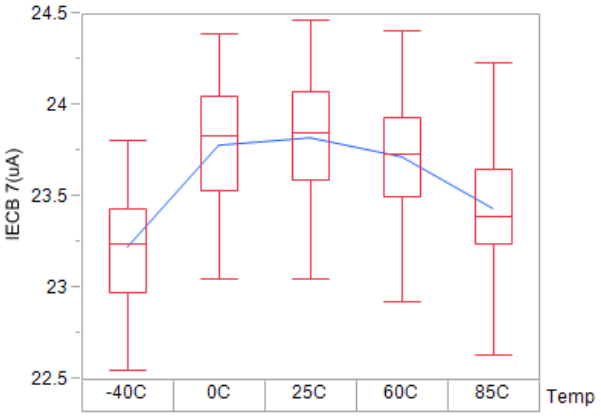


Figure 47. CB7 Pin Input Current (Active)

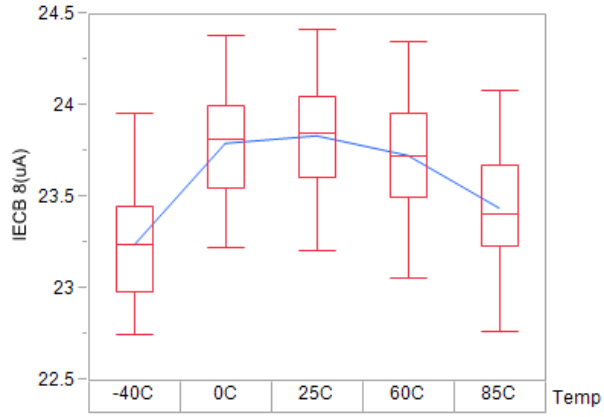


Figure 48. CB8 Pin Input Current (Active)

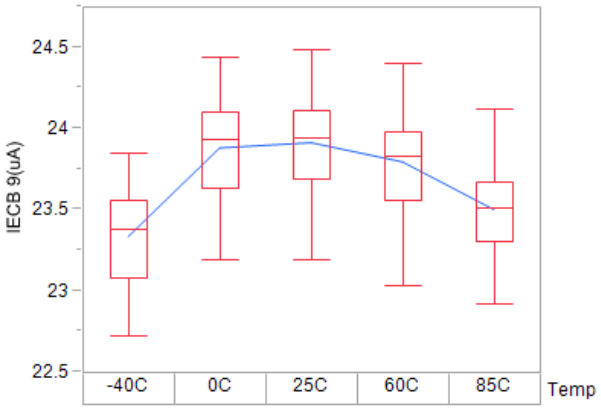


Figure 49. CB9 Pin Input Current (Active)

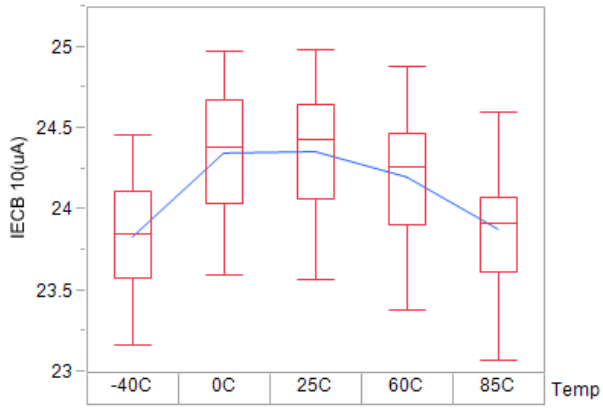


Figure 50. CB10 Pin Input Current (Active)

T_A = +25°C, V_{BAT1} =V_{BAT2} = 48V, (VC_n- VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, averages = 1, V_{SS} = DGND = 0V, unless otherwise specified. Cell balancing is off. (Cont.)

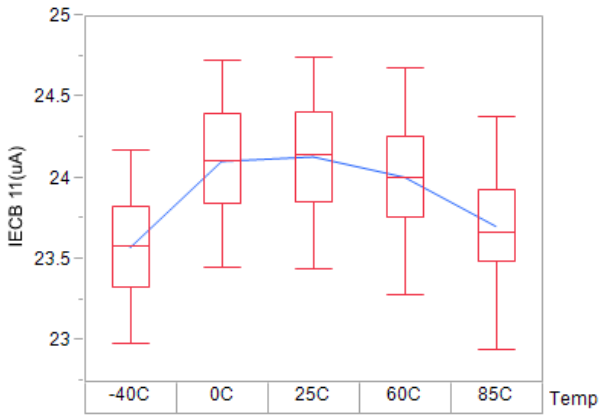


Figure 51. CB11 Pin Input Current (Active)

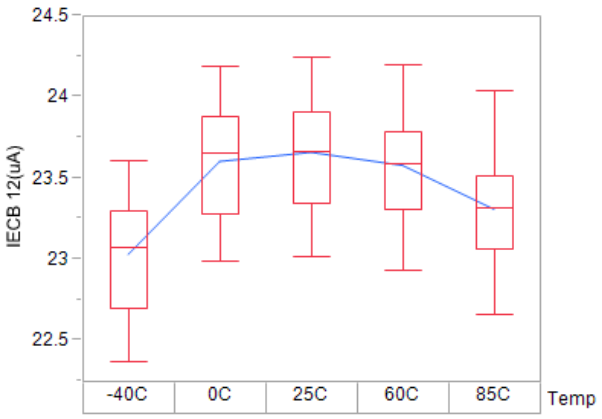


Figure 52. CB12 Pin Input Current (Active)

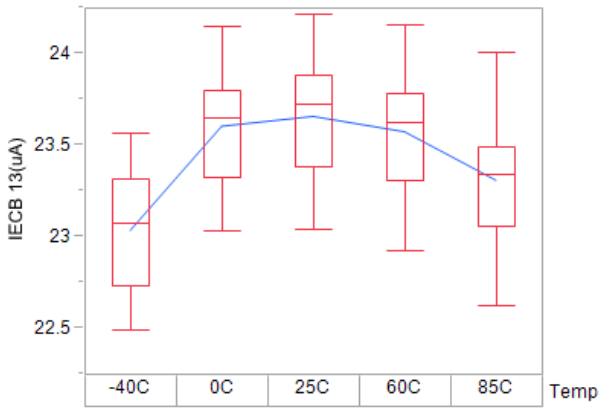


Figure 53. CB13 Pin Input Current (Active)

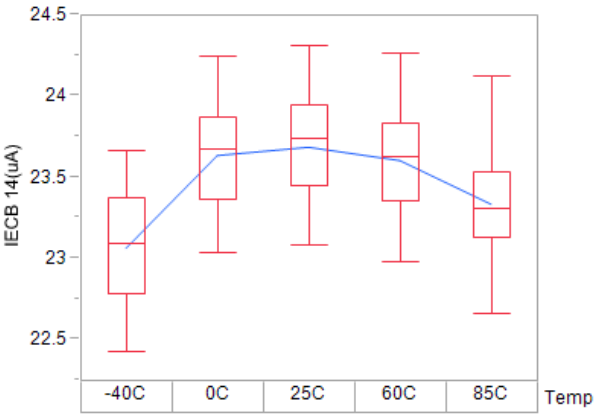


Figure 54. CB14 Pin Input Current (Active)

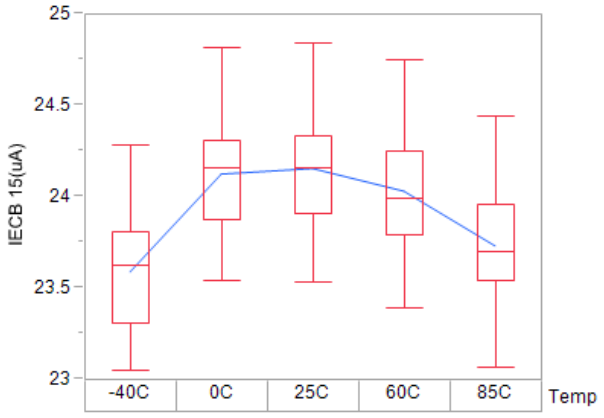


Figure 55. CB15 Pin Input Current (Active)

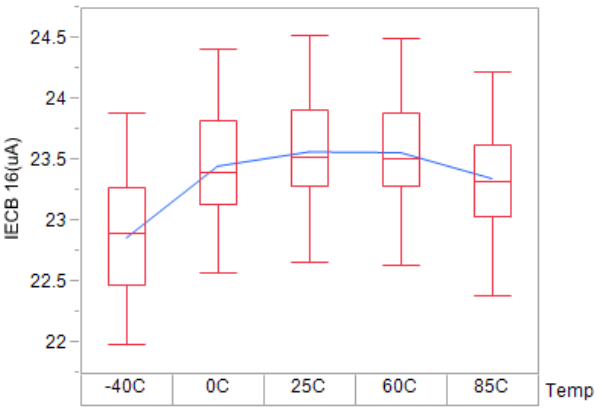


Figure 56. CB16 Pin Input Current (Active, CP On)

T_A = +25°C, V_{BAT1} =V_{BAT2} = 48V, (VC_n- VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, averages = 1, V_{SS} = DGND = 0V, unless otherwise specified. Cell balancing is off. (Cont.)

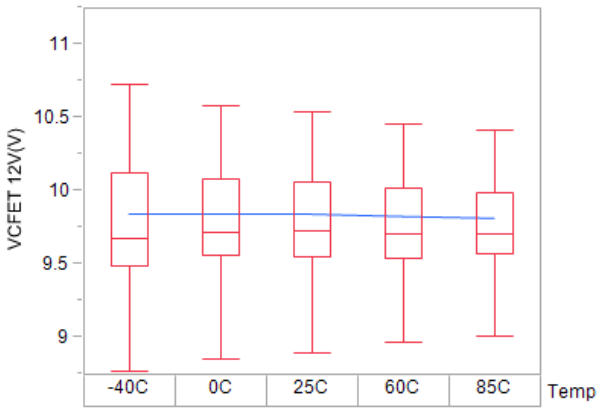


Figure 57. CFET Gate Drive Voltage at VBAT1 = 12V

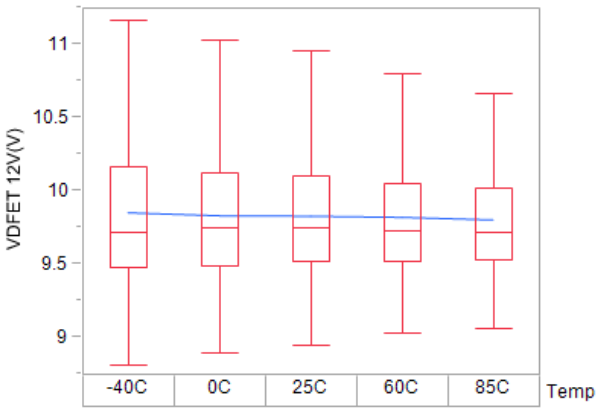


Figure 58. DFET Gate Drive Voltage at VBAT1 = 12V

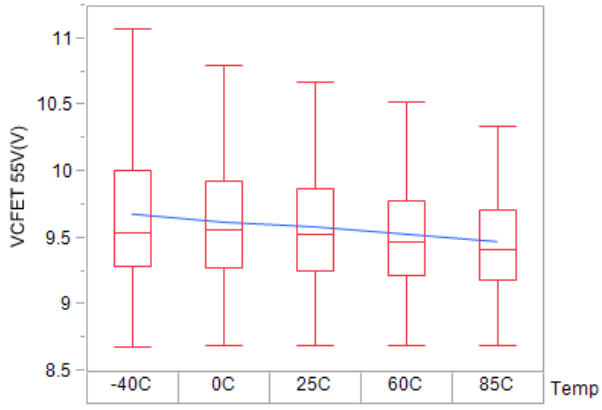


Figure 59. CFET Gate Drive Voltage at VBAT1 = 55V

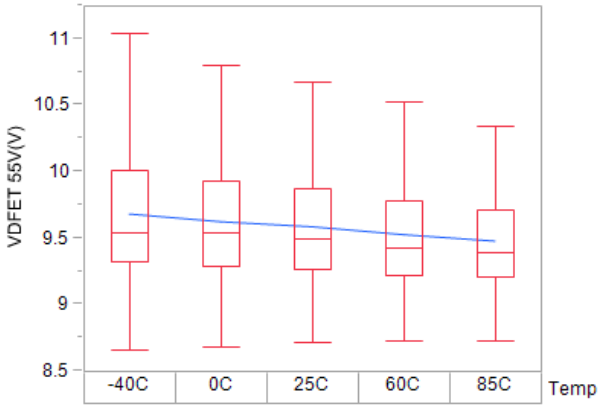


Figure 60. DFET Gate Drive Voltage at VBAT1 = 55V

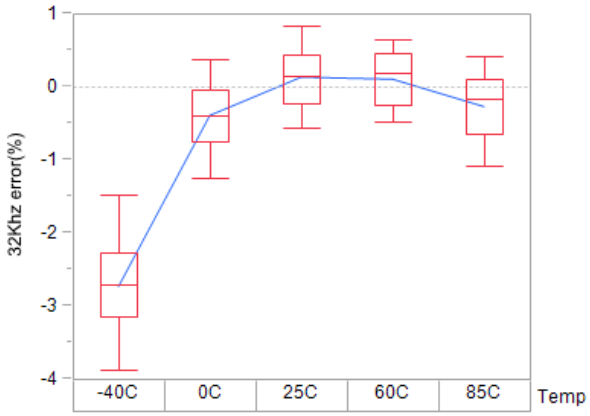


Figure 61. Internal 32kHz Oscillator Accuracy

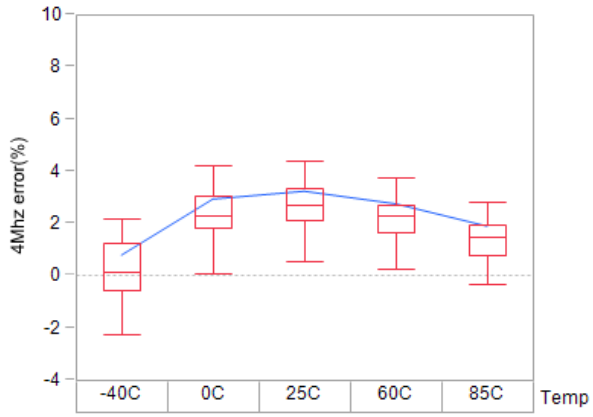


Figure 62. Internal 4MHz Oscillator Accuracy

T_A = +25°C, V_{BAT1} =V_{BAT2} = 48V, (VC_n- VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, averages = 1, V_{SS} = DGND = 0V, unless otherwise specified. Cell balancing is off. (Cont.)

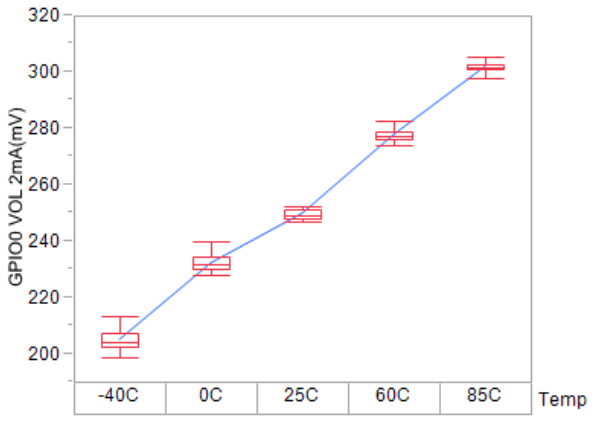


Figure 63. GPIO0 VOL at 2mA Load

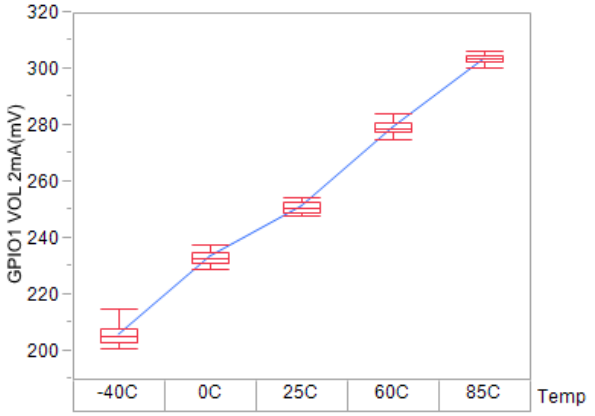


Figure 64. GPIO1 VOL at 2mA Load

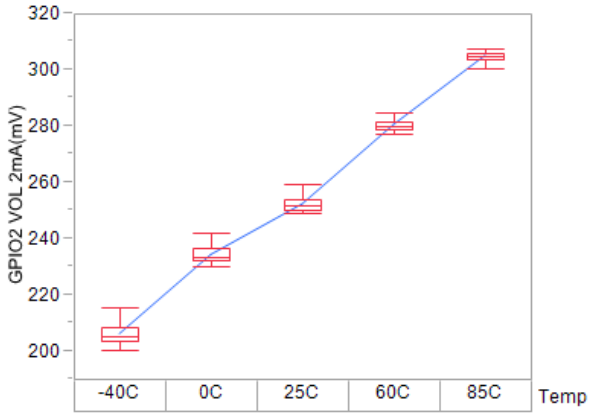


Figure 65. GPIO2 VOL at 2mA Load

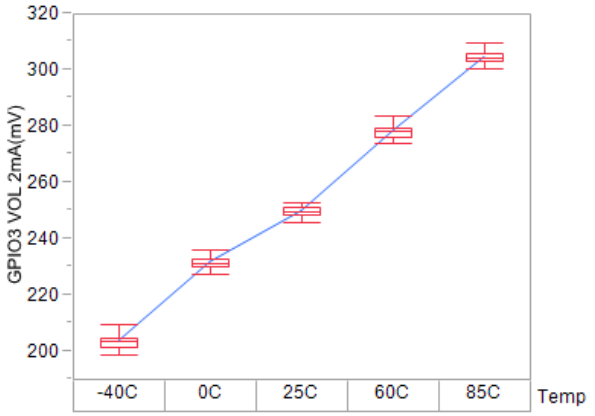


Figure 66. GPIO3 VOL at 2mA Load

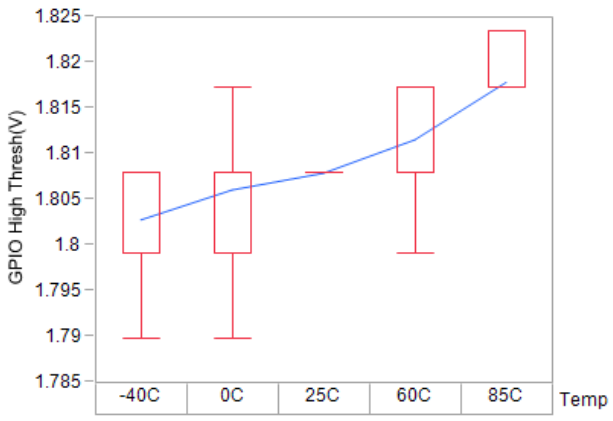


Figure 67. GPIO VIH

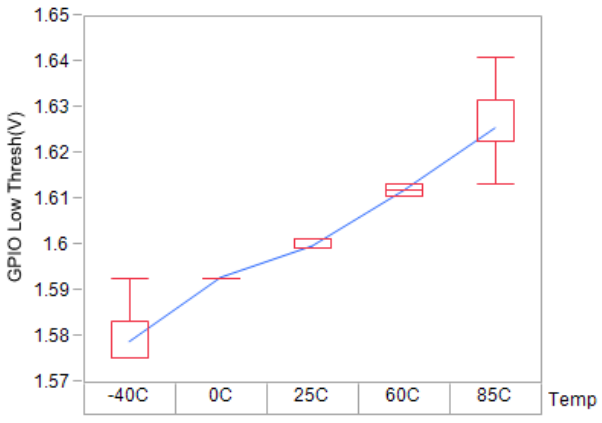


Figure 68. GPIO VIL

T_A = +25°C, V_{BAT1} =V_{BAT2} = 48V, (VC_n- VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, averages = 1, V_{SS} = DGND = 0V, unless otherwise specified. Cell balancing is off. (Cont.)

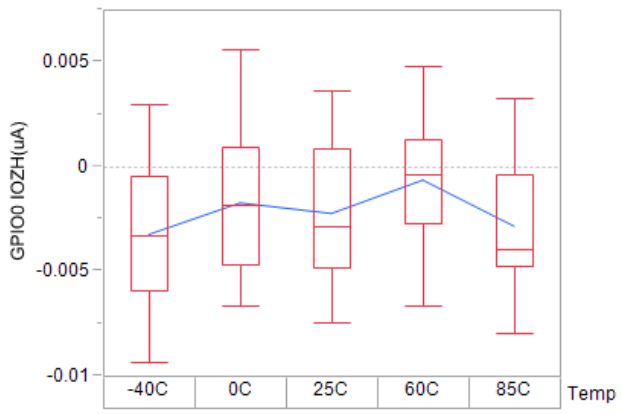


Figure 69. GPIO0 Leakage Current (3.3V)

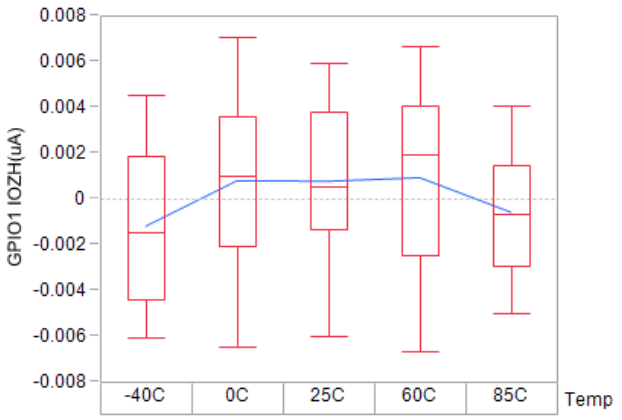


Figure 70. GPIO1 Leakage Current (3.3V)

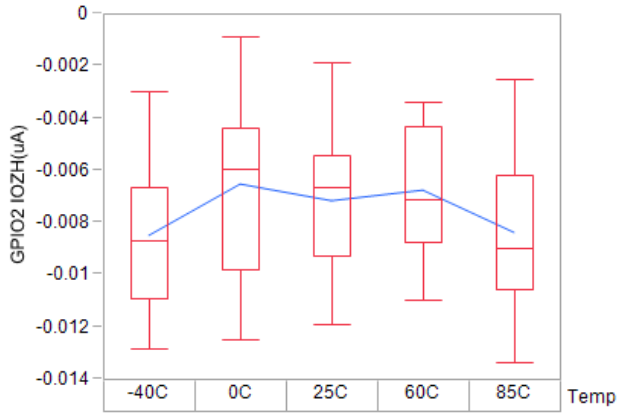


Figure 71. GPIO2 Leakage Current (3.3V)

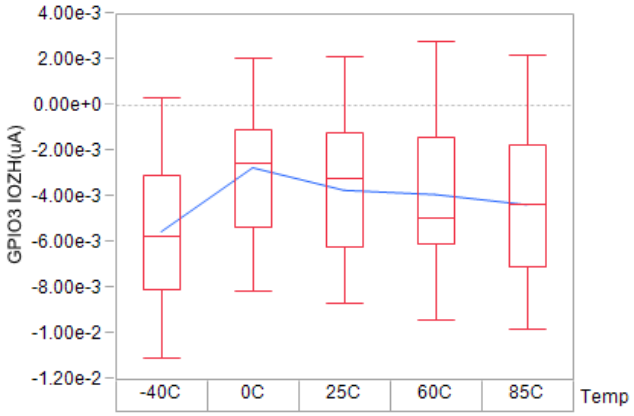


Figure 72. GPIO3 Leakage Current (3.3V)

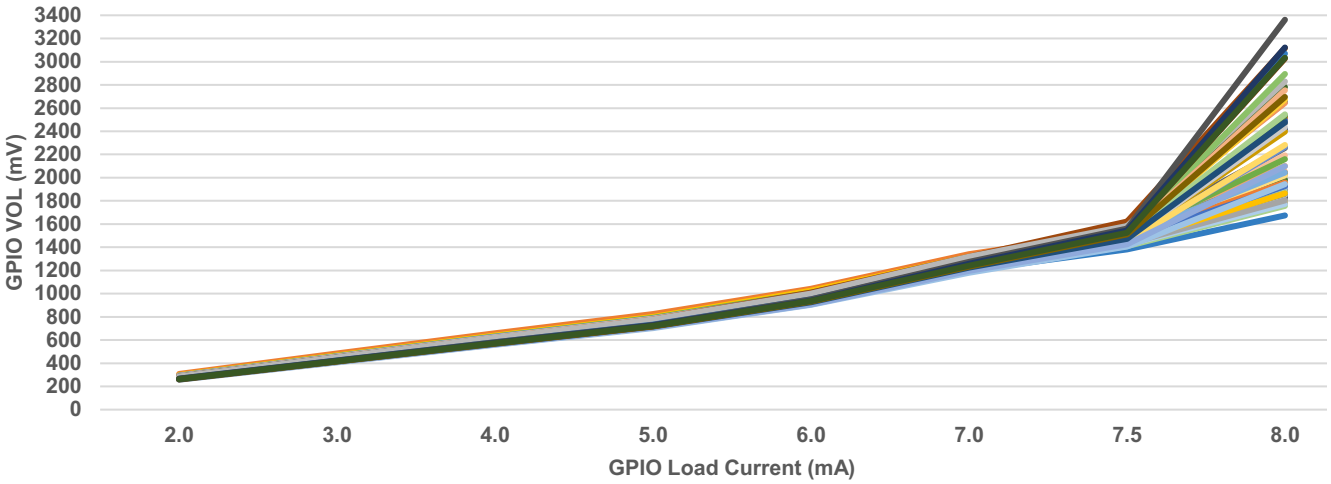


Figure 73. GPIO Sink Current vs Voltage

T_A = +25°C, V_{BAT1} =V_{BAT2} = 48V, (VC_n- VC_{n-1}) = 3V, V_{CC} = V_{DD} = 3.3V, averages = 1, V_{SS} = DGND = 0V, unless otherwise specified. Cell balancing is off. (Cont.)

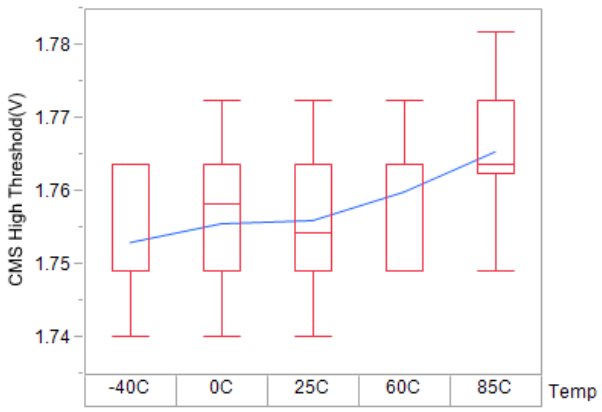


Figure 74. CMS0 Pin V_{IH}

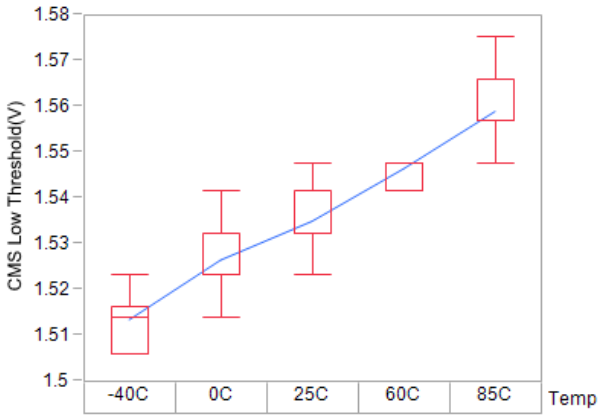


Figure 75. CMS0 Pin V_{IL}

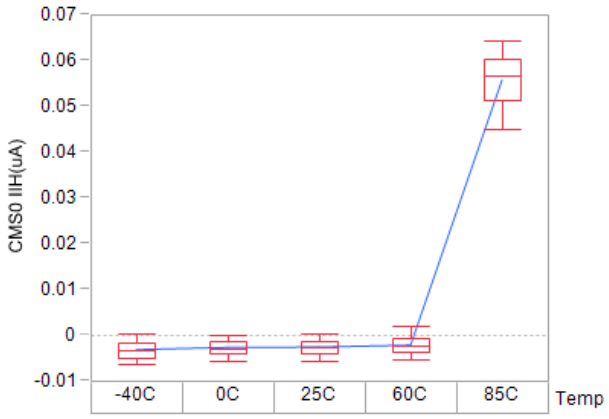


Figure 76. CMS0 Leakage Current (3.3V)

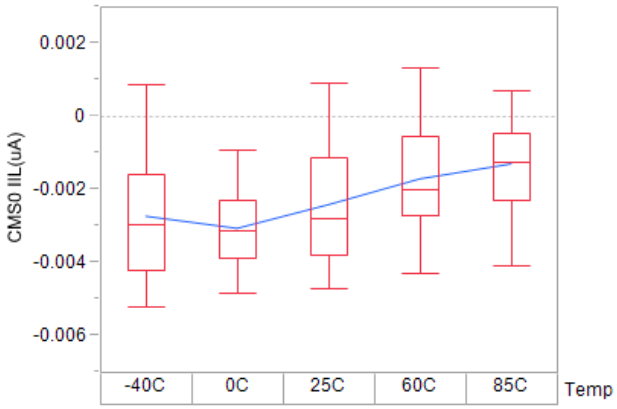


Figure 77. CMS0 Leakage Current (0V)

5. Registers

Each system register contains eight bits and is accessed using a 7-bit address plus an 8th bit that indicates a read or a write. For details about reading and writing registers, see Communication Interface and the register descriptions.

All system registers are listed in Table 1. Each register listing includes the address, register name, and a page number for more details, as well as a depiction of the contents with bit names, value at power-up or after the chip is reset (POR value), and the type of register follow (Read or Read/Write). The RAA489206 is configured for specific applications by a microcontroller accessing these registers.

The RAA489206 has a 16-bit ADC for voltage measurements. The outputs of many parameter readings use two 8-bit values to represent the digitized result. Register addresses of some readings are shown as two register values delimited with a comma. For example, 0x52, 53 are register addresses for the I_{PACK} voltage. Register 0x52 contains the MSB and register 0x53 contains the LSB. The 8-bit threshold registers are compared to the upper 8-bits of the 16-bit measurements.

The ranges and step-sizes listed for threshold and measurement registers are the ideal values to be used for calculation purposes. Threshold settings that would require operation outside of the recommended operating conditions are not supported. The usable measurement range is also limited by the recommended operating conditions and by non-idealities of the measurement channel. Measurement results registers may or may not reach the maximum or minimum for input voltages within the ideal voltage range listed.

Within some control registers are bits called Trigger bits that execute automatic sequences when set to 1. Triggered sequences are initiated by a 0 to 1 transition of a Trigger bit. See Trigger Bits for a detailed description of the use and limitations of Trigger bits.

Registers at addresses 0x83 through 0x89 contain Mask bits. Set Mask bits to 1 (default) to prevent the fault related to that bit from asserting the $\overline{ALRT}$ pin low. A Mask bit must be set to 0 to allow the assertion of the $\overline{ALRT}$ pin LOW when the fault related to that bit occurs.

Reserved bits (RSV) should be ignored when reading registers and set to 0 when writing to them.

Table 1. System Register List

Reg Add (Hex)	Register Name	Page	Bit Function								Power On Reset Value (Hex)	Type
			7 (MSB)	6	5	4	3	2	1	0 (LSB)		
Device Details												
00	System Information	37	Part ID				Product Revision			RSV	50	R
Global IC Controls												
01	Global Operation	37	SFT RST	RESET 2 IDLE	RCAL VOS Trigger	RCAL LPM EN	RCAL Scan	BUSY	SYS Scan SEL	SYS Scan Trigger	00	R/W
V_{CELL} and I_{PACK} Controls												
02	V_{CELL} Operation	39	V_{CELL} EN	DCHR WOV	CHRW UV	V_{CELL} Averages			Clear Faults and Status	V_{CELL} Trigger	80	R/W
03	I_{PACK} Operation	41	I_{PACK} EN	OW Update		I_{PACK} Averages			I_{DIR} Delay	I_{PACK} Trigger	80	R/W
04	Cell Select	43	Cell 16	Cell 15	Cell 14	Cell 13	Cell 12	Cell 11	Cell 10	Cell 9	FF	R/W
05			Cell 8	Cell 7	Cell 6	Cell 5	Cell 4	Cell 3	Cell 2	Cell 1	FF	R/W

Table 1. System Register List (Cont.)

Reg Add (Hex)	Register Name	Page	Bit Function 7 (MSB)	6	5	4	3	2	1	0 (LSB)	Power On Reset Value (Hex)	Type
30, 31--4E, 4F	V_{CELL} Voltage (16, 2-Byte read, Cells 1-16)	43	Step: 73.55µV; Range: 36.77µV to 4.820V								00 00	R
50, 51	V_{CELL} Max Delta Voltage	43	Two-Byte Read; Step 73.55µV; Range 36.77µV to 4.820V								00 00	R
52, 53	I_{PACK} Voltage	43	Two-Byte Read; Step 10.51µV; Range ±344.28mV								00 00	R
54 to 57	I_{PACK} Timer (4-byte read)	44	Step 15ms; Range: 0 to 2.043 years								00 00 00 00	R
V_{CELL} Detectors												
06	V_{CELL} OV Threshold	44	Step 18.83mV; Range 18.79mV to 4.820V								FF	R/W
07	V_{CELL} UV Threshold	44	Step 18.83mV; Range 36.77µV to 4.801V								00	R/W
08	V_{CELL} Max Delta Threshold	45	Step 18.83mV; Range 18.79mV to 4.820V								FF	R/W
09	Fault Delay	45	AUX Pull-up	ΔV_{CELL} Fault Delay	Other Fault Delay	ETAUX Fault Delay	V_{CELL} Fault Delay				00	R/W
I_{PACK} Detectors												
0A	Discharge Short-Circuit (DSC) Current Threshold	47	RSV	RSV	RSV	RSV	Step: -20.083mV; Range: -321.33mV to -40.167mV				0F	R/W
0B	Discharge Overcurrent (DOC) Threshold	48	Step -1.345mV; Range -342.95mV to -5.25µV								FF	R/W
0C	DSC Delay	48	RSV	Step 31.25µs; Range: 0 to 4000µs							00	R/W
0D	OC Delay	49	DOC Delay: Range 1 to 16 Scans				COC Delay: Range 1 to 16 Scans				00	R/W
0E	Load/Charge Operation	50	CFD	ELD		ELR	CPWR	FCDC	LDLP	RSV	B4	R/W
0F	Charge Overcurrent (COC) Threshold	53	Step 1.345mV; Range: 5.25µV to 342.95mV								FF	R/W
External Temperature/Auxiliary Port (ETAUX) Controls												
11	ETAUX Operation	54	ETAUX EN		RSV	ETAUX Average			RSV	ETAUX Trigger	C0	R/W
12	GPIO and $\overline{ALRT}$ Operation	56	$\overline{ALRT}$ Assert	$\overline{ALRT}$ Pulse EN	GPIO Config	GPIO STATUS					1F	R/W
58,59 5A,5B	ETAUX 0,1 Voltage (Four 8-bit reads)	57	Step: 24.51µV; Range: 12.26µV to 1.6067V								00 00	R
External Temperature/Auxiliary Port (ETAUX) Detectors												
13	DUT0 Limit	58	Step: 6.276mV; Range: 6.264mV to 1.6067V								FF	R/W
14	DOT0 Limit	58	Step: 6.276mV; Range: 6.264mV to 1.6067V								00	R/W

Table 1. System Register List (Cont.)

Reg Add (Hex)	Register Name	Page	Bit Function 7 (MSB)	6	5	4	3	2	1	0 (LSB)	Power On Reset Value (Hex)	Type
15	CUT0 Limit	58	Step: 6.276mV; Range: 6.264mV to 1.6067V								FF	R/W
16	COT0 Limit	58	Step: 6.276mV; Range: 6.264mV to 1.6067V								00	R/W
17	DUT1 Limit	58	Step: 6.276mV; Range: 6.264mV to 1.6067V								FF	R/W
18	DOT1 Limit	58	Step: 6.276mV; Range: 6.264mV to 1.6067V								00	R/W
19	CUT1 Limit	58	Step: 6.276mV; Range: 6.264mV to 1.6067V								FF	R/W
1A	COT1 Limit	58	Step: 6.276mV; Range: 6.264mV to 1.6067V								00	R/W
Internal Temperature												
22	IOTW Threshold	59	Internal Temp Warning: Step 0.839°C; Range: -63.7°C to +151.11°C								51	R/W
23	IOTF Threshold	59	Internal Temp Fault: Step 0.839°C; Range: -63.7°C to +151.11°C								45	R/W
5E	Internal Temperature	60	Step 0.839°C; Range: -63.7°C to +151.11°C								00	R
Voltage Regulator												
1B	V_{REG} Operation	61	Communications Timeout		UPDATE Other		LD DELAY		LP REG	VREG Trigger	F0	R/W
1C	V_{VCC} Minimum Threshold	62	Step 25.104mV; Range: 12.55mV to 6.414V								00	R/W
1D	I_{REGOC1} Threshold	63	(SCAN and IDLE modes); Step: 1.345mV; Range: 1.34mV to 344.28mV								FF	R/W
1E	I_{REGOC2} Threshold	63	(LOW POWER Mode); Step: 1.345mV; Range: 1.34mV to 344.28mV								FF	R/W
5F	V_{TEMP} Voltage	63	Step 3.138mV; Range; 0.80491V to 1.60511V								00	R
60	V_{CC} Voltage	64	Step 25.104mV; Range: 12.55mV to 6.414V								00	R
61, 62	I_{REG} Voltage (Two 8-Bit Reads)	64	Step 10.51µV; Range 5.25µV to 344.28mV								00 00	R
V_{BAT1} Controls												
1F	V_{BAT1} Operation	64	V_{BAT1} EN	I_{TEMP} EN	I_{TEMP} Trigger	Other Averages			Comm TO EN	V_{BAT1} Trigger	C2	R/W
20	OV_{BAT1} Threshold	66	Step: 301.25mV; Range: 300.66mV to 77.12V								FF	R/W
21	UV_{BAT1} Threshold	67	Step: 301.25mV; Range: 300.66mV to 77.12V								00	R/W
5C, 5D	V_{BAT1} Voltage	66	(Two 8-bit reads) Step: 1.177mV; Range: 0.588mV to 77.12V								00 00	R
Power FET Controls and Open-Wire												
24	Power FET Operation	68	CPMP EN	OW EN	OW Trigger	CELL CON	V_{BAT1} CON	ETAUX CON	DFET EN	CFET EN	5C	R/W
CELL Balancing Controls												
25	CB Operation	71	CB EN	AUTO CB EN	CB Config	CB Trigger	IEOC EN	CB Mask	CB EOC	CB CHRG	01	R/W
26	CB Cell State (2 8-bit reads/writes)	74	Cell 16	Cell 15	Cell 14	Cell 13	Cell 12	Cell 11	Cell 10	Cell 9	00	R/W
27			Cell 8	Cell 7	Cell 6	Cell 5	Cell 4	Cell 3	Cell 2	Cell 1	00	R/W
28	Cell Balance On Time	76	Step: 8 Range 0 to 1016							Unit	00	R/W

Table 1. System Register List (Cont.)

Reg Add (Hex)	Register Name	Page	Bit Function 7 (MSB)	6	5	4	3	2	1	0 (LSB)	Power On Reset Value (Hex)	Type
29	Cell Balance Off Time	76	Step: 8 Range 0 to 1016							Unit	00	R/W
CELL Balancing Detectors												
2A	CB Min Delta Threshold	74	Step 4.707mV; Range: 4.67mV to 1.20497V								00	R/W
2B	CBMAX Threshold	75	Step 18.828mV; Range: 18.79mV to 4.820V								FF	R/W
2C	CBMIN Threshold	75	Step 18.828mV; Range: 36.77µV to 4.801257V								00	R/W
2D	VEOC Threshold	76	Step 18.828mV; Range: 18.79mV to 4.820V								FF	R/W
10	EOC Current Threshold (IEOC)	76	Step 1.345mV; Range: 5.25µV to 342.95mV								00	R/W
System Faults and Indicators												
63	Priority Faults	78	VCCF	OWF	IOTF	COCF	DOCF	DSCF	UVF	OVF	00	R/W
64	ETAUX Faults	80	COT1	CUT1	DOT1	DUT1	COT0	CUT0	DOT0	DUT0	00	R/W
65	Other Faults	82	VBOVF	VBUVF	CPMP NRDY	OW xT1	OW xT0	OW V_{BAT1}	OW VSS	CRCF	20	R/W
66	CB Status	84	BAT FULL	IOTW	IEOC	VEOC	DVCF	2HI2CB	2LO2CB	NEED CB	00	R/W
67	Status	86	DCHRGI	CHRGI	CH PRESI	LD PRESI	OTHER FAULTS	IREG1	IREG2	VTMPF	00	R/W
68	Open-Wire Status (Two Bytes)	87	OW16	OW15	OW14	OW13	OW12	OW11	OW10	OW9	00	R/W
69			OW8	OW7	OW6	OW5	OW4	OW3	OW2	OW1	00	R/W
83	Priority Faults Mask	80	VCCF MASK	OWF MASK	IOTF MASK	COCF MASK	DOCF MASK	DSCF MASK	UVF MASK	OVF MASK	FF	R/W
84	ETAUX Faults Mask	81	COT1 MASK	CUT1 MASK	DOT1 MASK	DUT1 MASK	COT0 MASK	CUT0 MASK	DOT0 MASK	DUT0 MASK	FF	R/W
85	Other Faults Mask	83	VBOVF MASK	VBUVF MASK	CPMP NRDY MASK	RSV	RSV	RSV	CRCF MASK	BUSY MASK	FF	R/W
86	CB Status Mask	85	BAT FULL MASK	IOTW MASK	IEOC MASK	VEOC MASK	DVCF MASK	2HI2CB MASK	2LO2CB MASK	NEED CB MASK	FF	R/W
87	Status Mask	87	DCHRGI MASK	CHRGI MASK	CH PRESI MASK	LD PRESI MASK	OTHER FAULTS MASK	IREG1 MASK	IREG2 MASK	VTMPF MASK	FF	R/W
88	Open-Wire Mask (Two Bytes)	87	OWM Cell16	OWM Cell15	OWM Cell14	OWM Cell13	OWM Cell12	OWM Cell11	OWM Cell10	OWM Cell9	FF	R/W
89			OWM Cell8	OWM Cell7	OWM Cell6	OWM Cell5	OWM Cell4	OWM Cell3	OWM Cell2	OWM Cell1	FF	R/W
System Operation												
2E	Scan Operation	99	System Mode		LOW POWER Timer			Scan Delay			1B	R/W

5.1 Device Details

5.1.1 0x00 - Product ID Register (R)

The 1-byte Product Identification register contains information about the die and is read only.

Table 2. 0x00 Product ID Register

Bits	D[7:4]	D[3:1]	D[0]
Bit Name	Part ID	Revision	RSV
Default	1111	XXX	X

5.1.1.1 0x00.7:4 Part ID

The bit value of the Part ID represents the last two digits of the part ID minus one.

5.1.1.2 0x00.3:1 Product Revision

The product revision is indicated by the value of this register.

5.2 Global Controls

5.2.1 0x01 - Global Operation

The 1-byte Global Operation register includes controls and status of the overall state of the RAA489206.

Table 3. 0x01 Operation Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	SFT RST	RST2IDLE	RCAL V_{OS} Trigger	RCAL LPM	RCAL Scan	BUSY	Scan Sel	System Trigger
Default	0	0	0	0	0	0	0	0

5.2.1.1 0x01.7 - Soft Reset

Setting the Soft Reset bit of the Operation register to 1 resets all register values back to factory defaults, including data registers. All counters are set to 0, all timers and faults are cleared, and the System mode is set to IDLE. A low voltage offset calibration is performed, the power and cell balancing FETs are turned off, and the state machines are reset. This bit is cleared on completion.

5.2.1.2 0x01.6 - Reset to IDLE

When set to 1, the Reset to IDLE bit of the Operation register stops all state machines and moves the chip state to IDLE mode when receiving a stop bit. This command sets all counters to 0 and clears all timers and faults. The power and cell balancing FETs are turned off. The state machines are reset. All other register settings are not affected by this command and remain unchanged. This bit is cleared on completion.

5.2.1.3 0x01.5 - Recalibrate V_{OS} Trigger

For this bit, a transition from 0 to 1 in IDLE mode initiates a low voltage offset recalibration. Low voltage offset affects the V_{BAT1}, V_{VCC}, V_{TEMP}, IT, xT0, and xT1 measurements. This bit is cleared on completion.

This trigger bit is ignored in SHIP and LOW POWER Modes and can only trigger sequences in IDLE or SCAN mode.

5.2.1.4 0x01.4 - Recalibrate in LOW POWER Mode

Setting the Recalibrate in LOW POWER mode bit of the Operation register to 1 starts a low voltage offset recalibration for every measurement pass while in LOW POWER mode.

5.2.1.5 0x01.3 - Recalibrate Scan

Setting the Recalibrate Scan bit of the Operation register to 1 initiates a low voltage offset recalibration before performing another System Scan. This bit has significance only in SCAN mode and must be set before starting continuous Scan.

5.2.1.6 0x01.2 - Busy

A value of 1 for the Busy bit indicates that RAA489206 is busy either performing measurements or internal housekeeping. The Busy bit is read only and has a masking bit that connects the Busy bit status (inverted) to the $\overline{\text{ALRT}}$ pin. A Busy bit of 1 sets $\overline{\text{ALRT}}$ low. See 0x85 - Other Fault Mask for more information about the masking bit.
Note: Do not read measurement result registers when the RAA489206 is busy making measurements to avoid obtaining stale or mixed results. The RAA489206 saves each measurement result as it is obtained, reading data registers while Busy can produce a mix of previous and present scan results.

5.2.1.7 0x01.1 - Scan Select

The Scan Select bit chooses the type of System Scan that is performed when a System Trigger is initiated and the device is in SCAN mode.

If continuous System Scan (Default of 0) is chosen, the device periodically measures system parameters as described in System Scan Sequence. This selection reports a fault when the failure has exceeded the parameters fault delay setting. All fault counters are cleared at the beginning of a continuous scan, and no trace is left from previous System Scans. If a fault is detected, the power FETs turn off only if the fault output is connected to the FET driver (see 0x24 - Power FET Operation). A fault forces continuous scan to abort regardless of the connect bit settings and the MCU is expected to react.

If one instance of the System Scan is chosen (setting of 1), the device measures system parameters as described in System Scan Sequence. This System Scan also performs an open-wire check if 0x24.6 - OW EN is set to 1. One cycle of cell balancing is executed if appropriate per settings. Measurements are made if the function(s) are enabled. Any faults are reported after the single System Scan completes.

If changes to continuous scan are necessary, there are two options. The recommended method is to write the changes to the control register during 0x2E.2:0 - Scan Delay. The changes take effect before the start of the next scan. The second option is to set Scan Select bit to 1 and wait for the Busy bit to clear, indicating the Scan has completed. Make the necessary changes and set Scan Select bit to 0 and the System Trigger bit (0x01.0) to 1 to restart continuous Scan.

The second option is discouraged since fault counters are not used when Scan Select is set to 1, which can lead to a false fault following the transition from continuous scan. If this option is used, any fault should be verified by reading the related measurement data register.

5.2.1.8 0x01.0 - System Trigger

For this bit, a transition from 0 to 1 in SCAN mode initiates a System Scan (Figure 104). The type of System Scan is determined by the Scan Select bit setting. When the System Trigger bit has been received, the Busy bit (see 0x01.2 - Busy) transitions from a 0 to a 1, and the System Trigger bit returns to 0. The Busy bit remains high until the Scan Delay timer has started (0x2E.2:0 - Scan Delay), and returns to 0. If the System Trigger bit is set during an active scan, it is ignored and remains set until manually cleared.

If the Scan Select bit is set for continuous scan and there is an active fault, a System Scan is not initiated. The System Trigger bit does not automatically transition to a low. The fault must be cleared and the trigger bit set to a low before System Trigger is operational again. See Trigger Bits for detailed information.

The System Trigger bit is ignored when the System mode bits are SHIP, LOW POWER, or IDLE. It is executed only when the System mode bits are set to SCAN mode.

5.3 V_{CELL} and I_{PACK} Measurement

A level shifter/multiplexer and 16-bit ADC within the RAA489206 enable measurement of BMS parameters (Figure 78). The results of these measurements are compared to user-selected detection thresholds.

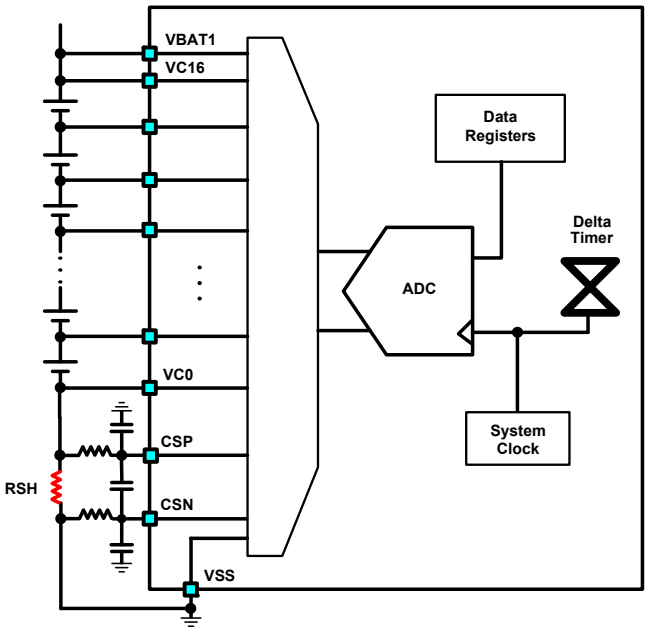


Figure 78. Voltage Measurement Block Diagram

An analog comparator checks for short-circuit conditions. Digital comparators are used for overcurrent and undercurrent, and overvoltage and undervoltage detection. For cell voltages, the detection thresholds are set by you to prevent overcharge or discharge of individual cells based on chemistry and/or other considerations.

The RAA489206 measures the pack current sense resistor (RSH) voltage before cell voltage measurements. A delta timer tracks elapsed time between current sense measurements.

5.3.1 0x02 - V_{CELL} Operation

The V_{CELL} Operation register controls data acquisition and part of the OV/UV fault behavior for V_{CELL} measurements. This register also contains the bit that clears latched fault and status bits.

Table 4. 0x02 V_{CELL} Operation Register

Bits	D[7]	D[6]	D[5]	D[4:2]	D[1]	D[0]
Bit Name	V_{CELL}EN	DCHRWOV	CHRWUV	V_{CELL} Averages	Clear Faults/Status	V_{CELL}Trigger
Default	1	0	0	0 00	0	0

5.3.1.1 0x02.7 - V_{CELL} EN

Set the V_{CELL} Enable bit to 1 (default) to enable V_{CELL} measurements within System Scans. The cells to be included in a System Scan are determined by the setting of registers 0x04 - 0x05 - Cell Select. Set this bit to 0 to disable V_{CELL} measurement during System Scans.

This bit does not prevent cell voltage measurements during Open Wire test or when started with the VCell Trigger bit 0x02.0.

5.3.1.2 0x02.6 - DCHRWOV

Set the Discharge While Overvoltage bit to 1 to disable V_{CELL} overvoltage detection during continuous System Scans while discharging. This setting allows the power FETs to remain on and discharging to occur if one or more cells are above the OV threshold set in register 0x06 - 0x07 - V_{CELL} OV Threshold and V_{CELL} UV Threshold. Set this bit to 0 (default) to allow an OV to disable DFET and/or CFET (also dependent on 0x0E.3 - CPWR and 0x24.4 - CELL CON) and/or stop System Scan.

5.3.1.3 0x02.5 - CHRWUV

Set the Charge While Undervoltage bit to 1 to disable V_{CELL} undervoltage detection while charging. This setting allows CFET to remain on and charging to occur if one or more cells are below the UV threshold set in register 0x06 - 0x07 - V_{CELL} OV Threshold and V_{CELL} UV Threshold. Set this bit to 0 (default) to allow a UV to disable CFET and/or DFET (also dependent on CPWR and CELLCON) and/or stop System Scan.

5.3.1.4 0x02.4:2 - V_{CELL} Averages

The V_{CELL} Averages bits set the number of samples averaged (per cell) before writing the measurement results to their respective registers. Table 5 lists the options for these bits.

The conversion time for each V_{CELL} measurement is estimated using Equation 1:

(EQ. 1) $$VCELL_{CT} = (3 + (SamplesToAverage)) \cdot ADC_{CT2}$$

ADC_{CT2} is the base conversion time of the ADC.

Table 5. V_{CELL} Average Bits

V_{CELL} Averages: D[4:2]			Samples to Average
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

5.3.1.5 0x02.1 - Clear Faults and Status

Write a 1 to the Clear Faults and Status bit to clear the faults and status. All bits in registers 0x63-0x69, except for 0x67.5 - CH PRESI, along with all counters are cleared (set to 0). Other register settings are maintained with this command. On completion the bit is set to 0, this command takes ~100µs to complete.

The Fault and Status bits cannot be cleared while the condition that sets them is present.

The CH PRESI (charger present) bit is a straight connection to the $\overline{\text{WAKEUP}}$ pin inverted and can only be set or cleared by the status of this pin.

5.3.1.6 0x02.0 - V_{CELL} Trigger

For this bit, a transition from 0 to 1 initiates cell voltage measurements if the Busy bit is 0 and no other trigger is active, regardless of the setting of bit 0x02.7 - V_{CELL} EN. The measured cells are determined by registers 0x04 - 0x05 - Cell Select. When the command bit has been received, the Busy bit (0x01.2 - Busy) transitions from a 0 to a 1 and the trigger bit clears. The Busy bit remains set until the measurement scan is completed, and returns to a 0.

This trigger bit is ignored in SHIP and LOW POWER Modes and can trigger sequences in IDLE or SCAN mode only. This trigger should be used in IDLE mode because Renesas recommends to reserve SCAN mode for System Scans only.

5.3.2 0x03 - I_{PACK} Operation

I_{PACK} Operation is a 1-byte register that controls the system behavior of related to I_{PACK} measurements and how often the open-wire test is executed.

Table 6. 0x03 I_{PACK} Operation Register

Bits	D[7]	D[6:5]	D[4:2]	D[1]	D[0]
Bit Name	I_{PACK}EN	OW Update	I_{PACK}AVE	I_{DIR}Delay	I_{PACK}Trigger
Default	1	00	0 00	0	0

5.3.2.1 0x03.7- I_{PACK} EN

Set this bit to 1 (default) to enable I_{PACK} measurement during System Scans. Set to 0 to disable I_{PACK} measurement during System Scans. This bit does not prevent I_{PACK} measurement during open-wire detection or when started by the I_{PACK} Trigger bit.

5.3.2.2 0x03.6:5 - OW Update

The Open-Wire Update bits of the I_{PACK} Operation register control how often the open-wire test is executed as part of continuous System Scans. The frequency of the open-wire test is defined in terms of System Scans in Table 7.

Open-Wire operation is detailed in Open-Wire Function and Aux Pins Open-Wire Test. The Aux Pins open-wire test is not controlled by the 0x03.6:5 OW Update bits or 0x24.6 - OW EN and is not triggered by 0x24.5 - OW Trigger.

Table 7. OW Update Bits

D[6:5]		How Often the Open-Wire Test is Executed?
0	0	256 (Update on scan 1, 257, 513, 769...)
0	1	512 (Update on scan 1, 513, 1025, 1567...)
1	0	1024 (Update on scan 1, 1025, 2049, 3071...)
1	1	2048 (Update on scan 1, 2049, 4097, 6145...)

5.3.2.3 0x03.4:2 - I_{PACK} Averages

The I_{PACK} Averages bits determine the number of samples averaged before writing the measurement result to its register. Table 8 lists the options for these bits.

Table 8. I_{PACK} Averages Bits

I_{PACK} Averages: D[4:2]			Samples to Average
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

The conversion time for an I_{PACK} measurement is estimated using Equation 2:

(EQ. 2) $$IPACK_{CT} = (3 + SamplesToAverage) \cdot ADC_{CT2}$$

ADC_{CT2} is the base conversion time of the ADC.

5.3.2.4 0x03.1 - I_{DIR} Delay

The Current Direction delay bit of the I_{PACK} Operation register sets the number of consecutive current measurement readings in one direction required before setting the CHRGI or DCHRGI (0x67 - Status) bits in SCAN mode. The default setting of 0 requires only one reading. Set this bit to 1 to require three consecutive readings in SCAN mode during continuous scans. This bit has no effect on single scans or in other operating modes.

The 0x67.6 - CHRGI and 0x67.7 - DCHRGI bits are evaluated at the end of each I_{PACK} measurement.

For an I_{DIR} Delay of 0, CHRGI is set to 1 immediately if the I_{PACK} measurement result is >208µV or it is reset to 0 if the result is <208µV. DCHRGI is set to 1 immediately if the I_{PACK} measurement result is <-219µV or it is reset to 0 if the result >-219µV (typical voltage thresholds).

With I_{DIR} Delay set to 1, CHRGI is set to 1 after three consecutive I_{PACK} measurement results >208µV or it is reset to 0 immediately if a result <208µV. DCHRGI is set to 1 after three consecutive I_{PACK} measurement results <-219µV or it is reset to 0 immediately if a result >-219µV (typical voltage thresholds).

5.3.2.5 0x03.0 - I_{PACK} Trigger

For this bit, a transition from 0 to 1 instructs the device to start an I_{PACK} and Delta Timer measurement. When received, the Busy bit transitions from a 0 to a 1 and the trigger bit clears. The Busy bit remains set until the action is completed and next returns to a 0.

The I_{PACK} Trigger bit initiates an I_{PACK} measurement regardless of the setting of the I_{PACK} Enable bit.

This trigger bit is ignored in SHIP and LOW POWER Modes and can trigger sequences in IDLE or SCAN mode only. Use the trigger bit in IDLE mode only as Renesas recommends that SCAN mode is reserved for System Scans.

5.3.3 0x04 - 0x05 - Cell Select

The Cell Select registers indicate to the RAA489206 state machine which cells exist in the BMS. This setting determines the cells to include during V_{CELL} scans, Open-Wire test, Cell Balancing, and System Scans. A 1 includes the cell and a 0 bypasses the cell in all functions. Unused cell locations MUST be disabled (set to 0) before starting System Scans or triggering measurements, Open-Wire, or Cell Balancing functions.

Table 9. 0x04 - 0x05 Cell Select Registers

Bit Name	Address - Bits	Default
Cell Number 16 (MSB) to 9 (LSB)	0x04 - D[7:0]	1111 1111
Cell Number 8 (MSB) to 1 (LSB)	0x05 - D[7:0]	1111 1111

5.3.4 0x30 - 0x4F - V_{CELL} Voltage (R)

Registers 0x30 through 0x4F report V_{CELL} measurements. The V_{CELL} output voltage is stored across two adjacent bytes as listed in Table 10.

Table 10. V_{CELL} Measurement Registers

Bit Name	Address - Bits	Default	$VCELL_{Step}$
Cell Number 15 (MSB) to 8 (LSB)	0x30, 32, 34...4E - D[7:0]	0000 0000	73.55µV
Cell Number 7 (MSB) to 0 (LSB)	0x31, 33, 35...4F- D[7:0]	0000 0000	

Addresses 0x30 and 0x31 contain the voltage reading for Cell 1. Locations 0x4E and 0x4F correspond to Cell 16's voltage reading.

(EQ. 3) $$VCell = (RegVal) \cdot VCELL_{Step} + 0.5 \cdot VCELL_{Step}$$

Use Equation 3 to calculate the cell voltage by multiplying the 16-bit register value by the step size $VCELL_{Step}$ and add the 1/2 LSB offset. The register records results from 36.77µV to 4.82V.

5.3.5 0x50 - 0x51 - V_{CELL} Max Delta Voltage (R)

The V_{CELL} Maximum Delta registers store the difference between the maximum V_{CELL} voltage and the minimum V_{CELL} voltage (registers 0x30-0x4F). It is evaluated immediately after a V_{CELL} scan completes. Table 11 shows the format of these registers.

Table 11. 0x50-51 V_{CELL} Delta Register

Address - Bits	Bit Name	Default	$VCELL_{Step}$
0x50 - D[7:0]	15 (MSB) to 8 (LSB)	0000 0000	73.55µV
0x51 - D[7:0]	7 (MSB) to 0 (LSB)	0000 0000	

(EQ. 4) $$VCellMaxDelta = (RegVal) \cdot VCELL_{Step}$$

Calculate the Maximum Delta Voltage by multiplying the 16-bit register value by the step size $VCELL_{Step}$ as shown in Equation 4. The register records results from 0V to 4.82V.

5.3.6 0x52 - 0x53 - I_{PACK} Voltage (R)

The I_{PACK} registers hold the 16-bit 2's complement measurement result representing the I_{PACK} sense resistor (R_{SHUNT}) voltage. Calculate the voltage as outlined below; next, divide the result by the shunt resistance R_{SHUNT} (see CSP and CSN Pins (24, 25)) to calculate the current.

The MSB of the 16-bit register reading (0x52.7) is the sign bit. If it is 0 then:

- $V(I_{PACK}) = (Code_{16})$ x LSB + ½LSB. Otherwise,
- $V(I_{PACK}) = (Code_{16} - 65536)$ x LSB + ½LSB

The LSB value is 10.51µV. Examples:

- $Code_{16}$ 0x0000 = ½LSB = 5.25µV
- $Code_{16}$ 0x7FFF = $(2^{15} - 1)$ x LSB + ½LSB = +344.28mV
- $Code_{16}$ 0x8000 = $(2^{15} - 65536)$ x LSB + ½LSB = -344.28mV

Note: Every time current is measured, the Delta Timer value is written to 0x54 - 0x57 - I_{PACK} Timer (R).

5.3.7 0x54 - 0x57 - I_{PACK} Timer (R)

The I_{PACK} Timer is 32 bits with a nominal step size of 15ms. It functions as a time stamp for I_{PACK} current measurements. When a pack current measurement is made, the value of the I_{PACK} Timer is pushed to these registers. The timer runs in LOW POWER, IDLE, and SCAN Modes and is designed to count to two years without rolling over.

Multiply the step size $\Delta Timer_{Step}$ by the 32-bit register value to calculate the elapsed time. The register records results from 0ms to 2.043 years. Multiplying the elapsed time between two measured currents by the current results in an electric charge value in Coulombs.

The timer is reset and begins counting immediately on POR, see RESET Pin (38), 0x01.7 - Soft Reset, and 0x01.6 - Reset to IDLE.

5.4 V_{CELL} Fault Detectors

The V_{CELL} Fault Detectors consist of digital OV/UV comparators and fault delay timers. The digital comparators and delay timers are responsible for detecting OV/UV events while charging and discharging in SCAN mode to provide an automatic fault response. Fault response is up to the MCU in IDLE mode. Figure 79 is a block diagram of the V_{CELL} Fault Detection function.

5.4.1 0x06 - 0x07 - V_{CELL} OV Threshold and V_{CELL} UV Threshold

Each V_{CELL} measurement is compared to overvoltage and undervoltage limits. During discharge, undervoltage threshold detectors alert the system to prevent discharging to a nonchargeable state. During charge, the overvoltage threshold detectors alert the system to discontinue charging at the selected voltage. These threshold detectors only operate under charge (0x67.6 - CHRGI) or discharge (0x67.7 - DCHRGI) conditions. The V_{CELL} Fault Delay counters are bypassed if the part is not running in continuous scan.

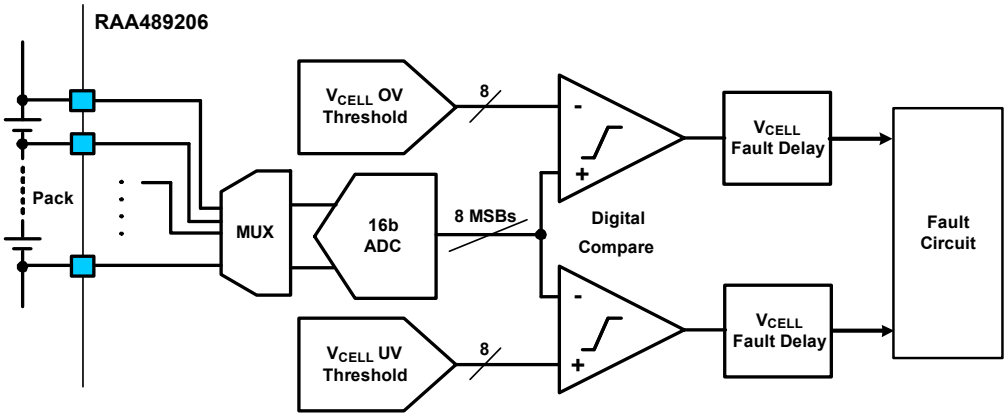


Figure 79. V_{CELL} OV/UV Detectors

The threshold detectors are digital comparators that require an ADC V_{CELL} conversion to compare. These two comparators (OV/UV) are fault detectors. If the FET control bit 0x24.4 - CELL CON is set, a OV or UV event can shut off the power FET(s) depending on the bit settings of 0x0E.3 - CPWR, 0x02.6 - DCHRWOV, and 0x02.5 - CHRWUV. The overvoltage and undervoltage registers are shown in Table 12.

Table 12. 0x06 OV and 0x07 UV V_{CELL} Threshold Registers

Address - Bits	Bit Name	Default	V_{thStep}	Offset
0x06 - D[7:0]	OV Threshold	1111 1111	18.83mV	18.79mV
0x07 - D[7:0]	UV Threshold	0000 0000		36.77µV

OV_{thStep} and UV_{thStep} are the same value for both thresholds, the Offsets are different. Multiply the register value by the step size, and add the fixed offset to calculate the threshold using Equation 5. The OV threshold register supports settings from 18.79mV to 4.82V while the UV threshold register supports settings from 36.77µV to 4.801V.

(EQ. 5) $$VThreshold = (RegVal) \cdot V_{thStep} + Offset$$

A V_{CELL} OV threshold violation sets the fault 0x63.0 - OVF when any cell is greater than the threshold and the device is charging. A UV threshold violation sets the fault 0x63.1 - UVF if any cell is less than or equal to the threshold and the device is discharging. These faults are gated by fault counters, see 0x09.3:0 - V_{CELL} Fault Delay.

5.4.2 0x08 - V_{CELL} Max Delta Threshold

The V_{CELL} Max Delta register sets the threshold for a digital compare with the V_{CELL} Max Delta Voltage (0x50 - 0x51). The detection is used to maintain cell voltage readings within a predetermined voltage range. Table 13 shows the format of this register.

Table 13. 0x08 V_{CELL} Maximum Delta Threshold Register

Bit Name	Bits	Default	$DVCELL_{Step}$	Offset
DVCMAX - V_{CELL} Max Delta Threshold	D[7:0]	1111 1111	18.83mV	18.79mV

Multiply the register value by the step size $DVCELL_{Step}$, and add the fixed offset to calculate the threshold using Equation 6. The register supports settings from 18.79mV to 4.82V.

(EQ. 6) $$VThreshold = (RegVal) \cdot DVCELL_{Step} + Offset$$

A V_{CELL} Max Delta threshold violation sets the fault 0x66.3 - DVCF when any cell voltage delta is greater than the threshold. This fault is gated by a fault counter, see 0x09.6 - Delta V_{CELL} Fault Delay.

5.4.3 0x09 - Fault Delay

When a fault is detected, the RAA489206 reacts following a set delay. The delay to report a fault is a function of the ADC conversion time, the functions included in scans, the type of scan, and the Fault Delay register settings (if in continuous scan). The fault delays are user-programmable scan counters that are active only during continuous scans. Table 14 shows the format of this register.

Table 14. 0x09 Fault Delay Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3:0]
Bit Name	AUX Pull-up	DV_{CELL} Fault Delay	Other Fault Delay	ETAUX Fault Delay	V_{CELL} Fault Delay
Default	0	0	0	0	0000

5.4.3.1 0x09.7 - AUX/xTn Pull-Up

When the Auxiliary input Pull-Up bit is 1, an internal test resistor (R_{ETAUX}) is connected between AUX0/xT0 and VCC and another between AUX1/xT1 and VCC.

The resistors should only be connected to conduct an open-wire test of the AUX0/xT0 and AUX1/xT1 pins and disconnected during normal operation by setting it back to 0 (default). See Aux Pins Open-Wire Test for details about the operation of this bit.

5.4.3.2 0x09.6 - Delta V_{CELL} Fault Delay

The DV_{CELL} fault detector has a scan delay counter gating the output of the DV_{CELL}Voltage threshold comparator when the device is in continuous SCAN mode. These counters are bypassed during single triggered scans. The DV_{CELL} Fault Delay is set to either a single failure (default of 0) or three consecutive scan failures (if set to 1) required. The selected count must be met during continuous scan before a fault is reported.

5.4.3.3 0x09.5 - Other Fault Delay

When the RAA489206 is in continuous SCAN mode, the Other Fault Delay bit controls individual scan delay counters that gate the output of the following fault comparators; 0x63.7 - VCCF, 0x67.0 - VTMPF, 0x67.2 - IREG1, 0x67.1 - IREG2, 0x65.7 - VBOVF, 0x65.6 - VBUVF, 0x63.5 - IOTF, and 0x66.6 - IOTW. The scan delay count can be set to either a single failure (default setting of 0) or three consecutive scan failures (if set to 1) before setting the fault bit. The selected count of consecutive errors must be met during continuous scan before a fault is reported. These counters are bypassed during single triggered scans.

5.4.3.4 0x09.4 - ETAUX Fault Delay

The ETAUX fault detector has a scan delay counter gating the output of the ETAUX Voltage threshold comparators when the device is in continuous SCAN mode, these counters are bypassed during single triggered scans. The ETAUX Fault Delay is set to either a single (default of 0) or three consecutive scan failures (if set to 1) required. The selected count must be met during continuous scan before a fault is reported.

5.4.3.5 0x09.3:0 - V_{CELL} Fault Delay

The V_{CELL} Fault Delay bits set the required count of consecutive V_{CELL} scans with a Cell OV or UV failure before a fault is reported (see 0x06 - 0x07 - V_{CELL} OV Threshold and V_{CELL} UV Threshold). This delay counter is only functional when the device is running continuous System Scans and a charge (0x67.6 - CHRGI) or discharge current (0x67.7 - DCHRGI) is detected. These counters are bypassed during single triggered scans. If the device is in continuous SCAN mode and a cell voltage is outside the limits during consecutive measurements that exceeds the V_{CELL} Fault Delay setting, a fault is reported. The V_{CELL} Fault Delay count threshold is the decimal value of these bits plus 1. The range is between 1 scan (default setting of 0000) and 16 scans (setting of 1111).

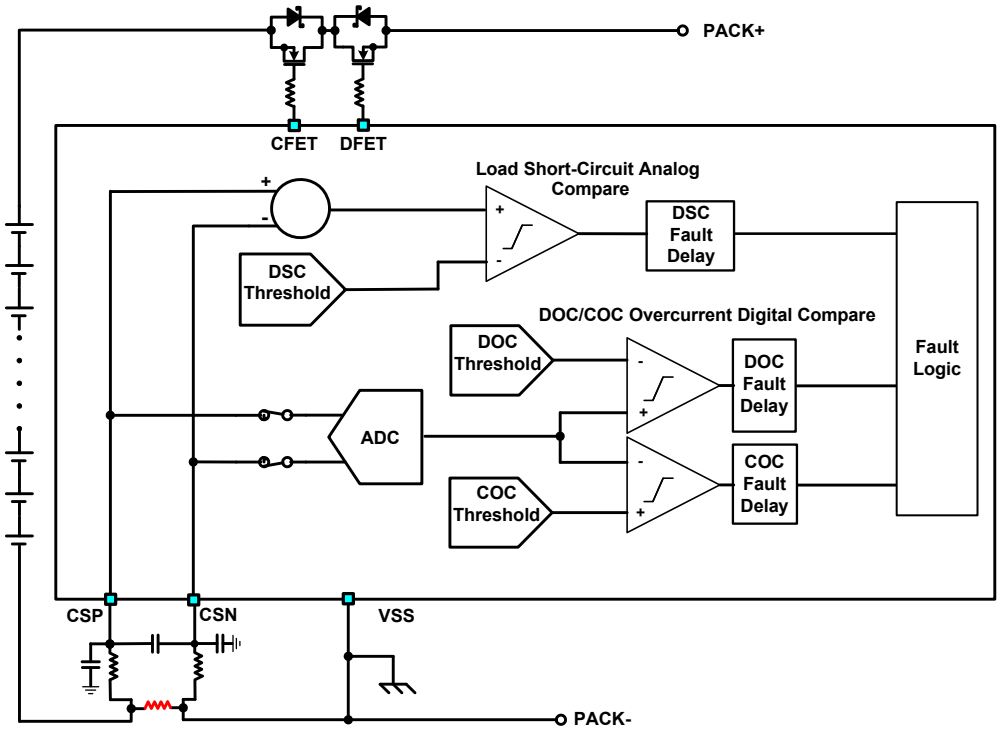


Figure 80. Current Sense Block Diagram

5.5 I_{PACK} Fault Detectors

The I_{PACK} Fault Detectors consist of a short-circuit analog comparator and two digital overcurrent comparators. The analog comparator disconnects the battery pack from the load when a short-circuit is detected. The comparator is operational in all modes except in SHIP. The digital comparators are responsible for detecting overcurrent events while charging and discharging. Figure 80 is a block diagram of the I_{PACK} Fault Detection function.

5.5.1 0x0A - DSC Threshold

The Discharge Short-Circuit Threshold register sets the short-circuit threshold of the analog comparator. Table 15 shows the format of the Discharge Short-Circuit Threshold register. Short-circuit detection is disabled by setting the register to 0x00. **Note:** This is for test purposes and is not recommended for normal operation.

Table 15. 0x0A DSC Threshold Register

Bit Name	Bits	Default	$VDSC_{Step}$	Offset	Min Threshold (0x0A.[3:0] = 0001)
RSV	D[7:4]	0000			
DSC Discharge Short-Circuit Threshold	D[3:0]	1111	-20.083mV	-20.083mV	-40.167mV

Multiply the register value by the step size $VDSC_{Step}$ and subtract the fixed offset to calculate the threshold for non-zero settings using Equation 7. The register supports settings from -40.167mV to -321.33mV (typical). This register represents a negative value without a sign bit. If the voltage across the current sense resistor (see CSP and CSN Pins (24, 25)) is more negative than this threshold for more than 0x0C - DSC Delay, fault bit 0x63.2 - DSCF is set. See Short-Circuit Detection and Recovery for a detailed description of the relationship between the DSC Threshold, DSC Delay and 0x0E.4 - ELR.

(EQ. 7) $$VThreshold = ((RegVal) \cdot VDSC_{Step}) + Offset$$

5.5.2 0x0B - DOC Threshold

The Discharge Overcurrent Threshold register sets the overcurrent threshold of a digital comparator. Table 16 shows the format of this register.

Table 16. 0x0B DOC Threshold Register

Bit Name	Bits	Default	$VDOC_{Step}$	Offset
DOC - Discharge Overcurrent Threshold	D[7:0]	1111 1111	-1.345mV	-5.25µV

The comparator for overcurrent detection relies on ADC conversions in addition to a number of System Scans. If the measurement is continuously above the threshold after the selected number of scans occurs (see 0x0D - OC Delay), a fault is asserted.

(EQ. 8) $$VThreshold = ((RegVal) \cdot VDOC_{Step}) + Offset$$

Multiply the register value by the step size $VDOC_{Step}$ and subtract the fixed offset to calculate the threshold Equation 8. The register supports settings from -5.25µV to -342.95mV. This register represents a negative value without a sign bit.

If the voltage across the current sense resistor (see CSP and CSN Pins (24, 25)) is less than or equal to this threshold for more than 0x0D.7:4 - DOCD Scans during discharge, the fault bit 0x63.3 - DOCF is set and continuous scan is halted. If bit 0x0E.7 - CFD is set, DFET is also shut off.

5.5.3 0x0C - DSC Delay

The Discharge Short-Circuit Delay register sets the delay time for short-circuit current detection. If the short-circuit remains (as determined by the 0x0A DSC threshold) after the delay has timed out, it shuts off the DFET and sets the fault bit 0x63.2 - DSCF. Table 17 outlines the Discharge Short-Circuit Delay register.

Table 17. 0x0C Discharge Short-Circuit Delay Register

Bit Name	Bits	Default	DSC_{Step}
RSV	D[7]	0	
DSC - Discharge Short-Circuit Delay	D[6:0]	000 0000	31.25µs

There is a fixed delay of 100-125µs between DSC comparator detection and $\overline{ALRT}$ assertion if the DSCF Mask bit is clear (0x83 - Priority Fault Mask), otherwise $\overline{ALRT}$ is not asserted. With DSC Delay set to 0x00, the comparator detection is decoupled from the delay circuitry and acts within a few µs to shut off the power FETs. This setting is recommended for applications capable of producing component damaging short-circuit currents.

For non-zero delay settings, the comparator output detection and $\overline{ALRT}$ assertion is delayed by this fixed delay plus the selected delay. The device acts to shut off the power FETs ~125µs after $\overline{ALRT}$ asserts. The total delay is composed of these two fixed delays of ~250µs plus the selected delay.

Multiply the 7-bit register value by the step size DSC_{Step} (31.25µs) then add the fixed delay to calculate the total delay. The register supports additional delay values from 0µs to 3968.75µs. Set this register to 0x00 for no DSC Delay.

5.5.3.1 Short-Circuit Detection and Recovery

When a discharge current exceeds the DSC Threshold for longer than the DSC Delay setting, the bit 0x63.2 - DSCF is set to 1 and the DFET is shut off. The DSCF bit is cleared by either the load detection circuitry or by writing a 0 to the bit. **Note:** Do not clear the DSCF bit until the load is removed and a pack current measurement confirms the current was shut off.

If the load detection (0x0E.6:5 - ELD) and recovery functions (0x0E.4 - ELR) are enabled, the load recovery circuitry checks if the load (or short) has been removed (Figure 81). This happens after a nominal delay of t_{LDEN} (~256ms) following the shutoff of the DFET. An on-chip pull-up resistor determined by the ELD setting (0x0E.6:5 - ELD) is connected between the LDMON and V_{BAT2} pins. After LD Delay (0x1B.3:2 - LD Delay) the LDMON voltage is compared to the V_{LDThr} threshold (1.2V nominal). If the LDMON voltage is less than the threshold, the load is considered present and bit 0x67.4 - LD PRESI is set. The load recovery circuitry is looking for a no load present before clearing the DSCF bit. When the voltage at the LDMON pin is above V_{LDThr}, and the DSC comparator no longer indicates the current is above the 0x0A - DSC Threshold setting, both the DSCF and LDPRESI bits are cleared and DFET is allowed to turn on. **Note:** The unsigned DSC Threshold represents a negative voltage because the discharge current generates a negative voltage across the current sense resistor.

The DFET output is not automatically turned back on when DSCF clears; it should be turned on by the microcontroller only following confirmation that the short-circuit is no longer present. The DSCF bit cannot be cleared by you while the Short-Circuit Recovery Sequence is in progress.

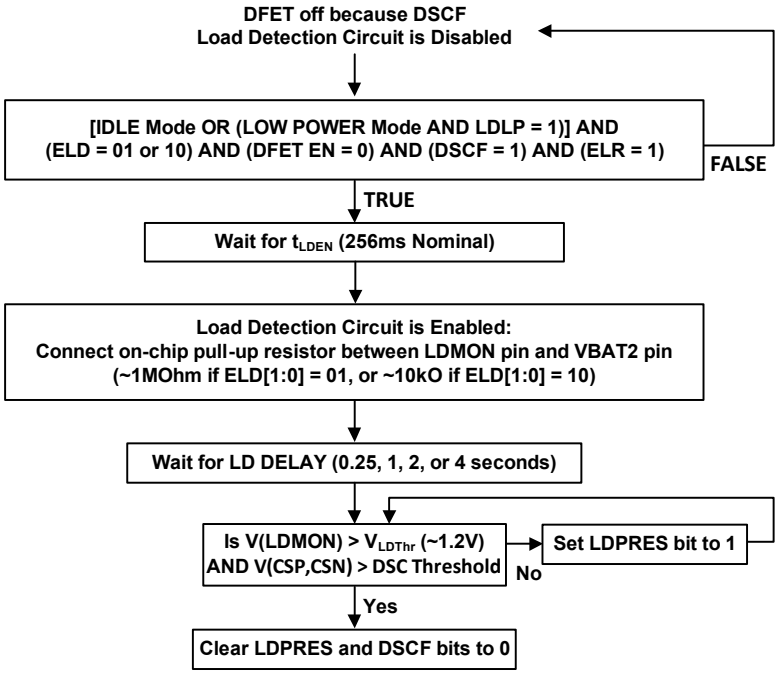


Figure 81. Simplified Short-Circuit Recovery Sequence

5.5.4 0x0D - OC Delay

The Overcurrent Delay register defines the delay in terms of System Scans for charge and discharge overcurrent detection. The delay function only operates when the device is in SCAN mode during a continuous scan, the delay is ignored in single triggered scans. Table 18 details the Overcurrent Delay register.

Table 18. 0x0D Overcurrent Delay Register

Bit Name	Bits	Default
DOCD - Discharge Overcurrent Delay	D[7:4]	0000
COCD - Charge Overcurrent Delay	D[3:0]	0000

5.5.4.1 0x0D.7:4 - DOCD

The Discharge Overcurrent Delay bits select the number of consecutive System Scans with a DOC threshold violation (0x0B - DOC Threshold) that is required before it is reported to the DFET control circuitry and fault bit 0x63.3 - DOCF is set. The number of System Scans can be programmed to between 1 and 15 scans. If this register is set to 0000, the fault is declared as soon as detected, a setting of 0001 or higher delays the fault declaration until the end of the selected number of scans.

5.5.4.2 0x0D.3:0 - COCD

The Charge Overcurrent Delay bits select the number of consecutive System Scans with a COC threshold violation (0x0F - COC Threshold) that is required before it is reported to the CFET control circuitry and fault bit 0x63.4 - COCF is set. The number of System Scans can be programmed to between 1 and 15 scans. If this register is set to 0000, the fault is declared as soon as detected, a setting of 0001 or higher delays the fault declaration until the end of the selected number of scans.

5.5.5 0x0E - Load/Charge Operations

This register is responsible for controlling various operations relevant to load and fault detection during charging and discharging and their relationship to the power FET drivers. Allocation of the Load/Charge Operations register is detailed in Table 19.

Table 19. 0x0E Load/Charge Operations Register

Bits	D[7]	D[6:5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	CFD	ELD	ELR	CPWR	FCDC	LDLP	RSV
Default	1	01	1	0	1	0	0

5.5.5.1 0x0E.7 - CFD

The Connect for Discharge fault bit of the Load/Charge Operations register connects a discharge overcurrent detection (0x0B - DOC Threshold) to the FET Driver when set to 1 (default). This allows the FET Driver to automatically turn off the power FET(s) if a DOC fault occurs during discharge (0x67.7 - DCHRGI is 1).

Setting bit CFD to 0 prevents a DOCF (0x63.3 - DOCF) from shutting off the power FET(s), transferring responsibility to the MCU.

A DOCF stops the continuous scan regardless of the setting of CFD.

Bit 0x0E.3 - CPWR determines if DFET or both DFET and CFET are turned off and System Scan is stopped.

5.5.5.2 0x0E.6:5 - ELD

The Enable Load Detection bits configure the load detection circuitry. Table 20 shows the configuration options of the ELD bits. ELR is ignored and automatic load recovery is not performed if the ELD bits are set to 00.

Load detection is described further in LDMON Pin (49) and Load Detection.

Table 20. ELD Bits

D[6:5]		ELD
0	0	Do Not Enable Load Detection
0	1	Load Detection Enabled with 1MΩ Pull Up to V_{BAT2}
1	0	Load Detection Enabled with 10kΩ Pull Up to V_{BAT2}
1	1	RSV

Leakage current when a load is not connected to a battery pack is often dependent on the protection circuitry on the load side of DFET. The amount of leakage usually increases with pack voltage and current rating. Too much

leakage can cause a false load detection. The maximum pull-down leakage current that does not trigger a false load detection is defined by Equation 9. The maximum leakage current before load detect is dependent on pack voltage, V_{LDThr} and R_{LDPU} resistance.

(EQ. 9) $$(LeakageCurrent(Max)) < (VBAT - VLDThr(Max))/(RLDPU(Max))$$

Note: About Off-Chip Protection Resistor at the LDMON pin and DFET:

When the DFET is off and the load pull-up resistor is 10kΩ, it is possible to turn on DFET if the value of R_{LDISO} is too high. Figure 91 illustrates DFET interacts with the load monitor pin. When the DFET is off, a switch connects R_{DFOFF} between the two pins. The LDMON pull-up resistor, R_{LDPU}, is also connected. If the value of R_{LDISO} is high enough, a large enough voltage between the gate and source of the DFET when Pack+ is close to ground can cause the DFET to turn on. To prevent this from happening, size R_{LDISO} to keep the VGS of the FET low enough to remain off but as high as possible for maximum protection.

5.5.5.3 0x0E.4 - ELR

The Enable Load Recovery bit enables the load recovery function. If a short-circuit is detected, the load recovery circuitry tests for load removal after a fixed delay of t_{LDEN} plus a selectable delay of $t_{LDDELAY}$ (0x1B.3:2 - LD Delay) following the shut off of DFET (default setting of 1). If set to 0, no load recovery test is executed and the DFET remains off until the MCU resolves the issue.

If ELR is enabled when a DSCF occurs, and the load recovery function determines if the load was removed, the DSCF bit is automatically cleared. This function does not re-enable the DFET. See Short-Circuit Detection and Recovery for a detailed description of the relationship between the DSC Threshold, DSC Delay and ELR.

Note: If the ELD bits are set to 00 (Table 20), ELR is ignored and a load recovery is not performed.

5.5.5.4 0x0E.3 - CPWR

The Configure Power FET bit configures the RAA489206 for either a series (default setting of 0) or parallel (if set to 1) CFET and DFET configuration (Figure 82). This setting determines whether one or both CFET and DFET are shut off and if System Scan stops when certain indicators and/or Faults are set to 1. The CPWR bit has no effect on short-circuit events, or events not directly related to charge or discharge.

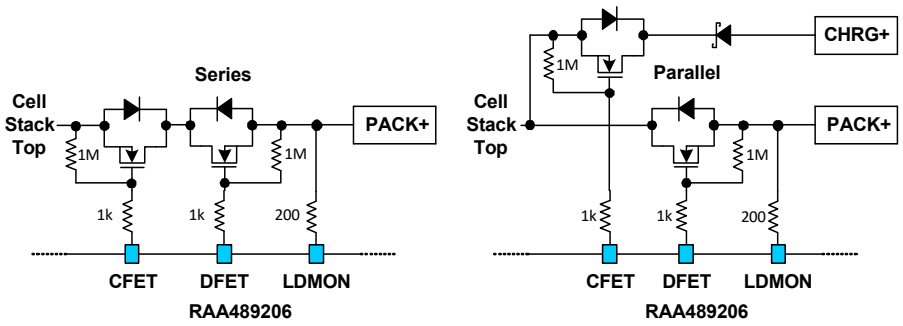


Figure 82. Power FET Configurations

See CFET and DFET Pins (50, 51) for complete details about the CPWR, fault, and control bits as they relate to FET control. See Scan Will Not Start for information about how the CPWR setting effects System Scan.

5.5.5.5 0x0E.2 - FCDC

The FET Charge Driver Connect bit of the Load/Charge Operations register connects the charge overcurrent (0x0F - COC Threshold) fault to the FET Driver when set to 1 (default). This allows the FET Driver to automatically turn off CFET when a COC fault (0x63.4 - COCF) occurs. When FCDC = 1, CPWR = 1 and COCF = 1, the CFET is turned off. When FCDC = 1, CPWR = 0, and COCF = 1, both CFET and DFET are turned off and System Scan stops.

Setting this bit to 0 prevents a COCF from shutting off CFET (and DFET if CPWR = 0), transferring responsibility to the MCU. A COCF causes continuous scan to halt regardless of the setting of FCDC.

5.5.5.6 0x0E.1 - LDLP

The Load Detect while in LOW POWER mode bit keeps the load detection circuit off when the RAA489206 is in LOW POWER mode with the default setting of 0. Setting the bit to 1 allows turning on load detection with bits 0x0E.6:5 - ELD while in LOW POWER mode. When LDLP is enabled a detection causes the RAA489206 to transition to IDLE mode.

This bit has no effect on other modes. See Load Detection for more details.

5.5.5.7 0x0E.0 - RSV

The Reserve bit should be ignored during a read command and should be set to 0 during a write command.

5.5.5.8 Load Detection

The Load Connection Detection state machine only operates when DFET is off. The LDMON circuit is disabled when DFET is turned on. The load detection circuit includes an analog comparator and a pull-up resistor to V_{BAT2}.

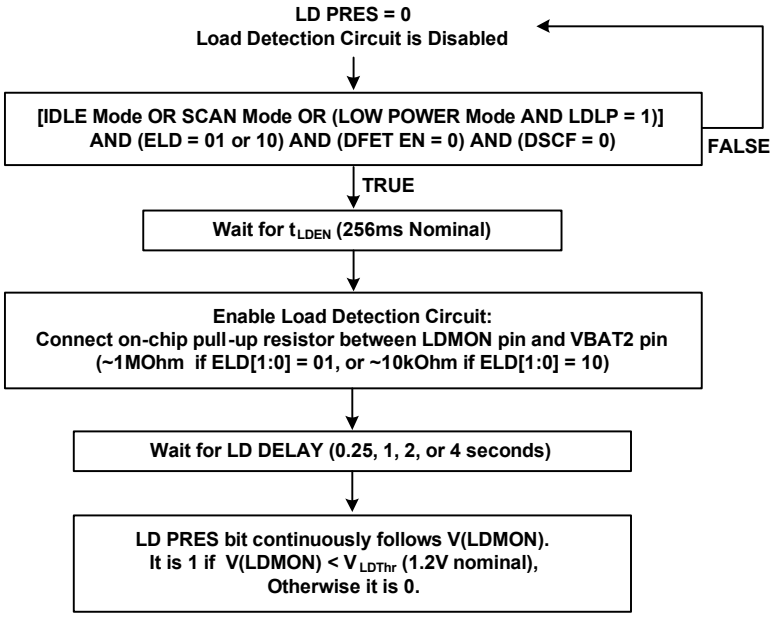


Figure 83. Simplified Load Connection Detection Sequence

When the DFET transitions to the off state, the LD PRESI bit is cleared (see 0x67.4 - LD PRESI). After a nominal delay of t_{LDEN} (~256ms) following DFET turn off an on-chip pull-up resistor determined by the ELD setting (0x0E.6:5) is connected between the LDMON and V_{BAT2} pins. After LD Delay (0x1B.3:2 - LD Delay) the LD PRESI bit continuously follows the LDMON voltage. It is 1 when the voltage is below V_{LDThr} (1.2V nominal) or 0 otherwise.

The load detection circuit operates in SCAN and IDLE modes if enabled by the ELD bits 0x0E.6:5, and in LOW POWER mode if also enabled by LDLP bit 0x0E.1.

5.5.6 0x0F - COC Threshold

The Charge Overcurrent Threshold register sets the overcurrent threshold of a digital comparator. Table 21 shows the format of this register. If the measurement is continuously above the threshold after the selected number of scans expires (see 0x0D - OC Delay), then a fault is asserted.

Table 21. 0x0F Charge Overcurrent Threshold Register

Bit Name	Bits	Default	$VCOC_{Step}$	Offset
COC - Charge Overcurrent Threshold	D[7:0]	1111 1111	1.345mV	5.25µV

The comparator for overcurrent detection relies on ADC conversions in addition to a number of System Scans set by 0x0D.3:0 - COCD. If the I_{Pack} voltage continuously measures greater than or equal to this threshold after the selected number of scans occurs, fault bit 0x63.4 - COCF is asserted and continuous scan is halted. If bit 0x0E.2 - FCDC is set, the CFET is automatically shut off. See Charge Overcurrent Detection and Table 18.

(EQ. 10) $$VThreshold = (RegVal) \cdot VCOC_{Step} + Offset$$

Multiply the register value by the step size $VCOC_{Step}$ add the fixed offset to calculate the threshold (Equation 10). The register supports settings from 5.25µV to 342.95mV.

5.5.6.1 Charge Overcurrent Detection

When the RAA489206 detects an overcurrent condition while charging for the number of consecutive System Scans set by COCD (0x0D.3:0 - COCD), fault bit 0x63.4 - COCF is set. If the COCF Mask bit is clear, the $\overline{ALRT}$ pin goes low. If the FET Charge Driver Connect bit (0x0E.2 - FCDC) is set, CFET is automatically turned off. If CPWR = 0 (0x0E.3 - CPWR), DFET also turns off and the chip transitions to IDLE mode.

The FET off state is the responsibility of the MCU when FCDC = 0. A COCF causes continuous scan to halt regardless of the setting of FCDC. Figure 84 is the flow diagram for charge overcurrent detection and response.

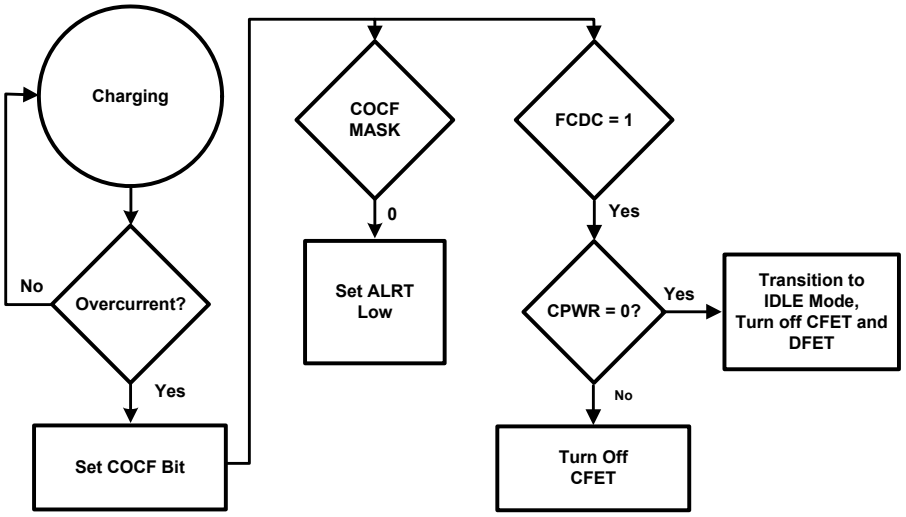


Figure 84. COC Detect Flow Diagram

5.6 ETAUX Port

Figure 85 shows the typical configuration of the External Temperature/Auxiliary (ETAUX) port with two external thermistors.

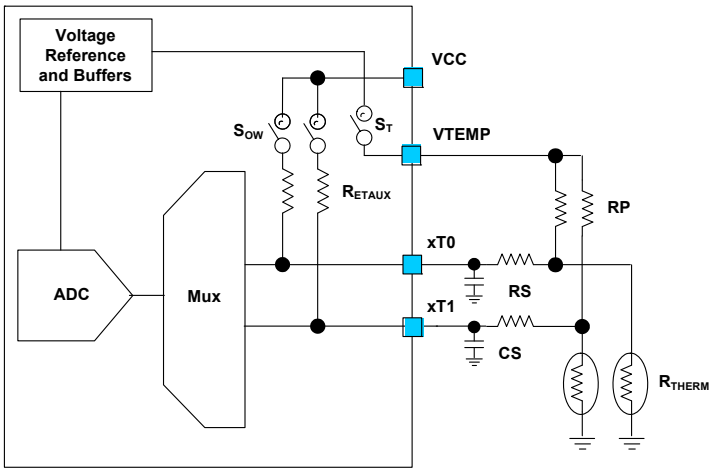


Figure 85. ETAUX Port Configured to Measure External Temperature

The RAA489206 ETAUX port consists of two analog input pins (xT0, xT1) that support two external thermistors, plus the VTEMP reference pin. Negative Temperature Coefficient thermistors (NTCs) typically measure temperature within the battery pack.

Battery cell temperature is monitored for safety purposes because of battery type and chemistry limits on when to allow charge or discharge. Other potential thermal monitoring locations are the DFET, CFET, or the current sense resistor.

5.6.1 0x11 - ETAUX Operation

The ETAUX Operation register controls the data acquisition behavior of the ETAUX inputs within the RAA489206.

Table 22. 0x11 ETAUX Operation Register

Bits	D[7:6]	D[5]	D[4:2]	D[1]	D[0]
Bit Name	ETAUX EN	RSV	ETAUX Averages	RSV	ETAUX Trigger
Default	11	0	0 00	0	0

5.6.1.1 0x11.7:6 - ETAUX Enable

If set to 1 (default), the ETAUX Enable bits include voltage measurement of the ETAUX pins xT0 and xT1 in SCAN mode. Set one or both bits to 0 to bypass measurement of the related pin during System Scans. See Table 23 for more information.

An 0x11.0 - ETAUX Trigger executes measurement of the enabled pins in IDLE or SCAN Mode.

Table 23. ETAUX Enable

D[7:6]		ETAUX Enable
0	0	ETAUX is Not Part of the System Scan
0	1	xT0 is Part of the System Scan
1	0	xT1 is Part of the System Scan
1	1	xT0 and xT1 is Part of the System Scan

5.6.1.2 0x11.5,1 - RSV

Reserve Bits 5 and 1 should be ignored during a read command and should be set to 0 during a write command.

5.6.1.3 0x11.4:2 - ETAUX Averages

The ETAUX Averages bits determine the number of samples averaged per measurement before reporting the results to the respective registers. The ETAUX averages bits control averaging for xT0 and xT1 measurements only. Table 24 lists the options for these bits.

Table 24. ETAUX Averages

ETAUX Averages: D[4:2]			Samples to Average
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

5.6.1.4 0x11.0 - ETAUX Trigger

For this bit, a transition from 0 to 1 in IDLE mode starts an ETAUX measurement. When received, the Busy bit transitions from 0 to 1 and the trigger bit clears. The Busy bit remains set until the action is completed and then returns to 0.

This trigger bit is ignored in SHIP and LOW POWER Modes and can trigger sequences in IDLE or SCAN mode only. This trigger should be used in IDLE mode because Renesas recommends reserving SCAN mode for System Scans only.

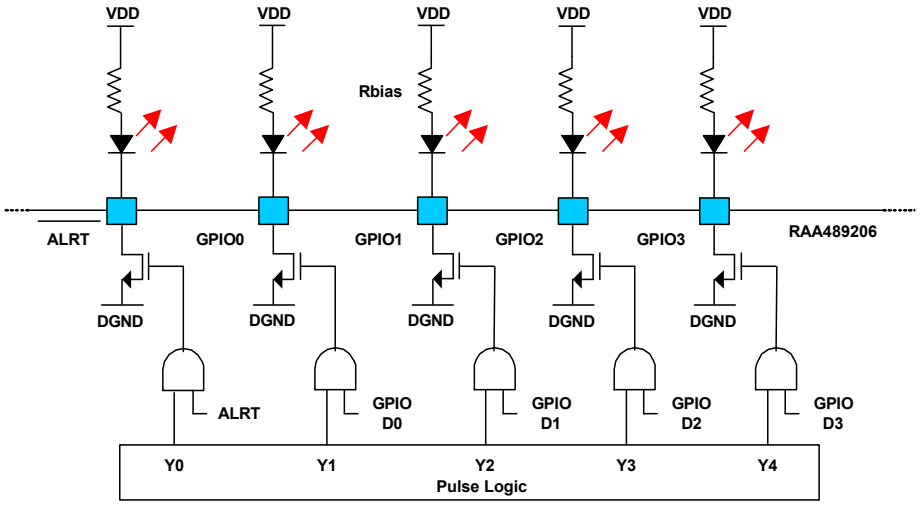


Figure 86. $\overline{\text{ALRT}}$ Pulse EN and GPIOx Drive LEDs

5.6.2 0x12 - $\overline{\text{ALRT}}$ and GPIO

This register displays the status of the GPIO pins and configures the GPIO port and the $\overline{\text{ALRT}}$ pin.

Table 25. 0x12 GPIO and $\overline{\text{ALRT}}$ Operation Register

Bits	D[7]	D[6]	D[5:4]	D[3:0]
Bit Name	$\overline{\text{ALRT}}$ Assert	$\overline{\text{ALRT}}$ PULSE EN	GPIO Config	GPIO Status
Default	0	0	01	1111

5.6.2.1 0x12.7 - $\overline{\text{ALRT}}$ Assert

The $\overline{\text{ALRT}}$ Assert bit forces the $\overline{\text{ALRT}}$ pin state to a low when the bit is set to 1. Clear the bit (default 0) to return the $\overline{\text{ALRT}}$ pin to normal operation. This bit enables testing of the connection between the $\overline{\text{ALRT}}$ pin and microcontroller.

5.6.2.2 0x12.6 - $\overline{\text{ALRT}}$ Pulse EN

The $\overline{\text{ALRT}}$ Pulse Enable bit can drive the $\overline{\text{ALRT}}$ pin in a more power efficient manner. When the bit is 1 and an alert is active, the RAA489206 turns on the $\overline{\text{ALRT}}$ pin output pull-down device for $GPIO_{pulse\_on}$ (~2ms) within a $GPIO_{pulse\_per}$ (~10ms) period. When this bit is 0 (Default) and an alert is active, the RAA489206 drives the $\overline{\text{ALRT}}$ pin LOW constantly. Figure 86 illustrates the circuit.

5.6.2.3 0x12.5:4 - GPIO CONFIG

GPIO Configuration bits allow the GPIO pins to be used as digital inputs, digital outputs, LED drivers, or as outputs to drive external power FET circuits. Table 26 shows the possible configurations of the GPIO port.

Table 26. GPIO Configuration Bits

D[5:4]	GPIO Configuration
00	Digital Inputs
01	Digital Outputs
10	Drive LED
11	Power FETs Gate Drive Out

See 0x12.3:0 - GPIO STATUS for Digital Input and Output configurations.

Drive LED: This option pulses the GPIO pins in a sequential manner to save power. Each GPIO pin is set LOW for $GPIO_{pulse\_on}$ (~2ms) within a $GPIO_{pulse\_per}$ (~10ms) period. A simplified schematic is shown in Figure 86. See 0x12.3:0 - GPIO STATUS to set the state of GPIO output. Set the GPIO Status bit to 1 to light an LED or to 0 to shut it off.

Power FETs Gate Drive Out: This selection enables the RAA489206 to be designed with a low-side FET configuration. It connects GPIO2 to the DFET state and GPIO3 to the CFET state. These states are dependent on bits 0x24.1 - DFET EN and 0x24.0 - CFET EN along with other settings and faults as described in CFET and DFET Pins (50, 51). The DFET and CFET states follow the same expected behavior of the DFET and CFET pins except that the state does not depend on the charge pump. That means the state can be on (LOW) even when the 0x24.7 - CPMP EN bit is 0 and/or the 0x65.5 - CPMP NRDY bit is 1 even though the high-side DFET and CFET pins are off. Table 27 defines the logic state of the GPIO output pins (3, 2, 0) as a function of the GPIO1 input, the device Mode, and the internal DFET and CFET enable bits.

GPIO1 is configured as a FETs Off digital input pin. If the logic input is high, both DFET and CFET GPIO pins, along with the high-side DFET and CFET pins (if enabled), turn off. If the logic input is low, the DFET and CFET states pass to GPIO2 and GPIO3. Before choosing this configuration, disable both CFET and DFET by setting their enable bits to 0; next, write 0x3E to register 0x12.

GPIO0 is configured as a FETs ON digital output pin. The output of the pin is LOW when CFET and DFET are both off. It is high impedance when one or both of the CFET and DFET GPIO outputs are on.

Table 27. GPIO Pins Logic States in FETs Out Mode

Internal State Variable			Input Pin	Output Pins		
Mode	DFET	CFET	FETs Off (GPIO1)	FETs On (GPIO0)	DFET (GPIO2)	CFET (GPIO3)
SCAN or IDLE	Off	Off	Low	Low	Hi-Z	Hi-Z
	Off	On	Low	Hi-Z	Hi-Z	low
	On	Off	Low	Hi-Z	Low	Hi-Z
	On	On	Low	Hi-Z	Low	Low
	X	X	High	Low	Hi-Z	Hi-Z
LOW POWER or SHIP	X	X	X	Hi-Z	Hi-Z	Hi-Z

5.6.2.4 0x12.3:0 - GPIO STATUS

The GPIO Status bits report the status of each GPIO pin. The GPIO Status bits are read only when configured as inputs. Reading these bits returns the input status of the GPIO pins.

If the GPIO pins are set up as Digital outputs, writing to these bits sets the GPIO pins state. Set a GPIO Status bit to 0 to pull the output pin low or to 1 to release it.

In Drive LED mode, set a GPIO Status bit to 1 to light an LED or to 0 to shut it off. The GPIO pins are connected to open-drain NMOS transistors designed to drive 2mA nominal LEDs. **Note:** Drive LED and Digital Output modes force the outputs to the opposite level given the same bit setting.

5.7 ETAUX Detectors

The ETAUX Detectors are threshold comparators that detect over-temperature and under-temperature conditions based on readings from the xT0 and xT1 pins. The ETAUX Fault Delay counters are bypassed if the part is not running in continuous SCAN mode. Figure 87 is the block diagram of the ETAUX fault detection function.

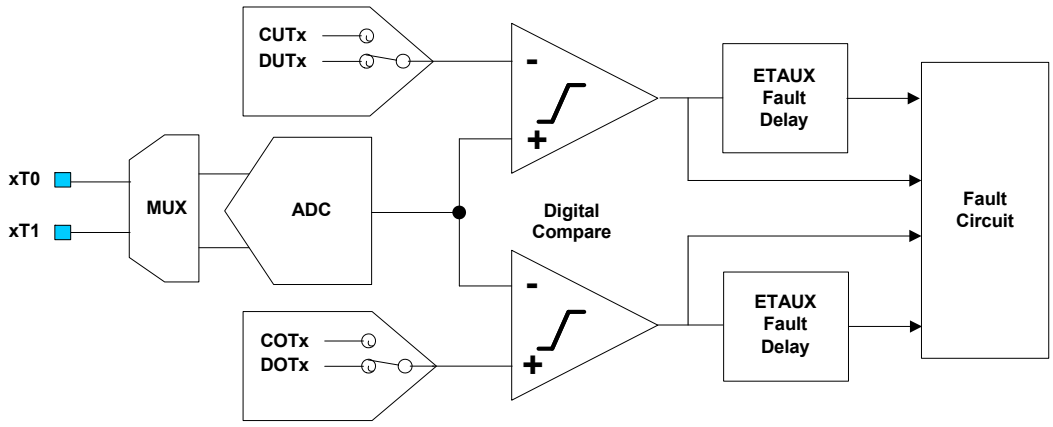


Figure 87. ETAUX Fault Detector Block Diagram

5.7.1 0x13-1A - ETAUX Thresholds

The Under-Temperature and Over-Temperature ETAUX fault detectors consist of two digital comparators with four digital thresholds for each ETAUX (xT0 or xT1) input. The device has two sets of limits to which the ETAUX readings are compared based on whether the pack is charging or discharging.

The thresholds for overvoltage (OT) and undervoltage (UT) are set by programing the CUTn, DUTn, COTn, and DOTn (n = 0 for AUX0/xT0 and n = 1 for AUX1/xT1) registers. Table 28 and Table 29 show the format of these registers.

Table 28. 0x13, 15, 17, 19 (D,C) UT Threshold Registers

Bit Name	Bits	Default	$ETAUX_{thstep}$	Offset
UT (OV) Threshold [7:0]	D[7:0]	1111 1111	6.276mV	6.263mV

Table 29. 0x14, 16, 18, 1A (D,C) OT Threshold Registers

Bit Name	Bits	Default	$ETAUX_{thstep}$	Offset
OT (UV) Threshold [7:0]	D[7:0]	0000 0000	6.276mV	6.263mV

To calculate the threshold voltage for all COT, DOT, CUT, and DUT registers, multiply the register value by the step size $ETAUX_{thstep}$, and add the offset (Equation 11). The registers support settings from 6.263mV to 1606.67mV.

(EQ. 11) $$VThreshold = (RegVal) \cdot ETAUX_{thStep} + Offset$$

Eight associated Fault/Indicator bits are located at Register Address 0x64 - ETAUX Fault. Each of the bits is linked to a UT or OT threshold register. Each time the RAA489206 measures AUX1/xT1 and AUX0/xT0 voltages (0x58-59 xT0, 0x5A-5B xT1 (R)), the results are compared to the relevant thresholds. If the external voltage is greater than the relevant UT threshold or less than or equal to the relevant OT threshold, the appropriate Fault/Indicator bit is set.

Each Fault/Indicator bit has a masking bit (see 0x84 - ETAUX Fault Mask) that connects the Fault/Indicator bit to the $\overline{ALRT}$ pin if cleared (set to 0/ The default is 1).

The bit 0x24.2 - ETA Connect determines if the ETAUX OT/UT faults control the power FETs automatically. These faults halt continuous scan regardless of ETA Connect.

UT thresholds detect under-temperature conditions when a pin connects to a negative temperature coefficient (NTC) circuit, or they detect overvoltage conditions when the pins are used for auxiliary input voltages.

OT thresholds detect over-temperature conditions when a pin connects to a negative temperature coefficient (NTC) circuit, or they detect undervoltage conditions when the pins are used for auxiliary input voltages.

The charge and discharge temperature comparisons are a function of bits 0x67.6 - CHRGI and 0x67.7 - DCHRGI. When the CHRGI bit is set, the AUXn readings are compared to the COT and CUT thresholds. When the DCHRGI bit is set, the AUXn readings are compared to the DUT and DOT threshold.

- When I_{PACK} < -20 (decimal), the chip compares V(xTn, VSS) to the COT/CUT thresholds.
- When I_{PACK} > 19, the chip compares V(xTn, VSS) to the DOT/DUT thresholds.
- When -20 ≤ I_{PACK} ≤ 19, the chip does not compare V(xTn, VSS) to any of the these thresholds.

If neither the CHRGI or DCHRGI bits are set, no action is taken in SCAN mode, but in IDLE mode a violation of any of these thresholds set the related fault bit.

5.7.2 0x58-59 xT0, 0x5A-5B xT1 (R)

The ETAUX Voltage registers report the voltage measurement readings for the xT0 and xT1 pins. Each register is two bytes.

Table 30. 0x58-5B ETAUX Voltage

Register Name	Address - Bits	Byte Order	$ETAUX_{Step}$
xT0/AUX0	0x58 - D[7:0]	MSB	24.52µV
	0x59 - D[7:0]	LSB	
xT1/AUX1	0x5A - D[7:0]	MSB	
	0x5B - D[7:0]	LSB	

(EQ. 12) $$xTnVoltage = (RegVal) \cdot ETAUX_{Step} + 0.5 \cdot ETAUX_{Step}$$

Multiply the 16-bit register value by the step size $ETAUX_{Step}$, and add the 1/2 LSB offset to calculate the voltage. The registers support values from 12.26µV to 1606.67mV.

These voltages are compared to 0x13-1A - ETAUX Thresholds, violations set fault bits in register 0x64 - ETAUX Fault and stop continuous scan. If the control bit 0x24.2 - ETA Connect is set, a fault in SCAN mode shuts off power FETs depending on the setting of 0x0E.3 - CPWR and current direction. A violation of any of these thresholds in IDLE mode sets the fault bit regardless of current direction.

5.8 Internal Temperature

5.8.1 0x22 - 0x23 - IOTW and IOTF Thresholds

The Internal Over-Temperature (IOT) Threshold detectors allow for two limit settings on the RAA489206 die temperature. The internal temperature sensor is monitored to prevent the die from over heating.

The Internal Over-Temperature Warning (IOTW) Threshold (0x22) is the first temperature threshold. It is intended to be a warning and sets the flag 0x66.6 - IOTW when the internal temperature exceeds its temperature limit.

If the internal temperature rises above the second temperature threshold, bit 0x63.5 - IOTF is set, the power FETs are disabled, and System Scan stops.

Both the IOTW and Internal Over-Temperature Fault (IOTF) bits require 0x09.5 - Other Fault Delay consecutive measurements in violation of the limit in continuous System Scan before the fault bit is set. The Other Fault Delay counters are bypassed if the part is not running in continuous SCAN mode. Figure 88 is the block diagram for the IOT detection functions.

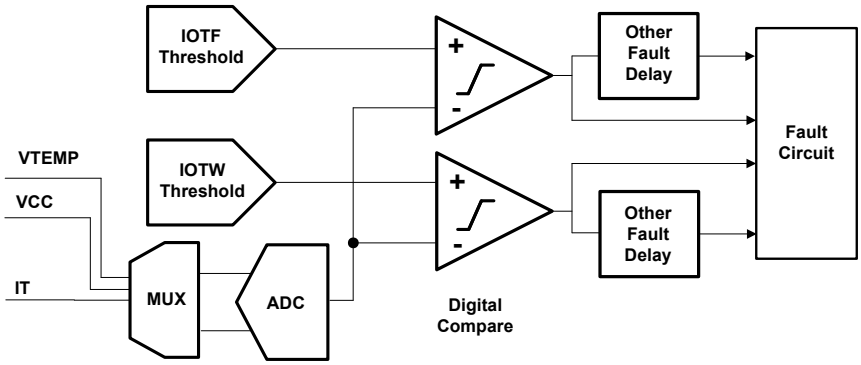


Figure 88. IOT Fault Detectors

Table 31 shows the format of these registers.

Table 31. 0x22, 0x23 IOT Threshold Registers

Bit Name	Bits	Default
Internal Over-Temperature Threshold (W or F)	D[7:0]	0x22 = 0x51 (~85C) 0x23 = 0x45 (~95C)

Setting IOT register(s) to the minimum of 0x00 equates to an internal temperature of +151.1°C. The maximum setting of 0xFF is -63.7°C. Round the result of Equation 13 to the nearest integer (max 255, min 0) to set the Temperature Threshold register values based on the desired temperature (°C).

(EQ. 13) $$RegVal = (-2.95\times10^{-4})\cdot Temp^{2} - 1.15975\cdot Temp + 182.23$$

Use Equation 14 to convert these two threshold register values (or the internal temperature register value) read from the RAA489206 to temperature in °C.

(EQ. 14) $$TempThreshold = (-1.82\times10^{-4})\cdot RegVal^{2} - 0.79605\cdot RegVal + 151.11$$

5.8.2 0x5E - Internal Temperature (R)

The Internal Temperature register reports the internal temperature of the RAA489206 based on an internal Negative Temperature Coefficient (NTC) temperature sensing circuit. As the internal temperature increases the voltage across the element decreases.

Use Equation 15 to calculate the internal temperature in °C directly from the register decimal value:

(EQ. 15) $$IT_{C} = (-1.82\times10^{-4})\cdot(RegVal^{2}) - 0.79605\cdot(RegVal) + 151.11$$

5.9 Regulator Measurements and Detectors

The regulator and voltage reference blocks with a typical external component configuration is illustrated in Figure 89. The external component configuration is detailed in Figure 98.

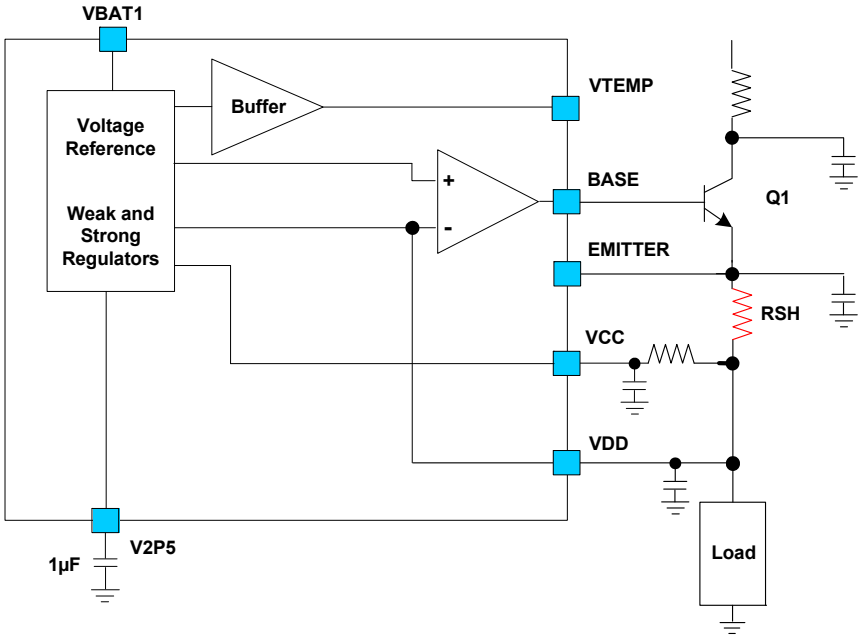


Figure 89. Regulator and Reference

The VBAT1 pin connects to internal regulators that have low current sourcing capabilities. Their purpose is to power up essential circuitry when the part starts up or is in LOW POWER or SHIP mode (with bit 0x1B.1 - LP REG set to 0).

The VCC pin is the analog power input of the device while the VDD pin is the digital power input. The VCC, VDD, and V2P5 pins have window comparators that monitor the voltages. If their respective voltages are outside the PG_{VCC}, PG_{VDD}, or PG_{2p5v} windows for 1ms, the device transitions to SHIP mode.

ADC multiplexer inputs (not shown) are connected to the VTEMP and VCC pins of the device. Voltage measurement of the these pins tests the health of the regulators and loads. The Emitter to VDD pin voltage is also measured by the ADC and is stored in register 0x61-62 - I_{REG} Voltage (R). This voltage can be used to calculate the NPN emitter current.

The amplifier driving the BASE pin sources a minimum of 1mA over the operating temperature range. This corresponds to a maximum regulation current of around 100mA assuming a minimum NPN β of 100.

5.9.1 0x1B - V_{REG} Operation

The V_{REG} Operation register holds settings for Communications Timeout, Other scan and load detect delays, regulator operation in LOW POWER and SHIP Modes and the V_{REG} measurement Trigger.

Table 32. 0x1B V_{REG} Operation Register

Bits	D[7:6]	D[5:4]	D[3:2]	D[1]	D[0]
Bit Name	Communications Timeout	Update Other	LD Delay	LP REG	V_{REG}Trig
Default	11	11	00	0	0

5.9.1.1 0x1B.7:6 - Communications Timeout

The Communications Timeout bits set the timeout period if bit 0x1F.1 - Communication Timeout EN is set (1) to enable the timer. The Communication Timeout Enable bit enables the t_{COM} timer that transitions the part from either SCAN or IDLE to LOW POWER Mode if no communications have been received in the selected time. The timeout setting is ignored if the Communication Timeout Enable bit is clear (0), disabling this feature and preventing the automatic mode transition.

Table 33. Timeout Selections

D[7:6]	Communications Timeout
00	128ms
01	512ms
10	2.048s
11	4.096s

5.9.1.2 0x1B.5:4 - Update Other

The Update Other bits set the number of System Scans required before ETAUX, V_{BAT1}, V_{VCC}, I_{REG}, V_{TEMP}, and Internal Temperature (IT) measurements are made in SCAN mode as part of continuous scans. Setting 00 enables an update on every System Scan while the other settings enable an update at other frequencies. This setting is ignored during single triggered scans.

Table 34. Update Other Bits

D[5:4]	Update Other Number of System Scans
00	1 (Update on every scan)
01	8 (Update on scan 1, 9, 17, 25...)
10	16 (Update on scan 1, 17, 33, 49...)
11	64 (Update on scan 1, 65, 129...)

5.9.1.3 0x1B.3:2 - LD Delay

The Load Detect time Delay bits set a time delay in addition to t_{LDEN} before testing for a load. Available settings for the LD Delay bits are listed in Table 35. See Short-Circuit Detection and Recovery, Load Detection, and LDMON Pin (49) for more information about load detection.

Table 35. Load Detect Time Delay

D[3:2]		LD Delay (s)
0	0	0.25
0	1	1
1	0	2
1	1	4

5.9.1.4 0x1B.1 - LP REG

The Low Power Regulator bit selects which regulator is on between sets of measurements during LOW POWER mode (measurements are not executed in SHIP mode). For the lowest power consumption in LOW POWER and SHIP Modes, set this bit to 0 (default, Weak regulator). This setting cannot power external circuitry in LOW POWER and SHIP Modes. A setting of 1 selects the Strong regulator that uses the external NPN transistor which can power external circuitry in both LOW POWER and SHIP Modes.

5.9.1.5 0x1B.0 - V_{REG} Trigger

For this bit, a transition from 0 to 1 in IDLE mode starts measurement of V_{VCC}, V_{VTEMP}, and I_{REG}. When received, the Busy bit transitions from 0 to 1, and the Trigger bit clears. The Busy bit remains set until the action is completed, and then returns to 0.

After measurement, the voltages are compared to the relevant threshold registers. See 0x60 - V_{VCC} Voltage (R), 0x5F - V_{VTEMP} Voltage (R), and 0x61-62 - I_{REG} Voltage (R) for details.

This trigger bit is ignored in SHIP and LOW POWER Modes and can trigger sequences in IDLE or SCAN mode only. This trigger should be used in IDLE mode because Renesas recommends to reserve SCAN mode for System Scans only.

5.9.2 0x1C - V_{VCC} Min Threshold

The V_{VCC} Minimum Threshold register sets the comparator threshold for the VCC voltage measurement. After a VCC measurement, this threshold voltage is compared to the measurement result stored at 0x60 - V_{VCC} Voltage (R). If the VCC voltage is less than or equal to the threshold, fault bit 0x63.7 - VCCF is set. This fault sets $\overline{ALRT}$ low if mask bit 0x83.7 is 0 (see 0x83 - Priority Fault Mask). Table 36 shows the format of this register.

Table 36. 0x1C V_{VCC} Min Threshold Register

Bit Name	Bits	Default	$V_{VCCStep}$
VCCMIN	D[7:0]	0000 0000	25.104mV

(EQ. 16) $VThreshold = (RegVal) \cdot V_{VCCStep} + 0.5 \cdot V_{VCCStep}$

Multiply the register value by the step size $V_{VCCStep}$ and add the ½ LSB offset to calculate the threshold value (Equation 16). The register supports settings from 12.55µV to 6.414V.

5.9.3 0x1D,1E - $IREG_{OC1, 2}$ Threshold

The Regulator Overcurrent Charge Threshold registers set the digital comparator overcurrent threshold for the EMITTER to VDD measurement. $IREG_{OC1}$ is the limit that the I_{REG} Voltage reading is compared to while the device is in SCAN or IDLE mode. $IREG_{OC2}$ is the limit that the reading is compared to while the device is in LOW POWER mode. After an I_{REG} measurement, the threshold voltage is compared to the measurement result stored at 0x61-62 - I_{REG} Voltage (R). If the I_{REG} measurement is greater than the threshold, the appropriate fault bit is set based on mode.

If the $IREG_{OC1}$ threshold comparison fails, the IREG1 fault bit 0x67.2 - IREG1 is set to 1 (applies in SCAN or IDLE modes). This fault sets $\overline{ALRT}$ low if mask bit 0x87.2 is set to 0 (see 0x87 - Status Mask).

If the $IREG_{OC2}$ threshold comparison fails, the IREG2 fault bit 0x67.1 - IREG2 is set to 1 (applies in LOW POWER mode). This fault sets $\overline{ALRT}$ low if mask bit 0x87.1 is set to 0 (see 0x87 - Status Mask).

Table 37. 0x1D $IREG_{OC1}$ and 0x1E $IREG_{OC2}$ Threshold Registers

Bit Name	Address - Bits	Default	$IREGOC_{Step}$	Offset
$IREG_{OC1}$	0x1D - D[7:0]	1111 1111	1.345mV	1.3396mV
$IREG_{OC2}$	0x1E - D[7:0]	1111 1111		

(EQ. 17) $VThreshold = (RegVal) \cdot IREGOC_{Step} + Offset$

Multiply the register value by the step size $IREGOC_{Step}$ and add the fixed offset from Table 37 to calculate the threshold (Equation 17). The registers support settings from 1.34mV to 344.28mV.

5.9.4 0x5F - V_{VTEMP} Voltage (R)

The V_{VTEMP} Voltage register stores the result from the measurement of the V_{TEMP} pin voltage, which is included in the group of measurements done in LOW POWER mode, in any System Scan, and in the group of measurements triggered with 0x1B.0 - V_{REG} Trigger in IDLE mode. The VTEMP reference voltage powers the external thermistors. After measurement, the voltage is compared to the threshold $VTEMP_{Min}$ (1.1V typical). If the voltage is less than or equal to the threshold, fault bit 0x67.0 - VTMPF is set. This fault can set $\overline{ALRT}$ low if mask bit 0x87.0 is set to 0 (see 0x87 - Status Mask).

Table 38. 0x5F V_{VTEMP} Voltage

Bits	Default	$V_{VTEMPStep}$	Offset
D[7:0]	N/A	3.138mV	804.908mV

(EQ. 18) $V_{VTEMP} = (RegVal) \cdot V_{VTEMPStep} + Offset$

Multiply the register value by the step size $V_{VTEMPStep}$, and add the fixed offset (minimum value of the V_{VTEMP} range) to calculate the voltage Equation 18. The register records results from 804mV to 1.605V.

5.9.5 0x60 - V_{VCC} Voltage (R)

The V_{VCC} Voltage register stores the result from the internal measurement of the VCC pin voltage. The voltage measurement is compared to the threshold register Power FET Block. If the comparison fails, the fault bit 0x63.7 - VCCF is set. This fault sets $\overline{ALRT}$ low if the mask bit 0x83.7 is set to 0 (see 0x83 - Priority Fault Mask).

Multiply the register value by the step size $V_{VCCStep}$ (Table 39) and add the ½ LSB offset to calculate the voltage Equation 19. The register records results from 12.55µV to 6.414V.

Table 39. 0x60 V_{VCC} Voltage

Bits	Default	V_{VCCtep}
D[7:0]	N/A	25.104mV

(EQ. 19) $$V_{VCC} = (RegVal) \cdot V_{VCCStep} + 0.5 \cdot V_{VCCStep}$$

5.9.6 0x61-62 - I_{REG} Voltage (R)

The read only I_{REG} registers contain the 16-bit result of the measurement of the voltage across the sense resistor between the EMITTER and VDD pins. After measurement, the voltage is compared to the 0x1D $IREG_{OC1}$ threshold register in SCAN or IDLE modes or the 0x1E $IREG_{OC2}$ threshold register if in LOW POWER mode (see 0x1D,1E - $IREG_{OC1, 2}$ Threshold). If the 0x1D $IREG_{OC1}$ comparison fails, the fault bit 0x67.2 - IREG1 is set. If the 0x1E $IREG_{OC2}$ comparison fails, the fault bit 0x67.1 - IREG2 is set. These faults set $\overline{ALRT}$ low if mask bits IREG1 and IREG2 are 0 (see 0x87 - Status Mask).

Table 40. 0x61-62 I_{REG} Voltage

Address - Bits	Byte Order	$IREG_{Step}$
0x61 - D[7:0]	MSB	10.507µV
0x62 - D[7:0]	LSB	

(EQ. 20) $$V_{IREG} = (RegVal) \cdot IREG_{Step} + 0.5 \cdot IREG_{Step}$$

Multiply the 16-bit register value by the step size $IREG_{Step}$ and add the ½ LSB offset to calculate the voltage (Equation 20); next, divide by the sense resistor value to calculate the current. The register records results from 5.25µV to 344.28V.

5.10 V_{BAT1}

5.10.1 0x1F - V_{BAT1} Operation

The V_{BAT1} Operation register enables and/or triggers measurement of V_{BAT1} and I_{TEMP}. It also controls averaging for these and regulator measurements.

Table 41. 0x1F V_{BAT1} Operation Register

Bits	D[7]	D[6]	D[5]	D[4:2]	D[1]	D[0]
Bit Name	V_{BAT1} EN	I_{TEMP} EN	I_{TEMP} Trigger	OTHER Averages	COMM TO EN	V_{BAT1} Trigger
Default	1	1	0	0 00	1	0

5.10.1.1 0x1F.7 - V_{BAT1} EN

The V_{BAT1} Enable bit set to 1 (default) includes V_{BAT1} measurement during System Scans. The measurement is excluded if this bit is set to 0. This bit has no effect on V_{BAT1} Trigger. The result of a V_{BAT1} voltage measurement is stored in register 0x5C - 0x5D - V_{BAT1} Voltage (R).

5.10.1.2 0x1F.6 - I_{TEMP} EN

The Internal Temperature Enable bit set to 1 (default) includes an internal temperature measurement during System Scans. The measurement is excluded if this bit is set to 0. This bit has no effect on I_{TEMP} Trigger. The result of a I_{TEMP} voltage measurement is stored in register 0x5E - Internal Temperature (R).

5.10.1.3 0x1F.5 - I_{TEMP} Trigger

For this bit, a transition from 0 to 1 instructs the device to start an I_{TEMP} measurement. When received, the Busy bit transitions from 0 to 1 and the trigger bit is cleared. The Busy bit remains set until the action is completed and then returns to a 0.

This trigger bit is ignored in SHIP and LOW POWER Modes and can only trigger sequences in IDLE or SCAN mode. This trigger should be used in IDLE mode because Renesas recommends to reserve SCAN mode for System Scans only.

5.10.1.4 0x1F.4:2 - Other Averages

The Other Averages bits set the number of samples averaged before passing the measurement results to the respective registers. The Other Averaging bits control averaging for 0x5C - 0x5D - V_{BAT1} Voltage (R), 0x60 - V_{VCC} Voltage (R), 0x61-62 - I_{REG} Voltage (R), 0x5F - V_{VTEMP} Voltage (R) and 0x5E - Internal Temperature (R). Table 42 lists the options for this bit.

Table 42. Other Averages

Other Averages: D[4:2]			Samples to Average
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

The conversion time for these measurements is estimated using Equation 21:

(EQ. 21) $$OTHER_{CT} = (3 + SamplesToAverage) \cdot ADC_{CT2}$$

ADC_{CT2} is the base conversion time of the ADC.

5.10.1.5 0x1F.1 - Communication Timeout EN

The Communication Timeout Enable bit enables the t_{COM} timer that transitions the part from SCAN or IDLE to LOW POWER mode if no communications have been received in the selected time. Set the bit to 1 (default) to enable the timer. Set to 0 to disable this feature and prevent the automatic mode transition. See 0x1B.7:6 - Communications Timeout for the timer settings available.

5.10.1.6 0x1F.0 - V_{BAT1} Trigger

For this bit, a transition from 0 to 1 instructs the device to start a V_{BAT1} measurement. When received, the Busy bit transitions from 0 to 1 and the trigger bit is cleared. The Busy bit remains set until the action is completed and returns to 0.

This trigger bit is ignored in SHIP and LOW POWER Modes and can trigger sequences in IDLE or SCAN mode only. This trigger should be used in IDLE mode because Renesas recommends to reserve SCAN mode for System Scans only.

5.10.2 0x20 - 0x21 - V_{BAT1} Thresholds

The V_{BAT1} Threshold registers set the upper and lower voltage thresholds that are compared to V_{BAT1} measurements. A violation of these thresholds may result in a disconnection of the power FETs. See 0x24.3 - VBAT1 CON. The simplified block diagram of the V_{BAT1} fault detection functions is illustrated in Figure 90.

The 0x09.5 - Other Fault Delay counters are bypassed if the part is not running in continuous SCAN mode.

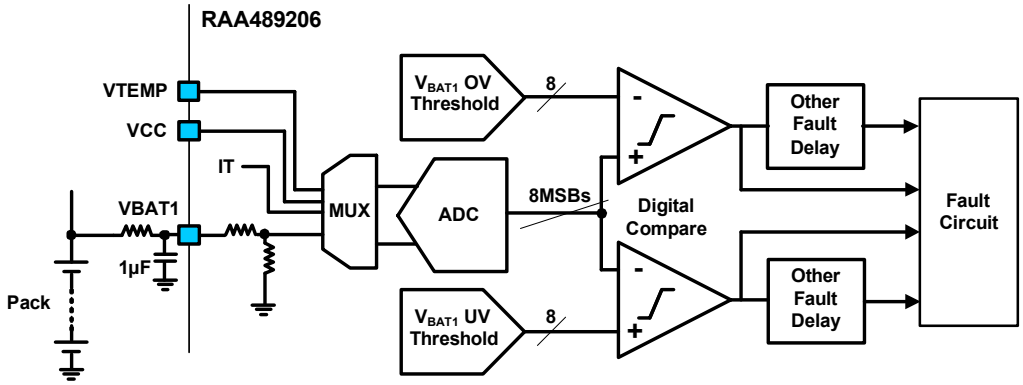


Figure 90. V_{BAT} OV/UV Detectors

5.10.2.1 0x20 - V_{BAT1} OV Threshold

The V_{BAT1} OV Threshold register sets the threshold voltage for the digital comparator that monitors for V_{BAT1} overvoltage. The V_{BAT1} overvoltage threshold register format is shown in Table 43.

Table 43. 0x20 OV_{BAT1} Threshold Register

Bit Name	Bits	Default	$VBAT1_{thStep}$	Offset
V_{BAT1} OV Threshold	D[7:0]	1111 1111	301.25mV	300.66mV

Multiply the register value by $VBAT1_{thStep}$ and add the fixed offset to calculate the threshold (Equation 22). The register supports settings from 300.66mV to 77.12V.

(EQ. 22) $$VThreshold = (RegVal) \cdot VBAT1_{thStep} + Offset$$

If the measured V_{BAT1} voltage exceeds this threshold for more than 0x09.5 - Other Fault Delay Scans during charge, then the fault 0x65.7 - VBOVF is set. The Other Fault Delay counter is bypassed if the part is not running in continuous SCAN mode.

5.10.2.2 0x21 - V_{BAT1} UV Threshold

The V_{BAT1} UV Threshold register sets the threshold voltage for the digital comparator that monitors for V_{BAT1} undervoltage. The V_{BAT1} undervoltage threshold register format is shown in Table 44.

Table 44. 0x21 UV_{BAT1} Threshold Register

Bit Name	Bits	Default	$VBAT1_{thStep}$	Offset
UVBAT1	D[7:0]	0000 0000	301.25mV	300.66mV

Multiply the register value by $VBAT1_{thStep}$ and add the fixed offset to calculate the threshold (Equation 22). The register supports settings from 300.66mV to 77.12V.

If the measured V_{BAT1} voltage is less than or equal to this threshold for more than 0x09.5 - Other Fault Delay scans during discharge, fault 0x65.6 - VBUVF is set. The Other Fault Delay counter is bypassed if the part is not running in continuous SCAN mode.

5.10.3 0x5C - 0x5D - V_{BAT1} Voltage (R)

The V_{BAT1} Voltage register stores the measured value of the voltage between the V_{BAT1} and VSS pins. The pin voltage is divided internally for measurement.

Table 45. 0x5C-5D V_{BAT1} Voltage

Address - Bits	Byte Order	$VBAT1_{Step}$
0x5C - D[7:0]	MSB	1.177mV
0x5D - D[7:0]	LSB	

Multiply the register value by the step size $VBAT1_{Step}$ and add the 1/2 LSB offset to calculate the voltage with Equation 23. The register records results from 588µV to 77.12V.

(EQ. 23) $$V_{BAT1} = (RegVal) \cdot VBAT1_{Step} + 0.5 \cdot VBAT1_{Step}$$

5.11 Power FET Block

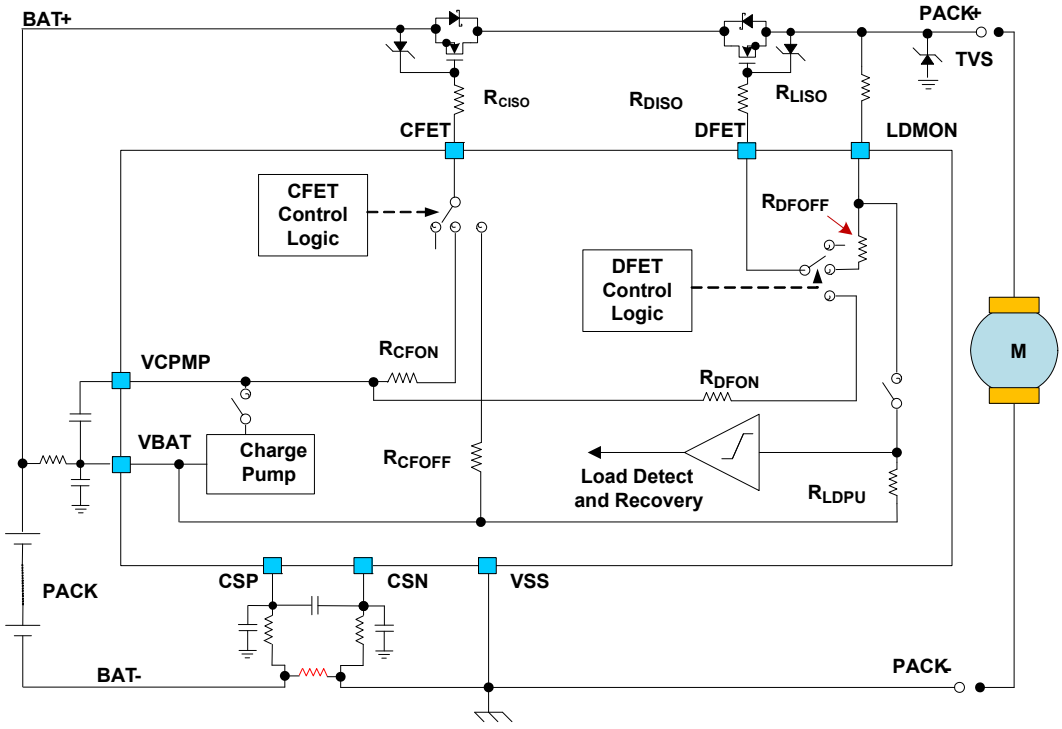


Figure 91. Block Diagram of Power FET Controls

5.11.1 0x24 - Power FET Operation

The Power FET Operation register allows control of power FET and Open Wire functionality within the RAA489206. This includes enable/disable of the charge pump and power FETS, and whether Cell, VBAT1 or ETAUX threshold violations can disconnect power FETs. Table 46 shows the format of this register.

See CFET and DFET Pins (50, 51) and Scan Will Not Start for details about how the Connect and Enable bits interact with fault and other control bits for FET control and System Scan.

Table 46. 0x24 Power FET Operation Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	CPMP EN	OW EN	OW Trigger	CELL CON	VBAT1 CON	ETA CON	DFET EN	CFET EN
Default	0	1	0	1	1	1	0	0

5.11.1.1 0x24.7 - CPMP EN

The Charge Pump Enable bit enables the charge pump in IDLE or SCAN Modes if set to 1. Set the bit to 0 (default) to disable the charge pump circuitry. The charge pump provides a biasing voltage to CB16. Disabling the charge pump reduces the CB16 pin maximum voltage.

When the charge pump is enabled (in IDLE or SCAN) and its output voltage rises above V_{pmpMin}, bit CPMP NRDY is automatically cleared to 0. If the voltage drops below $V_{pmpFall}$, bit 0x65.5 - CPMP NRDY is set to 1. If CPMP EN is set to 0, CPMP NRDY = 0.

There is a delay of about 1ms from enabling the charge pump, and also from setting CPMP NRDY to 1 by the $V_{pmpFall}$ comparator, before the $V_{pumpMin}$ comparator is allowed to clear CPMP NRDY.

If enabled, the charge pump circuitry is powered down when the device transitions to LOW POWER or SHIP mode, though the setting of the CPMP EN bit is not changed. When the device transitions back to IDLE or SCAN

mode, the charge pump restarts. If the CFET EN and/or DFET EN bits are 1, CFET and/or DFET drivers are also turned back on.

5.11.1.2 0x24.6 - OW EN

Set the Open-Wire enable bit to 1 (default) to include an open-wire test sequence during System Scans. Set this bit to 0 to disable open-wire test during System Scans. The frequency of open-wire tests is selected by bits 0x03.6:5 - OW Update.

During an open-wire test a current measurement is always performed, independent of the setting of the I_{PACK} EN bit 0x03.7. The current measurement determines if the device is discharging while the open-wire test is being performed. The results of the VSS and VBAT open-wire tests may be invalid during discharge so they are omitted.

5.11.1.3 0x24.5 - OW Trigger

The Open-Wire Trigger bit initiates an open-wire test sequence regardless of the setting of 0x24.6 OW Enable. For this bit, a transition from 0 to 1 instructs the device to start an open-wire test sequence. When the open-wire test has started, the Trigger bit clears, the Busy bit is set until the test complete and then it also clears. See Open-Wire Function for more information.

This Trigger bit is ignored in SHIP and LOW POWER modes and can trigger sequences in IDLE or SCAN mode only. This trigger should be used in IDLE mode because Renesas recommends to reserve SCAN mode for System Scans only.

The Open-Wire test sequence does not check the ETAUX pins; these must be checked separately. See Aux Pins Open-Wire Test for details.

5.11.1.4 0x24.4 - CELL CON

The V_{CELL} Connect bit connects the outputs of the Delta V_{Cell}, UV and OV comparators from a V_{CELL} scan to the FET control block. If any of the cell voltage OV, UV, or delta V_{CELL} max thresholds are violated (see 0x06 - 0x07 - V_{CELL} OV Threshold and V_{CELL} UV Threshold and 0x08 - V_{CELL} Max Delta Threshold), the CFET and/or DFET may be turned off per the setting of 0x0E.3 - CPWR. A 1 (default) connects the V_{CELL} fault outputs to the FET controller. Setting this bit to 0 moves fault handling responsibility to the MCU as these faults do not disconnect the power FET(s).

Continuous scans are halted on detection of these faults regardless of the setting of V_{CELL} Connect. See CFET and DFET Pins (50, 51) and Scan Will Not Start for details on fault reaction.

5.11.1.5 0x24.3 - VBAT1 CON

The V_{BAT1} Connect bit connects the results from the V_{BAT1} comparison bits to the FET control block. A 1 (default) connects the V_{BAT1} fault outputs to the FET controller.

If the measurement result for V_{BAT1} (0x20 - 0x21 - V_{BAT1} Thresholds) exceeds the OV threshold at 0x20 (0x20 - 0x21 - V_{BAT1} Thresholds) when bit 0x0E.3 - CPWR is set to 0, both CFET and DFET are shut off and System Scan is stopped.

- If CPWR is set to 1 and 0x67.6 - CHRGI is 1, a V_{BAT1} OV shuts off CFET.
- If CPWR is set to 1 and 0x67.7 - DCHRGI is 1, a V_{BAT1} UV shuts off DFET

Setting the VBAT1CON bit to 0 moves fault handling responsibility to the MCU because failing results from V_{BAT1} threshold comparisons do not disconnect the Power FET(s), though continuous scans are halted.

5.11.1.6 0x24.2 - ETA Connect

The External Temperature and Auxiliary Port Connect bit connects the results from the ETAUX comparison bits to the FET Control block. A 1 (default) connects the ETAUX fault outputs to the FET Controller.

If the measurement result for either the xT0 or xT1 voltage exceeds the related CUT threshold at 0x13 or 0x17 while CHRGI is 1 and CPWR is 0, the power FETs are disconnected and System Scan is stopped. If the CPWR bit is 1, in this case only, CFET is shut off.

If the measurement result for either the xT0 or xT1 voltage exceeds the related DUT threshold at 0x15 or 0x19 while DCHRGI is 1 and CPWR is 0, the power FETs are disconnected and System Scan is stopped. If the CPWR bit is 1, in this case only, DFET is shut off.

If the measurement result for either the xT0 or xT1 voltage drops below either the COT threshold at 0x14 or 0x18 while CHRGI is 1 and CPWR is 0, the power FETs are disconnected and System Scan is stopped. If the CPWR bit is 1, in this case only, CFET is shut off.

If the measurement result for either the xT0 or xT1 voltage drops below either the DOT threshold at 0x16 or 0x1A while DCHRGI is 1, and CPWR is 0, the power FETs are disconnected and System Scan is stopped. If the CPWR bit is 1, in this case only, DFET is shut off.

Setting the External Temperature and Auxiliary Port Connect bit to 0 moves fault handling responsibility to the MCU because these faults do not disconnect the power FET(s), though continuous scans are halted.

See the following sections for more information: ETAUX Detectors, 0x13-1A - ETAUX Thresholds, 0x67.6 - CHRGI, 0x67.7 - DCHRGI, and 0x0E.3 - CPWR.

5.11.1.7 0x24.1 - DFET EN

The DFET enable bit turns the DFET ON and OFF. A 1 activates the DFET unless prevented by a related fault. The default value of 0 disables the DFET. The DFET cannot be enabled when the chip is being reset, or if it is in LOW POWER or SHIP Modes. In the case of some faults, writing this bit does not turn on the DFET until the fault is cleared. This bit does not indicate the DFET pin status if a related fault is set.

The DFET is turned off and remains off under the following conditions:

```
[DSCF OR IOTF OR OWF OR VCCF OR CPMP NRDY OR IREG1 OR VTMPF]
OR
[NOT(CPWR) AND FCDC AND CHRGI AND COCF] OR [CFD AND DCHRGI AND DOCF]
```

The DFET is turned off and remains off under the following conditions if bit 0x24.4 CELLCON is set:

```
{CPWR AND [DVCF OR UVF OR (NOT{DCHRWOV} AND OVF)]}
OR
NOT(CPWR) AND {DVCF OR [CHRGI AND NOT(CHRWUV) OR DCHRGI] AND UVF
OR
[DCHRGI AND NOT(DCHRWOV) OR CHRGI] AND OVF}
```

V_{Cell} OVF does not disable DFET during discharge if bit 0x02.6 - DCHRWOV is set.

The DFET is turned off and remains off under the following conditions if bit 0x24.3 VBAT1CON is set:

```
[CPWR AND DCHRGI AND VBUVF] OR [NOT(CPWR) AND CHRGI AND VBOVF]
```

The DFET is turned off and remains off under the following conditions if bit 0x24.2 ETAUX Connect is set:

```
[DCHRGI AND (DUT0 OR DUT1 OR DOT0 OR DOT1)]
OR
[NOT(CPWR) AND CHRGI AND (CUT0 OR CUT1 OR COT0 OR COT1)]
```

See CFET and DFET Pins (50, 51) and Scan Will Not Start for details about how the Connect and Enable bits interact with fault and other control bits for FET control and System Scan.

5.11.1.8 0x24.0 - CFET EN

The CFET enable bit turns the CFET ON and OFF. A 1 activates the CFET unless prevented by a related fault. The default value of 0 disables the CFET. The CFET cannot be enabled when the chip is being reset, or if it is in LOW POWER or SHIP Modes. In the case of some faults, writing this bit does not turn on the CFET until the fault is cleared. This bit does not indicate status of the CFET pin if a related fault is indicated.

The CFET is turned off and remains off under the following conditions:

```
[DSCF OR IOTF OR OWF OR VCCF OR CPMP NRDY OR IREG1 OR VTMPF]
OR
[FCDC AND CHRGI AND COCF] OR [NOT(CPWR) AND CFD AND DCHRGI AND DOCF]
```

The CFET is turned off and remains off under the following conditions if bit 0x24.4 CELLCON is set:

```
{CPWR AND [DVCF OR OVF OR (NOT{CHRWOV} AND UVF)]}
OR
NOT(CPWR) AND {DVCF OR [CHRGI AND NOT(CHRWUV) OR DCHRGI] AND UVF
OR
[DCHRGI AND NOT(DCHRWOV) OR CHRGI] AND OVF}
```

V_{Cell} UVF does not disable the CFET during charge if bit 0x02.5 - CHRWUV is set.

The CFET is turned off and remains off under the following conditions if bit 0x24.3 VBAT1CON is set:

```
{NOT(CPWR) AND [CHRGI AND VBOVF OR DCHRGI AND VBUVF]}
OR
[CPWR AND CHRGI AND VBOVF]
```

The CFET is turned off and remains off under the following conditions if bit 0x24.2 ETAUX Connect is set:

```
[CHRGI AND (CUT0 OR CUT1 OR COT0 OR COT1)]
OR
[NOT(CPWR) AND DCHRGI AND (DUT0 OR DUT1 OR DOT0 OR DOT1)]
```

See CFET and DFET Pins (50, 51) and Scan Will Not Start for details about how Connect and Enable bits interact with fault and other control bits for FET control and System Scan.

5.12 Cell Balancing Registers

5.12.1 0x25 - CB Operation

The CB Operation register controls cell balancing features of the RAA489206. Table 47 shows the CB Operation register. Though some settings are automatically cleared on completion, Renesas recommends setting this register to default when cell balancing is not in operation.

Table 47. 0x25 CB Operation Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	CB EN	Auto CB EN	CB Config	CB TRIG	IEOC EN	CB Mask	CB EOC	CB CHRG
Default	0	0	0	0	0	0	0	1

5.12.1.1 0x25.7 - CB EN

Set this bit to 1 to enable cell balancing. Set this bit to 0 (default) to disable all forms of cell balancing.

5.12.1.2 0x25.6 - Auto CB EN

Set this bit to 1 for the RAA489206 to automatically select the cells to be balanced. If this bit is set to 0 (default), you must select the cells to be balanced in registers 0x26-27 - CB Cell State.

When the bit 0x66.7 - BAT FULL is set high indicating the completion of a charging cycle, bit Auto CB EN is reset to 0. This means the microcontroller must clear the battery-full bit before enabling Auto CB EN and the next cycle of cell balancing. See Automatic Cell Balancing for more information.

5.12.1.3 0x25.5 - CB Configuration

The CB Configuration bit sets the RAA489206 cell balance configuration to drive internal cell balancing FETs when the bit is set to 0 (default) or to drive external cell balancing FETs if set to 1.

The internal cell balancing FETs (Figure 92) are a space saving feature ideal for low current and slow battery charging applications.

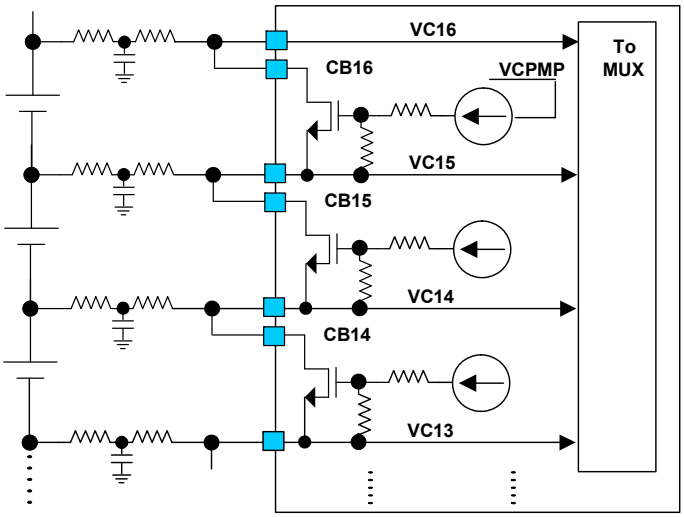


Figure 92. Internal Cell Balancing Configuration

Set the CB Config bit to 1 to configure the RAA489206 to drive external cell balancing FETs as shown in Figure 93. External balancing FETs are used with large capacity and/or fast charging battery packs.

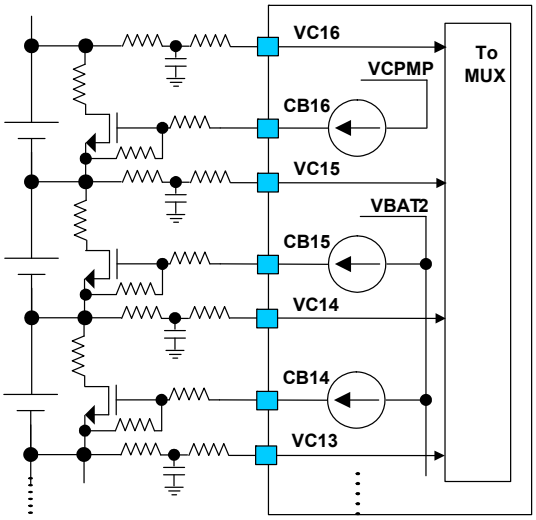


Figure 93. External Cell Balancing Configuration

5.12.1.4 0x25.4 - CB Trigger

For this bit, a transition from 0 to 1 in IDLE mode triggers one Cell Balancing cycle (Figure 94). When triggered, the Busy bit transitions from 0 to 1 and the trigger bit clears. The Busy bit remains set until the action is completed, and then returns to a 0.

The trigger bit is ignored in SHIP and LOW POWER Modes and can only trigger sequences in IDLE or SCAN mode. This trigger should be used only in IDLE mode because Renesas recommends to reserve SCAN mode for System Scans.

5.12.1.5 0x25.3 - IEOC EN

The Current End Of Charge Enable bit selects between ending charging when a voltage is reached or when the charge current drops below a set level. If IEOC EN is 0 (default), charging ends when any cell voltage reading is above the 0x2D - VEOC Threshold, which sets bits 0x66.4 - VEOC and 0x66.7 - BAT FULL, and shuts off CFET and DFET (if CPWR = 0). When IEOC EN is set to 1, charging stops after the VEOC bit has been set (DFET shuts off if CPWR=1) and the charge current drops below the 0x10 - IEOC Threshold, setting the bit 0x66.5 - IEOC. This shuts off CFET and DFET (if CPWR = 0) and BAT FULL sets.

IEOC EN does not enable or disable cell balancing, but determines which cells would be balanced (if any), and how the BAT FULL bit is set. IEOC EN combined with 0x0E.3 - CPWR determines when or if DFET is shut off. The IEOC EN, CB EOC, and CB CHRG bits select the type of cell balancing when auto cell balancing is enabled. See Automatic Cell Balancing for more information about the behavior of cell balancing versus these bits and related bit settings.

5.12.1.6 0x25.2 - CB Mask

The CB Mask bit prevents adjacent cells from balancing at the same time. Balancing adjacent cells may change the amount of cell balancing current.

If the CB mask bit is 1, the RAA489206 prevents turning on cell balancing FETs of adjacent cells at the same time. Instead, it toggles between two masks that either enable even cells or odd cells to be balanced for a period of time. For a cycle of cell balancing, each mask is applied once for CBON time before turning off cell balancing for CBOFF time (see 0x28, 0x29 - Cell Balancing Timers). The default of 0 disables the masking feature while balancing. The temperature rise of the IC because of the cell balancing FETs can be calculated using Equation 24.

(EQ. 24) $$\Delta T_{CB} = (\theta_{JA} \cdot no_{cbOn} \cdot I_{CB}^{2} \cdot R_{cb\_On})$$

ΔT_{CB} is the temperature rise of the RAA489206 because of cell balancing. Variable no_{cbOn} is the number of cells that are balancing at once, R_{CB_ON} is the cell balancing FET resistance, I_{CB} is the cell balancing current, and θ_{JA} (Thermal Information) is the thermal resistivity of the RAA489206.

5.12.1.7 0x25.1 - CB EOC

The Cell Balance End Of Charge bit is functional only when bit 0x66.4 - VEOC is set (1). The default CB EOC value of 0 disables cell balancing when any cell voltage reaches the setting of 0x2D - VEOC Threshold. If bit CB EOC is set to 1, cell balancing is allowed after one or more cells reach the VEOC threshold, and may continue (depending on settings and conditions) until bit 0x66.7 - BAT FULL is set. See Table 74.

The CB EOC, IEOC EN, and CB CHRG bits select the type of auto cell balancing when cell balancing is enabled. See Automatic Cell Balancing for more information.

5.12.1.8 0x25.0 - CB CHRG

The CB Charge bit is functional only when bit 0x66.4 - VEOC is clear (0). When 0, the CB CHRG bit disables cell balancing during constant current charging while VEOC = 0. Set CB CHRG to 1 to enable cell balancing during charging while VEOC = 0. The type of cell balancing is determined by this bit and the other control bits in this register. For more details, see Automatic Cell Balancing.

When bit 0x66.7 - BAT FULL is set to 1, both the Auto CB EN and CB CHRG bits are cleared.

5.12.2 0x26-27 - CB Cell State

The CB Cell State registers indicate the cells selected to be balanced during the next cell balancing cycle. Table 48 shows the format of these registers.

Table 48. 0x26-27 CB Cell State Register

Bit Name	Address - Bits	Default Value
CB Cells 16 to 9	0x26 - D[7:0]	0000 0000
CB Cells 8 to 1	0x27 - D[7:0]	0000 0000

In manual mode, when 0x25.6 - Auto CB EN is set to 0, these bits are written by you. Setting these bits to 1 turns on the cell balancing current source or internal cell balancing FET corresponding to that bit when cell balancing is enabled and triggered.

The CB Cell State registers show the cells automatically determined by the chip to need cell balancing following the most recent set of cell voltage measurements during automatic cell balancing.

For the three cases of automatic cell balancing with IEOC EN = 1 **OR** CB EOC = 0, the chip finds the minimum of all the cell voltages and calculates the difference between each cell voltage and the minimum. For cells with a calculated difference higher than the 0x2A - CB Min Delta Threshold, the CB Cell State bit is set to 1. For other cells, it is set to 0.

For automatic cell balancing cases with IEOC EN = 0 **AND** CB EOC = 1, the CB Cell State bit is set to 1 for cells that exceed the voltage set by the register 0x2D - VEOC Threshold minus four bits. For other cells, it is set to 0.

These registers do not indicate that any specific cell balancing pin is active. They indicate which cells are to be balanced during the next cell balancing cycle. See Automatic Cell Balancing and Manual Cell Balancing for more details.

5.12.3 0x2A - CB Min Delta Threshold

The Cell Balancing Minimum Delta Threshold register sets the minimum cell voltage difference that determines if a cell needs balancing. Table 49 shows the format of this register.

Table 49. 0x2A CB Min Delta Threshold Register

Byte Name	Bits	Default	$CBDMIN_{step}$	Offset
CBDMIN - Cell Balance Minimum Delta Threshold	D[7:0]	0000 0000	4.707mV	4.67mV

After a cell voltage scan has completed, the RAA489206 calculates all the differences between the lowest cell voltage and the rest of the cells in the battery pack. Under certain conditions, the delta value of each cell is compared to the CBDMIN threshold to determine if the cell needs balancing for automatic cell balancing cycles. If any cell needs balancing, the bit 0x66.0 - Need CB is set to 1. See 0x26-27 - CB Cell State for information about how this threshold is used to set those bits.

(EQ. 25) $$VThreshold = (RegVal) \cdot CBDMIN_{Step} + Offset$$

Multiply the register value by the step size $CBDMIN_{step}$ and add the fixed offset to calculate the threshold as shown in Equation 25. The register supports settings from 4.67mV to 1204.97mV.

5.12.4 0x2B - CBMAX Threshold

The Cell Balancing Maximum Threshold register sets the upper cell voltage threshold of the cell balancing range. Table 50 shows the format of this register.

Table 50. 0x2B CB Max Register

Bit Name	Bits	Default	$CBMAX_{step}$	Offset
CBMAX - Cell Balance Overvoltage Threshold	D[7:0]	1111 1111	18.828mV	18.791mV

The CBMAX register sets the threshold voltage for status bit 0x66.2 - 2HI2CB. After a cell voltage scan has completed, the RAA489206 compares the minimum cell voltage to the CBMAX threshold setting. If the minimum cell voltage is greater than the CBMAX value, bit 2HI2CB is set and cell balancing is blocked. Bit 2HI2CB cannot be cleared (and CB cannot restart) until the minimum measured cell voltage is below CBMAX by V_{CBHys}, which is set to 5 x $CBMAX_{step}$.

(EQ. 26) $$VThreshold = (RegVal) \cdot CBMAX_{Step} + Offset$$

Multiply the register value by the step size $CBMAX_{step}$, and add the fixed offset to calculate the threshold (Equation 26). The register supports settings from 18.791mV to 4.82V.

5.12.5 0x2C - CBMIN Threshold

The Cell Balancing Minimum Threshold register sets the lower cell voltage threshold of the cell balancing range. Table 51 shows the format of this register.

Table 51. 0x2C CB Minimum Register

Bit Name	Bits	Default	$CBMIN_{step}$	Offset
CBMIN Cell Balance Undervoltage Threshold	D[7:0]	0000 0000	18.828mV	36.774µV

The CBMIN register sets the threshold voltage for status bit 0x66.1 - 2LO2CB. After a cell voltage scan has completed, the RAA489206 compares the maximum cell voltage to the CBMIN threshold setting. If the maximum cell voltage is less than the CBMIN value, bit 2LO2CB is set and cell balancing is blocked. Bit 2LO2CB cannot be cleared (and CB cannot restart) until the maximum measured cell voltage is above CBMIN by V_{CBHys}, which is set to 5 x $CBMIN_{step}$.

(EQ. 27) $$VThreshold = (RegVal) \cdot CBMIN_{Step} + Offset$$

Multiply the register value by the step size $CBMIN_{step}$, and add the fixed offset to calculate the threshold (Equation 27). The register supports settings from 36.77µV to 4801.25mV.

5.12.6 0x2D - VEOC Threshold

The Voltage End of Charge Threshold register sets the cell voltage used to set the status bit 0x66.4 - VEOC, which in some cases ends charging by shutting off one or both power FETs. The VEOC status bit can be used by the microcontroller to signal a charger to switch from constant current to constant voltage. See Automatic Cell Balancing for the options and actions that follow VEOC. Table 52 shows the format and default value of the VEOC Threshold register.

Table 52. 0x2D VEOC Threshold Register

Bit Name	Bits	Default	$CBMAX_{step}$	Offset
VEOC - Voltage End of Charge Threshold	D[7:0]	1111 1111	18.828mV	18.791mV

The VEOC status bit can be cleared when all measured cell voltages are below the VEOC threshold and you write a 0 to it, or a 1 to the 0x02.1 - Clear Faults and Status.

(EQ. 28) $$VThreshold = (RegVal) \cdot VEOC_{Step} + Offset$$

Multiply the register value by the step size $VEOC_{Step}$ and add the fixed offset to calculate the threshold Equation 28. The register supports settings from 18.79mV to 4.82V.

This threshold comparison is not dependent on DCHRGI or CHRGI. If a cell voltage remains above the VEOC Threshold at the completion of a charge cycle in some cases it may be necessary to increase this threshold to allow turn on of DFET.

5.12.7 0x10 - IEOC Threshold

The Current End Of Charge Threshold register sets the minimum charge current by setting the threshold voltage of a digital comparator for undercurrent detection. This feature is used when bit 0x25.3 - IEOC EN is 1. The bit 0x66.5 - IEOC is set to indicate an end of charge condition when the charge current decreases to the point at which the voltage across the current sense resistor is less than this threshold setting while CFET is on. Table 53 shows the format and default value of the IEOC Threshold register.

Table 53. 0x10 IEOC Threshold Register

Bit Name	Bits	Default	$CBMAX_{step}$	Offset
IEOC - End of Charge Current Threshold	D[7:0]	0000 0000	1.345mV	5.253µV

To calculate the voltage threshold, multiply the register value by the step size $IEOC_{Step}$ and add the fixed offset as in Equation 29. Divide the voltage threshold by the sense resistor value to calculate the threshold current setting.

(EQ. 29) $$VThreshold = (RegVal) \cdot IEOC_{Step} + Offset$$

The register supports settings from 5.25µV to 342.95mV.

5.12.8 0x28, 0x29 - Cell Balancing Timers

The Cell Balancing Timer registers set the time the cell balancing circuitry is on and off. The operation of these timers is shown in Figure 94, an example of Automatic Cell Balancing as part of a System Scan or started by 0x25.4 - CB Trigger. If part of a System Scan, Return refers to the next step in the sequence as shown in Figure 94, otherwise the device waits for the next trigger.

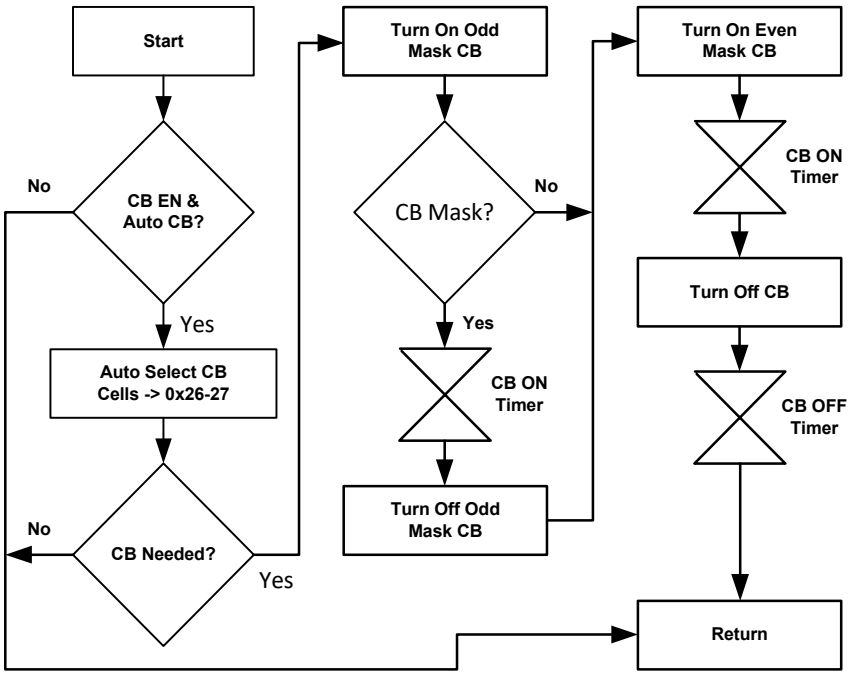


Figure 94. Simplified Auto CB Sequence

5.12.8.1 0x28 - CBON

The Cell Balancing On Timer bits and the Cell Balancing On Timer Unit bit of the CBON Timer register controls the amount of time the cells are balanced during each cycle. When the timer expires, the cell balancing circuitry is turned off. Table 54 shows the options for the CBON bits.

Table 54. 0x28 CBON Bits

CBON Timer D[7:1]	D[0]	CB ON Unit
0 to 1016	0	ms
0 to 1016	1	s
0000 0000	Default	0

The step size of the setting is 8. Multiply the unit value by the step size and the 7-bit register value to calculate the CBON time setting. The timing magnitude is set by configuring the CBON Unit bit to either seconds or ms.

5.12.8.2 0x29 - CBOFF

The Cell Balancing Off Timer bits and the Cell Balancing Off Timer Unit bit of the CBOFF Timer register controls the amount time that cell balancing is off before the timer controlled by 0x2E.2:0 - Scan Delay starts. The next continuous scan begins after the Scan Delay timer expires. If in SCAN mode following a triggered single scan, the device waits for the next trigger. Table 55 shows the options for the CBOFF bits.

Table 55. 0x29 CBOFF Bits

CBOFF Timer D[7:1]	D[0]	CBOFF Unit D[0]
0 to 1016	0	ms
0 to 1016	1	s
0000 0000	Default	0

The step size of the setting is 8. Multiply the unit value by the step size and the 7-bit register value to calculate the CBOFF time setting. The timing magnitude is set by configuring the CBOFF Unit bit to either seconds or milliseconds.

5.13 System Faults and Status

5.13.1 0x63 - Priority Fault

The Priority Fault register reports failures related to the battery pack. All bits in this register are latched high and can be cleared by writing a 0 to them, a chip $\overline{\text{RESET}}$ or by writing a 1 to the Clear Faults and Indicators bit (0x02.1). They cannot be cleared by writing a 0 while the condition that sets them HIGH is present. The bit locations in this register are shown in Table 56. The 0x83 - Priority Fault Mask can be used to mask bits within this register to prevent the fault from propagating to $\overline{\text{ALRT}}$.

Table 56. 0x63 Priority Fault Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	VCCF	OWF	IOTF	COCF	DOCF	DSCF	UVF	OVF
Default	0	0	0	0	0	0	0	0

5.13.1.1 0x63.7 - VCCF

The V_{CC} Fault bit of the Priority Fault register reports an undervoltage event at the VCC pin. The bit is set when the measured voltage is below the setting of register 0x1C - V_{VCC} Min Threshold.

In SCAN mode, setting VCCF requires three consecutive results below the minimum voltage threshold if 0x09.5 - Other Fault Delay is set to 1 and a continuous System Scan is running.

This bit shuts off both CFET and DFET and stops System Scan. If unmasked by setting bit 0x83.7 to 0, this bit also sets $\overline{\text{ALRT}}$ low.

5.13.1.2 0x63.6 - OWF

The Open-Wire Fault of the Priority Fault register ORs the open-wire faults from each cell, V_{BAT1}, VSS, xT0, and xT1 pin. A 1 indicates a failure has occurred. This bit shuts off both CFET and DFET and stops System Scan. This bit also sets $\overline{\text{ALRT}}$ low if unmasked by setting bit 0x83.6 to 0 (see 0x83 - Priority Fault Mask).

5.13.1.3 0x63.5 - IOTF

The Internal Over-Temperature Fault reports if an over-temperature fault detection by the internal temperature sensor has occurred. The bit is set if the internal temperature is above (voltage is below) the IOTF threshold (see 0x22 - 0x23 - IOTW and IOTF Thresholds).

In SCAN mode, setting IOTF requires three consecutive results below the voltage threshold (NTC Temp Sensor) if 0x09.5 - Other Fault Delay is set to 1 and a continuous System Scan is running.

This bit shuts off both CFET and DFET and stops System Scan. If unmasked by setting bit 0x83.5 to 0, this bit also sets $\overline{\text{ALRT}}$ low.

5.13.1.4 0x63.4 - COCF

The Charge Overcurrent Fault bit reports the result of the charge overcurrent comparison. If the voltage reading is above the 0x0F - COC Threshold, this bit is set to 1, otherwise the bit remains at the default of 0. If unmasked by setting mask bit 0x83.4 to 0, this bit also sets $\overline{\text{ALRT}}$ low.

In SCAN mode, setting COCF requires a number of consecutive results, set in register 0x0D.3:0 - COCD, above the overcurrent threshold while a continuous System Scan is running.

This bit shuts off CFET if the following conditions are true: the device detects charging current (I_{PACK} > 19 decimal), the CPWR bit is 1 for parallel FETs (0x0E.3 - CPWR), and the FCDC bit is 1 (0x0E.2 - FCDC).

This bit shuts off CFET and DFET and stops System Scans if the following is true; the device detects charging current (I_{PACK} > 19 decimal), CPWR bit is 0 for series FETs (0x0E.3 - CPWR) and FCDC bit is 1 (0x0E.2 - FCDC).

If FCDC is 0, a COCF does not shut off CFET or DFET but stops continuous scans.

5.13.1.5 0x63.3 - DOCF

The Discharge Overcurrent Fault bit reports the result of the discharge overcurrent comparison. If the voltage reading is below the 0x0B - DOC Threshold, this bit is set to 1. If unmasked by setting mask bit 0x83.3 to 0, this bit also sets $\overline{ALRT}$ low.

In SCAN mode, setting DOCF requires a number of consecutive results, set in register 0x0D.7:4 - DOCD, below the overcurrent threshold and a continuous System Scan is running.

This bit shuts off DFET if the following is true; the device detects discharge current (I_{PACK} < -20 decimal), CPWR bit is 1 for parallel FETs (0x0E.3 - CPWR) and CFD bit is 1 (0x0E.7 - CFD).

This bit shuts off CFET and DFET and stops System Scans if the following is true; the device detects discharge current (I_{PACK} < -20 decimal), CPWR bit is 0 for series FETs (0x0E.3 - CPWR) and CFD bit is 1 (0x0E.7 - CFD).

If the CFD bit is 0, a DOCF does not shut off either CFET or DFET but does stop continuous scan. This setting disconnects this fault detection from FET and scan control.

5.13.1.6 0x63.2 - DSCF

The Discharge Short-Circuit Fault bit reports the result of the analog discharge short-circuit comparison. If the current sense voltage is more negative than 0x0A - DSC Threshold for the time set by 0x0C - DSC Delay, the bit is set to 1.

When set, this bit shuts off both CFET and DFET and stops System Scan, and triggers a transition to IDLE mode. If unmasked by setting mask bit 0x83.2 to 0, it also sets $\overline{ALRT}$ low.

If bit 0x0E.4 - ELR is enabled when a DSCF occurs, and the load recovery function determines the load was removed, the DSCF bit is automatically cleared. See Short-Circuit Detection and Recovery. This function does not re-enable CFET or DFET.

5.13.1.7 0x63.1 - UVF

The Undervoltage Fault bit reports a fault if one or more of the cell voltages is below the undervoltage threshold (UV) set in register 0x07 (0x06 - 0x07 - V_{CELL} OV Threshold and V_{CELL} UV Threshold). A 1 indicates a UV fault.

In SCAN mode, setting UVF requires a number of consecutive results, set in register 0x09.3:0 - V_{CELL} Fault Delay, below the undervoltage threshold while a continuous System Scan is running.

See 0x24.1 - DFET EN and 0x24.0 - CFET EN for the settings that allow this fault to shut off CFET and/or DFET respectively. See Scan Will Not Start for conditions where this bit stops and prevents start of System Scans.

If unmasked by setting mask bit 0x83.1 to 0, this bit also sets $\overline{ALRT}$ low.

5.13.1.8 0x63.0 - OVF

The Overvoltage Fault bit reports a fault if one or more of the cell voltage readings is above the overvoltage threshold (OV) set in register 0x06 (0x06 - 0x07 - V_{CELL} OV Threshold and V_{CELL} UV Threshold). A 1 indicates an OV fault.

In SCAN mode, setting OVF requires a number of consecutive results, set in register 0x09.3:0 - V_{CELL} Fault Delay, above the overvoltage threshold while a continuous System Scan is running.

See 0x24.1 - DFET EN and 0x24.0 - CFET EN for the settings that allow this fault to shut off CFET and/or DFET respectively. See Scan Will Not Start for conditions where this bit stops and prevents start of System Scans.

If unmasked by setting mask bit 0x83.0 to 0, this bit also sets $\overline{ALRT}$ low.

5.13.2 0x83 - Priority Fault Mask

The Priority Fault Mask register masks the fault bits of the Priority Fault register from propagating to the $\overline{ALRT}$ pin. The default value of 1 for each bit masks the related fault. Write a 0 to the bit to allow the fault to propagate to the $\overline{ALRT}$ pin.

Table 57 displays the format and default values of the Priority Fault Mask register.

Table 57. 0x83 Priority Fault Mask Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	VCCF MASK	OWF MASK	IOTF MASK	COCF MASK	DOCF MASK	DSCF MASK	UVF MASK	OVF MASK
Default	1	1	1	1	1	1	1	1

5.13.3 0x64 - ETAUX Fault

The ETAUX Fault register reports faults relevant to the measured voltages at the xT0 and xT1 pins. All bits in this register are latched high and can be cleared by writing a 0 to them, performing a chip $\overline{RESET}$, or by writing a 1 to bit 0x02.1 - Clear Faults and Status. They cannot be cleared while the condition that sets them HIGH is present. Contents and default values of the ETAUX Fault register are displayed in Table 58. The function of these bits and polarity of the comparators is based on the assumption that an NTC thermistor voltage is the monitored input.

Bit 0x24.2 - ETA Connect must be set for ETAUX faults to shut off CFETs and DFETs per the bit setting of 0x0E.3 - CPWR. Continuous scan is halted for a threshold violation regardless of the setting of ETA Connect.

DFET and CFET are turned off and remain off under the following conditions if bit 0x0E.3 CPWR is 0:

[DCHRGI **AND** (DUT0 **OR** DUT1 **OR** DOT0 **OR** DOT1)

OR

[CHRGI **AND** (CUT0 **OR** CUT1 **OR** COT0 **OR** COT1)]

CFET is turned off and remains off under the following conditions if bit 0x0E.3 CPWR is 1:

[CHRGI **AND** (CUT0 **OR** CUT1 **OR** COT0 **OR** COT1)]

DFET is turned off and remains off under the following conditions if bit 0x0E.3 CPWR is 1:

[DCHRGI **AND** (DUT0 **OR** DUT1 **OR** DOT0 **OR** DOT1)

For a detailed description of the settings for the operation of the CFETs and DFETs see Power FET Block.

In SCAN mode, setting ETAUX Faults requires three consecutive results above/below the minimum/maximum (NTC Thermistors assumed) voltage thresholds if 0x09.4 - ETAUX Fault Delay is set to 1 while a continuous System Scan is running. See Scan Will Not Start for conditions where ETAUX faults stop and prevent start of System Scans.

These fault bits set regardless of current direction in IDLE mode if the related threshold voltage is violated.

You select whether the $\overline{ALRT}$ pin is asserted LOW when one or more of these faults are triggered by programming the corresponding mask register bit 0x84 - ETAUX Fault Mask.

Table 58. 0x64 ETAUX Fault Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	COT1	CUT1	DOT1	DUT1	COT0	CUT0	DOT0	DUT0
Default	0	0	0	0	0	0	0	0

5.13.3.1 0x64.7 - COT1

The Charge Over-Temperature Bit 1 of the ETAUX Fault register reports a fault if the xT1 voltage (0x5A-5B) is below the COT1 voltage threshold (0x18) during charge. A 1 indicates a fault.

5.13.3.2 0x64.6 - CUT1

The Charge Under-Temperature Bit 1 of the ETAUX Fault register reports a fault if the xT1 voltage (0x5A-5B) is above the CUT1 voltage threshold (0x17) during charge. A 1 indicates a fault.

5.13.3.3 0x64.5 - DOT1

The Discharge Over-Temperature Bit 1 of the ETAUX Fault register reports a fault if the xT1 voltage (0x5A-5B) is below the DOT1 voltage threshold (0x1A) during discharge. A 1 indicates a fault.

5.13.3.4 0x64.4 - DUT1

The Discharge Under-Temperature Bit 1 of the ETAUX Fault register reports a fault if the xT1 voltage (0x5A-5B) is above the DUT1 voltage threshold (0x19) during discharge. A 1 indicates a fault.

5.13.3.5 0x64.3 - COT0

The Charge Over-Temperature Bit 0 of the ETAUX Fault register reports a fault if the xT0 voltage (0x58-59) is below the COT0 voltage threshold (0x14) during charge. A 1 indicates a fault.

5.13.3.6 0x64.2 - CUT0

The Charge Under-Temperature Bit 0 of the ETAUX Fault register reports a fault if the xT0 voltage (0x58-59) is above the CUT0 voltage threshold (0x13) during charge. A 1 indicates a fault.

5.13.3.7 0x64.1 - DOT0

The Discharge Over-Temperature Bit 0 of the ETAUX Fault register reports a fault if the xT0 voltage (0x58-59) is below the DOT0 voltage threshold (0x16) during discharge. A 1 indicates a fault.

5.13.3.8 0x64.0 - DUT0

The Discharge Under-Temperature Bit 0 of the ETAUX Fault register reports a fault if the xT0 voltage (0x58-59) is above the DUT0 voltage threshold (0x15) during discharge. A 1 indicates a fault.

5.13.4 0x84 - ETAUX Fault Mask

The ETAUX Fault Mask register masks the fault bits of the ETAUX Fault register 0x64 from propagating to the $\overline{\text{ALRT}}$ pin. The default value 1 of each bit masks the related fault. Write a 0 to the bit to allow the fault to propagate to the $\overline{\text{ALRT}}$ pin.

The format and default values of the ETAUX Fault Mask register are displayed in Table 59.

Table 59. 0x84 ETAUX Fault Mask Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	COT1 MASK	CUT1 MASK	DOT1 MASK	DUT1 MASK	COT0 MASK	CUT0 MASK	DOT0 MASK	DUT0 MASK
Default	1	1	1	1	1	1	1	1

5.13.5 0x65 - Other Fault Register

The Other Fault register reports various faults and warnings. All bits in this register are latched high and can be cleared by writing a 0 to them unless the condition that sets them HIGH is present. Unless noted otherwise in the bit descriptions below, these faults are cleared by writing 1 to Clear Faults and Indicators (0x02.1 - Clear Faults and Status), Soft Reset (0x01.7 - Soft Reset), Reset To IDLE (0x01.6 - Reset to IDLE), or a hardware reset with the $\overline{\text{RESET}}$ pin. The format and default values of the Other Fault register are displayed in Table 60.

Table 60. 0x65 Other Fault Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	VBOVF	VBUVF	CPMP NRDY	OW XT1	OW XT0	OW VBAT1	OW VSS	CRCF
Default	0	0	1	0	0	0	0	0

5.13.5.1 0x65.7 - VBOVF

The V_{BAT1} Overvoltage Fault bit reports the result of the V_{BAT1} overvoltage comparison. If the V_{BAT1} voltage reading (0x5C - 0x5D - V_{BAT1} Voltage (R)) is above the 0x20 - V_{BAT1} OV Threshold, this bit is set to 1.

In SCAN mode, setting VBOVF requires a number of consecutive measured results, determined by 0x09.5 - Other Fault Delay, above the maximum voltage threshold while a continuous System Scan is running.

See 0x24.1 - DFET EN and 0x24.0 - CFET EN for the settings that allow this fault to shut off CFET and/or DFET respectively. See Scan Will Not Start for conditions where this fault stops and prevents start of System Scans.

5.13.5.2 0x65.6 - VBUVF

The V_{BAT1} Undervoltage Fault bit of the Other Fault register reports the result of the V_{BAT1} undervoltage comparison. If the V_{BAT1} voltage reading (0x5C - 0x5D - V_{BAT1} Voltage (R)) is below the 0x21 - V_{BAT1} UV Threshold, then this bit is set to 1.

In SCAN mode, setting VBUVF requires a number of consecutive measured results, determined by 0x09.5 - Other Fault Delay, below the minimum voltage threshold while a continuous System Scan is running.

See 0x24.1 - DFET EN and 0x24.0 - CFET EN for the settings that allow this fault to shut off CFET and/or DFET respectively. See Scan Will Not Start for conditions where this fault stops and prevents start of System Scans.

5.13.5.3 0x65.5 - CPMP NRDY

If the charge pump is enabled with bit 0x24.7 - CPMP EN set to 1, the Charge Pump Not Ready bit indicates the status of the voltage at the VCP pin. A 1 indicates that the charge pump is not ready for use because the voltage is substantially below its proper operating range. The power FETs do not turn on if the bit is set. The device clears the CPMP NRDY bit automatically when the charge pump voltage is in an acceptable range.

If the charge pump is disabled with bit 0x24.7 - CPMP EN set to 0, the CPMP NRDY bit is cleared (0). The CPMP NRDY fault can only be set if the charge pump is enabled and its voltage fails to rise above V_{pmpMin} or falls below $V_{pmpFall}$.

If CPMP NRDY is 1 when the charge pump is enabled (0x24.7 = 1), Cell Balancing on VC16 and continuous System Scans are inhibited and both C/DFET pins are shut off, but it does NOT clear either C/DFET_EN register bits.

5.13.5.4 0x65.4:5 - OW xT1 xT0

The Open-Wire xT1 and xT0 bits indicate if an open-wire fault has occurred on pins xT1 and/or xT0. After ETAUX pins are measured, if the voltage reading is near VTEMP, the corresponding OW status bit is set to 1.

The Open-Wire test function for pins xT1 and xT0 is not part of the open-wire test sequence. See Aux Pins Open-Wire Test for details.

5.13.5.5 0x65.2 - OW V_{BAT1}

This bit is set to 1 when the voltage at the VC16 pin is higher than the voltage at the VBAT1 pin by V_{OWth2}. Because the VBAT1 pin supplies power to various circuits within the RAA489206, an open wire leading to this pin renders the device nonfunctional during the open, which leads to a POR at reconnection. A Schottky diode connected from VC15 to VBAT1 can power the device during this fault condition. This enables the device to operate and alert the MCU to a VBAT1 open wire.

If the V_{BAT1} connection to the top cell is made through the pack high-side load current wire and is separate from the VC15 and VC16 voltage sense connections to their respective cells, an open in the high-side load current connection is detectable.

The open-wire test sequence does not test V_{BAT1} during discharge, when bit 0x67.7 - DCHRGI is 1. See Open-Wire Function for details.

5.13.5.6 0x65.1 - OW VSS

This bit is set to 1 when the voltage at the VSS pin is significantly higher than the voltage at the VC0 and/or the VC1 pins while the chip runs an open-wire sequence that includes the comparisons of VSS vs VC1 and VSS vs VC0. See the Electrical Specifications (V_{OWth3}) for the threshold voltage.

If the VSS connection to the bottom cell is made through the pack low-side load current wire and is separate from the VC0 and VC1 voltage sense connections to their respective cells, an open in the pack low-side load current connection is detectable. Because VSS is tied to CSN (and PACK-), the path from the VSS pin to the bottom of the pack includes the current sense resistor.

The open-wire test sequence does not test VSS during discharge. See Open-Wire Function for details.

5.13.5.7 0x65.0 - CRCF

The CRCF bit is set and latched by the RAA489206 if the 2-byte CRC word sent by the Master does not match the value calculated internally.

If this occurs during a write command, the RAA489206 ignores it and the register value remains unchanged. In the case of a read command from the Master with an incorrect CRC, the RAA489206 holds the MISO pin high during the SCL cycles when the read-back data is expected by the Master until CS returns high, signaling there was an error with an all 1's response.

As with the other bits in this register, this bit can be cleared by writing a 0 to it only if the condition that set the CRCF is cleared. Any valid Read or Write command can be used to clear the condition, and a valid Write command to this register can be used to clear the bit.

5.13.6 0x85 - Other Fault Mask

The Other Fault Mask register masks the fault bits of the Other Fault register 0x65 from propagating to the $\overline{ALRT}$ pin. The default value 1 of each bit masks the related fault. Write a 0 to the bit to enable the fault to propagate to the $\overline{ALRT}$ pin.

If bit 0x85.0 is set to 0, the Busy Bit (0x01.2 - Busy) is inverted and output on the $\overline{ALRT}$ pin. This prevents the MCU from reading measurement registers that may be in the process of being written by the RAA489206.

Table 61 displays the format and default values of the Other Fault Mask register.

Table 61. 0x85 Other Fault Mask Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	VBOVF Mask	VBUVF Mask	CPMP NRDY Mask	RSV	RSV	RSV	RSV	BUSY Mask
Default	1	1	1	1	1	1	1	1

5.13.7 0x66 - CB Status

The CB Status register reports cell balancing and charging related status for the RAA489206. All bits in this register are latched high unless otherwise noted and can be cleared by writing a 0 to them unless the condition that sets them HIGH is present. These bits also can be cleared by setting the Clear all Faults (0x02.1 - Clear Faults and Status) bit or executing one of the following actions: Soft Reset (0x01.7 - Soft Reset), Reset To Idle (0x01.6 - Reset to IDLE), or a hardware reset on the RESET pin.

The format and default values of the CB Status register are displayed in Table 62.

Table 62. 0x66 CB Status Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	BAT FULL	IOTW	IEOC	VEOC	DVCF	2HI2CB	2LO2CB	NEED CB
Default	0	0	0	0	0	0	0	0

5.13.7.1 0x66.7 - BAT FULL

The Battery Full bit indicates that charging and auto cell balancing (if enabled) has completed. The conditions that set BAT FULL with cell balancing enabled are summarized below and detailed in Automatic Cell Balancing.

For constant current charging with 0x25.3 - IEOC EN and 0x25.1 - CB EOC set to 0, BAT FULL sets when the highest cell voltage reaches the 0x2D - VEOC Threshold and the bit 0x66.4 - VEOC is set.

If CB EOC is 1 and IEOC EN is 0, when VEOC is set, CFET and DFET shut off. BAT FULL is set when cell balancing reduces the cell voltages below the VEOC threshold.

For charge cycles that end with constant voltage charging (CB EOC = 0 and IEOC EN = 1), BAT FULL sets after the cell voltages exceed the VEOC threshold (the VEOC bit is set and DFET shuts off) and the bit 0x66.5 - IEOC transitions from 0 to 1 because of the charge current dropping below the 0x10 - IEOC Threshold.

If CB EOC is 1 and IEOC EN is 1, when VEOC is set, DFET shuts off. BAT FULL is set when IEOC changes from 0 to 1 because of the charge current dropping below the IEOC Threshold.

Whenever BAT FULL is set high, 0x25.6 - Auto CB EN is reset to 0. The microcontroller must clear the BAT FULL bit before enabling the next cycle of automatic cell balancing (set AUTO CB EN to 1).

5.13.7.2 0x66.6 - IOTW

The Internal Over-Temperature Warning bit indicates that an internal temperature sensor over-temperature warning event occurred. The bit is set if the internal temperature is above (voltage is below) the IOTW threshold at 0x22 (0x22 - 0x23 - IOTW and IOTF Thresholds).

In SCAN mode, setting IOTW requires three consecutive results below the voltage threshold (NTC Temp Sensor) if 0x09.5 - Other Fault Delay is set to 1 while a continuous System Scan is running.

5.13.7.3 0x66.5 - IEOC

The Current End of Charge bit is set if CFET is on, the I_{PACK} voltage (0x52-53) has dropped below the setting of 0x10 - IEOC Threshold, and bit 0x25.3 - IEOC EN is set to 1. A transition from 0 to 1 of the IEOC bit indicates the charge current has dropped below the IEOC Threshold. See Automatic Cell Balancing.

The IEOC threshold voltage divided by the sense resistor value sets the IEOC current (see CSP and CSN Pins (24, 25)). The IEOC bit is not dependent on DCHRGI or CHRGI.

5.13.7.4 0x66.4 - VEOC

The Voltage End Of Charge bit indicates the result of the comparison of the 0x2D - VEOC Threshold with the maximum cell voltage. A 1 indicates that one or more of the scanned cells voltage is above the threshold. Setting the VEOC bit is not dependent on DCHRGI or CHRGI, and shuts off DFET and/or CFET in some cases, see Automatic Cell Balancing.

When VEOC is clear (0), cell balancing during charging is enabled by 0x25.0 - CB CHRG. When VEOC is set (1), cell balancing during charging is enabled by 0x25.1 - CB EOC.

5.13.7.5 0x66.3 - DVCF

The Delta V_{CELL} Max Fault bit indicates the result of the digital comparison of the 0x08 - V_{CELL} Max Delta Threshold with the 0x50 - 0x51 - V_{CELL} Max Delta Voltage (R). A 1 indicates the V_{CELL} Max Delta cell voltage has exceeded the V_{CELL} Max Delta threshold.

In SCAN mode, setting DVCF requires three consecutive results above the voltage threshold if 0x09.6 - Delta V_{CELL} Fault Delay is set to 1 while a continuous System Scan is running.

5.13.7.6 0x66.2 - 2HI2CB

The Too High To Cell Balance bit is set when the minimum of all the cell voltages is greater than 0x2B - CBMAX Threshold. This bit inhibits cell balancing when set, and must be clear along with the condition that set it before cell balancing can start. The minimum of all cell voltages has to be below CBMAX - 5bits (~94 mV hysteresis) before the RAA489206 clears this bit. Unlike the other bits in the register, 2HI2CB is not latched and clears automatically when the condition that set it clears.

5.13.7.7 0x66.1 - 2LO2CB

The Too Low To Cell Balance bit is set when the maximum of all the cell voltages is lower than 0x2C - CBMIN Threshold. This bit inhibits cell balancing when set, and must be clear along with the condition that set it before cell balancing can start. The maximum of all cell voltages has to be above CBMIN + 5bits (~94 mV hysteresis) before the RAA489206 clears this bit. Unlike the other bits in the register, 2LO2CB is not latched and clears automatically when the condition that set it clears.

5.13.7.8 0x66.0 - Need CB

The Need Cell Balancing bit of the CB Status register is set when the difference between one or more of all the measured cell voltages and the minimum of all of them is greater than the 0x2A - CB Min Delta Threshold. The comparison is evaluated as soon as a set of cell voltage measurements completes. A 1 indicates cell(s) need balancing.

If AUTO CB EN = 0, the Need CB bit is just an indicator to the user. See Figure 107.

5.13.8 0x86 - CB Status Mask

The Cell Balancing Status Mask register masks the status bits of the CB Status register (0x66) to prevent the status indicator from propagating to the $\overline{ALRT}$ pin. The default value 1 of each bit masks the related status bit. Write a 0 to the bit to enable the status to propagate to the $\overline{ALRT}$ pin.

Table 63 displays the format and default values of the CB Status Mask register.

Table 63. 0x86 CB Status Mask Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	BAT FULL MASK	IOTW MASK	IEOC MASK	VEOC MASK	DVCF MASK	2HI2CB MASK	2LO2CB MASK	NEED CB MASK
Default	1	1	1	1	1	1	1	1

5.13.9 0x67 - Status

The Status register reports the general status of the RAA489206 with monitors for load, charge and discharge. It also has regulator, reference and other fault bits. All bits in this register are latched high unless otherwise noted and can be cleared by writing a 0 to them, performing a chip $\overline{\text{RESET}}$, or by writing a 1 to the Clear Faults and Indicators bit (0x02.1). They cannot be cleared while the condition that sets them HIGH is present. Table 64 displays the format and default values of the Status register.

Table 64. 0x67 Status Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	DCHRGI	CHRGI	CH PRESI	LD PRESI	OTHER FAULTS	IREG1	IREG2	VTMPF
Default	0	0	0	0	0	0	0	0

5.13.9.1 0x67.7 - DCHRGI

The Discharge Current Indicator bit indicates if charge is being removed from the battery pack in SCAN mode. If the current sense voltage measurement is less than approximately -200µV (-20 decimal register value), the DCHRGI bit is set. This bit is not latched and indicates the current direction of the last pack current measurement. If cleared by the MCU, it remains clear until the next pack current measurement.

In continous Scan mode, setting DCHRGI requires three consecutive measurements below -200µV if 0x03.1 - I_{DIR} Delay is set to 1.

When discharging with a series power FET configuration (0x0E.3 - CPWR is set to 0), the discharge temperature limits are applied to the ETAUX pin measurements (ETAUX Detectors) in SCAN mode. If any ETAUX measurement exceeds the discharge limits and 0x24.2 - ETA Connect is enabled, both power FETs are turned OFF. For a parallel FET configuration (CPWR = 1), only DFET is shut OFF.

5.13.9.2 0x67.6 - CHRGI

The Charge Current Indicator bit indicates if charge is being supplied to the battery pack in SCAN mode. If the current sense voltage measurement is greater than approximately +200µV (+19 decimal register value), the CHRGI bit is set. This bit is not latched and indicates the current direction of the last pack current measurement. If cleared by the MCU, it remains clear until the next pack current measurement.

In continous Scan mode, setting CHRGI requires three consecutive measurements above 200µV if 0x03.1 - I_{DIR} Delay is set to 1.

When charging with a series power FET configuration (CPWR = 0), the charge temperature limits are applied to the ETAUX pin measurements (ETAUX Detectors) in SCAN mode. If any AUX measurement exceeds the charge limits and 0x24.2 - ETA Connect is enabled, both power FETs are turned OFF. For a parallel FET configuration (CPWR = 1) only the CFET is shut OFF.

5.13.9.3 0x67.5 - CH PRESI

The Charger Present bit continuously follows the state of the $\overline{\text{WAKEUP}}$ pin (inverted) and is not latched. If $\overline{\text{WAKEUP}}$ is low, the CH PRESI bit is 1. When the $\overline{\text{WAKEUP}}$ pin is high, the CH PRESI bit is 0.

5.13.9.4 0x67.4 - LD PRESI

The Load Present bit indicates that a load is connected, if the DFET is disabled. The bit is 0 when the load connection detection function is off. See Figure 83.

If a load is attached during LOW POWER mode and the Load Connection Detection function is enabled (0x0E.1 - LDLP is 1), then the device transitions to IDLE mode on the rising edge of LD PRESI. See Figure 103.

Though this bit is latched, it can be cleared by the LDLP and ELR (0x0E.4 - ELR) functions if either or both are enabled.

5.13.9.5 0x67.3 - Other Faults

The Other Faults bit of the Status register ORs the communication time out, and oscillator frequency error bits. If a serial communication transaction has not occurred in t_{COM} time while in IDLE mode, the flag is set and the device changes to LOW POWER mode. The t_{COM} timeout fault can be ignored by setting bit 0x1F.1 - Communication Timeout EN to 0. If the frequency of any of the on-chip oscillators is too high or too low, the bit is set.

5.13.9.6 0x67.2 - IREG1

The Regulator overcurrent 1 indicator reports an overcurrent event has occurred while in IDLE or SCAN Modes. The I_{REGOC1} threshold at 0x1D (0x1D,1E - $IREG_{OC1, 2}$ Threshold) is compared to the I_{REG} Voltage (0x61-62 - I_{REG} Voltage (R)) to determine this indicator. A 1 indicates a failure has occurred.

This fault shuts off both CFET and DFET and stops System Scan.

5.13.9.7 0x67.1 - IREG2

The Regulator overcurrent 2 indicator reports an overcurrent event has occurred while in LOW POWER mode. The I_{REGOC2} threshold at 0x1E (0x1D,1E - $IREG_{OC1, 2}$ Threshold) is compared to the I_{REG} Voltage (0x61-62 - I_{REG} Voltage (R)) to determine this indicator. A 1 indicates a failure has occurred.

5.13.9.8 0x67.0 - VTMPF

The VTEMP Fault bit reports an undervoltage condition of the VTEMP pin voltage. A 1 indicates a failure has occurred. It is set when the measurement of the VTEMP voltage is lower than the $VTEMP_{Min}$ voltage threshold (1.1V).

This fault shuts off both CFET and DFET and stops System Scan.

5.13.10 0x87 - Status Mask

The Status Mask register masks the bits of Status register 0x67 from asserting the $\overline{ALRT}$ pin low. The default value of each of the bits in this register is 1 (masked). Table 65 provides the definition of the Status Mask register. Write a 0 to the bit to allow signals to pass to the $\overline{ALRT}$ pin.

Table 65. 0x87 Status Mask Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Fault Masked	DCHRGI	CHRGI	CH PRESI	LD PRESI	OTHER FAULTS	IREG1	IREG2	VTMPF
Default	1	1	1	1	1	1	1	1

5.13.11 0x68-69 - Open-Wire Status

Each bit in the Open-Wire Status register corresponds to one battery cell. During an open-wire test sequence (see Open-Wire Function), the RAA489206 connects a resistor, one cell at a time, between the VCn and VCn-1 pins (n = 1:16), and measures the voltage V(VCn, VCn-1). OW Celln is set to 1 if the measured voltage is below a threshold when measuring V(VCn, VCn-1). See the Electrical Specifications (V_{OWth1}) for the threshold voltage. A bit can be set if either wire to Celln is open. An open-wire on pin VC0 is indicated with bit 0x69.0 set to 1.

To clear these fault bits, first reconnect the faulty wire(s) to the battery pack and execute an open-wire sequence. All bits in this register are latched high and can be cleared by writing a 0 to them, performing a chip $\overline{RESET}$, or by writing a 1 to the Clear Faults and Indicators bit (0x02.1). They cannot be cleared while the condition that sets them HIGH is present.

Note: Open Wire status of pins xT0, xT1, VSS, and V_{BAT1} are in the 0x65 - Other Fault Register.

Table 66. 0x68 OW Status Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	OW Cell16	OW Cell15	OW Cell14	OW Cell13	OW Cell12	OW Cell11	OW Cell10	OW Cell9
Default	0	0	0	0	0	0	0	0

Table 67. 0x69 OW Status Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Bit Name	OW Cell8	OW Cell7	OW Cell6	OW Cell5	OW Cell4	OW Cell3	OW Cell2	OW Cell1
Default	0	0	0	0	0	0	0	0

5.13.12 0x88-89 - Open-Wire Mask

The Open-Wire Mask prevents an open-wire failure on selected cell(s) from propagating to the $\overline{\text{ALRT}}$ pin and spans two 1-byte registers. Set the bits corresponding to unused cells to 1 in this register and in registers 0x04 - 0x05 - Cell Select.

If the Open-Wire Mask bit is 0 and an open-wire failure occurs on that cell, $\overline{\text{ALRT}}$ goes low to indicate a fault.

Table 68. 0x88 OW Mask Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Fault Masked	OWM Cell16	OWM Cell15	OWM Cell14	OWM Cell13	OWM Cell12	OWM Cell11	OWM Cell10	OWM Cell9
Default	1	1	1	1	1	1	1	1

Table 69. 0x89 OW Mask Register

Bits	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Fault Masked	OWM Cell8	OWM Cell7	OWM Cell6	OWM Cell5	OWM Cell4	OWM Cell3	OWM Cell2	OWM Cell1
Default	1	1	1	1	1	1	1	1

6. Pin Functionality

6.1 VCn Pins

The VC0-VC16 pins are the voltage sense inputs of the RAA489206 and are used in pairs to differentially measure each cell voltage. Positive pin VC_n and negative pin VC_{n-1} are connected to the ADC through a multiplexer. Each voltage sense input uses an external filter to protect against battery voltage transients. The basic input filter structure, with capacitors to the local ground, provides protection against transients and EMI for the cell inputs. They carry the loop currents produced by EMI and should be placed as close to the battery connector as possible. The ground terminals of the capacitors must be connected directly to a solid ground plane. Place any vias in line to the signal inputs so that the inductance of these forms a low pass filter with the grounded capacitors.

The filtered battery cell voltages internally connect to the cell voltage monitoring system. The monitoring system contains a multiplexer to select a specific input, and an analog to digital converter.

The components of the T network (see Figure 95) provide a current limit function during hot plug events. The typical application has a total of ~232Ω series isolation resistance between the VC_n inputs and the cells, with R_1 set to 50Ω and R_5 at 182Ω.

The recommended value for C_1 is 0.33µF. A short in one of these capacitors dissipates the charge in the battery cell if left uncorrected for an extended period of time. Renesas recommends that capacitors connected to cells are fail safe or open mode types.

Component values for the remaining resistors in Figure 95 are listed in the CBn Pins section.

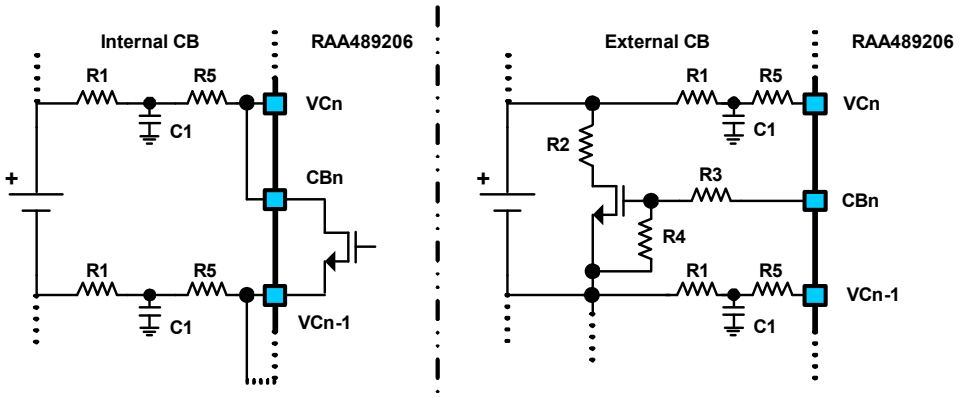


Figure 95. Voltage Sense and Cell Balance Pin Connections

See Reduced Cell Count for instructions about connecting unused VCn and CBn pins in systems with fewer than 16 cells.

6.2 CBn Pins

The CB1 - CB16 pins are the Cell Balance (CB) outputs of the RAA489206. They can be configured to use internal FETs or to drive external NMOS cell balancing FETs. The current drive for external FETs is ~25µA (I_{ECB}). The current sources are turned on and off as needed to control the external devices. The RAA489206 uses only N-channel FETs for the external balancing function.

Figure 95 shows the recommended cell balancing and voltage monitoring external component configuration. In the Internal CB configuration, the cell voltage is monitored through the cell balance resistors.

The external cell balance transistor requires two extra resistors for bias and pin protection. Set the value of R3 to 10KΩ and set R4 to 200kΩ (Figure 95). With a CB pin typical output current of 25µA, the cell balance transistor would see about 5V from gate to source.

Cell Balancing current is determined by the cell voltage divided by the resistance in the path from Cell+ through the CB FET to Cell-. The following equations assume configurations from Figure 95 and component values from VCn Pins.

For the external case, the CB current (CBI) is determined by the value of R2 and the FET on-resistance:

$$CBI = V_{CELL}/(R2 + R_{DSON})$$

For the internal case, CBI is determined by the values of R1, R5, and the FET on-resistance.

$$CBI = V_{CELL}/[2 \times (R1 + R5) + R_{CB\_ON}]$$

The internal CBI is obtained by assuming the nominal value for the internal CB FET R_{CB_ON} of 70Ω.

$$CBI = V_{CELL}/[2 \times (R1 + R5) + R_{CB\_ON}] = 4.2V/[2 \times (232\Omega) + 70\Omega] = \sim 8mA$$

Internal power dissipation of the RAA489206 increases when internal cell balancing is used (see 0x25.5 - CB Configuration and Equation 24). This must be accounted for in the system design to avoid triggering an Internal Over-Temperature Fault (0x63.5 - IOTF).

The Cell Balance pins should not be driven by an external source.

6.3 CSP and CSN Pins (24, 25)

The current monitor circuit tracks charge and discharge currents. The differential input voltage is sampled within System Scans (see 0x03.7- I_{PACK} EN) or with a trigger command (0x03.0 - I_{PACK} Trigger). Current is monitored by measuring the differential voltage across a current sense or shunt resistor connected between the CSP and CSN pin filters. This is a Low Side implementation; the Current Sense Positive (CSP) pin filter is connected to the bottom of the cell-stack (negative terminal of Cell 1) and the Current Sense Negative (CSN) pin filter is connected to PACK-, the negative load/charge terminal and system/board ground (Figure 91).

The RAA489206 compares the voltage across the sense resistor to several thresholds. The thresholds are discharge short-circuit (0x0A - DSC Threshold), discharge overcurrent (0x0B - DOC Threshold), and charge overcurrent (0x0F - COC Threshold). For short-circuit detection, an analog comparator is used instead of the sampled I_{PACK} measurement. If the measured voltage exceeds the selected limit beyond the chosen duration of time, the RAA489206 acts to protect the system (I_{PACK} Fault Detectors).

The current monitor tracks the direction of the current with digital comparators to determine if the battery is being charged or discharged (see 0x03.1 - I_{DIR} Delay and 0x67 - Status). If either condition is detected, the RAA489206 sets an appropriate flag. Discharge currents produce a negative voltage and charge currents produce a positive voltage. If the voltage drop across R_{SHUNT} is between approximately ±200µV (I_{Zero_THR}), neither charge or discharge condition is set.

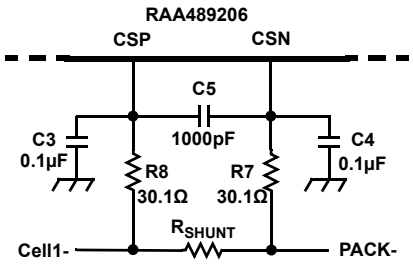


Figure 96. Current Sense Pin Connections

Recommended component values for the current monitor external circuitry are shown in Figure 96. Resistors R7 and R8 are chosen to minimize any error contributed by the pin's input current (~10µA) when the voltage is being measured. Capacitors C3 and C4 typically range from 1-100nF depending on the application.

The value of R_{SHUNT} is application specific and must be determined based on peak and nominal load currents, charge current, and end of charge current.

The maximum measurable voltage drop across R_{SHUNT} is approximately -642mV for a discharge current. During charge, the maximum measurable voltage is about 350mV. See 0x0A - DSC Threshold, 0x0B - DOC Threshold, and 0x0F - COC Threshold for current threshold settings.

While the overcurrent limits and operating maximum currents set the upper range of possible values for R_{SHUNT} the minimum value is often determined by the desired End Of Charge Current Threshold (0x10 - IEOC Threshold) and the zero current thresholds relative to the operational minimum current (I_{Zero_THR}). Current measurements are compared to the IEOC threshold when the IEOC EN bit (0x25.3 - IEOC EN) is set. The comparison determines the state of the BAT FULL bit (0x66.7 - BAT FULL). For more detail about how IEOC is used in cell balancing, see Automatic Cell Balancing.

Renesas does not recommend operating at the extreme limits of the inputs. In an application, care should be taken to guard-band against additional noise and transients that can cause current levels to reach or exceed the maximum limits. When the RAA489206 is consistently at or below threshold (I_{Zero_THR}), the device may transition to LOW POWER mode. See 0x2E.5:3 - Low Power Timer.

6.4 VSS Pin (26)

VSS is the RAA489206 analog ground pin. It must have a solid connection to the ground plane(s). The digital and analog ground planes should connect together as close to the VSS pin as possible. The Exposed Pad (EPAD) on the bottom of the RAA489206 must also be tied to analog ground. Multiple vias are recommended for good thermal conductivity.

The PACK- side of the current sense resistor must also be connected to the system and VSS ground planes (Block Diagram of Power FET Controls).

6.5 AUX0/xT0, VTEMP, AUX1/xT1 Pins (27, 29, 28)

6.5.1 External Components

AUX0/xT0 (pin 27) and AUX1/xT1 (pin 29) are auxiliary analog voltage input pins, also referred to as the ETAUX pins. Although they can be general purpose, these pins are optimized to work with external NTC thermistors to monitor the temperature of the battery pack if used in combination with the VTEMP output (Pin 28), as shown in Figure 97. When used as analog inputs, Pins 27 and 29 are called the AUX pins. When connected for temperature sense they are xT0 and xT1.

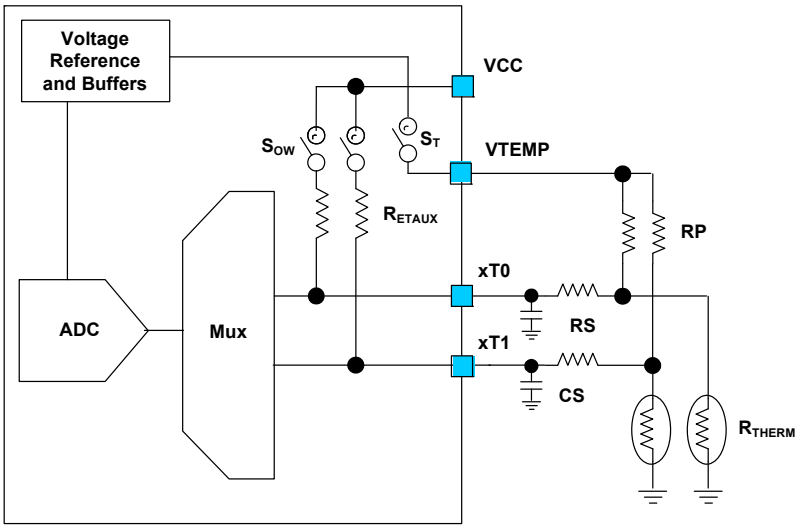


Figure 97. ETAUX Pin Configuration

The ETAUX inputs are sampled either as part of System Scans (see 0x11.7:6 - ETAUX Enable) or with a trigger command (0x11.0 - ETAUX Trigger). Before measurement, internal switch S_T is closed, connecting the two pull-up resistors RP through the VTEMP pin to the reference voltage. This sets up a pair of voltage dividers consisting of RP and R_{THERM}. The voltage between these resistors is a function of the temperature of R_{THERM}. This voltage is connected through the low pass filters consisting of RS and CS to the xT0 and xT1 inputs. Each of these inputs is measured in sequence relative to VSS. Switches S_{OW} are used only for Open-Wire test and must be open for accurate measurements.

Recommended values for the RS resistors are 10kΩ and 0.01µF for CS capacitors. RP values should match the nominal value of the thermistors used, with 10k and 100k supported. Thermistors R_{THERM} are usually located within the battery pack to monitor the cell temperature(s). Because the thermistors have a known value versus

temperature the temperature can be calculated based on the voltage divider created between R_{THERM} and RP given the known values for VTEMP and RP.

The VTEMP pin is the switched output of an analog buffer that forces the reference voltage at the pin when selected. This pin operates as an analog output and should not be driven by an external source.

6.5.2 Aux Pins Open-Wire Test

The auxiliary pins (xT0, xT1) are tested for opens indirectly and are not part of the open-wire test sequence. After the pin voltages are measured, either during system-scan or a stand-alone measurement, if their resulting voltage readings are high relative to VTEMP, the corresponding OW status bit is set high.

To test for or verify an OW on xT0 or xT1, connect the internal R_{ETAUX} pull-up resistors by setting bit 0x09.7 - AUX/xTn Pull-Up to 1. This bit closes switches S_{OW} as shown in Figure 97 when set to 1. Next, trigger an auxiliary pin measurement with 0x11.0 - ETAUX Trigger. The voltage reads full scale if the connection at the pin is open with the R_{ETAUX} resistors connected between the VCC pin and the auxiliary pins.

After the open-wire test of these pins, disconnect the internal pull-up resistors by setting the AUX Pull-up bit back to 0.

6.6 Regulator and Supply Pins (30-33)

The RAA489206 has an internal regulator that uses an external power transistor to provide regulated voltages for its internal circuits. The output of this regulator can also power other system circuitry, including the microcontroller. See Figure 98 while reviewing sections VCC Pin (30) through BASE Pin (33).

The EMITTER and VDD pins are connected through a multiplexer to the ADC, enabling the RAA489206 to monitor the regulator load current. The maximum voltage permitted across RSH is 344mV (0x1D,1E - $IREG_{OC1, 2}$ Threshold), this limits the selection of the sense resistor RSH.

These pins are to be connected per Figure 98 and should not be driven from external sources.

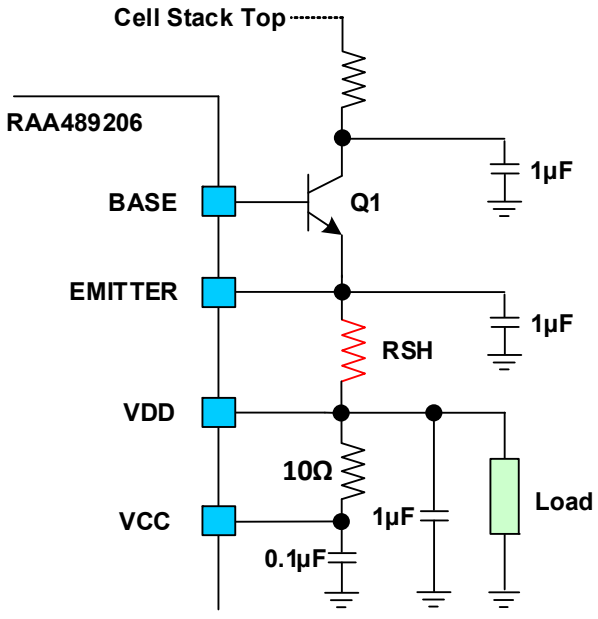


Figure 98. External Power Supply Components

6.6.1 VCC Pin (30)

The VCC pin is the analog 3.3V power supply input. External loads should not be tied to this pin. It connects externally to the VDD pin through a resistor and has a decoupling capacitor to VSS (analog ground). The VCC pin is also a sense input to the internal multiplexer and ADC that determines if the regulator is functioning properly.

6.6.2 VDD Pin (31)

The VDD pin is the digital 3.3V power supply input. It connects externally to the VCC pin through a resistor and has a decoupling capacitor to DGND (digital ground). This pin also connects to an off-chip sense resistor (RSH) tied to the EMITTER pin in the feedback loop of the regulator. The VDD and EMITTER pins are sense inputs to the internal multiplexer and ADC; together they are used to monitor the voltage across the off-chip sense resistor to determine the regulator current (see 0x61-62 - I_{REG} Voltage (R)). The VDD pin is also the feedback point for the regulator.

This node can support external loads, the regulator is designed to source but not sink current. The source current is limited by the available base current, the power dissipation tolerance of RSH, Q1 and its collector resistor.

6.6.3 EMITTER Pin (32)

The EMITTER pin connects to an off-chip sense resistor and the emitter terminal of the off-chip NPN in the regulator's loop. The other end of the sense resistor connects to the VDD pin.

6.6.4 BASE Pin (33)

The BASE Pin drives the base terminal of the external NPN transistor in the loop of the regulator. The amplifier driving the BASE pin sources a minimum of 1mA across the operating temperature range. This allows a maximum regulation current of around 100mA given a minimum NPN β of 100.

Use this pin only to drive the base pin of an external NPN as part of the regulator loop. It is not intended for any other purpose.

The NPN collector connection to the pack voltage should be routed separately to the battery pack from the high current load path to minimize any transient effects. Place a resistor between the collector and the pack along with a decoupling capacitor from collector to DGND. The value of the resistor is dependent on the expected collector current and the transistor chosen.

6.7 CMS0 Pin (34)

The CMS0 pin selects the communication protocol for the RAA489206 (see Serial Protocol Defined). CMS0 must be connected to DGND or VDD when power is applied.

6.8 DGND Pins (35,36)

DGND is the digital ground reference pin of the RAA489206. It must have a solid connection to the digital ground plane. If separate digital and analog ground planes are used, they should be connected together at the VSS pin.

6.9 V2P5 Pin (37)

The V2P5 pin is the internal 2.5V digital power supply. External connections must be limited to a decoupling capacitor to DGND. This pin is for internal use only. Do not load or drive this pin from an external source.

6.10 $\overline{\text{RESET}}$ Pin (38)

The $\overline{\text{RESET}}$ pin requires a pull-up resistor connected to V_{DD}, 100kΩ recommended. The pin is used to exit out of any mode and restores the factory default settings. The reset pin is referenced to the DGND pin.

When $\overline{\text{RESET}}$ is low, all the flip-flops return to the default state, all chip functions are disabled, and all bits are reset to default values. After $\overline{\text{RESET}}$ transitions from low to high, the fuses are read and internal calibration is performed. The chip has a communication lockout of t_{RESET} and POR lockout of $t_{StartUp}$. The whole power-up sequence takes the amount of time specified by $t_{StartUp}$. After all actions are complete, the device transitions to IDLE mode.

If V_{BAT1} voltage goes below V_{POR}, the actions by the chip are the same as if holding $\overline{\text{RESET}}$ pin low. When V_{BAT1} rises above V_{POR}, the action is equal to $\overline{\text{RESET}}$ transitioning from low to high.

6.11 $\overline{\text{WAKEUP}}$ Pin (39)

The $\overline{\text{WAKEUP}}$ pin is a digital input pin driven by the microcontroller to inform the RAA489206 that a charger is present. CH PRESI bit tracks the setting of this pin. The RAA489206 transitions to IDLE mode when $\overline{\text{WAKEUP}}$ transitions from a high to low if in SHIP or LOW POWER mode. The mode remains unchanged if in SCAN mode.

A 100kΩ pull-up to VDD is recommended.

6.12 $\overline{\text{ALRT}}$ Pin (40)

The $\overline{\text{ALRT}}$ pin is an active low digital output pin the RAA489206 uses to inform the microcontroller of a fault or status change. Faults, status bits, and mode transitions because of activity such as load attachment or inactivity such as no charge/discharge current can be unmasked (registers 0x83-89) to connect the bit state to the pin. A 100kΩ pull-up to VDD is recommended.

Unmasked incidences causing transitions to either SHIP or LOW POWER Modes hold the $\overline{\text{ALRT}}$ pin low for a minimum of time specified by t_{REGSW} before releasing it to conserve power.

The $\overline{\text{ALRT}}$ Pulse Enable bit of the GPIO Operation register (0x12.6 - ALRT Pulse EN) drives the $\overline{\text{ALRT}}$ pin in a more power efficient manner when set to 1 (see Figure 99). When the bit is enabled, the RAA489206 turns on the $\overline{\text{ALRT}}$ pin NMOS device for 2ms within a 10ms period if an alert is active. A 0 (Default) sets the circuit to constant drive.

The $\overline{\text{ALRT}}$ pin is configured as a digital output pin and should not be driven by an external source.

6.13 ADDR/$\overline{\text{CS}}$ Pin (41)

The ADDR/$\overline{\text{CS}}$ pin is used by both I^2C and SPI communications protocols. If I^2C is selected, this pin is designated ADDR and it determines the device address. See I^2C Address Values for details. When used as an address pin, it should be permanently tied to either VDD or DGND depending on desired address. The ADDR pin should not change state while the RAA489206 is powered, if it does a device RESET may be required to recover.

If the SPI protocol is selected, Pin 41 is designated as $\overline{\text{CS}}$ (Chip Select) and is active low. This pin is a digital input and is driven only by the master. A 100kΩ pull-up to VDD is recommended.

6.14 SCL Pin (42)

The SCL pin is the communications clock pin driven by the master for I^2C and SPI communications protocols. A pull-up of 4.7-10kΩ to VDD is recommended.

6.15 MOSI Pin (43)

The Master Output Slave Input pin is a digital input for the SPI protocol. The MOSI pin is driven only by the master and is monitored by the slave when $\overline{\text{CS}}$ is pulled low. No pull-up is required by the RAA489206, but it may be needed depending on the master.

This pin is not used for I^2C communications.

6.16 MISO/SDA Pin (44)

The MISO/SDA pin is used by all communications formats as determined by the CMS0 pin.

For I^2C communications the pin is the Serial Data (SDA) input/output pin. It is driven by the master for sending a slave address byte and for write commands. The pin is driven by the slave for data reads. In this mode, the device pin is an open drain. For this protocol a 4.7-10kΩ pull-up to VDD is recommended.

In SPI mode the Master Input Slave Output (MISO) pin is a CMOS serial data output pin from the slave to the master. No pull-up is necessary on this pin for SPI mode.

When operating as a digital output this pin should not be driven by an external source.

6.17 GPIO(0-3) Pin (45-48)

The General Purpose Input/Output pins are user configurable (see 0x12.5:4 - GPIO CONFIG) as a group as inputs or outputs. They cannot be configured individually.

If configured as inputs, the GPIO pins set the bit values of the GPIO Status bits. If configured as Outputs or Drive LED, the GPIO pins reflect the bit values of the GPIO Status bits. In Drive LED mode, the active outputs are pulled low for 2ms out of every 10ms to save power, as illustrated by Figure 99. These pins require pull-up resistors when configured as outputs. The pull-up resistor value for the pin should be greater than R_{GPIO_PU}.

The FETs Out selection connects GPIO2 to the DFET logic signal and GPIO3 to the CFET logic signal. This enables the RAA489206 to control a low-side FET configuration. Table 27 defines the logic state of the GPIO pins versus DFET and CFET state. GPIO1 is configured as a FETS OFF digital input pin. If the logic state is high, both DFET and CFET turn off. If the logic state is low, the DFET and CFET logic signals pass to GPIO2 and GPIO3. GPIO0 is configured as a FETs ON digital output pin. The output of the pin is high until CFET and DFET are both off.

The GPIO pins can tolerate up to 5V inputs when the RAA489206 is operated with VCC and VDD of 3.3V. If configured as digital outputs, these pins must not be driven by an external source.

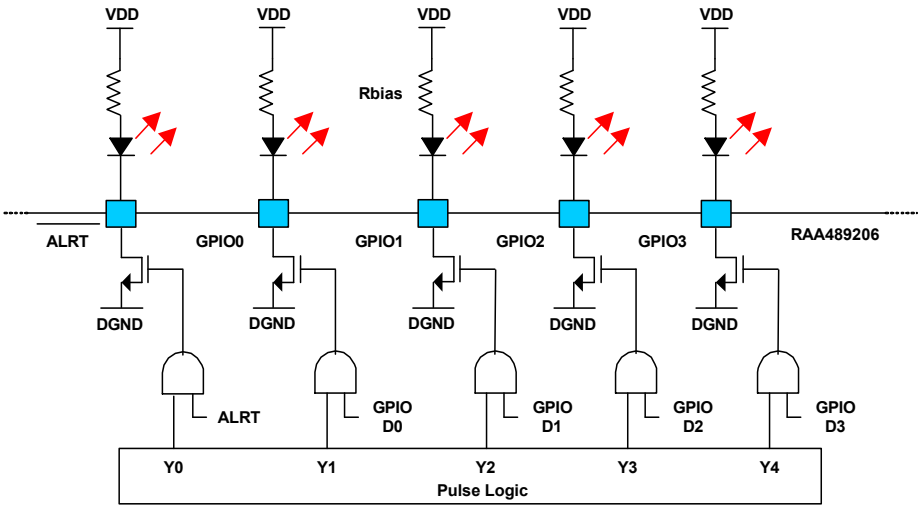


Figure 99. $\overline{\text{ALRT}}$ Pulse EN and GPIOx Drive LEDs

6.18 LDMON Pin (49)

The LDMON pin of the RAA489206 is used for load connection detection (Figure 83) and for short-circuit load release detection (Figure 81). The RAA489206 monitors the voltage at this pin, which is connected to the load side of the DFET through an isolation resistor (Figure 100). A Schottky diode (not pictured) may be added to protect the LDMON pin from excessive transients in high current applications, the diode must be oriented to enable current flow out of the LDMON pin.

The load detect function only operates when DFET is off. It connects an on-chip pull-up resistor, determined by the 0x0E.6:5 - ELD setting, between the LDMON and VBAT2 pins. If PACK+ has no load, the LDMON pin voltage is pulled above the load detect threshold V_{LDThr} (1.2V nominal). When a load is present, the LDMON voltage is determined by the voltage division between the internal resistance selected by ELD and the load connected between PACK+ and PACK-.

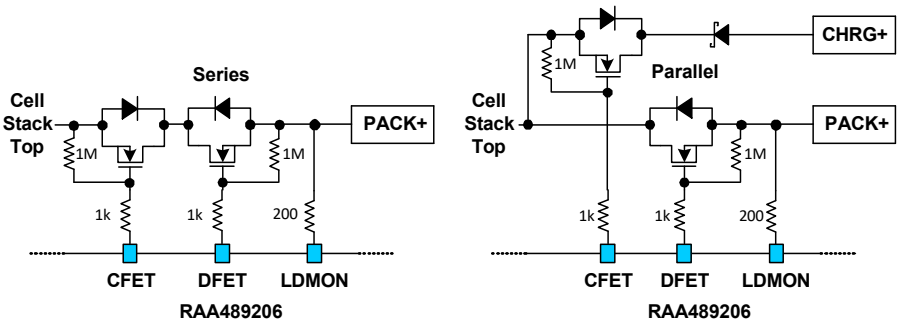


Figure 100. CFET, DFET and LDMON Connections

Setting bit 0x0E.4 - ELR to 1 (default) enables the Short Circuit Recovery Sequence. If a short-circuit is detected, the load recovery circuitry tests for load removal after a delay of t_{LDEN} plus $t_{LDDELAY}$ (0x1B.3:2 - LD Delay) following the shut off of DFET. If the ELR bit is set to 0, no Short Circuit Recovery Sequence is performed. In either case the DFET remains off until the MCU resolves the issue and enables it.

See Load Detection for more details.

6.19 CFET and DFET Pins (50, 51)

The CFET and DFET pins are driven above pin VBAT2 by the charge pump when enabled, which turns on the power FETs. These two pins are analog outputs and should not be driven by an external source. The power FETs can be arranged in either series or parallel configuration, see 0x0E.3 - CPWR.

Various conditions control the on and off state of these pins. The first group of conditions always applies. They turn off and keep off CFET and DFET and they stop and prevent starting System Scans:

- **Chip Reset:** POR, RESET Pin (38) is pulled low, set 0x01.7 - Soft Reset, or set 0x01.6 - Reset to IDLE.
- **System Mode:** SHIP or LOW POWER.
- **Asserted Fault(s):** 0x63.2 - DSCF **OR** 0x63.5 - IOTF **OR** 0x63.6 - OWF **OR** 0x63.7 - VCCF **OR** 0x65.5 - CPMP NRDY **OR** 0x67.2 - IREG1 **OR** 0x67.0 - VTMPF.

In SCAN mode, the following group of conditions applies when 0x0E.3 - CPWR bit is set to 0 for series connected power FETS. They turn off and keep off CFET and DFET, and inhibit System Scans when they are set to 1:

```
If 0x67.6 - CHRGI AND 0x0E.2 - FCDC AND 0x63.4 - COCF
If 0x67.7 - DCHRGI AND 0x0E.7 - CFD AND 0x63.3 - DOCF
If 0x24.3 - VBAT1 CON AND {[CHRGI AND VBOVF] OR [DCHRGI AND VBUVF]}
If 0x24.2 - ETA Connect AND
{(DCHRGI AND [DUT1 OR DUT0 OR DOT1 OR DOT0])
OR
(CHRGI AND [CUT1 OR CUT0 OR COT1 OR COT0])}
If 0x24.4 - CELL CON AND
{DVCF OR [{CHRGI AND NOT(CHRWUV)} OR DCHRGI] AND UVF
OR
[{DCHRGI AND NOT(DCHRWOV)} OR CHRGI] AND OVF}
```

See DFET Pin (50) and CFET Pin (51) for the cases of when CPWR is set to 1 for parallel power FET applications. See Figure 101 for the shutdown sequence for these pins.

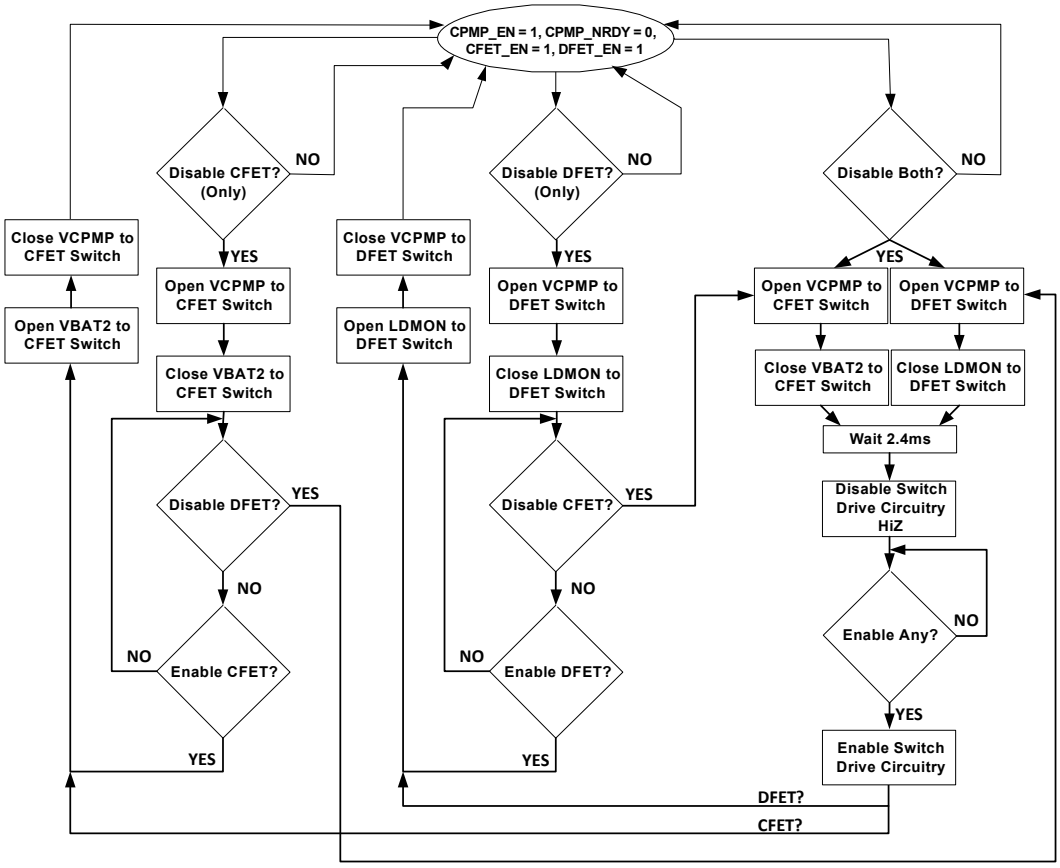


Figure 101. C/DFET Shutdown Flowchart

6.19.1 DFET Pin (50)

The DFET pin is the voltage driver output designed to pull the discharge FET gate to about 11V above the pack voltage to turn the device on to supply power to the load. A 1kΩ isolation resistor is recommended between this pin and the DFET gate (Figure 100). Use back-to-back gate-to-source Zener diodes (not pictured) to limit the FET gate-to-source voltage and transient induced currents at the DFET pin. Connect a large value resistor (~1MΩ) between the gate and source of the DFET. The resistor prevents the FET from turning on while in SHIP or LOW POWER mode, or when both power FETs are off.

When both power FETs are being shut off, an internal switch that connects the DFET pin to the LDMON pin is closed for 2.4ms to discharge the gate to source capacitance to shut off the discharge FET. Next, the DFET pin is set to high impedance. If only DFET is shut off, then the switch remains closed.

If the CPWR bit is set to 1 for parallel connected power FETS (separate charge and discharge paths) and any of the following conditions evaluate as True in SCAN mode, they cause only DFET to shut off and prevent turning it on.

```
If 0x25.3 - IEOC EN AND 0x66.4 - VEOC
If 0x0E.7 - CFD AND 0x67.7 - DCHRGI AND 0x63.3 - DOCF
If 0x24.3 - VBAT1 CON AND DCHRGI AND 0x65.6 - VBUVF
If 0x24.4 - CELL CON AND {DVCF OR UVF OR [NOT(DCHRWOV) AND OVF]}
If 0x24.2 - ETA Connect AND (DCHRGI AND [DUT1 OR DUT0 OR DOT1 OR DOT0])
```

6.19.2 CFET Pin (51)

The CFET pin is the voltage driver output designed to pull the charge FET gate to about 11V above the pack voltage to turn the device on to supply power to the battery pack. A 1kΩ isolation resistor is recommended between this pin and the CFET gate (Figure 100). Use back-to-back gate-to-source Zener diodes (not pictured) to

limit the FET gate to source voltage and transient induced currents at the CFET pin. Connect a large value resistor (~1MΩ) between the gate and source of the CFET. The resistor prevents the FET from turning on while in SHIP or LOW POWER mode, or when both power FETs are off.

When both power FETs are being shut off, an internal switch that connects the CFET pin to the VBAT2 pin is closed for 2.4ms to discharge the gate-to-source capacitance to shut off the charge FET. Next, the CFET pin is set to high impedance. If only CFET is shut off, the switch remains closed.

If CPWR bit is set to 1 for parallel connected power FETS (separate charge and discharge paths) and any of the following conditions evaluate as True in SCAN mode, they cause only CFET to shut off.

```
If 0x0E.2 - FCDC AND 0x67.6 - CHRGI AND 0x63.4 - COCF
If 0x24.3 - VBAT1 CON AND [CHRGI AND VBOVF]
If 0x24.4 - CELL CON AND {DVCF OR OVF OR [NOT(CHRWUV) AND UVF]}
If 0x24.2 - ETA Connect AND (CHRGI AND [CUT1 OR CUT0 OR COT1 OR COT0])
```

The following condition shuts off CFET in SCAN mode in association with the completion of battery charging and is not a function of the CPWR bit:

```
{(VEOC AND NOT[IEOC EN]) OR (VEOC AND IEOC AND IEOC EN)}
```

6.20 VCP Pin (52)

The VCP pin is the charge pump output connection to the charge pump capacitor, which is connected between the VCP pin and VBAT2 pin. A charge pump capacitor value of approximately 20 times the sum of the gate capacitance of the CFET and DFET is recommended. The capacitor should be placed close to the RAA489206 pins as shown in Figure 102.

The VCP pin is an analog output and should not be driven by an external source.

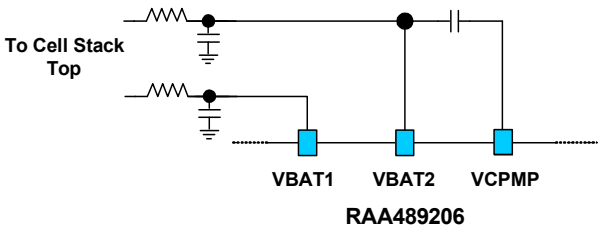


Figure 102. VBAT1, VBAT2 and VCP Connections

The charge pump is enabled with bit 0x24.7 - CPMP EN and its status is indicated by bit 0x65.5 - CPMP NRDY. See Charge Pump for a detailed description of the charge pump state machine.

6.21 VBAT2 Pin (53)

VBAT2 is a battery power input to the RAA489206. It provides power to the internal charge pump, gate drivers, load monitor, and cell balancing. This pin is connected internally to the CFET pin when CFET is OFF.

A filter consisting of a 200Ω resistor along with a 1.0µF capacitor to DGND is recommended between this pin and the top of the cell stack as shown in Figure 102. The low side of the charge pump capacitor also connects to this pin. These capacitors should be placed close to the RAA489206 pins.

Route the connection to the cell stack to the battery pack separately from the high current load path to minimize any transient effects.

6.22 VBAT1 Pin (54)

VBAT1 is a battery power input to the RAA489206. It provides power to the regulators, reference, and the V_{CELL} multiplexer. Strong or Weak regulators drive the VDD pin depending on the RAA489206 operating mode. For more information, see Regulator Measurements and Detectors.

The V_{PACK} voltage is measured at the VBAT1 pin by way of a resistor divider. The total resistance for the VBAT1 resistor divider is R_{VBAT1}.

A filter consisting of a 200Ω resistor along with a 1.0µF capacitor to DGND is recommended between this pin and the top of the cell stack as shown in Figure 102. Place the capacitor close to the VBAT1 pin.

Route the connection to the cell stack to the battery pack separately from the high current load path to minimize any transient effects.

7. System Operation

The RAA489206 is an integral part of a Battery Management System (BMS) providing a variety of operational modes and functions useful in a wide range of applications.

Figure 103 is a flow diagram that illustrates the top level interactions between modes. Additional flow diagrams tie all the individual sections together.

7.1 0x2E Scan Operation

The Scan Operation register must be set before triggering a single or continuous System Scan.

Table 70. 0x2E Scan Operation

Bits	D[7:6]	D[5:3]	D[2:0]
Bit Name	System Mode	Low Power Timer	Scan Delay
Default	00	01 1	011

7.1.1 0x2E.7:6 - System Mode

The System mode bits force the RAA489206 into a specific mode. If a scan or an open-wire test is executing, the mode change waits until they complete before transitioning to the new mode. Cell balancing is interrupted (stopped) by a mode change instruction without a delay.

Table 71. SM Mode

D[7:6	SM Mode
00	IDLE mode
01	SCAN mode
10	LOW POWER mode
11	SHIP mode

Select SCAN mode after all relevant settings have been written. Some changes may be ignored by the RAA489206 if made during an active System Scan.

7.1.2 0x2E.5:3 - Low Power Timer

The Low Power Timer bits control the number of consecutive System Scans with a zero current reading (between ±200µV, +19, and -20 decimal register value) that causes the RAA489206 to transition from SCAN mode to LOW

POWER mode. The format and default values of the Low Power Timer bits are displayed in Table 72. These bits must be set before triggering a single or continuous System Scan.

Table 72. Low Power Timer

Delay: D[5:3]			Number of Scans
0	0	0	OFF
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	4096
1	0	1	8192
1	1	0	16384
1	1	1	32768

7.1.3 0x2E.2:0 - Scan Delay

The Scan Delay bits of the Scan Operation register control the delay time between finishing a System Scan measurement/test/cell balancing sequence in continuous scan mode and starting a new one. After a System Scan has completed all measurements, tests, and cell balancing, a delay set by the Scan Delay bits occurs before starting the next System Scan. These bits have no effect when a single System Scan is triggered. The format and default values of the Scan Delay bits are displayed in Table 73. These bits must be set before triggering a continuous System Scan.

Table 73. Scan Delay

Delay: D[2:0]			Delay (ms)
0	0	0	0
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	2048
1	1	1	4096

7.2 System Modes

Reset has the highest priority and is initiated by either a $\overline{\text{RESET}}$ assertion, a V_{BAT1} voltage lower than V_{POR} (a POR event), a Reset to Idle (0x01.6 - Reset to IDLE), or a Soft Reset (0x01.7 - Soft Reset). The Reset function interrupts any action the RAA489206 is performing.

The second priority is a Discharge Short-Circuit fault (0x63.2 - DSCF). It interrupts any action the device is performing. DFET and CFET automatically turn off and short-circuit recovery begins if the bit 0x0E.4 - ELR is 1. The device transitions to IDLE mode if it is in a different mode.

After power-up, the default mode is IDLE. An MCU command can change the mode of the IC from the current mode to the desired mode (SM mode bits 0x2E.7:6 - System Mode). If a measurement or Open-Wire test is executing, the mode change happens when those complete. Cell balancing is interrupted (stopped) by a mode change without a delay.

If a command is not received by the RAA489206 for t_{COM} while in IDLE mode, the device transitions to LOW POWER mode unless bit 0x1F.1 - Communication Timeout EN is 0.

A $\overline{\text{WAKEUP}}$ assertion forces the mode to change to IDLE if in LOW POWER or SHIP mode. It does not force a mode change if in SCAN mode.

If in SCAN mode without a load or charge current ($|I_{PACK}| < I_{Zero\_THR}$) for a number of System Scans set by 0x2E.5:3 - Low Power Timer, the device transitions to LOW POWER mode.

SCAN mode exits to IDLE mode for short circuit or low VCC faults.

If in LOW POWER mode and a load is detected with bit 0x0E.1 - LDLP set to 1, the mode changes to IDLE mode.

Bad Clock (Oscillator) and Power Faults (VDD/VCC, or V2P5 regulators) cause a transition to SHIP mode.

Figure 103 illustrates the mode changes initiated by the RAA489206 or by the Master.

The various system modes are described in more detail in SHIP Mode, LOW POWER Mode, IDLE Mode, and SCAN Mode.

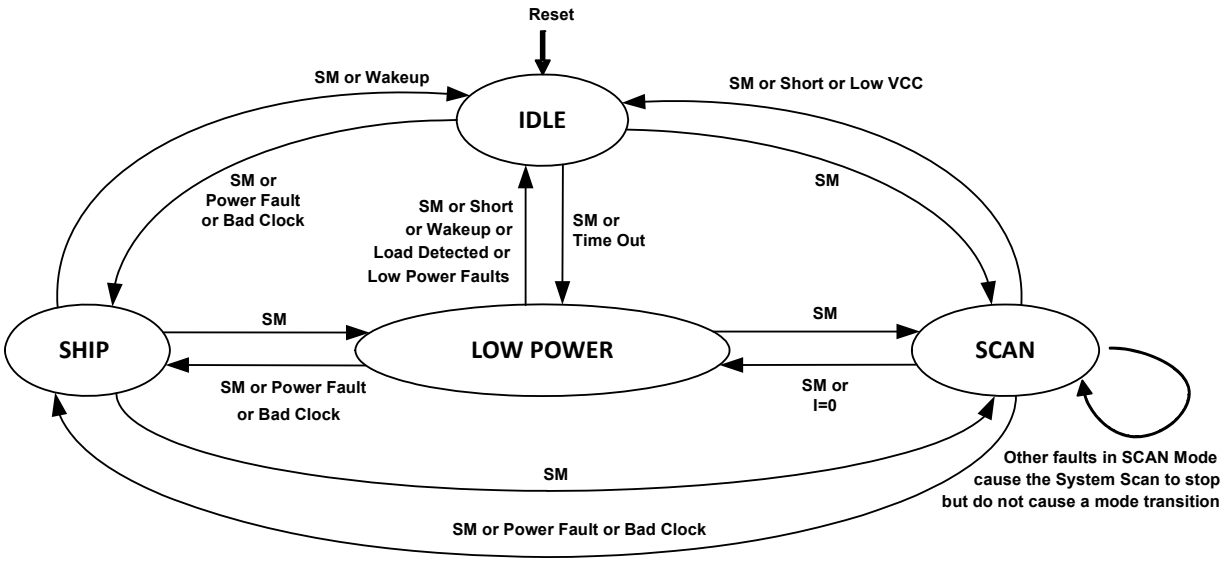


Figure 103. Top Level Flow Diagram of the RAA489206

7.2.1 SHIP Mode

SHIP mode is the lowest power mode of the RAA489206. It is entered by changing the SM mode bits (0x2E.7:6 - System Mode) to SHIP mode. If a fault is detected in the internal clock, VDD/VCC, or V2P5 regulators, the device changes to SHIP mode immediately. These faults take priority and anything in progress is interrupted immediately and is not completed. If $\overline{\text{ALRT}}$ is asserted by these faults, it is released following the transition to SHIP mode (by the t_{REGSW} timer) to save power.

The Busy bit (0x01.2 - Busy) is set during the transition to SHIP mode. All functional blocks are powered down except the Strong regulator (see 0x1B.1 - LP REG) and timer. First CFET and DFET, cell balancing, open-wire checks, and any measurements are shut off. Those functions remain disabled in SHIP mode. The t_{REGSW} timer is started to allow time for the MCU to transition to a low-power state. When the timer expires, the oscillator is turned off along with the power-good comparators, FET drivers and the charge pump. The Strong regulator is shut off if the LP REG bit is 0. The Busy bit is cleared. The regulator function is switched to the Weak regulator unless the LP REG bit is 1, which enables the Strong regulator during LOW POWER and SHIP Modes.

While in SHIP mode the IC does nothing but wait for a $\overline{\text{WAKEUP}}$ or a $\overline{\text{RESET}}$ assertion or a change mode command. All reads or writes that do not access the Scan Operation register (0x2E Scan Operation) return a NACK.

When $\overline{\text{WAKEUP}}$ or $\overline{\text{RESET}}$ are asserted or a change mode command is received, circuitry is enabled in a specific sequence:

Set Busy Bit → Oscillators → Strong Regulator → Power-Good comparators (VDD, VCC, V2P5) → Oscillator Fault Monitor → Power-Good State Machine → Wait a few milliseconds for Power-Good → Read Fuse Bits (if $\overline{\text{RESET}}$) → Cal ADC Single Ended Path → Charge Pump (if enabled).

The rest of the pack settings are restored and all faults and indicators are cleared.

If the Power-Good state machine determines that the power is not good while loading register defaults during initialization after a power-up or $\overline{\text{RESET}}$ event, the device completes loading and then transitions to SHIP mode. If the power-good state machine determines that the power is not good at any other time, the device immediately transitions to SHIP mode.

The Busy bit is cleared when the mode transition completes. From $\overline{\text{RESET}}$ rising edge or from V_{POR}, it takes about $t_{StartUp}$ (<20ms) typically to complete the transition to IDLE.

7.2.2 LOW POWER Mode

LOW POWER mode includes some measurements and enables timers. This mode is entered manually by changing the System mode bits (0x2E.7:6 - System Mode) or automatically by consecutive current readings below I_{Zero_THR} during continuous System Scans (0x2E.5:3 - Low Power Timer), or no communication from the MCU for t_{COM} while in IDLE mode unless bit 0x1F.1 - Communication Timeout EN is clear.

The Busy bit (0x01.2 - Busy) is set during the transition to LOW POWER mode. All functional blocks are powered down except the Strong regulator and the t_{REGSW} timer which is started. After the timer expires, power switches to the Weak regulator only if bit 0x1B.1 - LP REG is 0. The oscillator remains on so the 0x54 - 0x57 - I_{PACK} Timer (R) is operational. The Busy bit is cleared.

While in LOW POWER mode, every t_{LPMEAS} period relevant circuitry (including the Strong regulator) is powered up to measure V_{VCC}, I_{REG}, VTEMP, ETAUX, and V_{BAT1}. $IREG_{OC2}$ is the I_{REG} overcurrent limit in LOW POWER mode.

All control registers can be written to and read from while in LOW POWER mode. The measurement registers are not updated but the measurement results are compared to limits. After measurements complete, if an unmasked fault is detected and $\overline{\text{ALRT}}$ is asserted, the regulator remains on. Fault delay counters are not active in LOW POWER mode; single threshold violations trigger faults. A Fault causes the part to change to IDLE mode if $\overline{\text{ALRT}}$ is asserted. Status $\overline{\text{ALRT}}$ assertions from the unmasking of Busy and/or CPMP NRDY bits do not cause a transition to IDLE mode. When the device exits LOW POWER mode, the last measurement values are passed to the measurement registers before entering IDLE or SCAN mode.

When $\overline{\text{WAKEUP}}$ or $\overline{\text{RESET}}$ are asserted, a load connection is detected, or a change mode command is received, the strong regulator is powered up and the Busy bit is set. If bit 0x24.7 - CPMP EN is set, the charge pump circuitry starts. The rest of the pack settings are restored and all faults and indicators are cleared. The Busy bit is cleared when the IC completes the transition to IDLE mode.

Load Connection Detection in LOW POWER mode requires bit 0x0E.1 - LDLP to be set to 1 and 0x24.1 - DFET EN to be clear (0). Load detection is described further in 0x0E.6:5 - ELD, LDMON Pin (49), and Load Detection.

Note: If a fault is detected, the strong regulator remains on to allow the $\overline{\text{ALRT}}$ pin to be driven. The measurement registers are not refreshed until the mode is changed to SCAN or IDLE.

7.2.3 IDLE Mode

IDLE mode is entered by changing the SM mode bits (0x2E.7:6 - System Mode) to IDLE mode or asserting $\overline{\text{RESET}}$. A load detection changes the mode to IDLE if in LOW POWER mode and bit 0x0E.1 - LDLP is enabled. If in SCAN mode and a DSCF or VCCF fault is detected, the mode changes to IDLE. Asserting the $\overline{\text{WAKEUP}}$ pin in LOW POWER or SHIP mode also causes the mode to transition to IDLE.

Delay counters are disabled in IDLE mode. For example, a V_{BAT1} overvoltage reading would be passed to the VBOVF bit (0x65.7 - VBOVF) without requiring consecutive faulty readings.

Zero current can be read indefinitely in this mode. The Low Power Timer (0x2E.5:3 - Low Power Timer) is disabled in IDLE mode.

Commands from the MCU are executed while in IDLE mode.

No communication from the MCU for t_{COM} leads to a transition to the LOW POWER mode unless bit 0x1F.1 - Communication Timeout EN is 0.

Current direction indicator bits (0x67.7 - DCHRGI and 0x67.6 - CHRGI) are disabled in IDLE mode. Fault reaction is therefore limited and does not disable the power FETs. All external thermistor fault thresholds (ETAUX Detectors) are applied regardless of current direction.

7.2.4 SCAN Mode

SCAN mode is entered by changing the SM mode bits (0x2E.7:6 - System Mode) to SCAN mode. All delay counters are cleared when entering SCAN mode.

Faults DSCF, IOTF, OWF, VCCF, CPMP NRDY, IREG1, and VTMPF halt and prevent continuous System Scan from starting (see Scan Will Not Start).

SCAN mode executes system measurement scans as a single pass or continuously following a trigger (System Scan Sequence). The type of System Scan (single or continuous) is determined by the setting of bit 0x01.1 - Scan Select. Continuous System Scan can be paused without exiting SCAN mode by setting the System Scan Select bit to 1 for single Scan.

Some faults, too many current readings below I_{Zero_THR} (see 0x2E.5:3 - Low Power Timer), or a $\overline{\text{RESET}}$ causes an exit from SCAN to IDLE mode. Fault reaction is immediate for some faults while others wait until measurement completes. See the individual fault descriptions for details. Setting the 0x01.7 - Soft Reset or 0x01.6 - Reset to IDLE bits causes a transition from SCAN mode to IDLE mode.

7.2.4.1 System Scan Sequence

A System Scan is a sequence of tests that can be executed when the RAA489206 is in SCAN mode. This mode normally monitors the system during charge and discharge operation. The device includes a variety of settings that allow you wide flexibility in choosing how often and what is monitored. Figure 104 is a simplified state diagram that highlights the sequence and options that are described in the following subsections. Fault and measurement gating bits have been omitted.

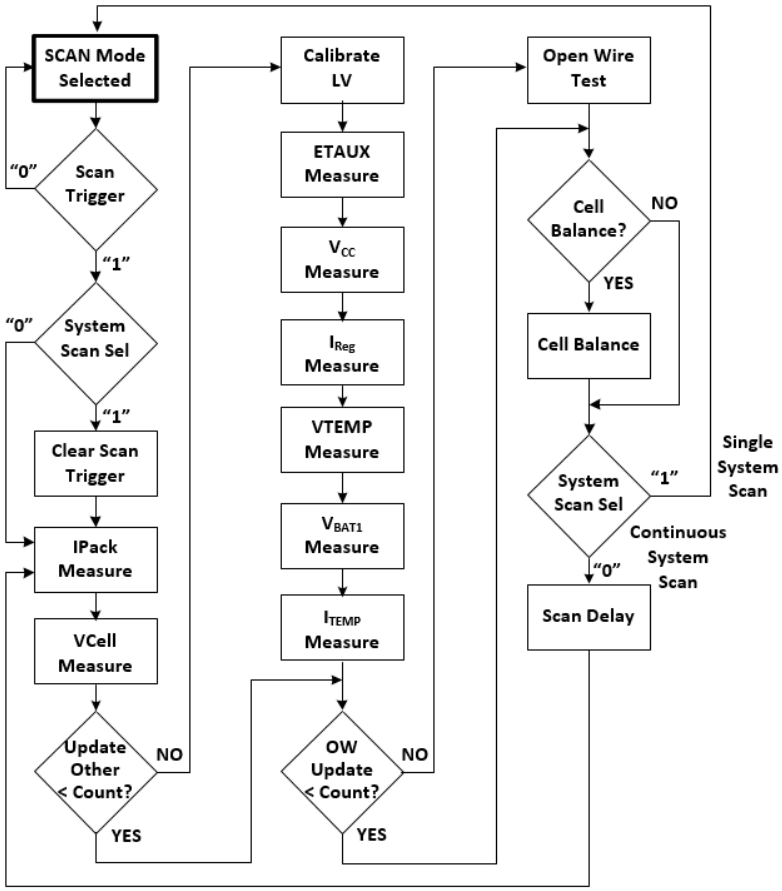


Figure 104. Simplified System Scan

7.2.4.2 SCAN Mode Selected

SCAN mode is selected by setting the bits 0x2E.7:6 - System Mode of the System Operation register to 01. After the master selects SCAN mode, the RAA489206 moves from the previous mode to this point and waits for a 0x01.0 - System Trigger to begin a System Scan.

All control bits and registers that determine what is measured, how frequently it is measured, and if the results affect CFET and DFET operation must be set before the assertion of a System Scan Trigger. This includes Mask Bits that gate Fault assertions of the $\overline{ALRT}$ pin. These bits and registers are listed in the following sections as they become relevant and all must be determined before the master sends the Trigger.

All continuous System Scan loop counters are initialized (see 0x1B.5:4 - Update Other, 0x03.6:5 - OW Update, and 0x03.1 - I_{DIR} Delay). The initial state of the counters is such that all selected tests and measurements associated with them run during the first System Scan during continuous scan.

All fault delay counts are set to 0 when a continuous System Scan is triggered. See 0x09.3:0 - V_{CELL} Fault Delay, 0x09.6 - Delta V_{CELL} Fault Delay, 0x09.4 - ETAUX Fault Delay, and 0x09.5 - Other Fault Delay.

7.2.4.3 Scan Trigger

A Scan Trigger is required to initiate any single or continuous System Scan. Bit 0x01.0 - System Trigger must be set to 1 by the master to initiate a System Scan. The type of System Scan (single or continuous) is determined by the setting of bit 0x01.1 - Scan Select.

If a System Trigger is set when any of the fault conditions listed in Scan Will Not Start is active, it is ignored.

When the System Trigger bit has been received, the Busy bit (0x01.2 - Busy) transitions from a 0 to a 1. If the Busy Mask bit 0x85.0 was cleared before the trigger, then $\overline{ALRT}$ pin goes low (see 0x85 - Other Fault Mask).

Using the mask bit and $\overline{ALRT}$ pin in this way enables the master to determine when the RAA489206 is making measurements to avoid the possibility of reading stale results.

The Busy bit is reset to 0 when each System Scan ends and it is set to 1 when a new System Scan starts.

7.2.4.4 System Scan Select

Following the System Trigger event, the bit setting for 0x01.1 - Scan Select determines if the triggered System Scan is a single pass or continuously looping System Scan. A setting of 0 enables continuous System Scan and a setting of 1 enables a single System Scan.

If a single System Scan is chosen, the System Trigger bit is cleared before the I_{PACK} Measure step in the sequence, otherwise the trigger bit is not cleared.

The System Scan Select bit also determines when a fault response occurs. In single System Scans, the fault response occurs at the end of the System Scan sequence. In continuous System Scans, the fault response is immediate when the fault thresholds and delays are met. By allowing the System Scan sequence to run to completion in single System Scan the RAA489206 gives the master the option to log status and measurements following a fault detection.

7.2.4.5 I_{PACK} Measure

I_{PACK} Measurement is gated by the bit 0x03.7- I_{PACK} EN. Setting this bit to 0 disables the measurement and the System Scan sequence moves to the next step. If this bit is set to 1, I_{PACK} Measurement is enabled and executes.

The RAA489206 connects pins CSP and CSN to the internal ADC and measures the differential voltage based on the setting of register bits 0x03.4:2 - I_{PACK} Averages, which sets the number of averages for I_{PACK} measurements. The measurement is stored in registers 0x52 - 0x53 - I_{PACK} Voltage (R) and the I_{PACK} Timer value is stored in registers 0x54 - 0x57 - I_{PACK} Timer (R).

A measurement result that exceeds either the 0x67.7 - DCHRGI or 0x67.6 - CHRGI thresholds (I_{Zero_THR}) sets the related bit. Also see 0x03.1 - I_{DIR} Delay for Continous Scans.

If the current is between these thresholds for the number of System Scans selected by the bits 0x2E.5:3 - Low Power Timer, the device transitions from SCAN to LOW POWER mode at the end of the sequence.

If the system is discharging, the I_{PACK} voltage measurement is compared to the 0x0B - DOC Threshold. A 0x63.3 - DOCF is set if the DOC threshold is exceeded for the consecutive number of System Scans set by 0x0D - OC Delay.

If the system is charging, I_{PACK} voltage measurement is compared to the 0x0F - COC Threshold. A 0x63.4 - COCF is set if the COC threshold is exceeded for the consecutive number of System Scans set by COC Delay (0x0D - OC Delay).

If the battery is charging with 0x25.3 - IEOC EN and 0x25.6 - Auto CB EN both set to 1, and the CFET is on, the I_{PACK} voltage measurement is compared to the 0x10 - IEOC Threshold to determine if the battery is full. See Automatic Cell Balancing for more information.

Any faults propagate to the $\overline{ALRT}$ pin if the associated mask bits are clear.

Timing of a fault response to DOCF or COCF is determined by System Scan Select. The action taken by the RAA489206 is controlled by register 0x0E - Load/Charge Operations. Set bit 0x0E.7 - CFD to 1 to enable shut off of power FETs because of a DOCF. Set bit 0x0E.2 - FCDC to 1 to enable shut off of power FETs because of a COCF. The setting of the configuration bit 0x0E.3 - CPWR determines if both power FETs are shut off in a series configuration or an individual FET is shut off in a parallel configuration. System Scan stops when the FETs are shut off in a series configuration.

A DSCF fault is not dependent on I_{PACK} measurements and always stops System Scans shutting off CFET and DFET. See 0x63.2 - DSCF.

7.2.4.6 V_{CELL} Measure

V_{CELL} Measurement is gated by the bit 0x02.7 - V_{CELL} EN. A 0 setting disables this measurement and the System Scan sequence moves to the next step.

The RAA489206 first connects pins VC1 and VC0 to the internal ADC and measures the differential voltage based on the setting of register bits 0x02.4:2 - V_{CELL} Averages, which sets the number of averages for V_{CELL} measurements. The MUX sequentially connects each enabled cell, per registers 0x04 - 0x05 - Cell Select, until all are measured. The results are stored in registers 0x30 - 0x4F - V_{CELL} Voltage (R). The difference between the highest and lowest cell voltages is calculated and stored in register 0x50 - 0x51 - V_{CELL} Max Delta Voltage (R).

If any V_{CELL} voltage measurement is greater than 0x06 V_{CELL} Overvoltage or less than 0x07 V_{CELL} Undervoltage thresholds (0x06 - 0x07 - V_{CELL} OV Threshold and V_{CELL} UV Threshold), a fault is set. A 0x63.0 - OVF is set if the V_{CELL} OV threshold is exceeded for the consecutive number of System Scans set by V_{CELL} Delay (0x09.3:0 - V_{CELL} Fault Delay). If any V_{CELL} voltage drops below the V_{CELL} UV threshold for more System Scans than the V_{CELL} Delay setting, fault 0x63.1 - UVF is set. These faults propagate to the $\overline{ALRT}$ pin if the associated mask bits are clear (see 0x83 - Priority Fault Mask).

The V_{CELL} Max Delta Voltage is compared to 0x08 - V_{CELL} Max Delta Threshold and if the threshold is exceeded for more System Scans than the setting 0x09.6 - Delta V_{CELL} Fault Delay, fault 0x66.3 - DVCF is set. This fault propagates to the $\overline{ALRT}$ pin if the associated mask bit is clear (see 0x86 - CB Status Mask).

Timing of the fault response to V_{CELL} OV/UV and/or DVCF is determined by System Scan Select. The action taken by the RAA489206 is controlled by register bit 0x24.4 - CELL CON. This bit must be set to 1 to allow V_{CELL} faults to shut off the power FETs. With CELLCON set to 1 an OVF, UVF, or DVCF shuts off both power FETs and stops System Scans.

The lowest cell voltage is compared to the 0x2B - CBMAX Threshold and bit 0x66.2 - 2HI2CB is set if all cell voltages are greater than this threshold.

The highest cell voltage is compared to the 0x2C - CBMIN Threshold and bit 0x66.1 - 2LO2CB is set if all cell voltages are less than this threshold.

The bit 0x66.0 - Need CB is set when the difference between one or more of all the measured cell voltages, and the minimum of all of them is greater than the 0x2A - CB Min Delta Threshold.

If Auto CB EN is set to 1, 0x26-27 - CB Cell State shows the cells automatically determined by the chip to need cell balancing. The RAA489206 finds the minimum of all the cell voltages and calculates the difference between each cell voltage and the minimum. The CB CELL STATE bit is 1 for cells in which the calculated difference is higher than 0x2A - CB Min Delta Threshold. The CB CELL STATE bit is 0 for other cells.

The bit 0x66.4 - VEOC is set if at least one cell voltage measures above the 0x2D - VEOC Threshold.

For constant current charging with bits 0x25.1 - CB EOC and 0x25.3 - IEOC EN both set to 0, 0x66.7 - BAT FULL sets when the VEOC bit (0x66.4) is set.

If bit CB EOC is set to 1 and bit IEOC EN is set to 0, BAT FULL sets when VEOC changes from 0 to 1 and then all cell voltages drop V_{CBHys} below the VEOC threshold.

For constant voltage charging with CB EOC set to 0 and the IEOC EN bit set to 1, 0x66.7 - BAT FULL sets after the highest cell voltage reaches the VEOC threshold (the VEOC bit is set) and the IEOC bit (0x66.5) sets because of the charge current dropping below the 0x10 - IEOC Threshold.

7.2.4.7 Update Other

If a single scan is triggered (0x01.1 System Scan Select set to 1), or this is the first iteration of continuous System Scan, the sequence moves to the next step Calibrate LV. Otherwise, the next step is determined by the Update Other setting.

Register bits 0x1B.5:4 - Update Other set the number of System Scans required to trigger system measurements beyond I_{PACK} and V_{CELL}. If the RAA489206 has completed a number of System Scans equal to the Update Other setting, the Scan counter is cleared and the sequence steps to Calibrate LV, otherwise the sequence steps to Open-Wire Test.

7.2.4.8 Calibrate LV

This step executes an internal calibration of the ADC/MUX path used for the ETAUX, VCC, VTEMP, VBAT1, and ITEMP measurements. It is followed by the ETAUX Measure step.

7.2.4.9 ETAUX Measure

ETAUX Measure is gated by bits 0x11.7:6 - ETAUX Enable. Set these bits to 0 to disable the measurement and move the sequence to the next step. If either or both bits are set to 1, the corresponding measurement is enabled and executes. The following description assumes both bits are set to 1 and the pins are connected to 10kΩ NTC thermistors as shown in Figure 97.

Bit 0x09.7 - AUX/xTn Pull-Up should be disabled with a setting of 0 before starting either type of System Scan. The pull-up is intended for open-wire test of the ETAUX pins. If it is enabled during the ETAUX, measurement results can be slightly higher (indicating a lower temperature). See Aux Pins Open-Wire Test.

Bits 0x11.4:2 - ETAUX Averages set the number of averages for each AUX pin measurement. If AUX0/xT0 is enabled (0x11.6 = 1) the ADC measures its voltage relative to VSS. AUX1/xT1 is measured next if enabled (0x11.7 = 1). The results are stored in registers ETAUX Detectors.

The results are next compared to thresholds for fault detection (see 0x13-1A - ETAUX Thresholds). When the device is charging (0x67.6 - CHRGI is 1), the measurement is compared to the CUTn and COTn thresholds (n = 0 and 1). While discharging (0x67.7 - DCHRGI is 1), the measurement is compared to the DUTn and DOTn thresholds. If the device is neither charging or discharging, the measurement is compared to all thresholds for the measurement pin. Any threshold violation(s) set the related fault bit(s) in register 0x64 - ETAUX Fault. These faults propagate to the $\overline{ALRT}$ pin if the associated mask bits are clear (see 0x84 - ETAUX Fault Mask).

Timing of the fault response to an OT or UT fault is determined by System Scan Select. The action taken when a fault is detected is determined by register bit 0x24.2 - ETA Connect. This bit must be set to 1 to allow OT or UT faults to shut off the power FETs. The setting of the configuration bit 0x0E.3 - CPWR determines if both power FETs are shut off in a series configuration or an individual FET is shut off in a parallel configuration.

7.2.4.10 VCC Measure

VCC Measure is not gated by an enable bit. It is always executed on the first iteration of continuous System Scan or whenever a single System Scan is triggered. During continuous System Scan, subsequent V_{CC} measurements are gated by 0x1B.5:4 - Update Other.

VCC is measured at the VCC pin relative to VSS. Bits 0x1F.4:2 - Other Averages of the V_{BAT1} Operation register set the number of readings averaged per measurement before storing the results to register 0x60 - V_{VCC} Voltage (R).

After measurement, the voltage is compared to the threshold register Power FET Block and if the comparison fails, the fault bit 0x63.7 - VCCF is set. Bit 0x09.5 - Other Fault Delay controls the required number of consecutive faults before action is taken. The fault propagates to the $\overline{ALRT}$ pin if the associated mask bit is clear (see 0x83 - Priority Fault Mask).

Timing of the fault response to VCCF is determined by System Scan Select. The fault response is not controlled by a register Connect bit. A VCCF shuts off both power FETs. The setting of the configuration bit 0x0E.3 - CPWR has no effect on VCC faults.

7.2.4.11 I_{Reg} Measure

I_{Reg} Measure is not gated by an enable bit. It is always executed on the first iteration of continuous System Scan or whenever a single System Scan is triggered. During continuous System Scan, subsequent I_{Reg} measurements are gated by 0x1B.5:4 - Update Other.

The I_{Reg} voltage is a differential measurement across the external sense resistor tied between the EMITTER and VDD pins, as shown in Figure 98. Bits 0x1F.4:2 - Other Averages of the V_{BAT1} Operation register set the number of readings averaged per measurement before storing the results to register 0x61-62 - I_{REG} Voltage (R).

This measurement has two thresholds, $IREG_{OC1}$ and $IREG_{OC2}$ (0x1D,1E - $IREG_{OC1, 2}$ Threshold). When the device is in IDLE or SCAN mode, the measurement is compared to $IREG_{OC1}$. In LOW POWER mode, the measurement is compared to $IREG_{OC2}$. If the comparison fails, the respective I_{Reg} fault bit (0x67.2 - IREG1 or 0x67.1 - IREG2) is set. This fault propagates to the $\overline{ALRT}$ pin if the associated mask bit is clear (see 0x87 - Status Mask).

Timing of the fault response to I_{Reg} Measure is determined by System Scan Select. The fault response is not controlled by a register Connect bit. An I_{Reg} fault shuts off both power FETs and stops System Scans, regardless of the setting of the configuration bit 0x0E.3 - CPWR.

7.2.4.12 VTEMP Measure

VTEMP Measure is not gated by an enable bit. It is always executed if a single System Scan is triggered or on the first iteration of continuous System Scan. During other iterations of continuous System Scan, its measurement is gated by 0x1B.5:4 - Update Other. The VTEMP voltage is a reference voltage used to pull up the external temperature sensor circuitry (see Figure 97). The Other Averaging bits (see 0x1F.4:2 - Other Averages) of the V_{BAT1} Operation register set the number of samples averaged per measurement before storing the results to register 0x5F - V_{VTEMP} Voltage (R).

The $\overline{VTEMP}$ voltage has a compare threshold that sets the bit 0x67.0 - VTMPF if violated. This fault propagates to the $\overline{ALRT}$ pin if the associated mask bit is clear (see 0x87 - Status Mask). The $VTEMP_{Min}$ threshold limit is a fixed value. An VTMPF fault shuts off both power FETs and stops System Scans, regardless of the setting of the configuration bit 0x0E.3 - CPWR.

7.2.4.13 V_{BAT1} Measure

V_{BAT1} Measure is gated by bit 0x1F.7 - V_{BAT1} EN. Set this bit to 0 to disable the measurement and move the System Scan sequence to the next step. Set this bit to 1 to enable and execute VBAT Measurement.

The V_{BAT1} voltage is measured by the ADC relative to VSS. The number of averages for the measurement are set by bits 0x1F.4:2 - Other Averages. The results are stored in registers 0x20 - 0x21 - V_{BAT1} Thresholds.

If the V_{BAT1} voltage measurement is greater than 0x20 - V_{BAT1} OV Threshold, bit 0x65.7 - VBOVF is set. If the measurement is less than 0x21 - V_{BAT1} UV Threshold, bit 0x65.6 - VBUVF is set. Bit 0x09.5 - Other Fault Delay controls the required number of consecutive faults before action is taken. VBOVF and VBUVF faults propagate to the $\overline{ALRT}$ pin if the associated mask bits are clear (see 0x85 - Other Fault Mask).

Timing of the fault response to V_{BAT} OV/UV is determined by System Scan Select. The action taken when a fault is detected is determined by register bit 0x24.3 - VBAT1 CON. This bit must be set to 1 to allow VBOVF or VBUVF to shut off the power FETs. The setting of the configuration bit 0x0E.3 - CPWR determines if both FETs are shut off in a series configuration or an individual FET is shut off in a parallel configuration.

7.2.4.14 I_{TEMP} Measure

Internal Temperature measurement is gated by bit 0x1F.6 - I_{TEMP} EN. Set this bit to 1 to enable measurement of the internal temperature while in SCAN mode. Set this bit to 0 to disable the measurement and move the sequence to the next step.

The RAA489206 connects the internal temperature sensor to the ADC and measures its voltage. Bits 0x1F.4:2 - Other Averages set the number of averages for I_{TEMP} measurements. The results are stored in register 0x5E - Internal Temperature (R). The bit 0x09.5 - Other Fault Delay controls the required number of consecutive faults before action is taken.

If the I_{TEMP} voltage measurement result is less than the 0x22 IOTW Threshold, a warning bit 0x66.6 - IOTW is set. If the I_{TEMP} measurement result is less than the 0x23 IOTF Threshold, fault bit 0x63.5 - IOTF is set. The warning/fault propagates to the $\overline{ALRT}$ pin if the associated mask bit is clear (see 0x86 - CB Status Mask and 0x83 - Priority Fault Mask). See 0x22 - 0x23 - IOTW and IOTF Thresholds for information about setting the thresholds.

Timing of the fault response to I_{TEMP} is determined by System Scan Select, otherwise the action taken by the RAA489206 is not controlled by a register Connect bit. An IOTW does not change the status of the power FETs or stop System Scans. An IOTF shuts off both power FETs and stops System Scans regardless of the setting of bit 0x0E.3 - CPWR.

7.2.4.15 Open-Wire Test

Open-Wire Test is gated by bit 0x24.6 - OW EN. Set this bit to 0 before starting System Scan to disable the test, and the sequence moves to the next step. When enabled, the Open-Wire Test executes if the System Scan counter set by 0x03.6:5 - OW Update is satisfied.

The results of the open-wire tests are found in locations 0x68-69 - Open-Wire Status, 0x65.2 - OW V_{BAT1}, and 0x65.1 - OW VSS. A 1 at an OW Celln bit indicates that at least one wire is not connected between the device and the corresponding cell. Bit 0x63.6 - OWF is the OR'd result of all the open-wire fault bits. The faults for any of the open-wire bits can propagate to the $\overline{ALRT}$ pin if the associated mask bits are cleared. See 0x88-89 - Open-Wire Mask and 0x85 - Other Fault Mask.

An OWF shuts off both power FETs and stops System Scans regardless of bit 0x0E.3 - CPWR.

See Open-Wire Function for a detailed description of the test sequence and options.

7.2.4.16 Cell Balance

Automatic Cell Balancing during a System Scan is gated by bits 0x25.7 - CB EN and 0x25.6 - Auto CB EN. Set either of these bits to 0 to disable Automatic Cell Balancing and move the sequence to the next step. If both bits are set to 1, Automatic Cell Balancing is enabled and executes per the following settings:

- 0x25.5 - CB Configuration selects internal or external Cell Balancing FETs.
- 0x25.3 - IEOC EN selects ending charging with either a voltage or current target.
- 0x25.2 - CB Mask selects allowing or preventing simultaneous balancing of adjacent cells.
- 0x25.1 - CB EOC selects allowing or preventing cell balancing after reaching VEOC.
- 0x25.0 - CB CHRG selects allowing or preventing cell balancing while charging below VEOC.
- 0x2A - CB Min Delta Threshold sets the minimum cell voltage difference for cell balancing.
- 0x2B - CBMAX Threshold sets the maximum cell voltage allowed for cell balancing.
- 0x66.2 - 2HI2CB is set if all cell voltages are greater than CB MAX Threshold.
- 0x2C - CBMIN Threshold sets the minimum cell voltage allowed for cell balancing.
- 0x66.1 - 2LO2CB is set if all cell voltages are less than CB MIN Threshold.
- 0x2D - VEOC Threshold sets the maximum cell voltage used to indicate end of (constant current) charge.
- 0x10 - IEOC Threshold sets the minimum charge current to indicate end of constant voltage charge.
- 0x28, 0x29 - Cell Balancing Timers sets the balance on and off times.

A thorough review of Sections Cell Balancing Registers and Automatic Cell Balancing is recommended to determine application-specific settings.

Cell balancing methods supported by the RAA489206 are detailed in Cell Balancing Examples.

7.2.4.17 Scan Delay

The setting of 0x2E.2:0 - Scan Delay controls the delay time between finishing a continuous System Scan cycle and starting the next. The Busy Bit (0x01.2 - Busy) is cleared at the start of Scan Delay.

7.2.4.18 System Scan Select

The continuous System Scan sequence is completed when the Scan Delay time ends. The bits 0x01.1 - Scan Select controls whether the System Scan is single or continuously looping. A setting of 0 enables continuous System Scan and a setting of 1 choses a single System Scan.

If a single System Scan is selected, the state machine returns to the SCAN mode start point System Scan Sequence and waits for the next Scan Trigger.

If continuous System Scan is selected and no faults occur, the System Scan counter is incremented and the state machine returns to step System Scan Select where the next sequence begins (see Figure 104).

The System Scan Select bit also determines when a fault response occurs. For single System Scan, the fault response occurs at the end of the System Scan sequence. In continuous System Scan, the fault response occurs when the fault thresholds and delay counters are met.

7.2.5 Scan Will Not Start

System Scan can not start if the RAA489206 is being reset by POR, $\overline{\text{RESET}}$ held low, or either 0x01.7 - Soft Reset or 0x01.6 - Reset to IDLE set to 1. System Scan only runs in SCAN mode, it can not run in IDLE, LOW POWER, or SHIP Modes.

If any of the following bits are set, System Scan may not start and/or stops until the fault is clear:

- 0x63.7 - VCCF
- 0x63.6 - OWF
- 0x63.5 - IOTF
- 0x63.2 - DSCF
- 0x67.2 - IREG1
- 0x67.0 - VTMPF
- 0x65.5 - CPMP NRDY

These conditions stop and prevent System Scans if the 0x0E.3 - CPWR bit is 0:

```
(0x0E.2 - FCDC AND 0x67.6 - CHRGI AND 0x63.4 - COCF)
OR
(0x0E.7 - CFD AND 0x67.7 - DCHRGI AND 0x63.3 - DOCF)
OR
(0x24.4 - CELL CON AND 0x66.3 - DVCF)
OR
CELLCON AND {[(CHRGI AND NOT[CHRWUV]) OR DCHRGI] AND UVF}
OR
CELLCON AND {[(DCHRGI AND NOT[DCHRWUV]) OR CHRGI] AND OVF}
OR
0x24.3 - VBAT1 CON AND [CHRGI AND VBOVF] OR [DCHRGI AND VBUVF]
OR
0x24.2 - ETA Connect AND DCHRGI AND (DOT0 OR DOT1 OR DUT0 OR DUT1)
OR
ETA CON AND CHRGI AND (COT0 OR COT1 OR CUT0 OR CUT1)
```

This condition stops and prevents System Scans if the CPWR bit is 1:

```
CELLCON AND {DVCF OR (NOT[CHRWUV] AND UVF) OR (NOT[DCHRWOV] AND OVF)}
```

For bit descriptions see the following:

- 0x63.1 - UVF
- 0x63.0 - OVF
- 0x02.5 - CHRWUV
- 0x02.6 - DCHRWOV
- 0x64.1 - DOT0
- 0x64.5 - DOT1
- 0x64.0 - DUT0
- 0x64.4 - DUT1
- 0x64.3 - COT0
- 0x64.7 - COT1
- 0x64.2 - CUT0
- 0x64.6 - CUT1
- 0x65.7 - VBOVF
- 0x65.6 - VBUVF
- 0x67.7 - DCHRGI
- 0x67.6 - CHRGI

7.3 Open-Wire Function

The open-wire function tests for broken connections between the battery cells and the BMS circuit board. A block diagram of the open-wire circuit is shown in Figure 105. The cell open-wire test (VC0 - VC16) checks the wires between the connector and cells (in blue) while VSS and V_{BAT1} OW checks the connections in red.

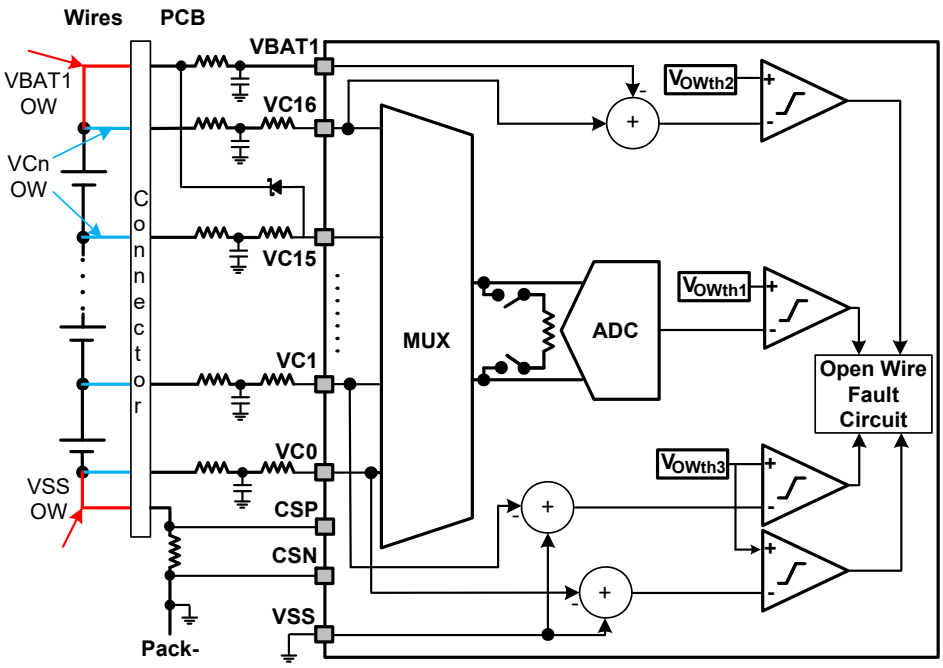


Figure 105. RAA489206 Open-Wire Circuit Block Diagram

An open-wire test can be triggered manually by setting bit 0x24.5 - OW Trigger to 1 while in IDLE mode. The test is executed automatically during System Scans if bit 0x24.6 - OW EN is set to 1. The open-wire test is run on the first and every nth System Scan per the setting of bits 0x03.6:5 - OW Update during continuous System Scans. If an open-wire fault occurs during a System Scan, the scan stops, DFET and CFET are turned off, and DFET EN and CFET EN are set to 0 (see 0x24 - Power FET Operation).

An internal resistor is connected across one cell at a time during the open-wire test. The resistor is connected for t_{OW} across the cell. A cell measurement is performed after $0.8*t_{OW}$. If the voltage reading is less than V_{OWth1}, at least one of the cell connections is considered open. Open-wire test results are a function of the capacitance connected to the device pins because the voltage across a larger capacitance takes longer to change. The open-wire circuit is designed to tolerate up to C_{OW} of equivalent capacitance on each pin.

As an example, consider the case when the OW Test resistor is connected between device pins VC5 and VC6. If the measured cell voltage is less than V_{OWth1}, the connection between the battery and pins VC5 and/or VC6 is likely to be bad. If only one pin has a bad connection, the specific pin can be determined with two open-wire fault bits. If only Cell(n) and Cell(n-1) fail open-wire, the open pin is VC(n-1) because bits OW Cell(n) and OW Cell(n-1) (0x68-69 - Open-Wire Status) are set. Open-wire mask bits are in registers 0x88-89 - Open-Wire Mask. If a mask bit is set to 0 and an open is detected on that cell, the $\overline{ALRT}$ pin transitions low. Open-wire status of VC0 is tested with VC1 and indicated by the bit for OW Cell1.

After all of the cell voltage sense connections have been tested, the pack current is measured. If the current measurement shows that the pack is discharging, the open-wire sequence ends. If in IDLE mode when the exit from open-wire test occurs, the Busy bit is cleared. If the pack is not discharging, the VSS and VBAT1 connections are tested for open-wires before the open-wire sequence ends.

If VSS connection to the bottom cell is made through the pack low-side sense resistor and load current wire (Figure 105), separate from the VC0 and VC1 voltage sense connections to their respective cells, an open in the pack ground return connection is detectable. The VSS pin voltage is compared to VC0 and VC1 pins. If (VSS - VC0) and/or (VSS - VC1) are greater than V_{OWth3}, the VSS ground return connection is considered open.

If a Schottky diode is connected from VC15 to V_{BAT1} and the V_{BAT1} connection to the top cell is made through the pack high-side load current wire, separate from VC15 and VC16 voltage sense connections to their respective cells, an open in the high-side load current connection is detectable. The V_{BAT1} pin voltage is compared to VC16. If (VC16 - VBAT1) is greater than V_{OWth2}, the V_{BAT1} pin connection is considered open.

Open-wire fault indicators for VSS and VBAT1 are located in 0x65 - Other Fault Register and the mask bits are in 0x85 - Other Fault Mask.

Note the difference between Status bit 0x67.7 - DCHRGI and internal states charging, discharging, and NOT discharging. If the current voltage measurement is less than -200µV (-20 decimal register value), the pack is discharging. If the current voltage measurement is greater than +200µV (+19 decimal register value), the pack is charging. If the current voltage measurement is greater than approximately -200µV (-20 decimal register value), the pack is NOT discharging. These internal states are not gated by counters; in Continuous Scan mode bits DCHRGI and 0x67.6 - CHRGI are gated by 0x03.1 - I_{DIR} Delay.

The open-wire sequence does not include testing the ETAUX pins for open wires. See Aux Pins Open-Wire Test for a description of the test method.

Voltage measurements done as part of the open-wire test sequence are only used for open-wire detection. They are not stored in registers or used to detect overvoltage or undervoltage faults.

7.4 Cell Balancing Examples

Register 0x25 - CB Operation controls cell balancing features of the RAA489206. The master must select either Automatic or Manual cell balancing, and the conditions under which balancing occurs.

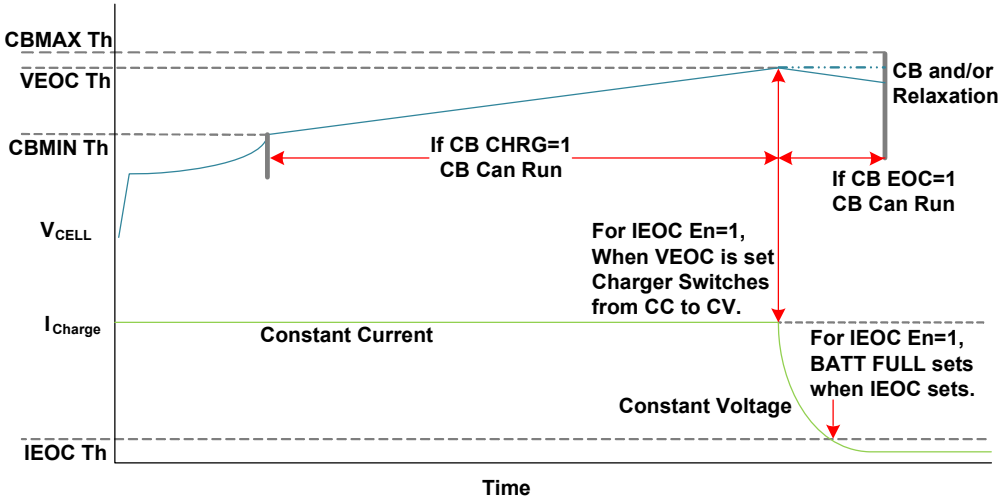


Figure 106. A Typical Charge Characteristic Curve

The RAA489206 has features that support both Constant Current (CC) and Constant Voltage (CV) charging. A typical charging profile for a battery cell is depicted in Figure 106. Cell balancing can occur only when the cell voltage is between the CBMIN and CBMAX limits, which are independent of CB EOC and CB CHRG bit settings.

The following examples are independent of the choice of internal versus external cell balancing FETs.

7.4.1 Automatic Cell Balancing

Bits 0x25.0 - CB CHRG, 0x25.1 - CB EOC, and 0x25.3 - IEOC EN determine the behavior of automatic cell balancing relative to 0x2D - VEOC Threshold and 0x10 - IEOC Threshold. The behavior of auto cell balancing in relation to these bits and thresholds is summarized in Table 74. This table assumes charging, automatic cell balancing is enabled, cell voltages are between CBMIN and CBMAX, VEOC is less than CBMAX, and at least one cell needs to be balanced.

Table 74. Auto CB vs Bit Settings

CB CHRG	IEOC EN	CB EOC	Sequence	Charge Type
1	0	0	Cell balancing starts when a cell needing balancing is greater than CBMIN and less than CBMAX. VEOC sets when the maximum cell voltage is >VEOC threshold, this triggers BAT FULL to set, which stops Cell Balancing, shuts off CFET (and DFET if CPWR = 0) and clears AUTO CB. DFET remains on if CPWR = 1.	Constant Current
1	0	1	Cell balancing starts when cell voltages are within ~60mV of the VEOC threshold. VEOC sets when the highest cell voltage is >VEOC threshold and CFET (and DFET if CPWR = 0) shuts off. Cell balancing is applied until all cell voltages fall below VEOC - V_{CBHys}. Next, Cell Balancing stops, the BATT FULL bit is set, and AUTO CB is cleared. DFET remains on if CPWR = 1.	Constant Current
1	1	0	Cell balancing starts when a cell needing balancing is greater than CBMIN and less than CBMAX. VEOC sets when the highest cell voltage is >VEOC threshold, and then cell balancing and DFET (if CPWR = 1) shut off. The charger changes from constant current to constant voltage. When the charge current drops below the 0x10 - IEOC Threshold) BATT FULL is set, CFET (and DFET if CPWR = 0) is shut off, and AUTO CB is cleared.	Constant Current followed by Constant Voltage

Table 74. Auto CB vs Bit Settings (Cont.)

CB CHRG	IEOC EN	CB EOC	Sequence	Charge Type
1	1	1	Cell balancing starts when a cell needing balancing is greater than CBMIN and less than CBMAX. CB continues after VEOC is reached and the bit is set, but DFET shuts off if CPWR = 1. The charger changes from constant current to constant voltage. Cell balancing continues until the charge current drops below the IEOC limit; next, BATT FULL is set, CFET (and DFET if CPWR = 0) is shut off, and AUTO CB is cleared.	Constant Current followed by Constant Voltage
0	0	1	Cells charged until the VEOC threshold is exceeded and the VEOC bit sets, which shuts off CFET (and DFET if CPWR = 0). Cell balancing starts and continues until cell voltages fall below VEOC and stops, the BATT FULL bit is set, and AUTO CB is cleared.	Constant Current
0	1	1	Constant current charging until the VEOC threshold is exceeded and the VEOC bit sets, which shuts off DFET if CPWR = 1. The charger changes from constant current to constant voltage. Cell balancing occurs while one or more cell voltages are above the VEOC limit AND the charge current is above the IEOC limit. BAT FULL is set when the charge current drops below the IEOC limit. When BATT FULL is set, CFET is shut off (and DFET if CPWR = 0), and AUTO CB is cleared.	Constant Current followed by Constant Voltage

Registers 0x26-27 - CB Cell State show the cells automatically determined by the chip to need cell balancing following the most recent set of cell voltage measurements during scan before automatic cell balancing.

Figure 107 is an illustration of the Automatic Cell Balancing sequence described in detail in the following subsections. All settings must be written to the RAA489206 before 0x01.0 - System Trigger is executed. This example assumes the RAA489206 is in SCAN mode, the system is charging the battery pack and the step Cell Balance has been reached. The same sequence is followed if AUTO CB is enabled and cell balancing is started by the bit 0x25.4 - CB Trigger.

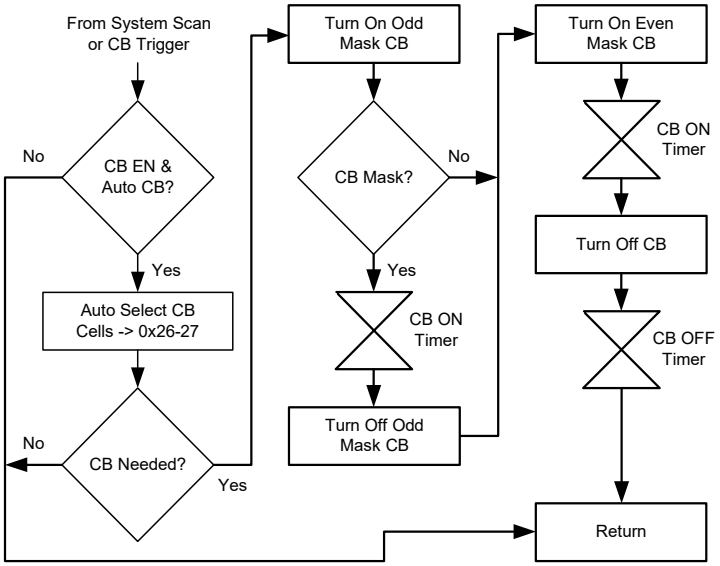


Figure 107. Auto CB Sequence

7.4.1.1 Auto CB Sequence

1. **CB EN & Auto CB? -** If 0x25.7 - CB EN and 0x25.6 - Auto CB EN are both enabled the CB sequence moves to the next step, otherwise it exits and returns to the System Scan sequence step Scan Delay.
2. **Auto Select CB Cells -** For the three cases of automatic cell balancing where IEOC EN = 1 **OR** CB EOC = 0, the chip finds the minimum of all the cell voltages and calculates the difference between each cell voltage and the minimum. For cells with a calculated difference higher than the 0x2A - CB Min Delta Threshold, the CB Cell

State bit is set to 1. For other cells, it is set to 0.
For automatic cell balancing cases with IEOC EN = 0 **AND** CB EOC = 1, the CB Cell State bit is set to 1 for cells that exceed the voltage set by the register 0x2D - VEOC Threshold minus four bits. For other cells, it is set to 0.

3. **CB Needed? -** If no cells require cell balancing or the criteria determined by the settings of bits CB CHRG, IEOC EN, and CB EOC as detailed in Table 74 are not met, the cell balance sequence exits and returns to step Scan Delay. Otherwise the CB sequence moves to the next step.
   Note: If AUTO CB EN = 0, the bit 0x66.0 - Need CB is an indicator to the user.
4. **Turn On Odd Mask CB -** Cell balance devices for the odd numbered cells that were automatically determined to require balancing as indicated by the CB Cell State registers 0x26-27 are turned on.
5. **CB Mask? -** If the bit 0x25.2 - CB Mask is clear (0), the sequence moves to the **Turn On Even Mask CB** step, otherwise the **CBON Timer** is activated per the following step.
6. **CBON Timer -** The timer setting 0x28 - CBON determines how long the cell balance FETs are enabled for each cycle of balancing. The sequence moves to the next step after the CBON Timer times out.
7. **Turn Off Odd Mask CB -** Cell balance FETs for the odd cells are turned off.
8. **Turn On Even Mask CB -** The cell balance FETs for the even numbered cells that were automatically determined to require balancing as indicated by the CB Cell State registers 0x26-27 are turned on.
9. **CBON Timer -** The timer setting 0x28 - CBON determines how long the cell balance FETs are enabled for each cycle of balancing. The sequence moves to the next step after the CBON Timer times out.
10. **Turn Off CB -** Cell Balance FETs for all cells are turned off.
11. **CBOFF Timer -** The timer setting 0x29 - CBOFF determines how long the cell balance FETs are disabled following each cycle of balancing. This step is necessary when long cell balancing times relative to the setting of 0x2E.2:0 - Scan Delay are used. The CBOFF timer also manages power dissipation. The sequence moves to the next step after the CBOFF Timer times out.
12. **Return -** The CB state machine exits and returns to the Scan sequence at Scan Delay after the CBOFF Timer times out.

7.4.2 Manual Cell Balancing

Manual Cell Balancing follows the sequence shown in Manual CB Sequence, which is very similar to that of Automatic Cell Balancing with a few important differences. Bit 0x25.7 - CB EN must be set to 1 to enable manual cell balancing, and bit 0x25.6 - Auto CB EN must be set to 0 to disable automatic cell balancing.

The master must determine the cells to be balanced and write the bits in registers 0x26-27 - CB Cell State. A 1 is written to cell locations selected for charge reduction and a 0 is written to cell locations that receive the full charge current.

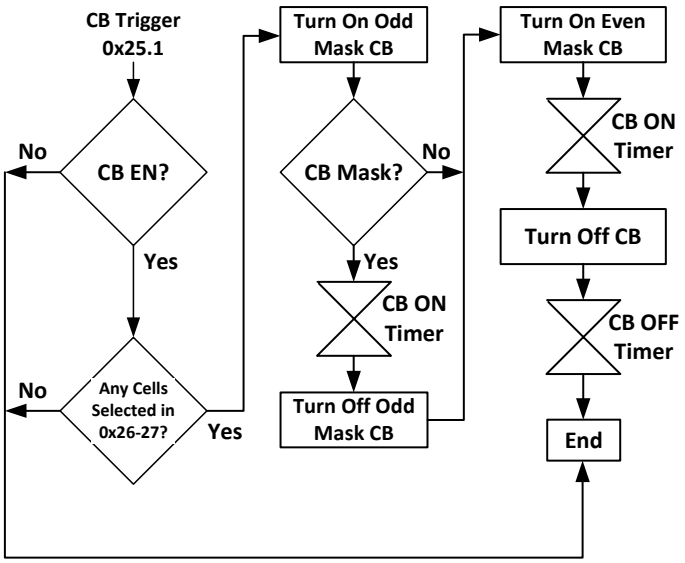


Figure 108. Manual CB Sequence

Bit 0x25.2 - CB Mask controls whether all cells that need balancing are turned on simultaneously or in separate ON cycles. Simultaneous cell balancing of too many and/or adjacent cells can be inefficient and raise the die temperature from the power dissipation of the internal cell balancing FETs if 0x25.5 - CB Configuration = 0.

All relevant settings must be written to the RAA489206 before cell balancing is triggered (0x25.4 - CB Trigger).

7.4.2.1 Manual CB Sequence

1. **CB Trigger -** With the RAA489206 in SCAN mode (0x01.1 - Scan Select must be set to 1 for single scan), the master must set the bits in registers 0x26-27 - CB Cell State to 1 for cells that have charged to relatively higher voltages than the rest of the pack. Bits for the other cells are set to 0 so they receive the full charge current. For manual cell balancing, the criteria used to determine which cells to get the reduced charge current is determined by you. When ready, the master triggers Cell Balancing by writing a 1 to 0x25.4 - CB Trigger.
2. **CB EN? -** If bit 0x25.7 - CB EN is not set to 1, the CB sequence exits, otherwise it moves to the next step.
3. **Any Cells Selected in 0x26-27? -** The master must determine the cells to be balanced, and write the bits in registers 0x26-27 - CB Cell State before the CB Trigger. If no cell is selected the cell balance sequence exits. **Note:** With Auto CB EN set to 0 for Manual Cell Balancing the NEED CB bit has no function.
4. **Turn On Odd Mask CB -** The cell balance FETs for the odd numbered cells that were manually determined to require balancing as indicated by the CB Cell State registers 0x26-27 are turned on.
5. **CB Mask -** If the bit 0x25.2 - CB Mask is clear (0), the CB sequence moves to the **Turn On Even Mask CB** step, otherwise the **CBON Timer** is activated per the next step.
6. **CBON Timer -** The Timer setting 0x28 - CBON determines how long the cell balance FETs are enabled for each cycle of balancing. The sequence moves to the next step after the CBON Timer times out.
7. **Turn Off Odd Mask CB -** Cell balance FETs for the odd cells are turned off.
8. **Turn On Even Mask CB -** The cell balance FETs for the even numbered cells that were manually determined to require balancing as indicated by the registers 0x26-27 - CB Cell State are turned on.
9. **CBON Timer -** The timer setting 0x28 - CBON determines how long the cell balance FETs are enabled for each cycle of balancing. The sequence moves to the next step after the CBON Timer times out.
10. **Turn Off CB -** Cell balance FETs for all cells are turned off.
11. **CBOFF Timer -** The timer setting 0x29 - CBOFF determines how long the cell balance FETs are disabled for each cycle of balancing. The sequence moves to the next step after the CBOFF Timer times out.
12. **End -** The CB state machine exits after the CBOFF Timer times out.

7.5 Charge Pump

The RAA489206 has an internal Charge Pump with an external capacitor used to drive the CFET, DFET, and CB16 pins. Control bit 0x24.7 - CPMP EN allows you to enable or disable the Charge Pump as needed. The default value for the control bit is 0 so the Charge Pump is disabled following a chip power up or reset. If the charge pump is enabled (0x24.7 = 1), the status bit 0x65.5 - CPMP NRDY is set by the RAA489206 to 1 until the charge pump voltage is up to its operating level, then it clears to 0. If the charge pump is disabled by the Master setting 0x24.7 = 0, bit CPMP NRDY is also set to 0.

Charge Pump circuitry is automatically disabled in SHIP and LOW POWER Modes regardless of the setting of bit 0x24.7 CPMP EN.

The charge Pump State Machine is detailed below in Figure 109.

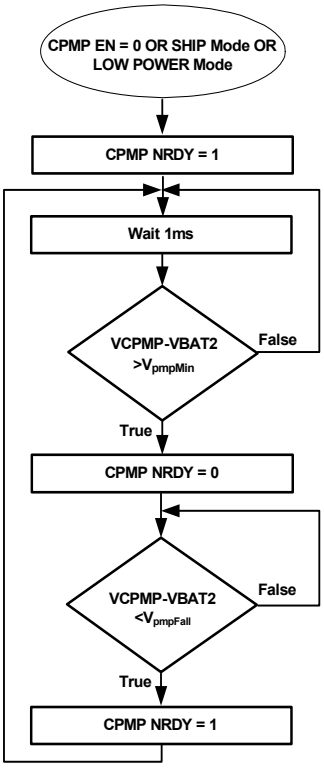


Figure 109. RAA489206 Charge Pump Ready State Machine

7.5.1 Charge Pump Ready State Machine

The state machine starts at the point at which the charge pump is disabled during the power up sequence (see Figure 109) or at chip reset, by being in SHIP or LOW POWER mode, or by bit 0x24.7 CPMP EN being 0. Bits 0x24.7 - CPMP EN and 0x65.5 - CPMP NRDY are set to 0 following POR or reset.

The state machine starts when the charge pump is enabled (0x24.7 = 1), in IDLE or SCAN Modes. The device begins charging the external capacitor at an operational frequency of ~4MHz. When the charge pump voltage is above the minimum threshold V_{pmpMin}, the state machine clears bit CPMP NRDY. Next, the charge pump voltage is continuously compared to the $V_{pmpFall}$ threshold. If the voltage drops below that threshold, the state machine sets bit CPMP NRDY.

The charge pump enable bit is set to 0 by default at POR or Reset, or by the master. Transitions to SHIP or LOW POWER mode automatically shut off the charge pump. The mode change shuts off the charge pump regardless of whether it was executed by the master or caused by a fault detection. If the charge pump was enabled, the not ready bit is also set when the charge pump voltage drops below the internal fixed threshold.

The charge pump enable bit is not affected by a mode change, it is only changed by the master directly. After the enable of the charge pump a minimum 1ms wait occurs to allow time for the circuitry to begin charging the external capacitor.

7.6 Trigger Bits

Some control registers have bits called Trigger bits that execute automatic sequences when set to 1. Triggered sequences are initiated by a 0 to 1 transition of a Trigger bit. When the triggered sequence starts, the Trigger bit is reset back to 0 automatically by the chip. A 0 to 1 transition of a Trigger bit is ignored if that triggered sequence is already in progress. If a Trigger bit is ignored, the chip does not clear the Trigger bit automatically. In this case, to start a triggered sequence, you must first write a 0 followed by a 1 to the Trigger bit.

The System Trigger bit (0x01.0 - System Trigger) is ignored when the System mode bits are SHIP, LOW POWER, or IDLE. It is executed only when the bits 0x2E.7:6 - System Mode are set to SCAN mode. All other Trigger bits are ignored in SHIP or LOW POWER Modes, and can only trigger sequences in IDLE or SCAN mode. These Trigger bits should be used only in IDLE mode because Renesas recommends to reserve SCAN mode for System Scans only.

If the RAA489206 is running a sequence started by a previous Trigger bit transition, the new Trigger bit transition is queued. It is scheduled for when the sequence in progress completes.

If the RAA489206 is in a condition that prevents running the desired sequence, the Trigger bit transition is ignored. It is not executed when the condition changes. For example, if the chip has a fault that prevents executing the Trigger bit, the fault goes away, and a new 0 to 1 transition of the Trigger bit is needed to start the sequence. This applies unless the chip is in the middle of a sequence started by a previous Trigger bit transition, in which case the triggered sequence executes.

When multiple Trigger bits are in the queue, only the one with highest priority is executed. When its execution starts, all other queued Trigger bits are cleared. This means that besides the triggered sequence in progress, only one more is executed later because the queue is cleared when the second starts. When the second starts, the user can queue a third one that is executed when the second completes. The priority is fixed in design, from high to low:

- 0x01.0 - System Trigger
- 0x01.5 - Recalibrate V_{OS} Trigger
- 0x02.0 - V_{CELL} Trigger
- 0x03.0 - I_{PACK} Trigger
- 0x11.0 - ETAUX Trigger
- 0x1B.0 - V_{REG} Trigger
- 0x1F.5 - I_{TEMP} Trigger
- 0x1F.0 - V_{BAT1} Trigger
- 0x24.5 - OW Trigger
- 0x25.4 - CB Trigger.

When the previous triggered sequence is completed, the circuit first takes the Trigger bit in queue with highest priority, and clears the entire queue. Next, it checks the conditions against the Trigger bit to be executed. If conditions do not allow it to be executed, the circuit goes back to IDLE mode, otherwise the circuit starts the new sequence. A Fault never clears the queue.

8. Communication Interface

The RAA489206 includes a digital interface for you to configure operation as well as monitor input and output parameters. Serial communication interfaces are available anytime the chip is not being reset. The RAA489206 supports I^2C, SPI, and SPIw/CRC serial interfaces. The protocol is chosen by connecting the CMS0 pin. The

CMS0 pin is a static input and must not change state while the RAA489206 is powered. If a voltage change occurs, set it to a valid state and RESET the RAA489206. The hardware configuration required to support each communication protocol is listed in Table 75.

The RAA489206 supports sequential read, which can start at any register address. If the master continues to send clock cycles or a presence bit is sent after reading one byte, the device indexes to the next byte and returns the byte value. This continues until the load bit or stop bit is received or CS returns high.

The RAA489206 supports sequential read back commands for all three protocols.

Table 75. Serial Protocol Defined

CMS0	Protocol
DGND	I^2C
VDD	SPI, SPI w/CRC

A comparison of the approximate read times for the three protocols is shown in Table 76.

Table 76. Approximate Read Times

Communication Sequence	Number of Bytes to Read Back	Transaction Time (ms)	
		I^2C (100kHz)	SPI (2MHz)
Read All (0x00-0x89)	138	14.11	0.69
Read V_{CELL} (0x30-0x51)	34	3.36	0.166
Read I_{PACK} (0x52-0x57)	6	0.84	0.041
Read OTHER (0x58-0x62)	11	1.29	0.062
Read FAULT (0x63-0x69)	7	0.93	0.045

8.1 I^2C Serial Interface

This device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the RAA489206 operates as the slave device in all applications. All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

8.1.1 I^2C Address

The RAA489206 can be used with any I^2C host device. Each device must have its own unique serial address to distinguish it from other devices on the bus. The device address is set by connecting the ADDR/$\overline{CS}$ pin to either VDD or DGND. The available addresses are listed in Table 77.

Table 77. I^2C Address Values

Logic Selections	Address (7-bit Binary)
ADDR/$\overline{CS}$ pin tied to VDD	0011 010
ADDR/$\overline{CS}$ pin tied to DGND	0001 010

8.1.2 Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. The SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 110). At power-up, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 110). A START condition is ignored during the power-up sequence.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 110). A STOP condition at the end of a Read operation, or at the end of a Write operation returns the I^2C state machine to its initial state where it waits for the next START.

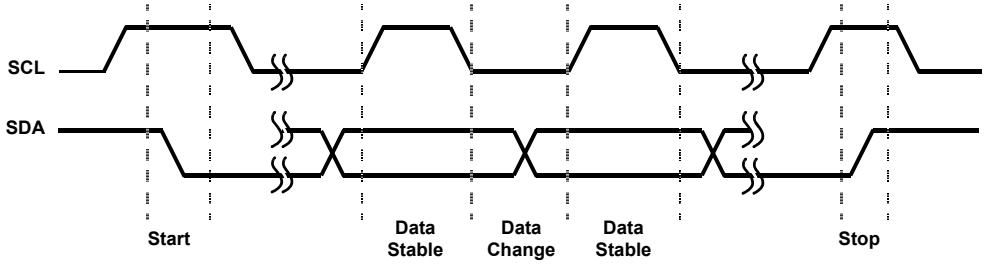


Figure 110. Valid Data Changes, Start, and Stop Conditions

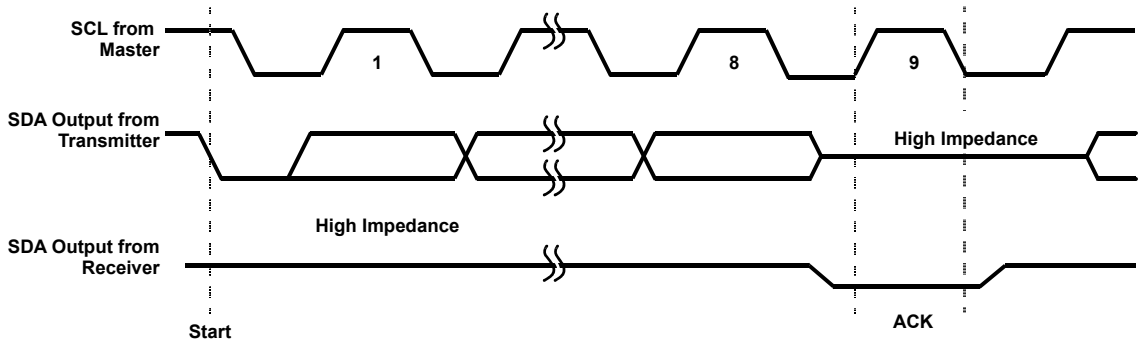


Figure 111. Acknowledge Response from Receiver

An Acknowledge (ACK) is a software convention that indicates a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 111). The device responds with an ACK after recognition of a START condition followed by a valid Slave Address byte, and once again after successful receipt of the Register Address Byte. The device also responds with an ACK after receiving each Data Byte of a Write operation. The master must respond with an ACK after receiving each Data Byte of a Read operation except the last one.

The last bit of the Slave Address byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a 1, a Read operation is selected. A 0 selects a Write operation (see Figure 112).

After loading the entire Slave Address byte from the SDA bus, the device compares it with the internal Slave Address. With a correct compare, the device outputs an acknowledge on the SDA line.

8.1.3 Write Operation

A Write operation requires a START condition, followed by a Slave Address byte, a Register Address byte, a Data byte, and a STOP condition (see Figure 112). The slave device responds with an ACK after successfully receiving each of the three bytes. The content of the Data byte is transferred to the RAA489206 registers at the rising edge of SCL during the ACK that follows the reception of the Data byte.

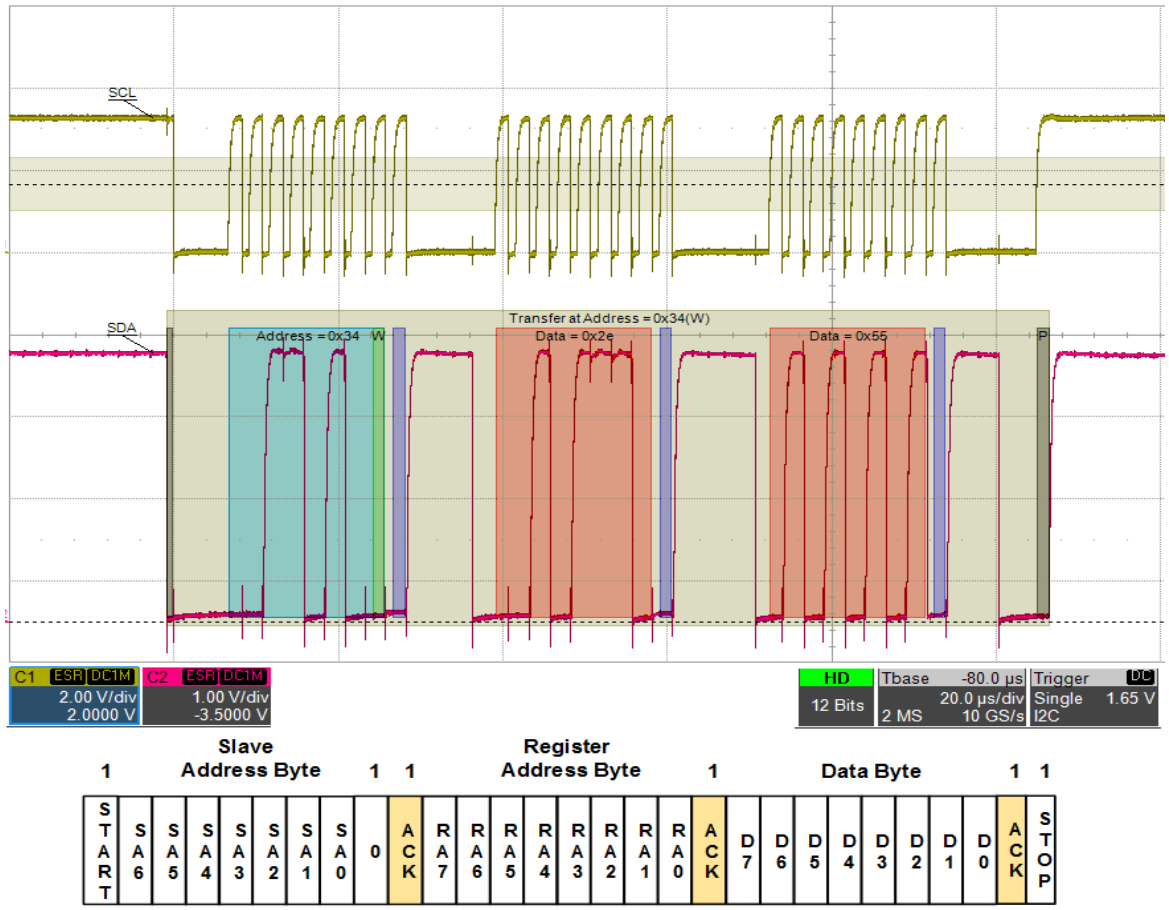


Figure 112. I²C Write Protocol

8.1.4 Read Operation

A Read operation consists of a three byte sequence, followed by one or more Data bytes (see Figure 113). The master initiates the operation issuing the following sequence: a START, the Slave Address byte with the R/W bit set to 0, a Register Address byte, a second START, and a second Slave Address byte with the same seven MSBs but with the R/W bit set to 1. After each of the three bytes, the RAA489206 responds with an ACK. The RAA489206 transmits Data bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of the first byte. The master terminates the Read operation by issuing a NACK followed by a STOP condition.

The Data bytes are from the memory location indicated by an internal pointer. This initial value of the pointer is determined by the address byte in the Read operation instruction, and increments by one during transmission of each Data byte.

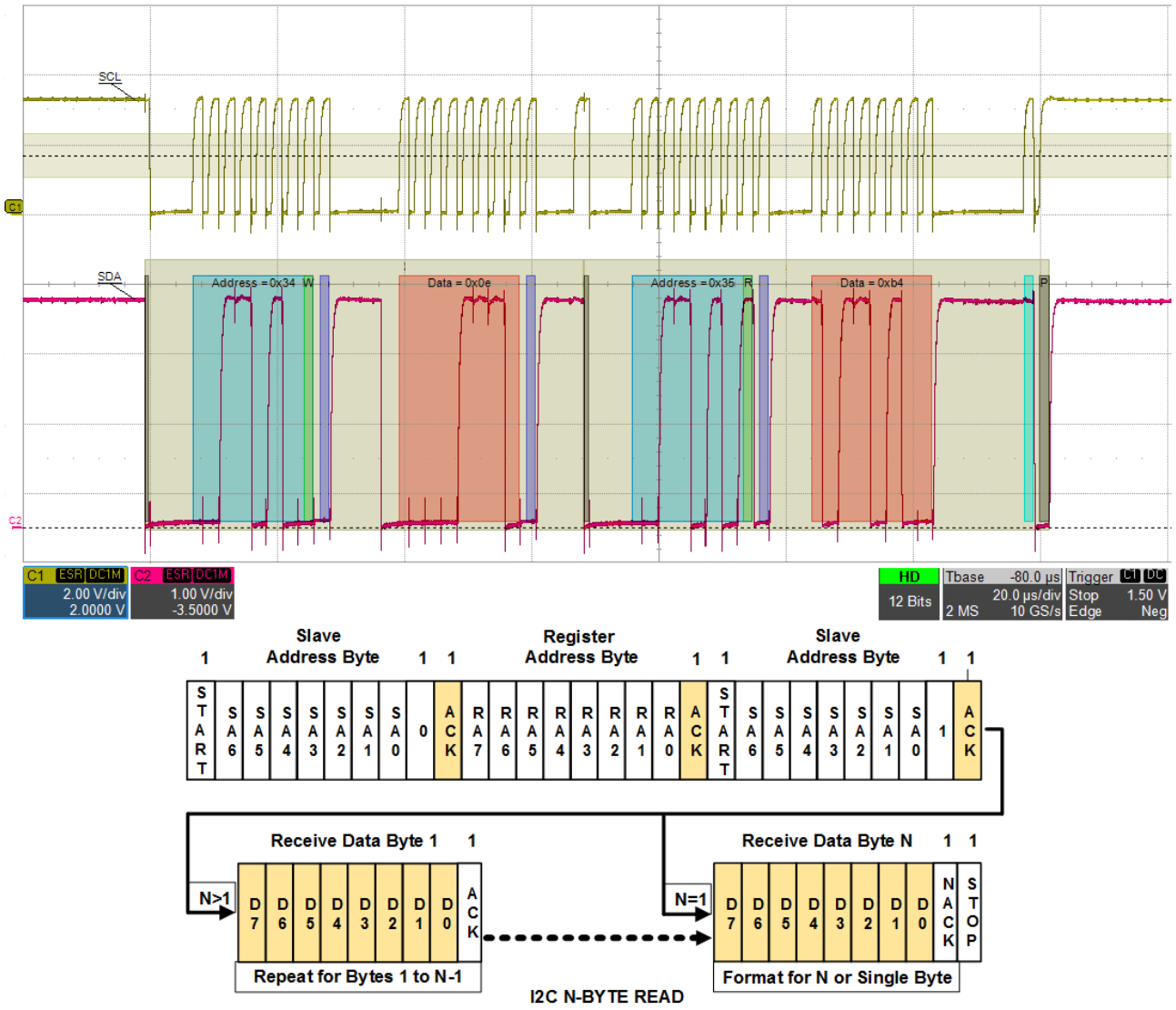


Figure 113. I²C Read Protocol

8.1.5 I²C Timing

I²C timing is illustrated in Figure 114, see specification table for specific values.

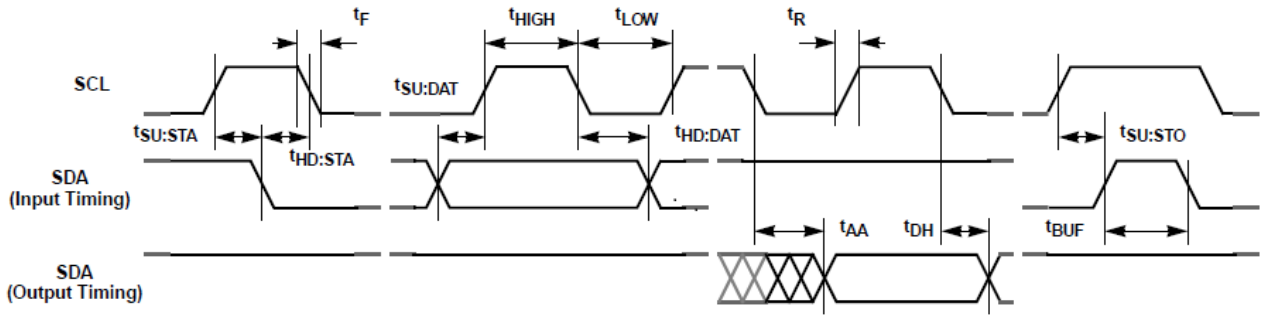


Figure 114. I²C Timing

8.2 SPI Serial Interface

The RAA489206 supports the SPI communication protocol. SPI has become a standard that does not have an officially released specification generated by any international committee. This gives some flexibility in implementing the SPI protocol but also requires programmable flexibility of the master microcontroller. This protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. The RAA489206 operates as a slave in all applications and all communication over the interface is conducted by sending the Most Significant Bit (MSB) of each byte first.

The RAA489206 is accessed through the MOSI (Master Output Slave Input) and SCL (Serial Clock) pins, and the output data is presented by the RAA489206 at the MISO (Master Input Slave Output) pin. Input data at pin MOSI is clocked in on the rising edge of SCL when $\overline{CS}$ is LOW. Output data at pin MISO is clocked out on the falling edge of SCL.

All commands start with a falling edge at the input pin $\overline{CS}$ and include the Identification, Register Address, and Data Bytes. Write operations end with a rising edge at the input pin $\overline{CS}$ after the last bit of the Data bytes being written is clocked in. Read operations end with a rising edge at the input pin $\overline{CS}$ after the last bit of the Data byte being read is clocked out.

Controlling the RAA489206 with a SPI interface is similar to I^2C in that the formats are comparable with the small differences. SPI requires the use of four data lines (SCL, MOSI, MISO, and $\overline{CS}$) for successful communication between master and slave. Unlike I^2C, SPI does not use ACK or NACK, START is replaced by the falling edge of $\overline{CS}$, and STOP is replaced by the rising edge of $\overline{CS}$.

The RAA489206 SPI interface has a maximum clock frequency of SPI_f_{SCL} (2Mhz). A time delay of SPI_t_{WAIT} (7µs) is required between bytes.

8.2.1 Identification Byte

The Identification byte is the first byte sent by the Master. It is a combination of the RAA489206 SPI Slave address and the Read/Write bit. The slave address is shifted left one bit while the R/W bit is the Least Significant Bit (LSB) of the Identification Byte (Figure 115).

8.2.1.1 CRC Disabled

To operate with CRC disabled, the Slave Address of the RAA489206 is 0x0A and the R/W bit is set to 1 for a Read or to 0 for a Write. When these are combined, the Identification byte is 0x15 for a Read (Figure 117) and 0x14 for a Write (Figure 115).

8.2.1.2 CRC Enabled

To operate with CRC enabled the Slave Address of the RAA489206 is 0x4E and the R/W bit is set to 1 for a Read or to 0 for a Write. When these are combined, the Identification byte is 0x9D for a Read and 0x9C for a Write (Figure 116) with CRC enabled.

8.2.2 Write Operation

Write Operation with CRC disabled is selected by setting the Read/Write bit in the Identification byte to 0 while using the slave address of 0x0A. On a write command with CRC disabled, the device transfers the Data byte to the register on the falling edge of the 24th (SCL) clock cycle. Figure 115 illustrates a single byte SPI Write sequence with CRC disabled.

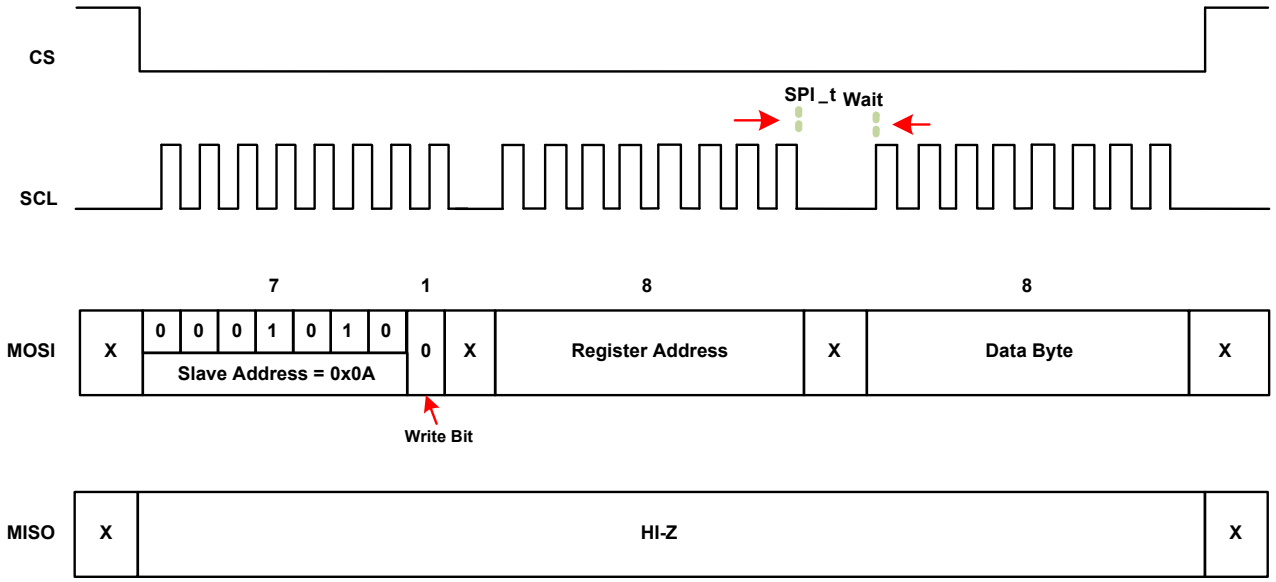


Figure 115. SPI Write

A single byte write operation with CRC enabled uses the slave address of 0x4E and requires two extra bytes for the 16-bit CRC word. Figure 116 is an example of a single byte write with CRC enabled. The CRC word is calculated by the Master from the Identification, Register Address and Data bytes. The MSB of the CRC word is transmitted first and the least significant byte follows it. See section CRC Calculation for details of CRC calculation.

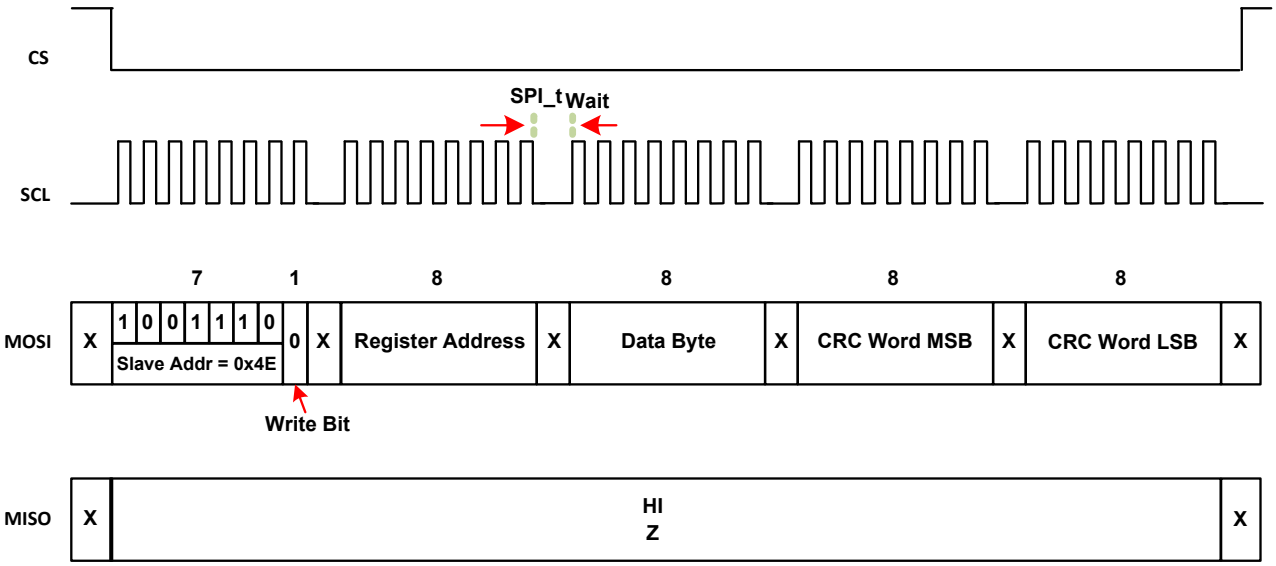


Figure 116. SPI Write w/CRC

8.2.3 Read Operation

Read Operation with CRC disabled is selected by setting the Read/Write bit in the Identification Byte to 1 while using the slave address of 0x0A. Figure 117 illustrates the SPI Read sequence with CRC disabled. The RAA489206 supports sequential read with CRC disabled by automatically incrementing the register address pointer to the next location.

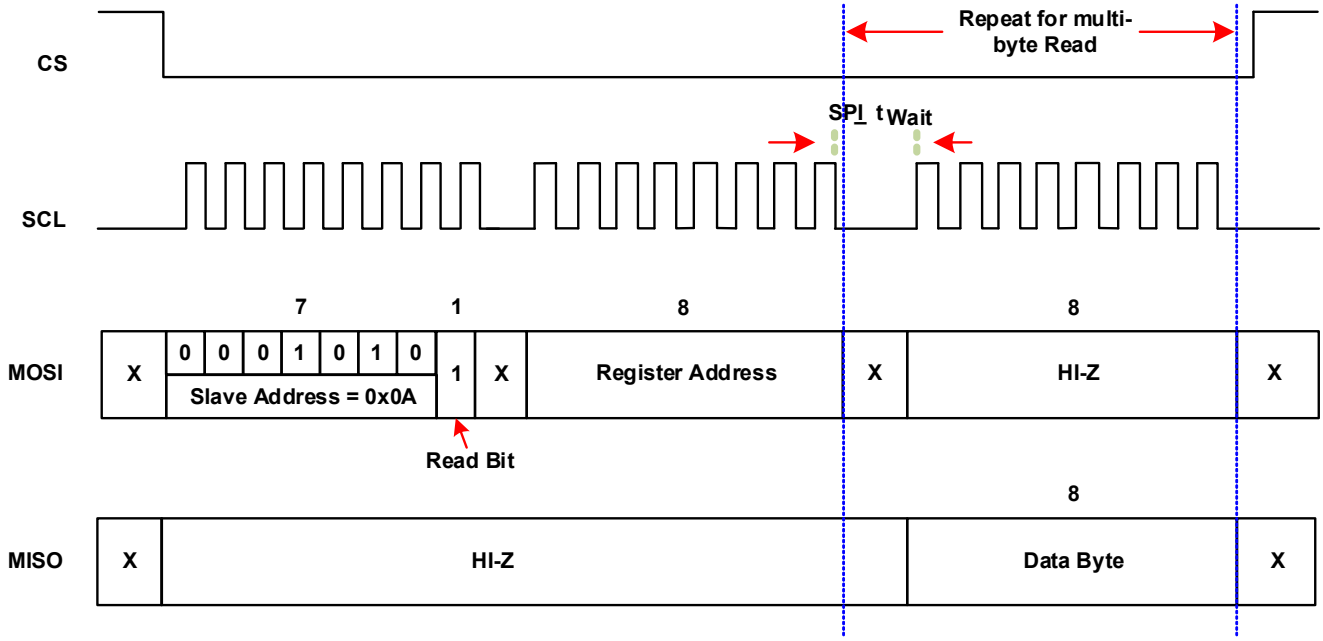


Figure 117. SPI Read

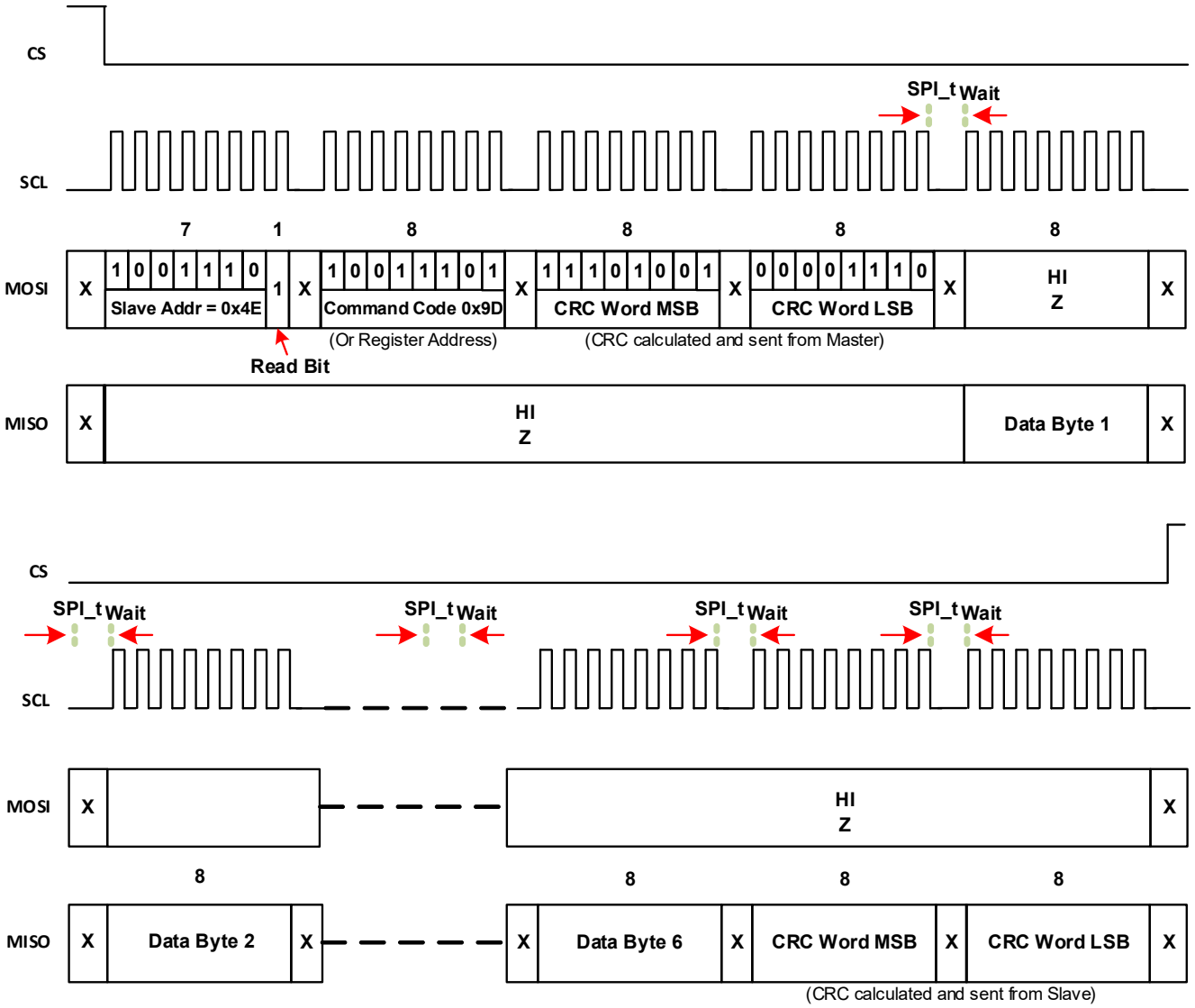
A read operation with CRC enabled uses the slave address of 0x4E and requires four bytes from the Master consisting of the Slave address with write bit (Identification Byte), an 8-bit address or command code byte and 2 bytes for the 16-bit CRC word. The read command CRC word is calculated by the Master from the Identification and Register Address (or command) bytes. If a register address is used, the Slave responds with one byte of register data and two bytes for the response 16-bit CRC word (calculated by the Slave).

The sequential read of multiple bytes with CRC enabled is supported by command codes used in place of the register address in the second byte sent by the Master. The supported command codes are listed in Table 78.

Table 78. CRC Read Command Codes

Read Registers	Command Code	Starting Address	Ending address	Byte Count
All Registers	0x9A	0x00	0x89	138
Measurement	0x9B	0x30	0x62	51
V_{CELL}	0x9C	0x30	0x51	34
I_{PACK}	0x9D	0x52	0x57	6
Other	0x9E	0x58	0x62	11
Faults	0x9F	0x63	0x69	7

Figure 118 is an example of a READ I_{PACK} command with CRC enabled. Again, the Master calculates and transmits the first CRC word based in the Identification and Command bytes while the Slave calculates and transmits the response CRC word based on the data it sends. If the Slave determines the read command CRC is incorrect, it sets fault bit 0x65.0 - CRCF and holds MISO high for the entire read back sequence until CS returns high, signaling the end of the sequence. A CRC of all 1s is an indication of a communications fault.



See section CRC Calculation, Example CRC VBA Code, and Example CRC C-Code for details on CRC calculation.

Figure 118. SPI I_{PACK} Read w/CRC

8.2.4 CRC Calculation

The RAA489206 CRC implementation is compliant with the CRC-CITT16 X25 protocol. See Example CRC VBA Code, Example CRC C-Code, and Figure 119 for calculation steps.

SPI Writes with CRC enabled include a 2-byte CRC word (Figure 116) calculated by the Master from the values of the first three bytes of the 5-byte sequence. SPI Reads are in the format of Figure 118 where the first CRC Word is calculated by the Master from the values of the first two bytes of the 4-byte MOSI sequence while the CRC Word at the end read sequence is calculated by the RAA489206 Slave based on the data it sent on MISO. In all three of these cases, it is the responsibility of the receiver to calculate the CRC value of the received bytes to compare with the received CRC and then act accordingly.

If the comparison for an SPI Write fails, the RAA489206 asserts fault bit 0x65.0 - CRCF and ignores the Write.

If the comparison for an SPI Read fails, the RAA489206 asserts fault bit 0x65.0 - CRCF and ignores the read. The RAA489206 holds MISO high until the Master releases CS. A CRC value of all 1's indicates a failure. If the Master determines the CRC comparison fails following the data read, it must determine the appropriate reaction.

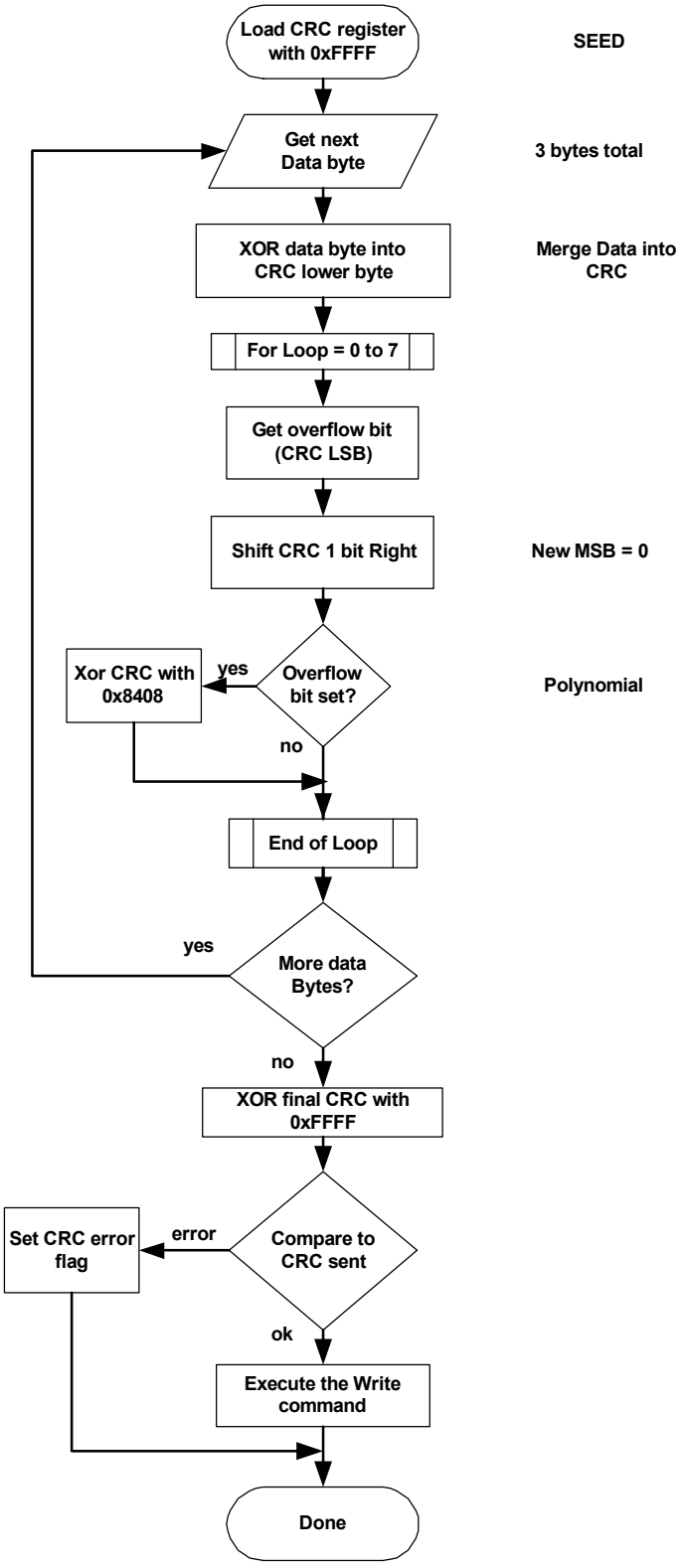


Figure 119. CRC Calculation Flowchart

8.2.4.1 Example CRC VBA Code

```
Example VBA code that calculates the CRC16-CITT-X25 checksum value (CRC word):
'*************************************************************************
Option Explicit
Public Function crcCheckValX25(ByVal buf As String) As Long
 '************************************************************************
 ' Equation is X16+X12+X5+1 or &H1021 (ignore X16)
 ' The X25 standard uses the CRC-CITT standard with the following conditions;
 '      The starting CRC value is 0xFFFF.
 '      The input bit stream is reflected.
 '      The output CRC is reflected.
 '      The final action is to XOR the value with 0xFFFF.
 ' Note: Reflecting the input data bits and the crc output bits is equivalent
 '      to reflecting the poly (0x1021 --> 0x8408) and shifting the CRC bits right as
opposed to left.
 '************************************************************************
 Dim NumBytes As Integer
 Dim DataStr As String
 Dim Databyte As Long
 Dim Bite As Byte
 Dim crc As Long
   If (Len(buf) Mod 2) <> 0 Then buf = "0" & buf      ' if excel drops leading zero
   If Len(buf) < 1 Then buf = "00"                   ' if no data
   NumBytes = Len(buf) \ 2
   crc = 65535                                    'Initializes the CRC to the seed
   Debug.Print "CCITT_X25 input " & buf & "  num bytes " & Str(NumBytes)
   For Bite = 0 To NumBytes - 1                     ' for each byte
      DataStr = Mid(buf, 2 * Bite + 1, 2)             'read next byte
      Databyte = CInt("&H" & DataStr)              'convert byte string to integer
      crc = (crc Xor Databyte) And 65535             ' XOR the data into lower 8 bits of
crc
      Debug.Print "  byte data " & Hex$(Databyte)
      Debug.Print "    byte crc " & Hex$(crc)
      crc = CRC16_X25(crc, &H8408)              ' shift the bits and XOR with polynomial
      crc = crc And 65535                          ' this keeps the CRC value in 16bit
format.
   Next Bite
   crc = (Not crc) And 65535                     ' XORing with 0xFFFF is the same as a
bit invert
   crcCheckValX25 = crc
End Function
Private Function CRC16_X25(ByVal crc As Long, polyVal As Long) As Long
 '************************************************************************
 ' Updates the CRC for each bit in the byte - reflected format
 '************************************************************************
 Dim i As Byte, XorFlag As Boolean, bit As Byte
  CRC16_X25 = crc
  For bit = 0 To 7                                 ' shift/XOR each bit in the byte
    XorFlag = False
    If (crc And &H1&) = 1 Then XorFlag = True       'LSB=1, need to xor with poly
    crc = (crc \ 2) And 65535                       ' shift right 1 bit
    Debug.Print "     shift " & Hex$(crc) & " " & Str$(XorFlag)
    If XorFlag Then crc = (crc Xor polyVal) And 65535      ' xor crc with poly
    Debug.Print "      bit crc " & Hex$(crc)
  Next bit
  CRC16_X25 = crc
  End Function
```

8.2.4.2 Example CRC C-Code

Example C code that calculates the CRC16-CITT-X25 checksum value (CRC word):

```
/*Calculates the CRC checksum for an array of bytes for RAA489206 Rev 0  03/21/19
Renesas Corp*/
#include <stdio.h>
void main()                                    // code to run the crc and print results
{
  int i;
  unsigned long int CRCval;                      // final checksum
  unsigned char INPUT_DATA[100];                // input array (uchar=1byte)
  int NumBytes;                                  // number of bytes to use
  NumBytes=3;
  INPUT_DATA[0] = 0x84;                         // fill in the input data
  INPUT_DATA[1] = 0xD0;
  INPUT_DATA[2] = 0x01;
  printf(" ---- RAA489206 CRC calculator ---- \n");
  printf("Number of Bytes   = %d    \n", NumBytes);
  printf("Input Data (hex)  = ");
  for(i=0; i<NumBytes; i++)  printf("%02x ", INPUT_DATA[i]);
  printf("\n");
  CRCval = Calc_CRC_94216(NumBytes, INPUT_DATA);         // find the CRC checksum
  printf("CRC16 final (hex) = %04x    \n", CRCval);
} //main
unsigned long int Calc_CRC_94216(int NumBytes, unsigned char *data)
{
// Call with input data array & NumBytes set, returns the final crc
// This code reflects the polynomial and shifts right instead of reflecting the data &
CRC (easier to code)
//                                standard X25       RAA489206 code
//  CRC_POLY             0x1201              0x8408
//  CRC_SEED             0xFFFF              0xFFFF
//  CRC_XOR              0xFFFF              0xFFFF
//  REFLECT_INPUT        TRUE                FALSE
//  REFLECT_OUTPUT       TRUE                FALSE
//  Byte XOR               MSB                 LSB
//  Bit Shift                Left                Right
//
  int i, j, XorFlag;
  unsigned long int CRCval;
   CRCval=0xFFFF;                                      // starting point = SEED
   for(i=0; i<NumBytes; i++)
     {
     CRCval = CRCval ^ long(data[i]);                      // XOR data with CRC
     for(j=0; j<8; j++)                                  // shift for each bit & check for
XOR
       {
       XorFlag=0;
              if(CRCval & 1)XorFlag=1;                           // LSB = Xor Flag
              CRCval=CRCval>>1;                                 // shift right 1 bit
              if(XorFlag>0) CRCval=CRCval ^ 0x8408;                 // XOR with poly
          } //for j
     } //for i
   CRCval=CRCval ^ 0xFFFF;                                 // xor the final crc
   return(CRCval);
} //Calc_
```

8.2.5 SPI Timing

SPI timing is illustrated in Figure 120 and Figure 121, see specification table for specific values. Symbol names listed in the specification tables include leading characters **SPI_**, which are omitted from the following figures for clarity.

Symbol t_{CS} is not specified because it is a function of the command sequence. Even though the device logic recognizes short t_{CS} pulse widths it cannot be expected to respond immediately with correct results if the preceding command has not completed execution. For example, a System Trigger command must be allowed to complete its task before attempting to read the results from a measurement register.

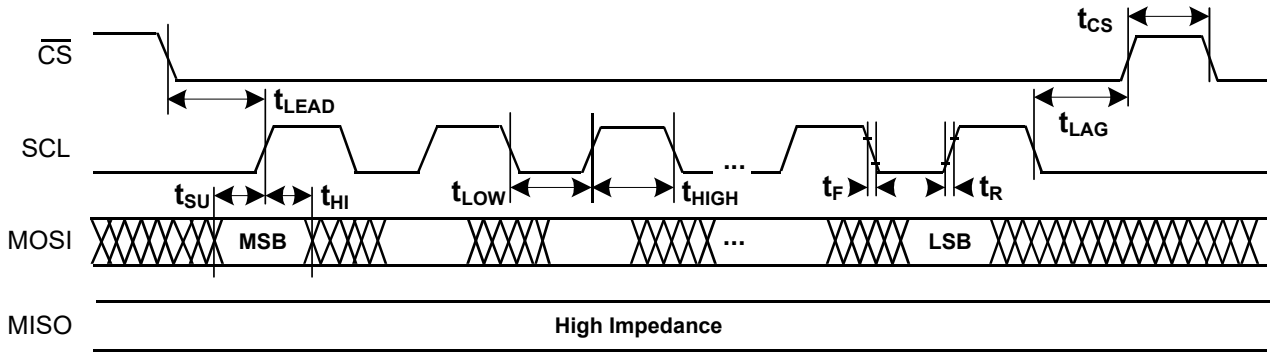


Figure 120. SPI Input Timing

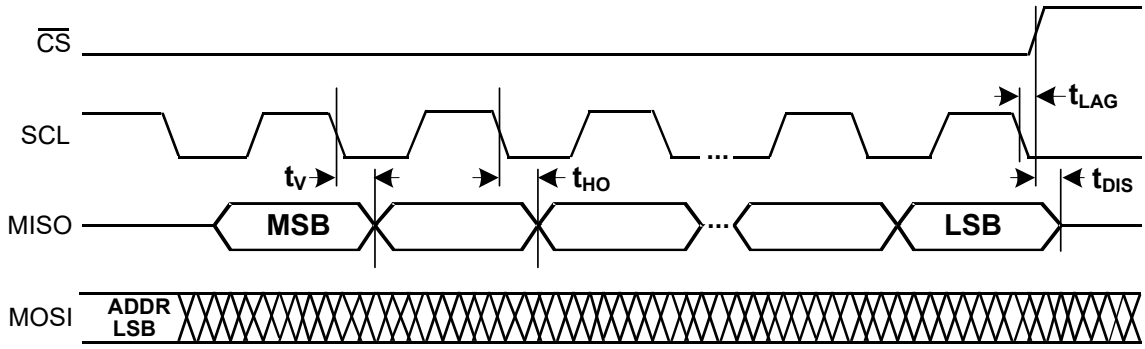


Figure 121. SPI Output Timing

9. Reduced Cell Count

The RAA489206 monitors between 4 and 16 cells. When using less than 16 cells, it is important that each used cell has a normal input circuit connection to the top and bottom monitoring inputs for that cell. The simplest way to use the RAA489206 with any number of cells is to always use the full input circuit arrangement for all VCn inputs, and short together the unused inputs at the battery terminal. In this way, each cell input sees a normal source impedance regardless of whether it is monitoring a cell.

The cell balancing components associated with unconnected cell inputs are not required and can be removed. Unused cell balance outputs should be tied to the cell voltage monitoring pin below it. For example, tie CB9 to VC8 in a 15-cell application.

The input circuit component count can be reduced in cases in which fewer than 14 cells are being monitored. It is important that cell inputs that are being used are not connected to other unused cell inputs, as this affects measurement accuracy.

See Figure 122 and the following table for connections with cell counts less than 16.

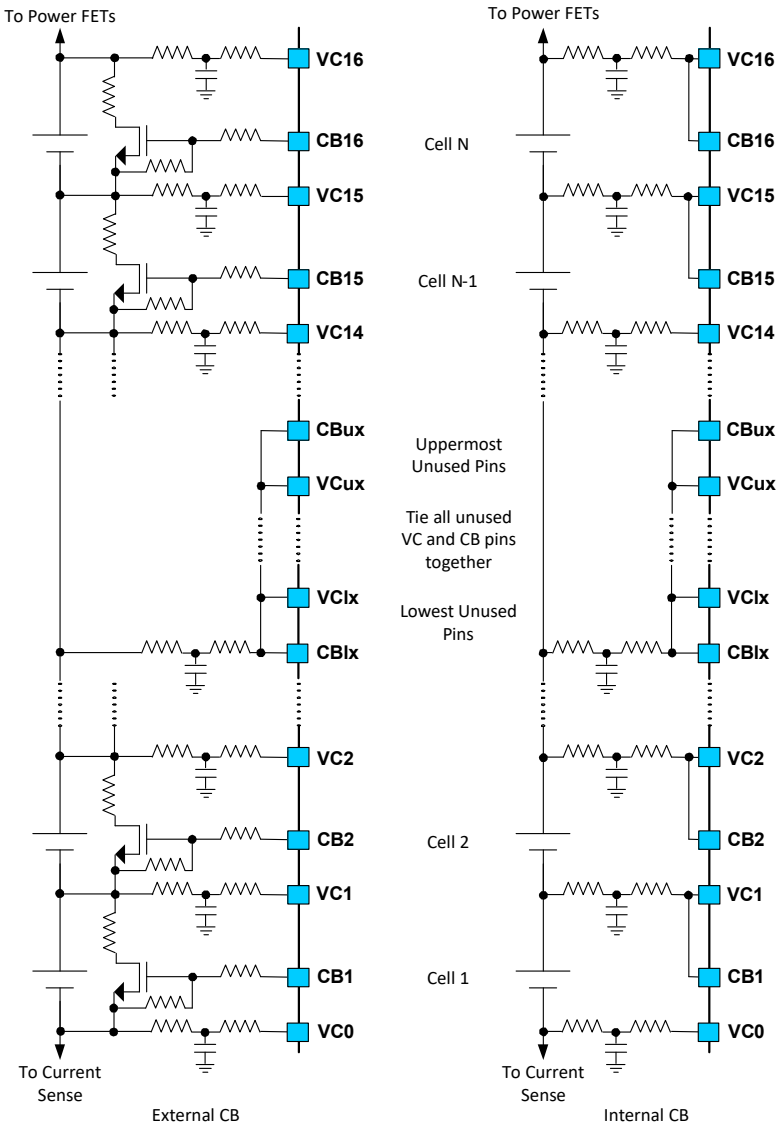


Figure 122. 4 to 14 Cell Count Example

Pin	Pos/Neg Cell Connection Versus Cell Count												
VC16	16	15	14	13	12	11	10	9	8	7	6	5	4
CB16													
VC15	15/16	14/15	13/14	12/13	11/12	10/11	9/10	8/9	7/8	6/7	5/6	4/5	3/4
CB15													
VC14	14/15	13/14	12/13	11/12	10/11	9/10	8/9	7/8	6/7	5/6	4/5	3/4	2/3
CB14												3/4	2/3
VC13	13/14	12/13	11/12	10/11	9/10	8/9	7/8	6/7	5/6	4/5	3/4	3/4	2/3
CB13										4/5	3/4	3/4	2/3
VC12	12/13	11/12	10/11	9/10	8/9	7/8	6/7	5/6	4/5	4/5	3/4	3/4	2/3
CB12								5/6	4/5	4/5	3/4	3/4	2/3
VC11	11/12	10/11	9/10	8/9	7/8	6/7	5/6	5/6	4/5	4/5	3/4	3/4	2/3
CB11						6/7	5/6	5/6	4/5	4/5	3/4	3/4	2/3
VC10	10/11	9/10	8/9	7/8	6/7	6/7	5/6	5/6	4/5	4/5	3/4	3/4	2/3
CB10				7/8	6/7	6/7	5/6	5/6	4/5	4/5	3/4	3/4	2/3
VC9	9/10	8/9	7/8	7/8	6/7	6/7	5/6	5/6	4/5	4/5	3/4	3/4	2/3
CB9		8/9	7/8	7/8	6/7	6/7	5/6	5/6	4/5	4/5	3/4	3/4	2/3
VC8	8/9	8/9	7/8	7/8	6/7	6/7	5/6	5/6	4/5	4/5	3/4	3/4	2/3
CB8			7/8	7/8	6/7	6/7	5/6	5/6	4/5	4/5	3/4	3/4	2/3
VC7	7/8	7/8	7/8	7/8	6/7	6/7	5/6	5/6	4/5	4/5	3/4	3/4	2/3
CB7					6/7	6/7	5/6	5/6	4/5	4/5	3/4	3/4	2/3
VC6	6/7	6/7	6/7	6/7	6/7	6/7	5/6	5/6	4/5	4/5	3/4	3/4	2/3
CB6							5/6	5/6	4/5	4/5	3/4	3/4	2/3
VC5	5/6	5/6	5/6	5/6	5/6	5/6	5/6	5/6	4/5	4/5	3/4	3/4	2/3
CB5									4/5	4/5	3/4	3/4	2/3
VC4	4/5	4/5	4/5	4/5	4/5	4/5	4/5	4/5	4/5	4/5	3/4	3/4	2/3
CB4											3/4	3/4	2/3
VC3	3/4	3/4	3/4	3/4	3/4	3/4	3/4	3/4	3/4	3/4	3/4	3/4	2/3
CB3													2/3
VC2	2/3	2/3	2/3	2/3	2/3	2/3	2/3	2/3	2/3	2/3	2/3	2/3	2/3
CB2													
VC1	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2	1/2
CB1													
VC0	1/CSP	1/CSP	1/CSP	1/CSP	1/CSP	1/CSP	1/CSP	1/CSP	1/CSP	1/CSP	1/CSP	1/CSP	1/CSP
Note	Tie these pins together then connect to cells through a single shared "T" network.												

Figure 123. Cell Count Matrix

Table 79. Reduced Cell Connect

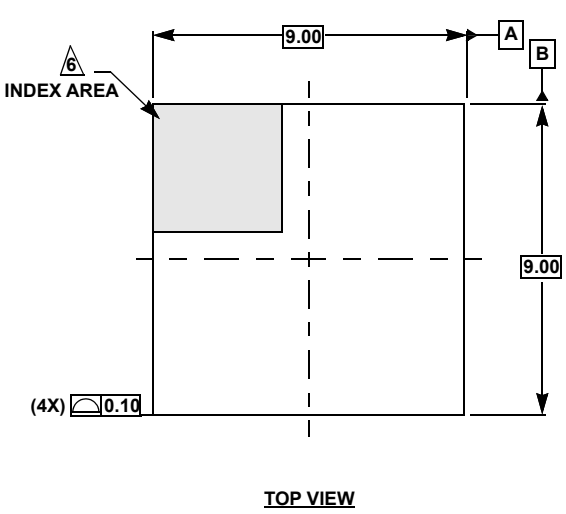
Pack Size	Skipped Inputs	Shorted VCn/CBn Pins	Cell Select Register Setting		
			Binary	Reg 0x04	Reg 0x05
15	VC9	VC8-VC9 and CB9	b 1111 1110 1111 1111	0xFE	0xFF
14	VC8-VC9	VC7-VC9 and CB8-CB9	b 1111 1110 0111 1111	0xFE	0x7F
13	VC8-VC10	VC7-VC10 and CB8-CB10	b 1111 1100 0111 1111	0xFC	0x7F
12	VC7-VC10	VC6-VC10 and CB7-CB10	b 1111 1100 0011 1111	0xFC	0x3F
11	VC7-VC11	VC6-VC11 and CB7-CB11	b 1111 1000 0011 1111	0xF8	0x3F
10	VC6-VC11	VC5-VC11 and CB6-CB11	b 1111 1000 0001 1111	0xF8	0x1F
9	VC6-VC12	VC5-VC12 and CB6- CB12	b 1111 0000 0001 1111	0xF0	0x1F
8	VC5-VC12	VC4-VC12 and CB5-CB12	b 1111 0000 0000 1111	0xF0	0x0F
7	VC5-VC13	VC4-VC13 and CB5-CB13	b 1110 0000 0000 1111	0xE0	0x0F
6	VC4-VC13	VC3-VC13 and CB4-CB13	b 1110 0000 0000 0111	0xE0	0x07
5	VC4-VC14	VC3-VC14 and CB4-CB14	b 1100 0000 0000 0111	0xC0	0x07
4	VC3-VC14	VC2-VC14 and CB3-CB14	b 1100 0000 0000 0011	0xC0	0x03

10. Package Outline Drawing

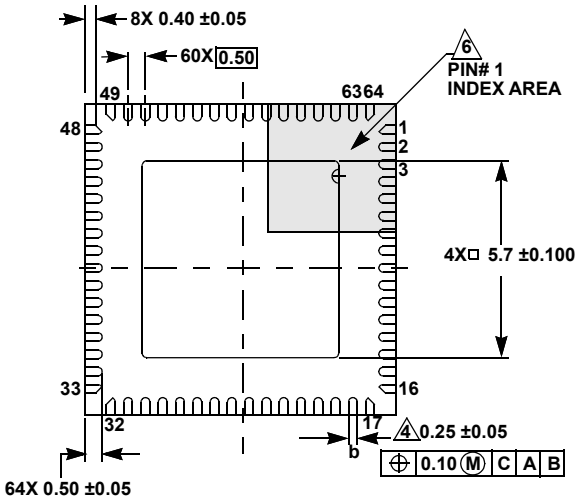
For the most recent package outline drawing, see L64.9x9B.

L64.9x9B

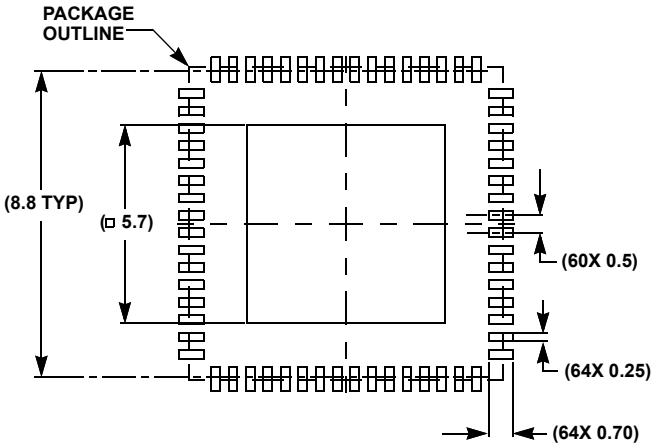
64 Lead Quad Flat No-Lead Plastic Package
Rev 1, 5/17



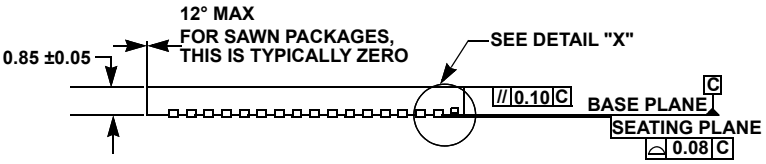
TOP VIEW



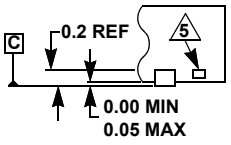
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension b applies to the metallized terminal and is measured between 0.20mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

11. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp Range
RAA4892062GNP#AA5	RAA489206 2GNP	64 Ld QFN	L64.9x9B	Tray	-40 to +85°C
RAA4892062GNP#HA5				Reel, 3k	
RAA4892062GNP#MA5				Reel, 1k	
RTKA489206DK0000BU	Evaluation Kit				

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak re-flow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA489206 product information page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

Table 80. Key Differences Between Family of Parts

Part Number	Cells Supported		Pack Voltage (Op)		Cell Bal.	I_{SENSE}	Charge/Discharge FET			Supply Current (Typ)		Stand-Alone Capable	Int. ADC	Daisy Chain
	Min	Max	Min (V)	Max (V)			Control	Arrangement	Location	Normal	Sleep (µA)			
RAA489206	4	16	12	59	Both	Low Side	Yes	Both	Both[1]	200µA	10	No	16b	No
RAA489204	6	14	12	65	Int./ Ext.	No	No	No	No	3.3mA	19	No	14b	Yes
ISL94212	6	12	6	60	Ext.	No	No	N/A	N/A	3.31mA	12	No	14b	Yes
ISL94216A	4	16	12	55	Both	Low Side	Yes	Both	Both[1]	200µA	10	No	16b	No
ISL94208	4	6	8	26.4	Both	Low Side	Yes	Both	Low Side	850µA	2	No	No	No
ISL94202	3	8	4	36	Ext.	High Side	Yes	Both	High Side	348µA	13	State Machine	14b	No
RAJ240100	3	10	4	50	Int.	Low Side	Yes	Both	High Side	50µA	1	Int MCU	15b/ 18b	No
RAJ240090	3	8	4	50	Int.	Low Side	Yes	Both	High Side	50µA	1	Int MCU	15b/ 18b	No
RAJ240080	2	5	4	25	Both	Low Side	Yes	Both	High Side	50µA	1	Int MCU	15b/ 18b	No

1. GPIO can be configured to support low-side C/DFETs.

12. Revision History

Rev.	Date	Description
2.02	Mar 21, 2025	Page 36, Register0x2B and 0x2D corrected the range value to 18.79mV. Updated the last paragraph in Section 5.2.1.7. Updated the last sentence in Section 5.13.7.7. Updated Figures 117 and 118. Added Table 79.
2.01	Oct 3, 2024	Changed parameter name from Charge Pump External Current Load Capacity to Charge Pump Peak Current and changed the symbol from Ipmp to ISC.
2.00	Jul 5, 2022	Updated Figure 1. In section 3.3, updated the following: ▪ Changed the VBAT1, VBAT2 Charge Pump Enabled maximum spec from 55 to 59. ▪ Removed the DFET, CFET, VCP row. In section 3.4, updated the following: ▪ Increased VBAT Voltage Range Max from 55V to 59V. ▪ Corrected Typo, moved Slave Access Time max of 200ns to min of 200ns, no max. In section 5.3.1.5, updated last sentence of the first paragraph. In section 5.4.1, corrected the typo by changing from 4801V to 4.801V. In section 5.12.4, changed maximum to minimum in the last sentence of the second paragraph. In section 5.12.5, changed CBMAXstep to CBMINstep in Table 51. Also changed minimum to maximum in the last sentence of the second paragraph. In section 5.12.8.2, deleted ...in IDLE mode following a manual CB or... from the 3rd sentence. In section 7.2.5, changed from CELLCON AND {DVCF OR (NOT[DCHRWUV] AND UVF) OR (NOT[CHRWUV] AND OVF)} to CELLCON AND {DVCF OR (NOT[CHRWUV] AND UVF) OR (NOT[DCHRWOV] AND OVF)} to correct typos. In section 7.4.2.1, inserted (0x01.1 - Scan Select must be set to 1 for single scan) in the first sentence of item 1. In section 11 table 79, updated the following: ▪ Changed RAA489206 Max Pack Voltage from 55 to 59 ▪ Changed ISL94216 to ISL94216A ▪ Added RAA489204 to the table.
1.01	Feb 3, 2022	Updated the default value in Table 52. Updated the Manual Cell Balancing section.l
1.00	Jun 21, 2021	Initial release

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