EFR32BG27 Wireless Gecko SoC Family Data Sheet

The EFR32BG27 Wireless Gecko family of SoCs is part of the Wireless Gecko portfolio. EFR32BG27 Wireless Gecko SoCs are ideal for enabling energy-friendly Bluetooth 5.x networking for IoT devices.

The single-die solution combines a 76.8 MHz Cortex-M33 with a high performance 2.4 GHz radio to provide an industry-leading, energy efficient wireless, SoC for IoT connected applications.

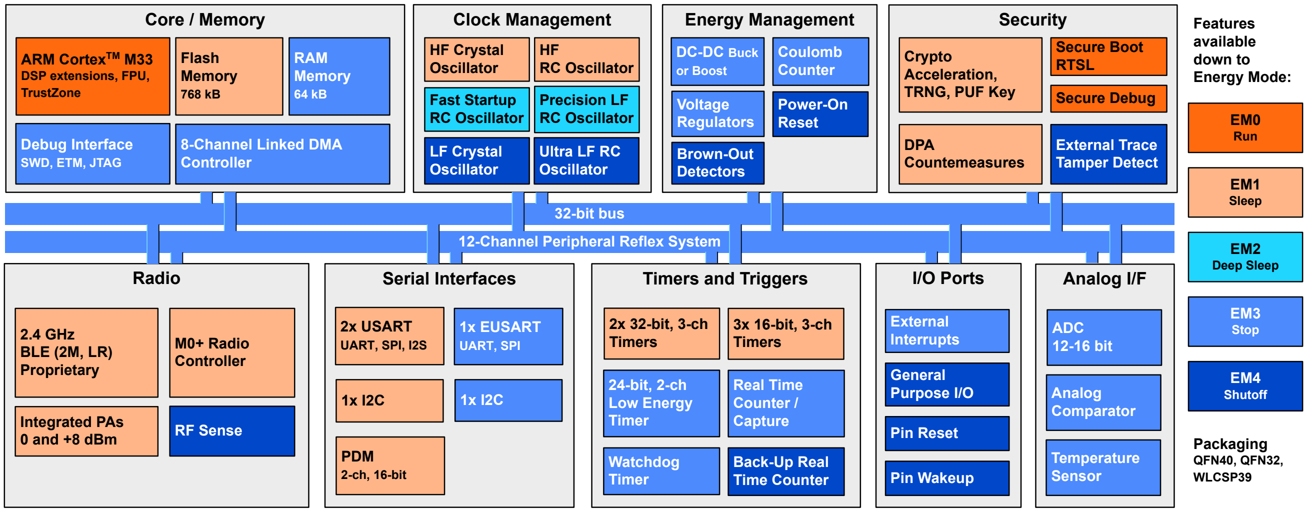
The devices are available with boost or buck DC-DC capabilities, enabling direct power from a wide variety of batteries.

Wireless Gecko applications include:

- Portable Medical
- Home End Devices
- Fleet/Asset Monitoring
- Industrial Automation
- Access Control
- Bluetooth Mesh
- Sports, Fitness, and Wellness devices
- Power Tools

KEY FEATURES

- 32-bit ARM® Cortex®-M33 core with 76.8 MHz maximum operating frequency
- 768 kB of flash and 64 kB of RAM
- Energy-efficient radio core with low active and sleep currents
- Integrated PA with up to 8 dBm (2.4 GHz) TX power
- Secure Boot with Root of Trust and Secure Loader (RTSL)
- Pin compatibility / feature superset with EFR32xG22 in QFN
- DC-DC supporting buck (1.8-3.8 V) or boost (0.8 - 1.7 V) operation
- Available in WLCSP and QFN packaging



1. Feature List

The EFR32BG27 highlighted features are listed below.

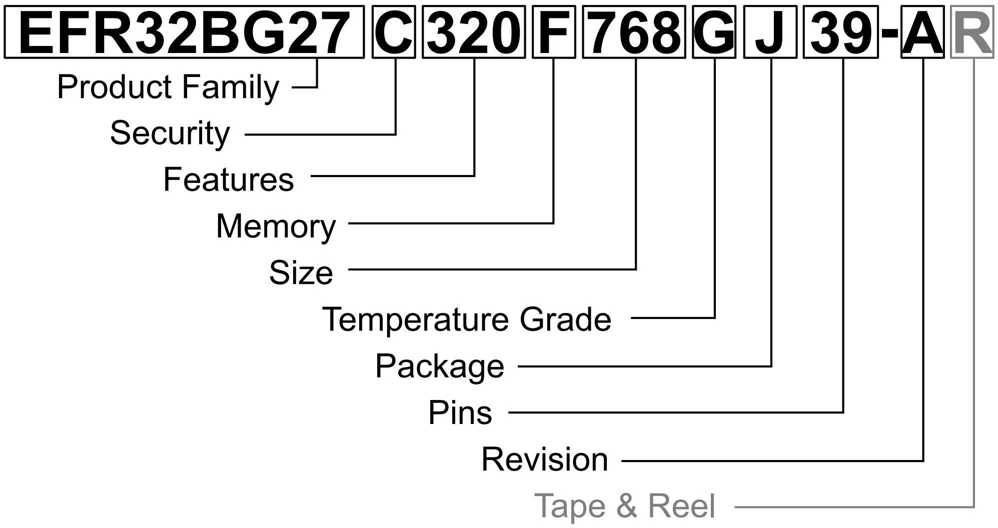
- **Low Power Wireless System-on-Chip**
  - High Performance 32-bit 76.8 MHz MHz ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
  - 768 kB flash program memory
  - 64 kB RAM data memory
  - 2.4 GHz radio operation
- **Radio Performance**
  - -106.9 dBm sensitivity @ 125 kbps GFSK
  - -99.2 dBm sensitivity @ 1 Mbit/s GFSK
  - -96.3 dBm sensitivity @ 2 Mbit/s GFSK
  - TX power up to 8 dBm
- **Low System Energy Consumption**
  - 3.6 mA RX current (1 Mbps GFSK)
  - 4.1 mA TX current @ 0 dBm output power
  - 9.2 mA TX current @ 6 dBm output power
  - 11.3 mA TX current @ 8 dBm output power
  - 29 μA/MHz in Active Mode (EM0) at 76.8 MHz
  - 1.6 μA EM2 DeepSleep current (64 kB RAM retention and RTC running from LFXO)
  - 0.18 μA EM4 current
- **Supported Modulation Format**
  - 2 (G)FSK with fully configurable shaping
  - OQPSK DSSS
  - (G)MSK
- **Protocol Support**
  - Bluetooth Low Energy (Bluetooth 5.x)
  - Proprietary
- **Security Features**
  - Secure Boot with Root of Trust and Secure Loader (RTSL)
  - Hardware Cryptographic Acceleration for AES128/256, SHA-1, SHA-2 (up to 256-bit), ECC (up to 256-bit), ECDSA, and ECDH
  - DPA Countermeasures
  - Key Management with PUF
  - True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
  - ARM® TrustZone®
  - Secure Debug with lock/unlock
  - External Tamper Detect
- **Wide selection of MCU peripherals**
  - Analog to Digital Converter (ADC)
    - 12-bit @ 1 Msps
    - 16-bit @ 76.9 ksps
  - Analog Comparator (ACMP)
  - Up to 26 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 2 × 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 3 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter
  - 24-bit Low Energy Timer for waveform generation
  - 1 × Watchdog Timer
  - 2 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - 1 × Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI)
  - 2 × I^2C interface with SMBus support
  - Digital microphone interface (PDM)
  - Precision Low-Frequency RC Oscillator to replace 32 kHz sleep crystal
  - RFSENSE with selective OOK mode
  - Die temperature sensor with +/-1.5 degree C accuracy after single-point calibration
  - Coulomb counter integrated into DC-DC
- **Wide Operating Range**
  - 1.8 V to 3.8 V single power supply for devices with Buck DC-DC
  - 0.8 V to 1.7 V single power supply for devices with Boost DC-DC
  - -40 °C to 125 °C
- **Packages**
  - **QFN40** 5 mm × 5 mm × 0.85 mm, 0.4 mm pitch
  - **QFN32** 4 mm × 4 mm × 0.85 mm, 0.4 mm pitch
  - **WLCSP39** 2.291 mm × 2.624 mm × 0.5 mm, 0.35 mm pitch

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Max TX Power	DC-DC	Flash (KB)	RAM (KB)	GPIO	Package	Temp Range
EFR32BG27C320F768IJ39-B	• Bluetooth 5.x • Direction Finding (AoA Transmitter) • Proprietary	4 dBm	Buck or Boost	768	64	19	WLCSP39	-40 to 125 °C
EFR32BG27C320F768GJ39-B	• Bluetooth 5.x • Direction Finding (AoA Transmitter) • Proprietary	4 dBm	Buck or Boost	768	64	19	WLCSP39	-40 to 85 °C
EFR32BG27C230F768IM40-B	• Bluetooth 5.x • Direction Finding (AoA Transmitter) • Proprietary	6 dBm	Boost	768	64	25	QFN40	-40 to 125 °C
EFR32BG27C230F768IM32-B	• Bluetooth 5.x • Direction Finding (AoA Transmitter) • Proprietary	6 dBm	Boost	768	64	17	QFN32	-40 to 125 °C
EFR32BG27C140F768IM40-B	• Bluetooth 5.x • Direction Finding (AoA Transmitter) • Proprietary	8 dBm	Buck	768	64	26	QFN40	-40 to 125 °C
EFR32BG27C140F768IM32-B	• Bluetooth 5.x • Direction Finding (AoA Transmitter) • Proprietary	8 dBm	Buck	768	64	18	QFN32	-40 to 125 °C

Bluetooth 5.x: As the Bluetooth standard evolves, Silicon Labs is regularly adding new features. For more information on supported Bluetooth capabilities, visit https://www.silabs.com/bluetooth-hardware.



Field	Options
Product Family	• **EFR32BG27**: Wireless Gecko BG27 Family
Security	• **C**: Secure Vault Mid

Features [f1][f2][f3]	• **f1**
	  • 1: DC-DC Buck Converter
	  • 2: DC-DC Boost Converter
	  • 3: DC-DC Buck or Boost Converter
	• **f2**
	  • 2: 4 dBm PA Transmit Power
	  • 3: 6 dBm PA Transmit Power
	  • 4: 8 dBm PA Transmit Power
	• **f3**
	  • 0: Unused

Memory	• **F**: Flash
Size	• **Memory Size** in kBytes
Temperature Grade	• **G**: -40 to +85 °C • **I**: -40 to +125 °C
Package	• **M**: QFN • **J**: WLCSP
Pins	• **Number of Package Pins**
Revision	• **A**: Revision A • **B**: Revision B
Tape & Reel	• **R**: Tape & Reel (optional)

Figure 2.1. Ordering Code Key

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3. System Overview

3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a high performance radio transceiver. The devices are well suited for secure connected IoT multi-protocol devices requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. A detailed functional description will be available in the EFR32xG27 Reference Manual.

3.2 Radio

The EFR32BG27 Wireless Gecko features a highly configurable radio transceiver supporting the Bluetooth Low Energy wireless protocol.

3.2.1 Antenna Interface

The 2.4 GHz antenna interface consists of a single-ended pin (RF2G4_IO). The external components for the antenna interface in typical applications are shown in the 5.2 RF Matching Networks section.

3.2.2 Fractional-N Frequency Synthesizer

The EFR32BG27 contains a high-performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency for the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides phase noise performance, frequency resolution better than 100 Hz, and low energy consumption. The synthesizer's fast frequency settling allows for very short receiver and transmitter wake up times to reduce system energy consumption.

3.2.3 Receiver Architecture

The EFR32BG27 uses a low-IF receiver architecture, which consists of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer. The I/Q signals are further filtered and amplified before being sampled by the IF Analog-to-Digital Converter (IFADC).

The IF frequency is configurable from 150 to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The 2.4 GHz radio is calibrated at production to improve image-rejection performance.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high-quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, level-based proximity detection, and RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

3.2.4 Transmitter Architecture

The EFR32BG27 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

The EFR32BG27 automatically times Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) and LBT algorithms. Regulatory standards typically define these algorithms to improve interoperability within a given bandwidth for devices that don't share synchronized RF channel access.

3.2.5 Packet and State Trace

The EFR32BG27 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data, and state information
- Data observability on a single-pin UART data output or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data, and state / meta information in a single serial data stream

3.2.6 Data Buffering

The EFR32BG27 features an advanced Radio Buffer Controller (BUFC) capable of handling up to four buffers of adjustable size from 64 to 4096 bytes. Each buffer can be used for RX, TX, or both. The buffer data is located in RAM, enabling zero-copy operations.

3.2.7 Radio Controller (RAC)

The RAC controls the top-level state of the radio subsystem in the EFR32BG27. It performs the following tasks:

- Precisely timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter, and frequency synthesizer
- Detailed frame transmission timing with optional LBT or CSMA-CA

3.2.8 RFSENSE Interface

The RFSENSE block allows the device to remain in EM2, EM3, or EM4 and wake when RF energy above a specified threshold is detected. When operated in selective mode, the RFSENSE block performs OOK preamble and sync word detection, preventing false wake-up events.

3.3 General Purpose Input/Output (GPIO)

EFR32BG27 supports up to 26 GPIO pins. Each GPIO pin is individually configurable as an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering are configurable on a per-pin basis. Peripheral connections can override the GPIO pins, and each peripheral connection is routeable to several GPIO pins on the device. GPIO inputs can be routed through the Peripheral Reflex System (PRS) to other peripherals. The GPIO subsystem also supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2-capable and can be used by low-energy peripherals in EM2 and EM3. These pins can also wake the device from EM2 or EM3. Pins on ports C and D retain their current state when entering EM2 until the device exits EM2, at which point internal peripherals can drive them again.

Some GPIO pins also support wake functionality down to EM4. These pins are listed in the Alternate Function Table with the function GPIO.EM4WU.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The CMU controls oscillators and clocks in the EFR32BG27. The CMU also enables and disables all peripheral module clocks. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFR32BG27 supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. The HFXO provides excellent RF clocking performance using a 38.4 MHz crystal. The HFXO can also support an external clock source such as a TCXO for applications that require an extremely accurate clock frequency over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast start-up at minimal energy consumption combined with a wide frequency range, from 1 MHz to 76.8 MHz.
- An integrated fast start-up RC oscillator (FSRCO) that runs at a fixed 20 MHz
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low power operation without an external crystal. Precision mode enables periodic recalibration against the 38.4 MHz HFXO crystal to improve accuracy to +/- 500 ppm, suitable for BLE sleep interval timing.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the Peripheral Reflex System (PRS). The core of each TIMER is a 16-bit or 32-bit counter with up to three compare/capture channels. Each channel is configurable in one of three modes:

- In capture mode, the counter state is stored in a buffer at a selected input event.
- In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value.
- In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers.

Complementary outputs with dead-time insertion are available on select TIMER output channels.

For information on the feature set of each timer, see 3.13 Configuration Summary

3.5.2 Low-Energy Timer (LETIMER)

The LETIMER is a 24-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. It supports timing and output generation when most of the device is powered down, allowing simple tasks to be performed while keeping system power consumption to a minimum. The LETIMER can generate a range of waveforms with minimal software involvement. The LETIMER is connected to the Peripheral Reflex System (PRS) and can start counting based on compare matches from other peripherals, such as the Real Time Clock.

3.5.3 Real Time Clock with Capture (RTCC)

The RTCC is a 32-bit counter that provides timekeeping down to EM3. The RTCC can be clocked by any of the on-board, low-frequency oscillators, and it is capable of providing system wake-up at user-defined intervals.

A secondary RTC is used by the RF protocol stack for event scheduling, leaving the primary RTCC block available exclusively for application software.

3.5.4 Back-Up Real Time Counter (BURTC)

The Back-Up Real Time Counter (BURTC) is a 32-bit counter providing timekeeping in all energy modes, including EM4. The BURTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user-defined intervals.

3.5.5 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog and as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by the Peripheral Reflex System (PRS).

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The USART is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire, and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.6.2 Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)

The EUSART supports full duplex asynchronous UART communication with hardware flow control, RS-485, and IrDA support. The EUSART also supports high-speed SPI. In EM0 and EM1, the EUSART provides a high-speed, buffered communication interface.

When routed to GPIO ports A or B, the EUSART0 may also be used in a low-energy mode and operate in EM2. A 32.768 kHz clock source allows full duplex UART communication up to 9600 baud. EUSART0 can also act as a SPI secondary device in EM2 and EM3, and wake the system when data is received from an external bus controller.

3.6.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as a main or secondary interface and supports multi-drop buses. Standard-mode, fast-mode, and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Bus arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of addresses is provided in active and low-energy modes. Not all instances of I^2C are available in all energy modes.

3.6.4 Peripheral Reflex System (PRS)

The PRS provides a communication network between different peripheral modules without software involvement. Peripheral modules producing reflex signals are called producers. The PRS routes reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality, such as simple logic operations (AND, OR, NOT), can be applied by the PRS to the signals. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

3.6.5 Pulse Density Modulation (PDM) Interface

The PDM module provides a serial interface and decimation filter for Pulse Density Modulation (PDM) microphones, isolated Sigma-delta ADCs, digital sensors, and other PDM or sigma delta bit stream peripherals. A programmable Cascaded Integrator Comb (CIC) filter is used to decimate the incoming bit streams. PDM supports stereo or mono input data and DMA transfer.

3.7 Security Features

The EFR32BG27 supports the following extended Secure Vault Mid features:

Table 3.1. Secure Vault Features

Feature	Secure Vault Mid
True Random Number Generator (TRNG)	Yes
Secure Boot with Root of Trust and Secure Loader (RTSL)	Yes
Secure Debug with Lock/Unlock	Yes
DPA Countermeasures	Yes
Anti-Tamper	External Tamper (ETAMPDET)
Secure Attestation	Using TrustZone
Secure Key Management	Using TrustZone
Symmetric Encryption	• AES 128 / 192 / 256 bit • ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC
Public Key Encryption - ECDSA / ECDH / EdDSA	• p192 and p256
Key Derivation	• ECJ-PAKE p192 and p256
Hashes	• SHA-1 • SHA-2/256

3.7.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed, and protects Over-The-Air (OTA) updates.

For more information about this feature, see AN1218: Series 2 Secure Boot with RTSL.

3.7.2 Cryptographic Accelerator

The Cryptographic Accelerator in Secure Element is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, Elliptic Curve Cryptography (ECC) to support public key operations and hashes.

Supported block cipher modes of operation for AES include:

- ECB (Electronic Code Book)
- CTR (Counter Mode)
- CBC (Cipher Block Chaining)
- CFB (Cipher Feedback)
- GCM (Galois Counter Mode)
- CBC-MAC (Cipher Block Chaining Message Authentication Code)
- GMAC (Galois Message Authentication Code)
- CCM (Counter with CBC-MAC)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the NIST (National Institute of Standards and Technology) recommended curves including P-192 and P-256 for ECDH(Elliptic Curve Diffie-Hellman) key derivation and ECDSA (Elliptic Curve Digital Signature Algorithm) sign and verify operations.

Supported hashes include SHA-1, SHA2/224, and SHA-2/256.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

Note: AES_ECB, AES_CBC, AES_CBCMAC, and SHA-1 are provided for legacy compatibility and are not recommended for cryptographic purposes without thoroughly understanding their potential security weaknesses.

3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31, as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.7.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

In addition, the EFR32BG27 also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

More information on this feature can be found in AN1190: Series 2 Secure Debug.

3.7.5 External Tamper Detection (ETAMPDET)

The ETAMPDET module enables detection of external tampering, such as unauthorized enclosure opening. ETAMPDET operates in all energy modes down to EM4. Up to two signals can be generated and monitored to identify external tamper events. When a tamper event occurs, an interrupt is generated to allow software to take system-appropriate actions.

3.8 Analog

3.8.1 Analog to Digital Converter (IADC)

The IADC is a hybrid architecture combining techniques from both SAR and Delta-Sigma style converters. It has a resolution of 12 bits at 1 Msps and 16 bits at up to 76.9 ksps. Hardware oversampling reduces system-level noise by averaging multiple front-end samples. The IADC also integrates voltage reference options and can operate in either single-ended or differential mode, with inputs selected from a wide range of internal and external sources.

3.8.2 Analog Comparator (ACMP)

The ACMP compares the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally programmable reference sources. The ACMP can also monitor the supply voltage and generate an interrupt when the supply falls below or rises above the programmable threshold.

3.9 Power

The EFR32BG27 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. Devices are available with an integrated DC-DC buck or DC-DC boost regulator to generate a stable 1.8 V from a wide variety of batteries. If used in an application, the DC-DC regulator requires one external inductor and one external capacitor.

The EFR32BG27 device family includes support for internal supply voltage scaling, as well as two different power domains groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

3.9.1 Energy Management Unit (EMU)

The EMU manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also implement system-wide voltage scaling and turn off the power to unused RAM blocks to optimize the energy consumption in the target application. The DC-DC regulator operation is tightly integrated with the EMU.

3.9.2 Voltage Scaling

The EFR32BG27 supports supply voltage scaling for the regulator powering DECOUPLE, with independent selections for EM0 / EM1 and EM2 / EM3. Voltage scaling helps to optimize the energy efficiency of the system by operating at lower voltages when possible. The EM0 / EM1 voltage scaling level defaults to VSCALE2, which allows the core to operate in active mode at full speed. The intermediate level, VSCALE1, allows operation in EM0 and EM1 at up to 40 MHz. The lowest level, VSCALE0, can conserve power further in EM2 and EM3. The EMU will automatically switch the target voltage scaling level when transitioning between energy modes.

3.9.3 Buck or Boost DC-DC Converter

The device family has a buck or boost DC-DC converter to provide a 1.8 V supply voltage for the device. The DC-DC converter covers a wide range of load currents, providing high efficiency in energy modes EM0, EM1, EM2 and EM3 for device and radio operation.

RF noise mitigation allows operation of the DC-DC converter without significantly degrading sensitivity of radio components. It employs soft switching at boot and DC-DC regulating-to-bypass transitions to limit the max supply slew rate and mitigate inrush current.

The buck DC-DC configuration provides up to 60 mA output current from a 2.2 - 3.8 V supply in energy modes EM0, EM1, EM2, and EM3. An on-chip supply-monitor signals when the supply voltage is low to allow bypass of the regulator, and extend the operating range down to 1.8 V. In bypass mode, the DC-DC operation is shut down and the input supply is switched directly to the output. The bypass mode of the buck DC-DC may be enabled to allow the system to go into EM4 and save energy.

The boost DC-DC configuration has an input range of 0.8 to 1.7 V and up to 25 mA output current, enabling operation directly from single-cell Silver Oxide, Alkaline, or other low-voltage battery chemistry. The boost DC-DC converter is operational in energy modes EM0, EM1, EM2,and EM3. It can be completely shut down using the dedicated BOOST_EN pin, saving system power during storage and shipping. BOOST_EN may also be used to re-enable the boost converter and power up the system.

3.9.4 Power Domains

Peripherals may exist on one of several independent power domains which are powered down to minimize supply current when not in use. Power domains are managed automatically by the EMU.

The lowest-energy power domain is the "high-voltage" power domain (PDHV), which supports extremely low-energy infrastructure and peripherals. Circuits powered from PDHV are always on and available in all energy modes down to EM4.

The next power domain is the low power domain (PD0), which is further divided to power subsets of peripherals. All PD0 power domains are shut down in EM4. Circuits powered from PD0 power domains may be available in EM0, EM1, EM2, and EM3.

Low power domain A (PD0A) is the base power domain for EM2 and EM3 and will always remain on in EM0-EM3. It powers the most commonly-used EM2 and EM3-capable peripherals and infrastructure required to operate in EM2 and EM3. Auxiliary PD0 power domains (PD0B, PD0C) power additional EM2 and EM3-capable peripherals on demand. If any peripherals on one of the auxiliary power domains is enabled, that power domain will be active in EM2 and EM3. Otherwise, the auxiliary PD0 power domains will be shut down to reduce current.

The active power domain (PD1) powers the rest of the device circuitry, including the CPU core and EM0 / EM1 peripherals. PD1 is always powered on in EM0 and EM1. PD1 is always shut down in EM2, EM3, and EM4.

Table 3.2. Peripheral Power Subdomains shows the peripherals on the PDHV and PD0x domains. Any peripheral not listed is on PD1.

Table 3.2. Peripheral Power Subdomains

Always On in EM2/EM3		Selectively On in EM2/3	
PDHV[1]	**PD0A**	**PD0B**	**PD0C**
LFRCO (Non-precision mode)	RTCC	LETIMER0	LFRCO (Precision Mode)
LFXO	FSRCO	IADC0	
BURTC		ACMP0	
RFSENSE		I2C0	
ULFRCO		WDOG0	
ETAMPDET		EUSART0	
BURAM		PRS	
		DEBUG	
		GPIO	

Note:

1. Peripherals on PDHV are also available in EM4.

3.10 Reset Management Unit (RMU)

The RMU handles reset of the EFR32BG27. A wide range of reset sources are available, including several power supply monitors, pin reset, software-controlled reset, core lockup reset, and watchdog reset.

3.11 Core and Memory

3.11.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M33 RISC processor achieving 1.50 Dhrystone MIPS/MHz
- ARM TrustZone security technology
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 768 KB flash program memory
- Up to 64 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.11.2 Memory System Controller (MSC)

The MSC is the program memory unit of the microcontroller. Both the Cortex-M33 and the LDMA can read from and write to flash memory.

In addition to the main flash array that stores program code, the MSC includes an information block. This block stores special user data and flash lock bits. It also contains a read-only page that holds system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.11.3 Linked Direct Memory Access Controller (LDMA)

The LDMA controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12 Memory Map

The EFR32BG27 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

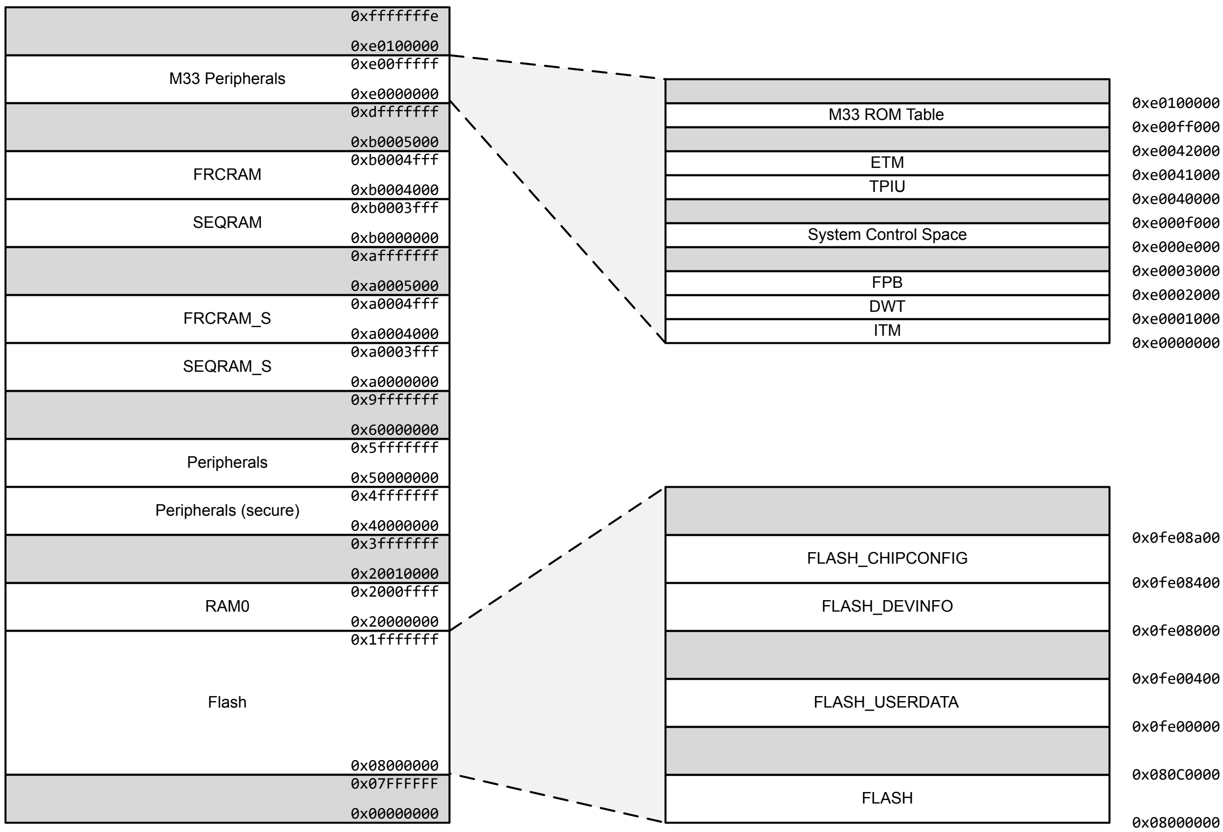


Figure 3.1. EFR32BG27 Memory Map — Core Peripherals and Code Space

3.13 Configuration Summary

The features of the EFR32BG27 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.3. Configuration Summary

Module	Lowest Energy Mode	Configuration
I2C0	EM3[1]	
I2C1	EM1	
IADC0	EM3	
LETIMER0	EM2[1]	
PDM	EM1	2-channel
TIMER0	EM1	32-bit, 3-channels, +DTI
TIMER1	EM1	32-bit, 3-channels, +DTI
TIMER2	EM1	16-bit, 3-channels, +DTI
TIMER3	EM1	16-bit, 3-channels, +DTI
TIMER4	EM1	16-bit, 3-channels, +DTI
EUSART0	EM1 - Full high-speed operation, all modes EM2[1] - Low-energy UART operation, 9600 Baud EM2 or EM3[1] - Low-energy SPI secondary receiver	
USART0	EM1	+IrDA, +I2S, +SmartCard
USART1	EM1	+IrDA, +I2S, +SmartCard

Note:

1. EM2 and EM3 operation is only supported for digital peripheral I/O on Port A and Port B. All GPIO ports support digital peripheral operation in EM0 and EM1.

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and all supplies at 3.0 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Power Supply Pin Dependencies

Due to on-chip circuitry (e.g., diodes), some EFR32 power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various EFR32 supply pins are defined below. Exceeding the below constraints can result in damage to the device and/or increased current draw.

Buck DC-DC or DC-DC not used

- VREGVDD and DVDD
  - In systems using the DCDC converter, DVDD (the buck converter output) should not be driven externally and VREGVDD (the buck converter input) must be greater than DVDD (VREGVDD ≥ DVDD)
  - In systems not using the DCDC converter, DVDD must be shorted to VREGVDD on the PCB (VREGVDD = DVDD)
- DVDD ≥ DECOUPLE
- PAVDD ≥ RFVDD
- AVDD, IOVDD: No dependency with each other or any other supply pin
- VBAT, BOOST_EN: Tie to VSS (WLCSP package only)

Boost DC-DC

- VBAT: DCDC converter input. Connect to recommended supply and L_{DCDC}.
- DVDD: DVDD is the boost converter output and should be bypassed with the recommended C_{DCDC}, it should not be driven by an off-chip regulator.
- VREGVDD: Tie directly to DVDD (WLCSP package only)
- DVDD ≥ DECOUPLE
- PAVDD ≥ RFVDD
- AVDD, IOVDD: No dependency with each other or any other supply pin

4.2 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Voltage on DVDD, AVDD, IOVDD, RFVDD, PAVDD or VREGVDD supply pins	V_{DDMAX}		-0.3	—	3.8	V
Voltage on VBAT supply pin	$V_{VBATMAX}$		-0.3	—	2.0	V
Storage temperature range	T_{STG}		-50	—	+150	°C
Junction temperature	T_{JMAX}	-G grade	—	—	+105	°C
		-I grade	—	—	+125	°C
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V / µs
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.4	V
DC voltage on any GPIO pin	V_{DIGPIN}		-0.3	—	V_{IOVDD} + 0.3	V
DC voltage on RESETn pin[1]	V_{RESETn}		-0.3	—	3.8	V
Input RF level on RF pins RF2G4_IO	$P_{RFMAX2G4}$		—	—	+10	dBm
Absolute voltage on RF pin RF2G4_IO	V_{MAX2G4}		-0.3	—	V_{PAVDD} + 0.3	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

Note:

1. The RESETn pin has a pull-up device to the DVDD supply. For minimum leakage, RESETn should not exceed the voltage at DVDD.

4.3 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-G temperature grade [1]	-40	—	+85	°C
		-I temperature grade [1]	-40	—	+125	° C
VREGVDD operating supply voltage (Buck DCDC or DCDC not used) [2] [3]	$V_{VREGVDD}$	Buck Mode DCDC in regulation, 60 mA load	2.2	3.0	3.8	V
		Buck Mode DCDC in bypass, 60 mA load	1.8	3.0	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.71	3.0	3.8	V
VBAT operating supply voltage (Boost DCDC) [2] [3]	V_{VBAT}	Boost Mode DCDC in regulation [4]	0.8	1.5	1.7	V
DVDD supply voltage	V_{DVDD}	EM0/1	1.71	3.0	3.8	V
		EM2/3/4[5]	1.71	3.0	3.8	V
AVDD supply voltage	V_{AVDD}		1.71	3.0	3.8	V
IOVDD0 operating supply voltage	V_{IOVDD0}	IOVDD0BODEN=0[6]	1.175	3.0	3.8	V
		IOVDD0BODEN=1[6]	1.71	3.0	3.8	V
RFVDD operating supply voltage	V_{RFVDD}		1.71	3.0	V_{PAVDD}	V
PAVDD operating supply voltage	V_{PAVDD}		1.71	3.0	3.8	V
DECOUPLE output capacitor[7]	$C_{DECOUPLE}$	1.0 µF ± 10% X8L capacitor used for performance characterization.	1.0	—	2.75	µF
HCLK and Core frequency	f_{HCLK}	VSCALE2, MODE = WS1	—	—	80	MHz
		VSCALE2, MODE = WS0	—	—	40	MHz
		VSCALE1, MODE = WS0	—	—	40	MHz
PCLK frequency	f_{PCLK}	VSCALE2 or VSCALE1	—	—	40	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE2	—	—	80	MHz
		VSCALE1	—	—	40	MHz
EM01 Group B clock frequency	$f_{EM01GRPBCLK}$	VSCALE2	—	—	80	MHz
		VSCALE1	—	—	40	MHz
HCLK Radio frequency[8]	$f_{HCLKRADIO}$	VSCALE2 or VSCALE1	—	38.4	—	MHz
External Clock Input	f_{CLKIN}	VSCALE2 or VSCALE1	—	—	40	MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DPLL Reference Clock	$f_{DPLLREFCLK}$	VSCALE2 or VSCALE1	—	—	40	MHz

Note:

1. The device may operate continuously at the maximum allowable ambient T_A rating as long as the absolute maximum T_{JMAX} is not exceeded. For an application with significant power dissipation, the allowable T_A may be lower than the maximum T_A rating. T_A = T_{JMAX} - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_{JMAX} and $THETA_{JA}$.
2. Devices in QFN packaging have only a Buck DCDC or Boost DCDC option. VREGVDD will be present if buck DCDC is available, and VBAT will be present if Boost DCDC is available.
3. Devices in WLCSP packaging have the option of Buck DCDC or Boost DCDC. The PCB design should establish connections for only one mode. See the connection diagram section for more details.
4. The VBAT supply may be as high as the Boost DCDC output, but DCDC and RF performance specifications willl degrade.
5. The DVDD supply is monitored by the DVDD BOD in EM0/1 and the LE DVDD BOD in EM2/3/4.
6. The IOVDD BOD enable bit is in the EMU_BOD3SENSE register. The BOD is disabled on reset.
7. Murata GCM21BL81C105KA58L used for performance characterization. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 0.6 μF.
8. The recommended radio crystal frequency is 38.4 MHz and all radio performance is specified at this frequency. See HFXO specifications for more detail on crystal tolerance.

4.4 Buck-Mode DC-DC Converter

Test conditions: L_{DCDC} = 2.2 µH, C_{DCDC} = 4.7 µF, $V_{VREGVDD}$ = 3.0 V, V_{OUT} = 1.8 V, IPKVAL in EM0/1 modes is set to 150 mA, and in EM2/3 modes is set to 90 mA, unless otherwise indicated.

Table 4.3. Buck-Mode DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range at VREGVDD pin	$V_{VREGVDD}$	DCDC in regulation, I_{LOAD} = 60 mA, EM0/EM1 mode	2.2	3.0	3.8	V
		DCDC in regulation, I_{LOAD} = 5 mA, EM0/EM1 or EM2/EM3 mode	1.8	3.0	3.8	V
		Bypass mode	1.8	3.0	3.8	V
Regulated output voltage	V_{OUT}		—	1.8	—	V
Regulation DC accuracy	ACC_{DC}	$V_{VREGVDD}$ ≥ 2.2 V, Steady state in EM0/EM1 mode or EM2/EM3 mode	-2.5	—	3.3	%
Regulation total accuracy	ACC_{TOT}	With mode transitions between EM0/EM1 and EM2/EM3 modes	-5	—	7	%
Steady-state output ripple	V_R	I_{LOAD} = 20 mA in EM0/EM1 mode	—	14.3	—	mVpp
DC line regulation	V_{REG}	I_{LOAD} = 60 mA in EM0/EM1 mode, $V_{VREGVDD}$ ≥ 2.2 V	—	5.5	—	mV/V
DC load regulation	I_{REG}	Load current between 100 µA and 60 mA in EM0/EM1 mode	—	0.27	—	mV/mA
Efficiency	EFF	Load current between 100 µA and 60 mA in EM0/EM1 mode, or between 10 µA and 5 mA in EM2/EM3 mode	—	91	—	%
Output load current[1]	I_{LOAD}	EM0/EM1 mode, DCDC in regulation	—	—	60	mA
		EM2/EM3 mode, DCDC in regulation	—	—	5	mA
		Bypass mode	—	—	60	mA
Nominal output capacitor	C_{DCDC}	4.7 µF ± 10% X7R capacitor used for performance characterization[2]	4.7	—	10	µF
Nominal inductor	L_{DCDC}	± 20% tolerance	—	2.2	—	µH
Nominal input capacitor	C_{IN}		C_{DCDC}	—	—	µF
Resistance in bypass mode	R_{BYP}	Bypass switch from VREGVDD to DVDD, $V_{VREGVDD}$ = 1.8 V	—	1.75	3	Ω
		Powertrain PFET switch from VREGVDD to VREGSW, $V_{VREGVDD}$ = 1.8 V	—	0.86	1.5	Ω
Supply monitor threshold programming range	V_{CMP_RNG}	Programmable in 0.1 V steps	2.0	—	2.3	V
Supply monitor threshold accuracy	V_{CMP_ACC}	Supply falling edge trip point	-5	—	5	%
Supply monitor threshold hysteresis	V_{CMP_HYST}	Positive hysteresis on the supply rising edge referred to the falling edge trip point	—	4	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply monitor response time	t_{CMP_DELAY}	Supply falling edge at -100 mV / µs	—	0.6	—	µs
Time to switch from EM2/3 mode to EM0/1 mode[3]	t_{MODE_SWITCH}		—	4	8	µs
		WLCSP devices only	—	16	32	µs

Note:

1. I_{LOAD} is the total current sourced by the DCDC, including on-chip and off-chip circuits powered from the DVDD supply rail.
2. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 2.4 µF.
3. Mode switch is initiated when a wake event is recognized, and occurs in parallel to the normal system wake time. During the mode switch I_{LOAD} should be limited to 20 mA or less.

4.4.1 Buck DC-DC Operating Limits

The maximum supported voltage on the VREGVDD supply pin is limited under certain conditions. Maximum input voltage is a function of temperature and the average load current over a 10-year lifetime. Figure 4.1. Lifetime average load current limit vs. Maximum input voltage shows the safe operating region under specific conditions. Exceeding this safe operating range may impact the reliability and performance of the DC-DC converter.

The average load current for an application can typically be determined by examining the current profile during the time the device is powered. For example, an application that is continuously powered which spends 99% of the time asleep consuming 2 μA and 1% of the time active and consuming 10 mA has an average lifetime load current of about 102 μA.

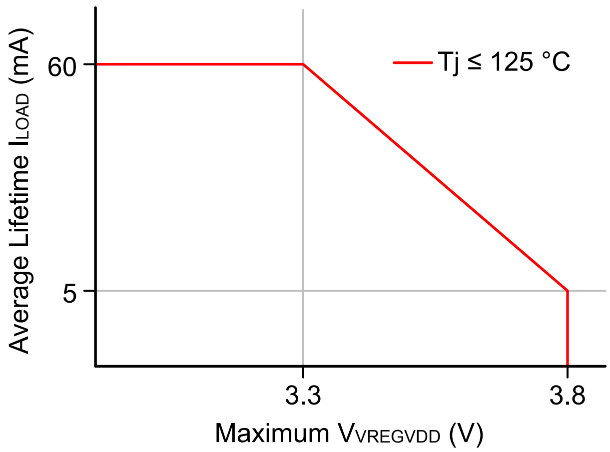


Figure 4.1. Lifetime average load current limit vs. Maximum input voltage

The minimum input voltage for the DC-DC in EM0/EM1 mode is a function of the maximum load current, and the peak current setting. Figure 4.2. Transient maximum load current vs. Minimum input voltage shows the max load current vs. input voltage for different DC-DC peak inductor current settings.

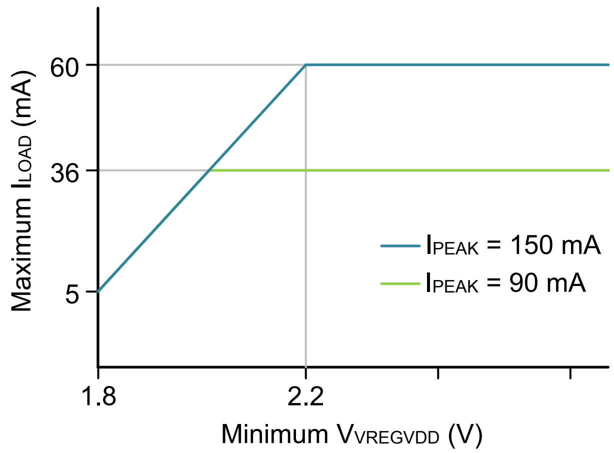


Figure 4.2. Transient maximum load current vs. Minimum input voltage

4.5 Boost-Mode DC-DC Converter

Test conditions: L_{DCDC} = 2.2 µH, C_{DCDC} = 10 µF, V_{VBAT} = 1.5 V, V_{OUT} = 1.8 V, IPKVAL in EM0/1 modes is set to 180 mA, and in EM2/3 modes is set to 150 mA, unless otherwise indicated.

Table 4.4. Boost-Mode DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range at VBAT pin	V_{VBAT}	C_{LOAD} = 10 µF	0.8	—	1.7	V
Regulated output voltage	V_{OUT}		—	1.8	—	V
Regulation DC accuracy	ACC_{DC}	0.8 V ≤ V_{VBAT} ≤ 1.7 V, Steady state in EM0/EM1 mode or EM2/EM3 mode	-2.7	—	3.5	%
Regulation total accuracy	ACC_{TOT}	With mode transitions between EM0/EM1 and EM2/EM3 modes	-5	—	7	%
Steady-state output ripple	V_R	I_{LOAD} = 20 mA in EM0/EM1 mode	—	16	—	mVpp
DC line regulation	V_{REG}	I_{LOAD} = 25 mA in EM0/EM1 mode, 0.8 V ≤ V_{VBAT} ≤ 1.6 V	—	17	—	mV/V
DC load regulation	I_{REG}	Load current between 100 µA and 25 mA in EM0/EM1 mode	—	-0.35	—	mV/mA
Efficiency	EFF	Load current between 100 µA and 25 mA in EM0/EM1 mode, or between 10 µA and 5 mA in EM2/EM3 mode	—	91	—	%
Output load current[1]	I_{LOAD}	EM0/EM1 mode, DCDC in regulation	—	—	25	mA
		EM2/EM3 mode, DCDC in regulation	—	—	25	mA
External load during startup[2]	I_{LOAD_START}	Off-chip load applied at DVDD supply rail	—	—	0.5	mA
Nominal output capacitor	C_{DCDC}	10 µF ± 10% X8L capacitor used for performance characterization[3]	7.5	10	—	µF
Nominal inductor	L_{DCDC}	± 20% tolerance	—	2.2	—	µH
Nominal input capacitor	C_{IN}		4.7	—	—	µF
Time to switch from EM2/3 mode to EM0/1 mode[4]	t_{MODE_SWITCH}		—	16	32	µs
Input high voltage on BOOST_EN	$V_{IH\_BOOST\_EN}$	V_{BAT} < 1.2 V	0.85 * V_{BAT}	—	—	V
		V_{BAT} ≥ 1.2 V	0.7 * V_{BAT}	—	—	V
Input low voltage on BOOST_EN	$V_{IL\_BOOST\_EN}$		—	—	0.3 * V_{BAT}	V
Hysteresis of input voltage on BOOST_EN	$V_{HYST\_BOOST\_EN}$		0.05 * V_{BAT}	—	—	V
Time from BOOST_EN high to output regulation at 1.8 V	t_{START}	With 500 µA off-chip I_{LOAD_START} on DVDD	—	5	10	ms

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Peak output voltage during startup (during t_{START})	V_{START}		—	2.06	2.8	V

Note:

1. I_{LOAD} is the total current sourced by the DCDC, including on-chip and off-chip circuits powered from the DVDD supply rail.
2. I_{LOAD_START} is the allowable current sourced by the DCDC during startup to off-chip circuits powered from the DVDD supply rail.
3. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 6.7 µF.
4. Mode switch is initiated when a wake event is recognized, and occurs in parallel to the normal system wake time. During the mode switch I_{LOAD} should be limited to 20 mA or less.

4.6 Coulomb Counter Calibration Load

Table 4.5. Coulomb Counter Calibration Load

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating temperature range	T_{CCLOAD}		-20	—	70	°C
Load current accuracy vs. production measurement[1]	I_{LOAD_ACC}	CCLVL = LOAD2 (1.0 mA nominal)	-2.4	—	2.4	%
		CCLVL = LOAD7 (8.0 mA nominal)	-2.4	—	2.4	%

Note:

1. Calibration load currents vary from part-to-part. The magnitude of the calibration load currents at 25 °C are measured in production on each device, and the measurement is written into DEVINFO space in the CCLOADxx locations. Accuracy is specified relative to the measured value across T_{CCLOAD}.

4.7 Thermal Characteristics

Table 4.6. Thermal Characteristics

Package	Board	Parameter	Symbol	Test Condition	Value	Unit
40QFN (5x5mm)	JEDEC - High Thermal Cond. (2s2p)[1]	Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air	30.0	°C/W
		Thermal Resistance, Junction to Top Center	Ψ_{JT}		0.5	°C/W
		Thermal Resistance, Junction to Board	Ψ_{JB}		12	°C/W
32QFN (4x4mm)	JEDEC - High Thermal Cond. (2s2p)[2]	Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air	39.8	°C/W
		Thermal Resistance, Junction to Top Center	Ψ_{JT}		0.7	°C/W
		Thermal Resistance, Junction to Board	Ψ_{JB}		16.8	°C/W
39WLCSP	JEDEC - High Thermal Cond. (2s2p)[3]	Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air	54.8	°C/W
		Thermal Resistance, Junction to Top Center	Ψ_{JT}		0.10	°C/W
		Thermal Resistance, Junction to Board	Ψ_{JB}		17.4	°C/W

Note:

1. Based on 4 layer PCB with dimension 3" x 4.5", PCB Thickness of 1.6 mm, per JEDEC. PCB Center Land with 9 Via to top internal plane of PCB.
2. Based on 4 layer PCB with dimension 3" x 4.5", PCB Thickness of 1.6 mm, per JEDEC. PCB Center Land with 4 Via to top internal plane of PCB.
3. Based on 4 layer PCB with dimension 3" x 4.5", PCB Thickness of 1.6 mm, per JEDEC. PCB Center Land with 6 Via to top internal GND plane and 5 Via to bottom internal VDD plane of PCB.

4.8 Current Consumption

4.8.1 MCU Current Consumption Using Buck DC-DC at 3.0 V VREGVDD Input

Unless otherwise indicated, typical conditions are: VREGVDD = 3.0 V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V from DC-DC. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.7. MCU Current Consumption Using Buck DC-DC at 3.0 V VREGVDD Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	32	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	29	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	42	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	30	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	30	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	43	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	25	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	27	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	33	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	229	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	19	—	µA/MHz
		38.4 MHz crystal	—	20	—	µA/MHz
		38 MHz HFRCO	—	16	—	µA/MHz
		26 MHz HFRCO	—	18	—	µA/MHz
		16 MHz HFRCO	—	23	—	µA/MHz
		1 MHz HFRCO	—	220	—	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	Full RAM retention and RTC running from LFXO	—	1.6	—	µA
		Full RAM retention and RTC running from LFRCO	—	1.6	—	µA
		24 kB RAM retention and RTC running from LFXO	—	1.4	—	µA
		24 kB RAM retention and RTC running from LFRCO in precision mode	—	1.8	—	µA
		8 kB RAM retention and RTC running from LFXO	—	1.3	—	µA
		8 kB RAM retention and RTC running from LFRCO	—	1.3	—	µA
		8 kB RAM retention and RTC running from LFXO, Radio RAM and CPU cache not retained	—	1.1	—	µA
		8 kB RAM retention and RTC running from LFXO, CPU cache not retained	—	1.3	—	µA
		8 kB RAM retention and RTC running from LFXO, Radio RAM, CPU cache, and EM0/1 peripheral states not retained	—	1.1	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	8 kB RAM retention and RTC running from ULFRCO	—	1.1	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	1.2	—	µA
Consumption for retained RAM bank in EM2	I_{RAM}	24 kB RAM bank	—	0.13	—	µA
		8 kB RAM bank	—	0.043	—	µA
		32 kB RAM bank	—	0.17	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.9.4 Power Domains for a list of the peripherals in each power domain.

4.8.2 MCU Current Consumption Using Boost DC-DC at 1.5 V VBAT Input

Unless otherwise indicated, typical conditions are: VBAT = 1.5 V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V from DC-DC. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.8. MCU Current Consumption Using Boost DC-DC at 1.5 V VBAT Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	65	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	59	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	86	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	61	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	60	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	86	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	50	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	55	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	65	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	447	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	38	—	µA/MHz
		38.4 MHz crystal	—	41	—	µA/MHz
		38 MHz HFRCO	—	31	—	µA/MHz
		26 MHz HFRCO	—	35	—	µA/MHz
		16 MHz HFRCO	—	46	—	µA/MHz
		1 MHz HFRCO	—	428	—	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	Full RAM retention and RTC running from LFXO	—	3.1	—	µA
		Full RAM retention and RTC running from LFRCO	—	3.1	—	µA
		24 kB RAM retention and RTC running from LFXO	—	2.6	—	µA
		24 kB RAM retention and RTC running from LFRCO in precision mode	—	3.5	—	µA
		8 kB RAM retention and RTC running from LFXO	—	2.5	—	µA
		8 kB RAM retention and RTC running from LFRCO	—	2.5	—	µA
		8 kB RAM retention and RTC running from LFXO, Radio RAM and CPU cache not retained	—	2.1	—	µA
		8 kB RAM retention and RTC running from LFXO, CPU cache not retained	—	2.4	—	µA
		8 kB RAM retention and RTC running from LFXO, Radio RAM, CPU cache, and EM0/1 peripheral states not retained	—	2.1	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	8 kB RAM retention and RTC running from ULFRCO	—	2.2	—	µA
Current with Boost DCDC shut down (BOOST_EN = 0)	I_{SHDN}	IOVDD, AVDD, RFVDD, and PAVDD connected to DVDD (unpowered)	—	10.4	20	nA
		IOVDD powered. AVDD, RFVDD, and PAVDD connected to DVDD (unpowered)	—	31.3	50	nA
Current consumption during reset	I_{RST}	Hard pin reset held, BOOST_EN = 1 (DCDC running)	—	629	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	2.3	—	µA
Consumption for retained RAM bank in EM2	I_{RAM}	24 kB RAM bank	—	0.26	—	µA
		8 kB RAM bank	—	0.086	—	µA
		32 kB RAM bank	—	0.34	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.9.4 Power Domains for a list of the peripherals in each power domain.

4.8.3 MCU Current Consumption at 3.0 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = VREGVDD = 3.0 V. DC-DC not used. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.9. MCU Current Consumption at 3.0 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	46	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	42	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	62	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	44	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	44	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	62	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	36	65	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	39	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	47	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	305	925	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	27	—	µA/MHz
		38.4 MHz crystal	—	30	—	µA/MHz
		38 MHz HFRCO	—	22	50	µA/MHz
		26 MHz HFRCO	—	25	—	µA/MHz
		16 MHz HFRCO	—	33	—	µA/MHz
		1 MHz HFRCO	—	290	910	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	Full RAM retention and RTC running from LFXO	—	2.2	—	µA
		Full RAM retention and RTC running from LFRCO	—	2.3	5.8	µA
		24 kB RAM retention and RTC running from LFXO	—	1.9	—	µA
		24 kB RAM retention and RTC running from LFRCO in precision mode	—	2.5	—	µA
		8 kB RAM retention and RTC running from LFXO	—	1.7	—	µA
		8 kB RAM retention and RTC running from LFRCO	—	1.8	—	µA
		8 kB RAM retention and RTC running from LFXO, Radio RAM and CPU cache not retained	—	1.5	—	µA
		8 kB RAM retention and RTC running from LFXO, CPU cache not retained	—	1.7	—	µA
		8 kB RAM retention and RTC running from LFXO, Radio RAM, CPU cache, and EM0/1 peripheral states not retained	—	1.4	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	8 kB RAM retention and RTC running from ULFRCO	—	1.5	3.9	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, no LF oscillator	—	0.18	0.4	µA
		BURTC with LFXO	—	0.51	—	µA
		ETAMPDET active[1]	—	0.42	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	530	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[2]	I_{PD0B_VS}		—	1.7	—	µA
Consumption for retained RAM bank in EM2	I_{RAM}	24 kB RAM bank	—	0.21	—	µA
		8 kB RAM bank	—	0.071	—	µA
		32 kB RAM bank	—	0.29	—	µA

Note:

1. ETAMPDET operating from ULFRCO divided down to 100 Hz, with 1 nF load capacitance to ground.
2. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.9.4 Power Domains for a list of the peripherals in each power domain.

4.8.4 MCU Current Consumption at 1.8 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = VREGVDD = 1.8 V. DC-DC not used. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.10. MCU Current Consumption at 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running Prime from flash, VSCALE2	—	46	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running while loop from flash, VSCALE2	—	42	—	µA/MHz
		76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	62	—	µA/MHz
		38.4 MHz crystal, CPU running Prime from flash	—	45	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	44	—	µA/MHz
		38.4 MHz crystal, CPU running CoreMark loop from flash	—	63	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	36	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	39	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	46	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	320	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	76.8 MHz HFRCO w/ DPLL referenced to 38.4 MHz crystal, VSCALE2	—	28	—	µA/MHz
		38.4 MHz crystal	—	30	—	µA/MHz
		38 MHz HFRCO	—	22	—	µA/MHz
		26 MHz HFRCO	—	25	—	µA/MHz
		16 MHz HFRCO	—	33	—	µA/MHz
		1 MHz HFRCO	—	306	—	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	Full RAM retention and RTC running from LFXO	—	2.2	—	µA
		Full RAM retention and RTC running from LFRCO	—	2.2	—	µA
		24 kB RAM retention and RTC running from LFXO	—	1.8	—	µA
		24 kB RAM retention and RTC running from LFRCO in precision mode	—	2.4	—	µA
		8 kB RAM retention and RTC running from LFXO	—	1.7	—	µA
		8 kB RAM retention and RTC running from LFRCO	—	1.7	—	µA
		8 kB RAM retention and RTC running from LFXO, Radio RAM and CPU cache not retained	—	1.4	—	µA
		8 kB RAM retention and RTC running from LFXO, CPU cache not retained	—	1.7	—	µA
		8 kB RAM retention and RTC running from LFXO, Radio RAM, CPU cache, and EM0/1 peripheral states not retained	—	1.4	—	µA
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	8 kB RAM retention and RTC running from ULFRCO	—	1.5	—	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, no LF oscillator	—	0.14	—	µA
		BURTC with LFXO	—	0.43	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	443	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	1.7	—	µA
Consumption for retained RAM bank in EM2	I_{RAM}	24 kB RAM bank	—	0.21	—	µA
		8 kB RAM bank	—	0.071	—	µA
		32 kB RAM bank	—	0.29	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.9.4 Power Domains for a list of the peripherals in each power domain.

4.8.5 Radio Current Consumption at 3.0 V using Buck-Mode DCDC

RF current consumption measured with RHCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VREGVDD = 3.0 V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.11. Radio Current Consumption at 3.0 V using Buck-Mode DCDC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.8	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	4.0	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4.2	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.8	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	4.1	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4.3	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.6	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	3.8	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4.0	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4.0	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	4.3	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4.5	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, listening for packet	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.8	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	4.0	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4.2	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.8	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	4.0	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4.2	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	3.6	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	3.9	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4.0	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	4.3	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	4.5	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	4.1	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	5.8	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	7.6	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	9.2	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	11.3	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1, EM1	—	4.3	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE1, EM1	—	6.1	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE1, EM1	—	7.9	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE1, EM1	—	9.4	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE1, EM1	—	11.5	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE2, EM1	—	4.5	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE2, EM1	—	6.2	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE2, EM1	—	8.0	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE2, EM1	—	9.6	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE2, EM1	—	11.7	—	mA

4.8.6 Radio Current Consumption at 1.5 V Using Boost-Mode DCDC

RF current consumption measured with RHCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VBAT = 1.5 V. AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.12. Radio Current Consumption at 1.5 V Using Boost-Mode DCDC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.9	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	8.4	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	8.8	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	8.0	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	8.5	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	8.9	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.5	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	8.0	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	8.4	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	8.4	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	8.9	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	9.4	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, listening for packet	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.9	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	8.4	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	8.8	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	8.0	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	8.4	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	8.8	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.6	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	8.1	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	8.5	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	8.6	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1	—	9.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2, EM1	—	9.6	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	8.2	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	12.2	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	15.9	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	19.2	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE1, EM1P (Radio clocks only)	—	23.4	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1, EM1	—	8.7	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE1, EM1	—	12.7	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE1, EM1	—	16.4	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE1, EM1	—	19.6	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE1, EM1	—	23.7	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE2, EM1	—	9.0	—	mA
		f = 2.4 GHz, CW, High-power PA, 0 dBm output power, VSCALE2, EM1	—	12.9	—	mA
		f = 2.4 GHz, CW, High-power PA, 4 dBm output power, VSCALE2, EM1	—	16.6	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power, VSCALE2, EM1	—	19.9	—	mA
		f = 2.4 GHz, CW, High-power PA, 8 dBm output power, VSCALE2, EM1	—	24.1	—	mA

4.9 Flash Characteristics

Table 4.13. Flash Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash Supply voltage during write or erase	V_{FLASH}		1.71	—	3.8	V
Flash erase cycles before failure[1]	EC_{FLASH}		10,000	—	—	cycles
Flash data retention[1]	RET_{FLASH}		10	—	—	years
Program Time	t_{PROG}	one word (32-bits)	40	44	48	uSec
		average per word over 128 words	10	11	12	uSec
Page Erase Time	t_{PERASE}		11	13	15	ms
Mass Erase Time	t_{MERASE}	Erases all of User Code area	62	77	87	ms
Program Current	I_{WRITE}	T_A = 25 °C	—	—	2.5	mA
Page Erase Current	I_{ERASE}	T_A = 25 °C	—	—	1.7	mA
Mass Erase Current	I_{MERASE}	T_A = 25 °C	—	—	1.8	mA

Note:

1. Flash data retention information is published in the Quarterly Quality and Reliability Report.

4.10 Energy Mode Wake-up and Entry Times

Unless otherwise specified, these times are measured using the HFRCO at 19 MHz.

Table 4.14. Energy Mode Wake-up and Entry Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake-up Time from EM1	t_{EM1_WU}	Code execution from flash	—	3	—	HCLKs
		Code execution from RAM	—	1.44	—	µs
Wake-up Time from EM2	t_{EM2_WU}	Code execution from flash, No Voltage Scaling	—	13.1	—	µs
		Code execution from RAM, No Voltage Scaling	—	5.2	—	µs
		Voltage scaling up one level[1]	—	37.7	—	µs
		Voltage scaling up two levels[2]	—	50.2	—	µs
Wake-up Time from EM3	t_{EM3_WU}	Code execution from flash, No Voltage Scaling	—	13.1	—	µs
		Code execution from RAM, No Voltage Scaling	—	5.2	—	µs
		Voltage scaling up one level[1]	—	37.7	—	µs
		Voltage scaling up two levels[2]	—	50.2	—	µs
Wake-up Time from EM4	t_{EM4_WU}	Code execution from flash	—	10.4	—	ms
Entry time to EM1	t_{EM1_ENT}	Code execution from flash	—	1.27	—	µs
Entry time to EM2	t_{EM2_ENT}	Code execution from flash	—	5.5	—	µs
Entry time to EM3	t_{EM3_ENT}	Code execution from flash	—	5.5	—	µs
Entry time to EM4	t_{EM4_ENT}	Code execution from flash	—	10.8	—	µs
Voltage scaling time in EM0[3]	t_{SCALE}	Up from VSCALE1 to VSCALE2	—	32	—	µs
		Down from VSCALE2 to VSCALE1	—	172	—	µs

Note:

1. Voltage scaling one level is between VSCALE0 and VSCALE1 or between VSCALE1 and VSCALE2.
2. Voltage scaling two levels is between VSCALE0 and VSCALE2.
3. During voltage scaling in EM0, RAM is inaccessible and processor will be halted until complete.

4.11 Boot Timing

Secure boot impacts the recovery time from all sources of device reset. In addition to the root code authentication process, which cannot be disabled or bypassed, the root code can authenticate a bootloader, and the bootloader can authenticate the application. In projects that include only an application and no bootloader, the root code can authenticate the application directly. The duration of each authentication operation depends on two factors: the computation of the associated image hash, which is proportional to the size of the image, and the verification of the image signature, which is independent of image size.

The duration for the root code to authenticate the bootloader will depend on the SE firmware version as well as on the size of the bootloader.

The duration for the bootloader to authenticate the application can depend on the size of the application.

The configurations below assume that the associated bootloader and application code images do not contain a bootloader certificate or an application certificate. Authenticating a bootloader certificate or an application certificate will extend the boot time by an additional 6 to 7 ms.

The table below provides the durations from the termination of reset until the completion of the secure boot process (start of main() function in the application image) under various conditions.

Conditions:

- VSE firmware version: 2.2.1
- Gecko Bootloader size: 13.3 kB

Timing is expected to be similar for subsequent VSE firmware versions. Refer to VSE firmware release notes for any significant changes.

Table 4.15. Boot Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Boot time[1]	t_{BOOT}	Secure boot application check disabled, no bootloader	—	16.0	—	ms
		Secure boot application check disabled, second stage bootloader check enabled[2], 50 KB application size	—	22.3	—	ms
		Secure boot application check enabled, second stage bootloader check enabled[2], 50 KB application size	—	47.9	—	ms
		Secure boot application check enabled, second stage bootloader check enabled[2], 150 KB application size	—	53.4	—	ms
		Secure boot application check enabled, second stage bootloader check enabled[2], 350 KB application size	—	64.5	—	ms

Note:

1. Excludes boost DCDC startup time.
2. Timing is measured with the specified bootloader size. Actual bootloader size will impact the boot timing slightly, with a similar μs / KB ratio as application size.

4.12 RFSENSE Low-energy Wake-on-RF

Table 4.16. RFSENSE Low-energy Wake-on-RF

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Average current	$I_{RFSENSE}$	RF energy below wake threshold	—	138	—	nA
		Selective mode, RF energy above threshold but no OOK sync detected	—	131	—	nA
RF level above which RFSENSE will detect signal[1]	$THRES_{TRIG}$	Threshold set to -34 dBm	-28	—	—	dBm
		Threshold set to -22 dBm	-19	—	—	dBm
RF level below which RFSENSE will not detect signal[1]	$THRES_{NOTRIG}$	Threshold set to -34 dBm	—	—	-40	dBm
		Threshold set to -22 dBm	—	—	-26	dBm
Sensitivity in selective OOK mode[1]	$SENS_{OOK}$	Sensitivity for > 90% probability of OOK detection[2], threshold set to -34 dBm	-28	—	—	dBm
		Sensitivity for > 90% probability of OOK detection[2], threshold set to -22 dBm	-19	—	—	dBm

Note:

1. Values collected with conducted measurements performed at the end of the matching network.
2. Selective wake signal is 1 kHz OOK Manchester-coded, 8 bits of preamble, 32-bit sync word.

4.13 2.4 GHz RF Transceiver Characteristics for QFN Packages

4.13.1 RF Transmitter Characteristics for QFN Packages

4.13.1.1 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.17. RF Transmitter General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		2400	—	2483.5	MHz
Radio-only current consumption while transmitting[1]	I_{TX_RADIO}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power	—	4.16	—	mA
		f = 2.4 GHz, CW, High-power PA, 6 dBm output power	—	8.73	—	mA
		f = 2.4 GHz, CW, High-Power PA, 8 dBm output power	—	11.39	—	mA
Maximum TX power[2]	$POUT_{MAX}$	High-power PA	—	8.28	—	dBm
		0 dBm PA	—	0	—	dBm
Minimum active TX power	$POUT_{MIN}$	High-power PA	—	-31.58	—	dBm
		0 dBm PA	—	-29.32	—	dBm
Output power variation vs supply voltage variation, frequency = 2450 MHz	$POUT_{VAR\_V}$	8 dBm PA output power, using DCDC with VREGVDD swept from 1.8 to 3.0 V	—	0.01	—	dB
		0 dBm PA output power, using DCDC with VREGVDD swept from 1.8 to 3.0 V	—	0.01	—	dB
Output power variation vs temperature, Frequency = 2450 MHz	$POUT_{VAR\_T}$	High-power PA at 8 dBm, (-40 to +125 °C)	—	1.09	—	dB
		0 dBm PA at 0 dBm, (-40 to +125 °C)	—	1.51	—	dB
		High-power PA at 8 dBm, (-40 to +85 °C)	—	0.84	—	dB
		0 dBm PA at 0 dBm, (-40 to +85 °C)	—	1.08	—	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	High-power PA, 8 dBm	—	0.13	—	dB
		0 dBm PA, 0 dBm	—	0.24	—	dB
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz.	—	-47	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30-88 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-26	—	dBc
Spurious emissions per ETSI EN300.440	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-60	—	dBm
		25-1000 MHz, excluding above frequencies. P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-42	—	dBm
		1G-14G, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-36	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band, per ETSI 300.328	$SPUR_{ETSI328}$	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-862 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-60	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 862-1000 MHz , P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-42	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-36	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-16	—	dBm

Note:

1. Supply current to radio, supplied by buck DC-DC with 3.0 V, measured at VREGVDD.
2. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this data sheet can be found in the Max TX Power column of the Ordering Information Table.

4.13.1.2 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.18. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 8 dBm	—	678	—	kHz
		P_{out} = 0 dBm	—	678	—	kHz
Power spectral density limit	PSD_{LIMIT}	P_{out} = 8 dBm, Per FCC part 15.247 at 8 dBm	—	2.0	—	dBm/3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-6.7	—	dBm/3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	7.8	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 8 dBm 99% BW at highest and lowest channels in band	—	1.02	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	1.03	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	P_{out} = 8 dBm, Inband spurs at ± 2 MHz	—	-39.9	—	dBm
		P_{out} = 0 dBm, Inband spurs at ± 2 MHz	—	-48.4	—	dBm
		P_{out} = 8 dBm Inband spurs at ± 3 MHz	—	-46.0	—	dBm
		P_{out} = 0 dBm Inband spurs at ± 3 MHz	—	-54.6	—	dBm

Note:

1. Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.13.1.3 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.19. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 8 dBm	—	1420	—	kHz
		P_{out} = 0 dBm	—	1420	—	kHz
Power spectral density limit	PSD_{LIMIT}	P_{out} = 8 dBm, Per FCC part 15.247 at 8 dBm	—	-1.8	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-10.5	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	6.8	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 8 dBm 99% BW at highest and lowest channels in band	—	2.05	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	2.05	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	P_{out} = 8 dBm, Inband spurs at ± 4 MHz	—	-39.1	—	dBm
		P_{out} = 0 dBm, Inband spurs at ± 4 MHz	—	-47.7	—	dBm
		P_{out} = 8 dBm Inband spurs at ± 6 MHz	—	-44.6	—	dBm
		P_{out} = 0 dBm Inband spurs at ± 6 MHz	—	-53.2	—	dBm

Note:

1. Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.13.1.4 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.20. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 8 dBm	—	711	—	kHz
		P_{out} = 0 dBm	—	711	—	kHz
Power spectral density limit	PSD_{LIMIT}	P_{out} = 8 dBm, Per FCC part 15.247 at 8 dBm	—	1.1	—	dBm/3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-7.6	—	dBm/3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	7.8	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 8 dBm 99% BW at highest and lowest channels in band	—	1.03	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	1.03	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	P_{out} = 8 dBm, Inband spurs at ± 2 MHz	—	-39.8	—	dBm
		P_{out} = 0 dBm, Inband spurs at ± 2 MHz	—	-48.5	—	dBm
		P_{out} = 8 dBm Inband spurs at ± 3 MHz	—	-46.0	—	dBm
		P_{out} = 0 dBm Inband spurs at ± 3 MHz	—	-54.6	—	dBm

Note:

1. Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.13.1.5 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.21. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 8 dBm	—	600	—	kHz
		P_{out} = 0 dBm	—	600	—	kHz
Power spectral density limit	PSD_{LIMIT}	P_{out} = 8 dBm, Per FCC part 15.247 at 8 dBm	—	2.0	—	dBm/3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-6.7	—	dBm/3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	7.8	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 8 dBm 99% BW at highest and lowest channels in band	—	1.03	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	1.03	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	P_{out} = 8 dBm, Inband spurs at ± 2 MHz	—	-39.5	—	dBm
		P_{out} = 0 dBm, Inband spurs at ± 2 MHz	—	-47.9	—	dBm
		P_{out} = 8 dBm Inband spurs at ± 3 MHz	—	-46.0	—	dBm
		P_{out} = 0 dBm Inband spurs at ± 3 MHz	—	-54.6	—	dBm

Note:

1. Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.13.1.6 RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.22. RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error vector magnitude per 802.15.4-2011	EVM	Average across frequency, signal is DSSS-OQPSK reference packet, P_{out} = 8 dBm	—	3.0	—	% rms
		Average across frequency, signal is DSSS-OQPSK reference packet, P_{out} = 0 dBm	—	3.0	—	% rms
Power spectral density limit	PSD_{LIMIT}	Relative, at carrier ± 3.5 MHz, P_{out} = 8 dBm	—	-51.0	—	dBc/100kHz
		Relative, at carrier ± 3.5 MHz, P_{out} = 0 dBm	—	-51.8	—	dBc/100kHz
		Absolute, at carrier ± 3.5 MHz, P_{out} = 8 dBm	—	-53.2	—	dBm/100kHz
		Absolute, at carrier ± 3.5 MHz, P_{out} = 0 dBm	—	-62.8	—	dBm/100kHz
		Per FCC part 15.247, P_{out} = 8 dBm	—	-2.3	—	dBm/3kHz
		Per FCC part 15.247, P_{out} = 0 dBm	—	-11.0	—	dBm/3kHz
		ETSI 300.328 P_{out} = 8 dBm	—	6.0	—	dBm
		ETSI 300.328 P_{out} = 0 dbm	—	-2.7	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	99% BW at highest and lowest channels in band, P_{out} = 8 dBm	—	2.22	—	MHz
		99% BW at highest and lowest channels in band, P_{out} = 0 dBm	—	2.22	—	MHz

4.13.2 RF Receiver Characteristics for QFN Packages

4.13.2.1 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.23. RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		2400	—	2483.5	MHz
Radio-only current consumption in receive mode[1]	I_{RX_RADIO}		—	2.46	—	mA
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	—	-63	—	dBm
		1 GHz to 12 GHz	—	-53	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216 MHz to 960 MHz, conducted measurement	—	-47	—	dBm
		Above 960 MHz, conducted measurement.	—	-47	—	dBm
2GFSK Sensitivity	$SENS_{2GFSK}$	2 Mbps 2GFSK signal[2], 1% PER	—	-93.5	—	dBm
		250 kbps 2GFSK signal[3], 0.1% BER	—	-105	—	dBm

Note:

1. Supply current to radio, supplied by DC-DC with 3.0 V, measured at VREGVDD.
2. Reference signal is 2 Mbps 2GFSK, BT=0.5, mi=1.0, Δf = ± 1 MHz, Channel bandwidth = 2.4 MHz.
3. Reference signal is 250 kbps 2GFSK, BT=0.5, mi=1.0, Δf = ± 125 kHz, Channel bandwidth = 350 kHz.

4.13.2.2 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz, Packet length is 255 bytes.

Table 4.24. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-99.2	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-97.7	—	dBm
		With non-ideal signals[3] [1]	—	-97.1	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1] [4]	—	8.4	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1] [5] [4] [6]	—	-6.7	—	dB
		Interferer is reference signal at -1 MHz offset[1] [5] [4] [6]	—	-6.5	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1] [5] [4] [6]	—	-40.8	—	dB
		Interferer is reference signal at -2 MHz offset[1] [5] [4] [6]	—	-40.2	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1] [5] [4] [6]	—	-46.5	—	dB
		Interferer is reference signal at -3 MHz offset[1] [5] [4] [6]	—	-46.7	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1] [6]	—	-23.7	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1] [6]	—	-40.8	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1] [6]	—	-6.7	—	dB
Intermodulation performance	IM	n = 3 (see note[7])	—	-19.0	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -67 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.
7. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.13.2.3 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz, Packet length is 255 bytes.

Table 4.25. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-96.3	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-94.7	—	dBm
		With non-ideal signals[3] [1]	—	-94.5	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1] [4]	—	8.6	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +2 MHz offset[1] [5] [4] [6]	—	-6.3	—	dB
		Interferer is reference signal at -2 MHz offset[1] [5] [4] [6]	—	-7.3	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +4 MHz offset[1] [5] [4] [6]	—	-42.5	—	dB
		Interferer is reference signal at -4 MHz offset[1] [5] [4] [6]	—	-45.5	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +6 MHz offset[1] [5] [4] [6]	—	-49.2	—	dB
		Interferer is reference signal at -6 MHz offset[1] [5] [4] [6]	—	-51.1	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1] [6]	—	-23.1	—	dB
Selectivity to image frequency ± 2 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz with 1 MHz precision[1] [6]	—	-42.5	—	dB
		Interferer is reference signal at image frequency -2 MHz with 1 MHz precision[1] [6]	—	-6.3	—	dB
Intermodulation performance	IM	n = 3 (see note[7])	—	-18.4	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -67 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.
7. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.13.2.4 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz, Packet length is 255 bytes.

Table 4.26. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-102.7	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-101.4	—	dBm
		With non-ideal signals[3] [1]	—	-100.3	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1] [4]	—	2.5	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1] [5] [4] [6]	—	-7.8	—	dB
		Interferer is reference signal at -1 MHz offset[1] [5] [4] [6]	—	-7.9	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1] [5] [4] [6]	—	-46.6	—	dB
		Interferer is reference signal at -2 MHz offset[1] [5] [4] [6]	—	-50.6	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1] [5] [4] [6]	—	-48.5	—	dB
		Interferer is reference signal at -3 MHz offset[1] [5] [4] [6]	—	-54.1	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1] [6]	—	-48.2	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1] [6]	—	-48.5	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1] [6]	—	-46.6	—	dB

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -72 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.

4.13.2.5 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz, Packet length is 255 bytes.

Table 4.27. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-106.9	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-106.5	—	dBm
		With non-ideal signals[3] [1]	—	-106.1	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1] [4]	—	0.80	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1] [5] [4] [6]	—	-13.4	—	dB
		Interferer is reference signal at -1 MHz offset[1] [5] [4] [6]	—	-13.3	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1] [5] [4] [6]	—	-52.1	—	dB
		Interferer is reference signal at -2 MHz offset[1] [5] [4] [6]	—	-55.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1] [5] [4] [6]	—	-52.3	—	dB
		Interferer is reference signal at -3 MHz offset[1] [5] [4] [6]	—	-60.2	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1] [6]	—	-51.4	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1] [6]	—	-52.3	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1] [6]	—	-52.1	—	dB

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -79 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.

4.13.2.6 RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.28. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 1% PER	RX_{SAT}	Signal is reference signal[1]. Packet length is 20 octets	—	10	—	dBm
Sensitivity, 1% PER	SENS	Signal is reference signal. Packet length is 20 octets	—	-102.2	—	dBm
Co-channel interferer rejection, 1% PER	CCR	Desired signal 3 dB above sensitivity limit	—	-1.86	—	dB
High-side adjacent channel rejection, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	ACR_{P1}	Interferer is reference signal at +1 channel-spacing	—	33.6	—	dB
Low-side adjacent channel rejection, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	ACR_{M1}	Interferer is reference signal at -1 channel-spacing	—	34.8	—	dB
Alternate channel rejection, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	ACR_2	Interferer is reference signal at ± 2 channel-spacing	—	46.3	—	dB
Image rejection , 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	IR	Interferer is CW in image band[3]	—	38.3	—	dB
Blocking rejection of all other channels, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]. Interferer is reference signal	BLOCK	Interferer frequency < Desired frequency - 3 channel-spacing	—	53.3	—	dB
		Interferer frequency > Desired frequency + 3 channel-spacing	—	52.7	—	dB
RSSI resolution	$RSSI_{RES}$	-100 dBm to +5 dBm	—	0.25	—	dB
RSSI accuracy in the linear region as defined by 802.15.4-2020	$RSSI_{LIN}$		—	+/-6	—	dB

Note:

1. Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksymbols/s.
2. Reference sensitivity level is -85 dBm.
3. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency ± 5 MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.

4.14 2.4 GHz RF Transceiver Characteristics for WLCSP39 Package

4.14.1 RF Transmitter Characteristics for WLCSP39 Package

4.14.1.1 WLCSP39 Package RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.29. WLCSP39 Package RF Transmitter General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		2400	—	2483.5	MHz
Maximum TX power[1]	$POUT_{MAX}$	High-power PA	—	4.2	—	dBm
		0 dBm PA	—	0.32	—	dBm
Minimum active TX power	$POUT_{MIN}$	High-power PA	—	-30.7	—	dBm
		0 dBm PA	—	-27.8	—	dBm
Output power variation vs supply voltage variation, frequency = 2450 MHz	$POUT_{VAR\_V}$	4 dBm PA output power, using DCDC with VREGVDD swept from 1.8 to 3.0 V	—	0.01	—	dB
		0 dBm PA output power, using DCDC with VREGVDD swept from 1.8 to 3.0 V	—	0.01	—	dB
Output power variation vs temperature, Frequency = 2450 MHz	$POUT_{VAR\_T}$	High-power PA at 4 dBm, (-40 to +125 °C)	—	0.76	—	dB
		0 dBm PA at 0 dBm, (-40 to +125 °C)	—	0.89	—	dB
		High-power PA at 4 dBm, (-40 to +85 °C)	—	0.53	—	dB
		0 dBm PA at 0 dBm, (-40 to +85 °C)	—	0.62	—	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	High-power PA, 4 dBm	—	0.12	—	dB
		0 dBm PA, 0 dBm	—	0.04	—	dB
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz.	—	-47	—	dBm
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30-88 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-47	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission CW carrier, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-26	—	dBc
Spurious emissions per ETSI EN300.440	$SPUR_{ETSI440}$	47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-60	—	dBm
		25-1000 MHz, excluding above frequencies. P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-42	—	dBm
		1G-14G, P_{out} = $POUT_{MAX}$, Test Frequency = 2450 MHz	—	-36	—	dBm
Spurious emissions out-of-band, per ETSI 300.328	$SPUR_{ETSI328}$	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-862 MHz, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-60	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 862-1000 MHz , P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-42	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = $POUT_{MAX}$, Test Frequency = 2440 MHz	—	-36	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = $POUT_{MAX}$, Test Frequency = 2402 and 2480 MHz	—	-16	—	dBm

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this data sheet can be found in the Max TX Power column of the Ordering Information Table.

4.14.1.2 WLCSP39 Package RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.30. WLCSP39 Package RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 4 dBm	—	678	—	kHz
		P_{out} = 0 dBm	—	678	—	kHz
Power spectral density limit	PSD_{LIMIT}	P_{out} = 4 dBm, Per FCC part 15.247 at 4 dBm	—	-1.6	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-6.4	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	4.8	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 4 dBm 99% BW at highest and lowest channels in band	—	1.02	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	1.03	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	P_{out} = 4 dBm, Inband spurs at ± 2 MHz	—	-44.2	—	dBm
		P_{out} = 0 dBm, Inband spurs at ± 2 MHz	—	-49.1	—	dBm
		P_{out} = 4 dBm Inband spurs at ± 3 MHz	—	-49.4	—	dBm
		P_{out} = 0 dBm Inband spurs at ± 3 MHz	—	-54.2	—	dBm

Note:

1. Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.14.1.3 WLCSP39 Package RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.31. WLCSP39 Package RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 4 dBm	—	1420	—	kHz
		P_{out} = 0 dBm	—	1420	—	kHz
Power spectral density limit	PSD_{LIMIT}	P_{out} = 4 dBm, Per FCC part 15.247 at 4 dBm	—	-4.8	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-9.5	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	3.7	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 4 dBm 99% BW at highest and lowest channels in band	—	2.05	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	2.05	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	P_{out} = 4 dBm, Inband spurs at ± 4 MHz	—	-42.3	—	dBm
		P_{out} = 0 dBm, Inband spurs at ± 4 MHz	—	-47.1	—	dBm
		P_{out} = 4 dBm Inband spurs at ± 6 MHz	—	-48.2	—	dBm
		P_{out} = 0 dBm Inband spurs at ± 6 MHz	—	-53.1	—	dBm

Note:

1. Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.14.1.4 WLCSP39 Package RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.32. WLCSP39 Package RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 4 dBm	—	711	—	kHz
		P_{out} = 0 dBm	—	711	—	kHz
Power spectral density limit	PSD_{LIMIT}	P_{out} = 4 dBm, Per FCC part 15.247 at 4 dBm	—	-1.8	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-6.6	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	4.7	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 4 dBm 99% BW at highest and lowest channels in band	—	1.04	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	1.04	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	P_{out} = 4 dBm, Inband spurs at ± 2 MHz	—	-44.2	—	dBm
		P_{out} = 0 dBm, Inband spurs at ± 2 MHz	—	-49.1	—	dBm
		P_{out} = 4 dBm Inband spurs at ± 3 MHz	—	-49.4	—	dBm
		P_{out} = 0 dBm Inband spurs at ± 3 MHz	—	-54.2	—	dBm

Note:

1. Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.14.1.5 WLCSP39 Package RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.33. WLCSP39 Package RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	P_{out} = 4 dBm	—	600	—	kHz
		P_{out} = 0 dBm	—	600	—	kHz
Power spectral density limit	PSD_{LIMIT}	P_{out} = 4 dBm, Per FCC part 15.247 at 4 dBm	—	-0.9	—	dBm/ 3kHz
		P_{out} = 0 dBm, Per FCC part 15.247 at 0 dBm	—	-5.7	—	dBm/ 3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	4.7	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	P_{out} = 4 dBm 99% BW at highest and lowest channels in band	—	1.03	—	MHz
		P_{out} = 0 dBm 99% BW at highest and lowest channels in band	—	1.03	—	MHz
In-band spurious emissions, with allowed exceptions[1]	$SPUR_{INB}$	P_{out} = 4 dBm, Inband spurs at ± 2 MHz	—	-43.7	—	dBm
		P_{out} = 0 dBm, Inband spurs at ± 2 MHz	—	-48.6	—	dBm
		P_{out} = 4 dBm Inband spurs at ± 3 MHz	—	-49.3	—	dBm
		P_{out} = 0 dBm Inband spurs at ± 3 MHz	—	-54.2	—	dBm

Note:

1. Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.14.1.6 WLCSP39 Package RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.34. WLCSP39 Package RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error vector magnitude per 802.15.4-2011	EVM	Average across frequency, signal is DSSS-OQPSK reference packet, P_{out} = 4 dBm	—	3.0	—	% rms
		Average across frequency, signal is DSSS-OQPSK reference packet, P_{out} = 0 dBm	—	3.0	—	% rms
Power spectral density limit	PSD_{LIMIT}	Relative, at carrier ± 3.5 MHz, P_{out} = 4 dBm	—	-52.0	—	dBc/ 100kHz
		Relative, at carrier ± 3.5 MHz, P_{out} = 0 dBm	—	-52.3	—	dBc/ 100kHz
		Absolute, at carrier ± 3.5 MHz, P_{out} = 4 dBm	—	-57.3	—	dBm/ 100kHz
		Absolute, at carrier ± 3.5 MHz, P_{out} = 0 dBm	—	-62.3	—	dBm/ 100kHz
		Per FCC part 15.247, P_{out} = 4 dBm	—	-5.2	—	dBm/ 3kHz
		Per FCC part 15.247, P_{out} = 0 dBm	—	-9.9	—	dBm/ 3kHz
		ETSI 300.328 P_{out} = 4 dBm	—	3.0	—	dBm
		ETSI 300.328 P_{out} = 0 dbm	—	-1.7	—	dBm
Occupied channel bandwidth per ETSI EN300.328	$OCP_{ETSI328}$	99% BW at highest and lowest channels in band, P_{out} = 4 dBm	—	2.21	—	MHz
		99% BW at highest and lowest channels in band, P_{out} = 0 dBm	—	2.21	—	MHz

4.14.2 RF Receiver Characteristics for WLCSP39 Package

4.14.2.1 WLCSP39 Package RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.35. WLCSP39 Package RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		2400	—	2483.5	MHz
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	—	-63	—	dBm
		1 GHz to 12 GHz	—	-53	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216 MHz to 960 MHz, conducted measurement	—	-47	—	dBm
		Above 960 MHz, conducted measurement.	—	-47	—	dBm
2GFSK Sensitivity	$SENS_{2GFSK}$	2 Mbps 2GFSK signal[1], 1% PER	—	-93.9	—	dBm
		250 kbps 2GFSK signal[2], 0.1% BER	—	-105.1	—	dBm

Note:

1. Reference signal is 2 Mbps 2GFSK, BT=0.5, mi=1.0, Δf = ± 1 MHz, Channel bandwidth = 2.4 MHz.
2. Reference signal is 250 kbps 2GFSK, BT=0.5, mi=1.0, Δf = ± 125 kHz, Channel bandwidth = 350 kHz.

4.14.2.2 WLCSP39 Package RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz, Packet length is 255 bytes.

Table 4.36. WLCSP39 Package RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-99.6	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-98.1	—	dBm
		With non-ideal signals[3] [1]	—	-97.6	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1] [4]	—	7.9	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1] [5] [4] [6]	—	-7.2	—	dB
		Interferer is reference signal at -1 MHz offset[1] [5] [4] [6]	—	-7.0	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1] [5] [4] [6]	—	-41.6	—	dB
		Interferer is reference signal at -2 MHz offset[1] [5] [4] [6]	—	-40.0	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1] [5] [4] [6]	—	-46.44	—	dB
		Interferer is reference signal at -3 MHz offset[1] [5] [4] [6]	—	-46.2	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1] [6]	—	-24.1	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1] [6]	—	-41.6	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1] [6]	—	-7.2	—	dB
Intermodulation performance	IM	n = 3 (see note[7])	—	-16.6	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -67 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.
7. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.14.2.3 WLCSP39 Package RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz, Packet length is 255 bytes.

Table 4.37. WLCSP39 Package RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-96.8	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-95.2	—	dBm
		With non-ideal signals[3] [1]	—	-95	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1] [4]	—	8	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +2 MHz offset[1] [5] [4] [6]	—	-6.7	—	dB
		Interferer is reference signal at -2 MHz offset[1] [5] [4] [6]	—	-7.9	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +4 MHz offset[1] [5] [4] [6]	—	-41.7	—	dB
		Interferer is reference signal at -4 MHz offset[1] [5] [4] [6]	—	-44.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +6 MHz offset[1] [5] [4] [6]	—	-48.8	—	dB
		Interferer is reference signal at -6 MHz offset[1] [5] [4] [6]	—	-50.4	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1] [6]	—	-23.5	—	dB
Selectivity to image frequency ± 2 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz with 1 MHz precision[1] [6]	—	-41.7	—	dB
		Interferer is reference signal at image frequency -2 MHz with 1 MHz precision[1] [6]	—	-6.7	—	dB
Intermodulation performance	IM	n = 3 (see note[7])	—	-15.7	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -67 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.
7. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4

4.14.2.4 WLCSP39 Package RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz, Packet length is 255 bytes.

Table 4.38. WLCSP39 Package RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-103.1	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-101.9	—	dBm
		With non-ideal signals[3 1]	—	-100.8	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1 4]	—	2.0	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1 5 4 6]	—	-8.3	—	dB
		Interferer is reference signal at -1 MHz offset[1 5 4 6]	—	-8.2	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1 5 4 6]	—	-47.1	—	dB
		Interferer is reference signal at -2 MHz offset[1 5 4 6]	—	-50.1	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1 5 4 6]	—	-48.2	—	dB
		Interferer is reference signal at -3 MHz offset[1 5 4 6]	—	-54.0	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1 6]	—	-48.7	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1 6]	—	-48.2	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1 6]	—	-47.1	—	dB

Note:
1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -72 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.

4.14.2.5 WLCSP39 Package RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz, Packet length is 255 bytes.

Table 4.39. WLCSP39 Package RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal[1]	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload[2]	—	-107.3	—	dBm
		Signal is reference signal, 255 byte payload[1]	—	-107.0	—	dBm
		With non-ideal signals[3] [1]	—	-106.4	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes)[1] [4]	—	0.3	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset[1] [5] [4] [6]	—	-13.8	—	dB
		Interferer is reference signal at -1 MHz offset[1] [5] [4] [6]	—	-13.7	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset[1] [5] [4] [6]	—	-53.0	—	dB
		Interferer is reference signal at -2 MHz offset[1] [5] [4] [6]	—	-56.1	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset[1] [5] [4] [6]	—	-52.7	—	dB
		Interferer is reference signal at -3 MHz offset[1] [5] [4] [6]	—	-59.0	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision[1] [6]	—	-52.8	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision[1] [6]	—	-52.7	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision[1] [6]	—	-53.0	—	dB

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -79 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.

4.14.2.6 WLCSP39 Package RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz.

Table 4.40. WLCSP39 Package RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 1% PER	RX_{SAT}	Signal is reference signal[1]. Packet length is 20 octets	—	10	—	dBm
Sensitivity, 1% PER	SENS	Signal is reference signal. Packet length is 20 octets	—	-102.7	—	dBm
Co-channel interferer rejection, 1% PER	CCR	Desired signal 3 dB above sensitivity limit	—	-1.1	—	dB
High-side adjacent channel rejection, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	ACR_{P1}	Interferer is reference signal at +1 channel-spacing	—	33.9	—	dB
Low-side adjacent channel rejection, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	ACR_{M1}	Interferer is reference signal at -1 channel-spacing	—	35.6	—	dB
Alternate channel rejection, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	ACR_2	Interferer is reference signal at ± 2 channel-spacing	—	46.6	—	dB
Image rejection , 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]	IR	Interferer is CW in image band[3]	—	38.5	—	dB
Blocking rejection of all other channels, 1% PER. Desired is reference signal at 3 dB above reference sensitivity level[2]. Interferer is reference signal	BLOCK	Interferer frequency < Desired frequency - 3 channel-spacing	—	53.4	—	dB
		Interferer frequency > Desired frequency + 3 channel-spacing	—	52.9	—	dB
RSSI resolution	$RSSI_{RES}$	-100 dBm to +5 dBm	—	0.25	—	dB
RSSI accuracy in the linear region as defined by 802.15.4-2020	$RSSI_{LIN}$		—	+/-6	—	dB

Note:

1. Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksymbols/s.
2. Reference sensitivity level is -85 dBm.
3. Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency ± 5 MHz on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.

4.15 Oscillators

4.15.1 High Frequency Crystal Oscillator

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.41. High Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{HFXO}	see note[1]	—	38.4	—	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO_38M4}	38.4 MHz, C_L = 10 pF[2 3]	—	40	60	Ω
Supported range of crystal load capacitance[4]	C_{L_HFXO}	38.4 MHz, ESR = 40 Ohm[3]	—	10	—	pF
Supply Current	I_{HFXO}		—	415	—	µA
Startup Time[5]	$T_{STARTUP}$	38.4 MHz, ESR = 40 Ω, C_L = 10 pF	—	160	—	µs
On-chip tuning cap step size[6]	SS_{HFXO}		—	0.04	—	pF

Note:

1. The BLE radio requires a 38.4 MHz crystal with a tolerance of ± 50 ppm over temperature and aging. Please use a crystal with the recommended frequency and tolerance.
2. The crystal should have a maximum ESR less than or equal to this maximum rating.
3. RF performance characteristics have been determined using crystals with an ESR of 40 Ω and C_L of 10 pF.
4. Total load capacitance as seen by the crystal.
5. Startup time does not include time implemented by programmable TIMEOUTSTEADY delay.
6. The tuning step size is the effective step size when incrementing both of the tuning capacitors by one count. The step size for the each of the individual tuning capacitors is twice this value.

4.15.2 Low Frequency Crystal Oscillator

Table 4.42. Low Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{LFXO}		—	32.768	—	kHz
Supported Crystal equivalent series resistance (ESR)	ESR_{LFXO}	GAIN = 0	—	—	80	kΩ
		GAIN = 1 to 3	—	—	100	kΩ
Supported range of crystal load capacitance [1]	C_{L_LFXO}	GAIN = 0	4	—	6	pF
		GAIN = 1	6	—	10	pF
		GAIN = 2 (see note[2])	10	—	12.5	pF
		GAIN = 3 (see note[2])	12.5	—	18	pF
Current consumption	I_{CL12p5}	ESR = 70 kΩ, C_L = 12.5 pF, GAIN[3] = 2, AGC[4] = 1	—	254	—	nA
Startup Time	$T_{STARTUP}$	ESR = 70 kΩ, C_L = 7 pF, GAIN[3] = 1, AGC[4] = 1	—	43	—	ms
On-chip tuning cap step size	SS_{LFXO}		—	0.26	—	pF
On-chip tuning capacitor value at minimum setting[5]	C_{LFXO_MIN}	CAPTUNE = 0	—	4	—	pF
On-chip tuning capacitor value at maximum setting[5]	C_{LFXO_MAX}	CAPTUNE = 0x4F	—	24.5	—	pF

Note:

1. Total load capacitance seen by the crystal
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register
4. In LFXO_CFG Register
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal

4.15.3 High Frequency RC Oscillator (HFRCO)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.43. High Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	F_{HFRCO_ACC}	For all production calibrated frequencies	-3	—	3	%
Current consumption on all supplies[1]	I_{HFRCO}	F_{HFRCO} = 4 MHz	—	28	—	µA
		F_{HFRCO} = 5 MHz	—	30	—	µA
		F_{HFRCO} = 7 MHz	—	60	—	µA
		F_{HFRCO} = 10 MHz	—	66	—	µA
		F_{HFRCO} = 13 MHz	—	79	—	µA
		F_{HFRCO} = 16 MHz	—	88	—	µA
		F_{HFRCO} = 19 MHz	—	92	—	µA
		F_{HFRCO} = 20 MHz	—	105	—	µA
		F_{HFRCO} = 26 MHz	—	118	—	µA
		F_{HFRCO} = 32 MHz	—	141	—	µA
		F_{HFRCO} = 38 MHz	—	172	—	µA
		F_{HFRCO} = 80 MHz	—	289	—	µA
Clock Out current for HFRCODPLL[2]	$I_{CLKOUT\_HFRCODPLL}$	FORCEEN bit of HFRCO0_CTRL = 1	—	3.0	—	µA/MHz
Startup Time[3]	$T_{STARTUP}$	FREQRANGE = 0 to 7	—	1.2	—	µs
		FREQRANGE = 8 to 15	—	0.6	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Band Frequency Limits[4]	f_{HFRCO_BAND}	FREQRANGE = 0	3.71	—	5.24	MHz
		FREQRANGE = 1	4.39	—	6.26	MHz
		FREQRANGE = 2	5.25	—	7.55	MHz
		FREQRANGE = 3	6.22	—	9.01	MHz
		FREQRANGE = 4	7.88	—	11.6	MHz
		FREQRANGE = 5	9.9	—	14.6	MHz
		FREQRANGE = 6	11.5	—	17.0	MHz
		FREQRANGE = 7	14.1	—	20.9	MHz
		FREQRANGE = 8	16.4	—	24.7	MHz
		FREQRANGE = 9	19.8	—	30.4	MHz
		FREQRANGE = 10	22.7	—	34.9	MHz
		FREQRANGE = 11	28.6	—	44.4	MHz
		FREQRANGE = 12	33.0	—	51.0	MHz
		FREQRANGE = 13	42.2	—	64.6	MHz
		FREQRANGE = 14	48.8	—	74.8	MHz
		FREQRANGE = 15	57.6	—	87.4	MHz

Note:

1. Does not include additional clock tree current. See specifications for additional current when selected as a clock source for a particular clock multiplexer.
2. When the HFRCO is enabled for characterization using the FORCEEN bit, the total current will be the HFRCO core current plus the specified CLKOUT current. When the HFRCO is enabled on demand, the clock current may be different.
3. Hardware delay ensures settling to within ± 0.5%. Hardware also enforces this delay on a band change.
4. The frequency band limits represent the lowest and highest frequency which each band can achieve over the operating range.

4.15.4 Fast Start_Up RC Oscillator (FSRCO)

Table 4.44. Fast Start_Up RC Oscillator (FSRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FSRCO frequency	F_{FSRCO}		17.2	20	21.2	MHz

4.15.5 Precision Low Frequency RC Oscillator (LFRCO)

Table 4.45. Precision Low Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		—	32.768	—	kHz
Frequency accuracy	F_{LFRCO_ACC}	Normal mode	-3	—	3	%
		Precision mode[1], across operating temperature range[2]	-500	—	500	ppm
Startup time	$t_{STARTUP}$	Normal mode	—	211	—	µs
		Precision mode[1]	—	11.7	—	ms
Current consumption	I_{LFRCO}	Normal mode	—	183	—	nA
		Precision mode[1], T = stable at 25 °C [3]	—	664	—	nA

Note:

1. The LFRCO operates in high-precision mode when CFG_HIGHPRECEN is set to 1. High-precision mode is not available in EM4.
2. Includes ± 40 ppm frequency tolerance of the HFXO crystal.
3. Includes periodic re-calibration against HFXO crystal oscillator.

4.15.6 Ultra Low Frequency RC Oscillator

Table 4.46. Ultra Low Frequency RC Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation Frequency	F_{ULFRCO}		0.944	1.0	1.095	kHz

4.16 GPIO with 3 V Nominal IOVDD

Table 4.47. GPIO with 3 V Nominal IOVDD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IOVDD Supply Range	V_{IO}		1.71	3.0	3.8	V
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, IOVDD = 1.71 V	—	1.9	—	nA
		MODEx = DISABLED, IOVDD = 3.0 V	—	2.5	—	nA
		MODEx = DISABLED, IOVDD = 3.8 V T_A = 85 °C	—	—	250	nA
		MODEx = DISABLED, IOVDD = 3.8 V T_A = 125 °C	—	—	250	nA
Input low voltage[1]	V_{IL}	Any GPIO pin	—	—	0.3 * IOVDD	V
		RESETn	—	—	0.3 * DVDD	V
Input high voltage[1]	V_{IH}	Any GPIO pin	0.7 * IOVDD	—	—	V
		RESETn	0.7 * DVDD	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05 * IOVDD	—	—	V
		RESETn	0.05 * DVDD	—	—	V
Output high voltage	V_{OH}	Sourcing 20 mA, IOVDD = 3.0 V	0.8 * IOVDD	—	—	V
		Sourcing 8 mA, IOVDD = 1.71 V	0.6 * IOVDD	—	—	V
Output low voltage	V_{OL}	Sinking 20 mA, IOVDD = 3.0 V	—	—	0.2 * IOVDD	V
		Sinking 8 mA, IOVDD = 1.71 V	—	—	0.4 * IOVDD	V
GPIO rise time	T_{GPIO_RISE}	IOVDD = 3.0 V, C_{load} = 50 pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
		IOVDD = 1.71 V, C_{load} = 50 pF, SLEWRATE = 4, 10% to 90%	—	13	—	ns
GPIO fall time	T_{GPIO_FALL}	IOVDD = 3.0 V, C_{load} = 50 pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
		IOVDD = 1.71 V, C_{load} = 50 pF, SLEWRATE = 4, 90% to 10%	—	11.9	—	ns
Pull up/down resistance[2]	R_{PULL}	Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0.	35	44	55	kΩ
		RESETn pin. Pull-up to DVDD	34	44	60	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RESETn low time to ensure pin reset	T_{RESET}		100	—	—	ns

Note:

1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD.

4.17 GPIO with 1.5 V Nominal IOVDD

Table 4.48. GPIO with 1.5 V Nominal IOVDD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IOVDD Supply Range	V_{IO}	IOVDD BOD Disabled	1.175	1.5	1.85	V
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, IOVDD = 1.175 V	—	1.4	—	nA
		MODEx = DISABLED, IOVDD = 1.5 V	—	1.5	—	nA
		MODEx = DISABLED, IOVDD = 1.71 V T_A = 85 °C	—	—	200	nA
		MODEx = DISABLED, IOVDD = 1.71 V T_A = 125 °C	—	—	200	nA
Input low voltage	V_{IL}		—	—	0.3 * IOVDD	V
Input high voltage	V_{IH}		0.7 * IOVDD	—	—	V
Hysteresis of input voltage	V_{HYS}		0.05 * IOVDD	—	—	V
Output high voltage	V_{OH}	Sourcing 8 mA, IOVDD = 1.71 V	0.6 * IOVDD	—	—	V
		Sourcing 4 mA, IOVDD ≥ 1.175 V	0.6 * IOVDD	—	—	V
Output low voltage	V_{OL}	Sinking 8 mA, IOVDD = 1.71 V	—	—	0.4 * IOVDD	V
		Sinking 4 mA, IOVDD ≥ 1.175 V	—	—	0.4 * IOVDD	V
Pull up/down resistance	R_{PULL}	Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0.	—	42	—	kΩ

4.18 Analog to Digital Converter (IADC)

Specified at 1 Msps, ADCCLK = 10 MHz, OSR=2, unless otherwise indicated.

Table 4.49. Analog to Digital Converter (IADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main analog supply	V_{AVDD}	Normal Mode	1.71	—	3.8	V
Maximum Input Range[1]	V_{IN_MAX}	Maximum allowable input voltage	0	—	AVDD	V
Full-Scale Voltage	V_{FS}	Voltage required for Full-Scale measurement	—	V_{REF} / Gain	—	V
Input Measurement Range	V_{IN}	Differential Mode - Plus and Minus inputs	$-V_{FS}$	—	$+V_{FS}$	V
		Single Ended Mode - One input tied to ground	0	—	V_{FS}	V
Input Sampling Capacitance	Cs	Analog Gain = 1x	—	1.8	—	pF
		Analog Gain = 2x	—	3.6	—	pF
		Analog Gain = 3x	—	5.4	—	pF
		Analog Gain = 4x	—	7.2	—	pF
		Analog Gain = 0.5x	—	0.9	—	pF
ADC clock frequency	f_{ADC_CLK}	Gain = 1x or 0.5x	—	—	10	MHz
		Gain = 2x	—	—	5	MHz
		Gain = 3x or 4x	—	—	2.5	MHz
Input sampling frequency	f_S		—	$f_{ADC\_CLK}/4$	—	MHz
Throughput rate	f_{SAMPLE}	f_{ADC_CLK} = 10 MHz, OSR = 2	—	—	1	Msps
		f_{ADC_CLK} = 10 MHz, OSR = 32	—	—	76.9	ksps
Current from all supplies, Continuous operation	I_{ADC_CONT}	1 Msps, OSR = 2, f_{ADC_CLK} = 10 MHz	—	290	385	μA
Current in Standby mode. ADC is not functional but can wake up in 1us.	I_{STBY}		—	16	—	μA
ADC Startup Time	$t_{startup}$	From power down state	—	5	—	μs
		From standby state	—	1	—	μs
ADC Resolution[2]	Resolution		—	12	—	bits
Differential Nonlinearity	DNL	Differential Input, OSR = 2, (No missing codes) .	-0.998	+/- 0.25	1.5	LSB12
Integral Nonlinearity	INL	Differential Input, OSR = 2.	-2.5	+/- 0.65	2.5	LSB12
Effective number of bits[3]	ENOB	Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V. OSR=2	10.5	11.7	—	bits
		Differential Input. Gain = 1x, OSR = 32, f_{IN} = 2.5 kHz, Internal VREF = 1.21 V.	—	13.5	—	bits
		Differential Input. Gain = 1x, OSR = 32, f_{IN} = 2.5 kHz, External VREF = 1.25 V.	—	14.3	—	bits

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal to Noise + Distortion Ratio[3]	SNDR	Differential Input. Gain=1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	65	72.3	—	dB
		Differential Input. Gain=2x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	72.3	—	dB
		Differential Input. Gain=4x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	68.8	—	dB
		Differential Input. Gain=0.5x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	72.5	—	dB
Total Harmonic Distortion	THD	Differential Input. Gain=1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	—	-80.8	-70	dB
Spurious-Free Dynamic Range	SFDR	Differential Input. Gain=1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF=1.21V	72	86.5	—	dB
Common Mode Rejection Ratio	CMRR	DC to 100 Hz	—	87.0	—	dB
		AC high frequency	—	68.6	—	dB
Power Supply Rejection Ratio	PSRR	DC to 100 Hz	—	80.4	—	dB
		AC high frequency, using VREF pad.	—	33.4	—	dB
		AC high frequency, using internal VBGR.	—	65.2	—	dB
Gain Error	GE	GAIN=1 and 0.5, using external VREF	-0.3	0.0165	0.3	%
		GAIN=2, using external VREF	-0.4	0.0426	0.4	%
		GAIN=3, using external VREF	-0.7	0.0864	0.7	%
		GAIN=4, using external VREF	-1.1	0.107	1.1	%
		Internal VREF[4], all GAIN settings	-1.5	0.064	1.5	%
Offset Error	OFFSET	GAIN = 1 and 0.5, Differential Input	-3	-0.45	3	LSB12
		GAIN = 2, Differential Input	-4	-0.44	4	LSB12
		GAIN = 3, Differential Input	-4	-0.47	4	LSB12
		GAIN = 4, Differential Input	-4	-0.47	4	LSB12
External reference voltage range[1]	V_{EVREF}		1.0	—	AVDD	V
Internal Reference voltage	V_{IVREF}		—	1.21	—	V

Note:

1. When inputs are routed to external GPIO pins, the maximum pin voltage is limited to the lower of the IOVDD and AVDD supplies.
2. ADC output resolution depends on the OSR and digital averaging settings. With no digital averaging, ADC output resolution is 12 bits at OSR=2, 13 bits at OSR = 4, 14 bits at OSR = 8, 15 bits at OSR = 16, 16 bits at OSR = 32 and 17 bits at OSR = 64. Digital averaging has a similar impact on ADC output resolution. See the product reference manual for additional details.
3. The relationship between ENOB and SNDR is specified according to the equation: ENOB = (SNDR - 1.76) / 6.02.
4. Includes error from internal VREF drift.

4.19 Analog Comparator (ACMP)

Table 4.50. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ACMP Supply current	I_{ACMP}	BIAS = 0 [1], HYST = DISABLED (100 °C max)	—	63	—	nA
		BIAS = 1 [1], HYST = DISABLED	—	252	—	nA
		BIAS = 2 [1], HYST = DISABLED	—	628	—	nA
		BIAS = 3 [1], HYST = DISABLED	—	2.3	—	µA
		BIAS = 4, HYST = DISABLED	—	5.2	—	µA
		BIAS = 5, HYST = DISABLED	—	10	—	µA
		BIAS = 6, HYST = DISABLED	—	25	—	µA
		BIAS = 7, HYST = DISABLED	—	47	80	µA
ACMP Supply current with Hysteresis	I_{ACMP_WHYS}	BIAS = 0 [1], HYST = SYM30MV (100 °C max)	—	81	—	nA
		BIAS = 1 [1], HYST = SYM30MV	—	346	—	nA
		BIAS = 2 [1], HYST = SYM30MV	—	871	—	nA
		BIAS = 3 [1], HYST = SYM30MV	—	3.23	—	µA
		BIAS = 4, HYST = SYM30MV	—	7.1	—	µA
		BIAS = 5, HYST = SYM30MV	—	15	—	µA
		BIAS = 6, HYST = SYM30MV	—	36	—	µA
		BIAS = 7, HYST = SYM30MV	—	67	—	µA
Current consumption from VREFDIV in continuous mode	$I_{VREFDIV}$	NEGSEL = VREFDIVAVDD	—	3.2	—	µA
		NEGSEL = VREFDIV1V25	—	4.2	—	µA
		NEGSEL = VREFDIV2V5	—	7.0	—	µA
Current consumption from VREFDIV in sample/hold mode	$I_{VREFDIV\_SH}$	NEGSEL = VREFDIV2V5LP	—	72	—	nA
		NEGSEL = VREFDIV1V25LP	—	66	—	nA
		NEGSEL = VREFDIVAVDDLP	—	68	—	nA
Current consumption from VSENSEDIV in continuous mode	$I_{VSENSEDIV}$	NEGSEL = VSENSE01DIV4	—	1.7	—	µA
Current consumption from VSENSEDIV in sample/hold mode	$I_{VSENSEDIV\_SH}$	NEGSEL = VSENSE01DIV4LP	—	55	—	nA
Hysteresis (BIAS = 0)	V_{HYST_0}	HYST = SYM10MV[2]	—	20	—	mV
		HYST = SYM20MV[2]	—	38	—	mV
		HYST = SYM30MV[2]	—	54	—	mV
Reference Voltage	$V_{ACMPREF}$	Internal 1.25 V Reference	1.18	1.25	1.3	V
		Internal 2.5 V Reference	2.36	2.5	2.61	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input offset voltage	V_{OFFSET}	BIAS = 0, VCM = 0.15 to AVDD - 0.15 V	-25	—	25	mV
		BIAS = 2, VCM = 0.15 to AVDD - 0.15 V	-25	—	25	mV
		BIAS = 4, VCM = 0.15 to AVDD - 0.15 V	-25	—	25	mV
		BIAS = 7, VCM = 0.15 to AVDD - 0.15 V	-25	—	25	mV
Input Range	V_{IN}	Input Voltage Range	0	—	AVDD	V
Comparator delay with 100 mV overdrive	T_{DELAY}	BIAS = 0, (100 °C max)	—	11	—	µs
		BIAS = 1	—	2.9	—	µs
		BIAS = 2	—	1.4	—	µs
		BIAS = 3	—	0.56	—	µs
		BIAS = 4	—	211	—	ns
		BIAS = 5	—	120	—	ns
		BIAS = 6	—	70	—	ns
		BIAS = 7	—	51	—	ns
Capacitive Sense Oscillator Resistance[3]	$R_{CSRESSEL}$	CSRESSEL = 0	—	14	—	kΩ
		CSRESSEL = 1	—	24	—	kΩ
		CSRESSEL = 2	—	43	—	kΩ
		CSRESSEL = 3	—	60	—	kΩ
		CSRESSEL = 4	—	80	—	kΩ
		CSRESSEL = 5	—	99	—	kΩ
		CSRESSEL = 6	—	120	—	kΩ

Note:

1. When using the 1.25 V or 2.5 V VREF in continuous mode (VREFDIV1V25 or VREFDIV2V5) and BIAS < 4, an additional 1 µA of supply current is required.
2. V_{CM} = 1.25 V
3. Capacitive Sense has been deprecated and is not recommended for use

4.20 Temperature Sensor

Table 4.51. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature sensor range[1]	T_{RANGE}		-40	—	125	°C
Temperature sensor resolution	$T_{RESOLUTION}$		—	0.25	—	°C
Measurement noise (RMS)	T_{NOISE}	Single measurement	—	0.6	—	°C
		16-sample average (TEMPAVG-NUM = 0)	—	0.17	—	°C
		64-sample average (TEMPAVG-NUM = 1)	—	0.12	—	°C
Temperature offset	T_{OFF}	Mean error of uncorrected output across full temperature range	—	0.85	—	°C
Temperature sensor accuracy[2 3]	T_{ACC}	Direct output accuracy after mean error (T_{OFF}) removed	—	+/-3	—	°C
		After linearization in software, no calibration	—	+/-2	—	°C
		After linearization in software, with single-temperature calibration at 25 °C[4]	—	+/-1.5	—	°C
Measurement interval	t_{MEAS}		—	250	—	ms

Note:

1. The sensor reports absolute die temperature in Kelvin (K). All specifications are in °C to match the units of the specified product temperature range.
2. Error is measured as the deviation of the mean temperature reading from the expected die temperature. Accuracy numbers represent statistical minimum and maximum using ± 4 standard deviations of measured error.
3. The raw output of the temperature sensor is a predictable curve. It can be linearized with a polynomial function for additional accuracy.
4. Assuming calibration accuracy of ± 0.25 °C.

4.21 Brown Out Detectors

4.21.1 DVDD BOD

BOD thresholds on DVDD in EM0 and EM1 only, unless otherwise noted. Typical conditions are at T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.52. DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{DVDD_BOD}	Supply Rising	—	1.67	1.71	V
		Supply Falling	1.62	1.65	—	V
BOD response time	$t_{DVDD\_BOD\_DELAY}$	Supply dropping at 100 mV/µs slew rate[1]	—	0.95	—	µs
BOD hysteresis	$V_{DVDD\_BOD\_HYST}$		—	20	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.21.2 LE DVDD BOD

BOD thresholds on DVDD pin for low energy modes EM2 to EM4, unless otherwise noted.

Table 4.53. LE DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	$V_{DVDD\_LE\_BOD}$	Supply Falling	1.5	—	1.71	V
BOD response time	$t_{DVDD\_LE\_BOD\_DELAY}$	Supply dropping at 2 mV/µs slew rate[1]	—	50	—	µs
BOD hysteresis	$V_{DVDD\_LE\_BOD\_HYST}$		—	20	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.21.3 AVDD and IOVDD BODs

BOD thresholds for AVDD BOD and IOVDD BOD. Available in all energy modes.

Table 4.54. AVDD and IOVDD BODs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{BOD}	Supply falling	1.45	—	1.71	V
BOD response time	t_{BOD_DELAY}	Supply dropping at 2 mV/µs slew rate[1]	—	50	—	µs
BOD hysteresis	V_{BOD_HYST}		—	20	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.22 PDM Timing Specifications

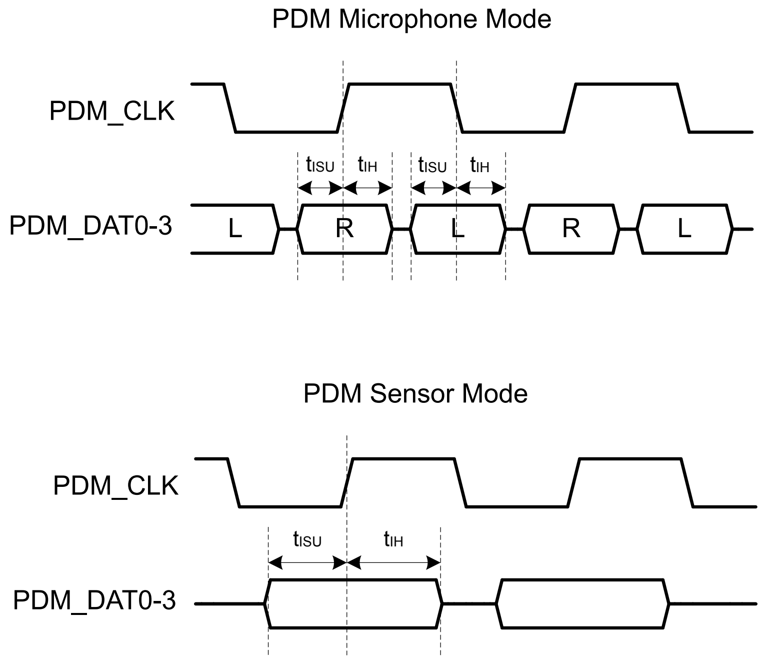


Figure 4.3. PDM Timing Diagrams

4.22.1 Pulse Density Modulator (PDM), Common DBUS

Timing specifications are for all PDM signals routed to the same DBUS (DBUSAB or DBUSCD), though routing to the same GPIO port is the optimal configuration. C_{LOAD} < 20 pF. System voltage scaling = VSCALE1 or VSCALE2. All GPIO set to slew rate = 6. Data delay (PDM_CFG1_DLYMUXSEL) = 0.

Table 4.55. Pulse Density Modulator (PDM), Common DBUS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PDM_CLK frequency during data transfer	F_{PDM_CLK}	Microphone mode	—	—	5	MHz
		Sensor mode	—	—	20	MHz
PDM_CLK duty cycle	DC_{PDM_CLK}		47.5	—	52.5	%
PDM_CLK rise time	t_R		—	—	5.5	ns
PDM_CLK fall time	t_F		—	—	5.5	ns
Input setup time	t_{ISU}	Microphone mode	30	—	—	ns
		Sensor mode	20	—	—	ns
Input hold time	t_{IH}		3	—	—	ns

4.23 USART SPI Main Timing

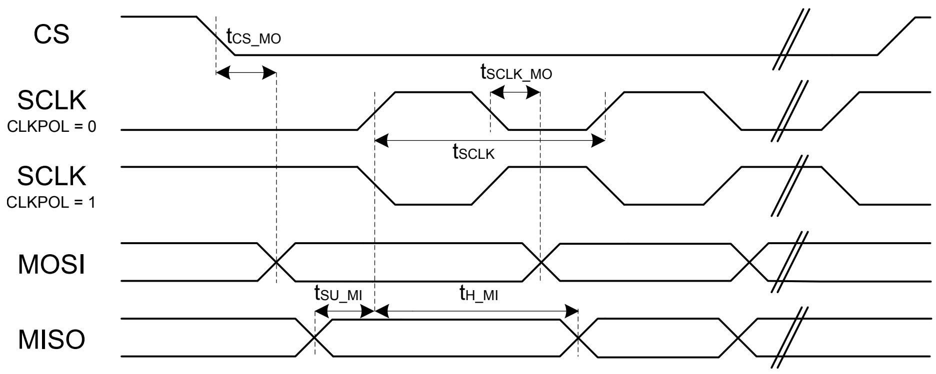


Figure 4.4. SPI Main Timing (SMSDELAY = 0)

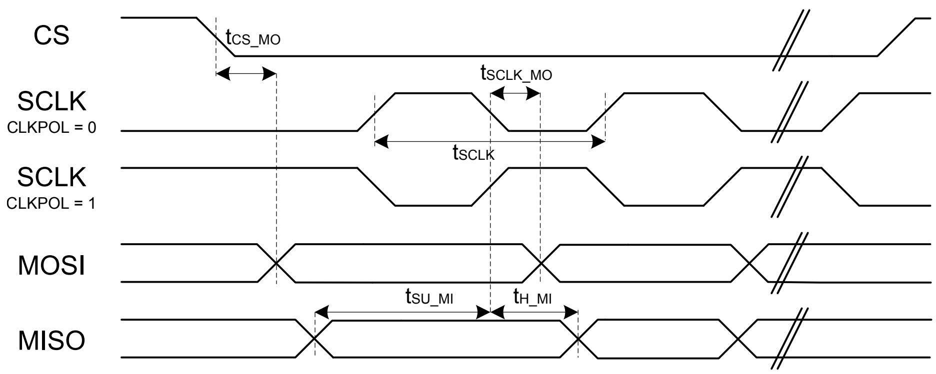


Figure 4.5. SPI Main Timing (SMSDELAY = 1)

4.23.1 USART SPI Main Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.56. USART SPI Main Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		2^*t_{PCLK}	—	—	ns
CS to MOSI[1 2]	t_{CS_MO}		-15	—	14	ns
SCLK to MOSI[1 2]	t_{SCLK_MO}		-7	—	13	ns
MISO setup time[1 2]	t_{SU_MI}	IOVDD = 1.8 V	40	—	—	ns
		IOVDD = 3.0 V	31	—	—	ns
MISO hold time[1 2]	t_{H_MI}		-9	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.23.2 USART SPI Main Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.57. USART SPI Main Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		2^*t_{PCLK}	—	—	ns
CS to MOSI[1 2]	t_{CS_MO}		-23	—	26	ns
SCLK to MOSI[1 2]	t_{SCLK_MO}		-10	—	22	ns
MISO setup time[1 2]	t_{SU_MI}	IOVDD = 1.8 V	48	—	—	ns
		IOVDD = 3.0 V	41	—	—	ns
MISO hold time[1 2]	t_{H_MI}		-9	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.24 USART SPI Secondary Timing

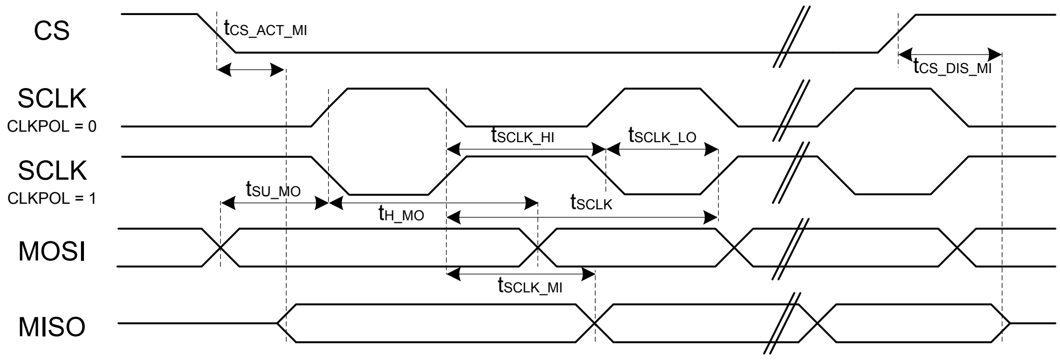


Figure 4.6. SPI Secondary Timing

4.24.1 USART SPI Secondary Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.58. USART SPI Secondary Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		6*t_{PCLK}	—	—	ns
SCLK high time[1 2 3]	t_{SCLK_HI}		2.5*t_{PCLK}	—	—	ns
SCLK low time[1 2 3]	t_{SCLK_LO}		2.5*t_{PCLK}	—	—	ns
CS active to MISO[1 2]	$t_{CS\_ACT\_MI}$		18	—	62	ns
CS disable to MISO[1 2]	$t_{CS\_DIS\_MI}$		15	—	54	ns
MOSI setup time[1 2]	t_{SU_MO}		7	—	—	ns
MOSI hold time[1 2 3]	t_{H_MO}		7	—	—	ns
SCLK to MISO[1 2 3]	t_{SCLK_MI}		15 + 1.5*t_{PCLK}	—	32 + 2.5*t_{PCLK}	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).
3. t_{PCLK} is one period of the selected PCLK.

4.24.2 USART SPI Secondary Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.59. USART SPI Secondary Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		6*t_{PCLK}	—	—	ns
SCLK high time[1 2 3]	t_{SCLK_HI}		2.5*t_{PCLK}	—	—	ns
SCLK low time[1 2 3]	t_{SCLK_LO}		2.5*t_{PCLK}	—	—	ns
CS active to MISO[1 2]	$t_{CS\_ACT\_MI}$		24	—	86	ns
CS disable to MISO[1 2]	$t_{CS\_DIS\_MI}$		21	—	76	ns
MOSI setup time[1 2]	t_{SU_MO}		11	—	—	ns
MOSI hold time[1 2 3]	t_{H_MO}		11	—	—	ns
SCLK to MISO[1 2 3]	t_{SCLK_MI}		18 + 1.5*t_{PCLK}	—	44 + 2.5*t_{PCLK}	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).
3. t_{PCLK} is one period of the selected PCLK.

4.25 EUSART SPI Main Timing

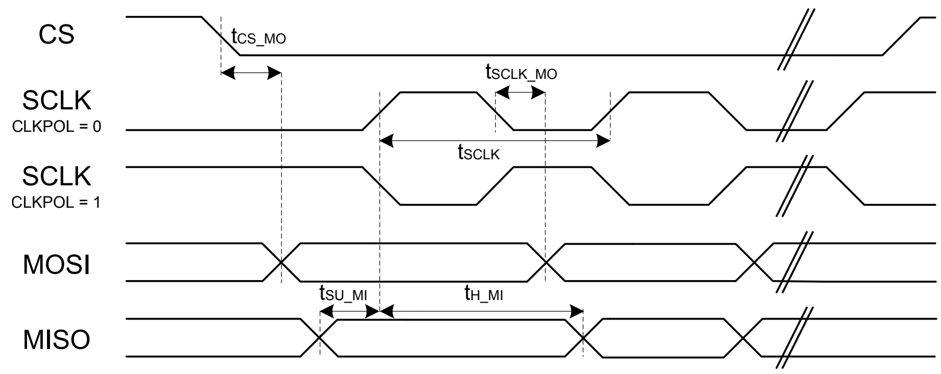


Figure 4.7. SPI Main Timing

4.25.1 EUSART SPI Main Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.60. EUSART SPI Main Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		t_{CLK}	—	—	ns
CS to MOSI[1 2]	t_{CS_MO}		-10.5	—	8.5	ns
SCLK to MOSI[1 2]	t_{SCLK_MO}		-2.5	—	8.5	ns
MISO setup time [1 2]	t_{SU_MI}		-6.5	—	—	ns
MISO hold time[1 2]	t_{H_MI}		-7	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.25.2 EUSART SPI Main Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.61. EUSART SPI Main Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		t_{CLK}	—	—	ns
CS to MOSI[1 2]	t_{CS_MO}		-19	—	14.5	ns
SCLK to MOSI[1 2]	t_{SCLK_MO}		-4	—	14	ns
MISO setup time [1 2]	t_{SU_MI}		8	—	—	ns
MISO hold time[1 2]	t_{H_MI}		7	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.26 EUSART SPI Secondary Timing

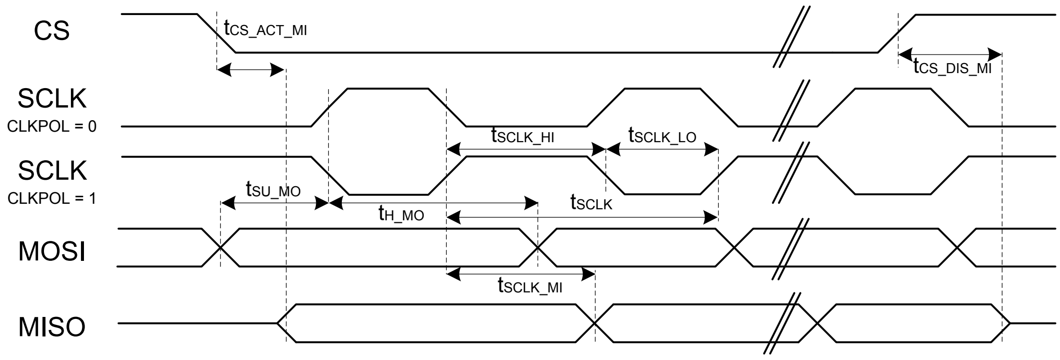


Figure 4.8. SPI Secondary Timing

4.26.1 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.62. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE2, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time[1 2]	t_{SCLK_HI}		50	—	—	ns
SCLK low time[1 2]	t_{SCLK_LO}		50	—	—	ns
CS active to MISO[1 2]	$t_{CS\_ACT\_MI}$		24	—	68	ns
CS disable to MISO[1 2]	$t_{CS\_DIS\_MI}$		5	—	31	ns
MOSI setup time[1 2]	t_{SU_MO}		3.5	—	—	ns
MOSI hold time[1 2]	t_{H_MO}		9	—	—	ns
SCLK to MISO[1 2]	t_{SCLK_MI}	IOVDD = 1.8 V	9	—	40	ns
		IOVDD = 3.3 V	9	—	30	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).

4.26.2 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.63. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE1, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time[1 2]	t_{SCLK_HI}		50	—	—	ns
SCLK low time[1 2]	t_{SCLK_LO}		50	—	—	ns
CS active to MISO[1 2]	$t_{CS\_ACT\_MI}$		25	—	88	ns
CS disable to MISO[1 2]	$t_{CS\_DIS\_MI}$		5	—	47	ns
MOSI setup time[1 2]	t_{SU_MO}		5.5	—	—	ns
MOSI hold time[1 2]	t_{H_MO}		15.5	—	—	ns
SCLK to MISO[1 2]	t_{SCLK_MI}	IOVDD = 1.8 V	10	—	50	ns
		IOVDD = 3.3 V	10	—	41	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).

4.26.3 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE0, IOVDD ≥ 1.8 V

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.64. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE0, IOVDD ≥ 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time[1 2]	t_{SCLK_HI}		100	—	—	ns
SCLK low time[1 2]	t_{SCLK_LO}		100	—	—	ns
CS active to MISO[1 2]	$t_{CS\_ACT\_MI}$		27	—	153	ns
CS disable to MISO[1 2]	$t_{CS\_DIS\_MI}$		7	—	96	ns
MOSI setup time[1 2]	t_{SU_MO}		10	—	—	ns
MOSI hold time[1 2]	t_{H_MO}		41	—	—	ns
SCLK to MISO[1 2]	t_{SCLK_MI}	IOVDD = 1.8 V	12	—	88	ns
		IOVDD = 3.3 V	12	—	80	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).

4.27 I2C Electrical Specifications

4.27.1 I2C Standard-mode (Sm)

CLHR set to 0 in the I2Cn_CTRL register.

Table 4.65. I2C Standard-mode (Sm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	µs
Repeated START condition hold time	t_{HD_STA}		4.0	—	—	µs
STOP condition set-up time	t_{SU_STO}		4.0	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.27.2 I2C Fast-mode (Fm)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.66. I2C Fast-mode (Fm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	µs
Repeated START condition hold time	t_{HD_STA}		0.6	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.27.3 I2C Fast-mode Plus (Fm+)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.67. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[1]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	µs
Repeated START condition hold time	t_{HD_STA}		0.26	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.28 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.28.1 Supply Current

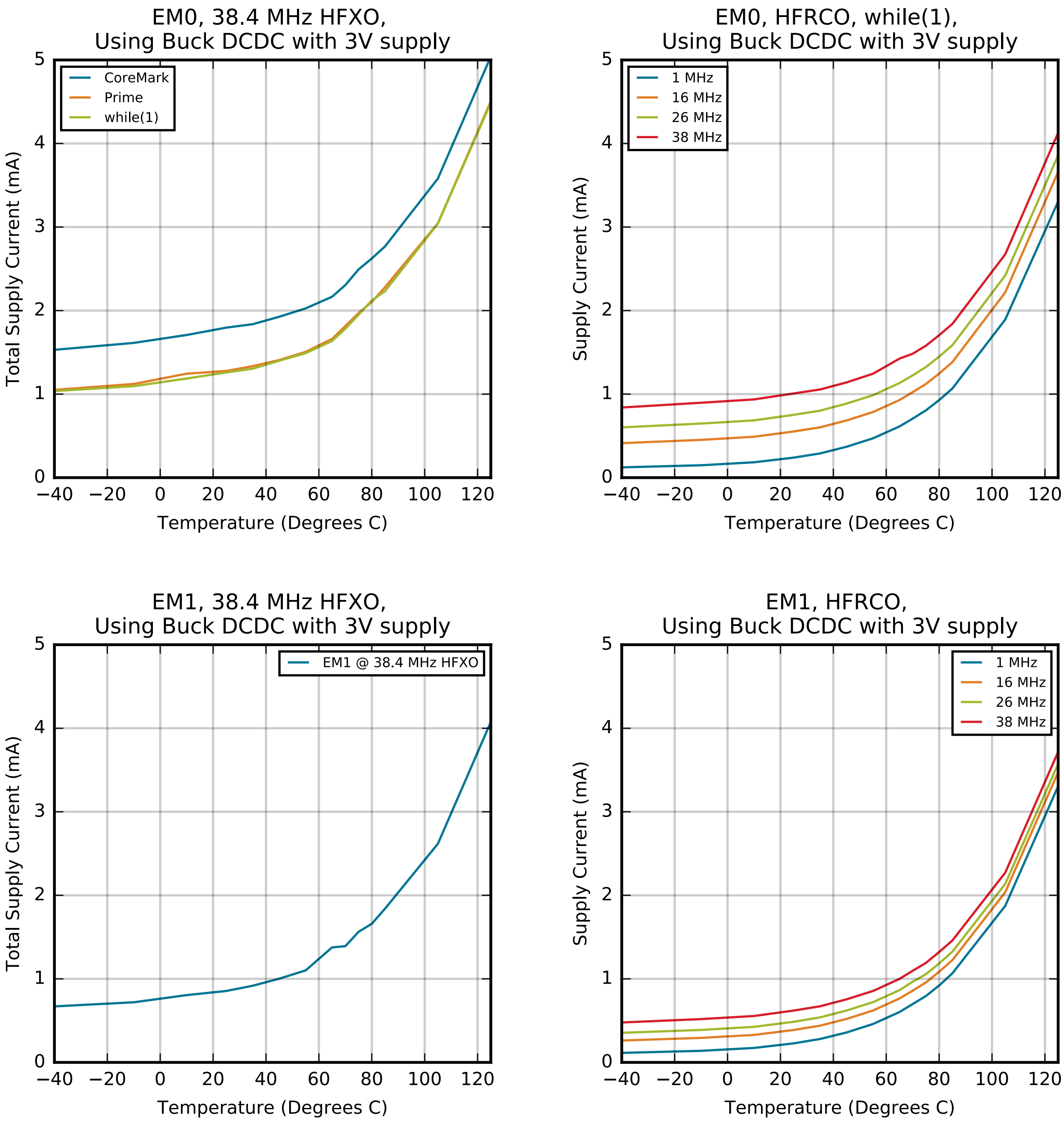


Figure 4.9. EM0 and EM1 Typical Supply Current vs. Temperature (Buck DCDC)

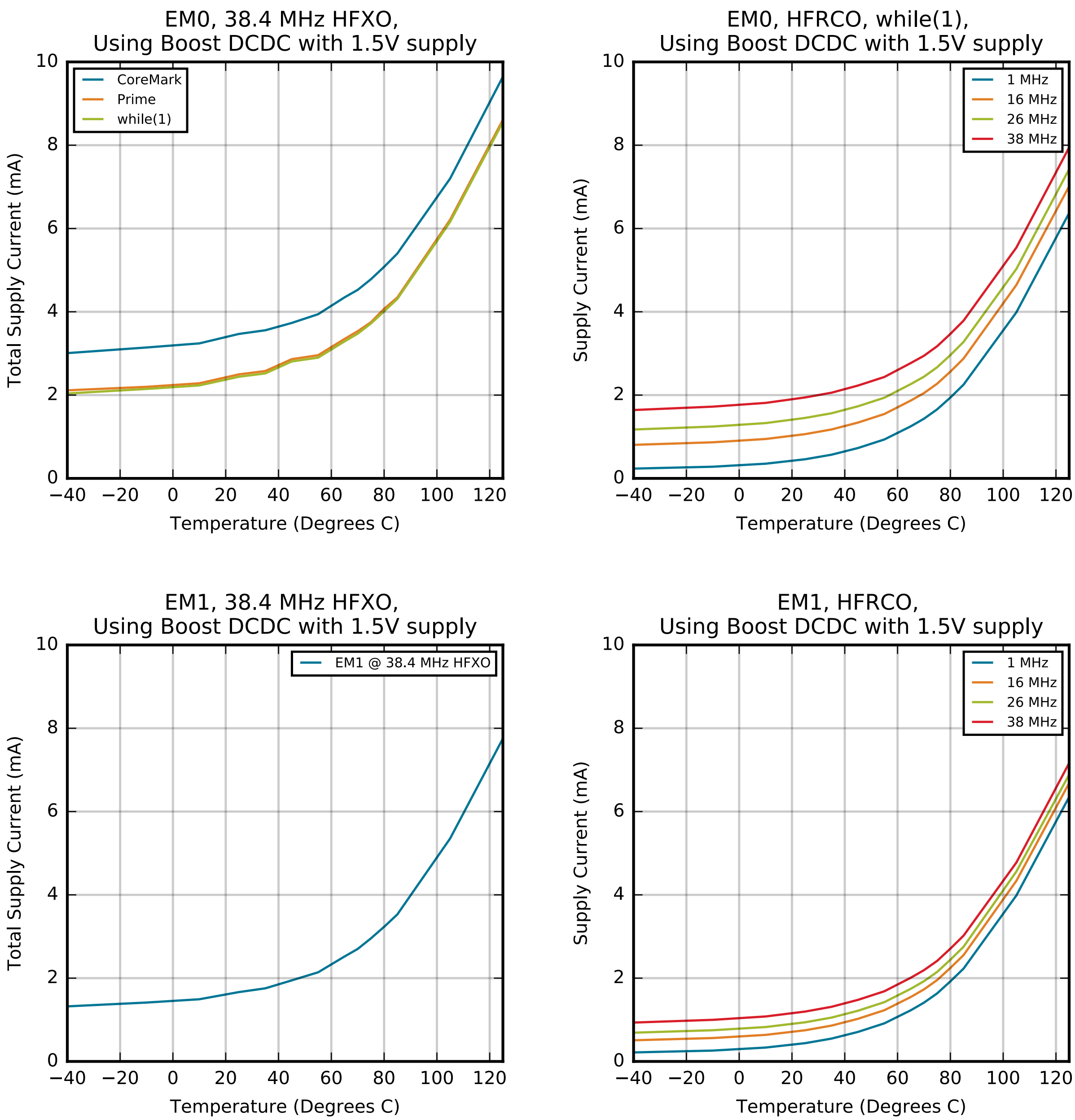


Figure 4.10. EM0 and EM1 Typical Supply Current vs. Temperature (Boost DCDC)

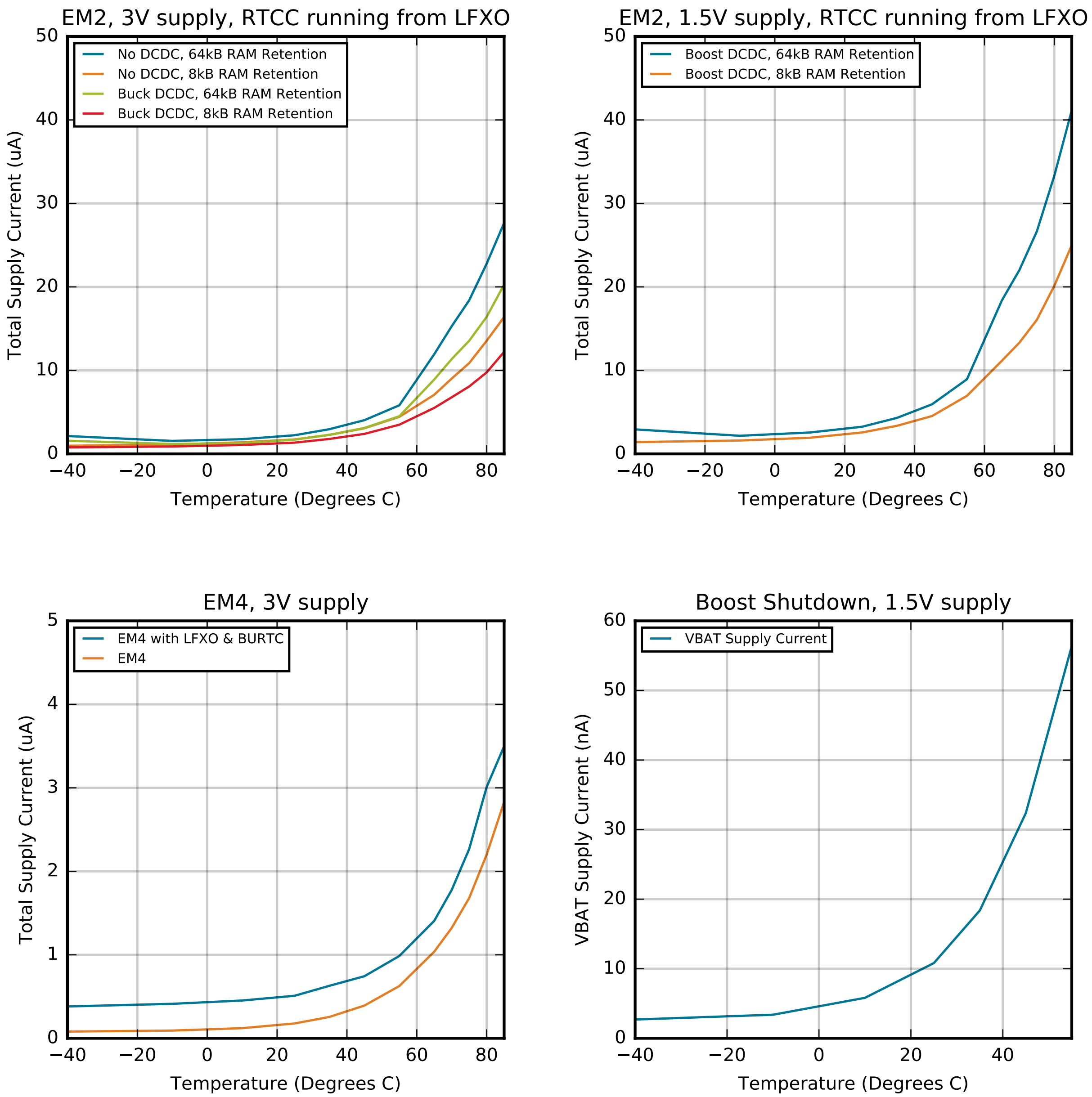


Figure 4.11. EM2, EM4, and Boost Shutdown Typical Supply Current vs. Temperature

4.28.2 RF Characteristics

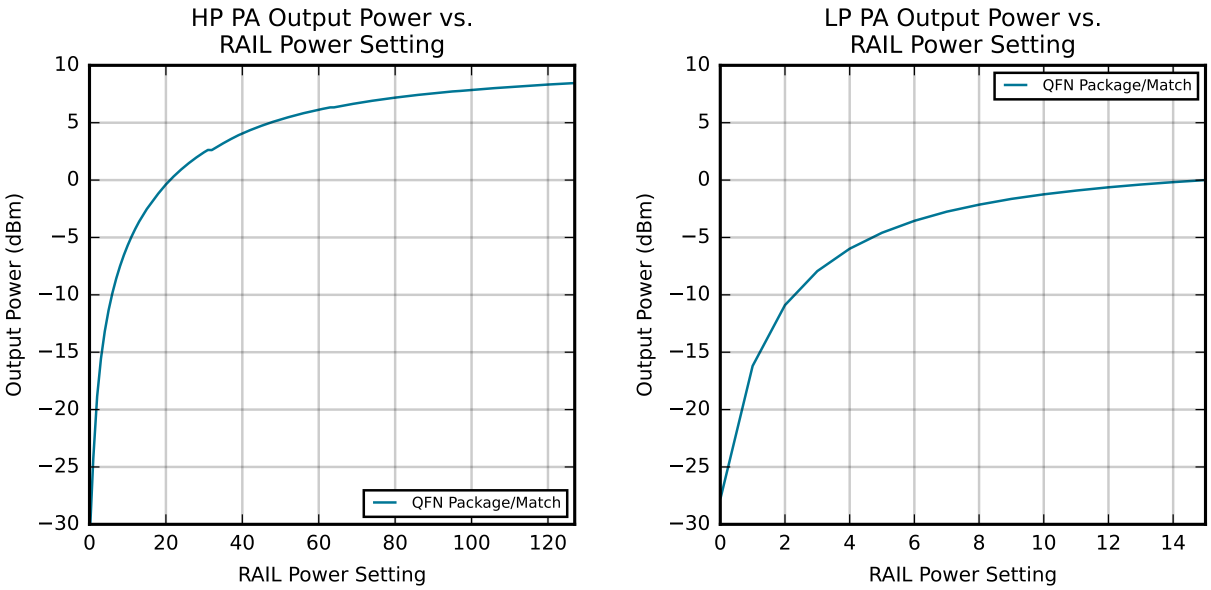


Figure 4.12. Transmitter Output Power, QFN Package / Matching

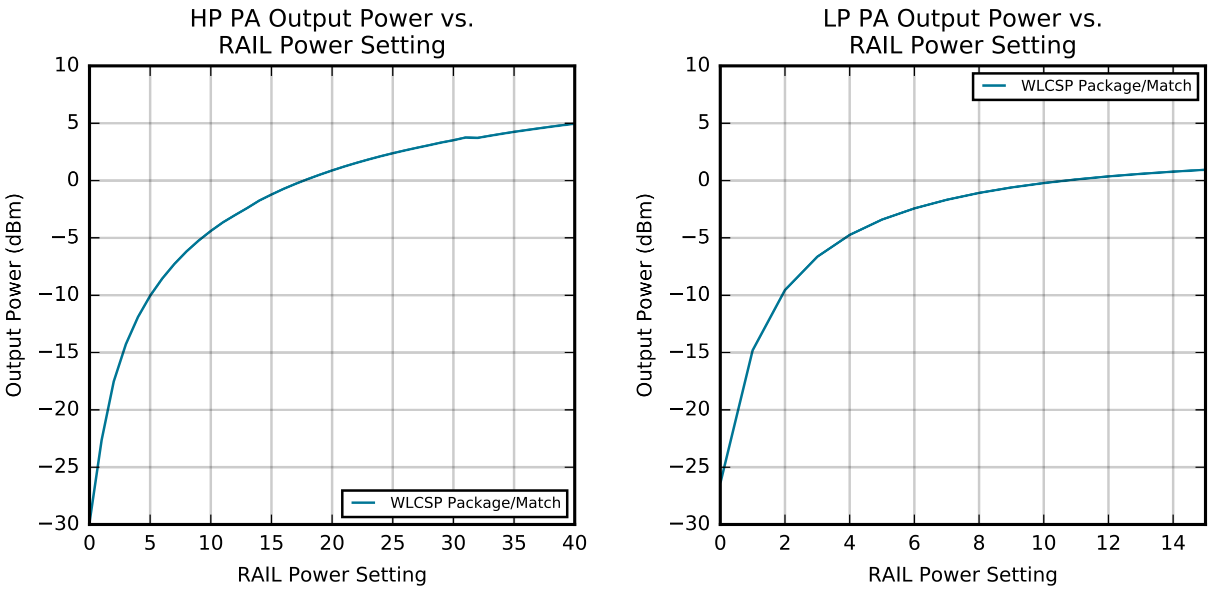


Figure 4.13. Transmitter Output Power, WLCSP Package / Matching

4.28.3 DC-DC Converter

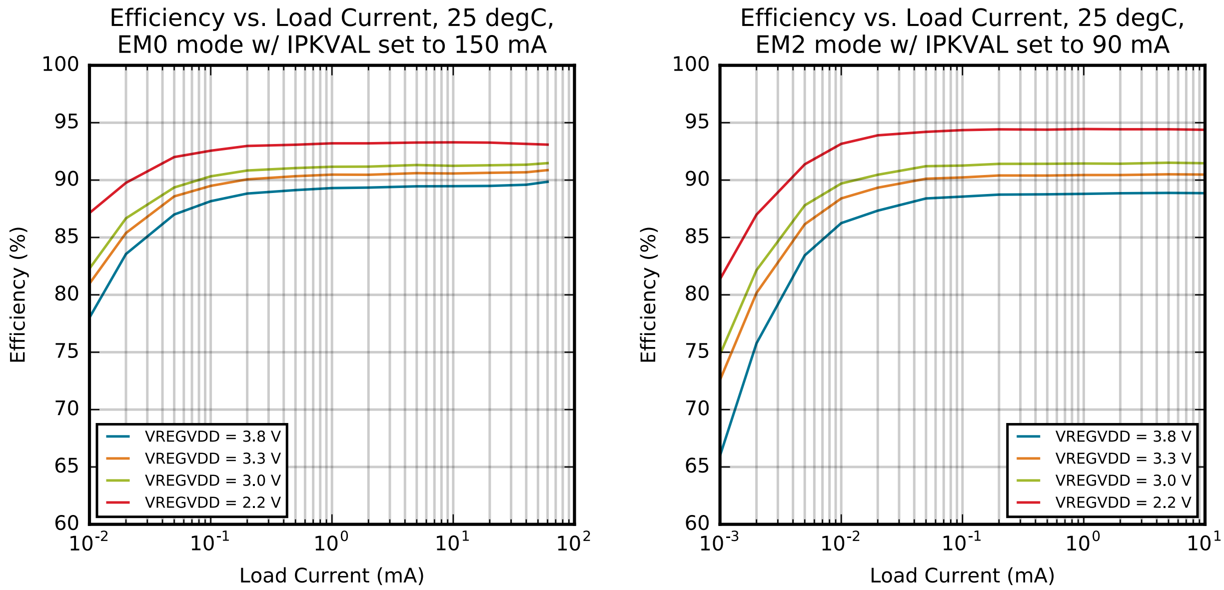


Figure 4.14. Buck DC-DC Efficiency

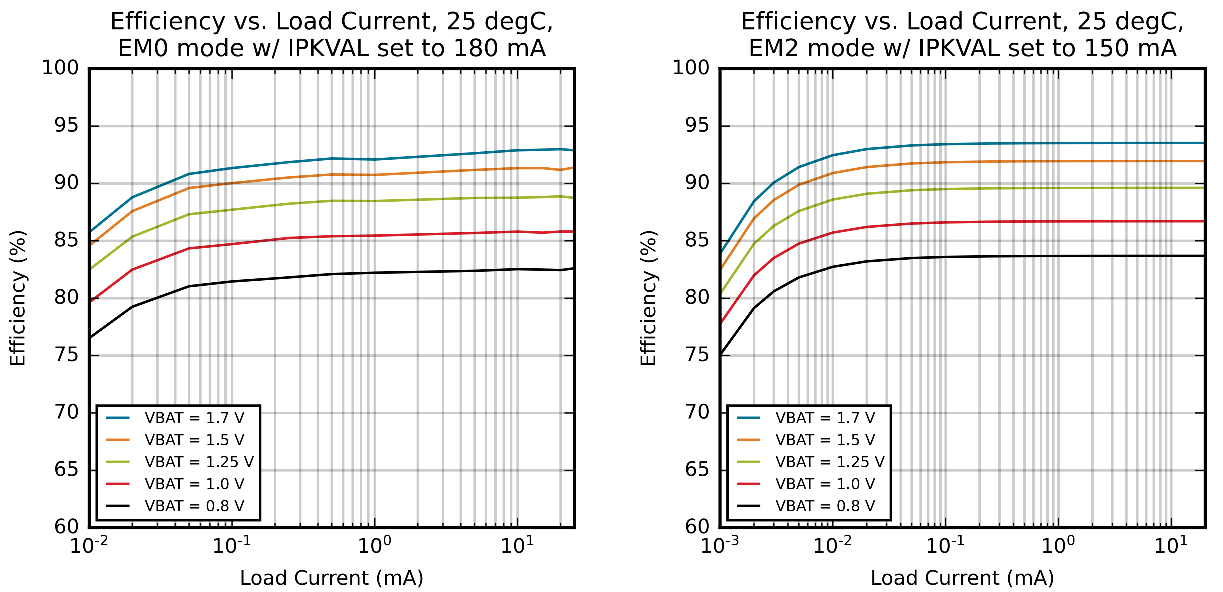
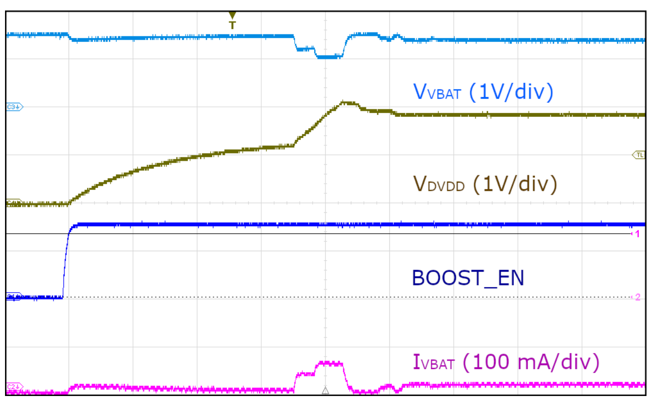


Figure 4.15. Boost DC-DC Efficiency



- Time scale = 1 ms / division
- V_{VBAT} = Input voltage at pin, 1.5 V source with 10 Ohm impedance
- V_{DVDD} = Output voltage at pin, target 1.8 V
- BOOST_EN = Boost enable input pin
- I_{VBAT} = Current seen at VBAT input pin

Figure 4.16. Boost DC-DC Startup Timing

4.28.4 IADC

Typical performance is shown using 10 MHz ADC clock for fastest sampling speed and adjusting oversampling ratio (OSR).

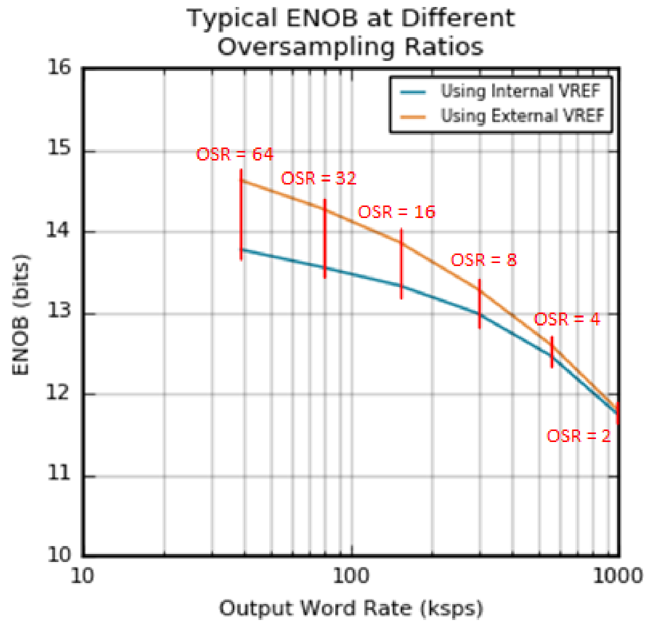


Figure 4.17. Typical ENOB vs. Oversampling Ratio

5. Typical Connections

5.1 Power

Typical power supply connections are shown in the following figures.

Note: PAVDD, RFVDD, AVDD, and IOVDD supply connections are flexible. They may be connected in other configurations or to external supplies as long as the supply limits described in 4.1 Electrical Characteristics are met.

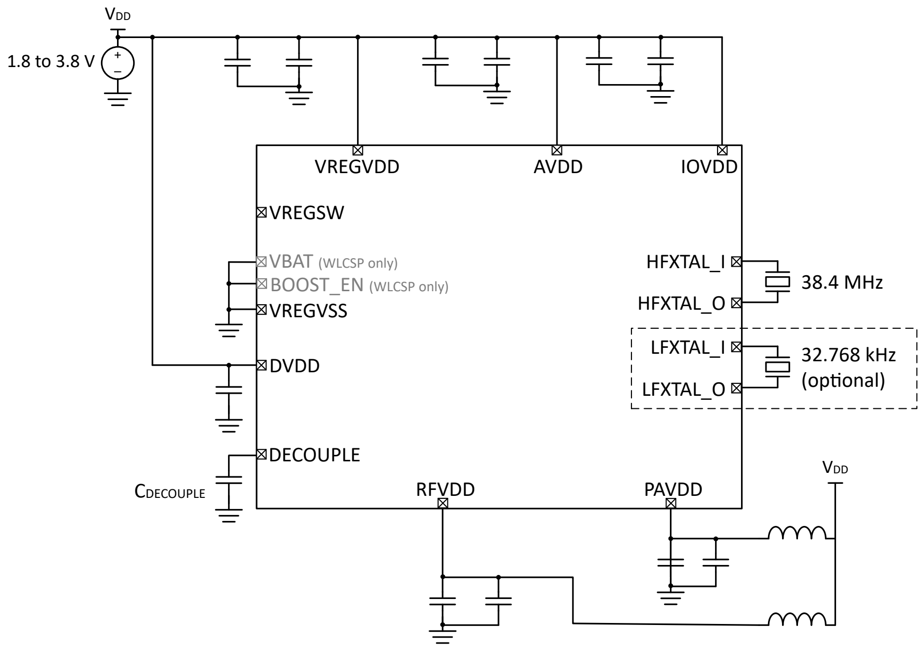


Figure 5.1. Typical Application Circuit: Direct Supply Configuration without DCDC (EFR32xG27C1x or EFR32xG27C3x)

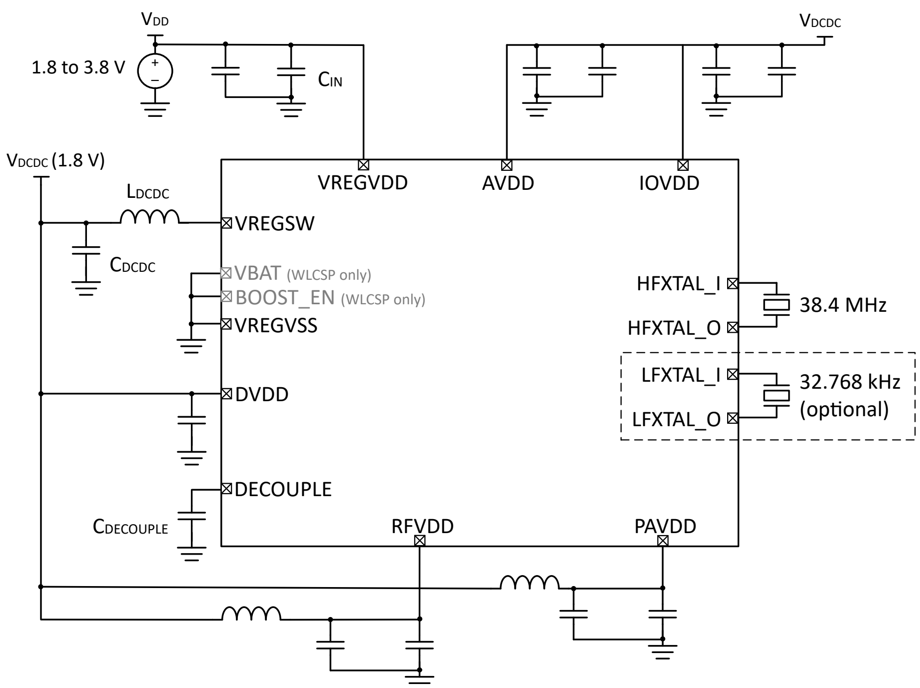


Figure 5.2. Typical Application Circuit: Buck DCDC Configuration with PAVDD, RFVDD, AVDD, and IOVDD from DCDC output (EFR32xG27C1x or EFR32xG27C3x)

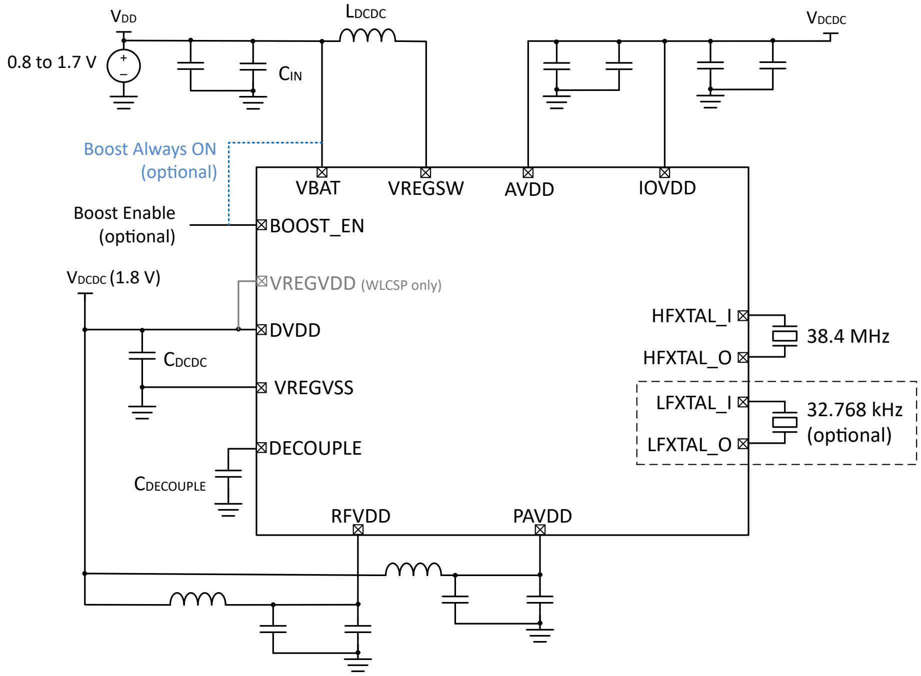


Figure 5.3. Typical Application Circuit: Boost DCDC Configuration with PAVDD, RFVDD, AVDD, and IOVDD from DCDC output (EFR32xG27C2x or EFR32xG27C3x)

5.2 RF Matching Networks

5.2.1 2.4 GHz Matching Network

The RF matching network circuit diagram used for RF characterization is shown in Figure 5.4. Typical RF impedance-matching network circuit. Typical component values are shown in Table 5.1. Component Values for QFN40 and QFN32 packages and Table 5.2. Component Values for WLCSP39 package. Please refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

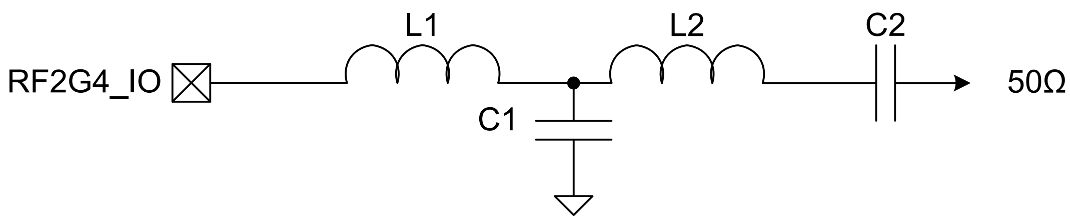


Figure 5.4. Typical RF impedance-matching network circuit

Table 5.1. Component Values for QFN40 and QFN32 packages

Designator	Value
L1	2.0 nH
C1	1.6 pF
L2	3.2 nH
C2	18 pF

Table 5.2. Component Values for WLCSP39 package

Designator	Value
L1	3.5 nH
C1	1.3 pF
L2	3.8 nH
C2	18 pF

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002.2: "EFR32 Wireless Gecko Series 2 Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 QFN40 with Buck DC-DC Device Pinout

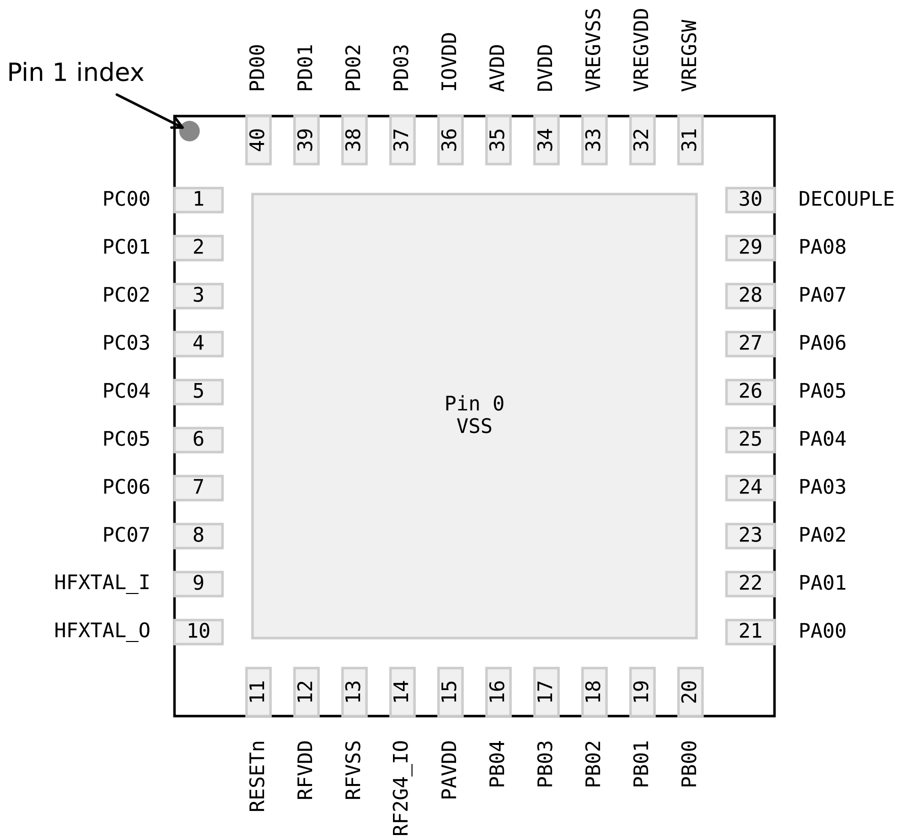


Figure 6.1. QFN40 with Buck DC-DC Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.6 Alternate Function Table, 6.7 Analog Peripheral Connectivity, and 6.8 Digital Peripheral Connectivity.

Table 6.1. QFN40 with Buck DC-DC Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
PC06	7	GPIO	PC07	8	GPIO
HFXTAL_I	9	High Frequency Crystal Input	HFXTAL_O	10	High Frequency Crystal Output
RESETn	11	Reset Pin. The RESETn pin is internally pulled up to DVDD.	RFVDD	12	Radio power supply

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RFVSS	13	Radio Ground	RF2G4_IO	14	2.4 GHz Single-ended RF input/output
PAVDD	15	Power Amplifier (PA) power supply	PB04	16	GPIO
PB03	17	GPIO	PB02	18	GPIO
PB01	19	GPIO	PB00	20	GPIO
PA00	21	GPIO	PA01	22	GPIO
PA02	23	GPIO	PA03	24	GPIO
PA04	25	GPIO	PA05	26	GPIO
PA06	27	GPIO	PA07	28	GPIO
PA08	29	GPIO	DECOUPLE	30	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
VREGSW	31	DCDC regulator switching node	VREGVDD	32	DCDC Buck regulator input supply
VREGVSS	33	DCDC ground	DVDD	34	Digital power supply
AVDD	35	Analog power supply	IOVDD	36	I/O power supply
PD03	37	GPIO	PD02	38	GPIO
PD01	39	GPIO	PD00	40	GPIO

6.2 QFN40 with Boost DC-DC Device Pinout

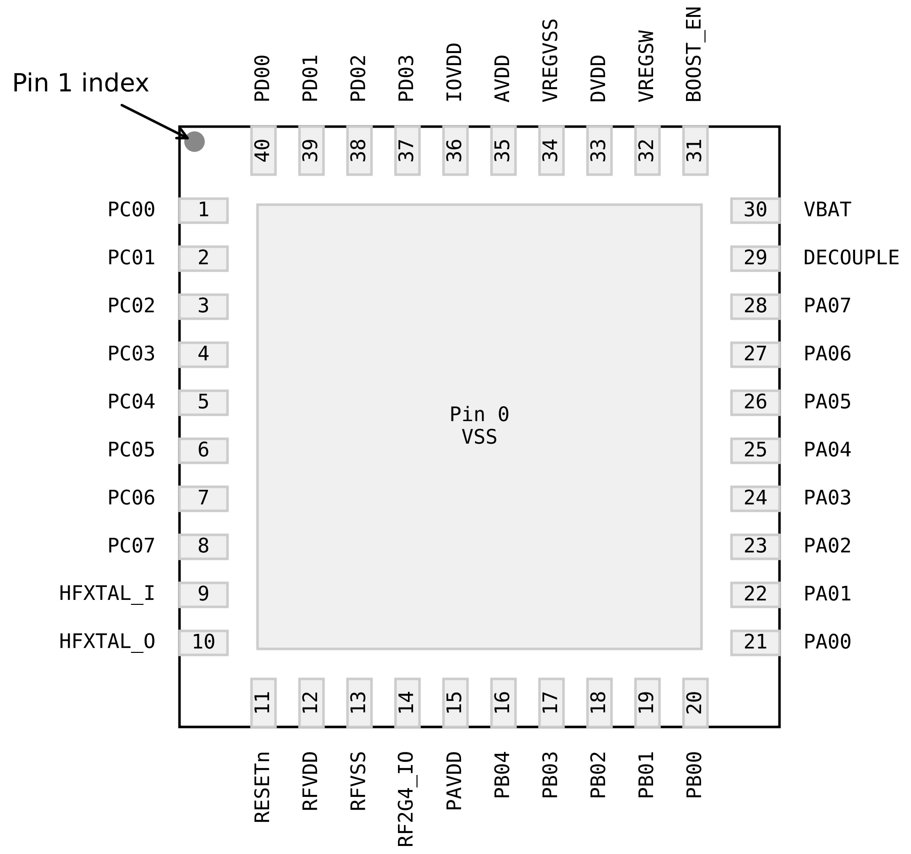


Figure 6.2. QFN40 with Boost DC-DC Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.6 Alternate Function Table, 6.7 Analog Peripheral Connectivity, and 6.8 Digital Peripheral Connectivity.

Table 6.2. QFN40 with Boost DC-DC Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
PC06	7	GPIO	PC07	8	GPIO
HFXTAL_I	9	High Frequency Crystal Input	HFXTAL_O	10	High Frequency Crystal Output
RESETn	11	Reset Pin. The RESETn pin is internally pulled up to DVDD.	RFVDD	12	Radio power supply
RFVSS	13	Radio Ground	RF2G4_IO	14	2.4 GHz Single-ended RF input/output
PAVDD	15	Power Amplifier (PA) power supply	PB04	16	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB03	17	GPIO	PB02	18	GPIO
PB01	19	GPIO	PB00	20	GPIO
PA00	21	GPIO	PA01	22	GPIO
PA02	23	GPIO	PA03	24	GPIO
PA04	25	GPIO	PA05	26	GPIO
PA06	27	GPIO	PA07	28	GPIO
DECOUPLE	29	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	VBAT	30	DCDC Boost regulator input supply
BOOST_EN	31	Boost DCDC enable	VREGSW	32	DCDC regulator switching node
DVDD	33	Digital power supply	VREGVSS	34	DCDC ground
AVDD	35	Analog power supply	IOVDD	36	I/O power supply
PD03	37	GPIO	PD02	38	GPIO
PD01	39	GPIO	PD00	40	GPIO

6.3 WLCSP39 Device Pinout

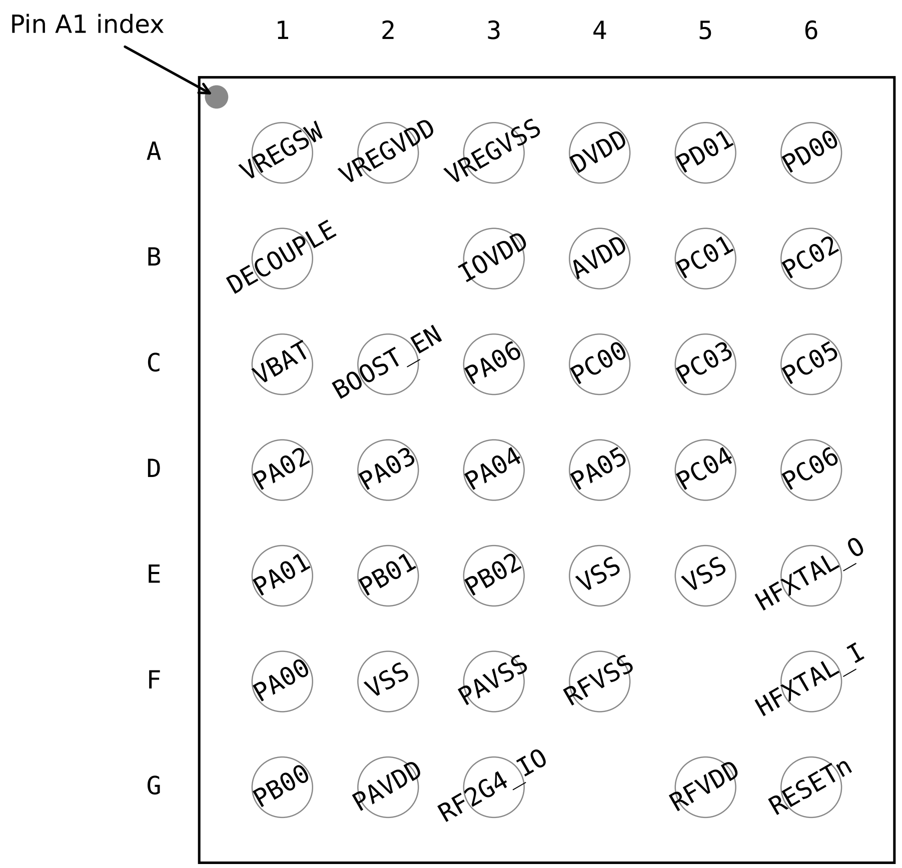


Figure 6.3. WLCSP39 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.6 Alternate Function Table, 6.7 Analog Peripheral Connectivity, and 6.8 Digital Peripheral Connectivity.

Table 6.3. WLCSP39 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGSW	A1	DCDC regulator switching node	VREGVDD	A2	DCDC Buck regulator input supply. Must be shorted to DVDD in boost configuration.
VREGVSS	A3	DCDC ground	DVDD	A4	Digital power supply
PD01	A5	GPIO	PD00	A6	GPIO
DECOUPLE	B1	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	IOVDD	B3	I/O power supply
AVDD	B4	Analog power supply	PC01	B5	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC02	B6	GPIO	VBAT	C1	DCDC Boost regulator input supply. Must be shorted to VSS in buck configuration.
BOOST_EN	C2	Boost DCDC enable. Must be shorted to VSS in buck configuration.	PA06	C3	GPIO
PC00	C4	GPIO	PC03	C5	GPIO
PC05	C6	GPIO	PA02	D1	GPIO
PA03	D2	GPIO	PA04	D3	GPIO
PA05	D4	GPIO	PC04	D5	GPIO
PC06	D6	GPIO	PA01	E1	GPIO
PB01	E2	GPIO	PB02	E3	GPIO
VSS	E4	Ground	VSS	E5	Ground
HFXTAL_O	E6	High Frequency Crystal Output	PA00	F1	GPIO
VSS	F2	Ground	PAVSS	F3	Power Amplifier (PA) ground
RFVSS	F4	Radio Ground	HFXTAL_I	F6	High Frequency Crystal Input
PB00	G1	GPIO	PAVDD	G2	Power Amplifier (PA) power supply
RF2G4_IO	G3	2.4 GHz Single-ended RF input/output	RFVDD	G5	Radio power supply
RESETn	G6	Reset Pin. The RESETn pin is internally pulled up to DVDD.			

6.4 QFN32 with Buck DC-DC Device Pinout

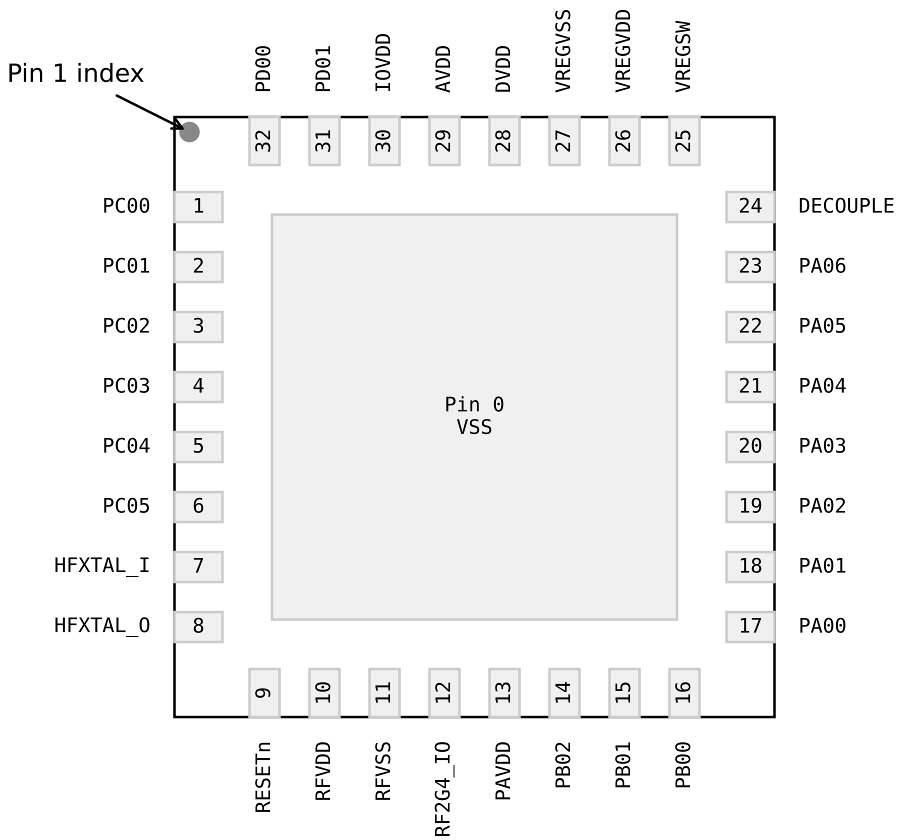


Figure 6.4. QFN32 with Buck DC-DC Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.6 Alternate Function Table, 6.7 Analog Peripheral Connectivity, and 6.8 Digital Peripheral Connectivity.

Table 6.4. QFN32 with Buck DC-DC Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
HFXTAL_I	7	High Frequency Crystal Input	HFXTAL_O	8	High Frequency Crystal Output
RESETn	9	Reset Pin. The RESETn pin is internally pulled up to DVDD.	RFVDD	10	Radio power supply
RFVSS	11	Radio Ground	RF2G4_IO	12	2.4 GHz Single-ended RF input/output
PAVDD	13	Power Amplifier (PA) power supply	PB02	14	GPIO
PB01	15	GPIO	PB00	16	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA00	17	GPIO	PA01	18	GPIO
PA02	19	GPIO	PA03	20	GPIO
PA04	21	GPIO	PA05	22	GPIO
PA06	23	GPIO	DECOUPLE	24	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
VREGSW	25	DCDC regulator switching node	VREGVDD	26	DCDC Buck regulator input supply
VREGVSS	27	DCDC ground	DVDD	28	Digital power supply
AVDD	29	Analog power supply	IOVDD	30	I/O power supply
PD01	31	GPIO	PD00	32	GPIO

6.5 QFN32 with Boost DC-DC Device Pinout

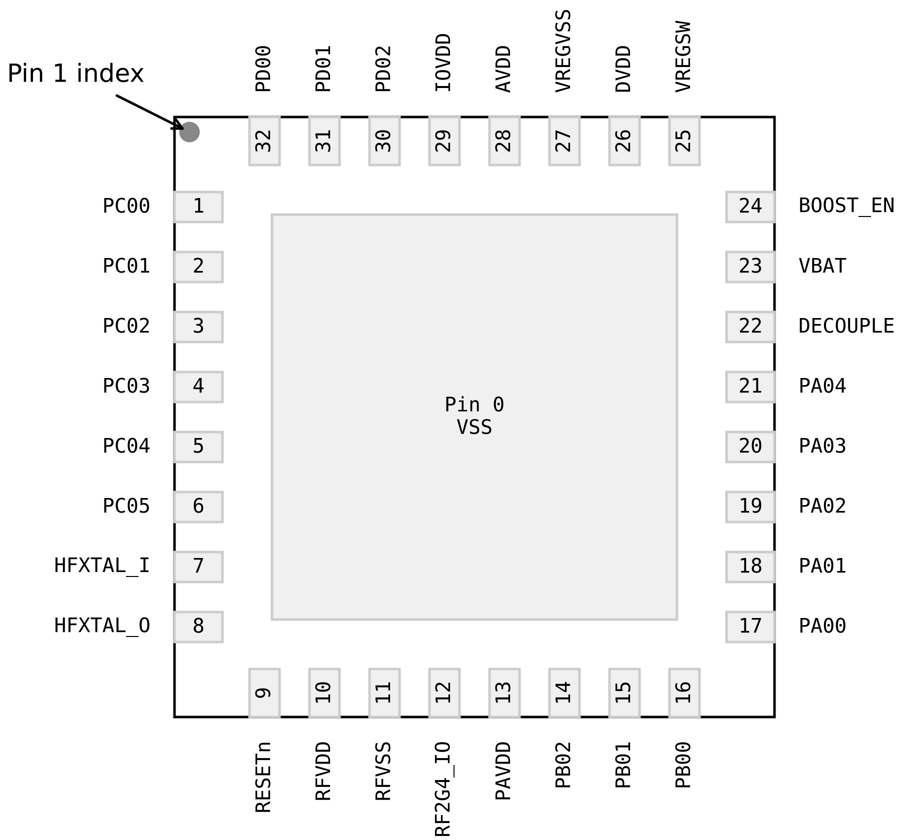


Figure 6.5. QFN32 with Boost DC-DC Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.6 Alternate Function Table, 6.7 Analog Peripheral Connectivity, and 6.8 Digital Peripheral Connectivity.

Table 6.5. QFN32 with Boost DC-DC Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
HFXTAL_I	7	High Frequency Crystal Input	HFXTAL_O	8	High Frequency Crystal Output
RESETn	9	Reset Pin. The RESETn pin is internally pulled up to DVDD.	RFVDD	10	Radio power supply
RFVSS	11	Radio Ground	RF2G4_IO	12	2.4 GHz Single-ended RF input/output
PAVDD	13	Power Amplifier (PA) power supply	PB02	14	GPIO
PB01	15	GPIO	PB00	16	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA00	17	GPIO	PA01	18	GPIO
PA02	19	GPIO	PA03	20	GPIO
PA04	21	GPIO	DECOUPLE	22	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
VBAT	23	DCDC Boost regulator input supply	BOOST_EN	24	Boost DCDC enable
VREGSW	25	DCDC regulator switching node	DVDD	26	Digital power supply
VREGVSS	27	DCDC ground	AVDD	28	Analog power supply
IOVDD	29	I/O power supply	PD02	30	GPIO
PD01	31	GPIO	PD00	32	GPIO

6.6 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows GPIO pins with support for dedicated functions across the different package options.

Table 6.6. GPIO Alternate Function Table

GPIO	Alternate Functions	QFN40 with Buck DC-DC Package[1]	QFN40 with Boost DC-DC Package[2]	WLCSP39 Package[3]	QFN32 with Buck DC-DC Package[4]	QFN32 with Boost DC-DC Package[5]
PA00	IADC0.VREFP	Yes	Yes	Yes	Yes	Yes
PA01	GPIO.SWCLK	Yes	Yes	Yes	Yes	Yes
PA02	GPIO.SWDIO	Yes	Yes	Yes	Yes	Yes
PA03	GPIO.SWV	Yes	Yes	Yes	Yes	Yes
	GPIO.TDO	Yes	Yes	Yes	Yes	Yes
	GPIO.TRACEDATA0	Yes	Yes	Yes	Yes	Yes
PA04	GPIO.TDI	Yes	Yes	Yes	Yes	Yes
	GPIO.TRACECLK	Yes	Yes	Yes	Yes	Yes
PA05	GPIO.TRACEDATA1	Yes	Yes	Yes	Yes	
	GPIO.EM4WU0	Yes	Yes	Yes	Yes	
PA06	GPIO.TRACEDATA2	Yes	Yes	Yes	Yes	
PA07	GPIO.TRACEDATA3	Yes	Yes			
PB01	ETAMPDET.ETAMPIN0	Yes	Yes	Yes	Yes	Yes
	GPIO.EM4WU3	Yes	Yes	Yes	Yes	Yes
PB03	GPIO.EM4WU4	Yes	Yes			
PC00	ETAMPDET.ETAMPIN1	Yes	Yes	Yes	Yes	Yes
	GPIO.EM4WU6	Yes	Yes	Yes	Yes	Yes
	GPIO.THMSW_EN	Yes	Yes	Yes	Yes	Yes
	GPIO.THMSW_HALFSWITCH	Yes	Yes	Yes	Yes	Yes
PC01	ETAMPDET.ETAMPOUT0	Yes	Yes	Yes	Yes	Yes
	GPIO.EFP_TX_SDA	Yes	Yes	Yes	Yes	Yes
PC02	ETAMPDET.ETAMPOUT1	Yes	Yes	Yes	Yes	Yes
	GPIO.EFP_TX_SCL	Yes	Yes	Yes	Yes	Yes
PC05	GPIO.EFP_INT	Yes	Yes	Yes	Yes	Yes
	GPIO.EM4WU7	Yes	Yes	Yes	Yes	Yes
PC07	GPIO.EM4WU8	Yes	Yes			
PD00	LFXO.LFXTAL_O	Yes	Yes	Yes	Yes	Yes
PD01	LFXO.LFXTAL_I	Yes	Yes	Yes	Yes	Yes
	LFXO.LF_EXTCLK	Yes	Yes	Yes	Yes	Yes

GPIO	Alternate Functions	QFN40 with Buck DC-DC Package[1]	QFN40 with Boost DC-DC Package[2]	WLCSP39 Package[3]	QFN32 with Buck DC-DC Package[4]	QFN32 with Boost DC-DC Package[5]
PD02	GPIO.EM4WU9	Yes	Yes			Yes

Note:

1. QFN40 with Buck DC-DC Package includes OPN EFR32BG27C140F768IM40-B
2. QFN40 with Boost DC-DC Package includes OPN EFR32BG27C230F768IM40-B
3. WLCSP39 Package includes OPNs EFR32BG27C320F768GJ39-B and EFR32BG27C320F768IJ39-B
4. QFN32 with Buck DC-DC Package includes OPN EFR32BG27C140F768IM32-B
5. QFN32 with Boost DC-DC Package includes OPN EFR32BG27C230F768IM32-B

6.7 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used Positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins. When a single ended connection is being used positive input is available on all pins. See the device Reference Manual for more details on the ABUS and analog peripherals. Note that some functions may not be available on all device variants.

Table 6.7. ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
ACMP0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IADC0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.8 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. Note that some functions may not be available on all device variants.

Table 6.8. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
ACMP0.DIGOUT	Available	Available	Available	Available
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
EUSART0.CS	Available	Available	Available	Available
EUSART0.CTS	Available	Available	Available	Available
EUSART0.RTS	Available	Available	Available	Available
EUSART0.RX	Available	Available	Available	Available
EUSART0.SCLK	Available	Available	Available	Available
EUSART0.TX	Available	Available	Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available
I2C1.SDA			Available	Available
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		

Peripheral.Resource	PORT			
	PA	PB	PC	PD
MODEM.DOUT	Available	Available		
PDM.CLK	Available	Available	Available	Available
PDM.DAT0	Available	Available	Available	Available
PDM.DAT1	Available	Available	Available	Available
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available
USART1.CLK	Available	Available		
USART1.CS	Available	Available		
USART1.CTS	Available	Available		
USART1.RTS	Available	Available		
USART1.RX	Available	Available		
USART1.TX	Available	Available		

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions

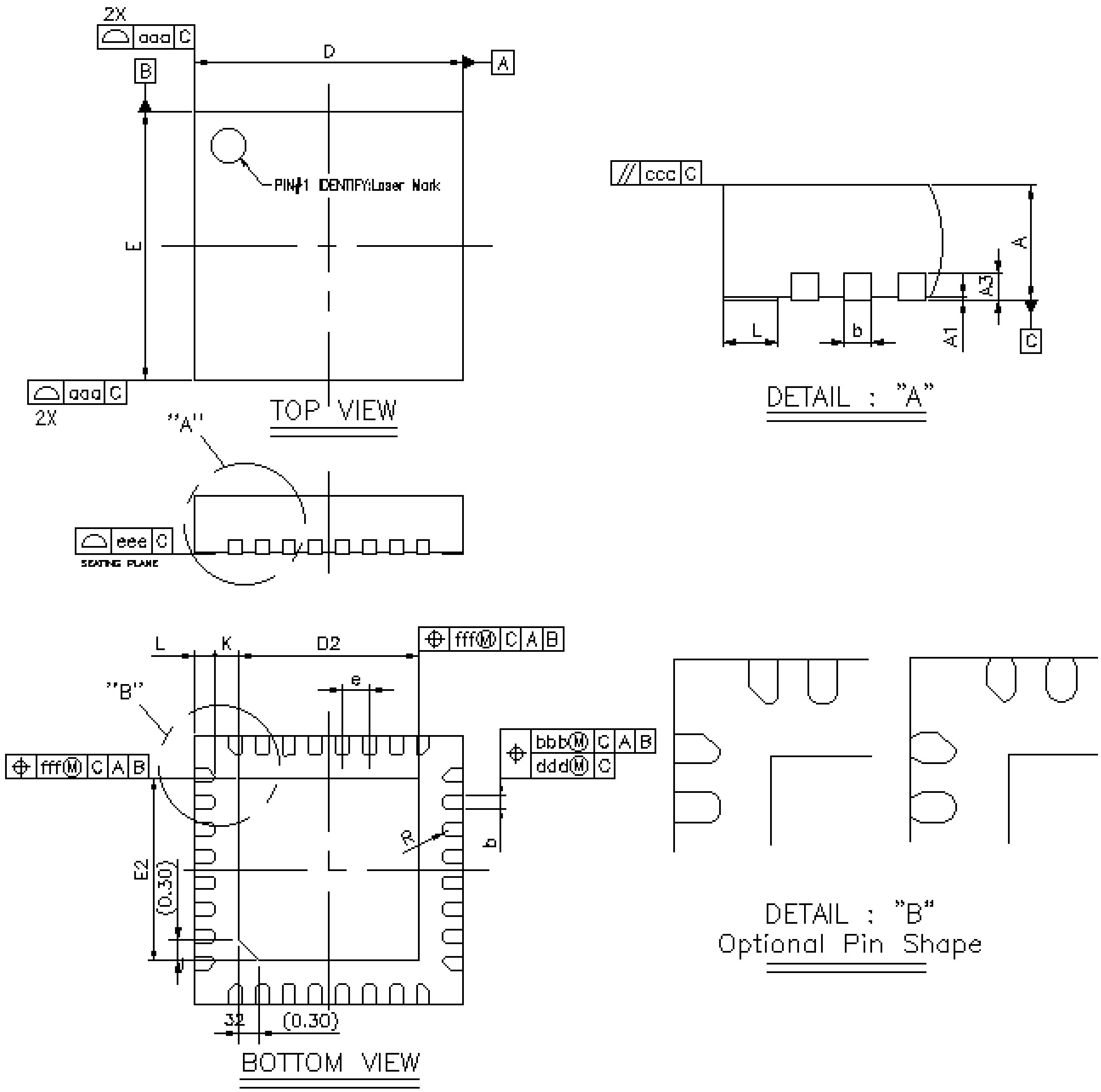


Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10

Dimension	Min	Typ	Max
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.40 BSC	
L	0.20	0.30	0.40
K	0.20	—	—
R	0.075	—	0.125
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 QFN32 PCB Land Pattern

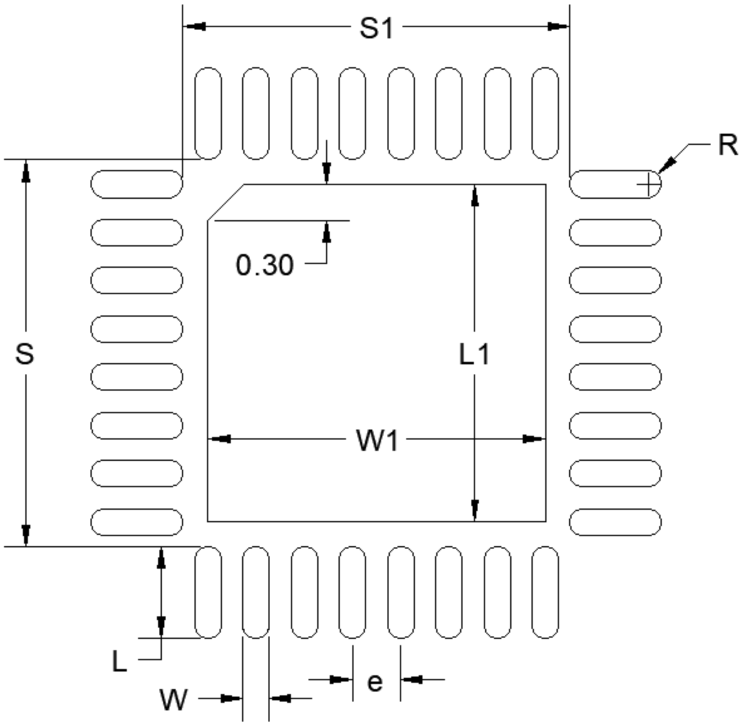


Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Typ
S	3.21
S1	3.21
e	0.40
W	0.22
L	0.76
W1	2.80
L1	2.80

Dimension	Typ
R	0.11

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.
5. All pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.101 mm (4 mils).
8. The ratio of stencil aperture to land pad size can be 1:1 for the perimeter pads.
9. A 2x2 array of 1.10 mm square openings on a 1.30 mm pitch should be used for the center ground pad.
10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.
12. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

7.3 QFN32 Package Marking

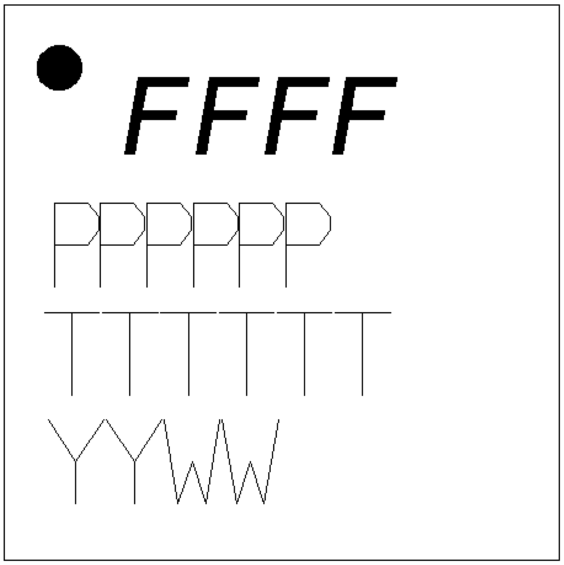


Figure 7.3. QFN32 Package Marking

The package marking consists of:

- FFFF – The product family codes (BG27 | MG27)
- PPPPPP – The product option codes:
  - 1) Security (C = Secure Vault Mid)
  - 2-4) Product Feature Codes
  - 5) Flash (S = 768k)
  - 6) Temperature grade (G = -40 to 85 °C | I = -40 to 125 °C)
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

8. QFN40 Package Specifications

8.1 QFN40 Package Dimensions

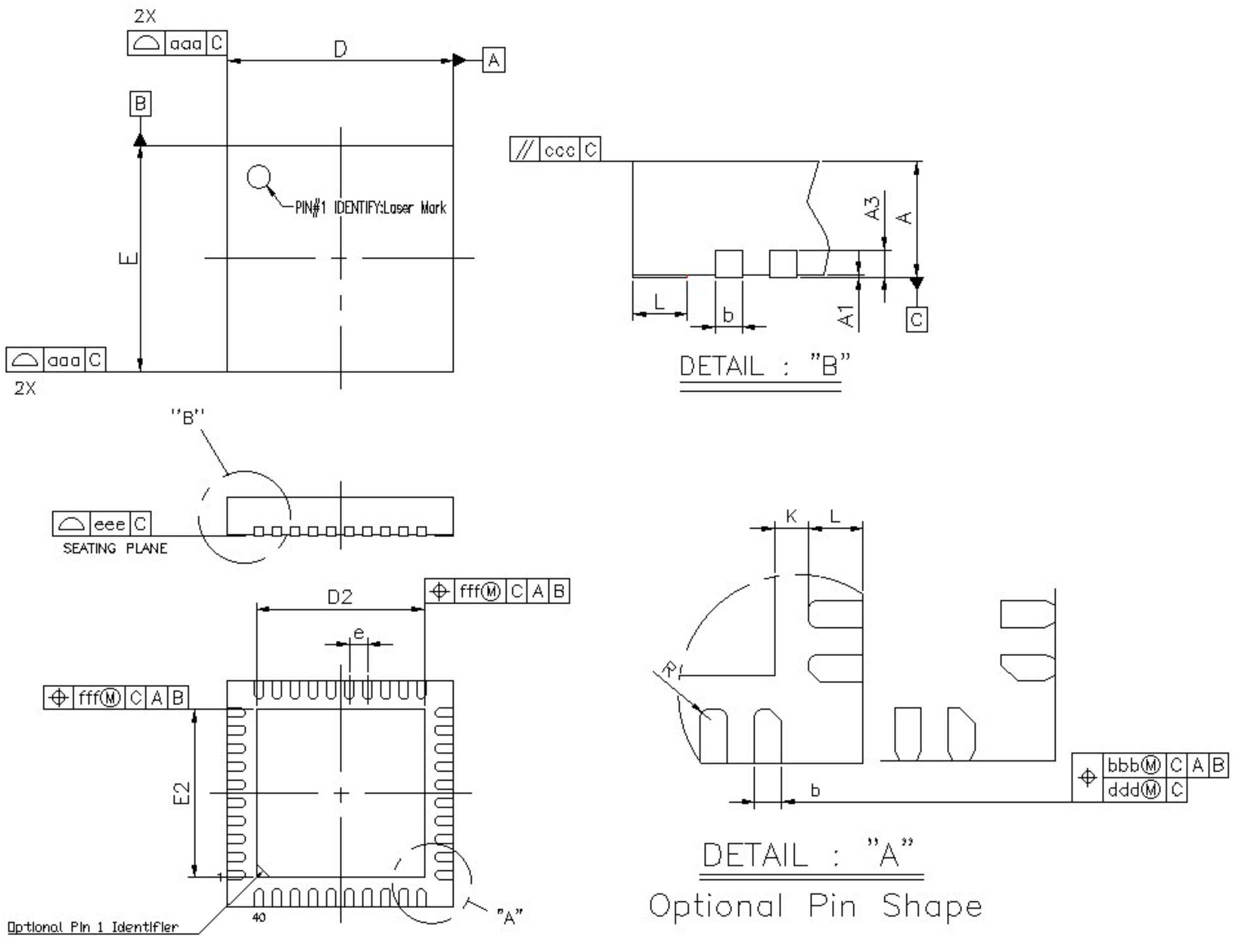


Figure 8.1. QFN40 Package Drawing

Table 8.1. QFN40 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.55	3.70	3.85
E2	3.55	3.70	3.85
e		0.40 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
R	0.075	—	—
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. Package external pad (epad) may have pin one chamfer.

8.2 QFN40 PCB Land Pattern

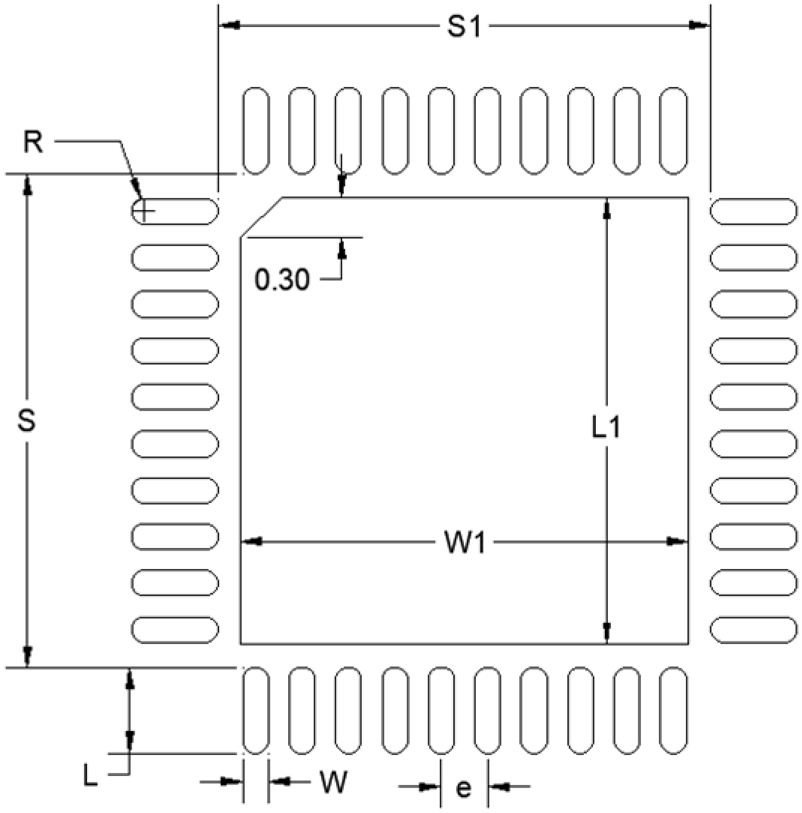


Figure 8.2. QFN40 PCB Land Pattern Drawing

Table 8.2. QFN40 PCB Land Pattern Dimensions

Dimension	Typ
S1	4.25
S	4.25
L1	3.85
W1	3.85
e	0.40
W	0.22
L	0.74
R	0.11

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
4. The stencil thickness should be 0.101 mm (4 mils).
5. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
6. A 3x3 array of 0.90 mm square openings on a 1.20 mm pitch can be used for the center ground pad.
7. A No-clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
9. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

8.3 QFN40 Package Marking

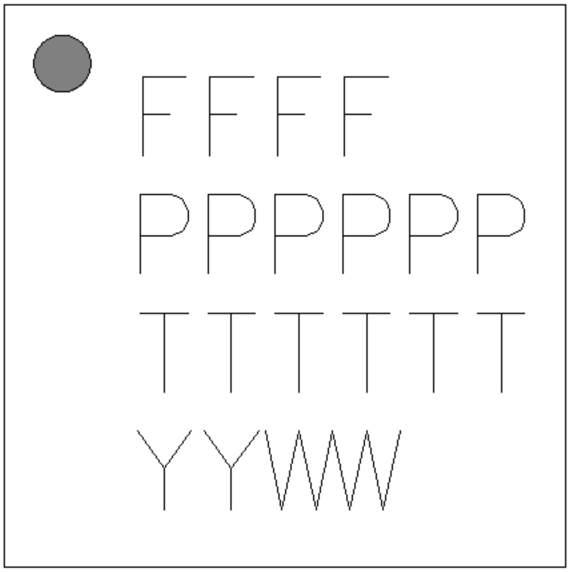


Figure 8.3. QFN40 Package Marking

The package marking consists of:

- FFFF – The product family codes (BG27 | MG27)
- PPPPPP – The product option codes:
  - 1) Security (C = Secure Vault Mid)
  - 2-4) Product Feature Codes
  - 5) Flash (S = 768k)
  - 6) Temperature grade (G = -40 to 85 °C | I = -40 to 125 °C)
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

9. WLCSP39 Package Specifications

9.1 WLCSP39 Package Dimensions

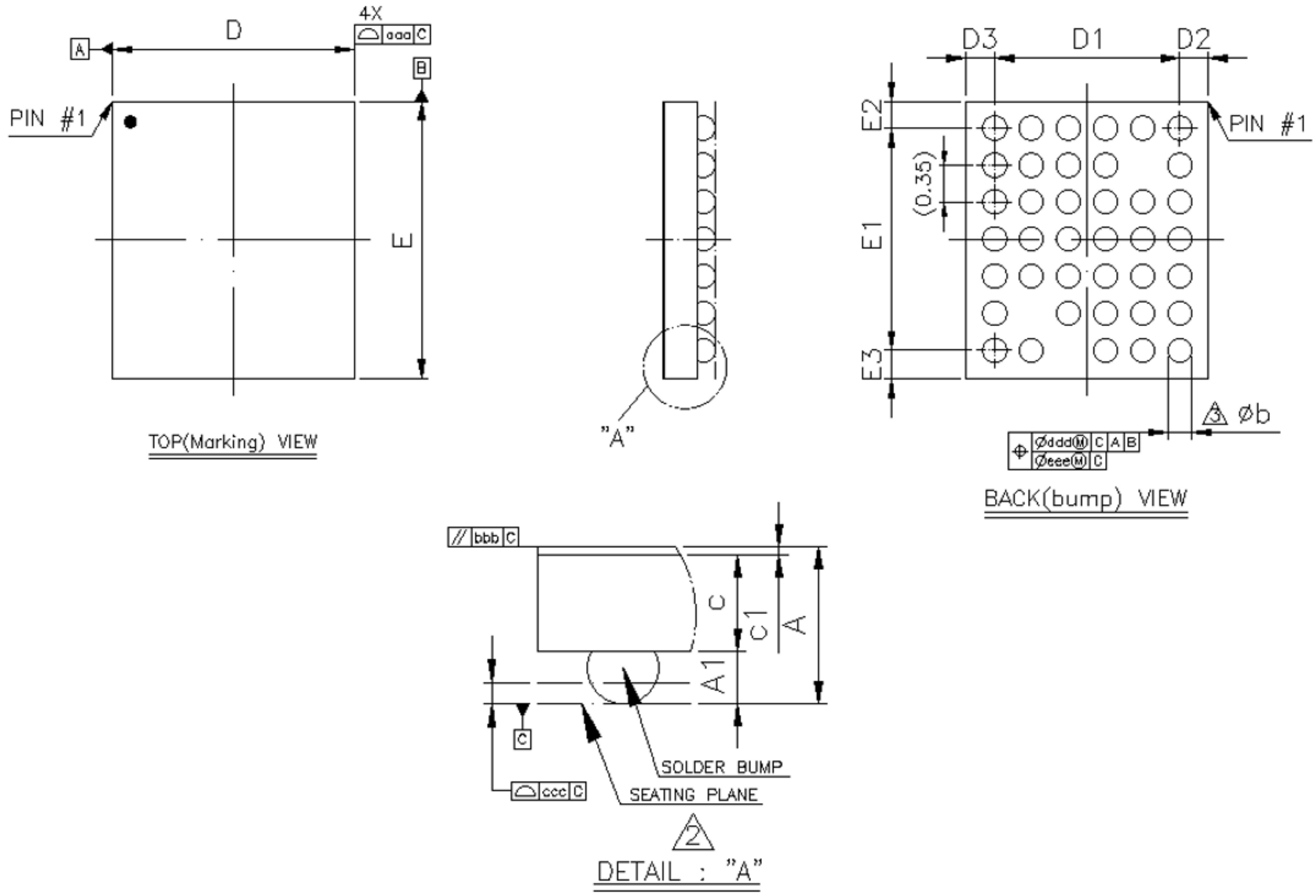


Figure 9.1. WLCSP39 Package Drawing

Table 9.1. WLCSP39 Package Dimensions

Dimension	Min	Typ	Max
A	0.466	0.495	0.524
A1	0.150	0.165	0.180
c	0.280	0.305	0.330
c1	0.022	0.025	0.028
D	2.236	2.291	2.316
E	2.569	2.624	2.649
b	0.195	0.225	0.255
D1	—	1.749	—
E1	—	2.100	—
D2	—	0.271	—
E2	—	0.254	—
D3	—	0.271	—

Dimension	Min	Typ	Max
E3	—	0.270	—
aaa		0.0300	
bbb		0.060	
ccc		0.050	
ddd		0.015	
eee		0.015	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder bumps.
3. Dimension b is measured at the maximum solder bump diameter, parallel to primary datum C.
4. Special characteristics C class: c
5. Minimum bump pitch 0.35mm
6. Dimensioning and tolerancing per ANSI Y14.5M-1994.
7. This drawing conforms to the JEDEC Solid State Outline MO-220.
8. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.2 WLCSP39 PCB Land Pattern

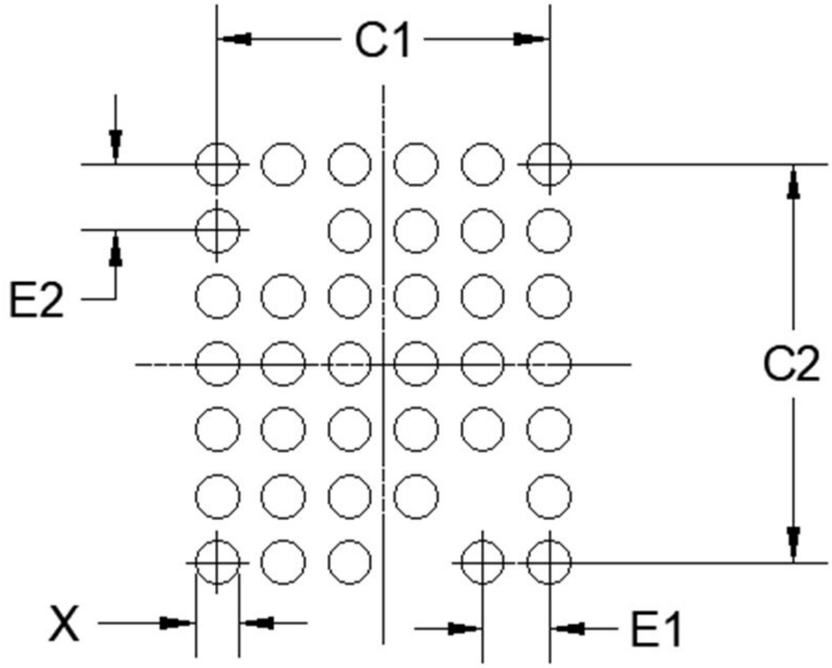


Figure 9.2. WLCSP39 PCB Land Pattern Drawing

Table 9.2. WLCSP39 PCB Land Pattern Dimensions

Dimension	NOM
X	0.20
C1	1.75
C2	2.10
E1	0.35
E2	0.35

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60um minimum, all the way around the pad.
5. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.101 mm (4 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
10. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

9.3 WLCSP39 Package Marking

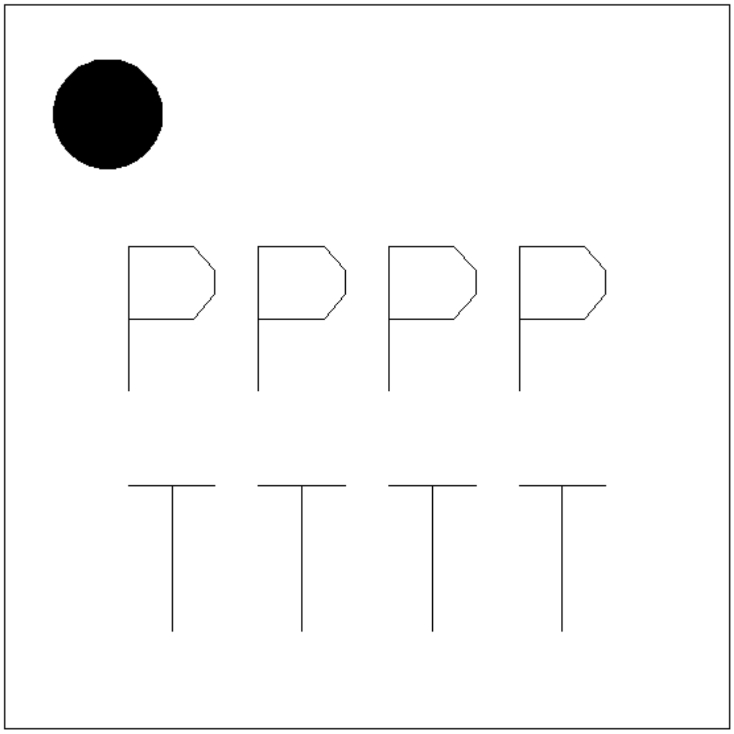


Figure 9.3. WLCSP39 Package Marking

The package marking consists of:
- PPPP – The product option codes:
  - 1) Security (C = Secure Vault Mid)
  - 2-4) Product Feature Codes
- TTTT – A trace or manufacturing code.

10. Revision History

Revision 1.3

April, 2026

- Updated VIH_Boost_En Min limit from 0.8*VBAT to 0.85*VBAT Table 4.4. Boost-Mode DC-DC Converter

Revision 1.2

July, 2024

- Added high-temperature WLCSP39 OPN: EFR32BG27C320F768IJ39-B
- Added specifications for $POUT_{VAR\_T}$ up to 125 °C in Table 4.29. WLCSP39 Package RF Transmitter General Characteristics for the 2.4 GHz Band.
- Added footnote to clarify conditions for I_{LOAD} in 4.4 Buck-Mode DC-DC Converter and 4.5 Boost-Mode DC-DC Converter.
- Separated startup load current into I_{LOAD_START} specification in 4.5 Boost-Mode DC-DC Converter.
- Updated QFN32 package thermal characteristics in 4.7 Thermal Characteristics.
- Updated QFN top mark drawings to more accurately represent text placement on package.

Revision 1.1

November, 2023

- Added capsense deprecation note to Table 4.50. Analog Comparator (ACMP).
- Corrected typical value for DVDD BOD rising threshold in Table 4.52. DVDD BOD.
- 9.3 WLCSP39 Package Marking: Fixed description of PPPP characters.

Revision 1.0

August, 2023

- Updated electrical specifications with final characterization results and test limits.
- Added RF output power plot in 4.28 Typical Performance Curves.
- Re-instated WLCSP OPN and related sections.

Revision 0.5

June, 2023

- Added additional security details to 3.7 Security Features.
- Updated characterization results with latest data and corrected test conditions.
- Moved WLCSP OPNs and related sections out of this document.
- Added section 4.4.1 Buck DC-DC Operating Limits.
- Added 4.6 Coulomb Counter Calibration Load.
- Added supply current, DCDC efficiency, and IADC plots in 4.28 Typical Performance Curves.

Revision 0.3

March, 2023

- Updated characterization results with latest data.

Revision 0.2

June, 2022

- Updated power domain descriptions in 3.9.4 Power Domains.
- Updated 5.2.1 2.4 GHz Matching Network with proposed match topology.
- Added section 9. WLCSP39 Package Specifications.
- Added RF tables separate for WLCSP package.
- Added preliminary characterization results where available.

Revision 0.1

September, 2021

Initial release.

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