THE DATASHEET OF

JS28F064M29EWH

Parallel NOR Flash Embedded Memory

JR28F032M29EWXX; PZ28F032M29EWXX; JS28F064M29EWXX
PC28F064M29EWXX; JR28F064M29EWXX; PZ28F064M29EWXX
JS28F128M29EWXX; PC28F128M29EWXX; RC28F128M29EWXX

Features

- Supply voltage
  - V_{CC} = 2.7–3.6V (program, erase, read)
  - V_{CCQ} = 1.65–3.6V (I/O buffers)
- Asynchronous random or page read
  - Page size: 8 words or 16 bytes
  - Page access: 25ns
  - Random access (V_{CCQ} = 2.7–3.6V): 60ns (BGA); 70ns (TSOP)
- Buffer program: 256-word MAX program buffer
- Program time
  - 0.56µs per byte (1.8 MB/s TYP when using 256-word buffer size in buffer program without V_{PPH})
  - 0.31µs per byte (3.2 MB/s TYP when using 256-word buffer size in buffer program with V_{PPH})
- Memory organization
  - 32Mb: 64 main blocks, 64KB each, or eight 8KB boot blocks (top or bottom) and 63 main blocks, 64KB each
  - 64Mb: 128 main blocks, 64KB each, or eight 8KB boot blocks (top or bottom) and 127 main blocks, 64 KB each
  - 128Mb: 128 main blocks, 128KB each
- Program/erase controller
  - Embedded byte/word program algorithms
- Program/erase suspend and resume capability
  - READ operation on another block during a PROGRAM SUSPEND operation
  - READ or PROGRAM operation on one block during an ERASE SUSPEND operation on another block
- BLANK CHECK operation to verify an erased block
- Unlock bypass, block erase, chip erase, and write to buffer capability
  - Fast buffered/batch programming
  - Fast block and chip erase
- V_{PP}/WP# pin protection
  - V_{PPH} voltage on V_{PP} to accelerate programming performance
  - Protects highest/lowest block (H/L uniform) or top/bottom two blocks (T/B boot)
- Software protection
  - Volatile protection
  - Nonvolatile protection
  - Password protection
  - Password access
- Extended memory block
  - 128-word (256-byte) block for permanent secure identification
  - Program or lock implemented at the factory or by the customer
- Low-power consumption: Standby mode
- JESD47H-compliant
  - 100,000 minimum ERASE cycles per block
  - Data retention: 20 years (TYP)
- 65nm single-bit cell process technology
- Packages (JEDEC-standard)
  - 56-pin TSOP (128Mb, 64Mb)
  - 48-pin TSOP (64Mb, 32Mb)
  - 64-ball FBGA (128Mb, 64Mb)
  - 48-ball BGA (64Mb, 32Mb)
- Green packages available
  - RoHS-compliant
  - Halogen-free
- Operating temperature
  - Ambient: –40°C to +85°C

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Part Numbering Information

This product is available with the prelocked extended memory block. Devices are shipped from the factory with memory content bits erased to 1. For a list of available options, such as packages or high/low protection, or for further information, contact your Micron sales representative.

Table 1: Part Number Information

Part Number Category	Category Details
Package	JS = 56-pin TSOP, 14mm x 20mm, lead-free, halogen-free, RoHS-compliant
	PC = 64-ball Fortified BGA, 11mm x 13mm, lead-free, halogen-free, RoHS-compliant
	RC = 64-ball Fortified BGA, 11mm x 13mm, leaded
	JR = 48-pin TSOP, 12mm x 20mm, lead-free, halogen-free, RoHS-compliant
	PZ = 48-ball BGA, 6mm x 8mm, lead-free, halogen-free, RoHS-compliant
Product designator	28F = Parallel NOR interface
Density	128 = 128Mb
	064 = 64Mb
	032 = 32Mb
Device type	M29EW = Embedded Flash memory (3V core, page read)
Device function	H = Highest block protected by V_{PP}/WP#; uniform block
	L = Lowest block protected by V_{PP}/WP#; uniform block
	B = Bottom boot; bottom two blocks protected by V_{PP}/WP#
	T = Top boot; top two blocks protected by V_{PP}/WP#
Features	A/B/F/X or an asterisk (*) = Combination of features, including packing media, security features, and specific customer request information

Valid M29EW Part Number Combinations

Table 2: Standard Part Numbers by Density, Medium, and Package

Density	Medium	Package				
		JS	PC	RC	JR	PZ
32Mb	Tray	–	–	–	JR28F032M29EWHA	PZ28F032M29EWHA
					JR28F032M29EWLA	PZ28F032M29EWLA
					JR28F032M29EWBA	PZ28F032M29EWBA
					JR28F032M29EWTA	PZ28F032M29EWTA
	Tape and reel	–	–	–	JR28F032M29EWBB	PZ28F032M29EWBB
					JR28F032M29EWTB	

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Table 2: Standard Part Numbers by Density, Medium, and Package (Continued)

Density	Medium	Package				
		JS	PC	RC	JR	PZ
64Mb	Tray	JS28F064M29EWHA	PC28F064M29EWHA	–	JR28F064M29EWHA	PZ28F064M29EWHA
		JS28F064M29EWLA	PC28F064M29EWLA		JR28F064M29EWLA	PZ28F064M29EWLA
		JS28F064M29EWBA	PC28F064M29EWBA		JR28F064M29EWBA	PZ28F064M29EWBA
		JS28F064M29EWTA	PC28F064M29EWTA		JR28F064M29EWTA	PZ28F064M29EWTA
	Tape and reel	JS28F064M29EWLB	–	–	JR28F064M29EWHB	PZ28F064M29EWBB
					JR28F064M29EWLB	
					JR28F064M29EWTB	
128Mb	Tray	JS28F128M29EWHF	PC28F128M29EWHF	RC28F128M29EWHF	–	–
		JS28F128M29EWLA	PC28F128M29EWLA	RC28F128M29EWLA		
	Tape and reel	–	–	–	–	–

Table 3: Part Numbers with Security Features by Density, Medium, and Package

Density	Medium	Package	
		PC	PZ
64Mb	Tray	PC28F064M29EWHX	PZ28F064M29EWHX
		PC28F064M29EWLX	PZ28F064M29EWLX
		PC28F064M29EWBX	PZ28F064M29EWBX
		PC28F064M29EWTX	PZ28F064M29EWTX
	Tape and Reel	PC28F064M29EWTY	–
128Mb	Tray	PC28F128M29EWHX	–
		PC28F128M29EWLX	
	Tape and Reel	–	–

Note: 1. This data sheet covers only standard parts. For security parts, contact your local Micron sales representative.

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General Description

The M29EW is an asynchronous, parallel NOR Flash memory device manufactured on 65nm single-bit cell (SBC) technology. READ, ERASE, and PROGRAM operations are performed using a single low-voltage supply. Upon power-up, the device defaults to read array mode.

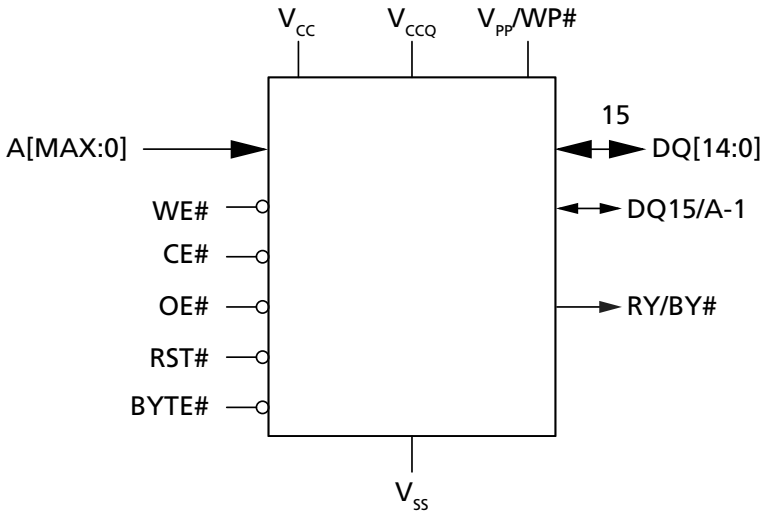
The main memory array is divided into uniform blocks that can be erased independently so that valid data can be preserved while old data is purged. PROGRAM and ERASE commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all special operations required to update the memory contents. The end of a PROGRAM or ERASE operation can be detected and any error condition can be identified. The command set required to control the device is consistent with JEDEC standards.

CE#, OE#, and WE# control the bus operation of the device and enable a simple connection to most microprocessors, often without additional logic.

The M29EW supports asynchronous random read and page read from all blocks of the array. It also features an internal program buffer that improves throughput by programming 256 words via one command sequence. The device contains a 128-word extended memory block which overlaps addresses with array block 0. The user can program this additional space and then protect it to permanently secure the contents. The device also features different levels of hardware and software protection to secure blocks from unwanted modification.

Refer to TN-13-30, System Design Considerations with Micron Flash Memory, for details on system design and V_{CC} and V_{CCQ} signals.

Figure 1: Logic Diagram



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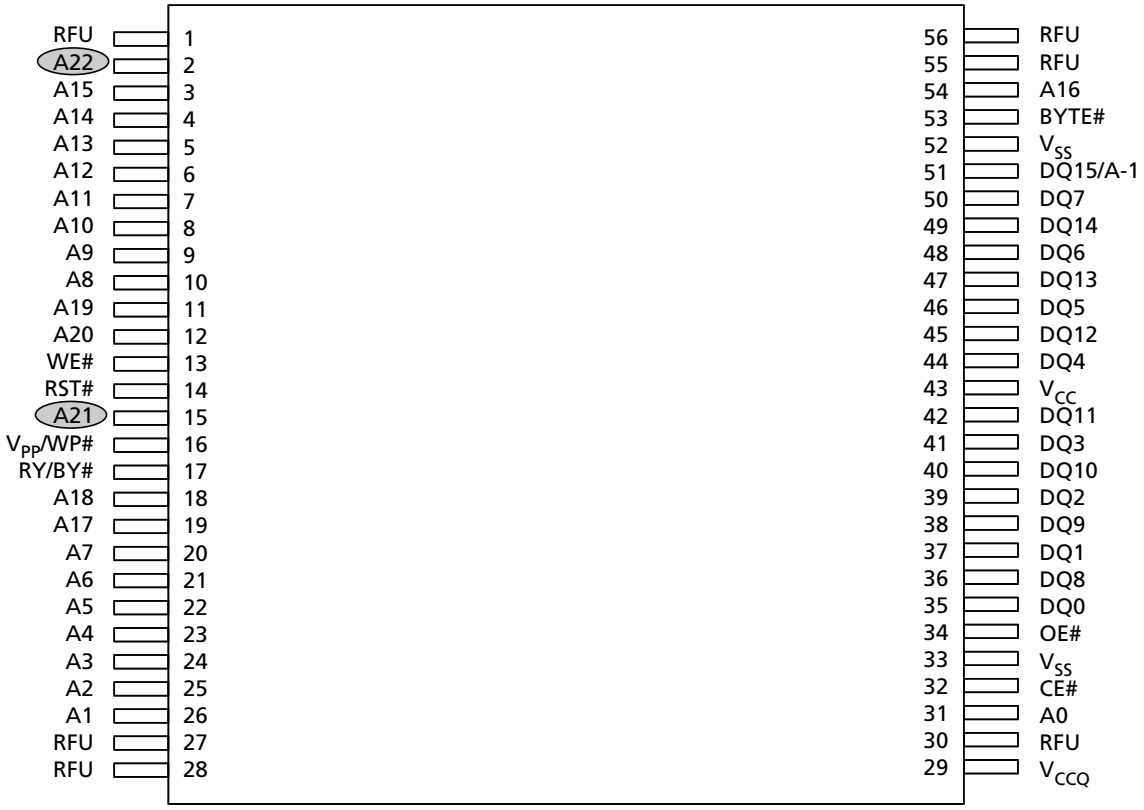
Signal Assignments

Figure 2: 56-Pin TSOP (Top View)



Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64Mb and above; otherwise, it is RFU.
3. A22 is valid for 128Mb and above; otherwise, it is RFU.
4. RFU = Reserved for future use.

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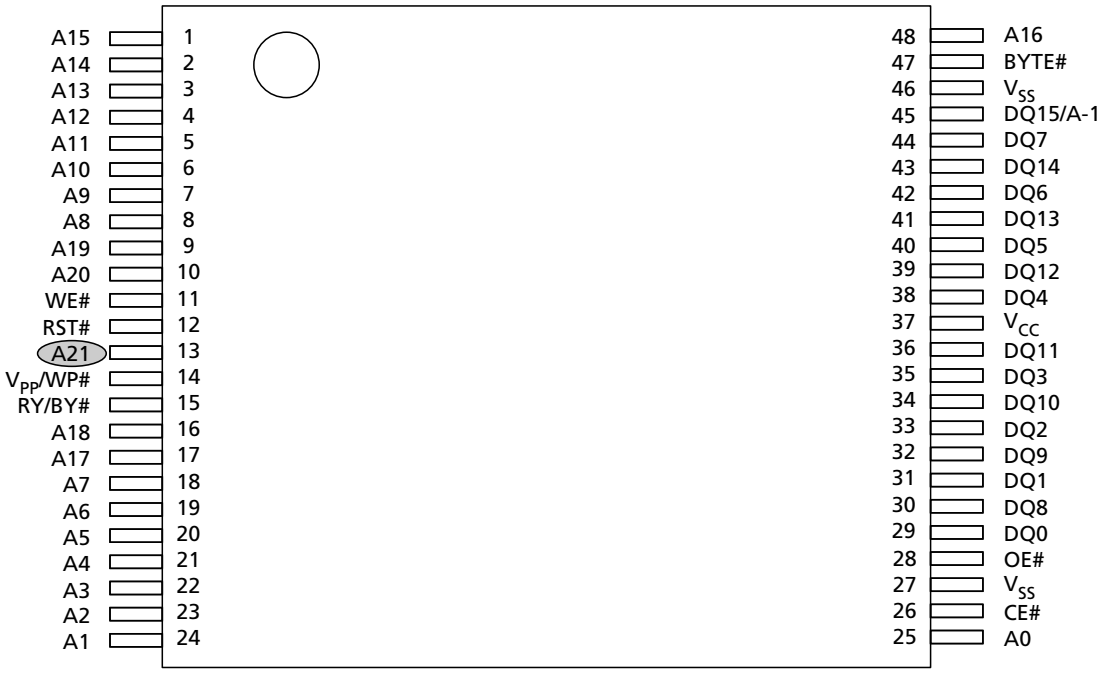
Figure 3: 48-Pin TSOP (Top View)



Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64Mb and above; otherwise, it is RFU.
3. For 48-Pin, there is no V_{CCQ} pin, V_{CC} also supply IO, it can only be 2.7V-3.6V
4. RFU = Reserved for future use.

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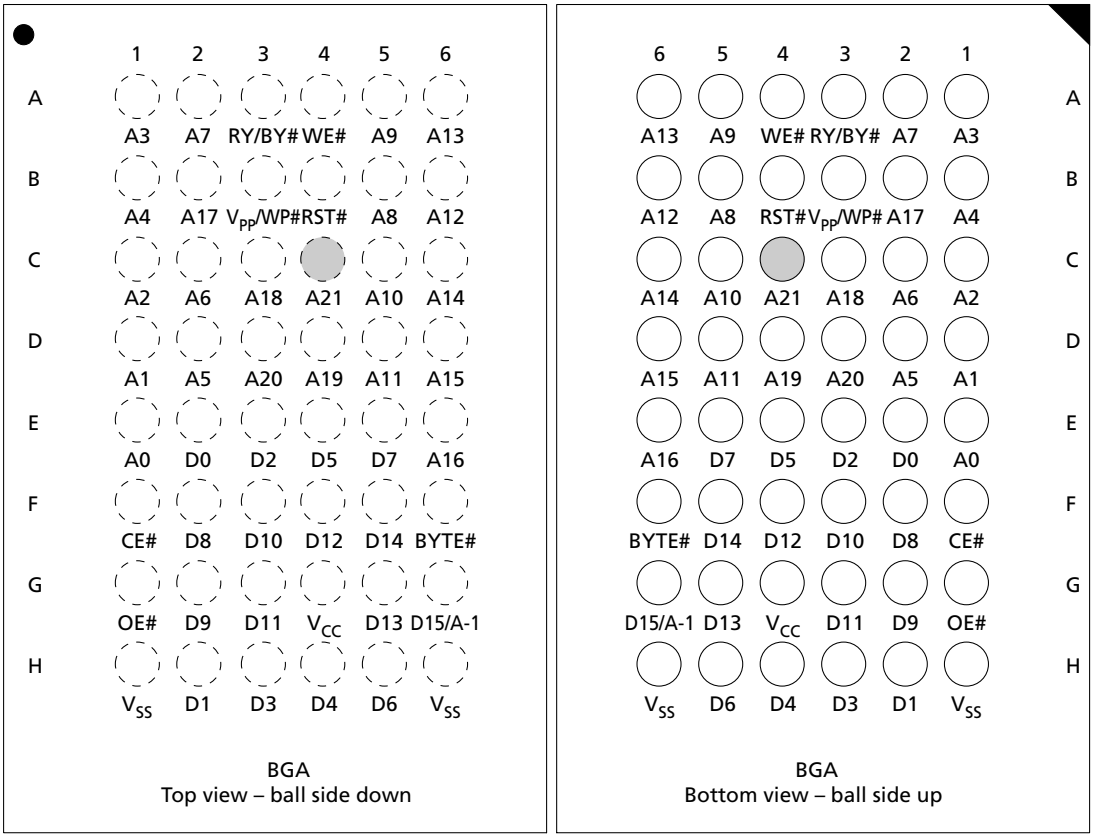
Figure 4: 48-Ball BGA (Top and Bottom Views)



Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64Mb and above; otherwise, it is RFU.
3. For 48-Pin, there is no V_{CCQ} pin, V_{CC} also supply IO, it can only be 2.7V-3.6V
4. RFU = Reserved for future use.

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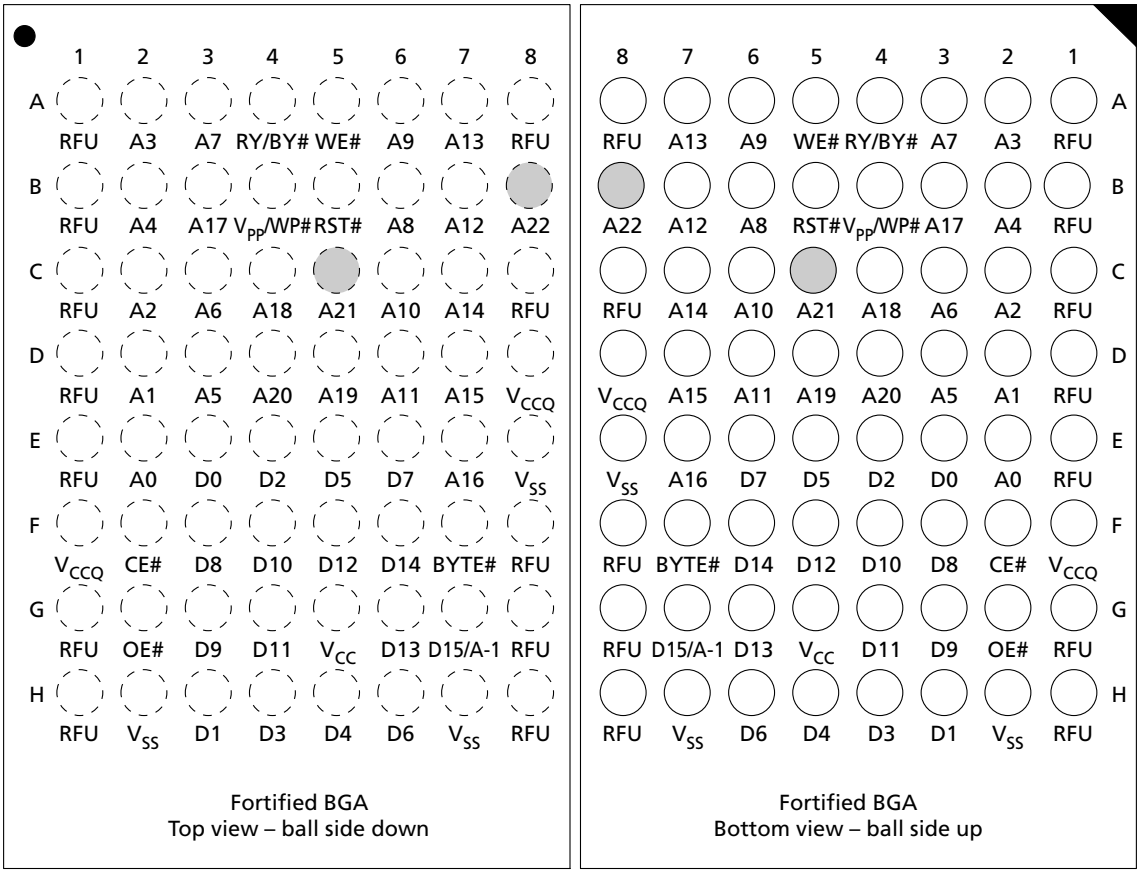
Figure 5: 64-Ball Fortified BGA (Top and Bottom Views)



Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A21 is valid for 64Mb and above; otherwise, it is RFU.
3. A22 is valid for 128Mb and above; otherwise, it is RFU.
4. RFU = Reserved for future use.

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Signal Descriptions

The signal description table below is a comprehensive list of signals for this device family. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 4: Signal Descriptions

Name	Type	Description
A[MAX:0]	Input	**Address:** Selects the cells in the array to access during READ operations. During WRITE operations, they control the commands sent to the command interface of the program/erase controller.
CE#	Input	**Chip enable:** Activates the device, enabling READ and WRITE operations to be performed. When CE# is HIGH, the device goes to standby and data outputs are at High-Z.
OE#	Input	**Output enable:** Controls the bus READ operation.
WE#	Input	**Write enable:** Controls the bus WRITE operation of the command interface.
V_{PP}/WP#	Input	**V_{PP}/Write Protect:** Provides WRITE PROTECT function and V_{PPH} function. These functions protect the lowest or highest block or top two blocks or bottom two blocks, enable the device to enter unlock bypass mode and accelerate program speed, respectively. (Refer to Hardware Protection, Bypass Operations, and Program Operations for details.) A 0.1µF capacitor should be connected between V_{PP}/WP# and V_{SS} to decouple the current surges from the power supply when V_{PPH} is applied. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operation when V_{PPH} is applied. (See DC Characteristics.)
BYTE#	Input	**Byte/word organization select:** Switches between x8 and x16 bus modes. When BYTE# is LOW, the device is in x8 mode; when HIGH, the device is in x16 mode.
RST#	Input	**Reset:** Applies a hardware reset to the device, which is achieved by holding RST# LOW for at least ^{t}PLPX. After RST# goes HIGH, the device is ready for READ and WRITE operations (after ^{t}PHEL or ^{t}RHEL, whichever occurs last). See RESET AC Specifications for more details.
DQ[7:0]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation. During WRITE operations, they represent the commands sent to the command interface of the internal state machine.
DQ[14:8]	I/O	**Data I/O:** Outputs the data stored at the selected address during a READ operation when BYTE# is HIGH. When BYTE# is LOW, these pins are not used and are High-Z. During WRITE operations, these bits are not used. When reading the status register, these bits should be ignored.
DQ15/A-1	I/O	**Data I/O or address input:** When the device operates in x16 bus mode, this pin behaves as data I/O, together with DQ[14:8]. When the device operates in x8 bus mode, this pin behaves as the least significant bit of the address. Except where stated explicitly otherwise, DQ15 = data I/O (x16 mode); A-1 = address input (x8 mode).

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Table 4: Signal Descriptions (Continued)

Name	Type	Description
RY/BY#	Output	**Ready busy:** Open-drain output that can be used to identify when the device is performing a PROGRAM or ERASE operation. During PROGRAM or ERASE operations, RY/BY# is LOW, and is High-Z during read mode, auto select mode, and erase suspend mode. After a hardware reset, READ and WRITE operations cannot begin until RY/BY# goes High-Z. (See RESET AC Specifications for more details.) The use of an open-drain output enables the RY/BY# pins from several devices to be connected to a single pull-up resistor to V_{CCQ}. A low value will then indicate that one (or more) of the devices is (are) busy. A 10K Ohm or bigger resistor is recommended as pull-up resistor to achieve 0.1V V_{OL}.
V_{CC}	Supply	**Supply voltage:** Provides the power supply for READ, PROGRAM, and ERASE operations. The command interface is disabled when V_{CC} <= V_{LKO}. This prevents WRITE operations from accidentally damaging the data during power-up, power-down, and power surges. If the program/erase controller is programming or erasing during this time, then the operation aborts and the contents being altered will be invalid. A 0.1µF capacitor should be connected between V_{CC} and V_{SS} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operations. (See DC Characteristics.)
V_{CCQ}	Supply	**I/O supply voltage:** Provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.
V_{SS}	Supply	**Ground:** All V_{SS} pins must be connected to the system ground.
RFU	–	**Reserved for future use:** RFUs should be not connected.

Memory Organization

Memory Configuration

The 32Mb device memory array (x8/x16) is divided into 63 main blocks (64KB each) and 8 top or bottom boot blocks (8KB each). It is also divided into 64 main uniform blocks (64KB each).

The 64Mb device memory array (x8/x16) is divided into 127 main blocks (64KB each) and 8 top or bottom boot blocks (8KB each). It is also divided into 128 main uniform blocks (64KB each).

The 128Mb device memory array (x8/x16) is divided into 128 main uniform blocks (128KB each).

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Memory Map – 32Mb

Table 5: 32Mb Memory Map – x8 Top and Bottom Boot [70:0]

Block	Block Size	Address Range (x8 Top Boot)		Block	Block Size	Address Range (x8 Bottom Boot)	
		Start	End			Start	End
70	8KB	003F E000	003F FFFF	70	64KB	003F 0000	003F FFFF
69		003F C000	003F DFFF	69		003E 0000	003E FFFF
68		003F A000	003F BFFF	68		003D 0000	003D FFFF
67		003F 8000	003F 9FFF	⋮	⋮	⋮	⋮
66		003F 6000	003F 7FFF	8	64KB	0001 0000	0001 FFFF
65		003F 4000	003F 5FFF	7	8KB	0000 E000	0000 FFFF
64		003F 2000	003F 3FFF	6		0000 C000	0000 DFFF
63		003F 0000	003F 1FFF	5		0000 A000	0000 BFFF
62	64KB	003E 0000	003E FFFF	4		0000 8000	0000 9FFF
⋮	⋮	⋮	⋮	3		0000 6000	0000 7FFF
2	64KB	0002 0000	0002 FFFF	2		0000 4000	0000 5FFF
1		0001 0000	0001 FFFF	1		0000 2000	0000 3FFF
0		0000 0000	0000 FFFF	0		0000 0000	0000 1FFF

Table 6: 32Mb Memory Map – x16 Top and Bottom Boot [70:0]

Block	Block Size	Address Range (x16 Top Boot)		Block	Block Size	Address Range (x16 Bottom Boot)	
		Start	End			Start	End
70	4KW	001F F000	001F FFFF	70	32KW	001F 8000	001F FFFF
69		001F E000	001F EFFF	69		001F 0000	001F 7FFF
68		001F D000	001F DFFF	68		001E 8000	001E FFFF
67		001F C000	001F CFFF	⋮	⋮	⋮	⋮
66		001F B000	001F BFFF	8	32KW	0000 8000	0000 FFFF
65		001F A000	001F AFFF	7	4KW	0000 7000	0000 7FFF
64		001F 9000	001F 9FFF	6		0000 6000	0000 6FFF
63		001F 8000	001F 8FFF	5		0000 5000	0000 5FFF
62	32KW	001F 0000	001F 7FFF	4		0000 4000	0000 4FFF
⋮	⋮	⋮	⋮	3		0000 3000	0000 3FFF
2	32KW	0001 0000	0001 7FFF	2		0000 2000	0000 2FFF
1		0000 8000	0000 FFFF	1		0000 1000	0000 1FFF
0		0000 0000	0000 7FFF	0		0000 0000	0000 0FFF

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Table 7: 32Mb Memory Map – x8/x16 Uniform Blocks [63:0]

Block	Block Size	Address Range (x8)		Block	Block Size	Address Range (x16)	
		Start	End			Start	End
63	64KB	03F 0000h	03F FFFFh	63	32KW	01F 8000h	01F FFFFh
⋮		⋮	⋮	⋮		⋮	⋮
0		000 0000h	000 FFFFh	0		000 0000h	000 7FFFh

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Memory Map – 64Mb

Table 8: 64Mb Memory Map – x8 Top and Bottom Boot [134:0]

Block	Block Size	Address Range (x8 Top Boot)		Block	Block Size	Address Range (x8 Bottom Boot)	
		Start	End			Start	End
134	8KB	007F E000	007F FFFF	134	64KB	007F 0000	007F FFFF
133		007F C000	007F DFFF	133		007E 0000	007E FFFF
132		007F A000	007F BFFF	132		007D 0000	007D FFFF
131		007F 8000	007F 9FFF	⋮	⋮	⋮	⋮
130		007F 6000	007F 7FFF	8	64KB	0001 0000	0001 FFFF
129		007F 4000	007F 5FFF	7	8KB	0000 E000	0000 FFFF
128		007F 2000	007F 3FFF	6		0000 C000	0000 DFFF
127		007F 0000	007F 1FFF	5		0000 A000	0000 BFFF
126	64KB	007E 0000	007E FFFF	4		0000 8000	0000 9FFF
⋮	⋮	⋮	⋮	3		0000 6000	0000 7FFF
2	64KB	0002 0000	0002 FFFF	2		0000 4000	0000 5FFF
1		0001 0000	0001 FFFF	1		0000 2000	0000 3FFF
0		0000 0000	0000 FFFF	0		0000 0000	0000 1FFF

Table 9: 64Mb Memory Map – x16 Top and Bottom Boot [134:0]

Block	Block Size	Address Range (x16 Top Boot)		Block	Block Size	Address Range (x16 Bottom Boot)	
		Start	End			Start	End
134	4KW	003F F000	003F FFFF	134	32KW	003F 8000	003F FFFF
133		003F E000	003F EFFF	133		003F 0000	003F 7FFF
132		003F D000	003F DFFF	132		003E 8000	003E FFFF
131		003F C000	003F CFFF	⋮	⋮	⋮	⋮
130		003F B000	003F BFFF	8	32KW	0000 8000	0000 FFFF
129		003F A000	003F AFFF	7	4KW	0000 7000	0000 7FFF
128		003F 9000	003F 9FFF	6		0000 6000	0000 6FFF
127		003F 8000	003F 8FFF	5		0000 5000	0000 5FFF
126	32KW	003F 0000	003F 7FFF	4		0000 4000	0000 4FFF
⋮	⋮	⋮	⋮	3		0000 3000	0000 3FFF
2	32KW	0001 0000	0001 7FFF	2		0000 2000	0000 2FFF
1		0000 8000	0000 FFFF	1		0000 1000	0000 1FFF
0		0000 0000	0000 7FFF	0		0000 0000	0000 0FFF

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Table 10: 64Mb Memory Map – x8/x16 Uniform Blocks [127:0]

Block	Block Size	Address Range (x8)		Block	Block Size	Address Range (x16)	
		Start	End			Start	End
127	64KB	07F 0000h	07F FFFFh	127	32KW	03F 8000h	03F FFFFh
⋮		⋮	⋮	⋮		⋮	⋮
63		03F 0000h	03F FFFFh	63		01F 8000h	01F FFFFh
⋮		⋮	⋮	⋮		⋮	⋮
0		000 0000h	000 FFFFh	0		000 0000h	000 7FFFh

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Memory Map – 128Mb

Table 11: 128Mb Memory Map – x8/x16 Uniform Blocks [127:0]

Block	Block Size	Address Range (x8)		Block	Block Size	Address Range (x16)	
		Start	End			Start	End
127	128KB	0FE 0000h	0FF FFFFh	127	64KW	07F 0000h	07F FFFFh
⋮		⋮	⋮	⋮		⋮	⋮
63		07E 0000h	07F FFFFh	63		03F 0000h	03F FFFFh
⋮		⋮	⋮	⋮		⋮	⋮
0		000 0000h	001 FFFFh	0		000 0000h	000 FFFFh

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Bus Operations

Table 12: Bus Operations

Notes 1 and 2 apply to entire table

Operation	CE#	OE#	WE#	RST#	V_{PP}/WP#	8-Bit Mode			16-Bit Mode	
						A[MAX:0], DQ15/A-1	DQ[14:8]	DQ[7:0]	A[MAX:0]	DQ15/A-1, DQ[14:0]
READ	L	L	H	H	X	Byte address	High-Z	Data output	Word address	Data output
WRITE	L	H	L	H	H[3]	Command address	High-Z	Data input[4]	Command address	Data input[4]
STANDBY	H	X	X	H	H	X	High-Z	High-Z	X	High-Z
OUTPUT DISABLE	L	H	H	H	X	X	High-Z	High-Z	X	High-Z
RESET	X	X	X	L	X	X	High-Z	High-Z	X	High-Z

Notes:
1. Typical glitches of less than 3ns on CE#, WE#, and RST# are ignored by the device and do not affect bus operations.
2. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
3. If WP# is LOW, then the highest or the lowest block remains protected, or the top two blocks or the bottom two blocks, depending on line item.
4. Data input is required when issuing a command sequence or when performing data polling or block protection.

Read

Bus READ operations read from the memory cells, registers, or CFI space. To accelerate the READ operation, the memory array can be read in page mode where data is internally read and stored in a page buffer.

Page size is 8 words (16 bytes) and is addressed by address inputs A[2:0] in x16 bus mode and A[2:0] plus DQ15/A-1 in x8 bus mode. The extended memory blocks and CFI area do not support page read mode.

A valid bus READ operation involves setting the desired address on the address inputs, taking CE# and OE# LOW, and holding WE# HIGH. The data I/Os will output the value. (See AC Characteristics for details about when the output becomes valid.)

Write

Bus WRITE operations write to the command interface. A valid bus WRITE operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. The data I/Os are latched by the command interface on the rising edge of CE# or WE#, whichever occurs first. OE# must remain HIGH during the entire bus WRITE operation. (See AC Characteristics for timing requirement details.)

Standby

Driving CE# HIGH in read mode causes the device to enter standby, and data I/Os to be High-Z. To reduce the supply current to the standby supply current (I_{CC2}), CE# must be held within V_{CC} ±0.3V. (See DC Characteristics.)

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During PROGRAM or ERASE operations the device will continue to use the program/erase supply current (I_{CC3}) until the operation completes.

Output Disable

Data I/Os are High-Z when OE# is HIGH.

Reset

During reset mode the device is deselected and the outputs are High-Z. The device is in reset mode when RST# is LOW. The power consumption is reduced to the standby level, independently from CE#, OE#, or WE# inputs.

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Registers

Status Register

Table 13: Status Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ7	Data polling bit	0 or 1, depending on operations	Monitors whether the program/erase controller has successfully completed its operation, or has responded to an ERASE SUSPEND operation.	2, 3, 4
DQ6	Toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors whether the program/erase controller has successfully completed its operations, or has responded to an ERASE SUSPEND operation. During a PROGRAM/ERASE operation, DQ6 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from any address.	3, 4, 5
DQ5	Error bit	0 = Success 1 = Failure	Identifies errors detected by the program/erase controller. DQ5 is set to 1 when a PROGRAM, BLOCK ERASE, or CHIP ERASE operation fails to write the correct data to the memory, or when a BLANK CHECK operation fails.	4, 6
DQ3	Erase timer bit	0 = Erase not in progress 1 = Erase in progress	Identifies the start of program/erase controller operation during a BLOCK ERASE command. Before the program/erase controller starts, this bit set to 0, and additional blocks to be erased can be written to the command interface.	4
DQ2	Alternative toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors the program/erase controller during ERASE operations. During CHIP ERASE, BLOCK ERASE, and ERASE SUSPEND operations, DQ2 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from addresses within the blocks being erased.	3, 4
DQ1	Buffered program abort bit	1 = Abort	Indicates a BUFFER PROGRAM operation abort. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode. (See WRITE TO BUFFER PROGRAM command.)	

Notes:
1. The status register can be read during PROGRAM, ERASE, or ERASE SUSPEND operations; the READ operation outputs data on DQ[7:0].
2. For a PROGRAM operation in progress, DQ7 outputs the complement of the bit being programmed. For a READ operation from the address previously programmed successfully, DQ7 outputs existing DQ7 data. For a READ operation from addresses with blocks to be erased while an ERASE SUSPEND operation is in progress, DQ7 outputs 0; upon successful completion of the ERASE SUSPEND operation, DQ7 outputs 1. For an ERASE or BLANK CHECK operation in progress, DQ7 outputs 0; upon either operation's successful completion, DQ7 outputs 1.
3. After successful completion of a PROGRAM, ERASE, or BLANK CHECK operation, the device returns to read mode.
4. During erase suspend mode, READ operations to addresses within blocks not being erased output memory array data as if in read mode. A protected block is treated the same as a block not being erased. See the Toggle Flowchart for more information.

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5. During erase suspend mode, DQ6 toggles when addressing a cell within a block being erased. The toggling stops when the program/erase controller has suspended the ERASE operation. See the Toggle Flowchart for more information.
6. When DQ5 is set to 1, a READ/RESET command must be issued before any subsequent command.

Table 14: Operations and Corresponding Bit Settings

Note 1 applies to entire table

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#	Notes
PROGRAM	Any address	DQ7#	Toggle	0	–	–	0	0	2
BLANK CHECK	Any address	1	Toggle	0	–	–	0	0	
CHIP ERASE	Any address	0	Toggle	0	1	Toggle	–	0	
BLOCK ERASE before time-out	Erasing block	0	Toggle	0	0	Toggle	–	0	
	Non-erasing block	0	Toggle	0	0	No toggle	–	0	
BLOCK ERASE	Erasing block	0	Toggle	0	1	Toggle	–	0	
	Non-erasing block	0	Toggle	0	1	No toggle	–	0	
PROGRAM SUSPEND	Programming block	Invalid operation						High-Z	
	Nonprogramming block	Outputs memory array data as if in read mode						High-Z	
ERASE SUSPEND	Erasing blk	1	No Toggle	0	–	Toggle	–	High-Z	
	Non-erasing blk	Outputs memory array data as if in read mode						High-Z	
PROGRAM during ERASE SUSPEND	Erasing block	DQ7#	Toggle	0	–	Toggle	–	0	2
	Non-erasing block	DQ7#	Toggle	0	–	No Toggle	–	0	2
BUFFERED PROGRAM ABORT	Any address	DQ7#	Toggle	0	–	–	1	High-Z	
PROGRAM Error	Any address	DQ7#	Toggle	1	–	–	–	High-Z	2
ERASE Error	Erase success block	0	Toggle	1	1	No toggle	–	High-Z	
	Erase fail block	0	Toggle	1	1	Toggle	–	High-Z	
BLANK CHECK Error	Any address	1	Toggle	1	1	Toggle	–	High-Z	

Notes: 1. Unspecified data bits should be ignored.
2. DQ7# for buffer program is related to the last address location loaded.

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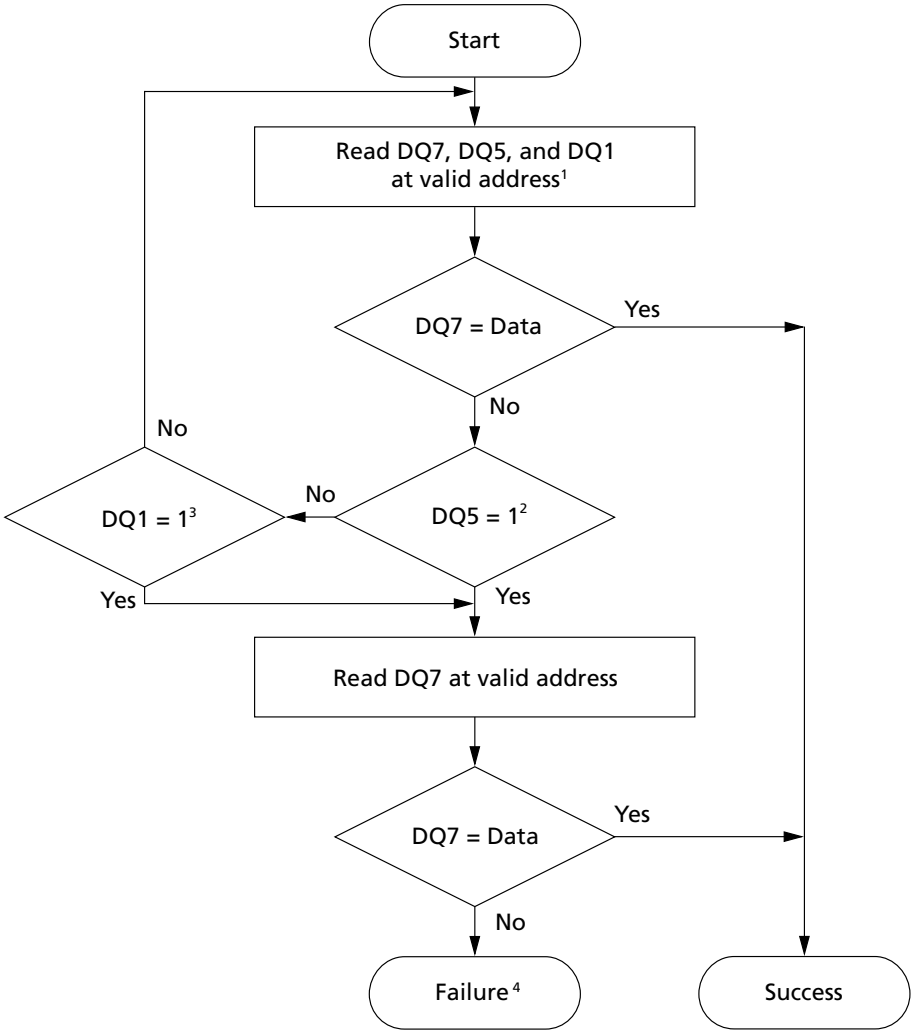
Figure 6: Data Polling Flowchart



Notes:
1. Valid address is the address being programmed or an address within the block being erased or on which a BLANK CHECK operation has been executed.
2. The data polling process does not support the BLANK CHECK operation. The process represented in the Toggle Bit Flowchart figure can provide information on the BLANK CHECK operation.
3. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

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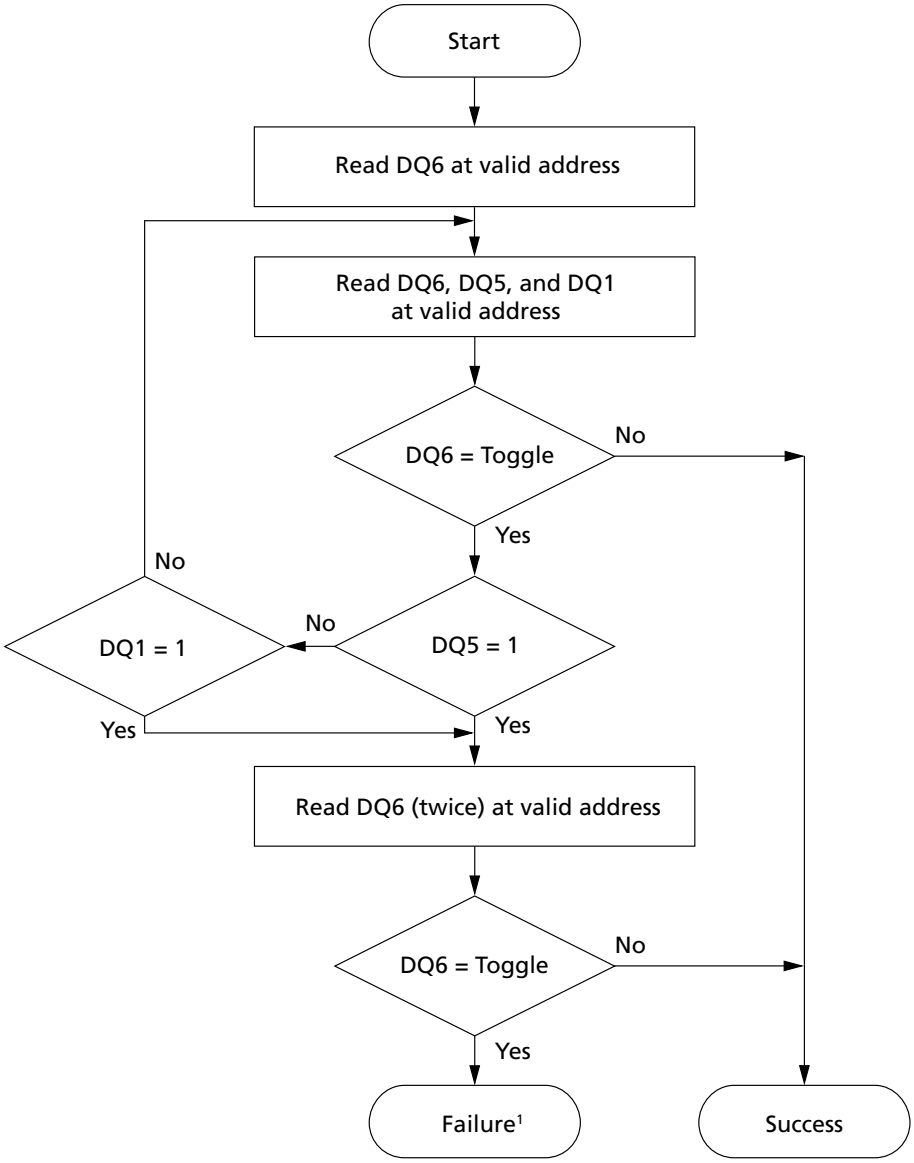
Figure 7: Toggle Bit Flowchart



Note: 1. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

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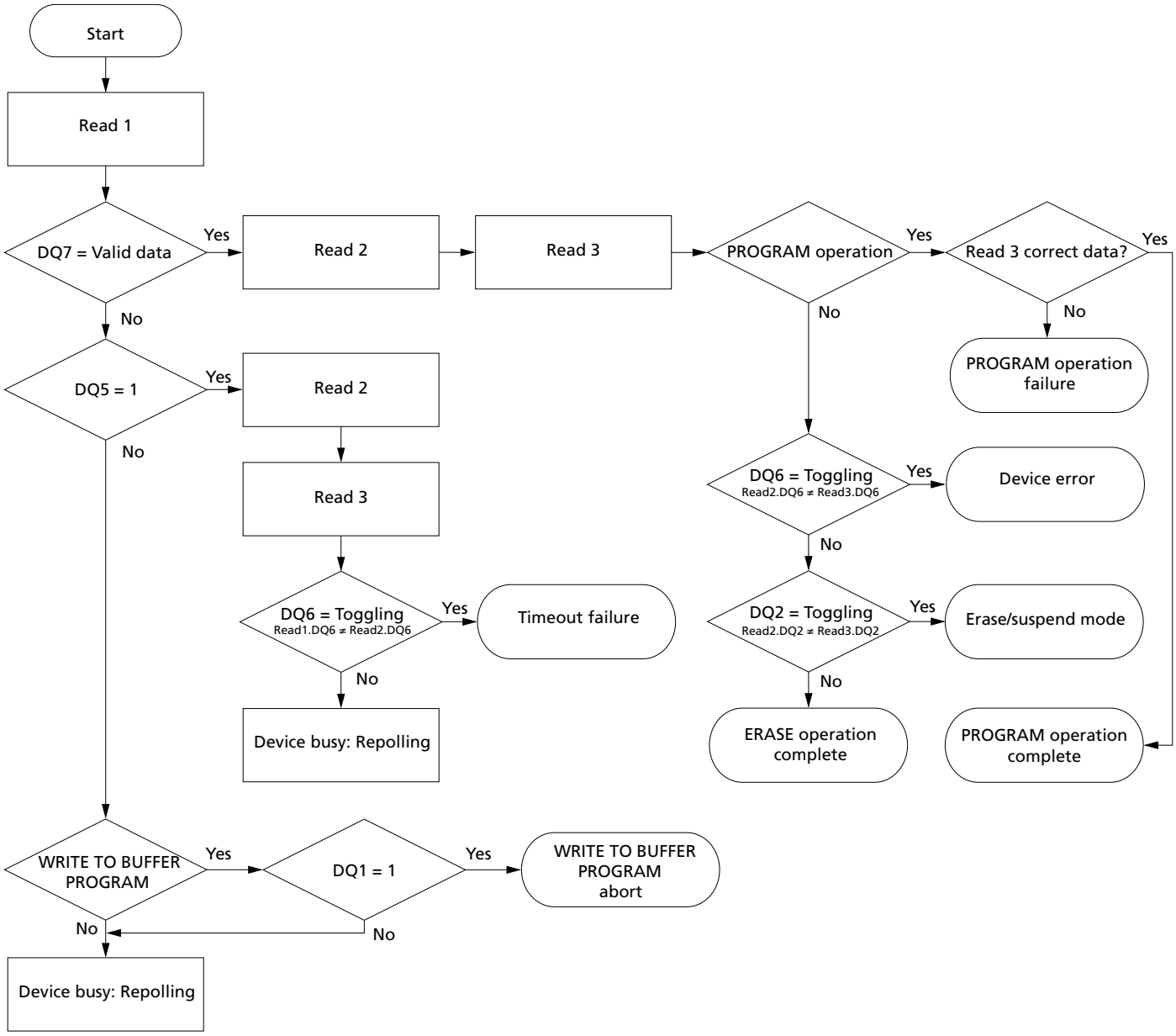
Figure 8: Status Register Polling Flowchart



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Lock Register

Table 15: Lock Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ2	Password protection mode lock bit	0 = Password protection mode enabled 1 = Password protection mode disabled (Default)	Places the device permanently in password protection mode.	2
DQ1	Nonvolatile protection mode lock bit	0 = Nonvolatile protection mode enabled with password protection mode permanently disabled 1 = Nonvolatile protection mode enabled (Default)	Places the device in nonvolatile protection mode with password protection mode permanently disabled. When shipped from the factory, the device will operate in nonvolatile protection mode, and the memory blocks are unprotected.	2
DQ0	Extended memory block protection bit	0 = Protected 1 = Unprotected (Default)	If the device is shipped with the extended memory block unlocked, the block can be protected by setting this bit to 0. The extended memory block protection status can be read in auto select mode by issuing an AUTO SELECT command.	

Notes:
1. The lock register is a 16-bit, one-time programmable register. DQ[15:3] are reserved and are set to a default value of 1.
2. The password protection mode lock bit and nonvolatile protection mode lock bit cannot both be programmed to 0. Any attempt to program one while the other is programmed causes the operation to abort, and the device returns to read mode. The device is shipped from the factory with the default setting.

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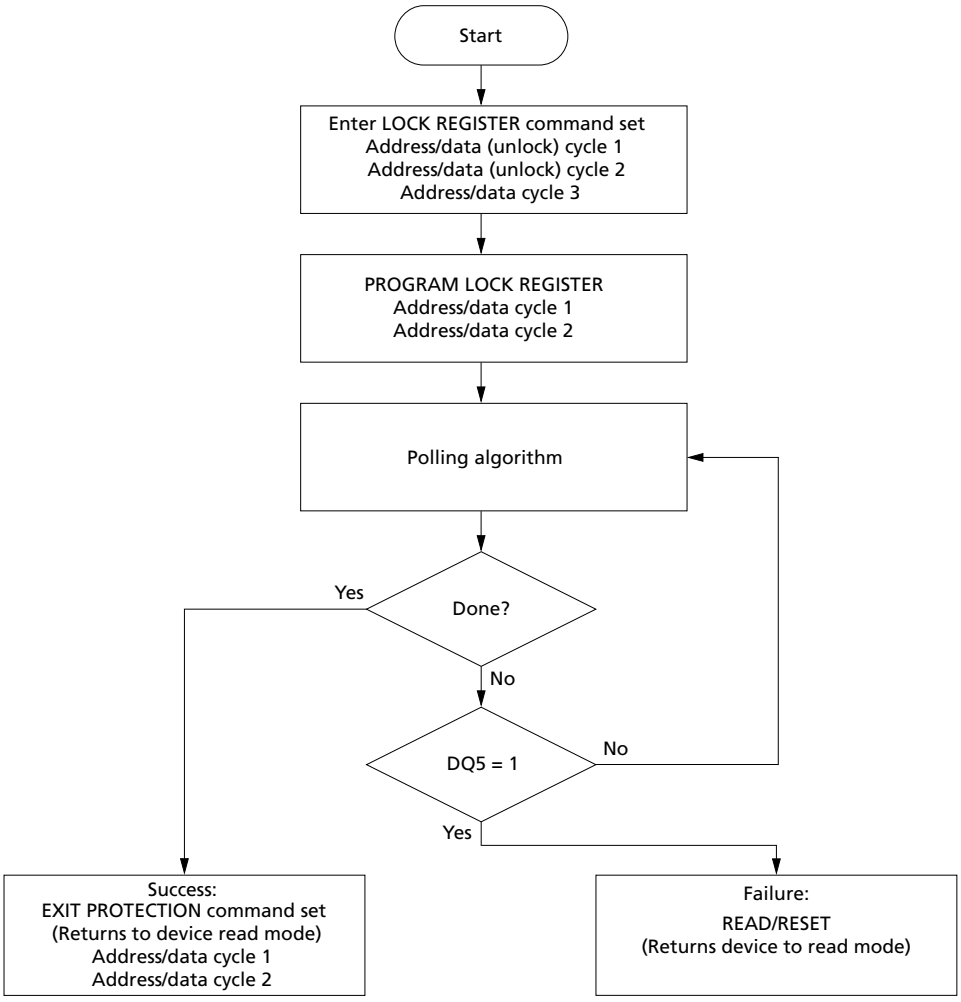
Figure 9: Lock Register Program Flowchart



Notes:
1. Each lock register bit can be programmed only once.
2. See the Block Protection Command Definitions table for address-data cycle details.

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Standard Command Definitions – Address-Data Cycles

Table 16: Standard Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit

Note 1 applies to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
READ and AUTO SELECT Operations														
READ/RESET (F0h)	x8	X	F0											
		AAA	AA	555	55	X	F0							
	x16	X	F0											
		555	AA	2AA	55	X	F0							
READ CFI (98h)	x8	AA	98											
	x16	55												
AUTO SELECT (90h)	x8	AAA	AA	555	55	AAA	90	Note 2	Note 2					2, 3, 4
	x16	555		2AA		555								
BYPASS Operations														
UNLOCK BYPASS (20h)	x8	AAA	AA	555	55	AAA	20							
	x16	555		2AA		555								
UNLOCK BYPASS RESET (90h/00h)	x8	X	90	X	00									
	x16													
PROGRAM Operations														
PROGRAM (A0h)	x8	AAA	AA	555	55	AAA	A0	PA	PD					
	x16	555		2AA		555								
UNLOCK BYPASS PROGRAM (A0h)	x8	X	A0	PA	PD									6
	x16													
DOUBLE BYTE/WORD PROGRAM (50h)	x8	AAA	50	PA2	PD									
	x16	555												
QUADRUPLE BYTE/ WORD PROGRAM (56h)	x8	AAA	56	PA4	PD									
	x16	555												
OCTUPLE BYTE PROGRAM (8Bh)	x8	AAA	8B	PA8	PD									5
WRITE TO BUFFER PROGRAM (25h)	x8	AAA	AA	555	55	BAd	25	BAd	N	PA	PD			7, 8, 9
	x16	555		2AA										
ENHANCED WRITE TO BUFFER PROGRAM (33h)	x16	555	AA	2AA	55	BAd	33	PA	PD					7, 9, 10
UNLOCK BYPASS WRITE TO BUFFER PROGRAM (25h)	x8	BAd	25	BAd	N	PA	PD							5
	x16													

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Table 16: Standard Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit (Continued)

Note 1 applies to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
UNLOCK BYPASS ENHANCED WRITE TO BUFFER PROGRAM (33h)	x16	BAd	33	PA	PD									10
WRITE TO BUFFER PROGRAM CONFIRM (29h)	x8	BAd	29											
	x16													
ENHANCED WRITE TO BUFFER PROGRAM CONFIRM (29h)	x8	BAd	29											
	x16													
BUFFERED PROGRAM ABORT and RESET (F0h)	x8	AAA	AA	555	55	AAA	F0							
	x16	555		2AA		555								
PROGRAM SUSPEND (B0h)	x8	X	B0											
	x16													
PROGRAM RESUME (30h)	x8	X	30											
	x16													
ERASE Operations														
CHIP ERASE (80/10h)	x8	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10	
	x16	555		2AA		555		555		2AA		555		
UNLOCK BYPASS CHIP ERASE (80/10h)	x8	X	80	X	10									5
	x16													
BLOCK ERASE (80/30h)	x8	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BAd	30	11
	x16	555		2AA		555		555		2AA				
UNLOCK BYPASS BLOCK ERASE (80/30h)	x8	X	80	BAd	30									5
	x16													
ERASE SUSPEND (B0h)	x8	X	B0											
	x16													
ERASE RESUME (30h)	x8	X	30											
	x16													
BLANK CHECK Operations														
BLANK CHECK SETUP (EB/76h)	x8	AAA	AA	555	55	BAd	EB	BAd	76	BAd	00	BAd	00	
	x16	555		2AA										
BLANK CHECK CONFIRM and READ (29h)	x8	BAd	29	BAd	Note 2									2
	x16													

Notes: 1. A = Address; D = Data; X = "Don't Care;" BAd = Any address in the block; N = Number of bytes to be programmed; PA = Program address; PA2 = Program address with constant AMAX:A0 for x8 or AMAX:A1 for x16, which should be used two times to select adjacent

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two bytes/words; PA4 = Program address with constant AMAX:A1 for x8 or AMAX:A2 for x16, which should be used four times to select adjacent four bytes/words; PA8 = Program address with constant AMAX:A2 for x8, which should be used eight times to select adjacent eight bytes; PD = Program data; Gray shading = Not applicable. All values in the table are hexadecimal. Some commands require both a command code and sub-code.

2. These cells represent READ cycles (versus WRITE cycles for the others).
3. AUTO SELECT enables the device to read the manufacturer code, device code, block protection status, and extended memory block protection indicator.
4. AUTO SELECT addresses and data are specified in the Electronic Signature table and the Extended Memory Block Protection table.
5. For any UNLOCK BYPASS ERASE/PROGRAM command, the first two UNLOCK cycles are unnecessary.
6. This command is only for x8 devices.
7. BAd must be the same as the address loaded during the WRITE TO BUFFER PROGRAM 3rd and 4th cycles.
8. WRITE TO BUFFER PROGRAM operation: maximum cycles = 261 (x8) and 261 (x16). UNLOCK BYPASS WRITE TO BUFFER PROGRAM operation: maximum cycles = 259 (x8), 259 (x16). WRITE TO BUFFER PROGRAM operation: N + 1 = bytes to be programmed; maximum buffer size = 256 bytes (x8) and 512 bytes (x16).
9. For x8, A[MAX:7] address pins should remain unchanged while A[6:0] and A-1 pins are used to select a byte within the N + 1 byte page. For x16, A[MAX:8] address pins should remain unchanged while A[7:0] pins are used to select a word within the N+1 word page.
10. This command is only for x16 devices. For ENHANCED WRITE TO BUFFER PROGRAM operation, total cycles = 259. For UNLOCK BYPASS ENHANCED WRITE TO BUFFER PROGRAM operation, total cycles = 257.
11. BLOCK ERASE address cycles can extend beyond six address-data cycles, depending on the number of blocks to erase.

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READ and AUTO SELECT Operations

READ/RESET Command

The READ/RESET (F0h) command returns the device to read mode and resets the errors in the status register. One or three bus WRITE operations can be used to issue the READ/RESET command.

To return the device to read mode, this command can be issued between bus WRITE cycles before the start of a PROGRAM or ERASE operation. If the READ/RESET command is issued during the timeout of a BLOCK ERASE operation, the device requires up to 10µs to abort, during which time no valid data can be read.

This command will not abort an ERASE operation while in erase suspend.

READ CFI Command

The READ CFI (98h) command puts the device in read CFI mode and is only valid when the device is in read array or auto select mode. One bus WRITE cycle is required to issue the command.

Once in read CFI mode, bus READ operations will output data from the CFI memory area. (Refer to the Common Flash Interface for details.) A READ/RESET command must be issued to return the device to the previous mode (read array or auto select). A second READ/RESET command is required to put the device in read array mode from auto select mode.

AUTO SELECT Command

At power-up or after a hardware reset, the device is in read mode. It can then be put in auto select mode by issuing an AUTO SELECT (90h) command. Auto select mode enables the following device information to be read:

- Electronic signature, which includes manufacturer and device code information as shown in the Electronic Signature table.
- Block protection, which includes the block protection status and extended memory block protection indicator, as shown in the Block Protection table.

Electronic signature or block protection information is read by executing a READ operation with control signals and addresses set, as shown in the Read Electronic Signature table or the Block Protection table, respectively. In addition, this device information can be read or set by issuing an AUTO SELECT command.

Auto select mode can be used by the programming equipment to automatically match a device with the application code to be programmed.

Three consecutive bus WRITE operations are required to issue an AUTO SELECT command. The device remains in auto select mode until a READ/RESET or READ CFI command is issued.

The device cannot enter auto select mode when a PROGRAM or ERASE operation is in progress (RY/BY# LOW). However, auto select mode can be entered if the PROGRAM or ERASE operation has been suspended by issuing a PROGRAM SUSPEND or ERASE SUSPEND command.

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Auto select mode is exited by performing a reset. The device returns to read mode unless it entered auto select mode after an ERASE SUSPEND or PROGRAM SUSPEND command, in which case it returns to erase or program suspend mode.

Table 17: Read Electronic Signature

Note 1 applies to entire table

Read Cycle		CE#	OE#	WE#	Address Input							Data Input/Output		
					8-Bit/16-Bit						8-Bit Only	8-Bit Only		16-Bit Only
					A[MAX:11]	A[10:4]	A3	A2	A1	A0	A-1	DQ[14:8]	DQ[7:0]	DQ[15:0]
Manufacturer code		L	L	H	X	L	L	L	L	L	X	X	89h	0089h
Device code 1		L	L	H	X	L	L	L	L	H	X	X	7Eh	227Eh
Device code 2	128Mb	L	L	H	X	L	H	H	H	L	X	X	21h	2221h
	64Mb boot												10h	2210h
	64Mb uniform												0Ch	220Ch
	32Mb boot												1Ah	221Ah
	32Mb uniform												1Dh	221Dh
Device code 3	128Mb uniform	L	L	H	X	L	H	H	H	H	X	X	01h	2201h
	64Mb uniform													
	64Mb top													
	32Mb top													
Device code 3	64Mb bottom	L	L	H	X	L	H	H	H	H	X	X	00h	2200h
	32Mb bottom													
	32Mb uniform													

Note: 1. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.

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Table 18: Block Protection

Note 1 applies to entire table

Read Cycle		CE#	OE#	WE#	Address Input						Data Input/Output		
					8-Bit/16-Bit					8-Bit Only	8-Bit Only		16-Bit Only
					A[MAX:15]	A[14:11]	A[10:2]	A1	A0	A-1	DQ[14:8]	DQ[7:0]	DQ[15:0]
Extended memory Block protection indicator (DQ7)	M29EWL 128Mb	L	L	H	X	X	L	H	H	X	X	89h[2]	0089h[2]
												09h[3]	0009h[3]
	M29EWH 128Mb	L	L	H	X	X	L	H	H	X	X	99h[2]	0099h[2]
												19h[3]	0019h[3]
	M29EWL 64Mb 32Mb	L	L	H	X	X	L	H	H	X	X	8Ah[2]	008Ah[2]
												0Ah[3]	000Ah[3]
	M29EWH 64Mb 32Mb	L	L	H	X	X	L	H	H	X	X	9Ah[2]	009Ah[2]
												1Ah[3]	001Ah[3]
	M29EWB 64Mb 32Mb	L	L	H	X	X	L	H	H	X	X	8Ah[2]	008Ah[2]
												0Ah[3]	000Ah[3]
	M29EWT 64Mb 32Mb	L	L	H	X	X	L	H	H	X	X	9Ah[2]	009Ah[2]
												1Ah[3]	001Ah[3]
Block protection status		L	L	H	Block base address[6]	L	L	H	L	X	X	01h[4]	0001h[4]
												00h[5]	0000h[5]

Notes:
1. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
2. Micron-prelocked (permanent).
3. Customer-lockable.
4. Protected: 01h (in x8 mode) is output on DQ[7:0].
5. Unprotected: 00h (in x8 mode) is output on DQ[7:0].
6. Block base address for 128Mb device, should be A[MAX:16], while A15 = X.

Bypass Operations

UNLOCK BYPASS Command

The UNLOCK BYPASS (20h) command is used to place the device in unlock bypass mode. Three bus WRITE operations are required to issue the UNLOCK BYPASS command.

When the device enters unlock bypass mode, the two initial UNLOCK cycles required for a standard PROGRAM or ERASE operation are not needed, thus enabling faster total program or erase time.

The UNLOCK BYPASS command is used in conjunction with UNLOCK BYPASS PROGRAM or UNLOCK BYPASS ERASE commands to program or erase the device faster than with standard PROGRAM or ERASE commands. Using these commands can save

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considerable time when the cycle time to the device is long. When in unlock bypass mode, only the following commands are valid:

- The UNLOCK BYPASS PROGRAM command can be issued to program addresses within the device.
- The UNLOCK BYPASS BLOCK ERASE command can then be issued to erase one or more memory blocks.
- The UNLOCK BYPASS CHIP ERASE command can be issued to erase the whole memory array.
- The UNLOCK BYPASS WRITE TO BUFFER PROGRAM and UNLOCK BYPASS ENHANCED WRITE TO BUFFER PROGRAM commands can be issued to speed up the programming operation.
- The UNLOCK BYPASS RESET command can be issued to return the device to read mode.

In unlock bypass mode, the device can be read as if in read mode.

In addition to the UNLOCK BYPASS command, when V_{PP}/WP# is raised to V_{PPH}, the device automatically enters unlock bypass mode. When V_{PP}/WP# returns to V_{IH} or V_{IL}, the device is no longer in unlock bypass mode, and normal operation resumes. The transitions from V_{IH} to V_{PPH} and from V_{PPH} to V_{IH} must be slower than ^{t}VHVPP. (See the Accelerated Program, Data Polling/Toggle AC Characteristics.)

Note: Micron recommends entering and exiting unlock bypass mode using the ENTER UNLOCK BYPASS and UNLOCK BYPASS RESET commands rather than raising V_{PP}/WP# to V_{PPH}. V_{PP}/WP# should never be raised to V_{PPH} from any mode except read mode; otherwise, the device may be left in an indeterminate state. V_{PP}/WP# should not remain at V_{PPH} for than 80 hours cumulative.

UNLOCK BYPASS RESET Command

The UNLOCK BYPASS RESET (90/00h) command is used to return to read/reset mode from unlock bypass mode. Two bus WRITE operations are required to issue the UNLOCK BYPASS RESET command. The READ/RESET command does not exit from unlock bypass mode.

Program Operations

PROGRAM Command

The PROGRAM (A0h) command can be used to program a value to one address in the memory array. The command requires four bus WRITE operations, and the final WRITE operation latches the address and data in the internal state machine and starts the program/erase controller. After programming has started, bus READ operations output the status register content.

Programming can be suspended and then resumed by issuing a PROGRAM SUSPEND command and a PROGRAM RESUME command, respectively.

If the address falls in a protected block, the PROGRAM command is ignored, and the data remains unchanged. The status register is not read, and no error condition is given.

After the PROGRAM operation has completed, the device returns to read mode, unless an error has occurred. When an error occurs, bus READ operations to the device contin-

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ue to output the status register. A READ/RESET command must be issued to reset the error condition and return the device to read mode.

The PROGRAM command cannot change a bit set to 0 back to 1, and an attempt to do so is masked during a PROGRAM operation. Instead, an ERASE command must be used to set all bits in one memory block or in the entire memory from 0 to 1.

The PROGRAM operation is aborted by performing a hardware reset or by powering-down the device. In this case, data integrity cannot be ensured, and it is recommended that the words or bytes that were aborted be reprogrammed.

UNLOCK BYPASS PROGRAM Command

When the device is in unlock bypass mode, the UNLOCK BYPASS PROGRAM (A0h) command can be used to program one address in the memory array. The command requires two bus WRITE operations instead of four required by a standard PROGRAM command; the final WRITE operation latches the address and data and starts the program/erase controller (The standard PROGRAM command requires four bus WRITE operations). The PROGRAM operation using the UNLOCK BYPASS PROGRAM command behaves identically to the PROGRAM operation using the PROGRAM command. The operation cannot be aborted. A bus READ operation to the memory outputs the status register.

DOUBLE BYTE/WORD PROGRAM Command

The DOUBLE BYTE/WORD PROGRAM (50h) command is used to write a page of two adjacent bytes/words in parallel. The two bytes/words must differ only for the address A-1 or A0, respectively. Three bus write cycles are necessary to issue the command: The first bus cycle sets up the command, the second bus cycle latches the address and data of the first byte/word to be programmed, and the third bus cycle latches the address and data of the second byte/word to be programmed and starts the program/erase controller.

Note: The DOUBLE BYTE/WORD PROGRAM command is available only in the 32Mb and 64Mb devices; also only V_{PPL} is to be applied to the V_{PP}/WP# pin.

QUADRUPLE BYTE/WORD PROGRAM Command

The QUADRUPLE BYTE/WORD PROGRAM (56h) command is used to write a page of four adjacent bytes/words in parallel. The four bytes/words must differ for addresses A0, DQ15/A-1 in x8 mode or for addresses A1, A0 in x16 mode. Five bus write cycles are necessary to issue the command: The first bus cycle sets up the command, the second bus cycle latches the address and data of the first byte/word to be programmed, the third bus cycle latches the address and data of the second byte/word to be programmed, the fourth bus cycle latches the address and data of the third byte/word to be programmed, and the fifth bus cycle latches the address and data of the fourth byte/word to be programmed and starts the program/erase controller.

Note: The QUADRUPLE BYTE/WORD PROGRAM command is available only in the 32Mb and 64Mb devices; also only V_{PPL} is to be applied to the V_{PP}/WP# pin.

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OCTUPLE BYTE PROGRAM Command

The OCTUPLE BYTE PROGRAM (8Bh) command is used to write a page of eight adjacent bytes in parallel. The eight bytes must differ for addresses A1, A0, DQ15/A-1 in x8 mode only.

Nine bus write cycles are necessary to issue the command: The first bus cycle sets up the command, the second bus cycle latches the address and data of the first byte to be programmed, the third bus cycle latches the address and data of the second byte to be programmed, the fourth bus cycle latches the address and data of the third byte to be programmed, the fifth bus cycle latches the address and data of the fourth byte to be programmed, the sixth bus cycle latches the address and data of the fifth byte to be programmed, the seventh bus cycle latches the address and data of the sixth byte to be programmed, the eighth bus cycle latches the address and data of the seventh byte to be programmed, and the ninth bus cycle latches the address and data of the eighth byte to be programmed, and starts the program/erase controller.

Note: The OCTUPLE BYTE PROGRAM command is available only in the 32Mb and 64Mb x8 devices; also only V_{PPL} is to be applied to the V_{PP}/WP# pin.

WRITE TO BUFFER PROGRAM Command

The WRITE TO BUFFER PROGRAM (25h) command makes use of the program buffer to speed up programming and dramatically reduces system programming time compared to the standard non-buffered PROGRAM command. 32Mb through 128Mb devices support a 256-word maximum program buffer.

When issuing a WRITE TO BUFFER PROGRAM command, V_{PP}/WP# can be held HIGH or raised to V_{PPH}. Also, it can be held LOW if the block is not the lowest or highest block or the top/bottom two blocks, depending on the part number. When V_{PPH} is applied to the V_{PP}/WP# pin during execution of the command, programming speed increases. (See the Accelerated Program, Data Polling/Toggle AC Characteristics section.)

The following successive steps are required to issue the WRITE TO BUFFER PROGRAM command:

First, two UNLOCK cycles are issued. Next, a third bus WRITE cycle sets up the WRITE TO BUFFER PROGRAM command. The set-up code can be addressed to any location within the targeted block. Then, a fourth bus WRITE cycle sets up the number of words/bytes to be programmed. Value *n* is written to the same block address, where *n + 1* is the number of words/bytes to be programmed. Value *n + 1* must not exceed the size of the program buffer, or the operation will abort. A fifth cycle loads the first address and data to be programmed. Last, *n* bus WRITE cycles load the address and data for each word/byte into the program buffer. Addresses must lie within the range from *the start address +1* to *the start address + (n - 1)*.

Optimum programming performance and lower power usage are achieved by aligning the starting address at the beginning of a 256-word boundary (A[7:0] = 0x000h). Any buffer size smaller than 256 words is allowed within a 256-word boundary, while all addresses used in the operation must lie within the 256-word boundary. In addition, any crossing boundary buffer program will result in a program abort. For a x8 device, maximum buffer size is 256 bytes; for a x16 device, the maximum buffer size is 512 bytes.

To program the content of the program buffer, this command must be followed by a WRITE TO BUFFER PROGRAM CONFIRM command.

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If an address is written several times during a WRITE TO BUFFER PROGRAM operation, the address/data counter will be decremented at each data load operation, and the data will be programmed to the last word loaded into the buffer.

Invalid address combinations or the incorrect sequence of bus WRITE cycles will abort the WRITE TO BUFFER PROGRAM command.

The status register bits DQ1, DQ5, DQ6, DQ7 can be used to monitor the device status during a WRITE TO BUFFER PROGRAM operation.

The WRITE TO BUFFER PROGRAM command should not be used to change a bit set to 0 back to 1, and an attempt to do so is masked during the operation. Rather than the WRITE TO BUFFER PROGRAM command, the ERASE command should be used to set memory bits from 0 to 1.

Figure 10: Boundary Condition of Program Buffer Size

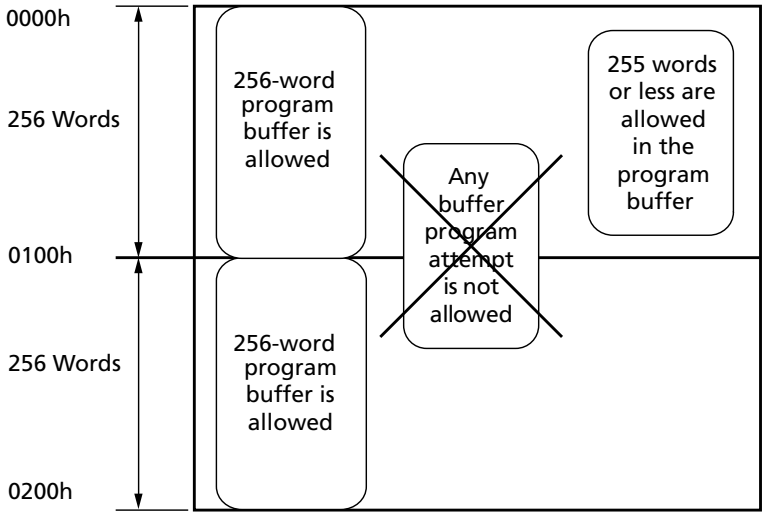

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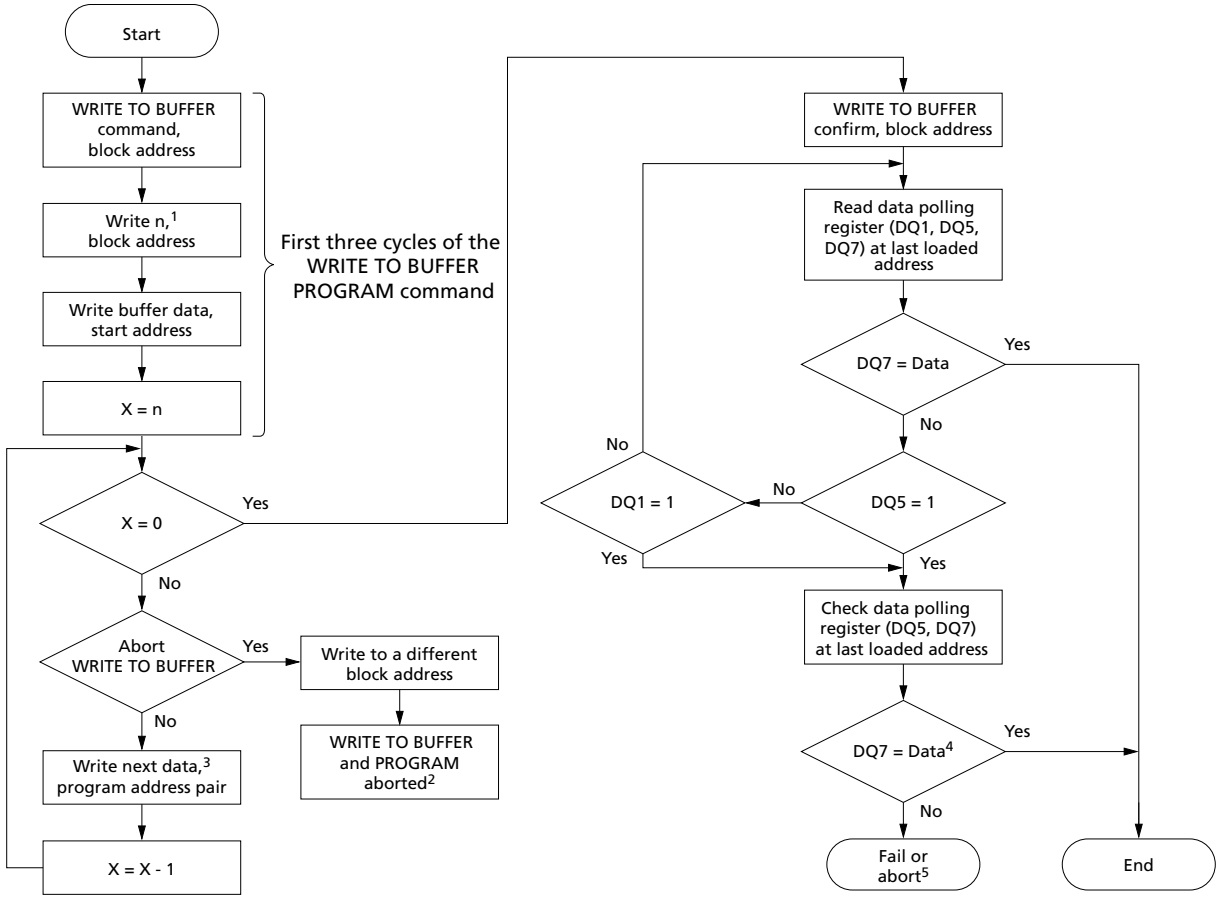
Figure 11: WRITE TO BUFFER PROGRAM Flowchart



Notes:
1. *n + 1* is the number of addresses to be programmed.
2. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode.
3. When the block address is specified, any address in the selected block address space is acceptable. However, when loading program buffer address with data, all addresses must fall within the selected program buffer page.
4. DQ7 must be checked because DQ5 and DQ7 may change simultaneously.
5. If this flowchart location is reached because DQ5 = 1, then the WRITE TO BUFFER PROGRAM command failed. If this flowchart location is reached because DQ1 = 1, then the WRITE TO BUFFER PROGRAM command aborted. In both cases, the appropriate RESET command must be issued to return the device to read mode: A RESET command if the operation failed; a WRITE TO BUFFER PROGRAM ABORT AND RESET command if the operation aborted.
6. See the Standard Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit table for details about the WRITE TO BUFFER PROGRAM command sequence.

UNLOCK BYPASS WRITE TO BUFFER PROGRAM Command

When the device is in unlock bypass mode, the UNLOCK BYPASS WRITE TO BUFFER (25h) command can be used to program the device in fast program mode. The com-

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mand requires two bus WRITE operations fewer than the standard WRITE TO BUFFER PROGRAM command.

The UNLOCK BYPASS WRITE TO BUFFER PROGRAM command behaves the same way as the WRITE TO BUFFER PROGRAM command: the operation cannot be aborted, and a bus READ operation to the memory outputs the status register.

The WRITE TO BUFFER PROGRAM CONFIRM command is used to confirm an UNLOCK BYPASS WRITE TO BUFFER PROGRAM command and to program the *n + 1* words/bytes loaded in the program buffer by this command.

ENHANCED WRITE TO BUFFER PROGRAM Command

The ENHANCED WRITE TO BUFFER PROGRAM (33h) command enables loading 256 words into the writer buffer to reduce system programming time. Each write buffer has the same A[22:8] addresses. Execution speed is identical to the 256-word WRITE TO BUFFER program speed. (See the Program/Erase Characteristics table for details.)

When issuing this command, the V_{PP}/WP# pin can be held HIGH or raised to V_{PPH} (programming acceleration).

Note: The ENHANCED WRITE TO BUFFER PROGRAM command is available only in the 128Mb x16 device,

The following successive steps are required to issue the command: Two unlock cycles begin the command, followed by a third bus write cycle that sets up the command with setup code that can be addressed to any location within the targeted block. The fourth bus write cycle loads the first address and data to be programmed. There are a total of 256 address and data loading cycles.

The command must be followed by an ENHANCED WRITE TO BUFFER PROGRAM CONFIRM command to program the buffer content, which confirm cycle ends the command.

Note that address/data cycles must be loaded in an increasing address order (A[7:0] from 00h to FFh) that includes all 256 words. Invalid address combinations or the correct sequence of bus write cycles will result in an abort.

Status register bits DQ1, DQ5, DQ6, and DQ7 enable monitoring the device status during operation. A 12V external supply can be used to improve programming efficiency. The ENHANCED WRITE TO BUFFER PROGRAM command should not be used to change a bit set to 0 back to 1. Any attempt to do so is masked during the operation. The ERASE command should be used to set memory bits from 0 to 1.

UNLOCK BYPASS ENHANCED WRITE TO BUFFER PROGRAM Command

The UNLOCK BYPASS ENHANCED WRITE TO BUFFER PROGRAM (33h)command can be used to program the memory in fast program mode. The command requires two address/data loading cycles less than the regular ENHANCED WRITE TO BUFFER PROGRAM command. This command behaves identically to the ENHANCED WRITE TO BUFFER PROGRAM command. The operation cannot be aborted and a bus READ operation to the memory outputs the status register. This command is confirmed by the ENHANCED WRITE TO BUFFER PROGRAM CONFIRM command, which programs the 256 words loaded in the buffer.

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WRITE TO BUFFER PROGRAM CONFIRM Command

The WRITE TO BUFFER PROGRAM CONFIRM (29h) command is used to confirm a WRITE TO BUFFER PROGRAM command and to program the *n + 1* words/bytes loaded in the program buffer by this command.

ENHANCED WRITE TO BUFFER PROGRAM CONFIRM Command

The ENHANCED WRITE TO BUFFER PROGRAM CONFIRM (29h) command is used to confirm an ENHANCED WRITE TO BUFFER PROGRAM command and to program the 256 words loaded in the buffer.

BUFFERED PROGRAM ABORT AND RESET Command

A BUFFERED PROGRAM ABORT AND RESET (F0h) command must be issued to reset the device to read mode when the BUFFER PROGRAM operation is aborted. The buffer programming sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the number of locations to program in the WRITE TO BUFFER PROGRAM command.
- Write to an address in a different block than the one specified during the WRITE BUFFER LOAD command.
- Write an address/data pair to a different write buffer page than the one selected by the starting address during the program buffer data loading stage of the operation.
- Write data other than the CONFIRM command after the specified number of data load cycles.

The abort condition is indicated by DQ1 = 1, DQ7 = DQ7# (for the last address location loaded), DQ6 = toggle, and DQ5 = 0 (all of which are status register bits). A BUFFERED PROGRAM ABORT and RESET command sequence must be written to reset the device for the next operation.

Note: The full three-cycle BUFFERED PROGRAM ABORT and RESET command sequence is required when using buffer programming features in unlock bypass mode.

PROGRAM SUSPEND Command

The PROGRAM SUSPEND (B0h) command can be used to interrupt a PROGRAM operation so that data can be read from any block. When the PROGRAM SUSPEND command is issued during a PROGRAM operation, the device suspends the operation within the program suspend latency time and updates the status register bits.

After the PROGRAM operation has been suspended, data can be read from any address. However, data is invalid when read from an address where a program operation has been suspended.

The PROGRAM SUSPEND command may also be issued during a PROGRAM operation while an erase is suspended. In this case, data may be read from any address not in erase suspend or program suspend mode. To read from the extended memory block area (one-time programmable area), the ENTER/EXIT EXTENDED MEMORY BLOCK command sequences must be issued.

The system may also issue the AUTO SELECT command sequence when the device is in program suspend mode. The system can read as many auto select codes as required.

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When the device exits auto select mode, the device reverts to program suspend mode and is ready for another valid operation.

The PROGRAM SUSPEND operation is aborted by performing a device reset or power-down. In this case, data integrity cannot be ensured, and it is recommended that the words or bytes that were aborted be reprogrammed.

PROGRAM RESUME Command

The PROGRAM RESUME (30h) command must be issued to exit a program suspend mode and resume a PROGRAM operation. The controller can use DQ7 or DQ6 status bits to determine the status of the PROGRAM operation. After a PROGRAM RESUME command is issued, subsequent PROGRAM RESUME commands are ignored. Another PROGRAM SUSPEND command can be issued after the device has resumed programming.

Erase Operations

CHIP ERASE Command

The CHIP ERASE (80/10h) command erases the entire chip. Six bus WRITE operations are required to issue the command and start the program/erase controller.

Protected blocks are not erased. If all blocks are protected, the data remains unchanged. No error is reported when protected blocks are not erased.

During the CHIP ERASE operation, the device ignores all other commands, including ERASE SUSPEND. It is not possible to abort the operation. All bus READ operations during CHIP ERASE output the data polling register on the data I/Os. See the Data Polling Register section for more details.

After the CHIP ERASE operation completes, the device returns to read mode, unless an error has occurred. If an error occurs, the device will continue to output the data polling register.

When the operation fails, a READ/RESET command must be issued to reset the error condition and return to read mode. The status of the array must be confirmed through the BLANK CHECK operation and the BLOCK ERASE command re-issued to the failed block.

The CHIP ERASE command sets all of the bits in unprotected blocks of the device to 1. All previous data is lost.

The operation is aborted by performing a reset or by powering down the device. In this case, data integrity cannot be ensured, and it is recommended that the entire chip be erased again.

UNLOCK BYPASS CHIP ERASE Command

When the device is in unlock bypass mode, the UNLOCK BYPASS CHIP ERASE (80/10h) command can be used to erase all memory blocks at one time. The command requires only two bus WRITE operations instead of six using the standard CHIP ERASE command. The final bus WRITE operation starts the program/erase controller.

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The UNLOCK BYPASS CHIP ERASE command behaves the same way as the CHIP ERASE command: the operation cannot be aborted, and a bus READ operation to the memory outputs the data polling register.

BLOCK ERASE Command

The BLOCK ERASE (80/30h) command erases a list of one or more blocks. It sets all bits in the selected, unprotected blocks to 1. All previous, selected, unprotected blocks data in the selected blocks is lost.

Six bus WRITE operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth bus WRITE operation using the address of the additional block. After the command sequence is written, a block erase timeout occurs.

During the period specified by the block erase timeout parameter, additional block addresses and BLOCK ERASE commands can be written. Any command except BLOCK ERASE or ERASE SUSPEND during this timeout period resets that block to the read mode. The system can monitor DQ3 to determine if the block erase timer has timed out.

After the program/erase controller has started, it is not possible to select any more blocks. Each additional block must therefore be selected within the timeout period of the last block. The timeout timer restarts when an additional block is selected. After the sixth bus WRITE operation, a bus READ operation outputs the data polling register. See the WE#-Controlled Program waveforms for details on how to identify if the program/erase controller has started the BLOCK ERASE operation.

After the BLOCK ERASE operation completes, the device returns to read mode, unless an error has occurred. If an error occurs, bus READ operations will continue to output the data polling register. A READ/RESET command must be issued to reset the error condition and return to read mode.

If any selected blocks are protected, they are ignored, and all the other selected blocks are erased. If all selected blocks are protected, the data remains unchanged. No error condition is given when protected blocks are not erased.

During the BLOCK ERASE operation, the device ignores all commands except the ERASE SUSPEND command and the READ/RESET command, which is accepted only during the timeout period. The operation is aborted by performing a hardware reset or powering down the device. In this case, data integrity cannot be ensured, and it is recommended that the aborted blocks be erased again.

UNLOCK BYPASS BLOCK ERASE Command

When the device is in unlock bypass mode, the UNLOCK BYPASS BLOCK ERASE (80/30h) command can be used to erase one or more memory blocks at a time. The command requires two bus WRITE operations instead of six using the standard BLOCK ERASE command. The final bus WRITE operation latches the address of the block and starts the program/erase controller.

To erase multiple blocks (after the first two bus WRITE operations have selected the first block in the list), each additional block in the list can be selected by repeating the second bus WRITE operation using the address of the additional block.

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Any command except BLOCK ERASE or ERASE SUSPEND during a timeout period resets that block to the read mode. The system can monitor DQ3 to determine if the block erase timer has timed out.

The UNLOCK BYPASS BLOCK ERASE command behaves the same way as the BLOCK ERASE command: the operation cannot be aborted, and a bus READ operation to the memory outputs the data polling register. See the BLOCK ERASE Command section for details.

ERASE SUSPEND Command

The ERASE SUSPEND (B0h) command temporarily suspends a BLOCK ERASE operation. One bus WRITE operation is required to issue the command. The block address is "Don't Care."

The program/erase controller suspends the ERASE operation within the erase suspend latency time of the ERASE SUSPEND command being issued. However, when the ERASE SUSPEND command is written during the block erase timeout, the device immediately terminates the timeout period and suspends the ERASE operation. After the program/erase controller has stopped, the device operates in read mode, and the erase is suspended.

During an ERASE SUSPEND operation, it is possible to execute these operations in arrays that are not suspended:

- READ (main memory array)
- PROGRAM
- WRITE TO BUFFER PROGRAM
- AUTO SELECT
- READ CFI
- UNLOCK BYPASS
- Extended memory block commands
- READ/RESET

Reading from a suspended block will output the data polling register. If an attempt is made to program in a protected or suspended block, the PROGRAM command is ignored and the data remains unchanged; also, the data polling register is not read and no error condition is given.

Before the RESUME command is initiated, the READ/RESET command must to issued to exit AUTO SELECT and READ CFI operations. In addition, the EXIT UNLOCK BYPASS and EXIT EXTENDED MEMORY BLOCK commands must be issued to exit unlock bypass and the extended memory block modes.

An ERASE SUSPEND command is ignored if it is written during a CHIP ERASE operation.

If the ERASE SUSPEND operation is aborted by performing a device hardware reset or power-down, data integrity cannot be ensured, and it is recommended that the suspended blocks be erased again.

ERASE RESUME Command

The ERASE RESUME (30h) command restarts the program/erase controller after an ERASE SUSPEND operation.

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The device must be in read array mode before the RESUME command will be accepted. An erase can be suspended and resumed more than once.

BLANK CHECK Operation

BLANK CHECK Commands

Two commands are required to execute a BLANK CHECK operation: BLANK CHECK SETUP (EB/76h) and BLANK CHECK CONFIRM AND READ (29h).

The BLANK CHECK operation determines whether a specified block is blank (that is, completely erased). It can also be used to determine whether a previous ERASE operation was successful, including ERASE operations that might have been interrupted by power loss.

The BLANK CHECK operation checks for cells that are programmed or over-erased. If it finds any, it returns a failure status, indicating that the block is not blank. If it returns a passing status, the block is guaranteed blank (all 1s) and is ready to program.

Before executing, the ERASE operation initiates an embedded BLANK CHECK operation, and if the target block is blank, the ERASE operation is skipped, benefitting overall cycle performance; otherwise, the ERASE operation continues.

The BLANK CHECK operation can occur in only one block at a time, and during its execution, reading the data polling register is the only other operation allowed. Reading from any address in the device enables reading the data polling register to monitor blank check progress or errors. Operations such as READ (array data), PROGRAM, ERASE, and any suspended operation are not allowed.

After the BLANK CHECK operation has completed, the device returns to read mode unless an error has occurred. When an error occurs, the device continues to output data polling register data. A READ/RESET command must be issued to reset the error condition and return the device to read mode.

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Block Protection Command Definitions – Address-Data Cycles

Table 19: Block Protection Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit

Notes 1 and 2 apply to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles											Notes
		1st		2nd		3rd		4th		…	nth		
		A	D	A	D	A	D	A	D		A	D	
LOCK REGISTER Commands													
ENTER LOCK REGISTER COMMAND SET (40h)	x8	AAA	AA	555	55	AAA	40						3
	x16	555	AA	2AA	55	555							
PROGRAM LOCK REGISTER (A0h)	x8	X	A0	X	Data								5
	x16												
READ LOCK REGISTER	x8	X	Data										4, 5, 6
	x16												
EXIT LOCK REGISTER (90h/00h)	x8	X	90	X	00								3
	x16												
PASSWORD PROTECTION Commands													
ENTER PASSWORD PROTECTION COMMAND SET (60h)	x8	AAA	AA	555	55	AAA	60						3
	x16	555	AA	2AA	55	555							
PROGRAM PASSWORD (A0h)	x8	X	A0	PWAn	PWDn								7
	x16												
READ PASSWORD	x8	00	PWD0	01	PWD1	02	PWD2	03	PWD3	…	07	PWD7	4, 6, 8, 9
	x16	00	PWD0	01	PWD1	02	PWD2	03	PWD3				
UNLOCK PASSWORD (25h/03h)	x8	00	25	00	03	00	PWD0	01	PWD1	…	00	29	8, 10
	x16												
EXIT PASSWORD PROTECTION (90h/00h)	x8	X	90	X	00								3
	x16												
NONVOLATILE PROTECTION Commands													
ENTER NONVOLATILE PROTECTION COMMAND SET (C0h)	x8	AAA	AA	555	55	AAA	C0						3
	x16	555	AA	2AA	55	555							
PROGRAM NONVOLATILE PROTECTION BIT (A0h)	x8	X	A0	BAd	00								11
	x16												
READ NONVOLATILE PROTECTION BIT STATUS	x8	BAd	READ (DQ0)										4, 6, 11
	x16												
CLEAR ALL NONVOLATILE PROTECTION BITS (80h/30h)	x8	X	80	00	30								12
	x16												

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Table 19: Block Protection Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit (Continued)

Notes 1 and 2 apply to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles											Notes
		1st		2nd		3rd		4th		...	nth		
		A	D	A	D	A	D	A	D		A	D	
EXIT NONVOLATILE PROTECTION (90h/00h)	x8	X	90	X	00								3
	x16												
NONVOLATILE PROTECTION BIT LOCK BIT Commands													
ENTER NONVOLATILE PROTECTION BIT LOCK BIT COMMAND SET (50h)	x8	AAA	AA	555	55	AAA	50						3
	x16	555	AA	2AA	55	555							
PROGRAM NONVOLATILE PROTECTION BIT LOCK BIT (A0h)	x8	X	A0	X	00								11
	x16												
READ NONVOLATILE PROTECTION BIT LOCK BIT STATUS	x8	X	READ (DQ0)										4, 6, 11
	x16												
EXIT NONVOLATILE PROTECTION BIT LOCK BIT (90h/00h)	x8	X	90	X	00								3
	x16												
VOLATILE PROTECTION Commands													
ENTER VOLATILE PROTECTION COMMAND SET (E0h)	x8	AAA	AA	555	55	AAA	E0						3
	x16	555	AA	2AA	55	555							
PROGRAM VOLATILE PROTECTION BIT (A0h)	x8	X	A0	BAd	00								11
	x16												
READ VOLATILE PROTECTION BIT STATUS	x8	BAd	READ (DQ0)										4, 6
	x16												
CLEAR VOLATILE PROTECTION BIT (A0h)	x8	X	A0	BAd	01								11
	x16												
EXIT VOLATILE PROTECTION (90h/00h)	x8	X	90	X	00								3
	x16												
EXTENDED MEMORY BLOCK Operations													
ENTER EXTENDED MEMORY BLOCK (88h)	x8	AAA	AA	555	55	AAA	88						
	x16	555		2AA		555							
PROGRAM EXTENDED MEMORY BLOCK (A0h)	x8	AAA	AA	555	55	AAA	A0	Word address	data				
	x16	555		2AA		555							
READ EXTENDED MEMORY BLOCK	x8	Word address	data										
	x16												

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Table 19: Block Protection Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit (Continued)

Notes 1 and 2 apply to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles											Notes
		1st		2nd		3rd		4th		…	*n*th		
		A	D	A	D	A	D	A	D		A	D	
EXIT EXTENDED MEMORY BLOCK (90h/00h)	x8	AAA	AA	555	55	555	90	X	00				
	x16	555		2AA									

Notes:
1. Key: A = Address and D = Data; X = "Don't Care;" BAd = Any address in the block; PWDn = Password bytes, n = 0 to 7 (×8)/words 0 to 3 (×16); PWAn = Password address, n = 0 to 7 (×8)/0 to 3 (×16); PWDn = Password words, n = 0 to 3 (×16); PWAn = Password address, n = 0 to 3(×16);Gray = Not applicable. All values in the table are hexadecimal.
2. DQ[15:8] are "Don't Care" during UNLOCK and COMMAND cycles. A[MAX:16] are "Don't Care" during UNLOCK and COMMAND cycles, unless an address is required.
3. The ENTER command sequence must be issued prior to any operation. It disables READ and WRITE operations from and to block 0. READ and WRITE operations from and to any other block are allowed. Also, when an ENTER COMMAND SET command is issued, an EXIT COMMAND SET command must be issued to return the device to READ mode.
4. READ REGISTER/PASSWORD commands have no command code; CE# and OE# are driven LOW and data is read according to a specified address.
5. Data = Lock register content.
6. All address cycles shown for this command are READ cycles.
7. Only one portion of the password can be programmed or read by each PROGRAM PASSWORD command.
8. Each portion of the password can be entered or read in any order as long as the entire 64-bit password is entered or read.
9. For the x8 READ PASSWORD command, the *n*th (and final) address cycle equals the 8th address cycle. From the 5th to the 8th address cycle, the values for each address and data pair continue the pattern shown in the table as follows: for x8, address and data = 04 and PWD4; 05 and PWD5; 06 and PWD6; 07 and PWD7.
10. For the x8 UNLOCK PASSWORD command, the *n*th (and final) address cycle equals the 11th address cycle. From the 5th to the 10th address cycle, the values for each address and data pair continue the pattern shown in the table as follows: address and data = 02 and PWD2; 03 and PWD3; 04 and PWD4; 05 and PWD5; 06 and PWD6; 07 and PWD7.

    For the x16 UNLOCK PASSWORD command, the *n*th (and final) address cycle equals the 7th address cycle. For the 5th and 6th address cycles, the values for the address and data pair continue the pattern shown in the table as follows: address and data = 02 and PWD2; 03 and PWD3.
11. Both nonvolatile and volatile protection bit settings are as follows: Protected state = 00; Unprotected state = 01.
12. The CLEAR ALL NONVOLATILE PROTECTION BITS command programs all nonvolatile protection bits before erasure. This prevents over-erasure of previously cleared nonvolatile protection bits.

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Protection Operations

Blocks can be protected individually against accidental PROGRAM, ERASE, or READ operations on both 8-bit and 16-bit configurations. The block protection scheme is shown in the Software Protection Scheme figure.

Memory block and extended memory block protection is configured through the lock register. (See Lock Register section.)

LOCK REGISTER Commands

After the ENTER LOCK REGISTER COMMAND SET (40h) command has been issued, all bus READ or PROGRAM operations can be issued to the lock register.

The PROGRAM LOCK REGISTER (A0h) command allows the lock register to be configured. The programmed data can then be checked with a READ LOCK REGISTER command by driving CE# and OE# LOW with the appropriate address data on the address bus.

PASSWORD PROTECTION Commands

After the ENTER PASSWORD PROTECTION COMMAND SET (60h) command has been issued, the commands related to password protection mode can be issued to the device.

The PROGRAM PASSWORD (A0h) command is used to program the 64-bit password used in the password protection mode. To program the 64-bit password, the complete command sequence must be entered eight times at eight consecutive addresses selected by A[1:0] plus DQ15/A-1 in 8-bit mode, or four times at four consecutive addresses selected by A[1:0] in 16-bit mode. By default, all password bits are set to 1. The password can be checked by issuing a READ PASSWORD command.

The READ PASSWORD command is used to verify the password used in password protection mode. To verify the 64-bit password, the complete command sequence must be entered eight times at eight consecutive addresses selected by A[1:0] plus DQ15/A-1 in 8-bit mode, or four times at four consecutive addresses selected by A[1:0] in 16-bit mode. If the password mode lock bit is programmed and the user attempts to read the password, the device will output FFh onto the I/O data bus.

The UNLOCK PASSWORD (25/03h) command is used to clear the nonvolatile protection bit lock bit, allowing the nonvolatile protection bits to be modified. The UNLOCK PASSWORD command must be issued, along with the correct password, and requires a 1µs delay between successive UNLOCK PASSWORD commands in order to prevent hackers from cracking the password by trying all possible 64-bit combinations. If this delay does not occur, the latest command will be ignored. Approximately 1µs is required for unlocking the device after the valid 64-bit password has been provided.

NONVOLATILE PROTECTION Commands

After the ENTER NONVOLATILE PROTECTION COMMAND SET (C0h) command has been issued, the commands related to nonvolatile protection mode can be issued to the device.

A block can be protected from program or erase by issuing a PROGRAM NONVOLATILE PROTECTION BIT (A0h) command, along with the block address. This command sets the nonvolatile protection bit to 0 for a given block.

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The status of a nonvolatile protection bit for a given block or group of blocks can be read by issuing a READ NONVOLATILE MODIFY PROTECTION BIT command, along with the block address.

The nonvolatile protection bits are erased simultaneously by issuing a CLEAR ALL NONVOLATILE PROTECTION BITS (80/30h) command. No specific block address is required. If the nonvolatile protection bit lock bit is set to 0, the command fails.

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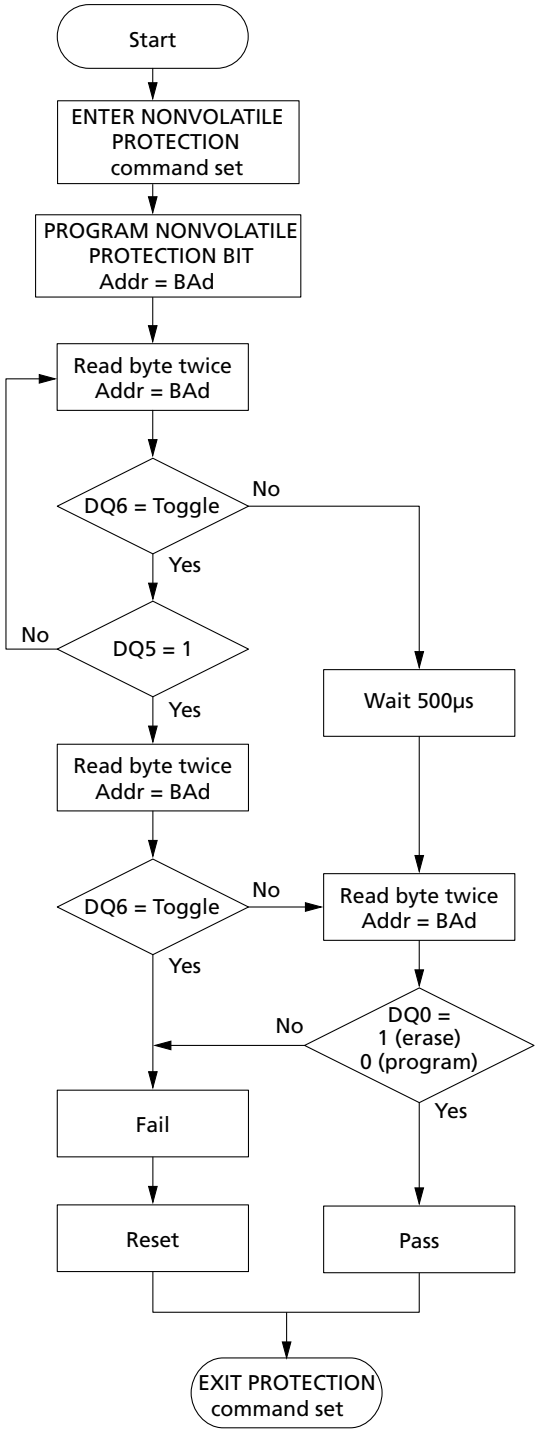
Figure 12: Program/Erase Nonvolatile Protection Bit Algorithm



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NONVOLATILE PROTECTION BIT LOCK BIT Commands

After the ENTER NONVOLATILE PROTECTION BIT LOCK BIT COMMAND SET (50h) command has been issued, the commands that allow the nonvolatile protection bit lock bit to be set can be issued to the device.

The PROGRAM NONVOLATILE PROTECTION BIT LOCK BIT (A0h) command is used to set the nonvolatile protection bit lock bit to 0, thus locking the nonvolatile protection bits and preventing them from being modified.

The READ NONVOLATILE PROTECTION BIT LOCK BIT STATUS command is used to read the status of the nonvolatile protection bit lock bit.

VOLATILE PROTECTION Commands

After the ENTER VOLATILE PROTECTION COMMAND SET (E0h) command has been issued, commands related to the volatile protection mode can be issued to the device.

The PROGRAM VOLATILE PROTECTION BIT (A0h) command individually sets a volatile protection bit to 0 for a given block. If the nonvolatile protection bit for the same block is set, the block is locked regardless of the value of the volatile protection bit. (See the Block Protection Status table.)

The status of a volatile protection bit for a given block can be read by issuing a READ VOLATILE PROTECTION BIT STATUS command along with the block address.

The CLEAR VOLATILE PROTECTION BIT (A0h) command individually clears (sets to 1) the volatile protection bit for a given block. If the nonvolatile protection bit for the same block is set, the block is locked regardless of the value of the volatile protection bit. (See the Block Protection Status table.)

EXTENDED MEMORY BLOCK Commands

The device has one extra 128-word extended memory block that can be accessed only by the ENTER EXTENDED MEMORY BLOCK (88h) command. The extended memory block is 128 words (x16) or 256 bytes (x8). It is used as a security block to provide a permanent 128-bit security identification number or to store additional information. The device can be shipped with the extended memory block prelocked permanently by Micron, including the 128-bit security identification number. Or, the device can be shipped with the extended memory block unlocked, enabling customers to permanently program and lock it. (See Lock Register, the AUTO SELECT command, and the Block Protection table.)

Table 20: Extended Memory Block Address and Data

Address			Data	
x8	x16	Micron prelocked	Customer Lockable	
000000h–00000Fh	000000h–000007h	Secure ID number	Determined by customer	Secure ID number
000010h–0000FFh	000008h–00007Fh	Protected and unavailable		Determined by customer

After the ENTER EXTENDED MEMORY BLOCK command has been issued, the device enters the extended memory block mode. All bus READ or PROGRAM operations are conducted on the extended memory block, and the extended memory block is ad-

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dressed using the addresses occupied by block 0 in the other operating modes. (See the Memory Map table.)

In extended memory block mode, ERASE, CHIP ERASE, ERASE SUSPEND, and ERASE RESUME commands are not allowed. The extended memory block cannot be erased, and each bit of the extended memory block can only be programmed once.

The extended memory block is protected from further modification by programming lock register bit 0. Once invoked, this protection cannot be undone.

The device remains in extended memory block mode until the EXIT EXTENDED MEMORY BLOCK (90/00h) command is issued, which returns the device to read mode, or until power is removed from the device. After a power-up sequence or hardware reset, the device will revert to reading memory blocks in the main array.

EXIT PROTECTION Command

The EXIT PROTECTION COMMAND SET (90/00h) command is used to exit the lock register, password protection, nonvolatile protection, volatile protection, and nonvolatile protection bit lock bit command set modes and return the device to read mode.

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Device Protection

Hardware Protection

The V_{PP}/WP# function provides a hardware method of protecting either the highest/lowest block or the top/bottom two blocks. When V_{PP}/WP# is LOW, PROGRAM and ERASE operations on either of these block options is ignored to provide protection. When V_{PP}/WP# is HIGH, the device reverts to the previous protection status for the highest/lowest block or top/bottom two blocks. PROGRAM and ERASE operations can modify the data in either of these block options unless block protection is enabled.

Note: Micron highly recommends driving V_{PP}/WP# HIGH or LOW. If a system needs to float the V_{PP}/WP# pin, without a pull-up/pull-down resistor and no capacitor, then an internal pull-up resistor is enabled.

Table 21: V_{PP}/WP# Functions

V_{PP}/WP# Settings	Function
V_{IL}	Highest/lowest block or the top/bottom two blocks are protected.
V_{IH}	Highest/lowest block or the top/bottom two blocks are unprotected unless software protection is activated.

Software Protection

The following software protection modes are available:

- Volatile protection
- Nonvolatile protection
- Password protection
- Password access

The device is shipped with all blocks unprotected. On first use, the device defaults to the nonvolatile protection mode but can be activated in either the nonvolatile protection or password protection mode.

The desired protection mode is activated by setting either the nonvolatile protection mode lock bit or the password protection mode lock bit of the lock register. (See the Lock Register section.) Both bits are one-time-programmable and nonvolatile; therefore, after the protection mode has been activated, it cannot be changed, and the device is set permanently to operate in the selected protection mode. It is recommended that the desired software protection mode be activated when first programming the device.

For the lowest and highest blocks or for the top/bottom two blocks, a higher level of block protection can be achieved by locking the blocks using nonvolatile protection mode and holding V_{PP} /WP# LOW.

Blocks with volatile protection and nonvolatile protection can coexist within the memory array. If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode.

The block protection status can be read by performing a read electronic signature or by issuing an AUTO SELECT command. (See the Block Protection table.)

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Refer to the Block Protection Status table and the Software Protection Scheme figure for details on the block protection scheme. Refer to the Protection Operations section for a description of the command sets.

Volatile Protection Mode

Volatile protection enables the software application to protect blocks against inadvertent change and can be disabled when changes are needed. Volatile protection bits are unique for each block and can be individually modified. Volatile protection bits control the protection scheme only for unprotected blocks whose nonvolatile protection bits are cleared to 1. Issuing a PROGRAM VOLATILE PROTECTION BIT or CLEAR VOLATILE PROTECTION BIT command sets to 0 or clears to 1 the volatile protection bits and places the associated blocks in the protected (0) or unprotected (1) state, respectively. The volatile protection bit can be set or cleared as often as needed.

When the device is first shipped, or after a power-up or hardware reset, the volatile protection bits default to 1 (unprotected).

Nonvolatile Protection Mode

A nonvolatile protection bit is assigned to each block. Each of these bits can be set for protection individually by issuing a PROGRAM NONVOLATILE PROTECTION BIT command. Also, each device has one global volatile bit called the nonvolatile protection bit lock bit; it can be set to protect all nonvolatile protection bits at once. This global bit must be set to 0 only after all nonvolatile protection bits are configured to the desired settings. When set to 0, the nonvolatile protection bit lock bit prevents changes to the state of the nonvolatile protection bits. When cleared to 1, the nonvolatile protection bits can be set and cleared using the PROGRAM NONVOLATILE PROTECTION BIT and CLEAR ALL NONVOLATILE PROTECTION BITS commands, respectively.

No software command unlocks the nonvolatile protection bit lock bit unless the device is in password protection mode; in nonvolatile protection mode, the nonvolatile protection bit lock bit can be cleared only by taking the device through a hardware reset or power-up.

Nonvolatile protection bits cannot be cleared individually; they must be cleared all at once using a CLEAR ALL NONVOLATILE PROTECTION BITS command. They will remain set through a hardware reset or a power-down/power-up sequence.

If one of the nonvolatile protection bits needs to be cleared (unprotected), additional steps are required: First, the nonvolatile protection bit lock bit must be cleared to 1, using either a power-cycle or hardware reset. Then, the nonvolatile protection bits can be changed to reflect the desired settings. Finally, the nonvolatile protection bit lock bit must be set to 0 to lock the nonvolatile protection bits. The device now will operate normally.

To achieve the best protection, the PROGRAM NONVOLATILE PROTECTION LOCK BIT command should be executed early in the boot code, and the boot code should be protected by holding V_{PP}/WP# LOW.

Nonvolatile protection bits and volatile protection bits have the same function when V_{PP}/WP# is HIGH or when V_{PP}/WP# is at the voltage for program acceleration (V_{PPH}).

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Password Protection Mode

The password protection mode provides a higher level of security than the nonvolatile protection mode by requiring a 64-bit password to unlock the nonvolatile protection bit lock bit. In addition to this password requirement, the nonvolatile protection bit lock bit is set to 0 after power-up and reset to maintain the device in password protection mode.

Executing the UNLOCK PASSWORD command by entering the correct password clears the nonvolatile protection bit lock bit, enabling the block nonvolatile protection bits to be modified. If the password provided is incorrect, the nonvolatile protection bit lock bit remains locked, and the state of the nonvolatile protection bits cannot be modified.

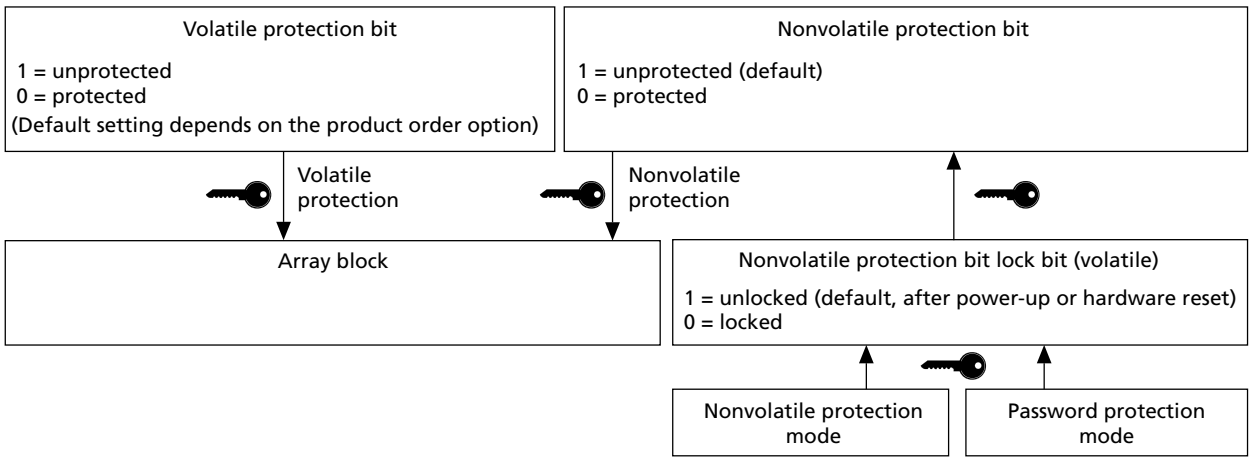
To place the device in password protection mode, the following two steps are required: First, before activating the password protection mode, a 64-bit password must be set and the setting verified. Password verification is allowed only before the password protection mode is activated. Next, password protection mode is activated by programming the password protection mode lock bit to 0. This operation is irreversible. After the bit is programmed, it cannot be erased, the device remains permanently in password protection mode, and the 64-bit password can be neither retrieved nor reprogrammed. In addition, all commands to the address where the password is stored are disabled.

Note: There is no means to verify the password after password protection mode is enabled. If the password is lost after enabling the password protection mode, there is no way to clear the nonvolatile protection bit lock bit.

Password Access

Password access is a security enhancement that protects information stored in the main array blocks by preventing content alteration or reads until a valid 64-bit password is received. Password access may be combined with nonvolatile and/or volatile protection to create a multi-tiered solution. Contact your Micron sales representative for further details.

Figure 13: Software Protection Scheme



Notes: 1. Volatile protection bits are programmed and cleared individually. Nonvolatile protection bits are programmed individually and cleared collectively.

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2. Once programmed to 0, the nonvolatile protection bit lock bit can be reset to 1 only by taking the device through a power-up or hardware reset.

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Common Flash Interface

The common Flash interface (CFI) is a JEDEC-approved, standardized data structure that can be read from the Flash memory device. It allows a system's software to query the device to determine various electrical and timing parameters, density information, and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the READ CFI QUERY command is issued, the device enters CFI query mode and the data structure is read from memory. The following tables show the addresses (A-1, A[7:0]) used to retrieve the data. The query data is always presented on the lowest order data outputs (DQ[7:0]), and the other data outputs (DQ[15:8]) are set to 0.

Table 22: Query Structure Overview

Note 1 applies to the entire table

Address		Subsection Name	Description
x16	x8		
10h	20h	CFI query identification string	Command set ID and algorithm data offset
1Bh	36h	System interface information	Device timing and voltage information
27h	4Eh	Device geometry definition	Flash device layout
40h	80h	Primary algorithm-specific extended query table	Additional information specific to the primary algorithm (optional)

Note: 1. Query data are always presented on the lowest order data outputs (DQ[7:0]). DQ[15:8] are set to 0.

Table 23: CFI Query Identification String

Note 1 applies to the entire table

Address		Data	Description	Value
x16	x8			
10h	20h	0051h	Query unique ASCII string "QRY"	"Q"
11h	22h	0052h		"R"
12h	24h	0059h		"Y"
13h 14h	26h 28h	0002h 0000h	Primary algorithm command set and control interface ID code 16-bit ID code defining a specific algorithm	–
15h 16h	2Ah 2Ch	0040h 0000h	Address for primary algorithm extended query table (see the Primary Algorithm-Specific Extended Query Table)	P = 40h
17h 18h	2Eh 30h	0000h 0000h	Alternate vendor command set and control Interface ID code second vendor-specified algorithm supported	–
19h 1Ah	32h 34h	0000h 0000h	Address for alternate algorithm extended query table	–

Note: 1. Query data are always presented on the lowest order data outputs (DQ[7:0]). DQ[15:8] are set to 0.

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Table 24: CFI Query System Interface Information

Note 1 applies to the entire table

Address		Data	Description	Value
x16	x8			
1Bh	36h	0027h	V_{CC} logic supply minimum program/erase voltage Bits[7:4] BCD value in volts Bits[3:0] BCD value in 100mV	2.7V
1Ch	38h	0036h	V_{CC} logic supply maximum program/erase voltage Bits[7:4] BCD value in volts Bits[3:0] BCD value in 100mV	3.6V
1Dh	3Ah	00B5h	V_{PPH} (programming) supply minimum program/erase voltage Bits[7:4] hex value in volts Bits[3:0] BCD value in 100mV	11.5V
1Eh	3Ch	00C5h	V_{PPH} (programming) supply maximum program/erase voltage Bits[7:4] hex value in volts Bits[3:0] BCD value in 100mV	12.5V
1Fh	3Eh	0004h	Typical timeout for single byte/word program = 2^nµs	16µs
20h	40h	0009h	Typical timeout for maximum size buffer program = 2^nµs	512µs
21h	42h	0009h	Typical timeout per individual block erase = 2^nms	0.5s
22h	44h	000Fh	Typical timeout for full chip erase = 2^nms	32Mb: 33s
		0010h		64Mb: 66s
		0011h		128Mb: 131s
23h	46h	0004h	Maximum timeout for byte/word program = 2^n times typical	256µs
24h	48h	0002h	Maximum timeout for buffer program = 2^n times typical	2048µs
25h	4Ah	0003h	Maximum timeout per individual block erase = 2^n times typical	4s
26h	4Ch	0002h	Maximum timeout for chip erase = 2^n times typical	32Mb: 131s
		0002h		64Mb: 262s
		0002h		128Mb: 524s

Note: 1. The values in this table are valid for all packages.

Table 25: Device Geometry Definition

Address		Data	Description	Value
x16	x8			
27h	4Eh	0016h	Device size = 2^n in number of bytes	4MB
		0017h		8MB
		0018h		16MB
28h 29h	50h 52h	0002h 0000h	Flash device interface code description	x8, x16 asynchro-nous
2Ah 2Bh	54h 56h	0008h[1] 0000h	Maximum number of bytes in multi-byte program or page = 2^n	256

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Table 25: Device Geometry Definition (Continued)

Address		Data	Description	Value
x16	x8			
2Ch	58h	(See table below)	Number of erase block regions. It specifies the number of regions containing contiguous erase blocks of the same size. 01h = Uniform device 02h = Boot device	–
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	(See table below)	Erase block region 1 information Bits[15:0] = y, y + 1 = Number of identical-size erase blocks Bits[31:16] = z, block size in region 1 is z x 256 bytes	–
31h 32h 33h 34h	62h 64h 66h 68h	(See table below)	Erase block region 2 information Bits[15:0] = y, y + 1 = Number of identical-size erase blocks Bits[31:16] = z, block size in region 1 is z x 256 bytes	–
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase block region 3 information	0
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase block region 4 information	0

Note: 1. The value at 2Ah in the CFI region is set to 08h (256 bytes) due to compatibility issues. The maximum 256-word program buffer can be used to optimize system program performance.

Table 26: Erase Block Region Information

Address	32Mb			64Mb			128Mb
	Top	Bottom	Uniform	Top	Bottom	Uniform	Uniform
2Ch	02h	02h	01h	02h	02h	01h	01h
2Dh	07h	07h	3Fh	07h	07h	7Fh	7Fh
2Eh	00h	00h	00h	00h	00h	00h	00h
2Fh	20h	20h	00h	20h	20h	00h	00h
30h	00h	00h	01h	00h	00h	01h	02h
31h	3Eh	3Eh	00h	7Eh	7Eh	00h	00h
32h	00h	00h	00h	00h	00h	00h	00h
33h	00h	00h	00h	00h	00h	00h	00h
34h	01h	01h	00h	01h	01h	00h	00h

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Table 27: Primary Algorithm-Specific Extended Query Table

Note 1 applies to the entire table

Address		Data	Description	Value
x16	x8			
40h	80h	0050h	Primary algorithm extended query table unique ASCII string “PRI”	"P"
41h	82h	0052h		"R"
42h	84h	0049h		"I"
43h	86h	0031h	Major version number, ASCII	"1"
44h	88h	0033h	Minor version number, ASCII	"3"
45h	8Ah	0018h	Address sensitive unlock (bits[1:0]): 00 = Required 01 = Not required Silicon revision number (bits[7:2])	Required
46h	8Ch	0002h	Erase suspend: 00 = Not supported 01 = Read only 02 = Read and write	2
47h	8Eh	0001h	Block protection: 00 = Not supported x = Number of blocks per group	1
48h	90h	0000h	Temporary block unprotect: 00 = Not supported 01 = Supported	Not supported
49h	92h	0008h	Block protect/unprotect: 08 = M29EWH/M29EWL	8
4Ah	94h	0000h	Simultaneous operations: Not supported	n/a
4Bh	96h	0000h	Burst mode: 00 = Not supported 01 = Supported	Not supported
4Ch	98h	0002h	Page mode: 00 = Not supported 01 = 8-word page 02 = 8-word page 03 = 16-word page	8-word page
4Dh	9Ah	00B5h	V_{PPH} supply minimum program/erase voltage: Bits[7:4] hex value in volts Bits[3:0] BCD value in 100mV	11.5V
4Eh	9Ch	00C5h	V_{PPH} supply maximum program/erase voltage: Bits[7:4] hex value in volts Bits[3:0] BCD value in 100mV	12.5V

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Table 27: Primary Algorithm-Specific Extended Query Table (Continued)

Note 1 applies to the entire table

Address		Data	Description	Value
x16	x8			
4Fh	9Eh	00xxh	Top/bottom boot block flag: xx = 02h: Bottom boot device, HW protection for bottom two blocks xx = 03h: Top boot device, HW protection for top two blocks xx = 04h: Uniform device, HW protection for lowest block xx = 05h: Uniform device, HW protection for highest block	Device type (bottom boot, top boot, uniform)
50h	A0h	0001h	Program suspend: 00 = Not supported 01 = supported	Supported

Note: 1. The values in this table are valid for both packages.

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Power-Up and Reset Characteristics

Table 28: Power-Up Specifications

Parameter	Symbol		Min	Unit	Notes
	Legacy	JEDEC			
V_{CC} HIGH to V_{CCQ} HIGH	–	^{t}VCHVCQH	0	µs	1
V_{CC} HIGH to rising edge of RST#	^{t}VCS	^{t}VCHPH	60	µs	2
V_{CCQ} HIGH to rising edge of RST#	^{t}VIOS	^{t}VCQHPH	0	µs	2
RST# HIGH to chip enable LOW	^{t}RH	^{t}PHEL	50	ns	
RST# HIGH to write enable LOW	–	^{t}PHWL	150	ns	

Notes:
1. V_{CC} and V_{CCQ} ramps must be synchronized during power-up.
2. If RST# is not stable for ^{t}VCS or ^{t}VIOS, the device will not allow any READ or WRITE operations, and a hardware reset is required.

Figure 14: Power-Up Timing

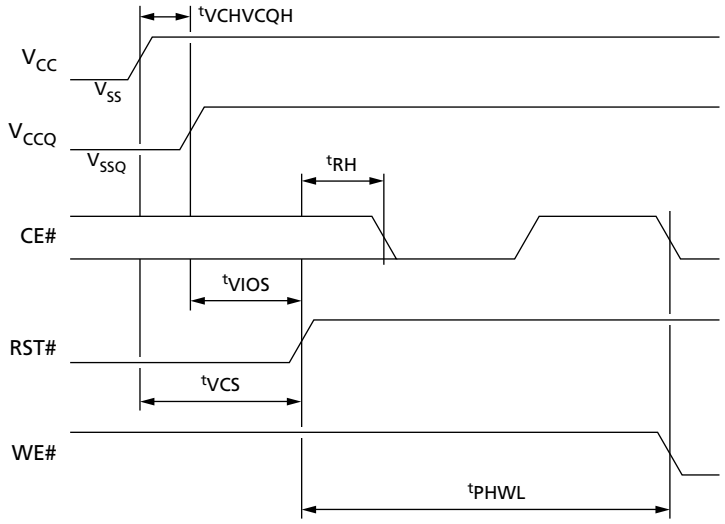

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Table 29: Reset AC Specifications

Condition/Parameter	Symbol		Min	Max	Unit	Notes
	Legacy	JEDEC				
RST# LOW to read mode during program or erase	^{t}READY	^{t}PLRH	–	25	µs	1
RST# pulse width	^{t}RP	^{t}PLPH	100	–	ns	
RST# HIGH to CE# LOW, OE# LOW	^{t}RH	^{t}PHEL, ^{t}PHGL	50	–	ns	1
RST# LOW to standby mode during read mode	^{t}RPD	–	10	–	µs	
RST# LOW to standby mode during program or erase			50	–	µs	
RY/BY# HIGH to CE# LOW, OE# LOW	^{t}RB	^{t}RHEL, ^{t}RHGL	0	–	ns	1

Note: 1. Sampled only; not 100% tested.

Figure 15: Reset AC Timing – No PROGRAM/ERASE Operation in Progress

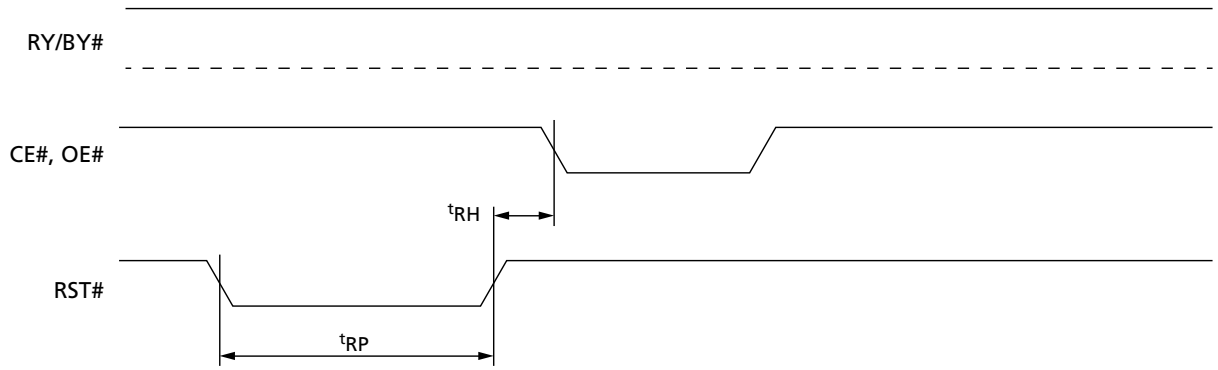
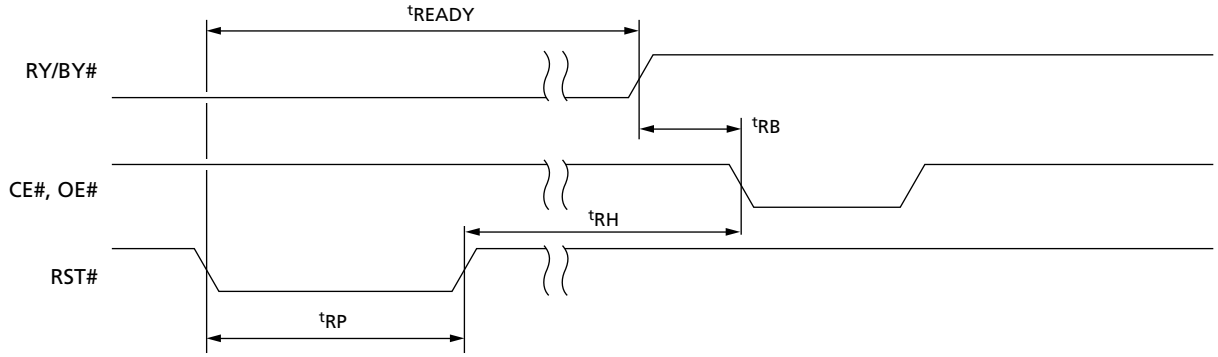


Figure 16: Reset AC Timing During PROGRAM/ERASE Operation



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Absolute Ratings and Operating Conditions

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 30: Absolute Maximum/Minimum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Temperature under bias	T_{BIAS}	–40	85	°C	
Storage temperature	T_{STG}	–65	125	°C	
Input/output voltage	V_{IO}	–0.6	V_{CC} + 0.6	V	1, 2
Supply voltage	V_{CC}	–2	5.6	V	1, 2
Input/output supply voltage	V_{CCQ}	–2	5.6	V	1, 2
Program voltage	V_{PPH}	–2	14.5	V	1, 2, 3

Notes:
1. During signal transitions, minimum voltage may undershoot to –2V during periods less than 20ns.
2. During signal transitions, maximum voltage may overshoot to V_{CC} + 2V for periods less than 20ns.
3. V_{PPH} must not remain at 12V for more than 80 hours cumulative.

Table 31: Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{CC}	2.7	3.6	V
Input/output supply voltage ($V_{CCQ} \le V_{CC}$)	V_{CCQ}	1.65	3.6	V
Program voltage	V_{PP}	–0.6	12.5	V
Ambient operating temperature	T_A	–40	85	°C
Load capacitance	C_L	30		pF
Input rise and fall times	–	–	2.5	ns
Input pulse voltages	–	0 to V_{CCQ}		V
Input and output timing reference voltages	–	$V_{CCQ}/2$		V

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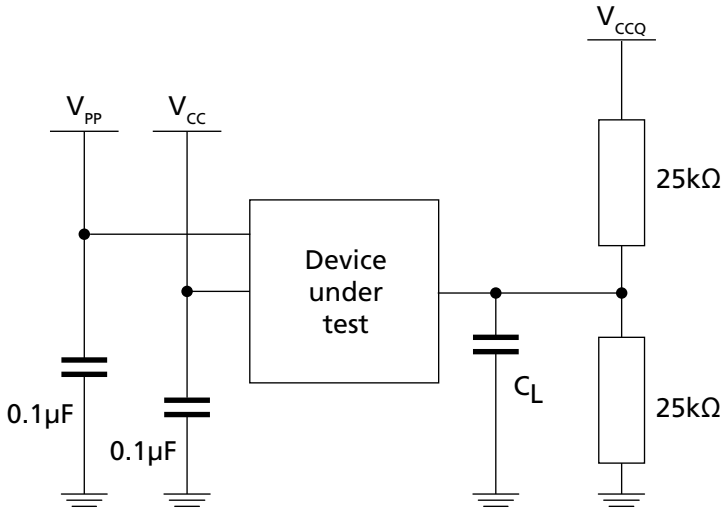
Figure 17: AC Measurement Load Circuit



Note: 1. C_L includes jig capacitance.

Figure 18: AC Measurement I/O Waveform

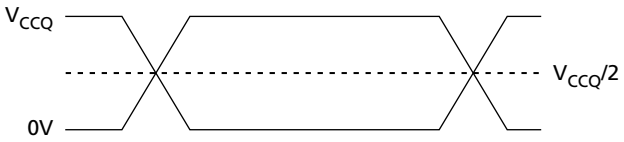


Table 32: Input/Output Capacitance

Parameter	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	2	7	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V	2	5	pF

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DC Characteristics

Table 33: DC Current Characteristics

Parameter		Symbol	Conditions		Min	Typ	Max	Unit	Notes
Input leakage current		I_{LI}	$0V \le V_{IN} \le V_{CC}$		–	–	±1	µA	1
Output leakage current		I_{LO}	$0V \le V_{OUT} \le V_{CC}$		–	–	±1	µA	
V_{CC} read current	Random read	I_{CC1}	CE# = V_{IL}, OE# = V_{IH}, *f* = 5 MHz		–	20	25	mA	
	Page read		CE# = V_{IL}, OE# = V_{IH}, *f* = 13 MHz		–	12	16	mA	
V_{CC} standby current	128Mb	I_{CC2}	CE# = V_{CCQ} ±0.2V, RST# = V_{CCQ} ±0.2V		–	50	120	µA	
	64Mb				–	35	120	µA	
	32Mb				–	35	120	µA	
V_{CC} program/erase/blank check current		I_{CC3}	Program/ erase controller active	V_{PP}/WP# = V_{IL} or V_{IH}	–	35	50	mA	2
				V_{PP}/WP# = V_{PPH}	–	26	33	mA	
V_{PP} current	Read	I_{PP1}	V_{PP}/WP# ≤ V_{CC}		–	2	15	µA	
	Standby				–	0.2	5	µA	
	Reset	I_{PP2}	RST# = V_{SS} ±0.2V		–	0.2	5	µA	
	PROGRAM operation ongoing	I_{PP3}	V_{PP}/WP# = 12V ±5%		–	5	10	mA	
			V_{PP}/WP# = V_{CC}		–	0.05	0.10	mA	
	ERASE operation ongoing	I_{PP4}	V_{PP}/WP# = 12V ±5%		–	5	10	mA	
			V_{PP}/WP# = V_{CC}		–	0.05	0.10	mA	

Notes:
1. The maximum input leakage current is ±5µA on the V_{PP}/WP# pin.
2. Sampled only; not 100% tested.

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Table 34: DC Voltage Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Notes
Input LOW voltage	V_{IL}	$V_{CC} \geq 2.7V$	–0.5	–	0.8	V	
Input HIGH voltage	V_{IH}	$V_{CC} \geq 2.7V$	V_{CCQ}–0.4	–	V_{CCQ}+0.5	V	1
Output LOW voltage	V_{OL}	I_{OL} = 100µA, $V_{CC} = V_{CC,min}$, $V_{CCQ} = V_{CCQ,min}$	–	–	0.2	V	
Output HIGH voltage	V_{OH}	I_{OH} = 100µA, $V_{CC} = V_{CC,min}$, $V_{CCQ} = V_{CCQ,min}$	V_{CCQ} - 0.2	–	–	V	
Voltage for V_{PP}/WP# program acceleration	V_{PPH}	–	11.5	–	12.5	V	
V_{PP} logic level	V_{PPL}		2.7	–	3.6	V	
Program/erase lockout supply voltage	V_{LKO}	–	2.3	–	–	V	2

Notes:
1. If V_{CCQ} range is 2.7v~3.6v, V_{IH} Min is 2v.
2. Sampled only; not 100% tested.

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Read AC Characteristics

Table 35: Read AC Characteristics

Parameter	Symbol		Condition	Package	Min	Max	Unit	Notes
	Legacy	JEDEC						
Address valid to next address valid	tRC	tAVAV	$V_{CCQ} \geq 2.7V$, CE# = V_{IL}, OE# = V_{IL}	BGA	60	–	ns	
				TSOP	70	–	ns	
			$V_{CCQ} < 2.7V$, CE# = V_{IL}, OE# = V_{IL}	BGA	65	–	ns	
				TSOP	75	–	ns	
Address valid to output valid	tACC	tAVQV	$V_{CCQ} \geq 2.7V$, CE# = V_{IL}, OE# = V_{IL}	BGA	–	60	ns	
				TSOP	–	70	ns	
			$V_{CCQ} < 2.7V$, CE# = V_{IL}, OE# = V_{IL}	BGA	-	65	ns	
				TSOP	-	75	ns	
Address valid to output valid (page)	tPAGE	tAVQV1	CE# = V_{IL}, OE# = V_{IL}	BGA	–	25	ns	
				TSOP	–	25	ns	
CE# LOW to output transition	tLZ	tELQX	OE# = V_{IL}	BGA	0	–	ns	1
				TSOP	0	–	ns	1
CE# LOW to output valid	tE	tELQV	$V_{CCQ} \geq 2.7V$, OE# = V_{IL}	BGA	–	60	ns	
				TSOP	–	70	ns	
			$V_{CCQ} < 2.7V$, OE# = V_{IL}	BGA	-	65	ns	
				TSOP	-	75	ns	
OE# LOW to output transition	tOLZ	tGLQX	CE# = V_{IL}	BGA	0	–	ns	1
				TSOP	0	–	ns	1
OE# LOW to output valid	tOE	tGLQV	CE# = V_{IL}	BGA	–	25	ns	
				TSOP	–	25	ns	
CE# HIGH to output High-Z	tHZ	tEHQZ	OE# = V_{IL}	BGA	–	20	ns	1
				TSOP	–	20	ns	1
OE# HIGH to output High-Z	tDF	tGHQZ	CE# = V_{IL}	BGA	–	15	ns	1
				TSOP	–	15	ns	1
CE#, OE#, or address transition to output transition	tOH	tEHQX, tGHQX, tAXQX	–	BGA	0	–	ns	
				TSOP	0	–	ns	
CE# to BYTE# LOW	tELFL	tELBL	–	BGA	–	10	ns	
				TSOP	–	10	ns	
CE# to BYTE# HIGH	tELFH	tELBH	–	BGA	–	10	ns	
				TSOP	–	10	ns	
BYTE# LOW to output valid	tFLQV	tBLQV	–	BGA	–	1	µs	
				TSOP	–	1	µs	

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Table 35: Read AC Characteristics (Continued)

Parameter	Symbol		Condition	Package	Min	Max	Unit	Notes
	Legacy	JEDEC						
BYTE# HIGH to output valid	^{t}FHQV	^{t}BHQV	–	BGA	–	1	µs	
				TSOP	–	1	µs	
BYTE# LOW to output in High-Z	^{t}FLQZ	^{t}BLQZ	–	BGA	–	1	µs	
				TSOP	–	1	µs	

Note: 1. Sampled only; not 100% tested.

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Figure 19: Random Read AC Timing (8-Bit Mode)

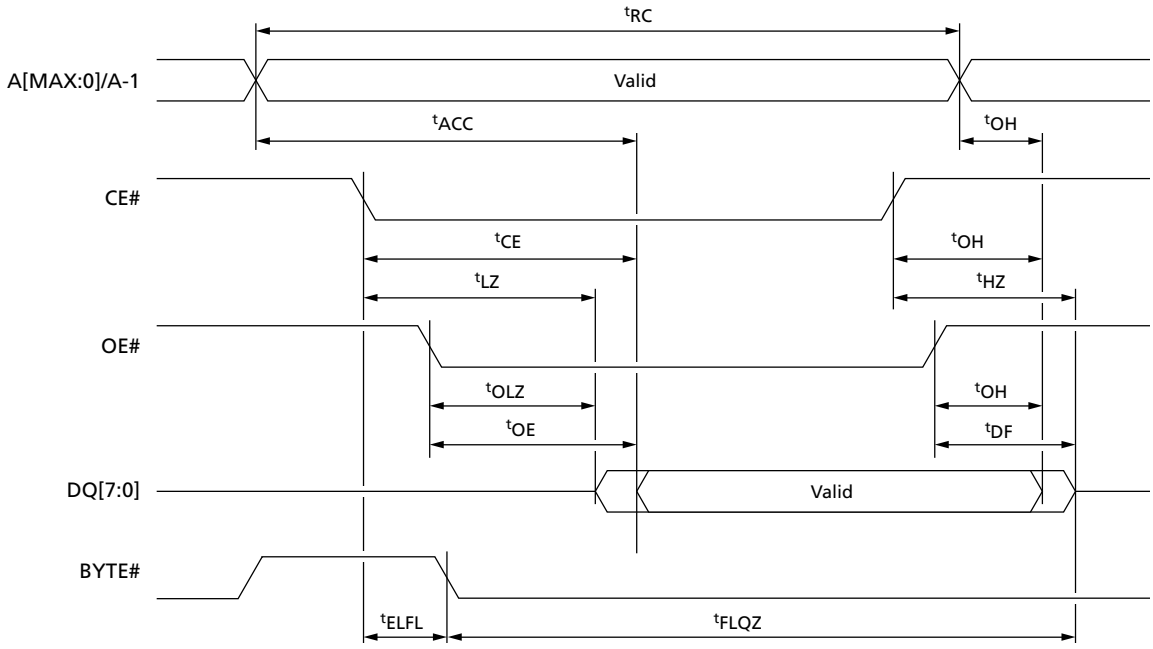

Figure 20: Random Read AC Timing (16-Bit Mode)

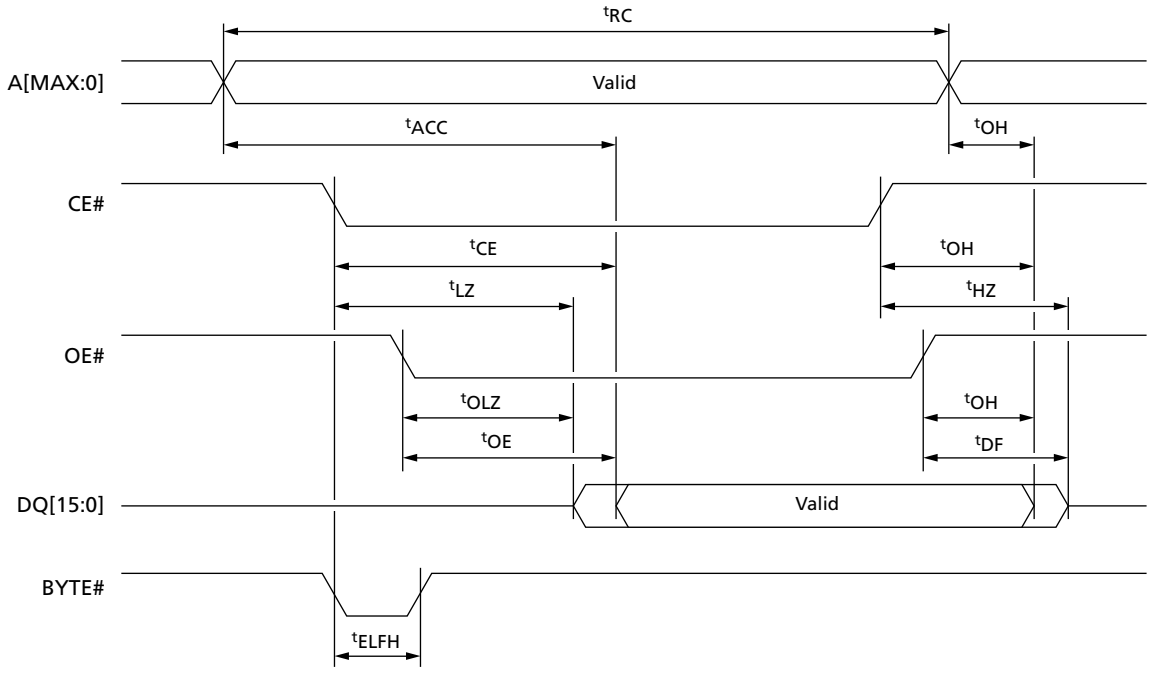

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Figure 21: BYTE# Transition Read AC Timing

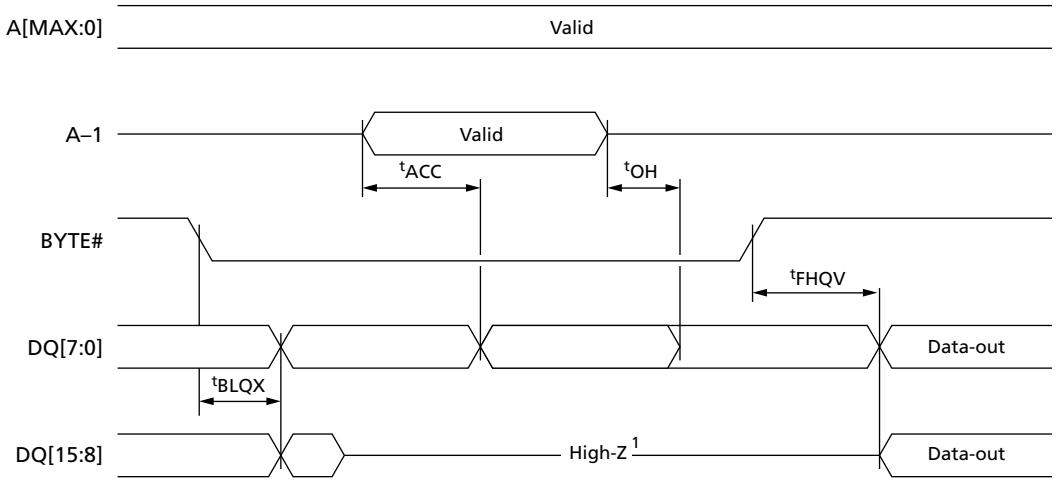
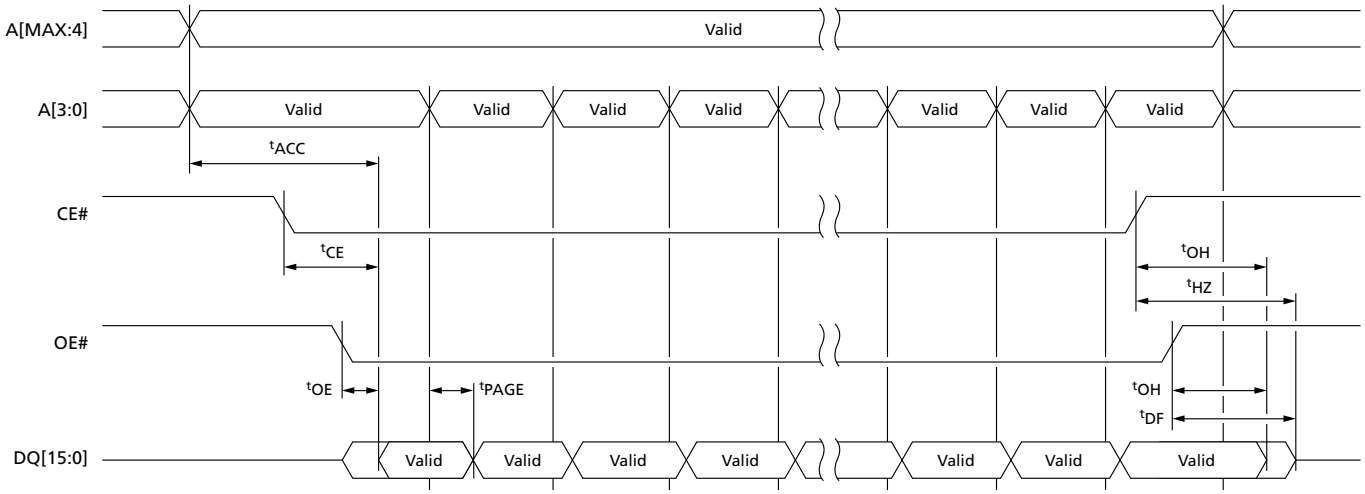


Figure 22: Page Read AC Timing (16-Bit Mode)



Note: 1. Page size is 8 words (16 bytes) and is addressed by address inputs A[2:0] in x16 bus mode and A[2:0] plus DQ15/A–1 in x8 bus mode.

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Write AC Characteristics

Table 36: WE#-Controlled Write AC Characteristics

Parameter	Symbol		Package	Min	Typ	Max	Unit	Notes
	Legacy	JEDEC						
Address valid to next address valid (V_{CCQ} ≥ 2.7V)	^{t}WC	^{t}AVAV	BGA	60	–	–	ns	
			TSOP	70	–	–	ns	
Address valid to next address valid (V_{CCQ} < 2.7V)			BGA	65	-	-	ns	
			TSOP	75	-	-	ns	
CE# LOW to WE# LOW	^{t}CS	^{t}ELWL	BGA	0	–	–	ns	
			TSOP	0	–	–	ns	
WE# LOW to WE# HIGH	^{t}WP	^{t}WLWH	BGA	35	–	–	ns	
			TSOP	35	–	–	ns	
Input valid to WE# HIGH	^{t}DS	^{t}DVWH	BGA	30	–	–	ns	
			TSOP	30	–	–	ns	
WE# HIGH to input transition	^{t}DH	^{t}WHDX	BGA	0	–	–	ns	
			TSOP	0	–	–	ns	
WE# HIGH to CE# HIGH	^{t}CH	^{t}WHEH	BGA	0	–	–	ns	
			TSOP	0	–	–	ns	
WE# HIGH to WE# LOW	^{t}WPH	^{t}WHWL	BGA	20	–	–	ns	
			TSOP	20	–	–	ns	
Address valid to WE# LOW	^{t}AS	^{t}AVWL	BGA	0	–	–	ns	
			TSOP	0	–	–	ns	
WE# LOW to address transition	^{t}AH	^{t}WLAX	BGA	45	–	–	ns	
			TSOP	45	–	–	ns	
OE# HIGH to WE# LOW	–	^{t}GHWL	BGA	0	–	–	ns	
			TSOP	0	–	–	ns	
WE# HIGH to OE# LOW	^{t}OEH	^{t}WHGL	BGA	0	–	–	ns	
			TSOP	0	–	–	ns	
Program/erase valid to RY/BY# LOW	^{t}BUSY	^{t}WHRL	BGA	–	–	90	ns	1
			TSOP	–	–	90	ns	1
V_{CC} HIGH to CE# LOW	^{t}VCS	^{t}VCHEL	BGA	60	–	–	µs	
			TSOP	60	–	–	µs	

Note: 1. Sampled only; not 100% tested.

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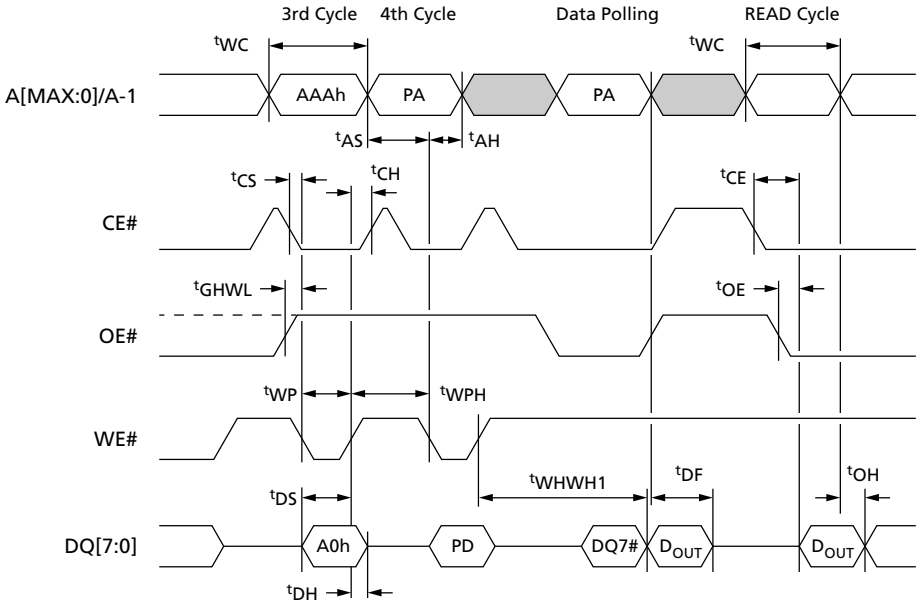
Figure 23: WE#-Controlled Program AC Timing (8-Bit Mode)



Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit and by a READ operation that outputs the data (D_{OUT}) programmed by the previous PROGRAM command.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7. (See Data Polling Bit [DQ7].)
4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

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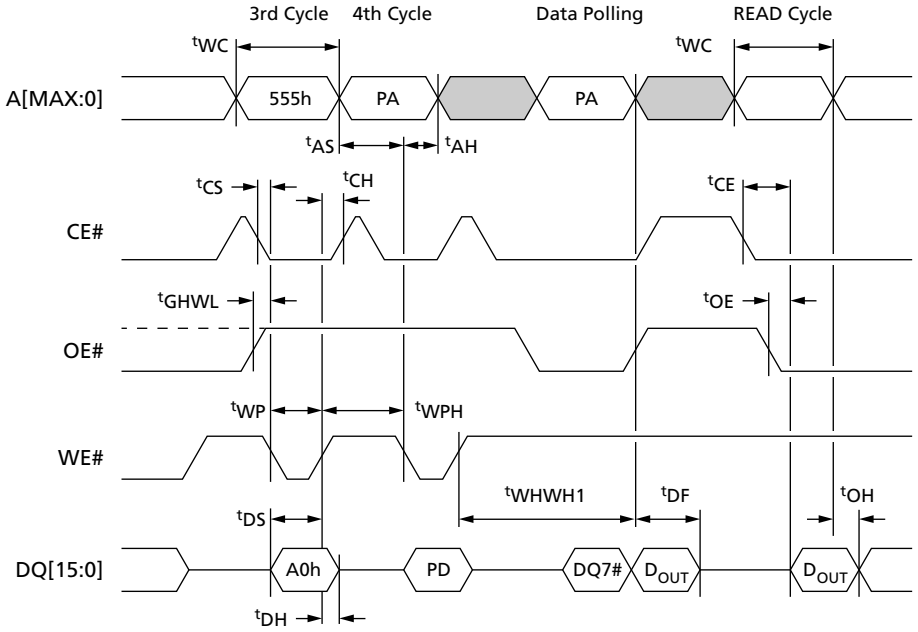
Figure 24: WE#-Controlled Program AC Timing (16-Bit Mode)



Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit and by a READ operation that outputs the data (D_{OUT}) programmed by the previous PROGRAM command.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7. (See Data Polling Bit [DQ7].)
4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

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Table 37: CE#-Controlled Write AC Characteristics

Parameter	Symbol		Package	Min	Typ	Max	Unit
	Legacy	JEDEC					
Address valid to next address valid(V_{CCQ} ≥ 2.7V)	^{t}WC	^{t}AVAV	BGA	60	–	–	ns
			TSOP	70	–	–	ns
Address valid to next address valid(V_{CCQ} < 2.7V)			BGA	65	-	-	ns
			TSOP	75	-	-	ns
WE# LOW to CE# LOW	^{t}WS	^{t}WLEL	BGA	0	–	–	ns
			TSOP	0	–	–	ns
CE# LOW to CE# HIGH	^{t}CP	^{t}ELEH	BGA	35	–	–	ns
			TSOP	35	–	–	ns
Input valid to CE# HIGH	^{t}DS	^{t}DVEH	BGA	30	–	–	ns
			TSOP	30	–	–	ns
CE# HIGH to input transition	^{t}DH	^{t}EHDX	BGA	0	–	–	ns
			TSOP	0	–	–	ns
CE# HIGH to WE# HIGH	^{t}WH	^{t}EHWH	BGA	0	–	–	ns
			TSOP	0	–	–	ns
CE# HIGH to CE# LOW	^{t}CPH	^{t}EHEL	BGA	20	–	–	ns
			TSOP	20	–	–	ns
Address valid to CE# LOW	^{t}AS	^{t}AVEL	BGA	0	–	–	ns
			TSOP	0	–	–	ns
CE# LOW to address transition	^{t}AH	^{t}ELAX	BGA	45	–	–	ns
			TSOP	45	–	–	ns
OE# HIGH to CE# LOW	–	^{t}GHEL	BGA	0	–	–	ns
			TSOP	0	–	–	ns

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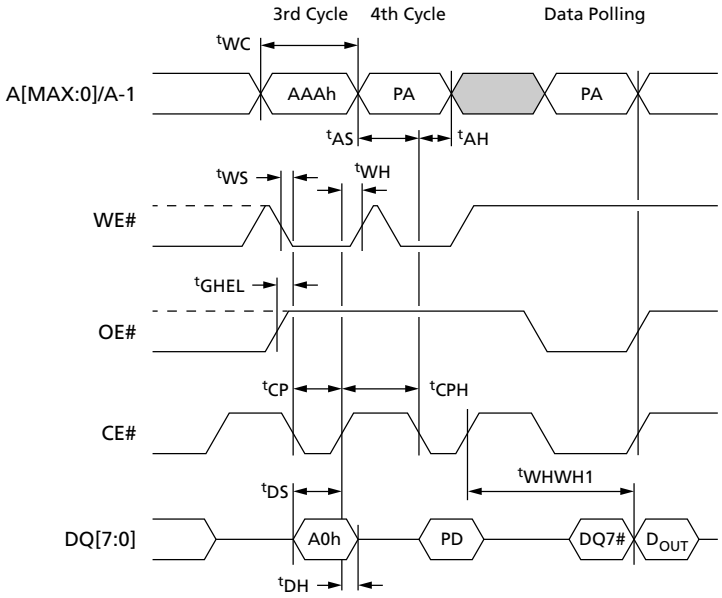
Figure 25: CE#-Controlled Program AC Timing (8-Bit Mode)



Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7. (See Data Polling Bit [DQ7].)
4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

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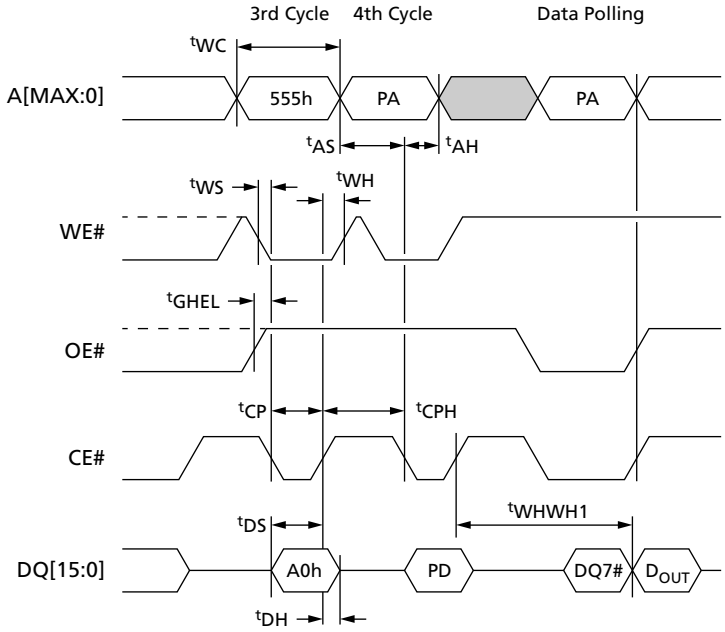
Figure 26: CE#-Controlled Program AC Timing (16-Bit Mode)



Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7. (See Data Polling Bit [DQ7].)
4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

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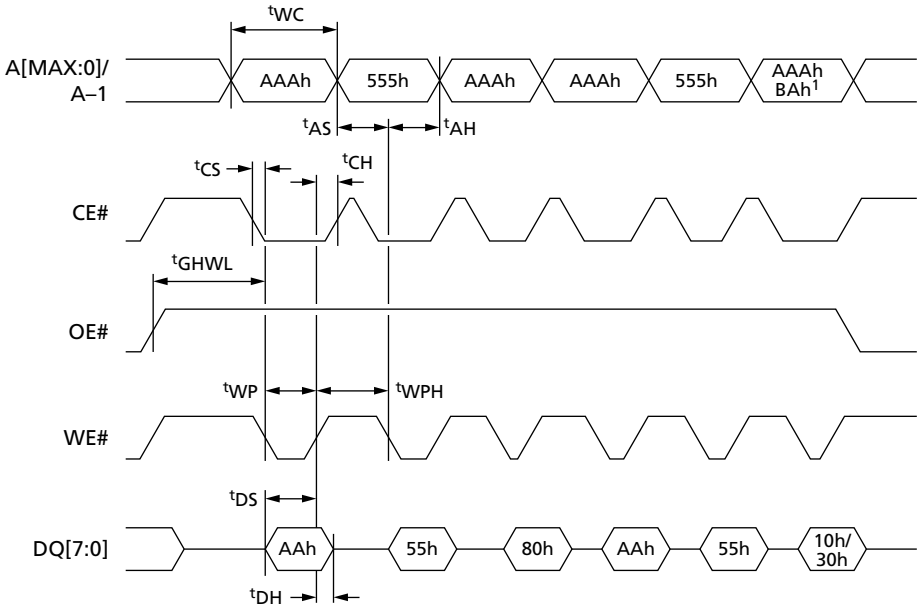
Figure 27: Chip/Block Erase AC Timing (8-Bit Mode)



Notes:
1. For a CHIP ERASE command, the address is 555h, and the data is 10h; for a BLOCK ERASE command, the address is BAd, and the data is 30h.
2. BAd is the block address.
3. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

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Accelerated Program, Data Polling/Toggle AC Characteristics

Table 38: Accelerated Program and Data Polling/Data Toggle AC Characteristics

Parameter	Symbol		Min	Max	Unit
	Legacy	JEDEC			
V_{PP}/WP# rising or falling time	–	^{t}VHVPP	250	–	ns
Valid V_{HH} on V_{PP}/WP# to WE# HIGH	–	^{t}VHHWH	50	–	ns
Address setup time to OE# LOW during toggle bit polling	^{t}ASO	^{t}AXGL	15	–	ns
Address hold time from OE# during toggle bit polling	^{t}AHT	^{t}GHAX, ^{t}EHAX	0	–	ns
CE# HIGH during toggle bit polling	^{t}EPH	^{t}EHEL2	20	–	ns
Output hold time during data and toggle bit polling	^{t}OEH	^{t}WHGL2, ^{t}GHGL2	20	–	ns
Program/erase valid to RY/BY# LOW	^{t}BUSY	^{t}WHRL	–	90	ns

Note: 1. Sampled only; not 100% tested.

Figure 28: Accelerated Program AC Timing

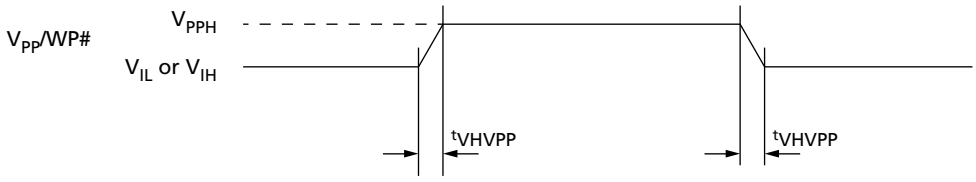
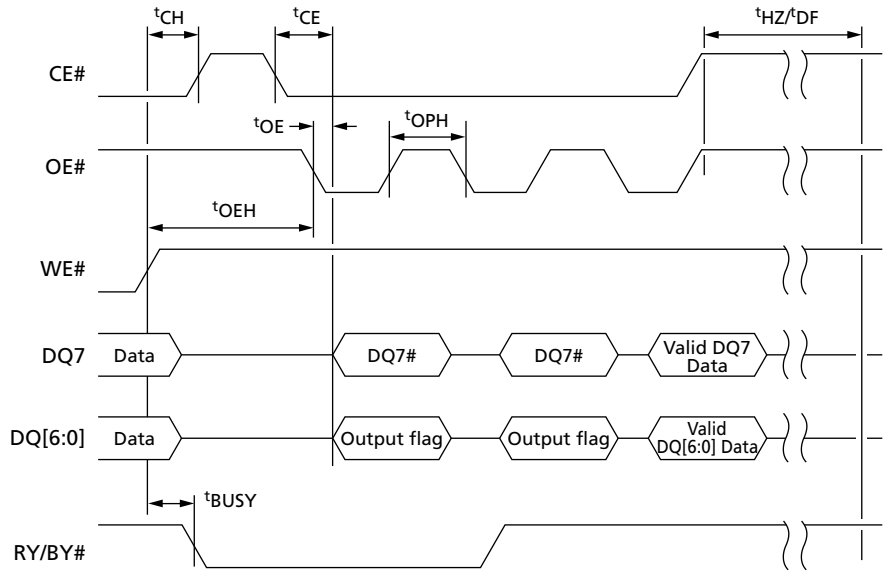


Figure 29: Data Polling AC Timing



Notes: 1. DQ7 returns a valid data bit when the PROGRAM or ERASE command has completed.

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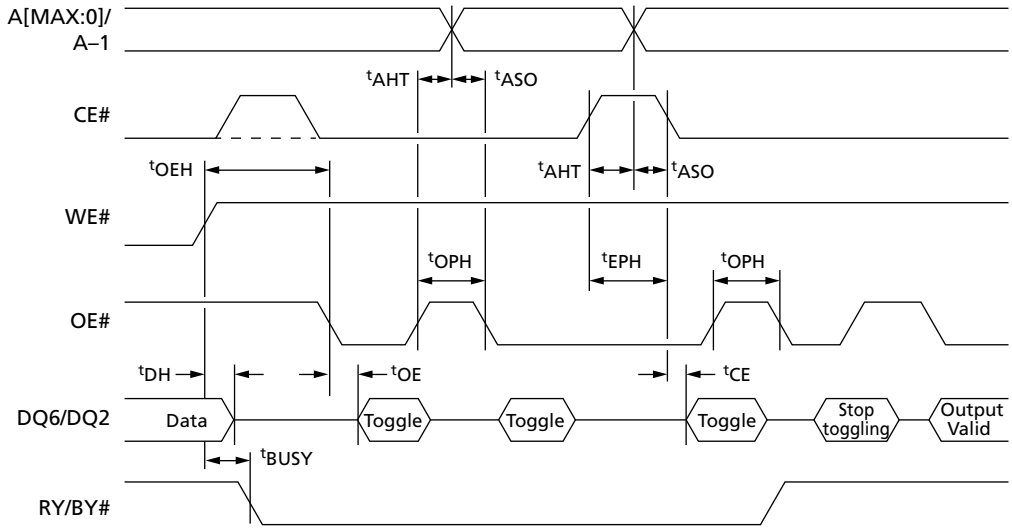
2. See the following tables for timing details: Read AC Characteristics, Accelerated Program and Data Polling/Data Toggle AC Characteristics.

Figure 30: Toggle/Alternative Toggle Bit Polling AC Timing (8-Bit Mode)



Notes:
1. DQ6 stops toggling when the PROGRAM or ERASE command has completed. DQ2 stops toggling when the CHIP ERASE or BLOCK ERASE command has completed.
2. See the following tables for timing details: Read AC Characteristics, Accelerated Program and Data Polling/Data Toggle AC Characteristics.

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Electrical Specifications – Program/Erase Characteristics

Table 39: Program/Erase Characteristics

Parameter		Buffer Size	Byte	Word	Min	Typ[1, 2]	Max[2]	Unit
Block erase		–	–	–	–	0.5	4	s
Erase suspend latency		–	–	–	–	20	25	µs
Block erase timeout		–	–	–	50	–	–	µs
Byte program	Single-byte program	–	–	–	–	15	175	µs
	Double-/ quadruple-/ octuple-byte program	–	–	–	–	10	200	µs
	Byte write to buffer program	32	32	–	–	70	200	µs
		64	64	–	–	85	200	µs
		256	256	–	–	160	710	µs
	Effective write to buffer program per byte	32	1	–	–	2.19	6.25	µs
		64	1	–	–	1.33	3.125	µs
		256	1	–	–	0.625	2.77	µs
Word program	Single-word program	–	–	–	–	15	175	µs
	Word write to buffer program	16	–	16	–	70	200	µs
		32	–	32	–	85	200	µs
		128	–	128	–	160	710	µs
		256	–	256	–	284	1280	µs
	Full buffer program with V_{PPH}	256	–	256	–	160	800	µs
	Effective write to buffer program per word	16	–	1	–	4.375	12.5	µs
		32	–	1	–	2.66	6.25	µs
		128	–	1	–	1.25	5.55	µs
		256	–	1	–	1.11	5	µs
	Effective full buffer program per word with V_{PPH}	256	–	1	–	0.625	3.125	µs
Program suspend latency		–	–	–	–	20	25	µs
Blank check		–	–	–	–	3.2	–	ms
PROGRAM/ERASE cycles (per block)		–	–	–	100,000	–	–	cycles

Notes:
1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.

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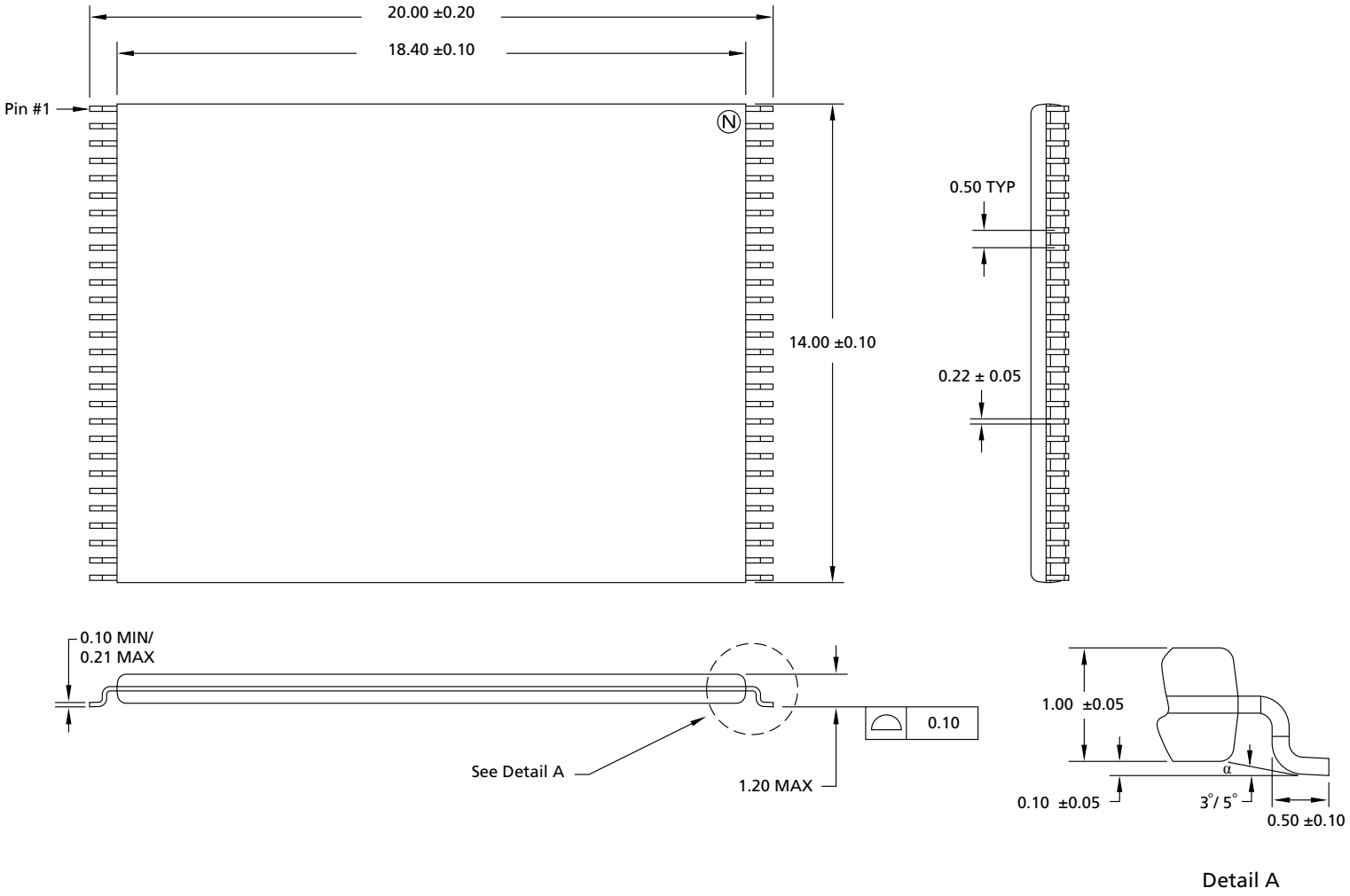
Package Dimensions

Figure 31: 56-Pin TSOP – 14mm x 20mm



Notes:
1. All dimensions are in millimeters.
2. For the lead width value of 0.22 ±0.05, there is also a legacy value of 0.15 ±0.05.

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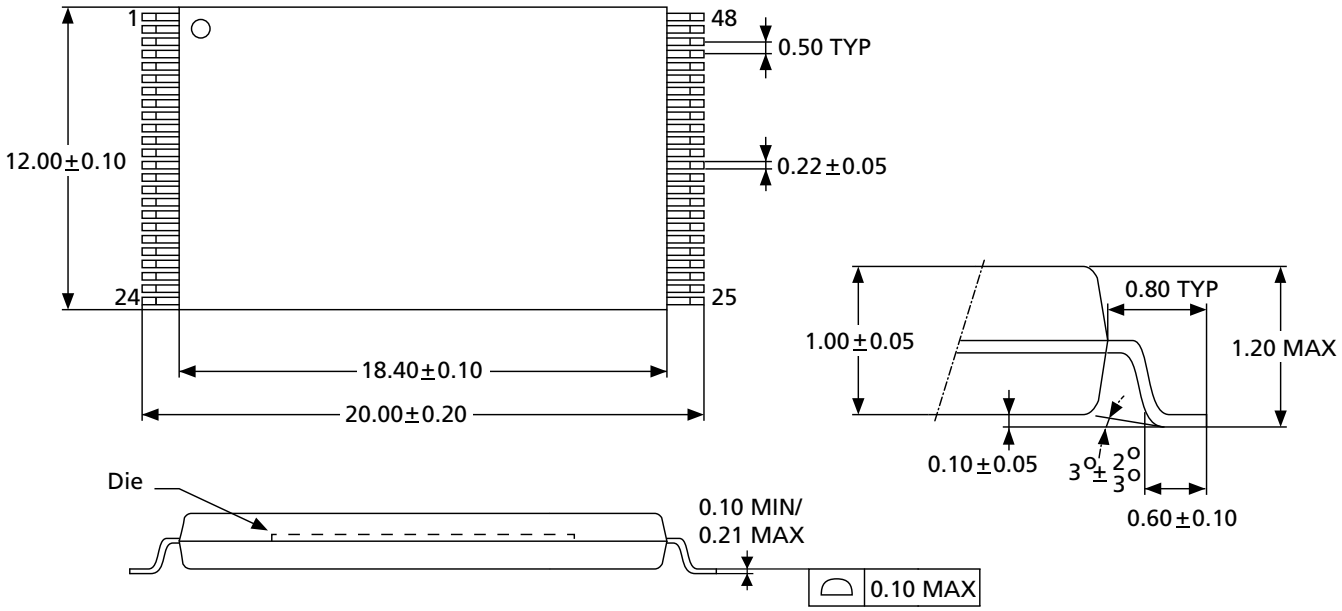
Figure 32: 48-Pin TSOP – 12mm x 20mm



Note: 1. All dimensions are in millimeters.

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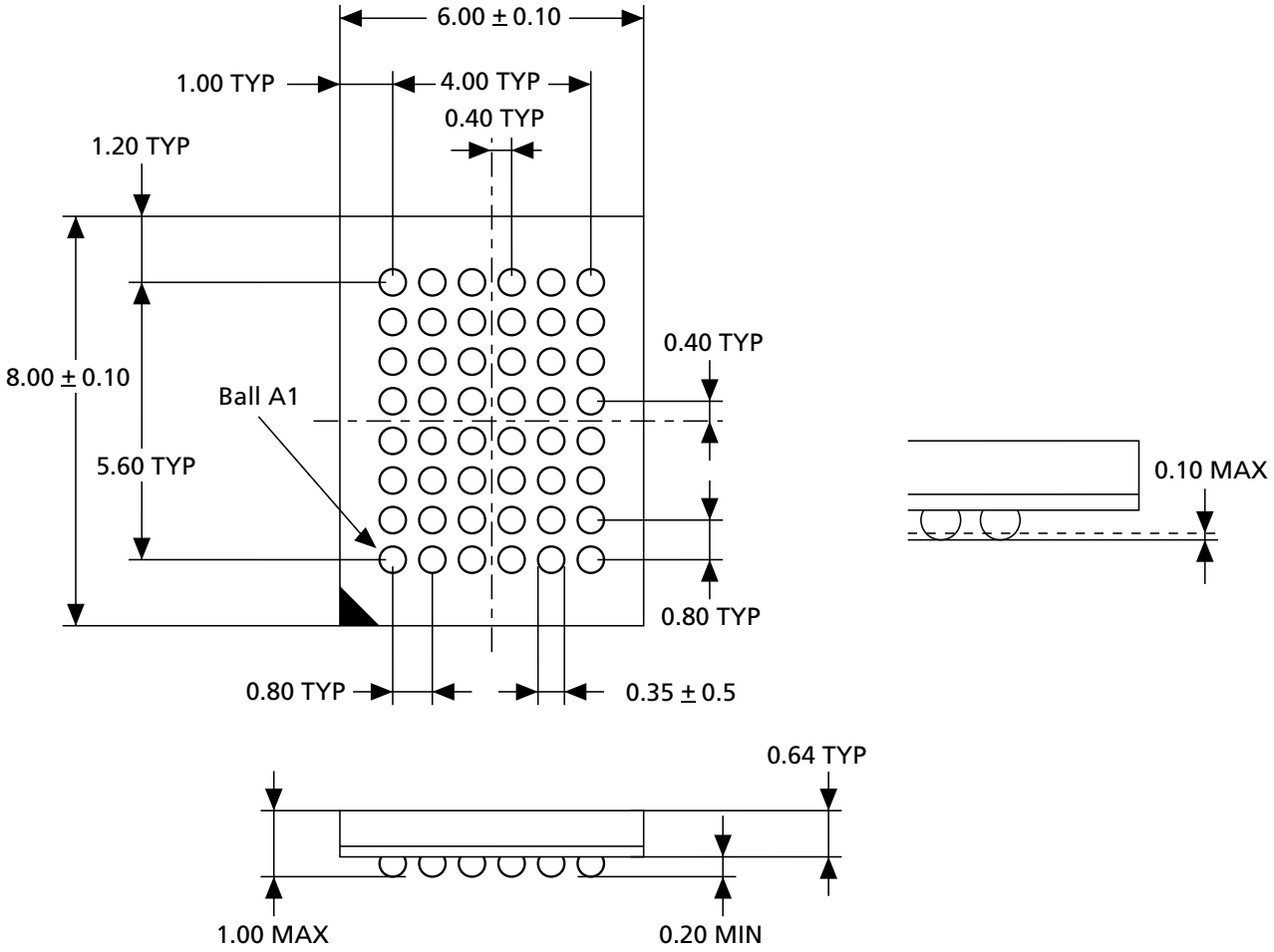
Figure 33: 48-Ball BGA – 6mm x 8mm



Note: 1. All dimensions are in millimeters.

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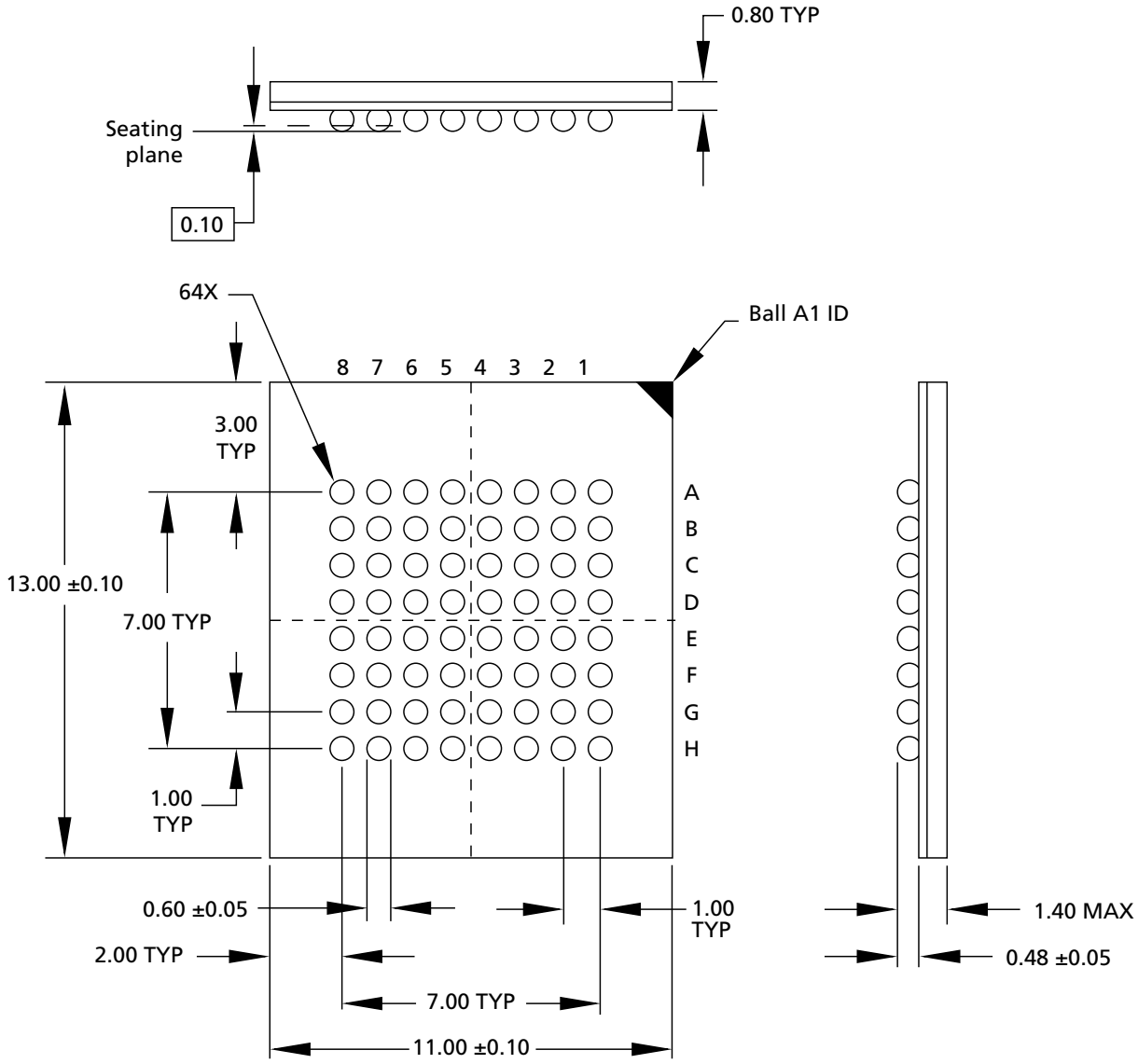
Figure 34: 64-Ball Fortified BGA – 11mm x 13mm



Note: 1. All dimensions are in millimeters.

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Revision History

Rev. B – 11/12

- Added text to Signal Descriptions to clarify V_{PP}/WP# and VSS decoupling requirement.
- Added note to DC Voltage Characteristics table to clarify VIH spec.

Rev. A – 08/12

- Initial Micron rebrand release

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Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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