



**THE DATASHEET OF
ISL90728WIE627Z-TK**



ISL90727, ISL90728

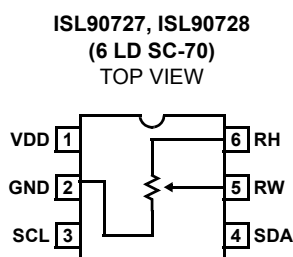
Single Volatile 128-Tap XDCP™ Digitally Controlled Potentiometer (XDCP)

FN8247
Rev 8.00
May 10, 2012

The Intersil ISL90727 and ISL90728 are digitally controlled potentiometers (XDCP™). Each device consists of a resistor array, wiper switches, and a control section. The wiper position is controlled by an I²C Bus™.

The potentiometer is implemented by a resistor array composed of 127 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the SDA and SCL inputs.

Pinout



Features

- Volatile Solid-State Potentiometer
- I²C Serial Bus Interface
- DCP Terminal Voltage, 2.7V to 5.5V
- Low Tempco
 - Rheostat - 45 ppm/°C Typical
 - Divider - 15 ppm/°C Typical
- 128 Wiper Tap Points
 - Wiper Resistance 70Ω Typ at V_{CC} = 3.3V
- Low Power CMOS
 - Active Current, 200μA Max
 - Standby Current, 500nA Max
- Available R_{TOTAL} Values = 50kΩ, 10kΩ
- Power-on Preset to Midscale
- Packaging
 - 6 Ld SC-70
- Pb-Free (RoHS Compliant)

Applications

- Mechanical Potentiometer Replacement
- Transducer Adjustment of Pressure, Temperature, Position, Chemical, and Optical Sensors
- RF Amplifier Biasing
- LCD Brightness and Contrast Adjustment
- Gain Control and Offset Adjustment

Ordering Information

| PART NUMBER (Notes 1, 2, 3, 4) | PART MARKING (Bottom Side) | R _{TOTAL} (kΩ) | TEMP RANGE (°C) | PACKAGE (Pb-Free) | PKG. DWG. # |
|-----------------------------------|-------------------------------|----------------------------|--------------------|----------------------|----------------|
| ISL90727UIE627Z-TK | ANI | 50 | -40 to +85 | 6 Ld SC-70 | P6.049 |
| ISL90727WIE627Z-T7A | ANH | 10 | -40 to +85 | 6 Ld SC-70 | P6.049 |
| ISL90727WIE627Z-TK | ANH | 10 | -40 to +85 | 6 Ld SC-70 | P6.049 |
| ISL90728UIE627Z-TK | CDY | 50 | -40 to +85 | 6 Ld SC-70 | P6.049 |
| ISL90728WIE627Z-T7A | CCF | 10 | -40 to +85 | 6 Ld SC-70 | P6.049 |
| ISL90728WIE627Z-TK | CCF | 10 | -40 to +85 | 6 Ld SC-70 | P6.049 |

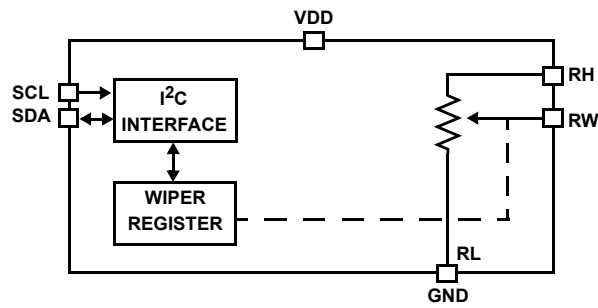
NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL90727](#), [ISL90728](#). For more information on MSL please see Tech Brief [TB363](#).
4. ISL90727 has an I²C address 5Ch and ISL90728 has an I²C address 7Ch.

Pin Descriptions

| PIN NUMBER | SYMBOL | DESCRIPTION |
|------------|--------|-------------------------------|
| 1 | VDD | Supply Voltage |
| 2 | GND | Ground |
| 3 | SCL | Open drain Serial Clock input |
| 4 | SDA | Open drain Serial Data I/O |
| 5 | RW | Potentiometer Wiper Terminal |
| 6 | RH | Potentiometer High Terminal |

Block Diagram



Absolute Maximum Ratings

| | |
|--------------------------------------|--------------------------------|
| Storage Temperature | -65°C to +150°C |
| Voltage at any Digital Interface Pin | |
| with Respect to V _{SS} | -0.3V to V _{CC} + 0.3 |
| V _{CC} | -0.3V to +7V |
| Voltage at any DCP Pin with | |
| Respect to V _{SS} | -0.3V to V _{CC} |
| I _W (10s) | ±6mA |
| Latchup | Class II, Level B at +85°C |
| ESD Rating | |
| Human Body Model | 2kV |

Thermal Information

| | | |
|---------------------------------|---|----------------------|
| Thermal Resistance (Typical) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
| 6 Ld SC-70 Package (Notes 5, 6) | 480 | 210 |
| Pb-Free Reflow Profile | see link below | |
| | http://www.intersil.com/pbfree/Pb-FreeReflow.asp | |

Recommended Operating Conditions

| | |
|--------------------------|----------------|
| Industrial | -40°C to +85°C |
| V _{CC} | 2.7V to 5.5V |
| Power Rating of Each DCP | 5mW |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.
- For θ_{JC} , the "case temp" location is taken at the package top center.

Analog Specifications Over recommended operating conditions, unless otherwise stated.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 19) | TYP (Note 7) | MAX (Note 19) | UNIT | |
|--|---|---|------------------|-----------------|------------------|-----------------|-----------------|
| R _{TOTAL} | R _H to R _L Resistance | W option | | 10 | | k Ω | |
| | | U option | | 50 | | k Ω | |
| | R _H to R _L Resistance Tolerance | | -20 | | +20 | % | |
| R _W | Wiper Resistance | V _{CC} = 3.3V @ +25°C | | 85 | 200 | Ω | |
| C _H /C _L /C _W | Potentiometer Capacitance | | | 10/10/25 | | pF | |
| I _{LkgDCP} | Leakage on DCP Pins | Voltage at pin from GND to V _{CC} | | 0.1 | | μ A | |
| VOLTAGE DIVIDER MODE | | | | | | | |
| INL | Integral Non-linearity | | -1 | ±0.2 | 1 | LSB (Note 8) | |
| DNL | Differential Non-linearity | Monotonic over all tap positions | W option | -1 | ±0.1 | 1 | LSB (Note 8) |
| | | | U option | -1 | ±0.1 | 1 | LSB (Note 8) |
| Z _{Error} (Note 9) | Zero-scale Error | W option | 0 | 1 | 3 | LSB (Note 8) | |
| | | U option | 0 | 0.5 | 1 | LSB (Note 8) | |
| F _{Error} (Note 10) | Full-scale Error | W option | -3 | -1 | 0 | LSB (Note 8) | |
| | | U option | -1 | -0.5 | 0 | LSB (Note 8) | |
| TC _V (Note 16) | Ratiometric Temperature Coefficient | DCP Register set to 80 hex | | ±15 | | ppm/°C | |
| RESISTOR MODE | | | | | | | |
| R _{INL} (Note 14) | Integral Non-linearity | DCP register set between 20 hex and FF hex. Monotonic over all tap positions | -2 | ±0.25 | 2 | MI (Note 11) | |
| R _{DNL} (Note 13) | Differential Non-linearity | DCP register set between 20 hex and FF hex. Monotonic over all tap positions | W option | -1 | ±0.1 | 1 | MI (Note 11) |
| | | | U option | -1 | ±0.1 | 1 | MI (Note 11) |
| R _{OFFSET} (Note 12) | Offset | W option | 0 | 1 | 3 | MI (Note 11) | |
| | | U option | 0 | 0.5 | 1 | MI (Note 11) | |
| TC _R (Notes 15, 16) | Resistance Temperature Coefficient | DCP register set between 20 hex and FF hex | | ±45 | | ppm/°C | |

Operating Specifications

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 19) | TYP (Note 7) | MAX (Note 19) | UNIT |
|--------------------------------|--|--|------------------|-----------------|------------------|------|
| I _{CC1} | V _{CC} Supply Current (Volatile write/read) | f _{SCL} = 400kHz; SDA = Open; (for I ² C, Active, Read and Volatile Write States only) | | | 200 | μA |
| I _{SB} | V _{CC} Current (standby) | V _{CC} = +5.5V, I ² C Interface in Standby State | | | 500 | nA |
| I _{ComLkg} | Common-Mode Leakage | Voltage at SDA pin to GND or V _{CC} | | | 3 | μA |
| t _{DCP} (Note 16) | DCP Wiper Response Time | SCL falling edge of last bit of DCP Data Byte to wiper change | | 500 | | ns |
| V _{CC} Ramp (Note 20) | V _{CC} Ramp Rate | | 0.2 | | | V/ms |
| t _D | Power-up Delay | V _{CC} above V _{POR} , to DCP Initial Value Register recall completed, and I ² C Interface in standby state | | | 3 | ms |

SERIAL INTERFACE SPECIFICATIONS

| | | | | | | |
|----------------------------|--|---|--------------------------|--|--------------------------|-----|
| V _{IL} | SDA, and SCL Input Buffer LOW Voltage | (Note 17) | -0.3 | | 0.3* V _{CC} | V |
| V _{IH} | SDA, and SCL Input Buffer HIGH Voltage | (Note 17) | 0.7* V _{CC} | | V _{CC} + 0.3 | V |
| Hysteresis | SDA and SCL Input Buffer Hysteresis | | 0.05* V _{CC} | | | V |
| V _{OL} | SDA Output Buffer LOW Voltage, Sinking 4mA | | 0 | | 0.4 | V |
| C _{pin} (Note 18) | SDA and SCL Pin Capacitance | | | | 10 | pF |
| f _{SCL} | SCL Frequency | | | | 400 | kHz |
| t _{IN} | Pulse Width Suppression Time at SDA and SCL Inputs | Any pulse narrower than the max spec is suppressed. | | | 50 | ns |
| t _{AA} | SCL Falling Edge to SDA Output Data Valid | SCL falling edge crossing 30% of V _{CC} , until SDA exits the 30% to 70% of V _{CC} window. | | | 900 | ns |
| t _{BUF} | Time the Bus Must be Free Before the Start of a New Transmission | SDA crossing 70% of V _{CC} during a STOP condition, to SDA crossing 70% of V _{CC} during the following START condition. | 1300 | | | ns |
| t _{LOW} | Clock LOW Time | Measured at the 30% of V _{CC} crossing. | 1300 | | | ns |
| t _{HIGH} | Clock HIGH Time | Measured at the 70% of V _{CC} crossing. | 600 | | | ns |
| t _{SU:STA} | START Condition Setup Time | SCL rising edge to SDA falling edge. Both crossing 70% of V _{CC} . | 600 | | | ns |
| t _{HD:STA} | START Condition Hold Time | From SDA falling edge crossing 30% of V _{CC} to SCL falling edge crossing 70% of V _{CC} . | 600 | | | ns |
| t _{SU:DAT} | Input Data Setup Time | From SDA exiting the 30% to 70% of V _{CC} window, to SCL rising edge crossing 30% of V _{CC} | 100 | | | ns |
| t _{HD:DAT} | Input Data Hold Time | From SCL rising edge crossing 70% of V _{CC} to SDA entering the 30% to 70% of V _{CC} window. | 0 | | | ns |
| t _{SU:STO} | STOP Condition Setup Time | From SCL rising edge crossing 70% of V _{CC} , to SDA rising edge crossing 30% of V _{CC} . | 600 | | | ns |
| t _{HD:STO} | STOP Condition Hold Time for Read, or Volatile Only Write | From SDA rising edge to SCL falling edge. Both crossing 70% of V _{CC} . | 600 | | | ns |
| t _{DH} | Output Data Hold Time | From SCL falling edge crossing 30% of V _{CC} , until SDA enters the 30% to 70% of V _{CC} window. | 0 | | | ns |
| t _R (Note 18) | SDA and SCL Rise Time | From 30% to 70% of V _{CC} | 20 + 0.1*Cb | | 250 | ns |

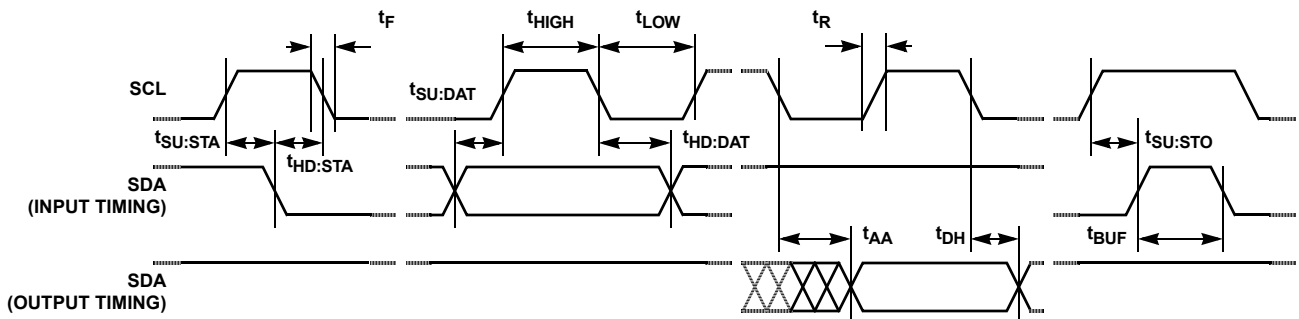
Operating Specifications (Continued)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 19) | TYP (Note 7) | MAX (Note 19) | UNIT |
|---------------------------|---|--|---------------|--------------|---------------|------|
| t _F (Note 18) | SDA and SCL Fall Time | From 70% to 30% of V _{CC} | 20 + 0.1*Cb | | 250 | ns |
| C _b (Note 18) | Capacitive Loading of SDA or SCL | Total on-chip and off-chip | 10 | | 400 | pF |
| R _{pu} (Note 18) | SDA and SCL Bus Pull-up Resistor Off-chip | Maximum is determined by t _R and t _F . For C _b = 400pF, max is about 2kΩ ~ 2.5kΩ. For C _b = 40pF, max is about 15kΩ ~ 20kΩ | 1 | | | kΩ |

NOTES:

- Typical values are for T_A = +25°C and 3.3V supply voltage.
- LSB: [V(R_W)₁₂₇ - V(R_W)₀]/127. V(R_W)₁₂₇ and V(R_W)₀ are V(R_W) for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
- ZS error = V(R_W)₀/LSB.
- FS error = [V(R_W)₁₂₇ - V_{CC}]/LSB.
- MI = |R₁₂₇ - R₀|/127. R₁₂₇ and R₀ are the measured resistances for the DCP register set to FF hex and 00 hex respectively.
R_{OFFSET} = R₀/MI, when measuring between R_W and R_L.
- R_{OFFSET} = R₁₂₇/MI, when measuring between R_W and R_H.
- RDNL = (R_i - R_{i-1})/MI - 1, for i = 32 to 127.
- RINL = [R_i - (MI • i) - R₀]/MI, for i = 32 to 127.
- $TC_R = \frac{[\text{Max}(R_i) - \text{Min}(R_i)]}{[\text{Max}(R_i) + \text{Min}(R_i)]/2} \times \frac{10^6}{+125^\circ\text{C}}$ for i = 32 to 127, T = -40°C to +85°C. Max () is the maximum value of the resistance and Min () is the minimum value of the resistance over the temperature range.
- This parameter is not 100% tested.
- V_{IL} = 0V, V_{IH} = V_{CC}.
- These are I²C-specific parameters and are not directly tested, however, they are used in the device testing to validate specifications.
- Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
- The ramp must be >0.2V/ms at any voltage <2.7V starting from 0VDC. A power down to any voltage other than 0V is not included in the ramp rate spec and may result in improper operation.

SDA vs SCL Timing



Principles of Operation

The ISL90727 and ISL90728 are integrated circuits incorporating one DCP with its associated registers and an I²C serial interface providing direct communication between a host and the potentiometer.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of the DCP are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L pins). The R_W pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by a 7-bit volatile Wiper Register (WR). The DCP has its own WR. When the WR of the DCP contains all zeroes ($WR<6:0> = 00h$), its wiper terminal (R_W) is closest to its “Low” terminal (R_L). When the WR of the DCP contains all ones ($WR<6:0> = 7Fh$), its wiper terminal (R_W) is closest to its “High” terminal (R_H). As the value of the WR increases from all zeroes (00h) to all ones (127 decimal), the wiper moves monotonically from the position closest to R_L to the position closest to R_H . At the same time, the resistance between R_W and R_L increases monotonically, while the resistance between R_H and R_W decreases monotonically. R_L is connected to the GND pin of the device, so the wiper movement will always be relative to R_L .

While the ISL90727 and ISL90728 are being powered up, the WR is reset to 40h (64 decimal), which locates R_W roughly at the center between R_L and R_H .

The WR and IVR can be read or written directly using the I²C serial interface as described in the following sections.

I²C Serial Interface

The ISL90727 and ISL90728 support bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL90727 and ISL90728 operate as slave devices in all applications.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 1). On power-up of the ISL90727 and ISL90728, the SDA pin is in the input mode.

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL90727 and ISL90728 continuously monitor the SDA and SCL lines for the START condition and do not respond to any

command until this condition is met (see Figure 1). A START condition is ignored during the power-up sequence and during internal non-volatile write cycles.

All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 1).

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting 8 bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 2).

The ISL90727 and ISL90728 respond with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL90727 and ISL90728 also respond with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 0101110 as the seven MSBs for the ISL90727 and 0111110 as the seven MSBs for the ISL90728. The LSB in the Read/Write bit. Its value is “1” for a Read operation, and “0” for a Write operation (see Table 1).

TABLE 1. IDENTIFICATION BYTE FORMAT

| | | | | | | | | | |
|----------|-----|---|---|---|---|---|---|-----|--|
| ISL90727 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | R/W | |
| ISL90728 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | R/W | |
| | MSB | | | | | | | LSB | |

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL90727 and ISL90728 respond with an ACK. At this time, the device enters its standby state (see Figure 3).

Data Protection

A valid Identification Byte, Address Byte, and total number of SCL pulses act as a protection of both volatile and non-volatile registers. During a Write sequence, the Data Byte is loaded into an internal shift register as it is received. If the Address Byte is 0, the Data Byte is transferred to the Wiper Register (WR) at the falling edge of the SCL pulse that loads the last bit (LSB) of the Data Byte. If an address other than 00h or an invalid slave address is sent, then the device will respond with no ACK.

Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 4). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/W bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/W

bit set to "1". After each of the three bytes, the ISL90727 and ISL90728 respond with an ACK. Then the ISL90727 and ISL90728 transmit the Data Byte as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master then terminates the read

operation (issuing a STOP condition) following the last bit of the Data Byte (see Figure 4).

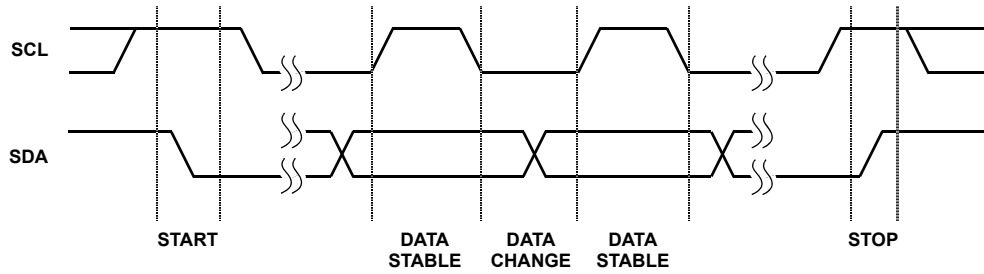


FIGURE 1. VALID DATA CHANGES, START AND STOP CONDITIONS

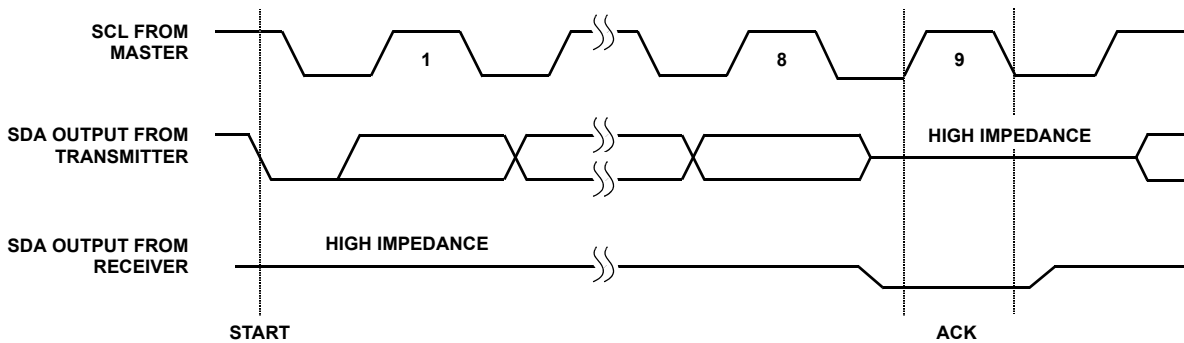


FIGURE 2. ACKNOWLEDGE RESPONSE FROM RECEIVER

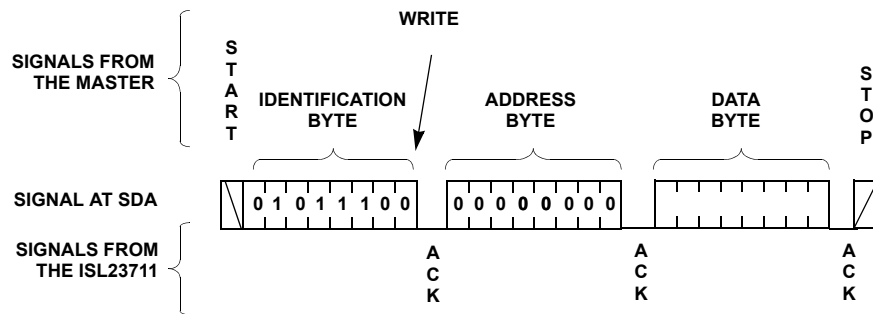


FIGURE 3. BYTE WRITE SEQUENCE (ISL90727 VERSION SHOWN)

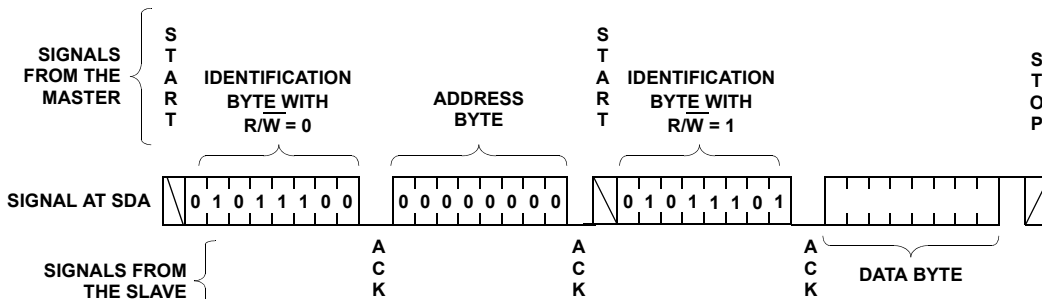
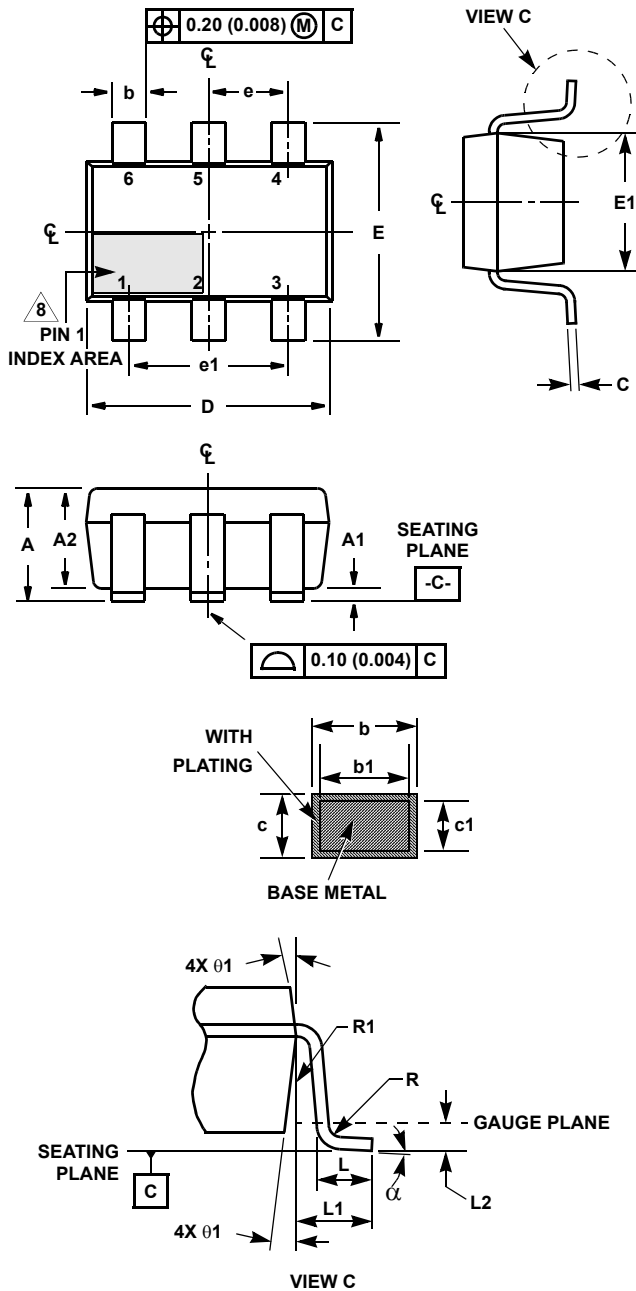


FIGURE 4. READ SEQUENCE (ISL90727 VERSION SHOWN)

Small Outline Transistor Plastic Packages (SC70-6)



P6.049

6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|----------|------------|-------|-------------|------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.031 | 0.043 | 0.80 | 1.10 | - |
| A1 | 0.000 | 0.004 | 0.00 | 0.10 | - |
| A2 | 0.031 | 0.039 | 0.00 | 1.00 | - |
| b | 0.006 | 0.012 | 0.15 | 0.30 | - |
| b1 | 0.006 | 0.010 | 0.15 | 0.25 | |
| c | 0.003 | 0.009 | 0.08 | 0.22 | 6 |
| c1 | 0.003 | 0.009 | 0.08 | 0.20 | 6 |
| D | 0.073 | 0.085 | 1.85 | 2.15 | 3 |
| E | 0.071 | 0.094 | 1.80 | 2.40 | - |
| E1 | 0.045 | 0.053 | 1.15 | 1.35 | 3 |
| e | 0.0256 Ref | | 0.65 Ref | | - |
| e1 | 0.0512 Ref | | 1.30 Ref | | - |
| L | 0.010 | 0.018 | 0.26 | 0.46 | 4 |
| L1 | 0.017 Ref. | | 0.420 Ref. | | |
| L2 | 0.006 BSC | | 0.15 BSC | | |
| N | 6 | | 6 | | 5 |
| R | 0.004 | - | 0.10 | - | |
| R1 | 0.004 | 0.010 | 0.15 | 0.25 | |
| α | 0° | 8° | 0° | 8° | - |

Rev. 3 4/12

NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO203AB.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. "N" is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.
8. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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