



**THE DATASHEET OF
ISL83072EIBZA-T7A**



ISL83070E/71E/72E/73E/75E/76E/77E/78E

±15kV ESD Protected, 3.3V, Full Fail-safe, Low Power, High Speed or Slew Rate Limited, RS-485/RS-422 Transceivers

FN6115
Rev 5.00
October 5, 2012

The Intersil ISL8307XE are BiCMOS 3.3V powered, single transceivers that meet both the RS-485 and RS-422 standards for balanced communication. These devices have very low bus currents (+125mA/-100mA), so they present a true "1/8 unit load" to the RS-485 bus. This allows up to 256 transceivers on the network without violating the RS-485 specification's 32 unit load maximum, and without using repeaters. For example, in a remote utility meter reading system, individual meter readings are routed to a concentrator via an RS-485 network, so the high allowed node count minimizes the number of repeaters required.

Receiver (Rx) inputs feature a "Full Fail-Safe" design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or terminated but undriven.

Hot Plug circuitry ensures that the Tx and Rx outputs remain in a high impedance state while the power supply stabilizes.

The ISL83070E through ISL83075E utilize slew rate limited drivers which reduce EMI, and minimize reflections from improperly terminated transmission lines, or unterminated stubs in multidrop and multipoint applications. Slew rate limited versions also include receiver input filtering to enhance noise immunity in the presence of slow input signals.

The ISL83070E, ISL83071E, ISL83073E, ISL83076E, ISL83077E are configured for full duplex (separate Rx input and Tx output pins) applications. The half duplex versions multiplex the Rx inputs and Tx outputs to allow transceivers with output disable functions in 8 lead packages.

Features

- Pb-Free (RoHS Compliant)
- RS-485 I/O Pin ESD Protection ±15kV HBM
- Class 3 ESD Level on all Other Pins >7kV HBM
- Full Fail-safe (Open, Short, Terminated/Floating) Receivers
- Hot Plug - Tx and Rx Outputs Remain Three-state During Power-up (Only Versions with Output Enable Pins)
- True 1/8 Unit Load Allows up to 256 Devices on the Bus
- Single 3.3V Supply
- High Data Rates up to 20Mbps
- Low Quiescent Supply Current 800µA (Max)
- Ultra Low Shutdown Supply Current 10nA
- -7V to +12V Common Mode Input/Output Voltage Range
- Half and Full Duplex Pinouts
- Three State Rx and Tx Outputs Available
- Current Limiting and Thermal Shutdown for driver Overload Protection
- Tiny MSOP package offering saves 50% board space

Applications

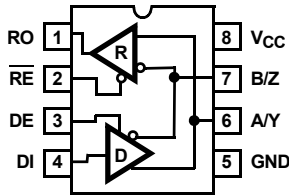
- Automated Utility Meter Reading Systems
- High Node Count Systems
- Field Bus Networks
- Security Camera Networks
- Building Environmental Control/ Lighting Systems
- Industrial/Process Control Networks

TABLE 1. SUMMARY OF FEATURES

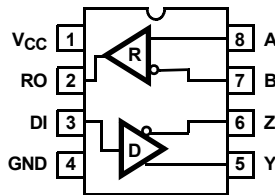
| PART NUMBER | HALF/FULL DUPLEX | DATA RATE (Mbps) | SLEW-RATE LIMITED? | HOT PLUG? | #DEVICES ON BUS | RX/TX ENABLE? | QUIESCENT I _{CC} (µA) | LOW POWER SHUTDOWN? | PIN COUNT |
|-------------|------------------|------------------|--------------------|-----------|-----------------|---------------|--------------------------------|---------------------|-----------|
| ISL83070E | FULL | 0.25 | YES | YES | 256 | YES | 510 | YES | 14 |
| ISL83071E | FULL | 0.25 | YES | NO | 256 | NO | 510 | NO | 8 |
| ISL83072E | HALF | 0.25 | YES | YES | 256 | YES | 510 | YES | 8 |
| ISL83073E | FULL | 0.5 | YES | YES | 256 | YES | 510 | YES | 14 |
| ISL83075E | HALF | 0.5 | YES | YES | 256 | YES | 510 | YES | 8 |
| ISL83076E | FULL | 20 | NO | YES | 256 | YES | 510 | YES | 14 |
| ISL83077E | FULL | 20 | NO | NO | 256 | NO | 510 | NO | 8 |
| ISL83078E | HALF | 20 | NO | YES | 256 | YES | 510 | YES | 8 |

Pinouts

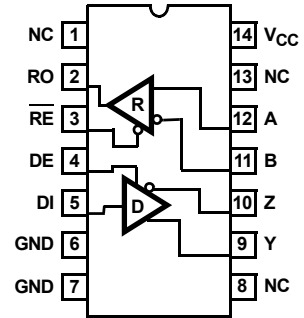
ISL83072E, ISL83075E, ISL83078E
(8 LD MSOP, SOIC)
TOP VIEW



ISL83071E, ISL83077E
(8 LD SOIC)
TOP VIEW



ISL83070E, ISL83073E, ISL83076E
(14 LD SOIC)
TOP VIEW



Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (Pb-Free) | PKG. DWG. # |
|--------------------------------|--------------|---------------------|----------------------|-------------|
| ISL83070EIBZA | 83070EIBZ | -40 to 85 | 14 Ld SOIC | M14.15 |
| ISL83071EIBZA | 83071 EIBZ | -40 to 85 | 8 Ld SOIC | M8.15 |
| ISL83072EIBZA | 83072 EIBZ | -40 to 85 | 8 Ld SOIC | M8.15 |
| ISL83072EIUZA | 3072Z | -40 to 85 | 8 Ld MSOP | M8.118 |
| ISL83073EIBZA | 83073EIBZ | -40 to 85 | 14 Ld SOIC | M14.15 |
| ISL83075EIBZA | 83075 EIBZ | -40 to 85 | 8 Ld SOIC | M8.15 |
| ISL83075EIUZA | 3075Z | -40 to 85 | 8 Ld MSOP | M8.118 |
| ISL83076EIBZA | 83076EIBZ | -40 to 85 | 14 Ld SOIC | M14.15 |
| ISL83077EIBZA | 83077 EIBZ | -40 to 85 | 8 Ld SOIC | M8.15 |
| ISL83078EIBZA | 83078 EIBZ | -40 to 85 | 8 Ld SOIC | M8.15 |
| ISL83078EIUZA | 3078Z | -40 to 85 | 8 Ld MSOP | M8.118 |

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL83070E](#), [ISL83071E](#), [ISL83072E](#), [ISL83073E](#), [ISL83075E](#), [ISL83076E](#), [ISL83077E](#), [ISL83078E](#). For more information on MSL please see tech brief [TB363](#).

Truth Tables

| TRANSMITTING | | | | |
|-----------------|----|----|---------|---------|
| INPUTS | | | OUTPUTS | |
| \overline{RE} | DE | DI | Z | Y |
| X | 1 | 1 | 0 | 1 |
| X | 1 | 0 | 1 | 0 |
| 0 | 0 | X | High-Z | High-Z |
| 1 | 0 | X | High-Z* | High-Z* |

NOTE: *Shutdown Mode (See Note 10), except for ISL83071E/77E

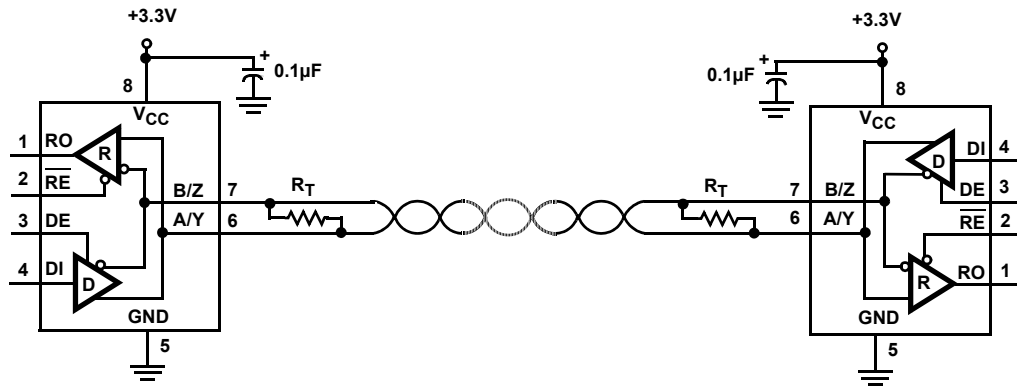
| RECEIVING | | | | |
|-----------------|-------------------|-------------------|------------------------|---------|
| INPUTS | | | | OUTPUT |
| \overline{RE} | DE Half Duplex | DE Full Duplex | A-B | RO |
| 0 | 0 | X | $\geq -0.05V$ | 1 |
| 0 | 0 | X | $\leq -0.2V$ | 0 |
| 0 | 0 | X | Inputs Open/Shorted | 1 |
| 1 | 0 | 0 | X | High-Z* |
| 1 | 1 | 1 | X | High-Z |

NOTE: *Shutdown Mode (See Note 10), except for ISL83071E/77E

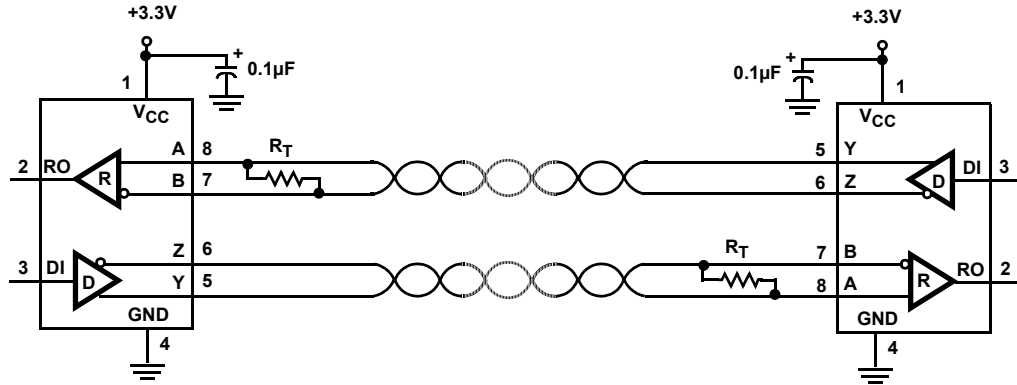
Pin Descriptions

| PIN | FUNCTION |
|------------------------|---|
| RO | Receiver output: If $A - B \geq -50\text{mV}$, RO is high; If $A - B \leq -200\text{mV}$, RO is low; RO = High if A and B are unconnected (floating) or shorted. |
| $\overline{\text{RE}}$ | Receiver output enable. RO is enabled when $\overline{\text{RE}}$ is low; RO is high impedance when $\overline{\text{RE}}$ is high. If the Rx enable function isn't required, connect $\overline{\text{RE}}$ directly to GND or through a $1\text{k}\Omega$ to $3\text{k}\Omega$ resistor to GND. |
| DE | Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high, and are high impedance when DE is low. If the Tx enable function isn't required, connect DE to V_{CC} through a $1\text{k}\Omega$ to $3\text{k}\Omega$ resistor. |
| DI | Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low. |
| GND | Ground connection. |
| A/Y | $\pm 15\text{kV}$ HBM ESD Protected RS-485/RS-422 level, noninverting receiver input and noninverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1. |
| B/Z | $\pm 15\text{kV}$ HBM ESD Protected RS-485/RS-422 level, Inverting receiver input and inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1. |
| A | $\pm 15\text{kV}$ HBM ESD Protected RS-485/RS-422 level, noninverting receiver input. |
| B | $\pm 15\text{kV}$ HBM ESD Protected RS-485/RS-422 level, inverting receiver input. |
| Y | $\pm 15\text{kV}$ HBM ESD Protected RS-485/RS-422 level, noninverting driver output. |
| Z | $\pm 15\text{kV}$ HBM ESD Protected RS-485/RS-422 level, inverting driver output. |
| V_{CC} | System power supply input (3.0V to 3.6V). |
| NC | No Connection. |

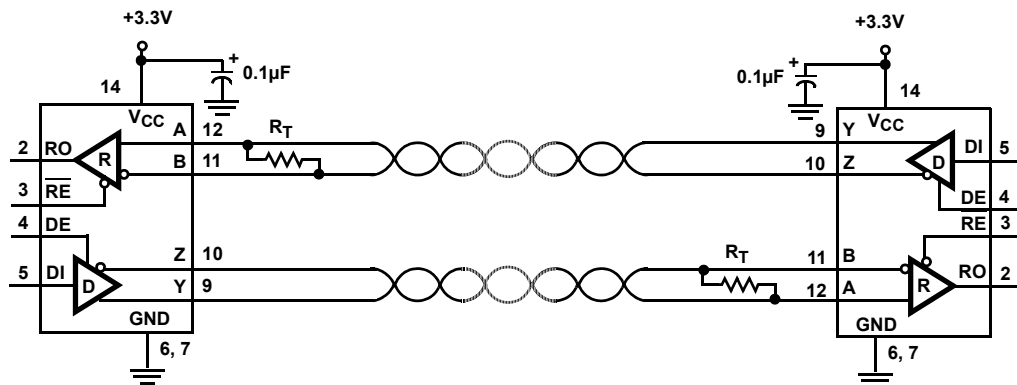
Typical Operating Circuits



ISL83072E, ISL83075E, ISL83078E



ISL83071E, ISL83077E



ISL83070E, ISL83073E, ISL83076E

Absolute Maximum Ratings

V_{CC} to Ground 7V

Input Voltages

DI -0.3V to 7V

DE, RE (Note 20) -0.3V to 7V

Input/Output Voltages

A, B, Y, Z -9V to +13V

RO -0.3V to (V_{CC} +0.3V)

Short Circuit Duration

Y, Z Continuous

ESD Rating See Specification Table

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)

8 Ld SOIC Package 105

8 Ld MSOP Package 140

14 Ld SOIC Package 128

Maximum Junction Temperature (Plastic Package) +150°C

Maximum Storage Temperature Range -65°C to +150°C

Pb-free reflow profile see link below

<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

Operating Conditions

Temperature Range -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

- 4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.

Electrical Specifications Test Conditions: V_{CC} = 3.0V to 3.6V; Unless Otherwise Specified. Typicals are at V_{CC} = 3.3V, T_A = +25°C (Note 5).

| PARAMETER | SYMBOL | TEST CONDITIONS | TEMP (°C) | MIN (Note 19) | TYP | MAX (Note 19) | UNITS | |
|---|-------------------|--|-----------------------|---------------|------|-----------------|-------|----|
| DC CHARACTERISTICS | | | | | | | | |
| Driver Differential V _{OUT} | V _{OD} | R _L = 100Ω (RS-422) (Figure 1A, Note 16) | Full | 2 | 2.3 | - | V | |
| | | R _L = 54Ω (RS-485) (Figure 1A) | Full | 1.5 | 2 | V _{CC} | V | |
| | | No Load | | - | - | V _{CC} | | |
| | | R _L = 60Ω, -7V ≤ V _{CM} ≤ 12V (Figure 1B) | Full | 1.5 | 2.2 | - | V | |
| Change in Magnitude of Driver Differential V _{OUT} for Complementary Output States | ΔV _{OD} | R _L = 54Ω or 100Ω (Figure 1A) | Full | - | 0.01 | 0.2 | V | |
| Driver Common-Mode V _{OUT} | V _{OC} | R _L = 54Ω or 100Ω (Figure 1A) | Full | - | 2 | 3 | V | |
| Change in Magnitude of Driver Common-Mode V _{OUT} for Complementary Output States | ΔV _{OC} | R _L = 54Ω or 100Ω (Figure 1A) | Full | - | 0.01 | 0.2 | V | |
| Logic Input High Voltage | V _{IH} | DI, DE, RE | Full | 2 | - | - | V | |
| Logic Input Low Voltage | V _{IL} | DI, DE, RE | Full | - | - | 0.8 | V | |
| Logic Input Hysteresis | V _{HYS} | DE, RE, (Note 15) | 25 | - | 100 | - | mV | |
| Logic Input Current | I _{IN1} | DI = DE = RE = 0V or V _{CC} . (Note 18) | Full | -2 | - | 2 | μA | |
| Input Current (A, B, A/Y, B/Z) | I _{IN2} | DE = 0V, V _{CC} = 0V or 3.6V | V _{IN} = 12V | Full | - | 80 | 125 | μA |
| | | | V _{IN} = -7V | Full | -100 | -50 | - | μA |
| Output Leakage Current (Y, Z) (Full Duplex Versions Only, Note 13) | I _{IN3} | RE = 0V, DE = 0V, V _{CC} = 0V or 3.6V | V _{IN} = 12V | Full | - | 10 | 40 | μA |
| | | | V _{IN} = -7V | Full | -40 | -10 | - | μA |
| Output Leakage Current (Y, Z) in Shutdown Mode (Full Duplex, Note 13) | I _{IN4} | RE = V _{CC} , DE = 0V, V _{CC} = 0V or 3.6V | V _{IN} = 12V | Full | - | 10 | 40 | μA |
| | | | V _{IN} = -7V | Full | -40 | -10 | - | μA |
| Driver Short-Circuit Current, V _O = High or Low | I _{OSD1} | DE = V _{CC} , -7V ≤ V _Y or V _Z ≤ 12V (Note 7) | Full | - | - | ±250 | mA | |
| Receiver Differential Threshold Voltage | V _{TH} | -7V ≤ V _{CM} ≤ 12V | Full | -200 | -125 | -50 | mV | |
| Receiver Input Hysteresis | ΔV _{TH} | V _{CM} = 0V | 25 | - | 15 | - | mV | |

Electrical Specifications Test Conditions: $V_{CC} = 3.0V$ to $3.6V$; Unless Otherwise Specified. Typical values are at $V_{CC} = 3.3V$, $T_A = +25^\circ C$ (Note 5). **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | TEMP (°C) | MIN (Note 19) | TYP | MAX (Note 19) | UNITS | |
|--|----------------|---|--|----------------|-----------|---------------|------------|---------|
| Receiver Output High Voltage | V_{OH} | $I_O = -4mA$, $V_{ID} = -50mV$ | Full | $V_{CC} - 0.6$ | - | - | V | |
| Receiver Output Low Voltage | V_{OL} | $I_O = -4mA$, $V_{ID} = -200mV$ | Full | - | 0.17 | 0.4 | V | |
| Three-State (high impedance) Receiver Output Current (Note 13) | I_{OZR} | $0.4V \leq V_O \leq 2.4V$ | Full | -1 | 0.015 | 1 | μA | |
| Receiver Input Resistance | R_{IN} | $-7V \leq V_{CM} \leq 12V$ | Full | 96 | 150 | - | $k\Omega$ | |
| Receiver Short-Circuit Current | I_{OSR} | $0V \leq V_O \leq V_{CC}$ | Full | ± 7 | 30 | ± 60 | mA | |
| Thermal Shutdown Threshold | T_{SD} | | Full | - | 150 | - | $^\circ C$ | |
| SUPPLY CURRENT | | | | | | | | |
| No-Load Supply Current (Note 6) | I_{CC} | $DI = 0V$ or V_{CC} | $\overline{DE} = V_{CC}$, $\overline{RE} = 0V$ or V_{CC} | Full | - | 510 | 800 | μA |
| | | | $DE = 0V$, $\overline{RE} = 0V$ | Full | - | 480 | 700 | μA |
| Shutdown Supply Current (Note 13) | I_{SHDN} | $DE = 0V$, $\overline{RE} = V_{CC}$, $DI = 0V$ or V_{CC} | Full | - | 0.01 | 1 | μA | |
| ESD PERFORMANCE | | | | | | | | |
| RS-485 Pins (A, Y, B, Z) | | Human Body Model (HBM), Pin to GND | 25 | - | ± 15 | - | kV | |
| All Other Pins | | HBM, per MIL-STD-883 Method 3015 | 25 | - | $> \pm 7$ | - | kV | |
| DRIVER SWITCHING CHARACTERISTICS (ISL83070E, ISL83071E, ISL83072E, 250kbps) | | | | | | | | |
| Maximum Data Rate | f_{MAX} | $V_{OD} = \pm 1.5V$, $C_D = 820pF$ (Figure 4, Note 17) | Full | 250 | 800 | - | kbps | |
| Driver Differential Output Delay | t_{DD} | $R_{DIFF} = 54\Omega$, $C_D = 50pF$ (Figure 2) | Full | 250 | 1100 | 1500 | ns | |
| Driver Differential Output Skew | t_{SKEW} | $R_{DIFF} = 54\Omega$, $C_D = 50pF$ (Figure 2) | Full | - | 6 | 100 | ns | |
| Driver Differential Rise or Fall Time | t_R , t_F | $R_{DIFF} = 54\Omega$, $C_D = 50pF$ (Figure 2) | Full | 350 | 960 | 1600 | ns | |
| Driver Enable to Output High | t_{ZH} | $R_L = 500\Omega$, $C_L = 50pF$, $SW = GND$ (Figure 3), (Notes 8, 13) | Full | - | 26 | 600 | ns | |
| Driver Enable to Output Low | t_{ZL} | $R_L = 500\Omega$, $C_L = 50pF$, $SW = V_{CC}$ (Figure 3), (Notes 8, 13) | Full | - | 200 | 600 | ns | |
| Driver Disable from Output High | t_{HZ} | $R_L = 500\Omega$, $C_L = 50pF$, $SW = GND$ (Figure 3), (Note 13) | Full | - | 28 | 55 | ns | |
| Driver Disable from Output Low | t_{LZ} | $R_L = 500\Omega$, $C_L = 50pF$, $SW = V_{CC}$ (Figure 3), (Note 13) | Full | - | 30 | 55 | ns | |
| Time to Shutdown | t_{SHDN} | (Notes 10, 13) | Full | 50 | 200 | 600 | ns | |
| Driver Enable from Shutdown to Output High | $t_{ZH(SHDN)}$ | $R_L = 500\Omega$, $C_L = 50pF$, $SW = GND$ (Figure 3), (Notes 10, 11, 13) | Full | - | 180 | 700 | ns | |
| Driver Enable from Shutdown to Output Low | $t_{ZL(SHDN)}$ | $R_L = 500\Omega$, $C_L = 50pF$, $SW = V_{CC}$ (Figure 3), (Notes 10, 11, 13) | Full | - | 100 | 700 | ns | |
| DRIVER SWITCHING CHARACTERISTICS (ISL83073E, ISL83075E, 500kbps) | | | | | | | | |
| Maximum Data Rate | f_{MAX} | $V_{OD} = \pm 1.5V$, $C_D = 820pF$ (Figure 4, Note 17) | Full | 500 | 1600 | - | kbps | |
| Driver Differential Output Delay | t_{DD} | $R_{DIFF} = 54\Omega$, $C_D = 50pF$ (Figure 2) | Full | 180 | 350 | 800 | ns | |
| Driver Differential Output Skew | t_{SKEW} | $R_{DIFF} = 54\Omega$, $C_D = 50pF$ (Figure 2) | Full | - | 1 | 30 | ns | |
| Driver Differential Rise or Fall Time | t_R , t_F | $R_{DIFF} = 54\Omega$, $C_D = 50pF$ (Figure 2) | Full | 200 | 380 | 800 | ns | |
| Driver Enable to Output High | t_{ZH} | $R_L = 500\Omega$, $C_L = 50pF$, $SW = GND$ (Figure 3), (Notes 8, 13) | Full | - | 26 | 350 | ns | |
| Driver Enable to Output Low | t_{ZL} | $R_L = 500\Omega$, $C_L = 50pF$, $SW = V_{CC}$ (Figure 3), (Notes 8, 13) | Full | - | 100 | 350 | ns | |

Electrical Specifications Test Conditions: $V_{CC} = 3.0V$ to $3.6V$; Unless Otherwise Specified. Typical values are at $V_{CC} = 3.3V$, $T_A = +25^\circ C$ (Note 5). **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | TEMP (°C) | MIN (Note 19) | TYP | MAX (Note 19) | UNITS | |
|---|--------------------|---|---------------|------------------|-----|------------------|-------|------|
| Driver Disable from Output High | t_{HZ} | $R_L = 500\Omega$, $C_L = 50pF$, SW = GND (Figure 3), (Note 13) | Full | - | 28 | 55 | ns | |
| Driver Disable from Output Low | t_{LZ} | $R_L = 500\Omega$, $C_L = 50pF$, SW = V_{CC} (Figure 3), (Note 13) | Full | - | 30 | 55 | ns | |
| Time to Shutdown | t_{SHDN} | (Notes 10, 13) | Full | 50 | 200 | 600 | ns | |
| Driver Enable from Shutdown to Output High | $t_{ZH(SHDN)}$ | $R_L = 500\Omega$, $C_L = 50pF$, SW = GND (Figure 3), (Notes 10, 11, 13) | Full | - | 180 | 700 | ns | |
| Driver Enable from Shutdown to Output Low | $t_{ZL(SHDN)}$ | $R_L = 500\Omega$, $C_L = 50pF$, SW = V_{CC} (Figure 3), (Notes 10, 11, 13) | Full | - | 100 | 700 | ns | |
| DRIVER SWITCHING CHARACTERISTICS (ISL83076E, ISL83077E, ISL83078E, 20Mbps) | | | | | | | | |
| Maximum Data Rate | f_{MAX} | $V_{OD} = \pm 1.5V$, $C_D = 350pF$ (Figure 4, Note 17) | Full | 20 | 28 | - | Mbps | |
| Driver Differential Output Delay | t_{DD} | $R_{DIFF} = 54\Omega$, $C_D = 50pF$ (Figure 2) | Full | - | 27 | 40 | ns | |
| Driver Differential Output Skew | t_{SKEW} | $R_{DIFF} = 54\Omega$, $C_D = 50pF$ (Figure 2) | Full | - | 1 | 3 | ns | |
| Driver Output Skew, Part-to-Part | Δt_{DSKEW} | $R_{DIFF} = 54\Omega$, $C_D = 50pF$ (Figure 2, Note 14) | Full | - | - | 11 | ns | |
| Driver Differential Rise or Fall Time | t_R, t_F | $R_{DIFF} = 54\Omega$, $C_D = 50pF$ (Figure 2) | Full | - | 9 | 15 | ns | |
| Driver Enable to Output High | t_{ZH} | $R_L = 500\Omega$, $C_L = 50pF$, SW = GND (Figure 3), (Notes 8, 13) | Full | - | 17 | 50 | ns | |
| Driver Enable to Output Low | t_{ZL} | $R_L = 500\Omega$, $C_L = 50pF$, SW = V_{CC} (Figure 3), (Notes 8, 13) | Full | - | 16 | 40 | ns | |
| Driver Disable from Output High | t_{HZ} | $R_L = 500\Omega$, $C_L = 50pF$, SW = GND (Figure 3), (Note 13) | Full | - | 25 | 40 | ns | |
| Driver Disable from Output Low | t_{LZ} | $R_L = 500\Omega$, $C_L = 50pF$, SW = V_{CC} (Figure 3), (Note 13) | Full | - | 28 | 50 | ns | |
| Time to Shutdown | t_{SHDN} | (Notes 10, 13) | Full | 50 | 200 | 600 | ns | |
| Driver Enable from Shutdown to Output High | $t_{ZH(SHDN)}$ | $R_L = 500\Omega$, $C_L = 50pF$, SW = GND (Figure 3), (Notes 10, 11, 13) | Full | - | 180 | 700 | ns | |
| Driver Enable from Shutdown to Output Low | $t_{ZL(SHDN)}$ | $R_L = 500\Omega$, $C_L = 50pF$, SW = V_{CC} (Figure 3), (Notes 10, 11, 13) | Full | - | 90 | 700 | ns | |
| RECEIVER SWITCHING CHARACTERISTICS (All Versions) | | | | | | | | |
| Maximum Data Rate | f_{MAX} | $V_{ID} = \pm 1.5V$ (Note 17) | ISL83070E-75E | Full | 12 | 20 | - | Mbps |
| | | | ISL83076E-78E | Full | 20 | 35 | - | Mbps |
| Receiver Input to Output Delay | t_{PLH}, t_{PHL} | (Figure 5) | ISL83070E-75E | Full | 25 | 70 | 120 | ns |
| | | | ISL83076E-78E | Full | 25 | 33 | 60 | ns |
| Receiver Skew $t_{PLH} - t_{PHL}$ | t_{SKD} | (Figure 5) | Full | - | 1.5 | 4 | ns | |
| Receiver Skew, Part-to-Part | Δt_{RSKEW} | (Figure 5, Note 14) | Full | - | - | 15 | ns | |
| Receiver Enable to Output High | t_{ZH} | $R_L = 1k\Omega$, $C_L = 15pF$, SW = GND (Figure 6), (Notes 9, 13) | ISL83070E-75E | Full | 5 | 15 | 20 | ns |
| | | | ISL83076E-78E | Full | 5 | 11 | 17 | ns |
| Receiver Enable to Output Low | t_{ZL} | $R_L = 1k\Omega$, $C_L = 15pF$, SW = V_{CC} (Figure 6), (Notes 9, 13) | ISL83070E-75E | Full | 5 | 15 | 20 | ns |
| | | | ISL83076E-78E | Full | 5 | 11 | 17 | ns |
| Receiver Disable from Output High | t_{HZ} | $R_L = 1k\Omega$, $C_L = 15pF$, SW = GND (Figure 6), (Note 13) | ISL83070E-75E | Full | 5 | 12 | 20 | ns |
| | | | ISL83076E-78E | Full | 4 | 7 | 15 | ns |

Electrical Specifications Test Conditions: $V_{CC} = 3.0V$ to $3.6V$; Unless Otherwise Specified. Typical values are at $V_{CC} = 3.3V$, $T_A = +25^\circ C$ (Note 5). **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | TEMP (°C) | MIN (Note 19) | TYP | MAX (Note 19) | UNITS | |
|--|----------------|--|---------------|---------------|-----|---------------|-------|----|
| Receiver Disable from Output Low | t_{LZ} | $R_L = 1k\Omega$, $C_L = 15pF$, $SW = V_{CC}$ (Figure 6), (Note 13) | ISL83070E-75E | Full | 5 | 13 | 20 | ns |
| | | | ISL83076E-78E | Full | 4 | 7 | 15 | ns |
| Time to Shutdown | t_{SHDN} | (Notes 10, 13) | Full | 50 | 180 | 600 | ns | |
| Receiver Enable from Shutdown to Output High | $t_{ZH}(SHDN)$ | $R_L = 1k\Omega$, $C_L = 15pF$, $SW = GND$ (Figure 6), (Notes 10, 12, 13) | Full | - | 240 | 500 | ns | |
| Receiver Enable from Shutdown to Output Low | $t_{ZL}(SHDN)$ | $R_L = 1k\Omega$, $C_L = 15pF$, $SW = V_{CC}$ (Figure 6), (Notes 10, 12, 13) | Full | - | 240 | 500 | ns | |

NOTES:

- All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
- Supply current specification is valid for loaded drivers when $DE = 0V$.
- Applies to peak current. See "Typical Performance Curves" for more information.
- When testing devices with the shutdown feature, keep $\overline{RE} = 0$ to prevent the device from entering SHDN.
- When testing devices with the shutdown feature, the \overline{RE} signal high time must be short enough (typically $<100ns$) to prevent the device from entering SHDN.
- Versions with a shutdown feature are put into shutdown by bringing \overline{RE} high and DE low. If the inputs are in this state for less than $50ns$, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least $600ns$, the parts are guaranteed to have entered shutdown. See "Low Power Shutdown Mode" on page 11.
- Keep $\overline{RE} = V_{CC}$, and set the DE signal low time $>600ns$ to ensure that the device enters SHDN.
- Set the \overline{RE} signal high time $>600ns$ to ensure that the device enters SHDN.
- Does not apply to the ISL83071E and ISL83077E.
- Δt_{SKEW} is the magnitude of the difference in propagation delays of the specified terminals of two units tested with identical test conditions (V_{CC} , temperature, etc.). Only applies to the ISL83076E - 78E.
- ISL83070E - ISL83075E only.
- $V_{CC} \geq 3.15V$
- Limits established by characterization and are not production tested.
- If the Tx or Rx enable function isn't needed, connect the enable pin to the appropriate supply (see "Pin Descriptions" table) through a $1k\Omega$ to $3k\Omega$ resistor.
- Parts are 100% tested at $+25^\circ C$. Full temperature limits are guaranteed by bench and tester characterization.
- If the DE or \overline{RE} input voltage exceeds the V_{CC} voltage by more than $500mV$, then current will flow into the logic pin. The current is limited by a 340Ω resistor (so $\approx 13mA$ with $V_{IN} = 5V$ and $V_{CC} = 0V$) so no damage will occur if $V_{CC} \leq V_{IN} \leq 7V$ for short periods of time.

Test Circuits and Waveforms

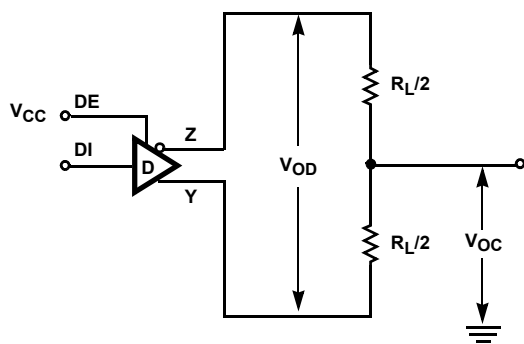


FIGURE 1A. V_{OD} AND V_{OC}

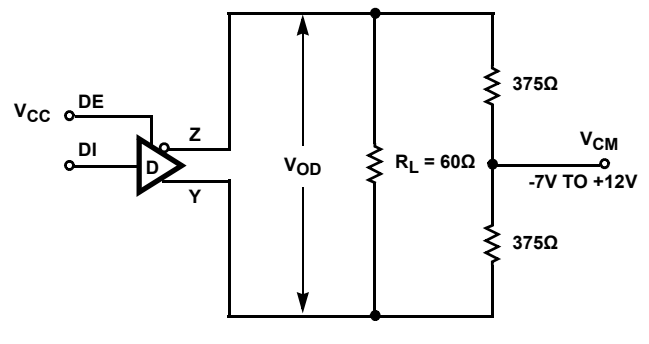


FIGURE 1B. V_{OD} WITH COMMON MODE LOAD

FIGURE 1. DC DRIVER TEST CIRCUITS

Test Circuits and Waveforms (Continued)

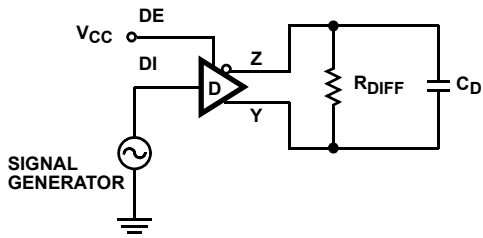


FIGURE 2A. TEST CIRCUIT

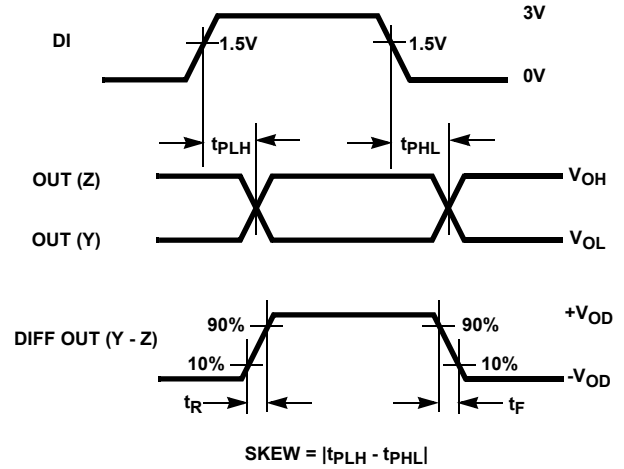
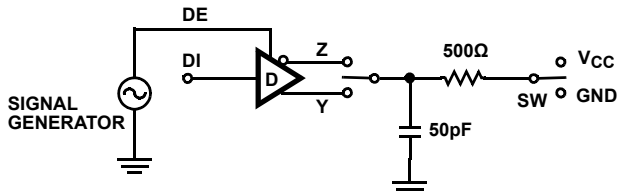


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



| PARAMETER | OUTPUT | RE | DI | SW |
|----------------|--------|-------------|-----|----------|
| t_{HZ} | Y/Z | X | 1/0 | GND |
| t_{LZ} | Y/Z | X | 0/1 | V_{CC} |
| t_{ZH} | Y/Z | 0 (Note 8) | 1/0 | GND |
| t_{ZL} | Y/Z | 0 (Note 8) | 0/1 | V_{CC} |
| $t_{ZH(SHDN)}$ | Y/Z | 1 (Note 11) | 1/0 | GND |
| $t_{ZL(SHDN)}$ | Y/Z | 1 (Note 11) | 0/1 | V_{CC} |

FIGURE 3A. TEST CIRCUIT

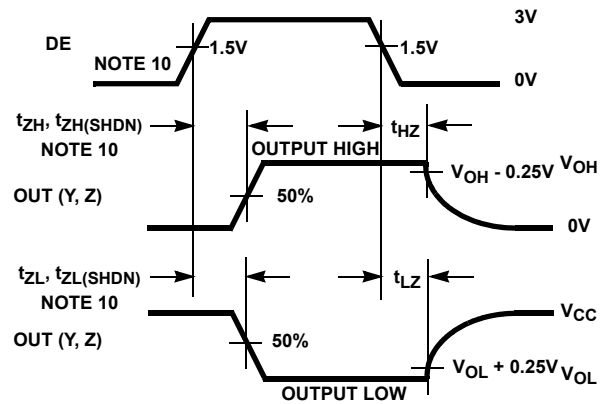


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES (EXCEPT ISL83071E, ISL83077E)

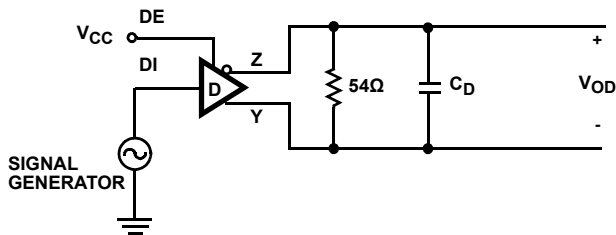


FIGURE 4A. TEST CIRCUIT

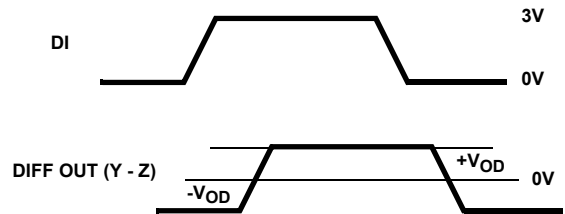


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. DRIVER DATA RATE

Test Circuits and Waveforms (Continued)

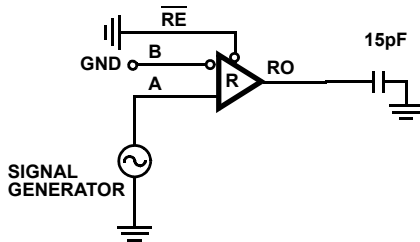


FIGURE 5A. TEST CIRCUIT

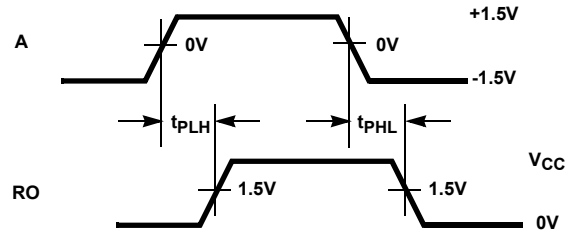
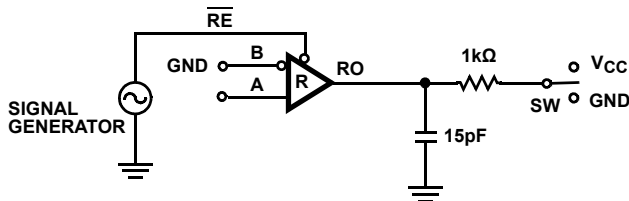


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER PROPAGATION DELAY



| PARAMETER | DE | A | SW |
|--------------------------|----|-------|----------|
| t_{HZ} | X | +1.5V | GND |
| t_{LZ} | X | -1.5V | V_{CC} |
| t_{ZH} (Note 9) | 0 | +1.5V | GND |
| t_{ZL} (Note 9) | 0 | -1.5V | V_{CC} |
| $t_{ZH(SHDN)}$ (Note 12) | 0 | +1.5V | GND |
| $t_{ZL(SHDN)}$ (Note 12) | 0 | -1.5V | V_{CC} |

FIGURE 6A. TEST CIRCUIT

FIGURE 6. RECEIVER ENABLE AND DISABLE TIMES (EXCEPT ISL83071E, ISL83077E)

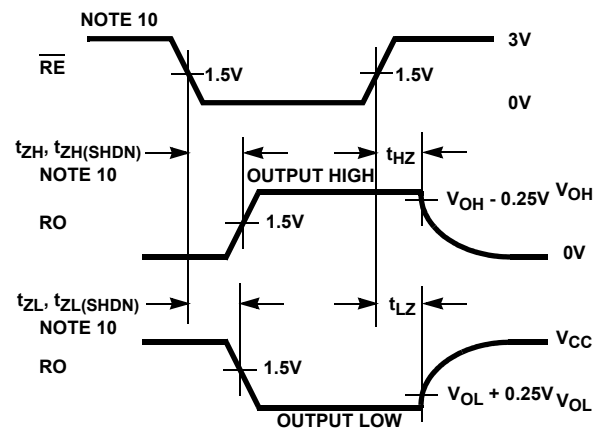


FIGURE 6B. MEASUREMENT POINTS

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 spec requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended common mode range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000', so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

Receiver Features

These devices utilize a differential input receiver for maximum noise immunity and common mode rejection. Input sensitivity is better than $\pm 200\text{mV}$, as required by the RS-422 and RS-485 specifications.

Receiver input resistance of $96\text{k}\Omega$ surpasses the RS-422 spec of $4\text{k}\Omega$, and is eight times the RS-485 "Unit Load (UL)" requirement of $12\text{k}\Omega$ minimum. Thus, these products are known as "one-eighth UL" transceivers, and there can be up to 256 of these devices on a network while still complying with the RS-485 loading spec.

Receiver inputs function with common mode voltages as great as +9V/-7V outside the power supplies (i.e., +12V and -7V), making them ideal for long networks where induced voltages, and ground potential differences, are realistic concerns.

All the receivers include a "full fail-safe" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating) or shorted. Fail-safe with shorted inputs is achieved by setting the Rx upper switching point to -50mV, thereby ensuring that the Rx sees 0V differential as a high input level.

Receivers easily meet the data rates supported by the corresponding driver, and all receiver outputs (except on the ISL83071E and ISL83077E) are tri-statable via the active low \overline{RE} input.

Driver Features

The RS-485, RS-422 driver is a differential output device that delivers at least 1.5V across a 54 Ω load (RS-485), and at least 2V across a 100 Ω load (RS-422). The drivers feature low propagation delay skew to maximize bit width, and to minimize EMI.

All drivers are tri-statable via the active high DE input, except on the ISL83071E and ISL83077E.

The 250kbps and 500kbps driver outputs are slew rate limited to minimize EMI, and to reduce reflections in unterminated or improperly terminated networks. Outputs of the ISL83076E through ISL83078E drivers are not limited, so faster output transition times allow data rates of at least 20Mbps.

Hot Plug Function

When a piece of equipment powers up, there is a period of time where the processor or ASIC driving the RS-485 control lines (DE, \overline{RE}) is unable to ensure that the RS-485 Tx and Rx outputs are kept disabled. If the equipment is connected to the bus, a driver activating prematurely during power up may crash the bus. To avoid this scenario, the ISL8307XE versions with output enable pins incorporate a "Hot Plug" function. During power up, circuitry monitoring V_{CC} ensures that the Tx and Rx outputs remain disabled for a period of time, regardless of the state of DE and \overline{RE} . This gives the processor/ASIC a chance to stabilize and drive the RS-485 control lines to the proper states.

ESD Protection

All pins on these devices include class 3 (>7kV) Human Body Model (HBM) ESD protection structures, but the RS-485 pins (driver outputs and receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of ± 15 kV HBM. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, protect without allowing any latchup mechanism to activate, and without degrading the RS-485 common mode range of -7V to +12V. This built-in ESD protection eliminates the need for board level protection structures (e.g., transient suppression diodes), and the associated, undesirable capacitive load they present.

Data Rate, Cables, and Terminations

RS-485, RS-422 are intended for network lengths up to 4000', but the maximum system data rate decreases as the transmission length increases. Devices operating at 20Mbps are limited to lengths less than 100', while the 250kbps

versions can operate at full data rates with lengths of several thousand feet.

Twisted pair is the cable of choice for RS-485, RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative, when using the 20Mbps devices, to minimize reflections. Short networks using the 250kbps versions need not be terminated, but, terminations are recommended unless power dissipation is an overriding concern.

In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120 Ω) at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

Built-In Driver Overload Protection

As stated previously, the RS-485 spec requires that drivers survive worst case bus contentions undamaged. These devices meet this requirement via driver output short circuit current limits, and on-chip thermal shutdown circuitry.

The driver output stages incorporate short circuit current limiting circuitry which ensures that the output current never exceeds the RS-485 spec, even at the common mode voltage range extremes. Additionally, these devices utilize a foldback circuit which reduces the short circuit current, and thus the power dissipation, whenever the contending voltage exceeds either supply.

In the event of a major short circuit condition, devices also include a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about +15°. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

Low Power Shutdown Mode

These CMOS transceivers all use a fraction of the power required by their bipolar counterparts, but some also include a shutdown feature that reduces the already low quiescent I_{CC} to a 10nA trickle. These devices enter shutdown whenever the receiver and driver are **simultaneously** disabled ($\overline{RE} = V_{CC}$ and DE = GND) for a period of at least 600ns. Disabling both the driver and the receiver for less than 50ns guarantees that the transceiver will not enter shutdown.

Note that receiver and driver enable times increase when the transceiver enables from shutdown. Refer to Notes 8 through 12, at the end of the "Electrical Specifications" table on page 8 for more information.

Typical Performance Curves $V_{CC} = 3.3V$, $T_A = +25^\circ C$; Unless Otherwise Specified

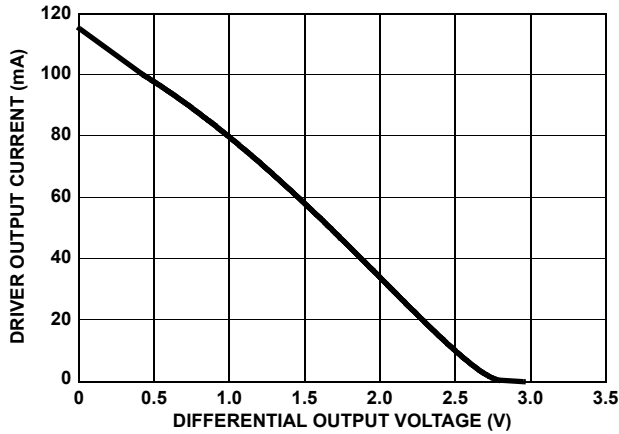


FIGURE 7. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

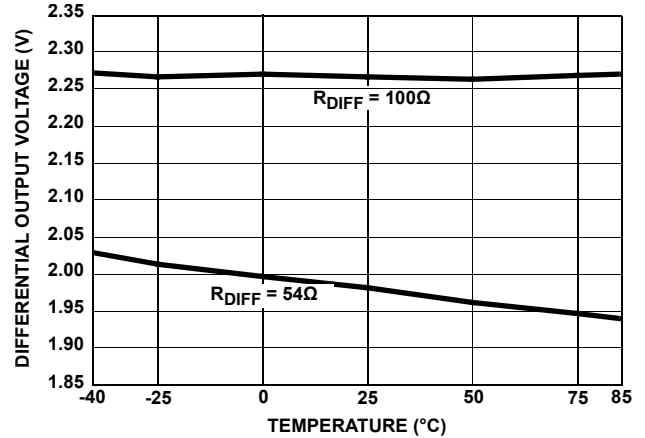


FIGURE 8. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

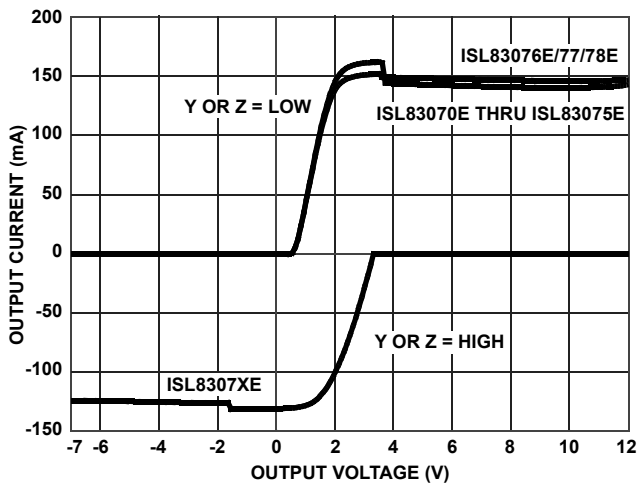


FIGURE 9. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

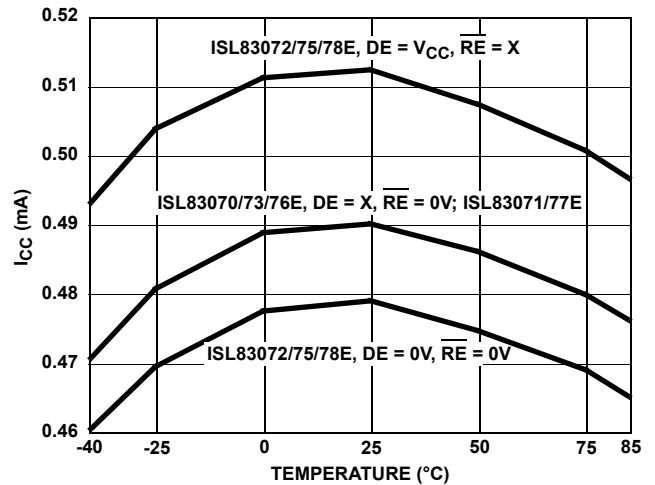


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

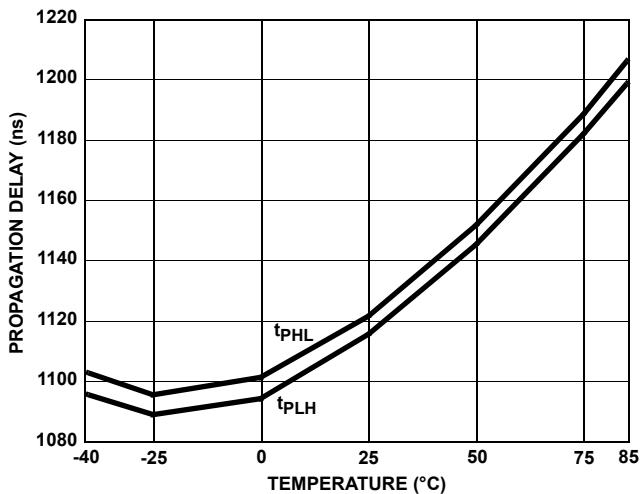


FIGURE 11. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL83070E, ISL83071E, ISL83072E)

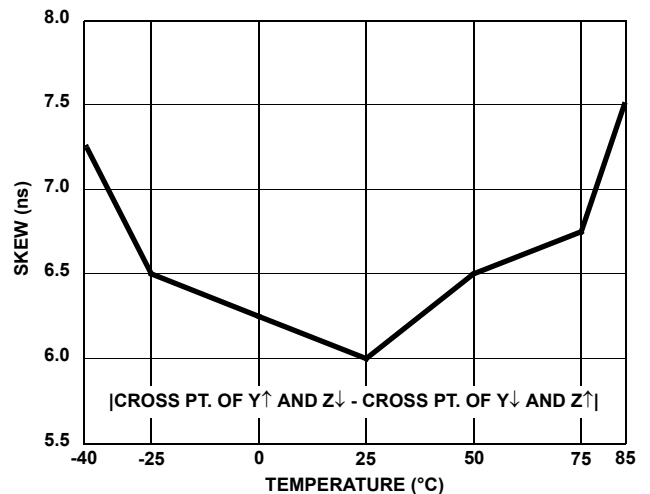


FIGURE 12. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL83070E, ISL83071E, ISL83072E)

Typical Performance Curves $V_{CC} = 3.3V$, $T_A = +25^\circ C$; Unless Otherwise Specified (Continued)

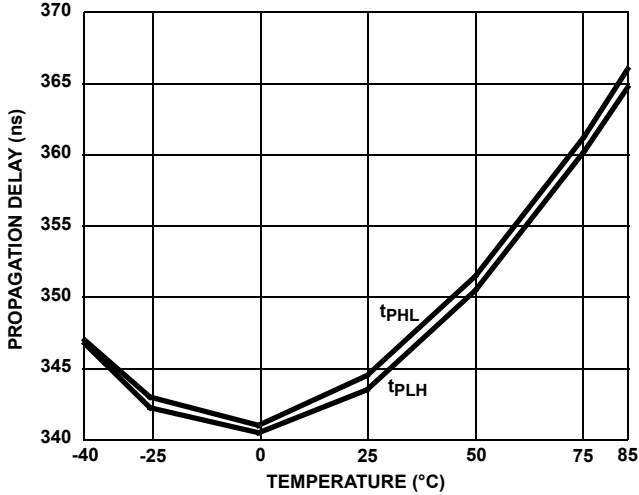


FIGURE 13. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL83073E, ISL83075E)

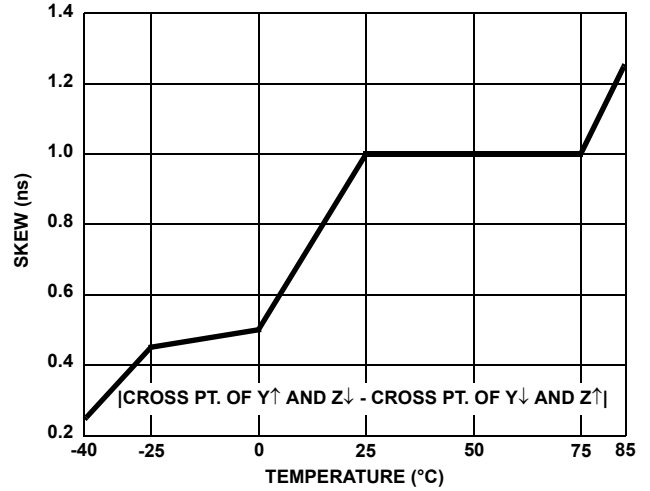


FIGURE 14. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL83073E, ISL83075E)

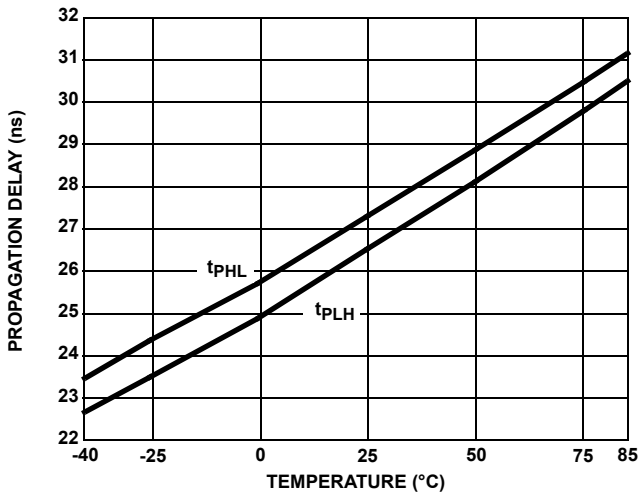


FIGURE 15. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL83076E, ISL83077E, ISL83078E)

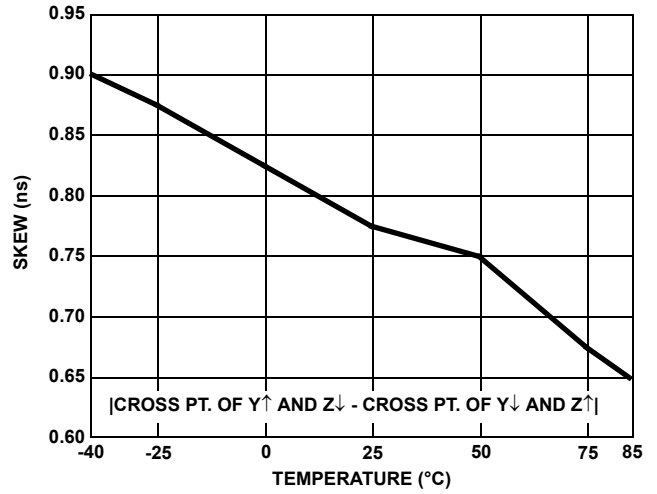


FIGURE 16. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL83076E, ISL83077E, ISL83078E)

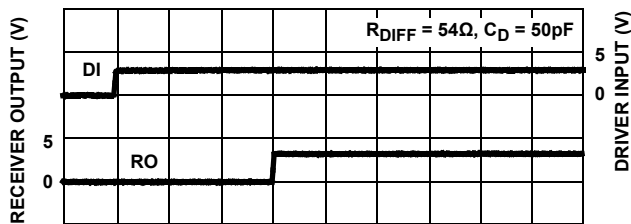


FIGURE 17. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL83070E, ISL83071E, ISL83072E)

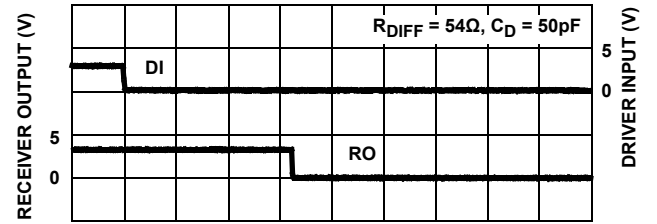


FIGURE 18. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL83070E, ISL83071E, ISL83072E)

Typical Performance Curves $V_{CC} = 3.3V$, $T_A = +25^\circ C$; Unless Otherwise Specified (Continued)

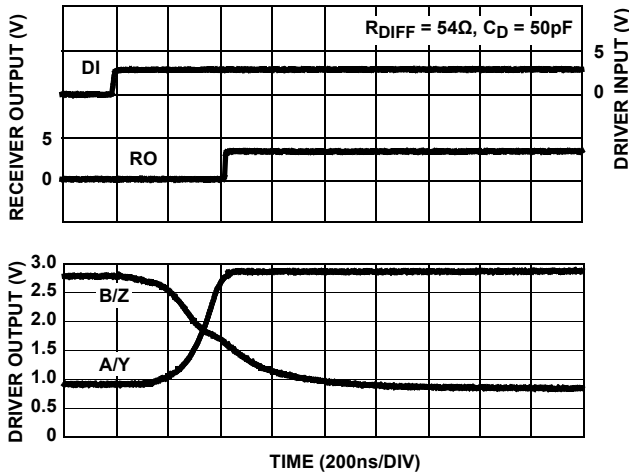


FIGURE 19. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL83073E, ISL83075E)

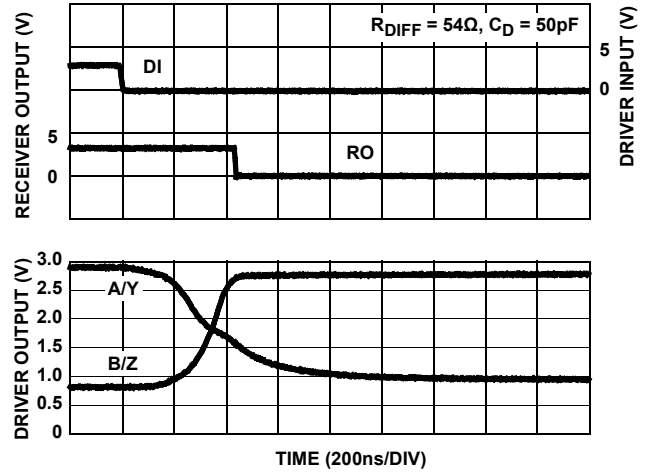


FIGURE 20. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL83073E, ISL83075E)

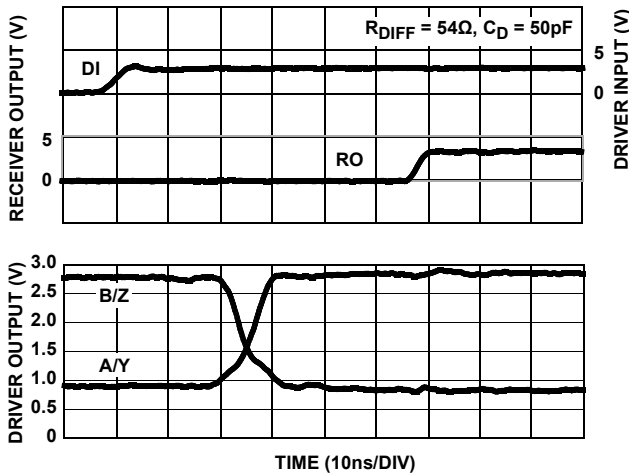


FIGURE 21. DRIVER AND RECEIVER WAVEFORMS, LOW TO HIGH (ISL83076E, ISL83077E, ISL83078E)

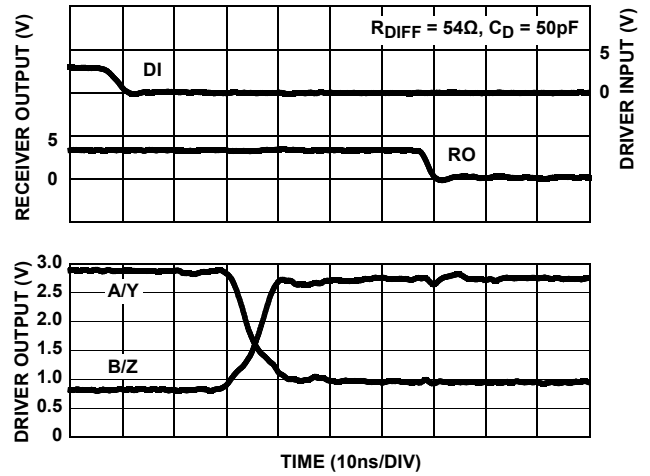


FIGURE 22. DRIVER AND RECEIVER WAVEFORMS, HIGH TO LOW (ISL83076E, ISL83077E, ISL83078E)

Typical Performance Curves $V_{CC} = 3.3V$, $T_A = +25^\circ C$; Unless Otherwise Specified (Continued)

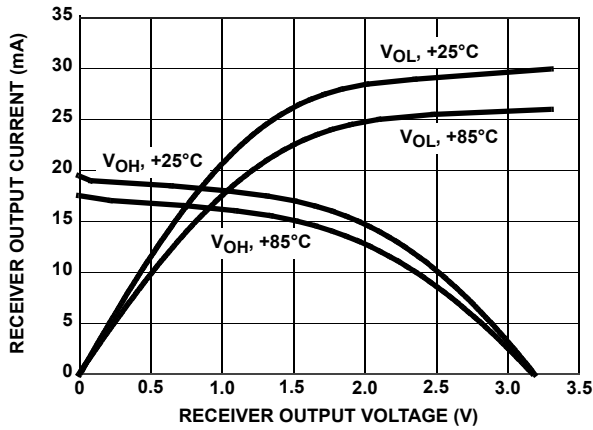


FIGURE 23. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

535

PROCESS:

Si Gate BiCMOS

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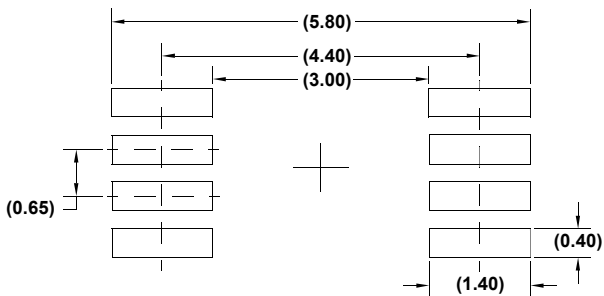
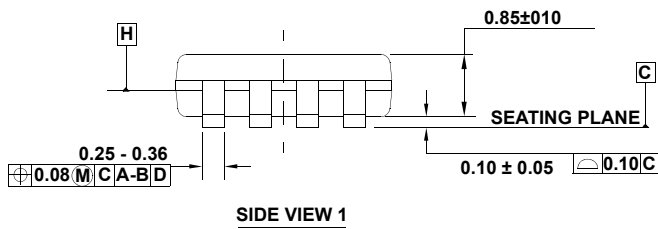
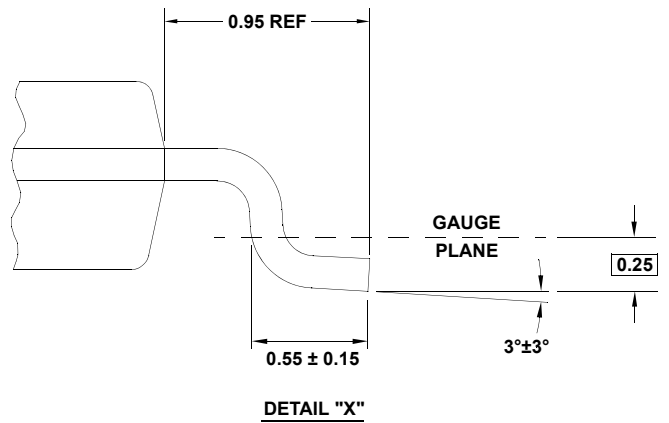
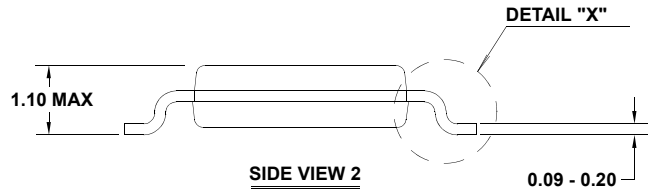
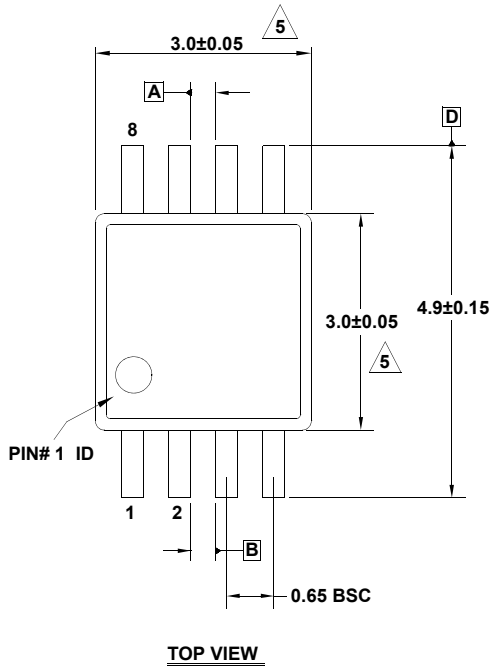
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Package Outline Drawing

M8.118

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 7/11



NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.

5. Dimensions are measured at Datum Plane "H".

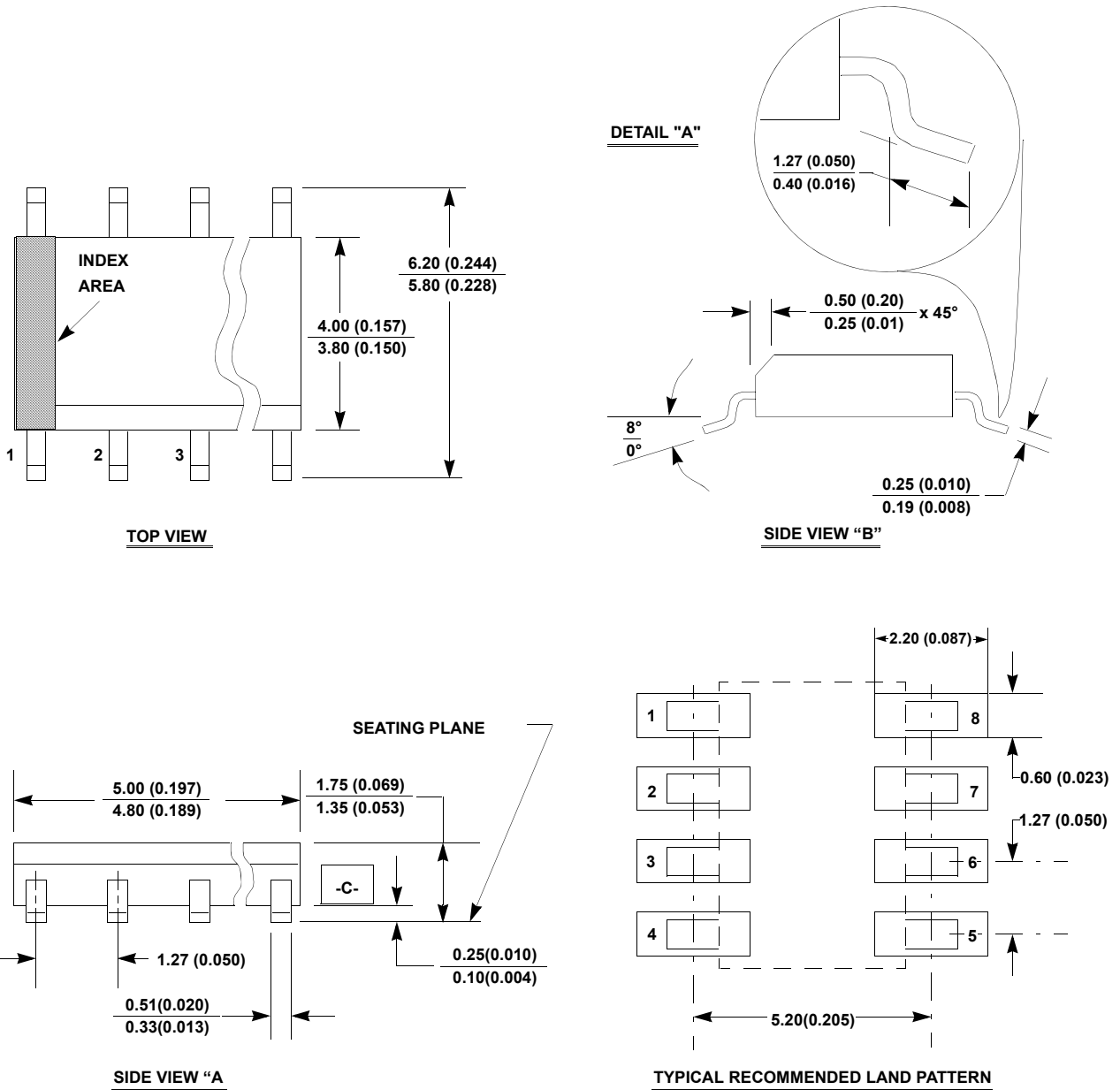
6. Dimensions in () are for reference only.

Package Outline Drawing

M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 1/12



NOTES:

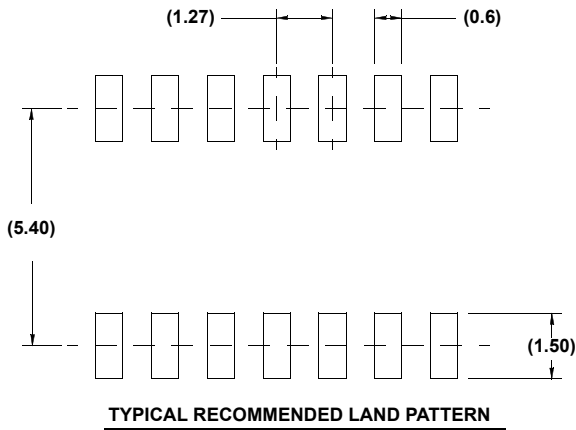
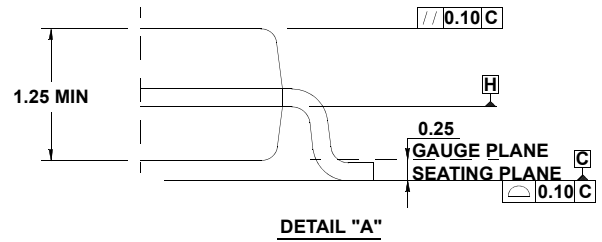
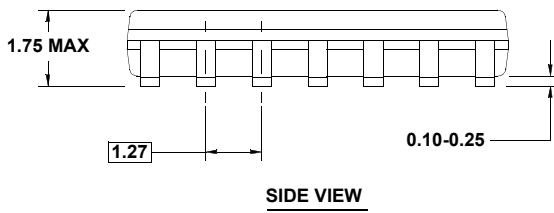
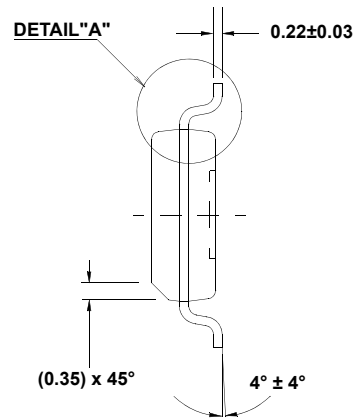
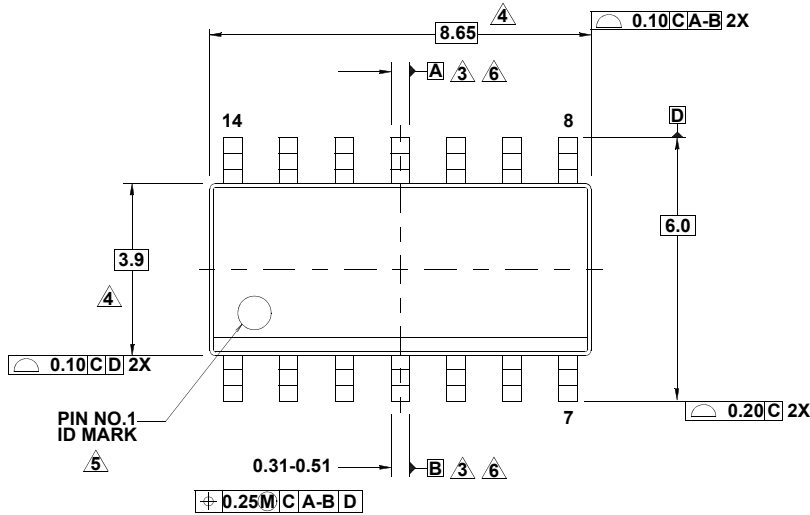
1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Package Outline Drawing

M14.15

14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

Rev 1, 10/09



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions.
Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.

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