# THE DATASHEET OF

# ISL6605CBZ-T

# ISL6605

Synchronous Rectified MOSFET Driver

FN9091
Rev 7.00
May 9, 2006

The ISL6605 is a high frequency, MOSFET driver optimized to drive two N-Channel power MOSFETs in a synchronous-rectified buck converter topology. This driver combined with an Intersil HIP63xx or ISL65xx Multi-Phase Buck PWM controller forms a complete single-stage core-voltage regulator solution with high efficiency performance at high switching frequency for advanced microprocessors.

The IC is biased by a single low voltage supply (5V) and minimizes low driver switching losses for high MOSFET gate capacitance and high switching frequency applications. Each driver is capable of driving a 3000pF load with an 8ns propagation delay and less than 10ns transition time. This product implements bootstrapping on the upper gate with an internal bootstrap Schottky diode, reducing implementation cost, complexity, and allowing the use of higher performance, cost effective N-Channel MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

The ISL6605 features 4A typical sink current for the lower gate driver, which is capable of holding the lower MOSFET gate during the Phase node rising edge to prevent shoot-through power loss caused by the high dv/dt of the Phase node.

The ISL6605 also features a Three-State PWM input that, working together with Intersil multi-phase PWM controllers, will prevent a negative transient on the output voltage when the output is being shut down. This feature eliminates the Schottky diode that is usually seen in a microprocessor power system for protecting the microprocessor from reversed-output-voltage damage.

## Features

- Drives Two N-Channel MOSFETs
- Adaptive Shoot-Through Protection
- 0.4Ω On-Resistance and 4A Sink Current Capability
- Supports High Switching Frequency
  - Fast Output Rise and Fall Time
  - Ultra Low Propagation Delay 8ns
- Three-State PWM Input for Power Stage Shutdown
- Internal Bootstrap Schottky Diode
- Low Bias Supply Current (5V, 30µA)
- Enable Input
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN-Quad Flat No Leads-Product Outline.
  - Near Chip-Scale Package Footprint; Improves PCB Efficiency and Thinner in Profile.
- Pb-Free Plus Anneal Available (RoHS Compliant)

## Applications

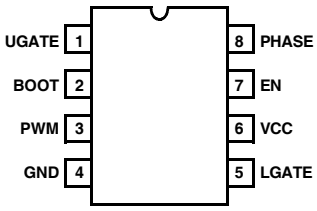
- Core Voltage Supplies for Intel® and AMD® Microprocessors
- High Frequency Low Profile DC/DC Converters
- High Current Low Voltage DC/DC Converters
- Synchronous Rectification for Isolated Power Supplies

## Related Literature

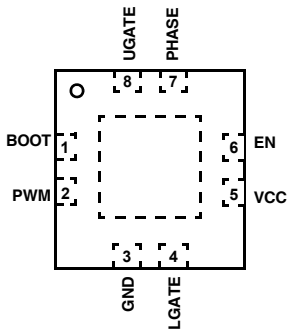
- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

## Pinouts

**ISL6605**
**(8 LD SOIC)**
TOP VIEW




**ISL6605**
**(8 LD QFN)**
TOP VIEW



## Ordering Information

| PART NUMBER* | PART MARKING | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|---|
| ISL6605CB | ISL6605CB | 0 to 70 | 8 Ld SOIC | M8.15 |
| ISL6605CBZ (Note) | ISL6605CBZ | 0 to 70 | 8 Ld SOIC (Pb-free) | M8.15 |
| ISL6605CBZA (Note) | ISL6605CBZ | 0 to 70 | 8 Ld SOIC (Pb-free) | M8.15 |
| ISL6605CR | 605C | 0 to 70 | 8 Ld 3x3 QFN | L8.3x3 |
| ISL6605CRZ (Note) | 05CZ | 0 to 70 | 8 Ld 3x3 QFN (Pb-free) | L8.3x3 |
| ISL6605CRZA (Note) | 05CZ | 0 to 70 | 8 Ld 3x3 QFN (Pb-free) | L8.3x3 |
| ISL6605IB | ISL6605IB | -40 to 85 | 8 Ld SOIC | M8.15 |
| ISL6605IBZ (Note) | 6605IBZ | -40 to 85 | 8 Ld SOIC (Pb-free) | M8.15 |

## Ordering Information

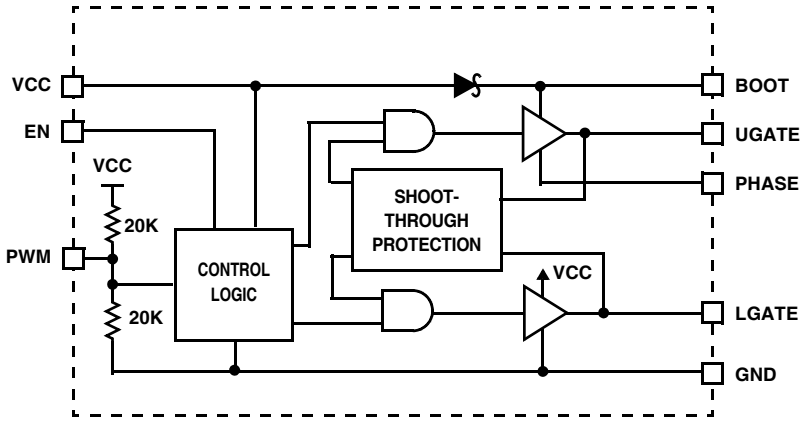
| PART NUMBER* | PART MARKING | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|---|
| ISL6605IBZA (Note) | 6605IBZ | -40 to 85 | 8 Ld SOIC (Pb-free) | M8.15 |
| ISL6605IR | 605I | -40 to 85 | 8 Ld 3x3 QFN | L8.3x3 |
| ISL6605IRZ (Note) | 05IZ | -40 to 85 | 8 Ld 3x3 QFN (Pb-free) | L8.3x3 |
| ISL6605IRZA (Note) | 05IZ | -40 to 85 | 8 Ld 3x3 QFN (Pb-free) | L8.3x3 |
| ISL6558EVAL2 | Evaluation Platform (ISL6558IR+ISL6605IR) | | | |

*Add “-T” suffix for tape and reel.

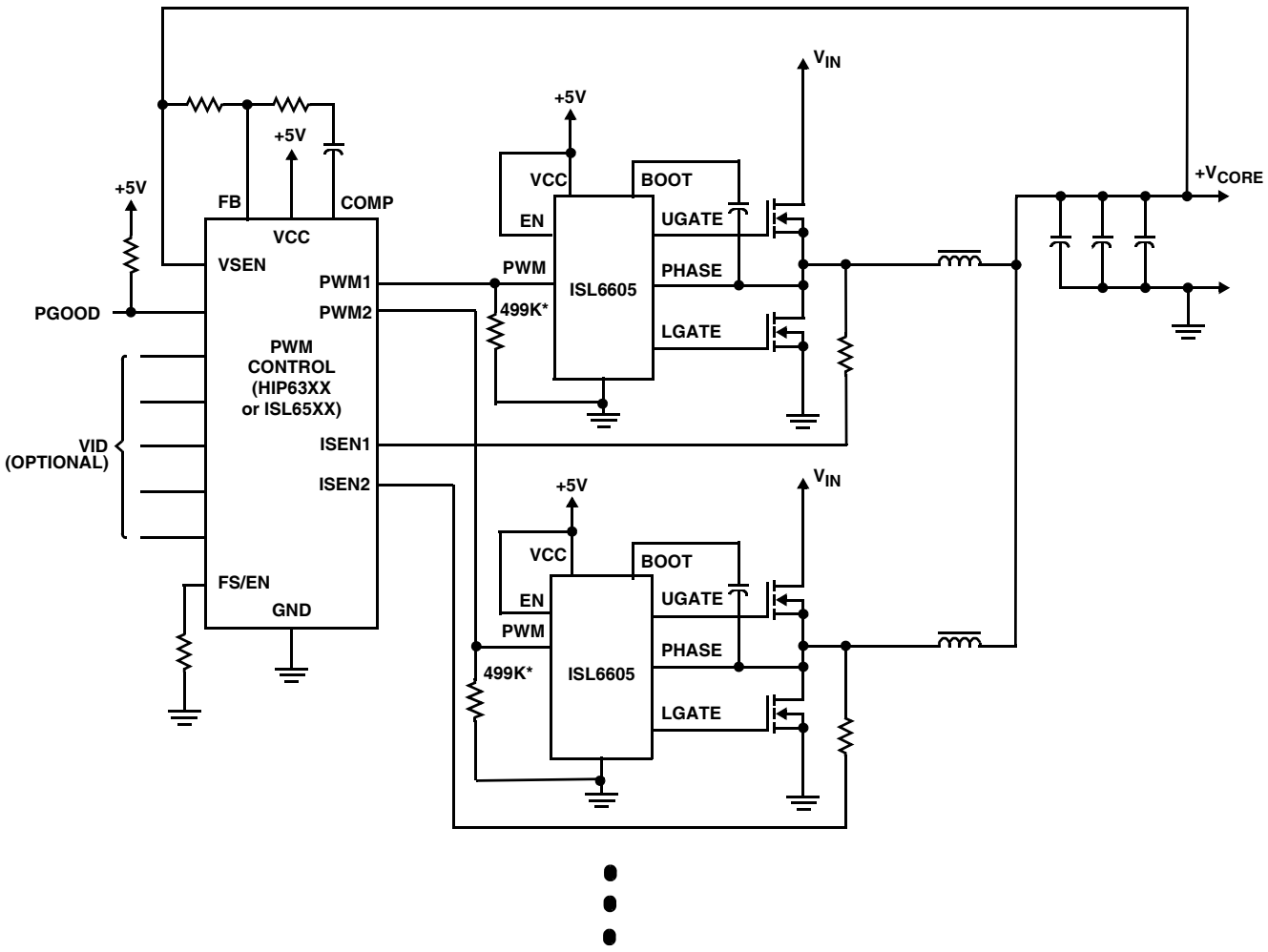
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Block Diagram

**ISL6605**



## *Typical Application - Multi-Phase Converter Using ISL6605 Gate Drivers*




*** 499K IS USED TO PULL DOWN THE PWM INPUT TO PREVENT THE PWM FROM FALSE TRIGGERING UGATE DURING STARTUP.**

## Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.3V to 7V
Input Voltage ($V_{EN}$, $V_{PWM}$) . . . . . -0.3V to VCC + 0.3V
BOOT Voltage ($V_{BOOT}$) . . . . . -0.3V to 22V (DC) or 33V (<200ns)
BOOT To PHASE Voltage ($V_{BOOT-PHASE}$) . . . . . -0.3V to 7V
PHASE Voltage . . . . . GND - 0.3V (DC) to 28V (<200ns)
. . . . . GND - 5V (<100ns Pulse Width, 10µJ) to 28V (<200ns)
UGATE Voltage . . . . . $V_{PHASE}$ - 0.3V (DC) to $V_{BOOT}$+0.3V
. . . . . $V_{PHASE}$ - 4V (<200ns Pulse Width, 20µJ) to $V_{BOOT}$+0.3V
LGATE Voltage . . . . . GND - 0.3V (DC) to $V_{CC}$ + 0.3V
. . . . . GND - 2V (<100ns Pulse Width, 4µJ) to $V_{CC}$ + 0.3V
Ambient Temperature Range. . . . . -40°C to 125°C
ESD Rating
HBM Class 1 JEDEC STD

## Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to 85°C
Maximum Operating Junction Temperature . . . . . 125°C
Supply Voltage, VCC . . . . . 5V ±10%

## Thermal Information

| Thermal Resistance (Notes 1, 2, & 3) | $\theta_{JA}$(°C/W) | $\theta_{JC}$(°C/W) |
|---|---|---|
| SOIC Package (Note 1) . . . . . | 110 | N/A |
| QFN Package (Notes 2, 3). . . . . | 95 | 36 |

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:
1. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.
3. $\theta_{JC}$, "case temperature" location is at the center of the package underside exposed pad. See Tech Brief TB379 for details.

## Electrical Specifications

These specifications apply for $T_A$ = -40°C to 85°C, unless otherwise noted

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **VCC SUPPLY CURRENT** | | | | | | |
| Bias Supply Current | $I_{VCC}$ | EN = LOW, $T_A$ = 0°C to 70°C | - | - | 1.5 | µA |
| | | EN = LOW, $T_A$ = -40°C to 85°C | - | - | 2 | µA |
| Bias Supply Current | $I_{VCC}$ | PWM pin floating, $V_{VCC}$ = 5V | - | 30 | - | µA |
| **PWM INPUT** | | | | | | |
| Input Current | $I_{PWM}$ | $V_{PWM}$ = 5V | - | 250 | - | µA |
| | | $V_{PWM}$ = 0V | - | -250 | - | µA |
| PWM Three-State Rising Threshold | | $V_{VCC}$ = 5V, $T_A$ = 0°C to 70°C | - | - | 1.70 | V |
| | | $V_{VCC}$ = 5V, $T_A$ = -40°C to 85°C | - | - | 1.75 | V |
| PWM Three-State Falling Threshold | | $V_{VCC}$ = 5V | 3.3 | - | - | V |
| Three-State Shutdown Holdoff Time | | $V_{VCC}$ = 5V, temperature = 25°C | - | 420 | - | ns |
| **EN INPUT** | | | | | | |
| EN LOW Threshold | | | 1.0 | - | - | V |
| EN HIGH Threshold | | | - | - | 2.0 | V |
| **SWITCHING TIME** | | | | | | |
| UGATE Rise Time | $t_{RUGATE}$ | $V_{VCC}$ = 5V, 3nF Load | - | 8 | - | ns |
| LGATE Rise Time | $t_{RLGATE}$ | $V_{VCC}$ = 5V, 3nF Load | - | 8 | - | ns |
| UGATE Fall Time | $t_{FUGATE}$ | $V_{VCC}$ = 5V, 3nF Load | - | 8 | - | ns |
| LGATE Fall Time | $t_{FLGATE}$ | $V_{VCC}$ = 5V, 3nF Load | - | 4 | - | ns |
| UGATE Turn-Off Propagation Delay | $t_{PDLUGATE}$ | $V_{VCC}$ = 5V, 3nF Load | - | 8 | - | ns |
| LGATE Turn-Off Propagation Delay | $t_{PDLLGATE}$ | $V_{VCC}$ = 5V, 3nF Load | - | 8 | - | ns |
| **OUTPUT** | | | | | | |
| Upper Drive Source Resistance | $R_{UGATE}$ | 500mA Source Current | - | 1.0 | 2.5 | Ω |
| Upper Driver Source Current (Note 4) | $I_{UGATE}$ | $V_{UGATE-PHASE}$ = 2.5V | - | 2.0 | - | A |
| Upper Drive Sink Resistance | $R_{UGATE}$ | 500mA Sink Current | - | 1.0 | 2.5 | Ω |
| Upper Driver Sink Current (Note 4) | $I_{UGATE}$ | $V_{UGATE-PHASE}$ = 2.5V | - | 2.0 | - | A |
| Lower Drive Source Resistance | $R_{LGATE}$ | 500mA Source Current | - | 1.0 | 2.5 | Ω |
| Lower Driver Source Current (Note 4) | $I_{LGATE}$ | $V_{LGATE}$ = 2.5V | - | 2.0 | - | A |
| Lower Drive Sink Resistance | $R_{LGATE}$ | 500mA Sink Current | - | 0.4 | 1.0 | Ω |
| Lower Driver Sink Current (Note 4) | $I_{LGATE}$ | $V_{LGATE}$ = 2.5V | - | 4.0 | - | A |

NOTE:
4. Guaranteed by design. Not 100% tested in production.

## Functional Pin Description

Note: Pin numbers refer to the SOIC package. Check PINOUT diagrams for QFN pin numbers.

### UGATE (Pin 1)

Upper gate drive output. Connect to gate of high-side power N-Channel MOSFET.

### BOOT (Pin 2)

Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Bootstrap Diode and Capacitor section under DESCRIPTION for guidance in choosing the appropriate capacitor value.

### PWM (Pin 3)

The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation (see the three-state PWM Input section under DESCRIPTION for further details). Connect this pin to the PWM output of the controller.

### GND (Pin 4)

Ground pin. All signals are referenced to this node.

### LGATE (Pin 5)

Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.

### VCC (Pin 6)

Connect this pin to a +5V bias supply. Place a high quality bypass capacitor from this pin to GND.

### EN (Pin 7)

Enable input pin. Connect this pin to HIGH to enable and LOW to disable the IC. When disabled, the IC draws less than 1µA bias current.

### PHASE (Pin 8)

Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin provides a return path for the upper gate driver.

### Thermal Pad (in QFN only)

In the QFN package, the pad underneath the center of the IC is a thermal substrate. The PCB “thermal land” design for this exposed die pad should include thermal vias that drop down and connect to one or more buried copper plane(s). This combination of vias for vertical heat escape and buried planes for heat spreading allows the QFN to achieve its full thermal potential. This pad should be either grounded or floating, and it should not be connected to other nodes. Refer to TB389 for design guidelines.

## Description

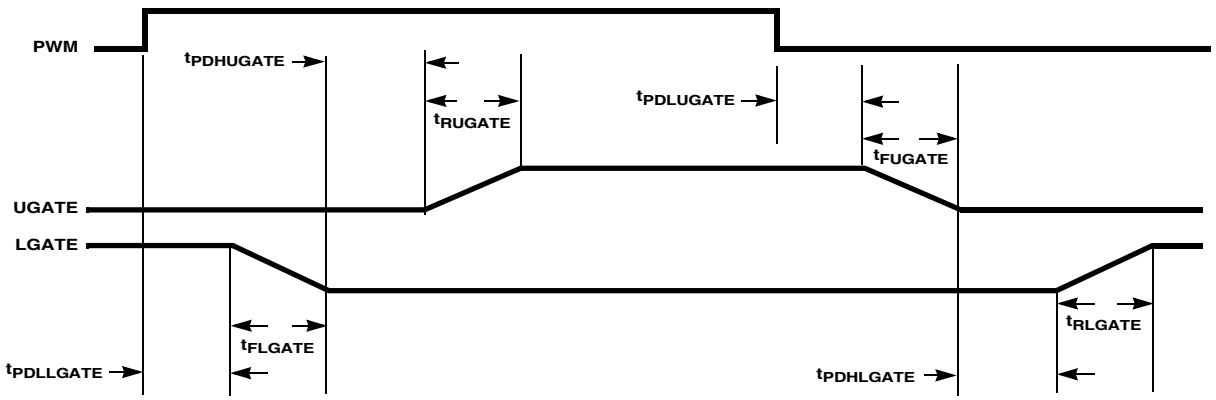
### Operation

Designed for speed, the ISL6605 MOSFET driver controls both high-side and low-side N-Channel FETs from one externally provided PWM signal.

A rising edge on PWM initiates the turn-off of the lower MOSFET (see Timing Diagram). After a short propagation delay [$t_{PDLLGATE}$], the lower gate begins to fall. Typical fall times [$t_{FLGATE}$] are provided in the Electrical Specifications section. Adaptive shoot-through circuitry monitors the LGATE voltage and determines the upper gate delay time [$t_{PDHUGATE}$] based on how quickly the LGATE voltage drops below 1V. This prevents both the lower and upper MOSFETs from conducting simultaneously or shoot-through. Once this delay period is completed the upper gate drive begins to rise [$t_{RUGATE}$] and the upper MOSFET turns on.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [$t_{PDLUGATE}$] is encountered before the upper gate begins to fall [$t_{FUGATE}$]. Again, the adaptive shoot-through circuitry determines the lower gate delay time, $t_{PDHLGATE}$. The upper MOSFET gate voltage is monitored and the lower gate is allowed to rise after the upper MOSFET gate-to-source voltage drops below 1V. The lower gate then rises [$t_{RLGATE}$], turning on the lower MOSFET.

## Timing Diagram



This driver is optimized for voltage regulators with large step down ratio. The lower MOSFET is usually sized much larger compared to the upper MOSFET because the lower MOSFET conducts for a much longer time in a switching period. The lower gate driver is therefore sized much larger to meet this application requirement. The 0.4Ω on-resistance and 4A sink current capability enable the lower gate driver to absorb the current injected to the lower gate through the drain-to-gate capacitor of the lower MOSFET and prevent a shoot through caused by the high dv/dt of the phase node.

### *Three-State PWM Input*

A unique feature of the ISL6605 and other Intersil drivers is the addition of a shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the ELECTRICAL SPECIFICATIONS determine when the lower and upper gates are enabled.

### *Adaptive Shoot-Through Protection*

Both drivers incorporate adaptive shoot-through protection to prevent upper and lower MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.

During turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches a 1V threshold, at which time the UGATE is released to rise. Adaptive shoot-through circuitry monitors the upper MOSFET gate voltage during UGATE turn-off. Once the upper MOSFET gate-to-source voltage has dropped below a threshold of 1V, the LGATE is allowed to rise.

### *Internal Bootstrap Diode*

This driver features an internal bootstrap Schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit.The bootstrap capacitor can be chosen from the following equation:

$$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V_{BOOT}}$$

where $Q_{GATE}$ is the amount of gate charge required to fully charge the gate of the upper MOSFET. The $\Delta V_{BOOT}$ term is defined as the allowable droop in the rail of the upper drive. The above relationship is illustrated in Figure 1.
As an example, suppose an upper MOSFET has a gate charge, $Q_{GATE}$, of 65nC at 5V and also assume the droop in the drive voltage over a PWM cycle is 200mV. One will find that a bootstrap capacitance of at least 0.125µF is required. The next larger standard value capacitance is 0.15µF. A good quality ceramic capacitor is recommended.

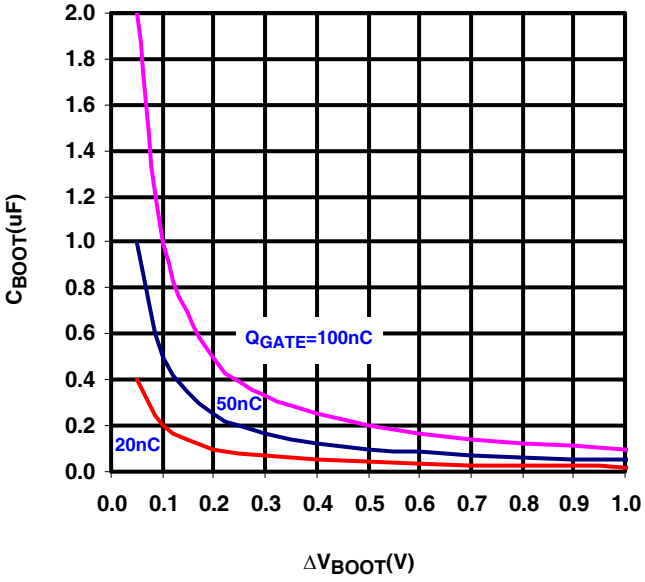



**FIGURE 1. BOOTSTRAP CAPACITANCE vs. BOOT RIPPLE VOLTAGE**

### *Power Dissipation*

Package power dissipation is mainly a function of the switching frequency and total gate charge of the selected MOSFETs. Calculating the power dissipation in the driver for a desired application is critical to ensuring safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of 125°C. The maximum allowable IC power dissipation for the SO-8 package is approximately 800mW. When designing the driver into an application, it is recommended that the following calculation be performed to ensure safe operation at the desired frequency for the selected MOSFETs. The power dissipated by the driver is approximated as below and plotted as in Figure 2.

$$P = f_{sw}(1.5V_U Q_U + V_L Q_L) + I_{DDQ} V_{CC}$$

where $f_{sw}$ is the switching frequency of the PWM signal. $V_U$ and $V_L$ represent the upper and lower gate rail voltage. $Q_U$ and $Q_L$ are the upper and lower gate charge determined by MOSFET selection and any external capacitance added to the gate pins. The $I_{DDQ}$ $V_{CC}$ product is the quiescent power of the driver and is typically negligible.

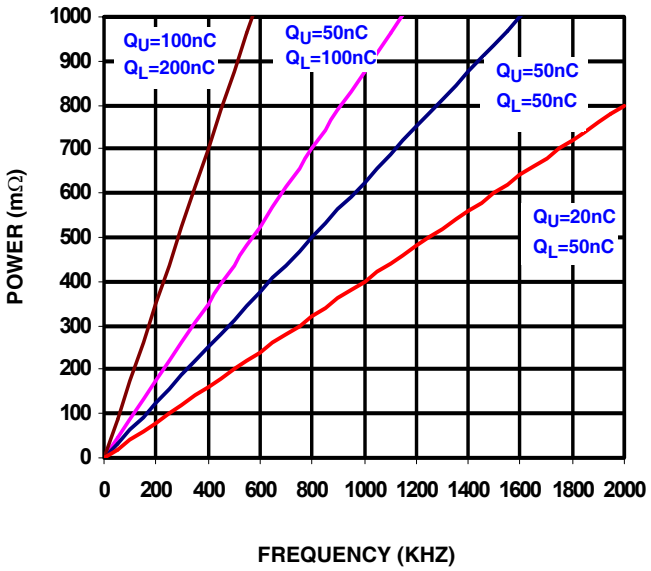



FIGURE 2. POWER DISSIPATION VS. FREQUENCY

## Application Information

### Fault Mode at Repetitive Startups

At a low VCC (<2V), the Thevenin equivalent of the 20k divider at the PWM pin, as shown in the Block Diagram on page 2, is no longer true; very high impedance will be seen from the PWM pin to GND. Junction leakage currents from the VCC to the resistor tub will tend to pull up the PWM input and falsely trigger the UGATE. If the energy stored in the bootstrap capacitor is not completely discharged during the previous power-down period, then the upper MOSFET could be turned on and generate a spike at the output when VCC ramps up. A 499kΩ resistor at the PWM to GND, as shown in Figure 3, helps bleed the leakage currents, thus eliminating the startup spike.

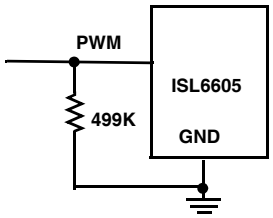



FIGURE 3. 499kΩ RESISTOR

### Layout Considerations and MOSFET Selection

The parasitic inductances of the PCB and the power devices (both upper and lower FETs) generate a negative ringing at the trailing edge of the PHASE node. This negative ringing plus the VCC adds charges to the bootstrap capacitor through the internal bootstrap schottky diode when the PHASE node is low. If the negative spikes are too large, especially at high current applications with a poor layout, the voltage on the bootstrap capacitor could exceed the VCC and the device's maximum rating. The $V_{BOOT-PHASE}$ voltage should be checked at the worst case (maximum VCC and prior to overcurrent trip point), especially for applications with higher than 20A per $D^2PAK$ FET. MOSFETs with low parasitic lead inductances, such as multi-SOURCE leads devices (SO-8 and LFPAK), are recommended.

Careful layout would help reduce the negative ringing peak significantly:

- Tie the SOURCE of the upper FET and the DRAIN of the lower FET as close as possible;
- Use the shortest low-impedance trace between the SOURCE of the lower FET and the power ground;
- Tie the GND of the ISL6605 closely to the SOURCE of the lower FET.

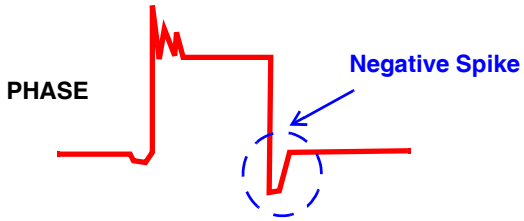



FIGURE 4. TYPICAL PHASE NODE VOLTAGE WAVEFORM

A resistor placement of $R_{BOOT}$, as shown in Figure 5, in the earlier design is recommended; it helps eliminate the overcharge of the BOOT capacitor, in terms of voltage stress across the BOOT to PHASE. When needed, 1 to 2 Ohm $R_{BOOT}$ is sufficient and has little impact on the overall efficiency. However, a design with good layout and using MOSFETs with low parasitic lead inductances, such as multi-SOURCE leads devices (SO-8 and LFPAK), is generally not required such a resistor.

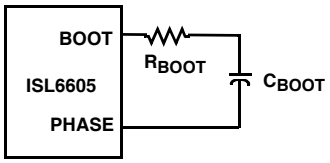
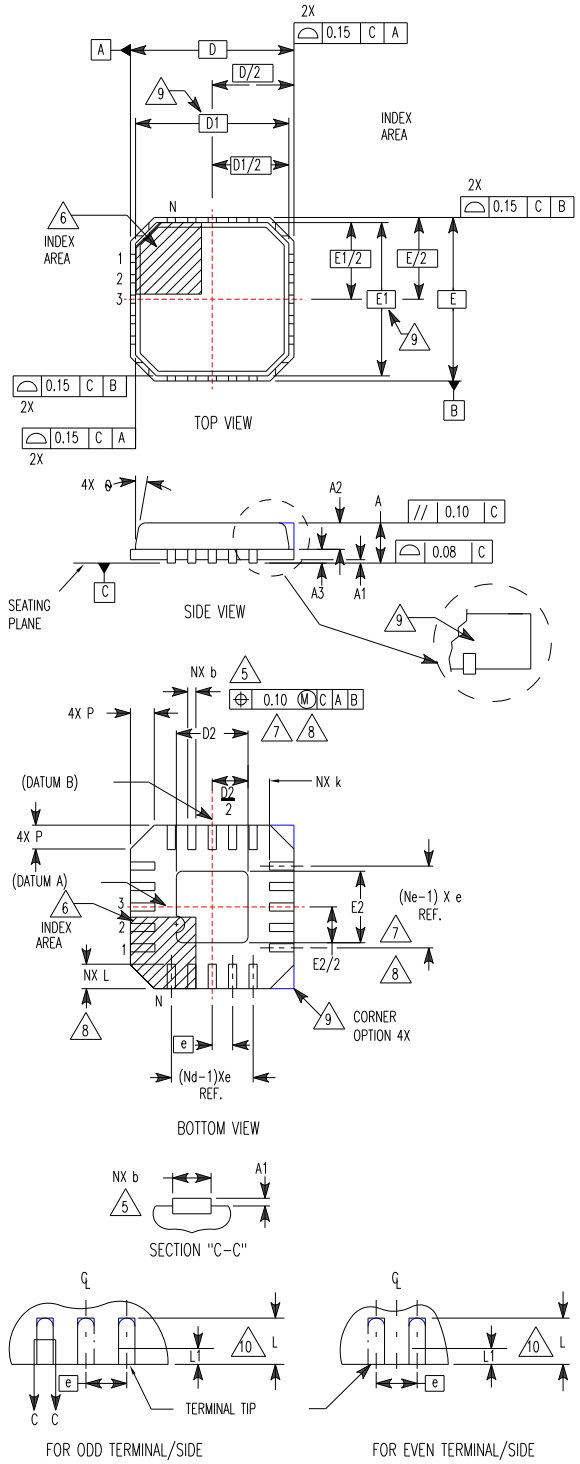



FIGURE 5. RESISTOR PLACEMENT FOR THE $R_{BOOT}$

When placing the QFN part on the board, no vias or trace should be running in between pin numbers 1 and 8 since a small piece of copper is underneath the corner for the orientation. In addition, connecting the thermal pad of the QFN part to the power ground with a via, or placing a low noise copper plane underneath the SOIC part is strongly recommended for high switching frequency, high current applications. This is for heat spreading and allows the part to achieve its full thermal potential.

## *Quad Flat No-Lead Plastic Package (QFN)*
## *Micro Lead Frame Plastic Package (MLFP)*




## L8.3x3

**8 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VEEC ISSUE C)**

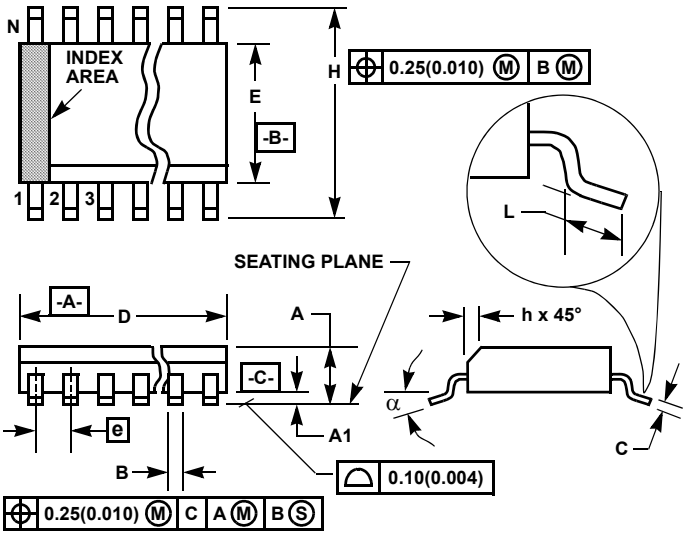
| SYMBOL | MILLIMETERS | | | NOTES |
|---|---|---|---|---|
| | MIN | NOMINAL | MAX | |
| A | 0.80 | 0.90 | 1.00 | - |
| A1 | - | - | 0.05 | - |
| A2 | - | - | 1.00 | 9 |
| A3 | | 0.20 REF | | 9 |
| b | 0.23 | 0.28 | 0.38 | 5, 8 |
| D | | 3.00 BSC | | - |
| D1 | | 2.75 BSC | | 9 |
| D2 | 0.25 | 1.10 | 1.25 | 7, 8 |
| E | | 3.00 BSC | | - |
| E1 | | 2.75 BSC | | 9 |
| E2 | 0.25 | 1.10 | 1.25 | 7, 8 |
| e | | 0.65 BSC | | - |
| k | 0.25 | | - | - |
| L | 0.35 | 0.60 | 0.75 | 8 |
| L1 | - | - | 0.15 | 10 |
| N | | 8 | | 2 |
| Nd | | 2 | | 3 |
| Ne | | 2 | | 3 |
| P | - | - | 0.60 | 9 |
| θ | - | - | 12 | 9 |

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

## *Small Outline Plastic Packages (SOIC)*




NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

**M8.15 (JEDEC MS-012-AA ISSUE C)**
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 8 | | 8 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

Rev. 1 6/05

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